

## Features

- Temperature ranges
  - Industrial: -40 °C to 85 °C
- Very high speed: 55 ns
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62127BV
- Ultra-low active power
  - Typical active current: 0.85 mA at f = 1 MHz
  - Typical active current: 5 mA at f = f<sub>MAX</sub>
- Ultra-low standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- Available in Pb-free 48-ball FBGA and 44-pin TSOP Type II packages

## Functional Description

The CY62127DV30 is a high-performance CMOS static RAM organized as 64K words by 16-bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable

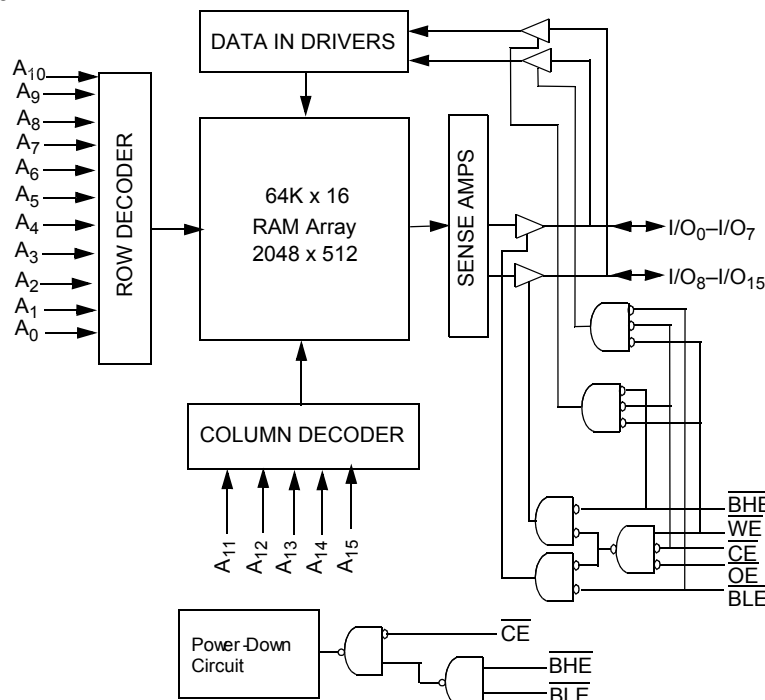
applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH or both BHE and BLE are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), both byte high enable and byte low enable are disabled (BHE, BLE HIGH) or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs LOW. If byte low enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If byte high enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Reading from the device is accomplished by taking chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) LOW while forcing the write enable ( $\overline{WE}$ ) HIGH. If byte low enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If byte high enable (BHE) is LOW, then data from memory appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this datasheet for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram

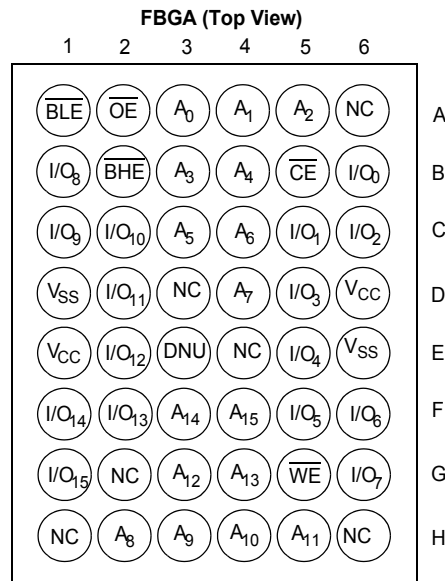
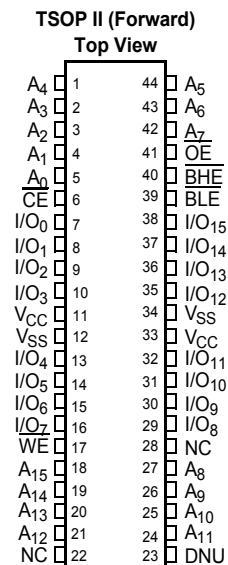


## Contents

<b>Product Portfolio</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>12</b>
<b>Pin Configurations</b> .....	<b>3</b>	Ordering Code Definitions .....	12
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>13</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>14</b>
<b>DC Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>14</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	14
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>15</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>17</b>
<b>Data Retention Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	17
<b>Data Retention Waveform</b> .....	<b>6</b>	Products .....	17
<b>Switching Characteristics</b> .....	<b>7</b>	PSoC@Solutions .....	17
<b>Switching Waveforms</b> .....	<b>8</b>	Cypress Developer Community .....	17
<b>Truth Table</b> .....	<b>11</b>	Technical Support .....	17

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation						
					Operating, I <sub>CC</sub> (mA)					Standby I <sub>SB2</sub> (μA)	
	f = 1 MHz		f = f <sub>MAX</sub>								
	Min	Typ	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Range	Typ <sup>[1]</sup>	Max
CY62127DV30LL	2.2	3.0	3.6	55	0.85	1.5	5	10	Industrial	1.5	4

**Pin Configurations**
**Figure 1. 48-ball FBGA pinout** [2, 3]

**Figure 2. 44-pin TSOP Type II pinout** [2, 3]

**Notes**

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
2. NC pins are not connected to the die. Expansion pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M
3. Pin #23 of TSOP-II and E3 ball of FBGA are DNU, which have to be left floating or tied to V<sub>ss</sub> to ensure proper application.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power applied .....	-55 °C to +125 °C
Supply voltage to ground potential .....	-0.3 V to 3.9 V
DC voltage applied to outputs in high Z State <sup>[4]</sup> .....	-0.3 V to $V_{CC} + 0.3$ V

DC input voltage <sup>[4]</sup> .....	-0.3 V to $V_{CC} + 0.3$ V
Output current into outputs (LOW) .....	20 mA
Static discharge voltage (per MIL-STD-883, method 3015) .....	> 2001 V
Latch-up current .....	> 200 mA

## Operating Range

Range	Ambient Temperature ( $T_A$ )	$V_{CC}$ <sup>[5]</sup>
Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-55			Unit	
			Min	Typ <sup>[6]</sup>	Max		
$V_{OH}$	Output HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1$ mA	2.0	-	-	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0$ mA	2.4	-	-	
$V_{OL}$	Output LOW voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1$ mA	-	-	0.4	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OL} = 2.1$ mA	-	-	0.4	
$V_{IH}$	Input HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$		1.8	-	$V_{CC} + 0.3$	V
		$2.7 \leq V_{CC} \leq 3.6$		2.2	-	$V_{CC} + 0.3$	
$V_{IL}$	Input LOW voltage	$2.2 \leq V_{CC} \leq 2.7$		-0.3	-	0.6	V
		$2.7 \leq V_{CC} \leq 3.6$		-0.3	-	0.8	
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$		-1	-	+1	$\mu$ A
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , Output disabled		-1	-	+1	$\mu$ A
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6$ V, $I_{OUT} = 0$ mA, CMOS level	-	5	10	mA
		$f = 1$ MHz		-	0.85	1.5	
$I_{SB1}$	Automatic CE power-down current – CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{MAX}$ (Address and data only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ , $\overline{BHE}$ and $\overline{BLE}$ )		-	1.5	4	$\mu$ A
$I_{SB2}$	Automatic CE power-down current – CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 3.6$ V		-	1.5	4	$\mu$ A

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.,  $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device operation requires linear ramp of  $V_{CC}$  from 0 V to  $V_{CC(min)}$  and  $V_{CC}$  must be stable at  $V_{CC(min)}$  for 500  $\mu$ s.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.

## Capacitance

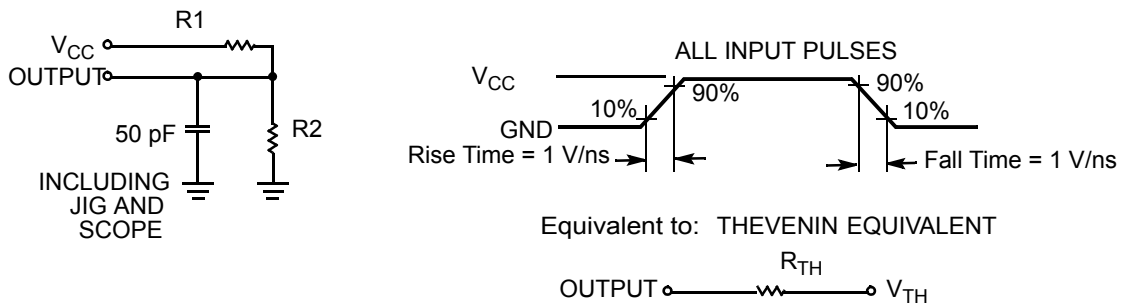
Parameter <sup>[7]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

## Thermal Resistance

Parameter <sup>[8]</sup>	Description	Test Conditions	FBGA	TSOP-II	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	52.02	62.01	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		10.98	22.08	°C/W

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V–2.7 V)	3.0 V (2.7 V–3.6 V)	Unit
R <sub>1</sub>	16600	1103	Ω
R <sub>2</sub>	15400	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

### Note

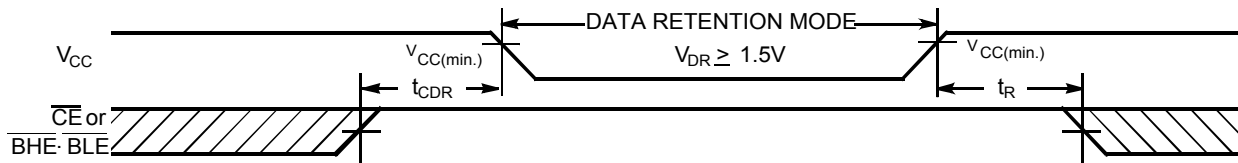
7. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

Parameter	Description	Conditions	Min	Typ <sup>[9]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 1.5\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$		–	3	$\mu\text{A}$
$t_{CDR}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[10]}$	Operation recovery time		55	–	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform <sup>[11]</sup>



### Notes

8. Tested initially and after any design or process changes that may affect these parameters.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
10. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} > 200\text{ }\mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

Parameter <sup>[12]</sup>	Description	CY62127DV30-55		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	55	–	ns
$t_{AA}$	Address to data valid	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[13]</sup>	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[13, 14]</sup>	–	20	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[13]</sup>	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[13, 14]</sup>	–	20	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	–	55	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
$t_{LZBE}$ <sup>[15]</sup>	$\overline{BLE}/\overline{BHE}$ LOW to low Z <sup>[13]</sup>	5	–	ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to high Z <sup>[13, 14]</sup>	–	20	ns
<b>Write Cycle<sup>[16, 17]</sup></b>				
$t_{WC}$	Write cycle time	55	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	40	–	ns
$t_{AW}$	Address setup to write end	40	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	40	–	ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to write end	40	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[13, 14]</sup>	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[13]</sup>	10	–	ns

### Notes

11.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip can be deselected by either disabling the Chip Enable signals or by disabling both byte enable pins.
12. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}$ .
13. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
14.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
15. If both byte enables are toggled together, this value is 10 ns.
16. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
17. The minimum write pulse width for WRITE Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [18, 19]

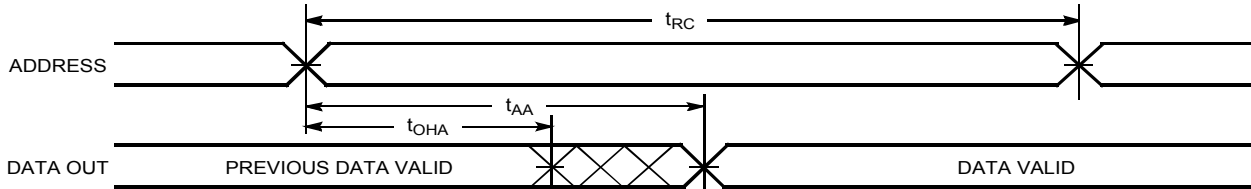
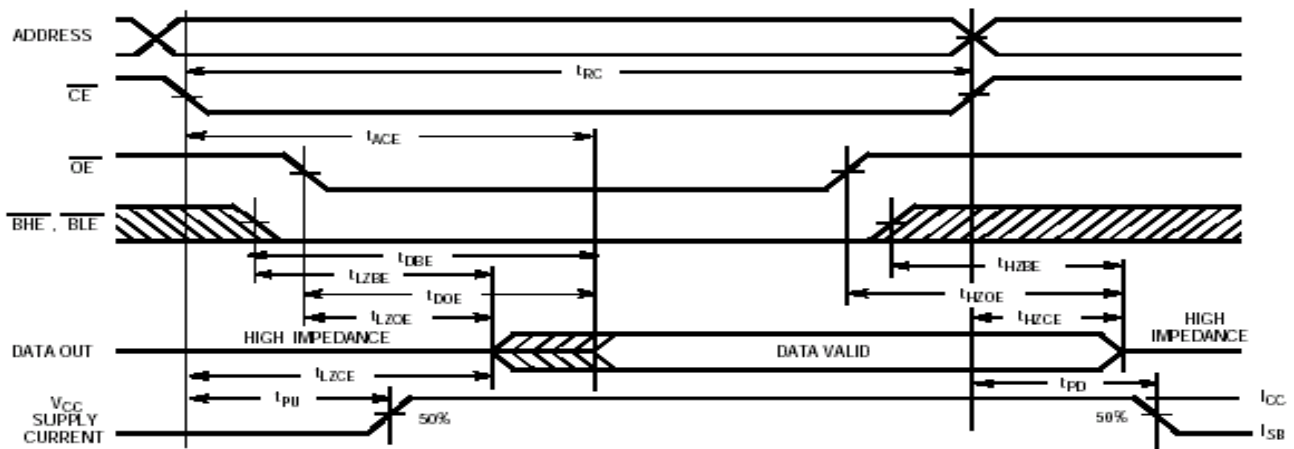


Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [18, 19, 20]



**Notes**

- 18. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  =  $V_{IL}$ .
- 19.  $\overline{WE}$  is HIGH for Read cycle.
- 20. Address valid prior to or coincident with  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.



Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ( $\overline{WE}$  Controlled) [21, 22, 23, 24, 25]

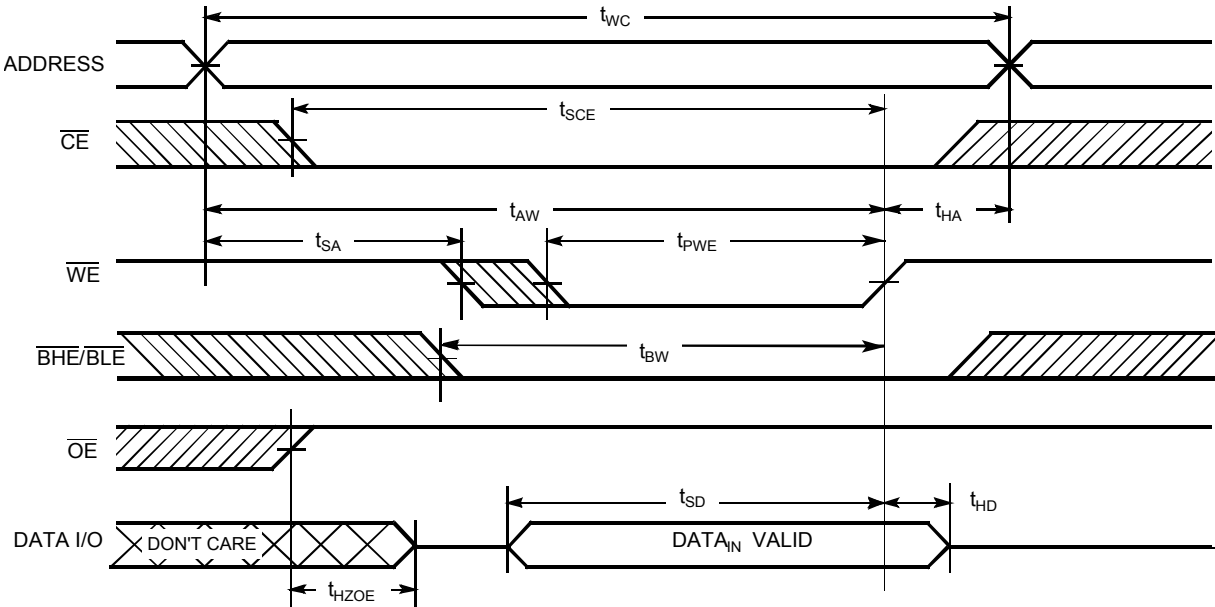
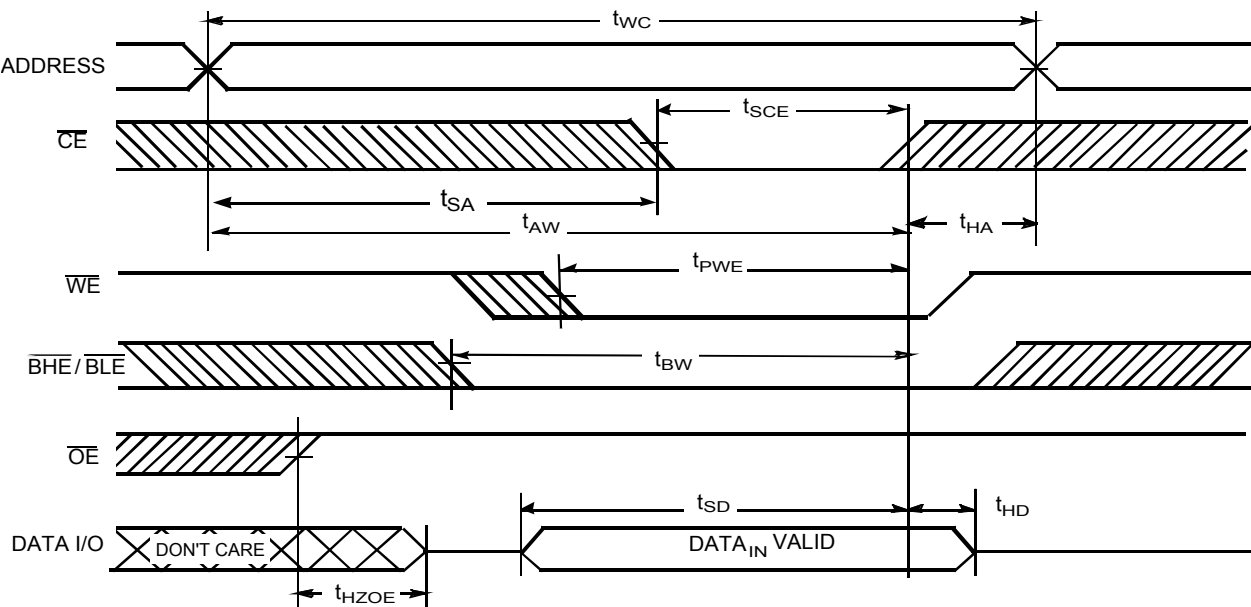


Figure 8. Write Cycle No. 2 ( $\overline{CE}$  Controlled) [21, 22, 23, 24, 25]



Notes

- 21.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
- 22. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 23. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 24. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 25. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [26, 27, 28]

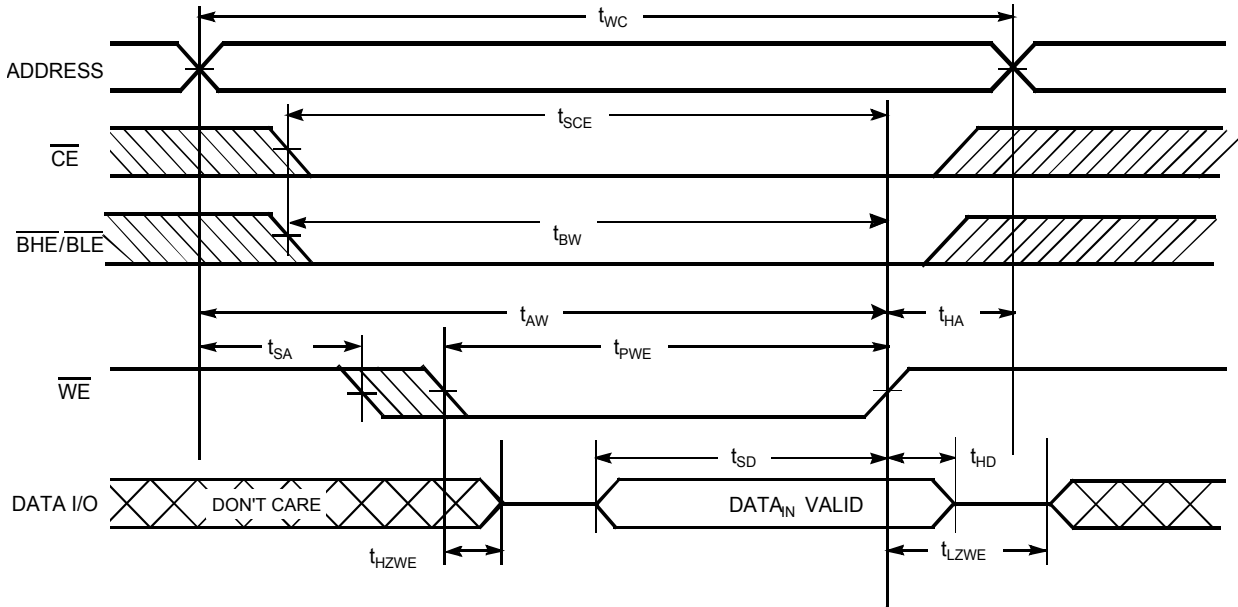
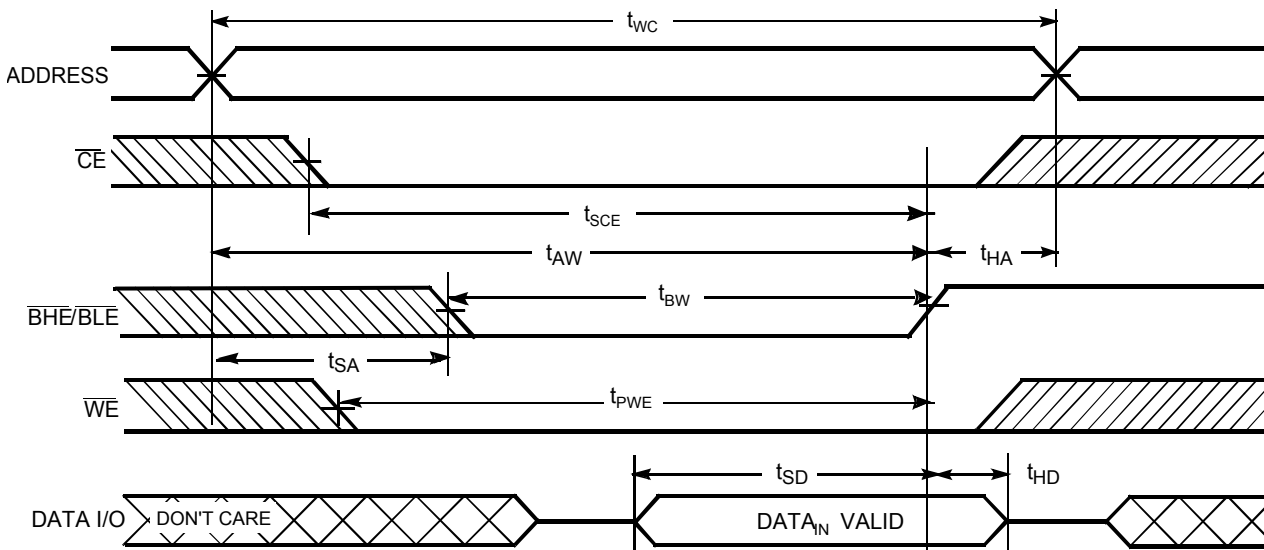


Figure 10. Write Cycle No. 4 ( $\overline{BHE} / \overline{BLE}$  Controlled) [26, 27]



Notes

- 26. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 27. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.
- 28. The minimum write pulse width for WRITE Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Truth Table**

$\overline{\text{CE}}$ [29, 30]	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	X	X	H	H	High Z	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	H	L	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	H	L	H	L	Data Out	High Z	Read Lower Byte Only	Active (I <sub>CC</sub> )
L	H	L	L	H	High Z	Data Out	Read Upper Byte Only	Active (I <sub>CC</sub> )
L	H	H	L	L	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	L	H	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	L	X	L	L	Data in	Data in	Write	Active (I <sub>CC</sub> )
L	L	X	H	L	Data in	High Z	Write Lower Byte Only	Active (I <sub>CC</sub> )
L	L	X	L	H	High Z	Data in	Write Upper Byte Only	Active (I <sub>CC</sub> )

**Notes**

29. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.

30. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

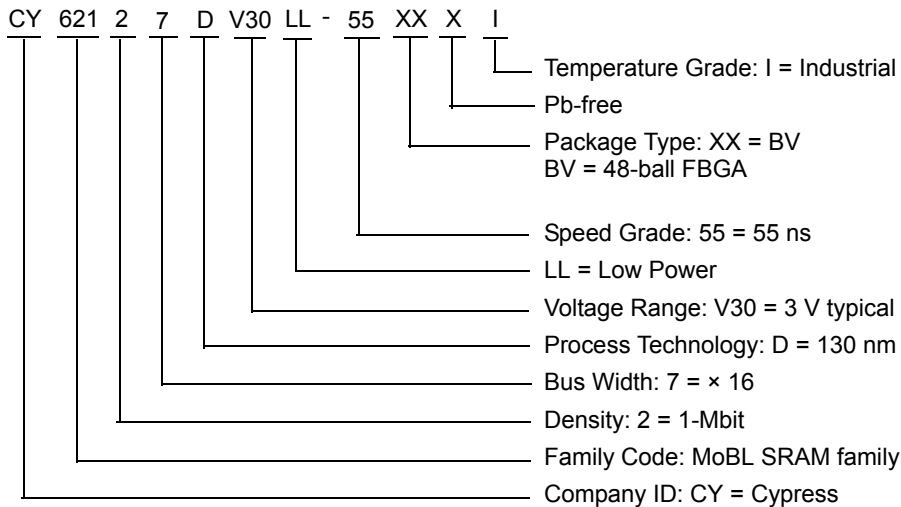
## Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and see product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

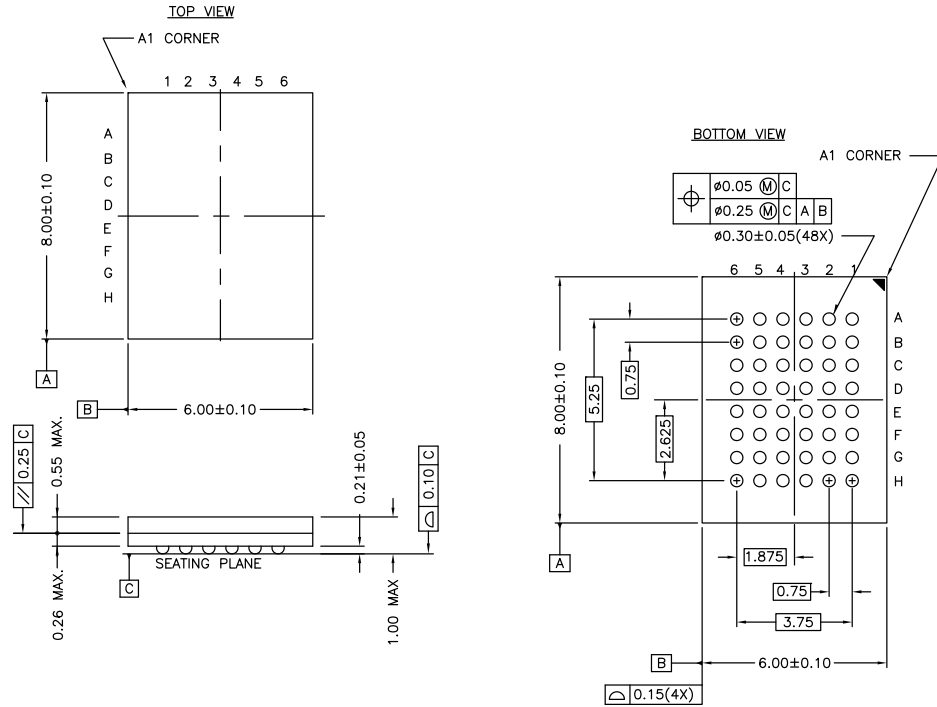
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62127DV30LL-55BVXI	51-85150	48-ball FBGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial

## Ordering Code Definitions



Package Diagrams

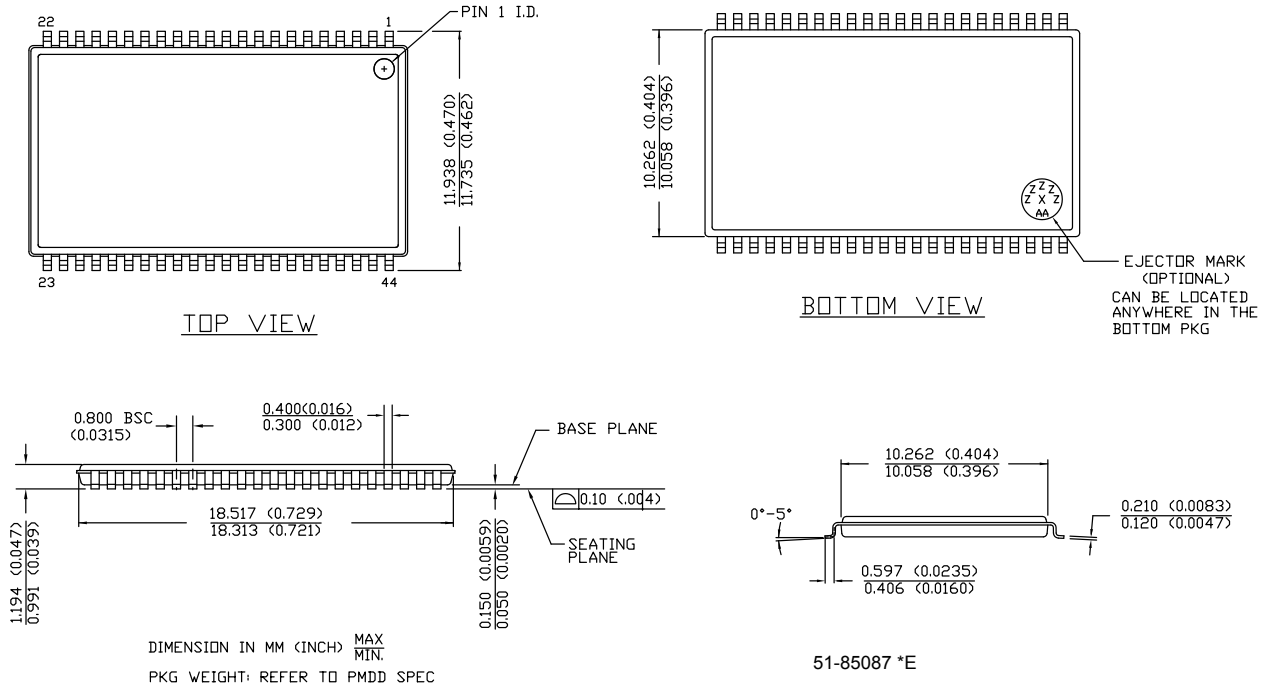
Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:  
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
mA	milliampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62127DV30 MoBL <sup>®</sup> , 1-Mbit (64K × 16) Static RAM Document Number: 38-05229				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	117690	JUI	08/27/02	New data sheet
*A	127311	MPR	06/13/03	<p>Changed status from Advanced to Preliminary.</p> <p>Updated <a href="#">DC Electrical Characteristics</a>:            Changed maximum value of I<sub>SB2</sub> parameter from 4 μA to 5 μA corresponding to Test Condition "L".            Changed maximum value of I<sub>SB2</sub> parameter from 3 μA to 4 μA corresponding to Test Condition "LL".</p> <p>Updated <a href="#">Capacitance</a>:            Changed value of C<sub>IN</sub> parameter from 6 pF to 8 pF.</p> <p>Updated <a href="#">Data Retention Characteristics</a>:            Changed maximum value of I<sub>CCDR</sub> parameter from 1.2 μA to 4 μA corresponding to Test Condition "L".            Changed maximum value of I<sub>CCDR</sub> parameter from 0.8 μA to 3 μA corresponding to Test Condition "LL".</p>
*B	128341	JUI	07/22/03	<p>Changed status from Preliminary to Final.</p> <p>Add 70 ns speed related information in all instances across the document.</p> <p>Updated <a href="#">Ordering Information</a>.</p>
*C	129000	CDY	08/29/03	<p>Updated <a href="#">DC Electrical Characteristics</a>:            Changed typical value of I<sub>CC</sub> parameter corresponding to Test Condition "f = 1 MHz" from 0.5 mA to 0.85 mA.</p>
*D	316039	PCI	See ECN	<p>Added 45 ns speed bin related information in all instances across the document.</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a>:            Added Note "Test condition for the 45-ns part is a load capacitance of 30 pF." and referred the same note in <a href="#">Figure 3</a>.</p> <p>Updated <a href="#">Ordering Information</a>:            Updated part numbers.            Changed name of 44-lead TSOP-II package from Z44 to ZS44 in "Package Name" column.</p>
*E	346982	AJU	See ECN	<p>Added 56-pin QFN package related information in all instances across the document.</p> <p>Updated <a href="#">Ordering Information</a>.</p>
*F	369955	SYT	See ECN	<p>Added Automotive related information in all instances across the document.</p> <p>Updated <a href="#">Features</a>:            Added Temperature Ranges.</p> <p>Updated <a href="#">Ordering Information</a>:            Added Pb-free Automotive parts for 55 ns Speed bin.</p>
*G	457685	NXR	See ECN	<p>Removed 56-pin QFN package related information in all instances across the document.</p> <p>Updated <a href="#">Ordering Information</a>.</p>
*H	470383	NXR	See ECN	<p>Updated <a href="#">Pin Configurations</a>:            Updated <a href="#">Figure 2</a> (Changed pin 23 of TSOP II from NC to DNU).            Updated Note 3.</p>
*I	2897885	RAME / NIKM	03/22/10	<p>Updated <a href="#">Ordering Information</a> (Removed inactive parts).            Updated <a href="#">Package Diagrams</a>.</p>

**Document History Page** *(continued)*

Document Title: CY62127DV30 MoBL®, 1-Mbit (64K × 16) Static RAM				
Document Number: 38-05229				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*J	3010373	AJU	08/20/2010	Updated <a href="#">Features</a> . Updated <a href="#">Product Portfolio</a> . Updated <a href="#">Operating Range</a> . Updated <a href="#">DC Electrical Characteristics</a> . Updated <a href="#">Data Retention Characteristics</a> . Updated <a href="#">Switching Characteristics</a> . Updated <a href="#">Ordering Information</a> and added <a href="#">Ordering Code Definitions</a> . Minor edits. Updated to new template.
*K	3329789	RAME	07/27/11	Updated <a href="#">Functional Description</a> : Removed the Note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <a href="http://www.cypress.com">http://www.cypress.com</a> website." and its reference. Updated to new template.
*L	3393183	RAME	10/03/11	Post to web.
*M	3861271	TAVA	01/08/2013	Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated <a href="#">Package Diagrams</a> : spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E.
*N	4499469	MEMJ	09/11/2014	Updated <a href="#">Switching Characteristics</a> : Added Note 17 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 28 and referred the same note in <a href="#">Figure 9</a> . Updated to new template. Completing Sunset Review.
*O	4576478	MEMJ	11/21/2014	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end.
*P	4920942	VINI	09/15/2015	Updated to new template. Completing Sunset Review.
*Q	5444200	VINI	09/21/2016	Updated <a href="#">Thermal Resistance</a> : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Updated all values of $\theta_{JA}$ and $\theta_{JC}$ parameters. Updated to new template. Completing Sunset Review.
*R	5997966	AESATMP9	12/21/2017	Updated logo and copyright.



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