



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature range
 - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Ultra low standby power
 - Typical standby current: 2.5 μA
 - Maximum standby current: 7 μA (Industrial)
- Ultra low active power
 - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} Features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package
- Byte power down feature

Functional Description

The CY621472E30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly

reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both \overline{BLE} and \overline{BHE} are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when:

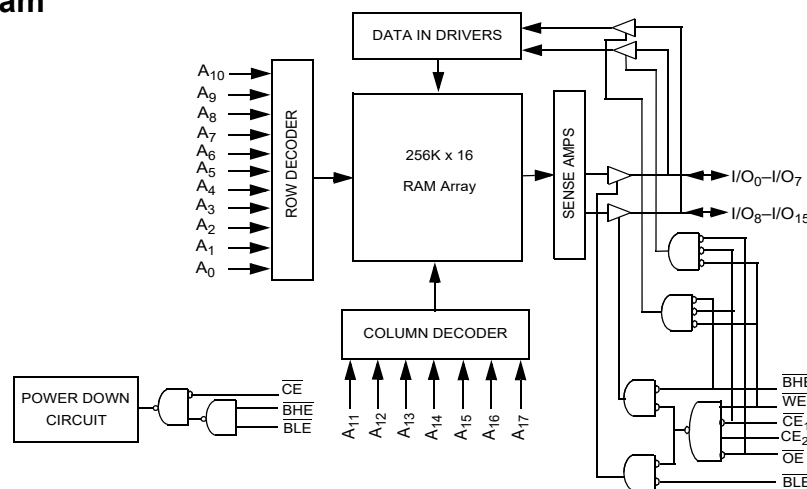
- Deselected (\overline{CE}_1 HIGH or CE_2 LOW)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH)
- Write operation is active (\overline{CE}_1 LOW and CE_2 HIGH and \overline{WE} LOW)

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the [Truth Table on page 11](#) for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Contents

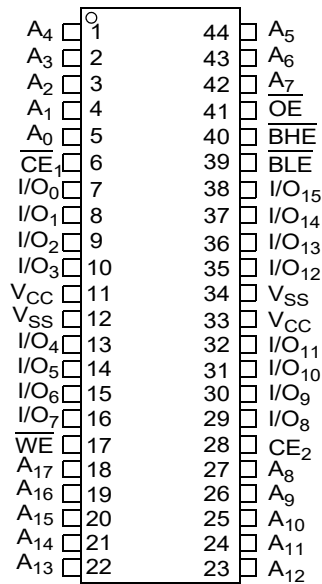
Product Portfolio	3	Ordering Information	12
Pin Configuration	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagram	13
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	16
Data Retention Characteristics	6	Worldwide Sales and Design Support	16
Data Retention Waveform	6	Products	16
Switching Characteristics	7	PSoC® Solutions	16
Switching Waveforms	8	Cypress Developer Community	16
Truth Table	11	Technical Support	16

Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
		f = 1 MHz		f = f _{max}							
		Typ ^[1]	Max	Typ ^[1]		Max	Typ ^[1]	Max			
CY621472E30LL	Industrial	2.2	3.0	3.6	45	3.5	6	15	20	2.5	7

Pin Configuration

Figure 1. 44-pin TSOP II pinout



Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.3 V to +3.9 V ($V_{CCmax} + 0.3$ V)
DC Voltage Applied to Outputs in High Z State ^[2, 3]	-0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

DC input voltage ^[2, 3]	-0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)
Output current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch up current.....	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[4]
CY621472E30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ ^[5]	Max	
V_{OH}	Output HIGH voltage	$I_{OH} = -0.1$ mA	2.0	-	-	V
		$I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70$ V	2.4	-	-	V
V_{OL}	Output LOW voltage	$I_{OL} = 0.1$ mA	-	-	0.4	V
		$I_{OL} = 2.1$ mA, $V_{CC} = 2.70$ V	-	-	0.4	V
V_{IH}	Input HIGH voltage	$V_{CC} = 2.2$ V to 2.7 V	1.8	-	$V_{CC} + 0.3$	V
		$V_{CC} = 2.7$ V to 3.6 V	2.2	-	$V_{CC} + 0.3$	V
V_{IL}	Input LOW voltage	$V_{CC} = 2.2$ V to 2.7 V	-0.3	-	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V	-0.3	-	0.8	V
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	-	+1	μ A
I_{OZ}	Output leakage current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1	-	+1	μ A
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	-	15	20	mA
		$f = 1$ MHz	-	3.5	6	
I_{SB1} ^[6]	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (address and data only), $f = 0$ (\overline{OE} , \overline{BHE} , \overline{BLE} and \overline{WE}), $V_{CC} = 3.60$ V	-	2.5	7	μ A
I_{SB2} ^[6]	Automatic CE Power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = 3.60$ V	-	2.5	7	μ A

Notes

- $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75$ V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μ s ramp time from 0 to $V_{CC(min)}$ and 200 μ s wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
- Chip enables (\overline{CE}_1 and CE_2) need to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

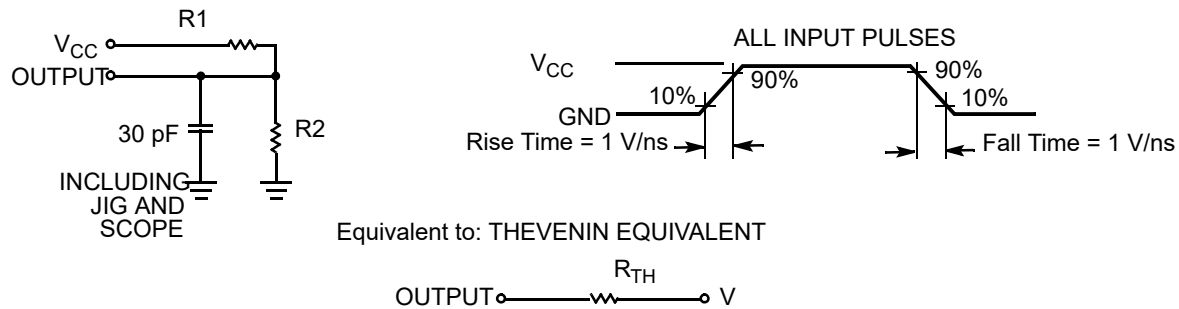
Parameter ^[7]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[7]	Description	Test Conditions	44-pin TSOP II Package	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	°C/W
Θ _{JC}	Thermal resistance (junction to case)		13	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R ₁	16667	1103	Ω
R ₂	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

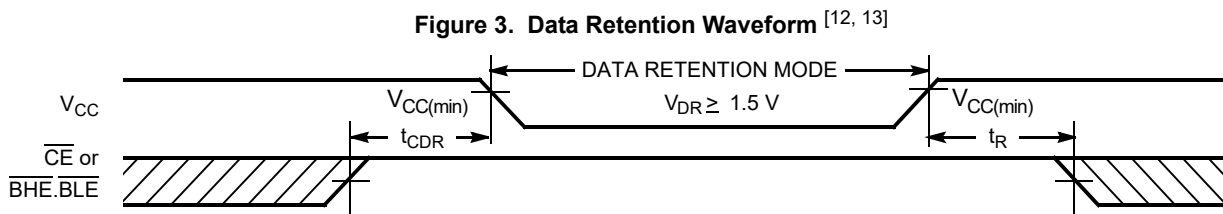
7. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[8]	Max	Unit
V _{DR}	V _{CC} for data retention		1.5	–	–	V
I _{CCDR} ^[9]	Data retention current	V _{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, V _{IN} ≥ V _{CC} – 0.2 V or V _{IN} ≤ 0.2 V	–	3	8.8	μA
t _{CDR} ^[10]	Chip deselect to data retention time		0	–	–	ns
t _R ^[11]	Operation recovery time		45	–	–	ns

Data Retention Waveform



Notes

- 8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- 9. Chip enables (\overline{CE}_1 and CE₂) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- 10. Tested initially and after any design or process changes that may affect these parameters.
- 11. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.
- 12. \overline{CE} refers to the internal logical combination of \overline{CE}_1 and CE₂ such that when \overline{CE}_1 is LOW and CE₂ is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.
- 13. $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Over the Operating Range

Parameter ^[14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE}_1 LOW/ CE_2 HIGH to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[15]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[15, 16]	–	18	ns
t_{LZCE}	\overline{CE}_1 LOW/ CE_2 HIGH to Low Z ^[15]	10	–	ns
t_{HZCE}	\overline{CE}_1 HIGH/ CE_2 LOW to High Z ^[15, 16]	–	18	ns
t_{PU}	\overline{CE}_1 LOW/ CE_2 HIGH to Power-up	0	–	ns
t_{PD}	\overline{CE}_1 HIGH/ CE_2 LOW to Power-down	–	45	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[15, 17]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[15, 16]	–	18	ns
Write Cycle ^[18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE}_1 LOW/ CE_2 HIGH to Write End	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[15, 16]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[15]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 2 on page 5](#).
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. If both byte enables are together, this value is 10 ns.
18. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for WRITE Cycle 4 (\overline{WE} controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

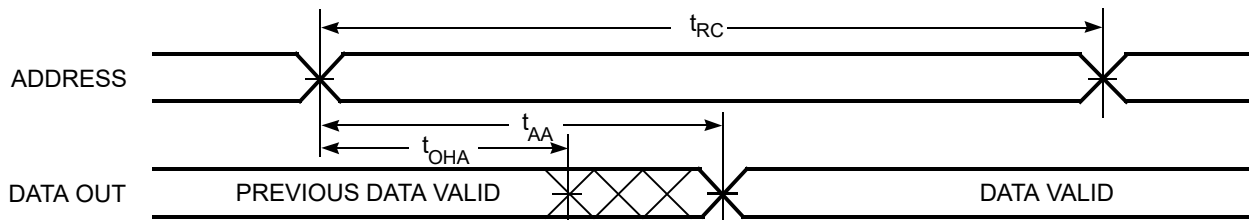
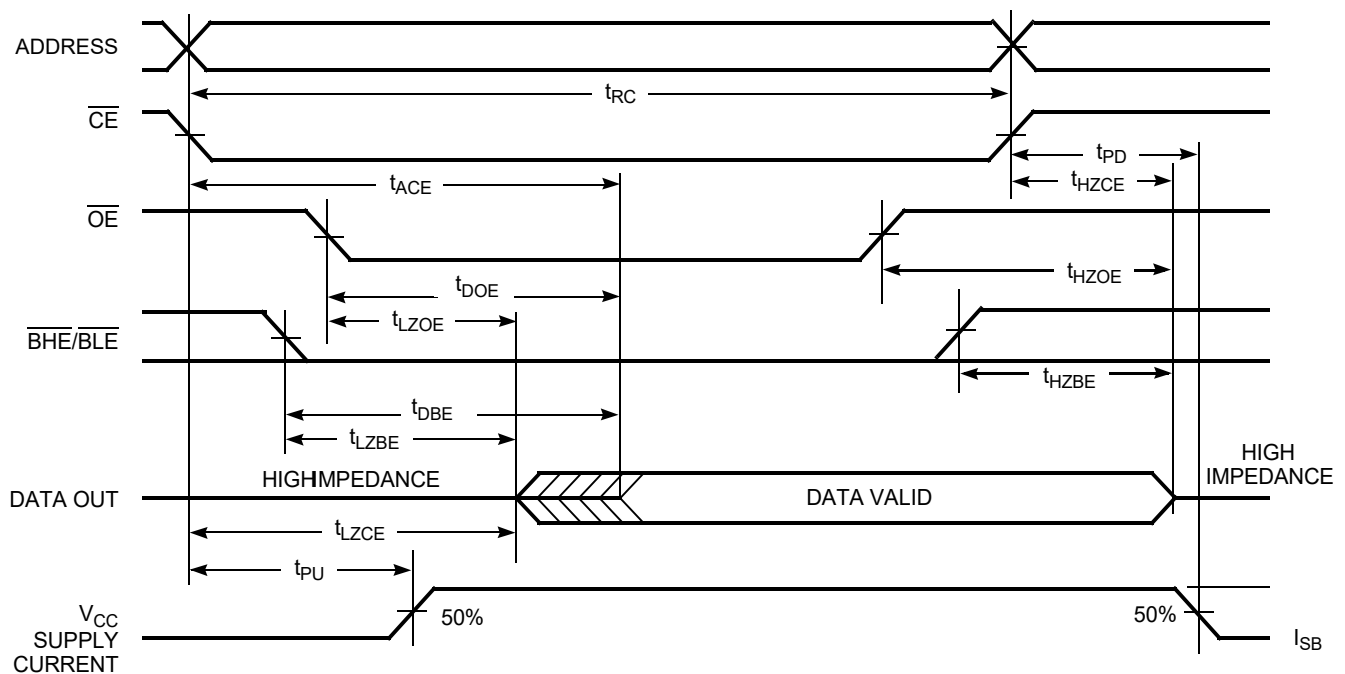


Figure 5. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [21, 22, 23]



Notes

20. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, or both = V_{IL} .

21. $\overline{\text{WE}}$ is HIGH for read cycle.

22. $\overline{\text{CE}}$ refers to the internal logical combination of $\overline{\text{CE}}_1$ and CE_2 such that when $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW. For all other cases $\overline{\text{CE}}$ is HIGH.

23. Address valid before or similar to $\overline{\text{CE}}$ and $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 (\overline{WE} Controlled) [24, 25, 26, 27]

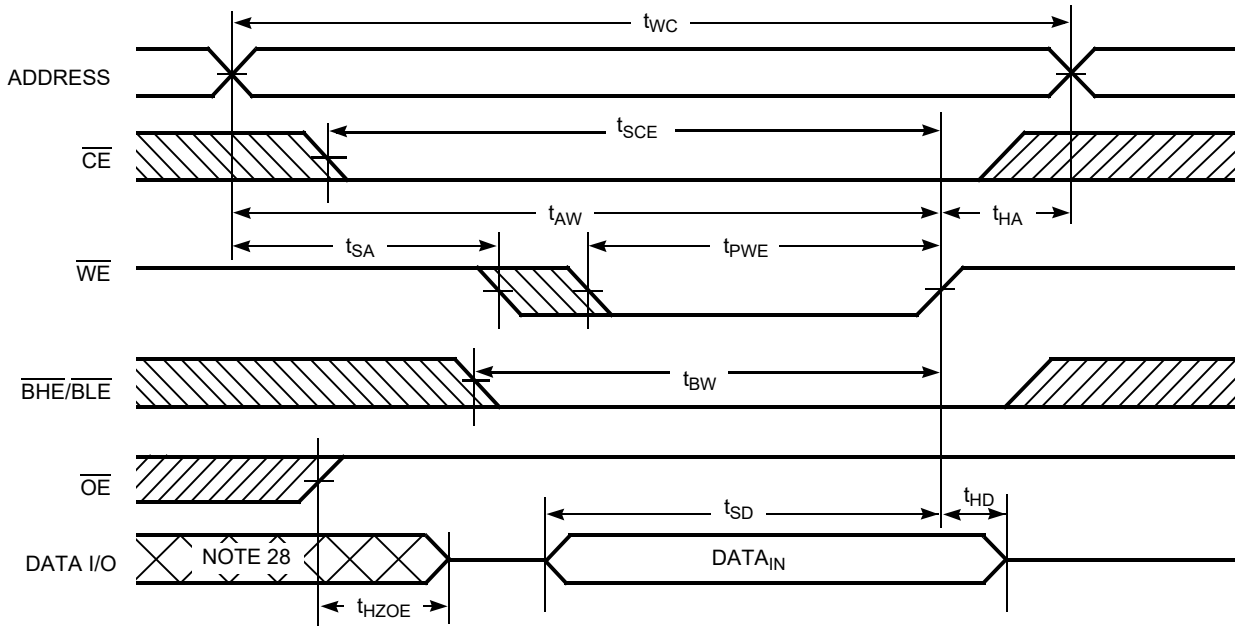
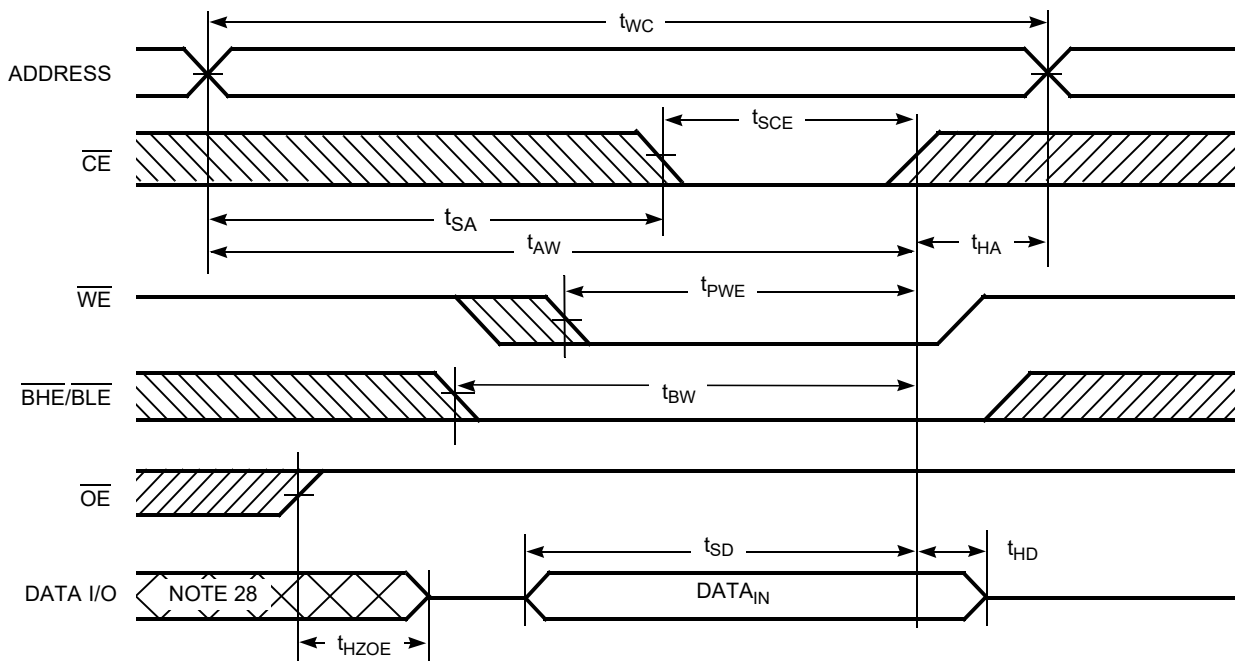


Figure 7. Write Cycle No. 2 (\overline{CE} Controlled) [24, 25, 26, 27]



Notes

- 24. \overline{CE} refers to the internal logical combination of \overline{CE}_1 and CE_2 such that when \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.
- 25. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 27. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [29, 30, 31]

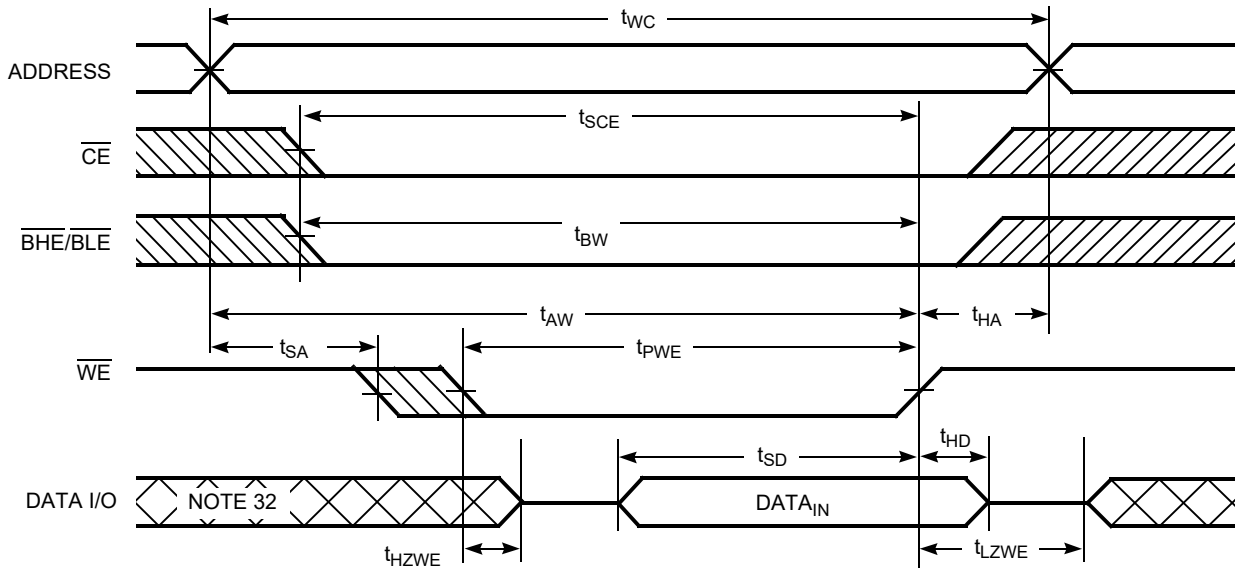
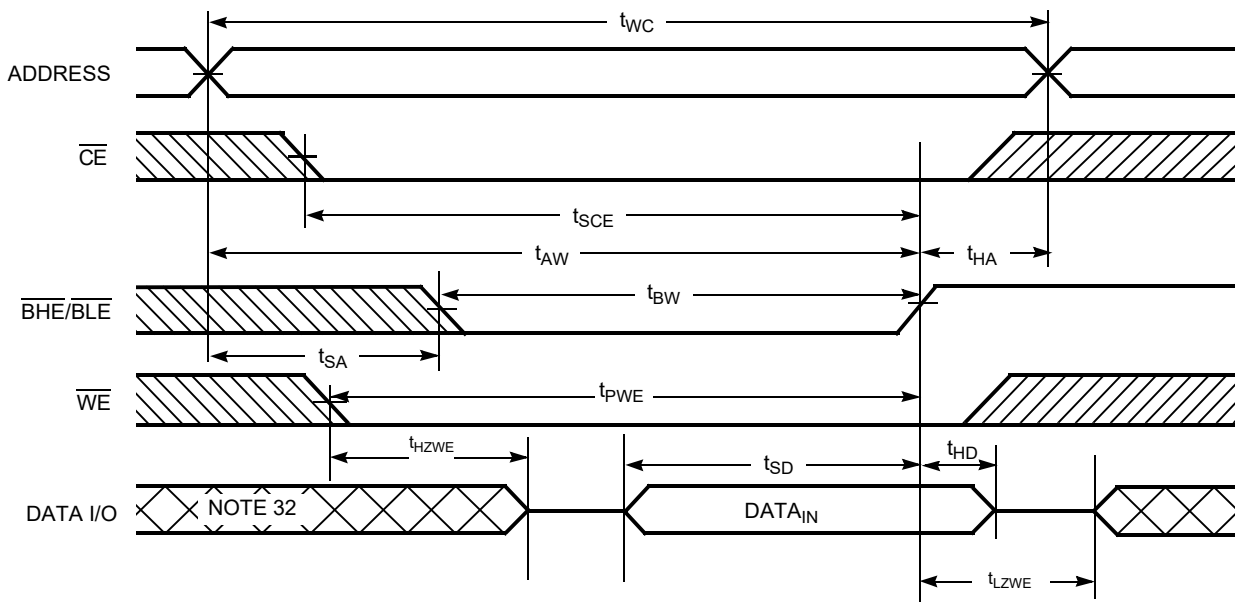


Figure 9. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW) [29, 30]



Notes

- 29. \overline{CE} refers to the internal logical combination of \overline{CE}_1 and CE_2 such that when \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.
- 30. If \overline{CE} goes HIGH simultaneously with $WE = V_{IH}$, the output remains in a high impedance state.
- 31. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD} .
- 32. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	I/Os	Mode	Power
H	X ^[33]	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X ^[33]	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X ^[33]	X ^[33]	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O ₀ –I/O ₁₅)	Read	Active (I_{CC})
L	H	H	L	H	L	Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I_{CC})
L	H	H	L	L	H	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I_{CC})
L	H	L	X	H	L	Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I_{CC})
L	H	L	X	L	H	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I_{CC})

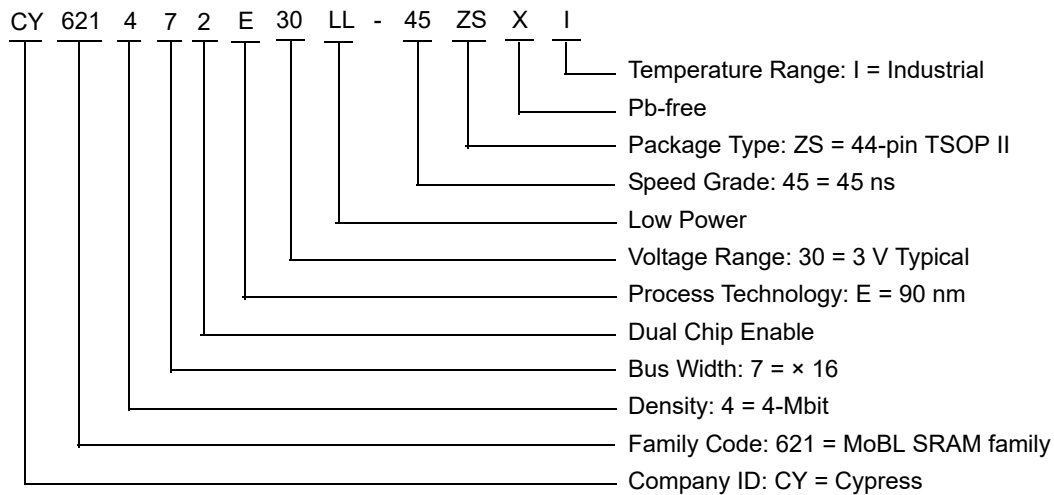
Note

33. The 'X' (Don't care) state for the chip enables (\overline{CE}_1 and CE_2) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

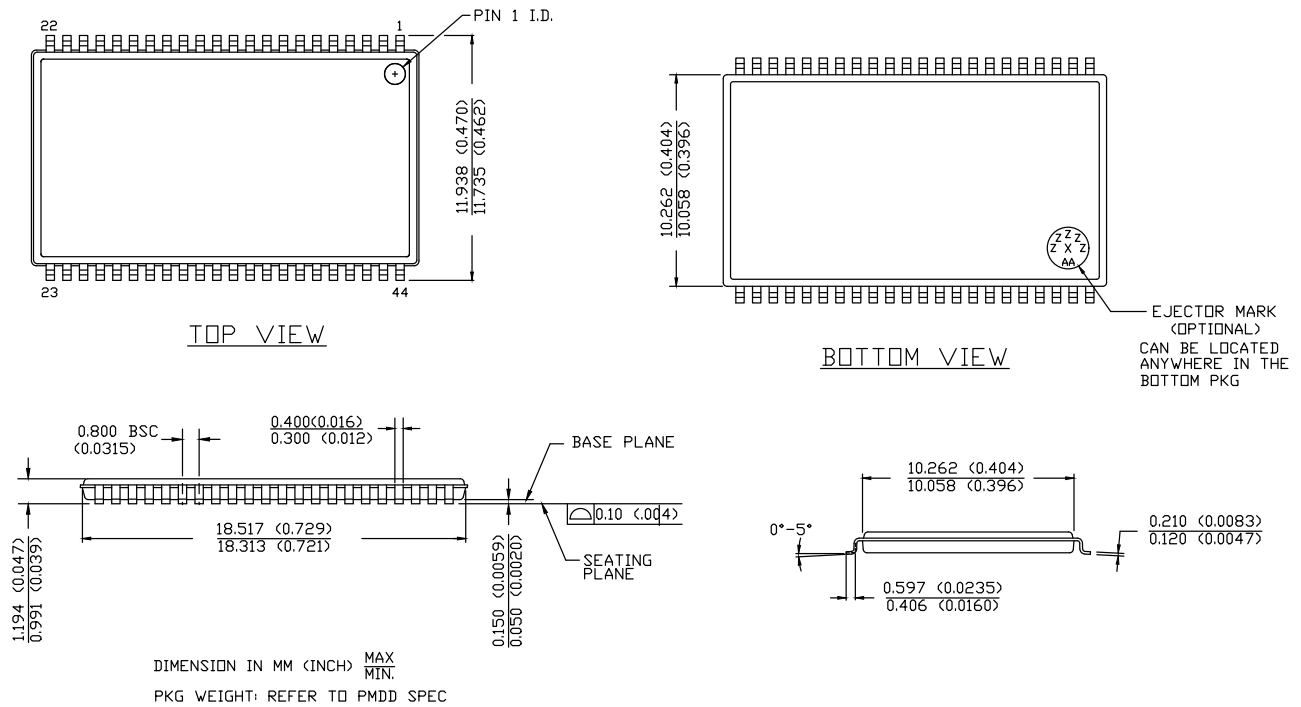
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY621472E30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



51-85087 *F

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY621472E30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-67798			
Rev.	ECN No.	Submission Date	Description of Change
**	3184883	03/01/2011	New data sheet.
*A	3223503	04/15/2011	Updated Truth Table : Removed overline bar for CE ₂ in column heading. Updated to new template.
*B	3261142	05/19/2011	Updated Switching Characteristics : Changed minimum value of t _{LZBE} parameter from 10 ns to 5 ns. Added Ordering Information and Ordering Code Definitions . Added Acronyms and Units of Measure .
*C	3365953	09/08/2011	Changed status from Preliminary to Final. Updated Package Diagram : spec 51-85087 – Changed revision from *C to *D.
*D	3414567	10/20/2011	Replaced CY62147EV30 with CY621472E30 in all instances across the document.
*E	4331825	04/03/2014	Updated Switching Characteristics : Added Note 19 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Note 31 and referred the same note in Figure 8 . Updated Package Diagram : spec 51-85087 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*F	4573121	11/18/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end.
*G	6906316	06/26/2020	Updated Features : Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio : Changed typical value of Operating I _{CC} from 2 mA to 3.5 mA corresponding to "f = 1 MHz". Changed maximum value of Operating I _{CC} from 2.5 mA to 6 mA corresponding to "f = 1 MHz". Changed typical value of Standby, I _{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics : Changed typical value of I _{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I _{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I _{SB1} parameter from 1 µA to 2.5 µA. Changed typical value of I _{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics : Changed typical value of I _{CCDR} parameter from 0.8 µA to 3 µA. Changed maximum value of I _{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagram : spec 51-85087 – Changed revision from *E to *F. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2011–2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [SRAM](#) category:

Click to view products by [Cypress](#) manufacturer:

Other Similar products are found below :

[CY6116A-35DMB](#) [CY7C1049GN-10VXI](#) [CY7C128A-45DMB](#) [GS8161Z36DD-200I](#) [GS88237CB-200I](#) [RMLV0408EGSB-4S2#AA0](#)
[IDT70V5388S166BG](#) [IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#)
[CY7C1353S-100AXC](#) [AS6C8016-55BIN](#) [AS7C164A-15PCN](#) [515712X](#) [IDT71V67603S133BG](#) [IS62WV51216EBLL-45BLI](#)
[IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#) [70V639S10BCG](#) [IS66WVE4M16EALL-70BLI](#) [IS62WV6416DBLL-45BLI](#)
[IS61WV102416DBLL-10TLI](#) [CY7C1381KV33-100AXC](#) [CY7C1381KVE33-133AXI](#) [8602501XA](#) [5962-3829425MUA](#) [5962-3829430MUA](#)
[5962-8855206YA](#) [5962-8866201YA](#) [5962-8866204TA](#) [5962-8866206MA](#) [5962-8866208UA](#) [5962-8872502XA](#) [5962-9062007MXA](#) [5962-](#)
[9161705MXA](#) [70V3579S6BFI](#) [GS882Z18CD-150I](#) [M38510/28902BVA](#) [8413202RA](#) [5962-9161708MYA](#) [5962-8971203XA](#) [5962-](#)
[8971202ZA](#) [5962-8872501LA](#) [5962-8866208YA](#) [5962-8866205YA](#) [5962-8866205UA](#) [5962-8866203YA](#) [5962-8855202YA](#)