

4-Mbit (256K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed: 45 ns/55 ns
- Temperature Ranges
 - Automotive-A: -40 °C to +85 °C
 - Automotive-E: -40 °C to +125 °C
- Ultra-low standby power
 - Typical standby current: 3.5 μA
- Embedded ECC for single-bit error correction^[1, 2]
- Wide voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

CY62147G/CY621472G is high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC. Both devices are offered in single and dual chip enable options and in multiple pin configurations.

Devices with a single chip enable input are accessed by asserting the chip enable (\overline{CE}) input LOW. Dual chip enable devices are accessed by asserting both chip enable inputs – \overline{CE}_1 as low and CE_2 as HIGH.

Data writes are performed by asserting the Write Enable (\overline{WE}) input LOW, while providing the data on I/O₀ through I/O₁₅ and address on A₀ through A₁₇ pins. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) inputs control write operations to the upper and lower bytes of the specified memory location. \overline{BHE} controls I/O₈ through I/O₁₅ and \overline{BLE} controls I/O₀ through I/O₇.

Data reads are performed by asserting the Output Enable (\overline{OE}) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O₀ through I/O₁₅). Byte accesses can be performed by asserting the required byte enable signal (\overline{BHE} or \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O₀ through I/O₁₅) are placed in a HI-Z state when the device is deselected (\overline{CE} HIGH for a single chip enable device and \overline{CE}_1 HIGH/ CE_2 LOW for a dual chip enable device), or control signals are deasserted (\overline{OE} , \overline{BLE} , \overline{BHE}).

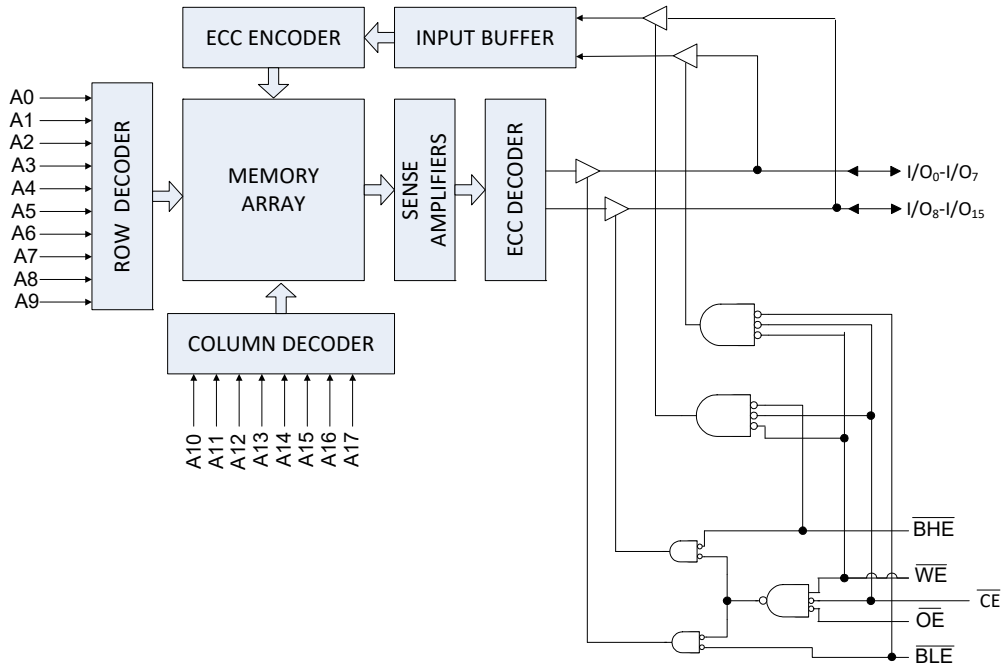
The device also has a unique Byte Power down feature, where, if both the Byte Enables (\overline{BHE} and \overline{BLE}) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enables, thereby saving power.

The logic block diagrams are on page 2.

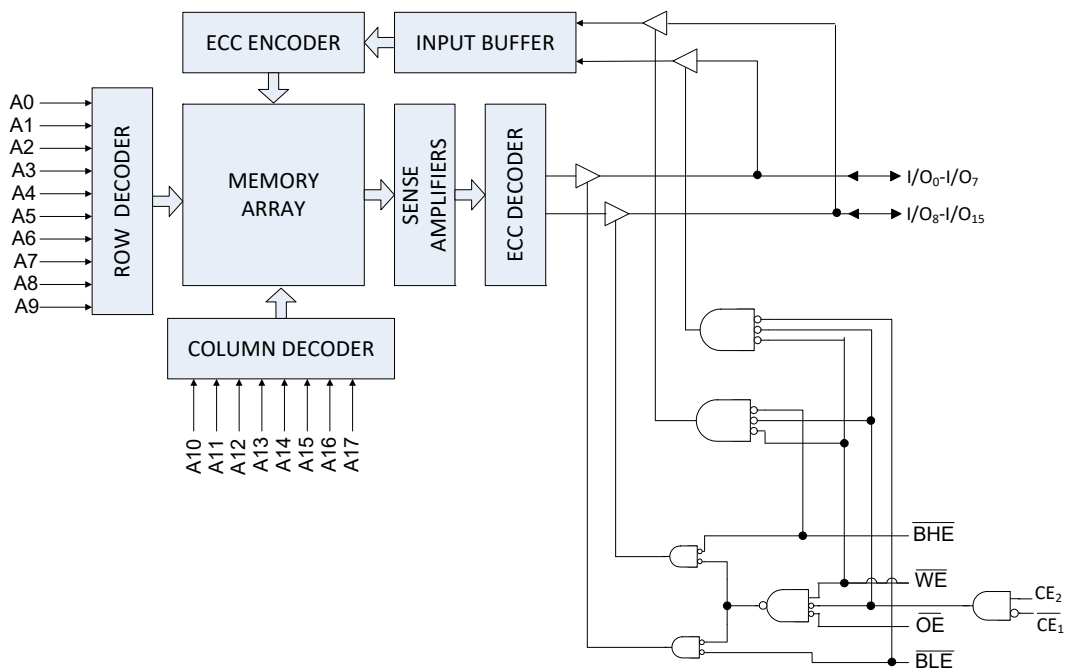
Notes

1. This device does not support automatic write-back on error detection.
2. SER FIT Rate <0.1 FIT/Mb. Refer [AN88889](#) for details.

Logic Block Diagram – CY62147G



Logic Block Diagram – CY621472G



Contents

Pin Configuration – CY62147G	4	Ordering Information	16
Pin Configuration – CY621472G	5	Ordering Code Definitions	16
Product Portfolio	5	Package Diagrams	17
Maximum Ratings	6	Acronyms	18
Operating Range	6	Document Conventions	18
DC Electrical Characteristics	6	Units of Measure	18
Capacitance	8	Document History Page	19
Thermal Resistance	8	Sales, Solutions, and Legal Information	20
AC Test Loads and Waveforms	8	Worldwide Sales and Design Support	20
Data Retention Characteristics	9	Products	20
Data Retention Waveform	9	PSoC@Solutions	20
AC Switching Characteristics	10	Cypress Developer Community	20
Switching Waveforms	11	Technical Support	20
Truth Table – CY62147G/CY621472G	15		

Pin Configuration – CY62147G

Figure 1. 48-ball VFBGA pinout (Single Chip Enable without ERR) – CY62147G [3]

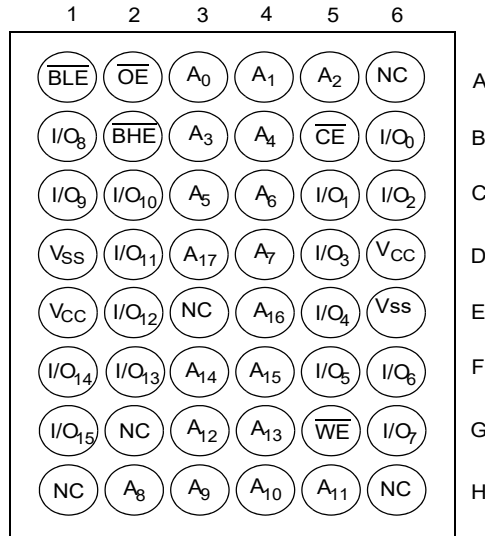
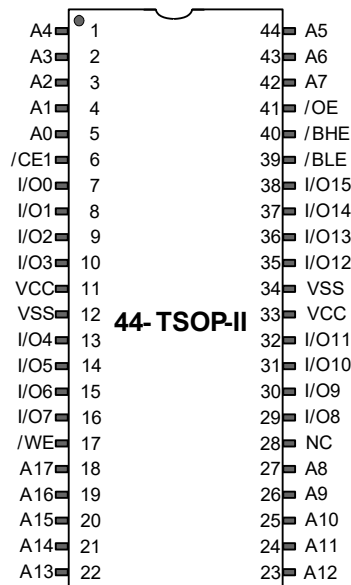


Figure 2. 44-pin TSOP II pinout (Single Chip Enable without ERR) – CY62147G [3]

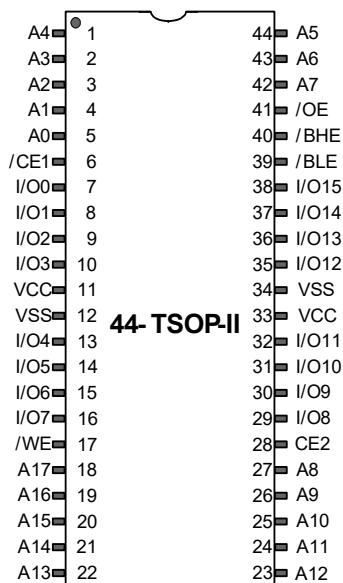


Note

3. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configuration – CY621472G

Figure 3. 44-pin TSOP II pinout (Dual Chip Enable without ERR) – CY621472G



Product Portfolio

Product	Features and Options (see the Pin Configurations section)	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I _{CC} , (mA)		Standby, I _{SB2} (μA)	
					f = f _{max}		Typ ^[4]	Max
CY62147G30/ CY621472G30	Single or dual Chip Enables	Automotive-A	2.2 V–3.6 V	45	15	20	3.5	8.7
		Automotive-E		55	15	24	–	35

Note

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to + 150 °C
Ambient temperature with power applied	-55 °C to + 125 °C
Supply voltage to ground potential ^[5]	-0.3 V to V _{CC} + 0.3 V
DC voltage applied to outputs in HI-Z state ^[5]	-0.3 V to V _{CC} + 0.3 V

DC input voltage ^[5]	-0.3 V to V _{CC} + 0.3 V
Output current into outputs (in low state)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	>2001 V
Latch-up current	>140 mA

Operating Range

Grade	Ambient Temperature	V _{CC}
Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V
Automotive-E	-40 °C to +125 °C	

DC Electrical Characteristics

Over the operating range

Parameter	Description		Test Conditions	45 ns (Automotive-A)			55 ns (Automotive-E)			Unit	
				Min	Typ	Max	Min	Typ	Max		
V _{OH}	Output HIGH voltage	2.2 V to 2.7 V	V _{CC} = Min, I _{OH} = -0.1 mA	2	-	-	2	-	-	V	
		2.7 V to 3.6 V	V _{CC} = Min, I _{OH} = -1.0 mA	2.4	-	-	2.4	-	-		
V _{OL}	Output LOW voltage	2.2 V to 2.7 V	V _{CC} = Min, I _{OL} = 0.1 mA	-	-	0.4	-	-	0.4	V	
		2.7 V to 3.6 V	V _{CC} = Min, I _{OL} = 2.1 mA	-	-	0.4	-	-	0.4		
V _{IH}	Input HIGH voltage	2.2 V to 2.7 V	-	1.8	-	V _{CC} + 0.3 ^[5]	2	-	V _{CC} + 0.3 ^[5]	V	
		2.7 V to 3.6 V	-	2	-	V _{CC} + 0.3 ^[5]	2	-	V _{CC} + 0.3 ^[5]		
V _{IL}	Input LOW voltage	2.2 V to 2.7 V	-	-0.3 ^[5]	-	0.6	-0.3 ^[5]	-	0.6	V	
		2.7 V to 3.6 V	-	-0.3 ^[5]	-	0.8	-0.3 ^[5]	-	0.8		
I _{IX}	Input leakage current		GND ≤ V _{IN} ≤ V _{CC}	-1	-	+1	-5	-	+5	μA	
I _{OZ}	Output leakage current		GND ≤ V _{OUT} ≤ V _{CC} , Output disabled	-1	-	+1	-5	-	+5	μA	
I _{CC}	V _{CC} operating supply current		Max V _{CC} , I _{OUT} = 0 mA, CMOS levels	f = f _{MAX}	-	15	20	-	15	24	mA
				f = 1 MHz	-	3.5	6	-	3.5	10	

Note

5. V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 20 ns.

DC Electrical Characteristics (continued)

Over the operating range

Parameter	Description	Test Conditions	45 ns (Automotive-A)			55 ns (Automotive-E)			Unit
			Min	Typ	Max	Min	Typ	Max	
$I_{SB1}^{[6]}$	Automatic power down current – CMOS inputs; $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$, $f = f_{max}$ (address and data only), $f = 0$ (\overline{OE} , and \overline{WE}), Max V_{CC}	–	3.5	8.7	–	–	35	μA
$I_{SB2}^{[6]}$	Automatic power down current – CMOS inputs $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$, $f = 0$, Max V_{CC}	–	3.5	8.7	–	–	35	μA

Note

 6. Chip enables (\overline{CE}_1 and CE_2) must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

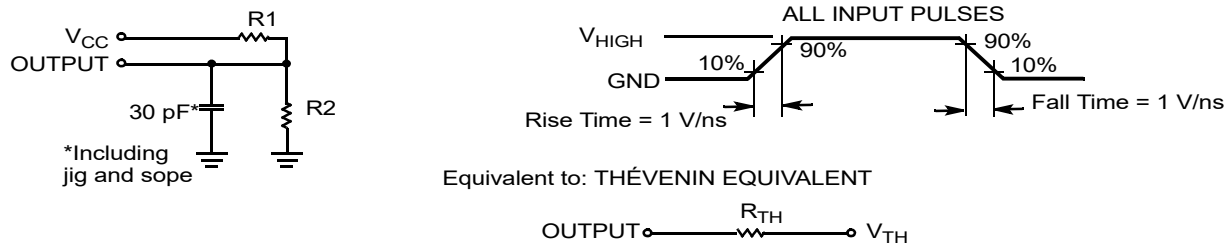
Parameter ^[7]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[7]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.17	66.82	°C/W
Θ _{JC}	Thermal resistance (junction to case)		14.90	15.97	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms ^[8]



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R ₁	13500	16667	1103	1800	Ω
R ₂	10800	15385	1554	990	Ω
R _{TH}	6000	8000	645	639	Ω
V _{TH}	0.80	1.20	1.75	1.77	V

Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full-device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.

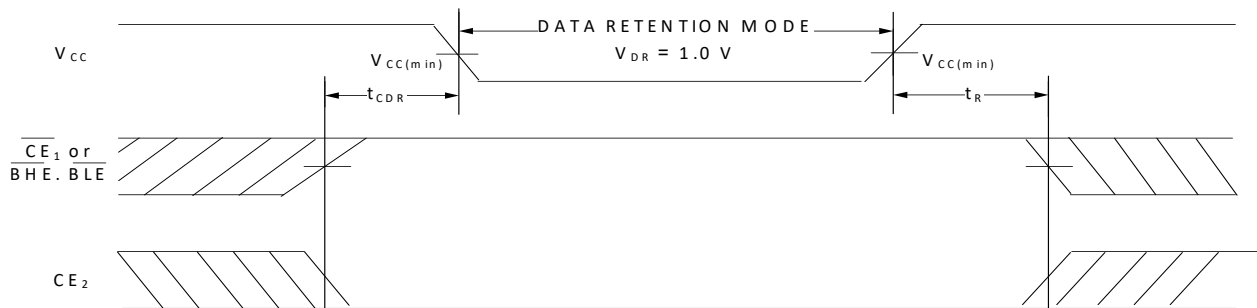
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	(Automotive-A)			(Automotive-E)			Unit
			Min	Typ ^[9]	Max	Min	Typ ^[9]	Max	
V_{DR}	V_{CC} for data retention		1	–	–	1	–	–	V
$I_{CCDR}^{[10, 11]}$	Data retention current	$V_{CC} = 1.2\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	13	–	–	50	μA
$t_{CDR}^{[12]}$	Chip deselect to data retention time		0	–	–	0	–	–	ns
$t_R^{[12, 13]}$	Operation recovery time		45	–	–	55	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform ^[14]



Notes

9. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8\text{ V}$ (for V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3\text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5\text{ V}$ (for V_{CC} range of 4.5 V–5.5 V), $T_A = 25\text{ }^\circ\text{C}$.
10. Chip enables (\overline{CE}_1 and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. I_{CCDR} is guaranteed only after the device is first powered up to $V_{CC(\text{min})}$ and then brought down to V_{DR} .
12. These parameters are guaranteed by design.
13. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

AC Switching Characteristics

Parameter ^[15]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid	–	45	–	55	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	–	25	ns
t_{LZOE}	\overline{OE} LOW to Low impedance ^[16, 17]	5	–	5	–	ns
t_{HZOE}	\overline{OE} HIGH to HI-Z ^[16, 17, 18]	–	18	–	18	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low impedance ^[16, 17]	10	–	10	–	ns
t_{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to HI-Z ^[16, 17, 18]	–	18	–	18	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to power-up ^[17]	0	–	0	–	ns
t_{PD}	\overline{CE}_1 HIGH and CE_2 LOW to power-down ^[17]	–	45	–	55	ns
t_{DBE}	$\overline{BLE} / \overline{BHE}$ LOW to data valid	–	45	–	55	ns
t_{LZBE}	$\overline{BLE} / \overline{BHE}$ LOW to Low impedance ^[16, 17]	5	–	5	–	ns
t_{HZBE}	$\overline{BLE} / \overline{BHE}$ HIGH to HI-Z ^[16, 17, 18]	–	18	–	18	ns
Write Cycle ^[19, 20]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE} / \overline{BHE}$ LOW to write end	35	–	45	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	\overline{WE} LOW to HI-Z ^[16, 17, 18]	–	18	–	20	ns
t_{LZWE}	\overline{WE} HIGH to Low impedance ^[16, 17]	10	–	10	–	ns

Notes

15. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
17. These parameters are guaranteed by design.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} , or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
20. The minimum pulse width in Write Cycle No 3 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 6. Read Cycle No. 1 of CY62147G/CY621472G (Address Transition Controlled) [21, 22]

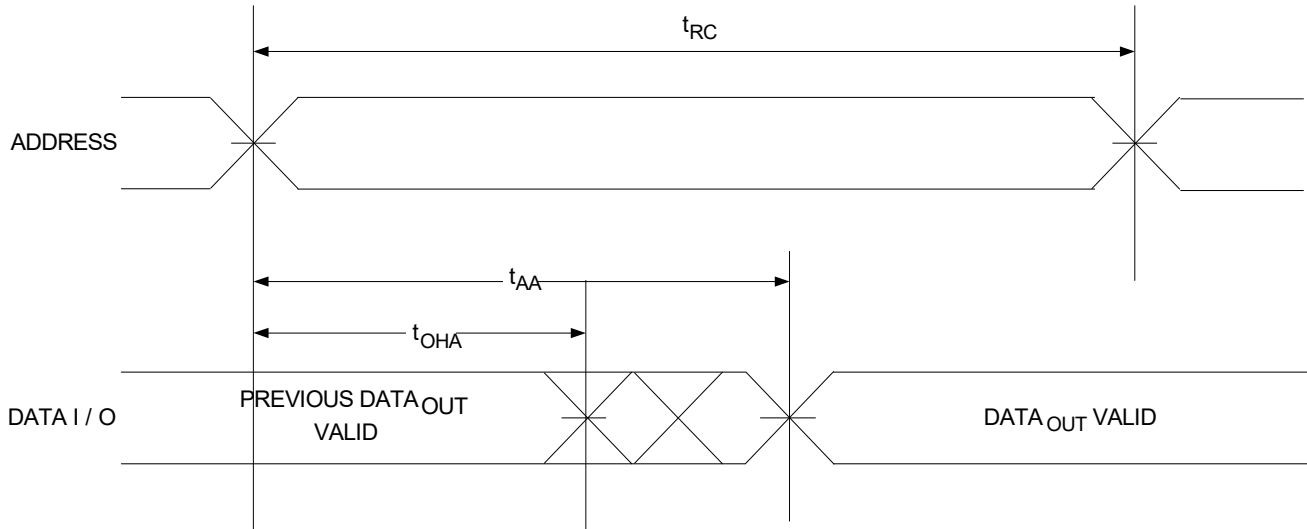
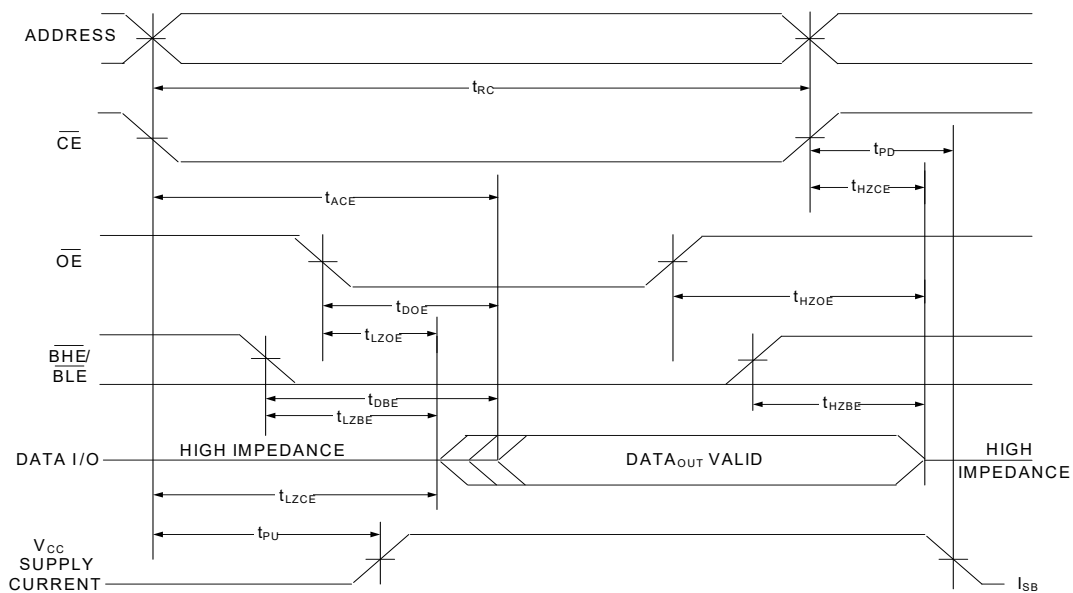


Figure 7. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [22, 23, 24]

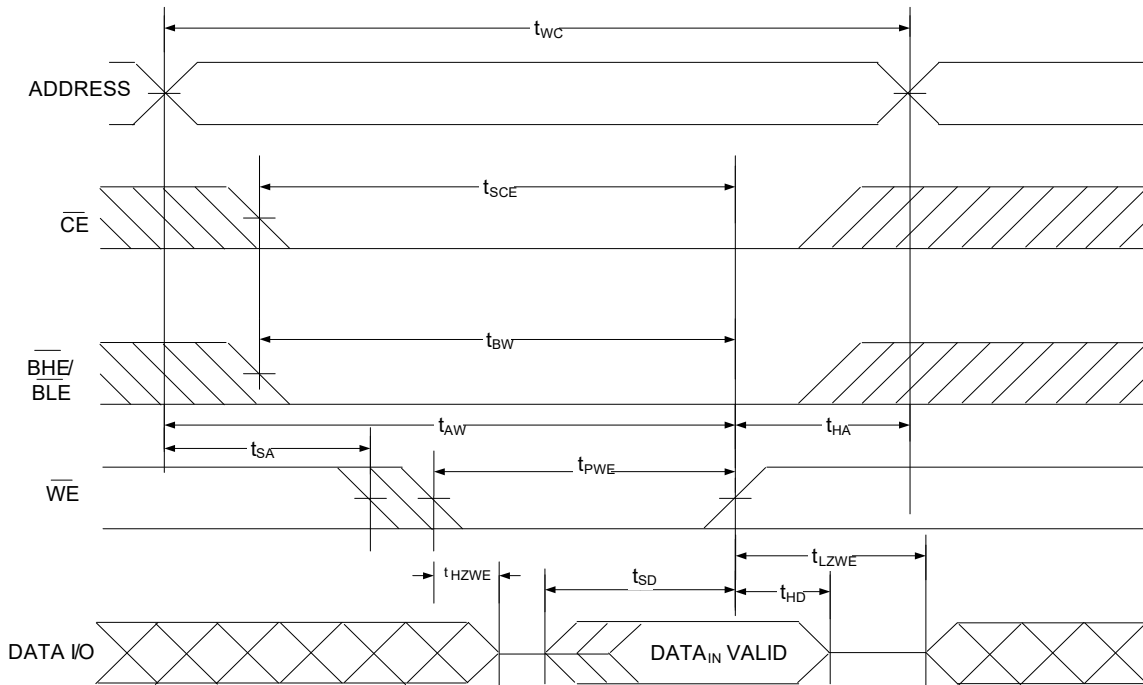


Notes

21. The device is continuously selected. $\overline{\text{OE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} .
22. $\overline{\text{WE}}$ is HIGH for Read cycle.
23. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
24. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.

Switching Waveforms (continued)

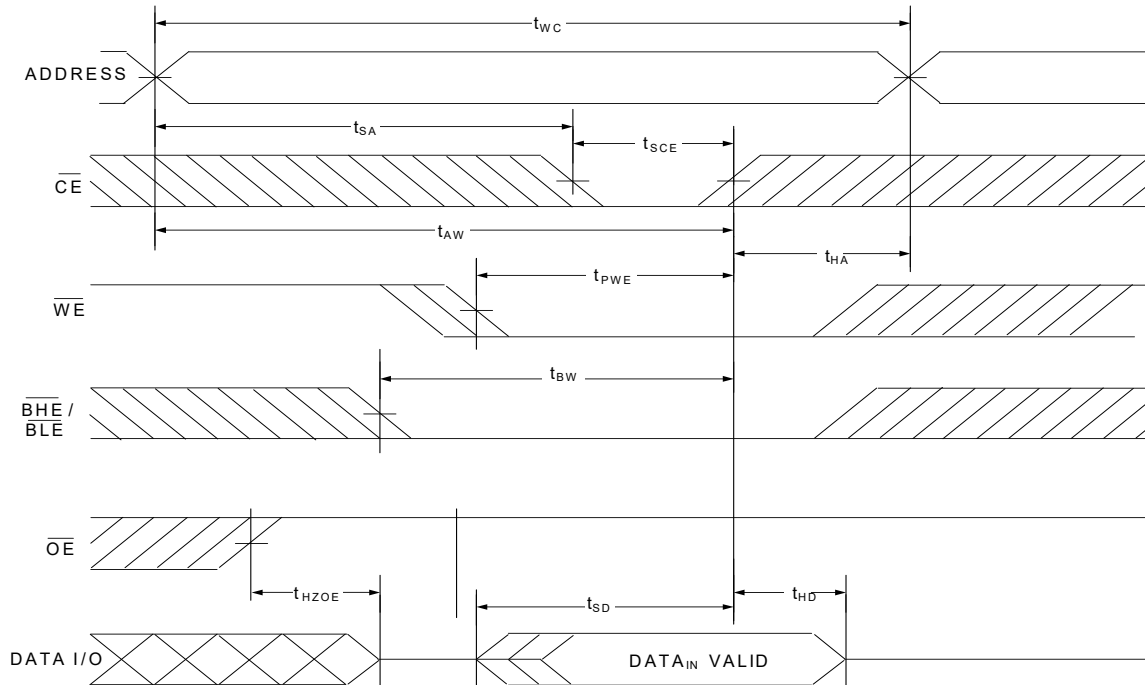
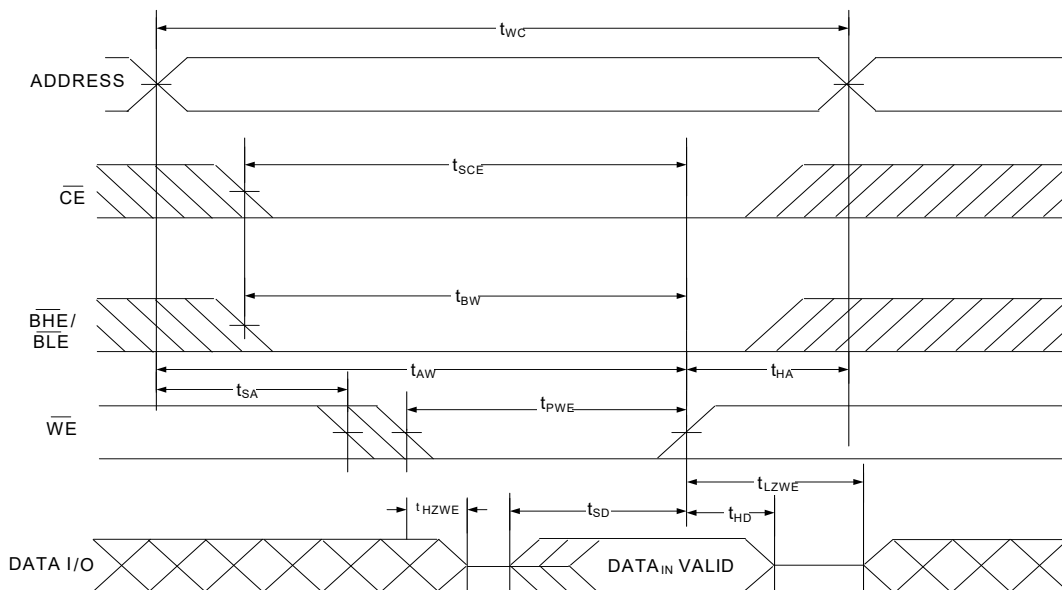
Figure 8. Write Cycle No. 1 (\overline{WE} Controlled) [25, 26, 27]



Notes

- 25. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 26. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 27. Data I/O is in a HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

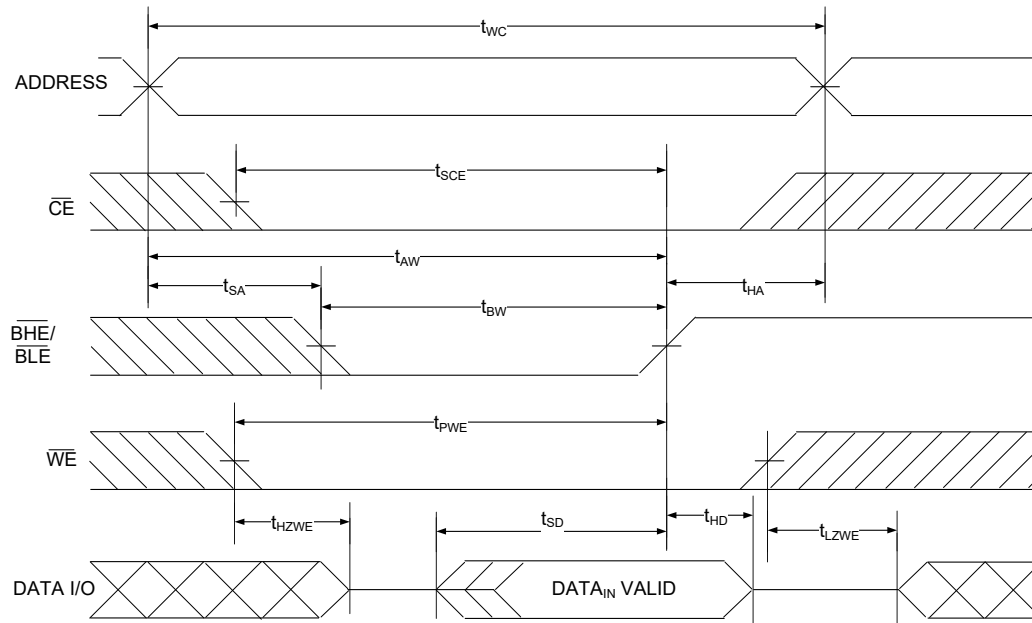
Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [28, 29, 30]

Figure 10. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [28, 29, 30, 31]

Notes

28. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
29. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{\text{IH}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
30. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
31. The minimum write pulse width for Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms (continued)

Figure 11. Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled) [32, 33, 34]



Notes

32. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
33. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{\text{IH}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
34. Data I/O is in a HI-Z state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

Truth Table – CY62147G/CY621472G

$\overline{CE} / \overline{CE}_1$	CE_2	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X ^[35]	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I _{SB})
X ^[35]	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I _{SB})
X ^[35]	X ^[35]	X	X	H	H	HI-Z	Deselect/Power-down	Standby (I _{SB})
L	H	H	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	H	H	L	H	L	Data Out (I/O ₀ –I/O ₇); HI-Z (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	H	H	L	L	H	HI-Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	H	H	H	L	H	HI-Z	Output disabled	Active (I _{CC})
L	H	H	H	H	L	HI-Z	Output disabled	Active (I _{CC})
L	H	H	H	L	L	HI-Z	Output disabled	Active (I _{CC})
L	H	L	X	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	H	L	X	H	L	Data In (I/O ₀ –I/O ₇); HI-Z (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})
L	H	L	X	L	H	HI-Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})

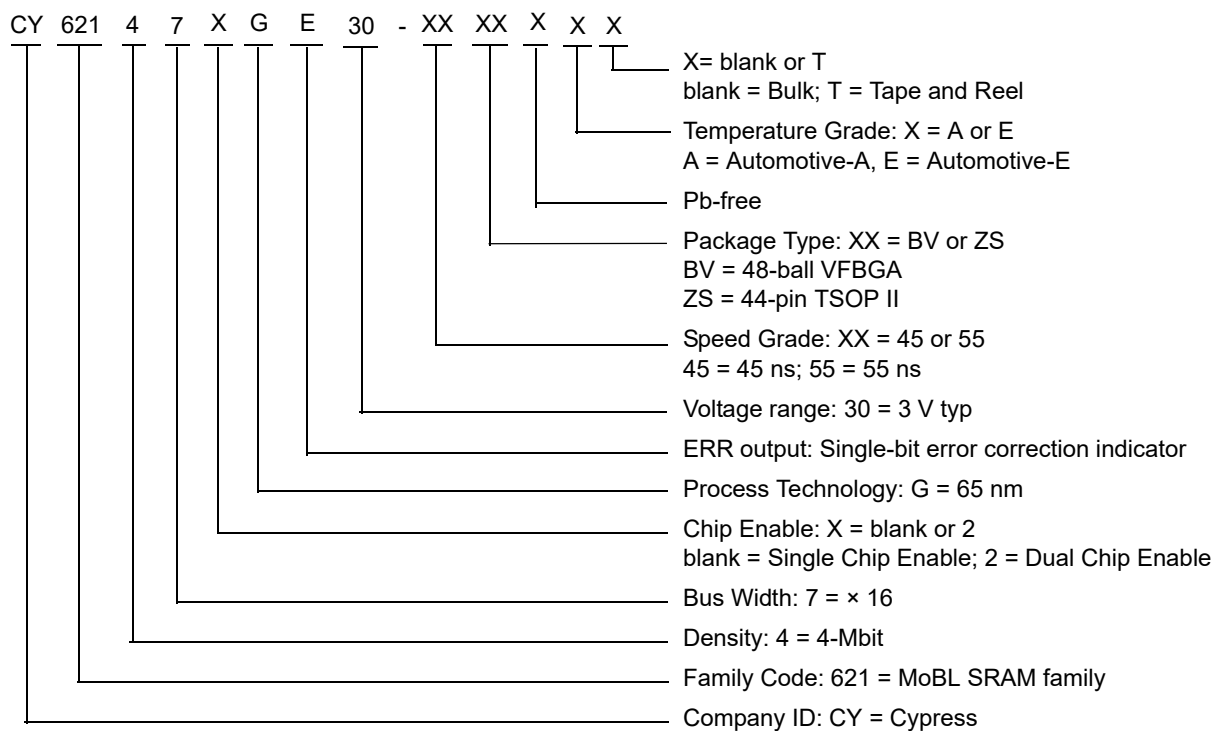
Note

35. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62147G30-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	Automotive-A
		CY62147G30-45BVXAT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	
		CY62147G30-45ZSXA	51-85087	44-pin TSOP II without ERR	
		CY62147G30-45ZSXAT	51-85087	44-pin TSOP II without ERR, Tape and Reel	
		CY621472G30-45ZSXA	51-85087	44-pin TSOP II, Dual Chip Enable	
		CY621472G30-45ZSXAT	51-85087	44-pin TSOP II, Dual Chip Enable, Tape and Reel	
55	2.2 V–3.6 V	CY62147G30-55BVXE	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	Automotive-E
		CY62147G30-55BVXET	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	
		CY62147G230-55ZSXE	51-85087	44-pin TSOP II, Dual Chip Enable	
		CY62147G230-55ZSXET	51-85087	44-pin TSOP II, Dual Chip Enable, Tape and Reel	
		CY62147G30-55ZSXE	51-85087	44-pin TSOP II	
		CY62147G30-55ZSXET	51-85087	44-pin TSOP II, Tape and Reel	

Ordering Code Definitions



Package Diagrams

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087

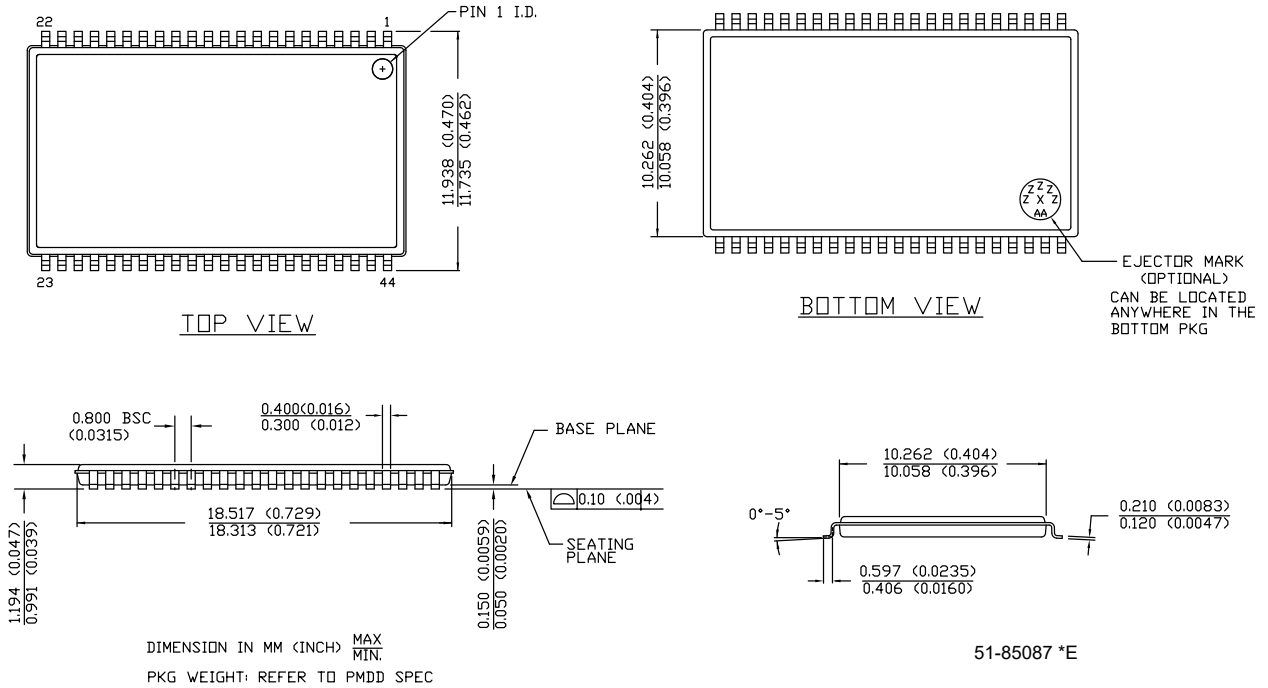
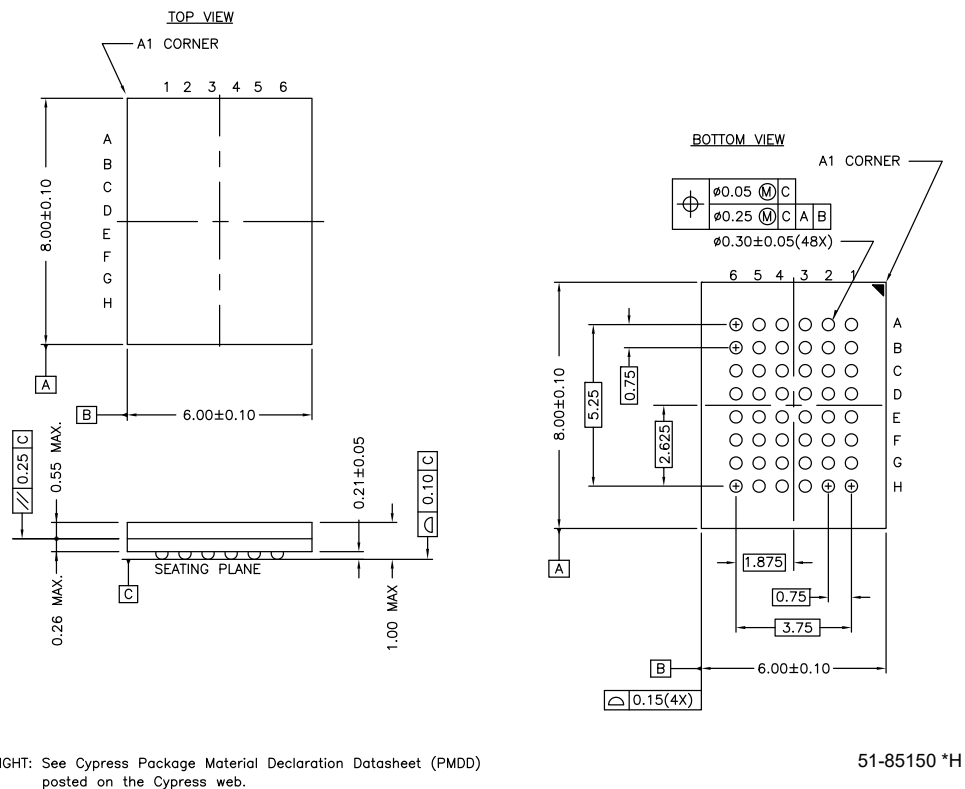


Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62147G/CY621472G MoBL [®] Automotive, 4-Mbit (256K words × 16-bit) Static RAM with Error-Correcting Code (ECC)				
Document Number: 001-95424				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B	5032662	NILE	12/01/2015	Changed status from Preliminary to Final.
*C	5428830	NILE	09/07/2016	Updated Maximum Ratings : Updated Note 5 (Replaced "2 ns" with "20 ns"). Updated DC Electrical Characteristics : Changed minimum value of V _{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range "2.7 V to 3.6 V" and Test Condition "V _{CC} = Min, I _{OH} = -1.0 mA". Changed minimum value of V _{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range "2.2 V to 2.7 V". Updated Ordering Information : Updated part numbers. Updated to new template.
*D	5997948	AESATMP8	12/18/2017	Updated logo and Copyright.
*E	6119305	NILE	04/02/2018	Updated Features : Added Note 2 and referred the same note in "Embedded ECC for single-bit error correction". Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2015-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [SRAM](#) category:

Click to view products by [Cypress](#) manufacturer:

Other Similar products are found below :

[CY6116A-35DMB](#) [CY7C1049GN-10VXI](#) [CY7C128A-45DMB](#) [GS8161Z36DD-200I](#) [GS88237CB-200I](#) [RMLV0408EGSB-4S2#AA0](#)
[IDT70V5388S166BG](#) [IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#)
[CY7C1353S-100AXC](#) [AS6C8016-55BIN](#) [AS7C164A-15PCN](#) [515712X](#) [IDT71V67603S133BG](#) [IS62WV51216EBLL-45BLI](#)
[IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#) [70V639S10BCG](#) [IS66WVE4M16EALL-70BLI](#) [IS62WV6416DBLL-45BLI](#)
[IS61WV102416DBLL-10TLI](#) [CY7C1381KV33-100AXC](#) [CY7C1381KVE33-133AXI](#) [8602501XA](#) [5962-3829425MUA](#) [5962-3829430MUA](#)
[5962-8855206YA](#) [5962-8866201YA](#) [5962-8866204TA](#) [5962-8866206MA](#) [5962-8866208UA](#) [5962-8872502XA](#) [5962-9062007MXA](#) [5962-](#)
[9161705MXA](#) [70V3579S6BFI](#) [GS882Z18CD-150I](#) [M38510/28902BVA](#) [8413202RA](#) [5962-9161708MYA](#) [5962-8971203XA](#) [5962-](#)
[8971202ZA](#) [5962-8872501LA](#) [5962-8866208YA](#) [5962-8866205YA](#) [5962-8866205UA](#) [5962-8866203YA](#) [5962-8855202YA](#)