# CY7C09269V/79V/89V
# CY7C09369V/89V

# 3.3 V 16K / 32K / 64K × 16 / 18 Synchronous Dual-Port Static RAM

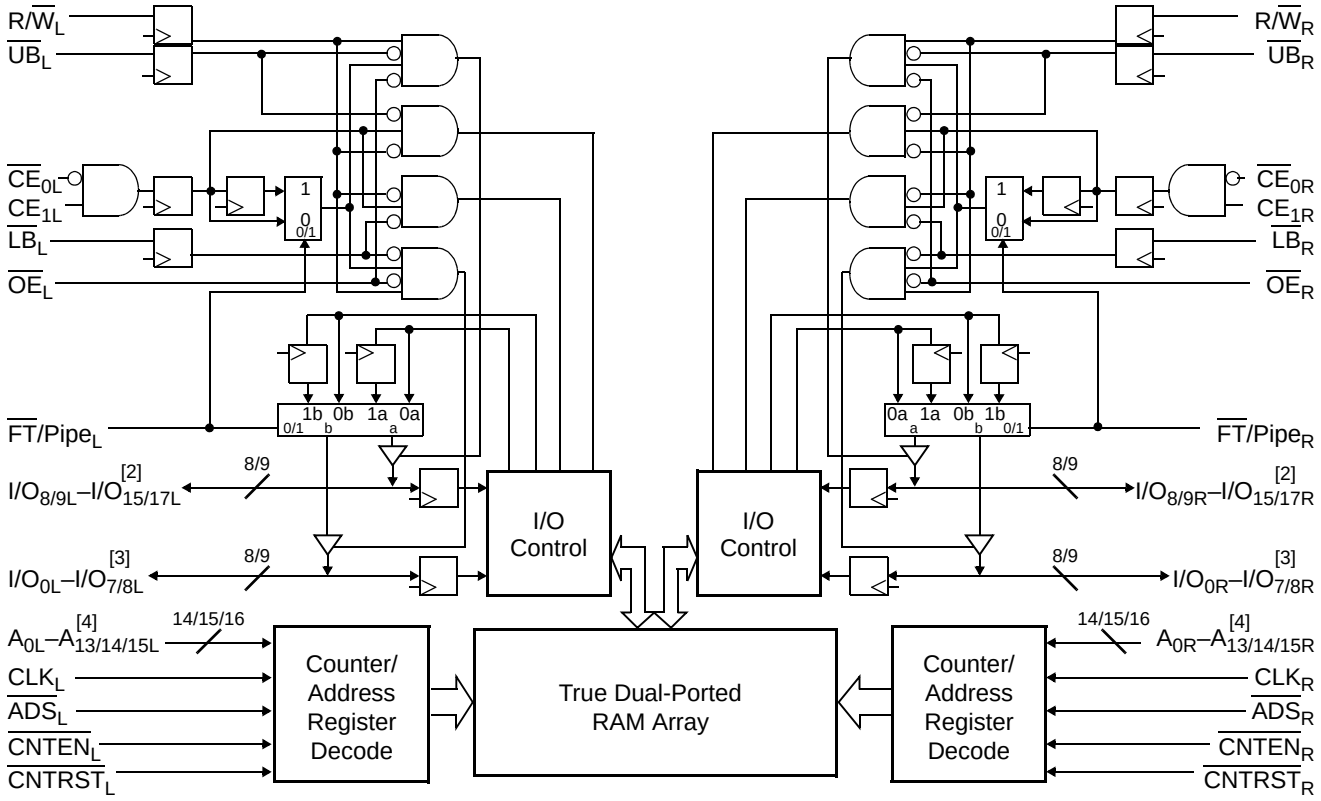
## Features

- True dual-ported memory cells that allow simultaneous access of the same memory location
- Six flow through/pipelined devices:
  - 16K × 16 / 18 organization (CY7C09269V/369V)
  - 32K × 16 organization (CY7C09279V)
  - 64K × 16 / 18 organization (CY7C09289V/389V)
- Three modes:
  - Flow through
  - Pipelined
  - Burst
- Pipelined output mode on both ports allows fast 100 MHz operation
- 0.35 micron CMOS for optimum speed and power
- High speed clock to data access: 7.5[1], 9, 12 ns (max)
- 3.3 V low operating power:
  - Active = 115 mA (typical)
  - Standby = 10 μA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally:
  - Shorten cycle times
  - Minimize bus noise
  - Supported in flow through and pipelined modes
- Dual chip enables easy depth expansion
- Upper and lower byte controls for bus matching
- Automatic power down
- Commercial and industrial temperature ranges
- Pb-free 100-pin TQFP package available

## Functional Description

For a complete list of related documentation, click here.

## Logic Block Diagram

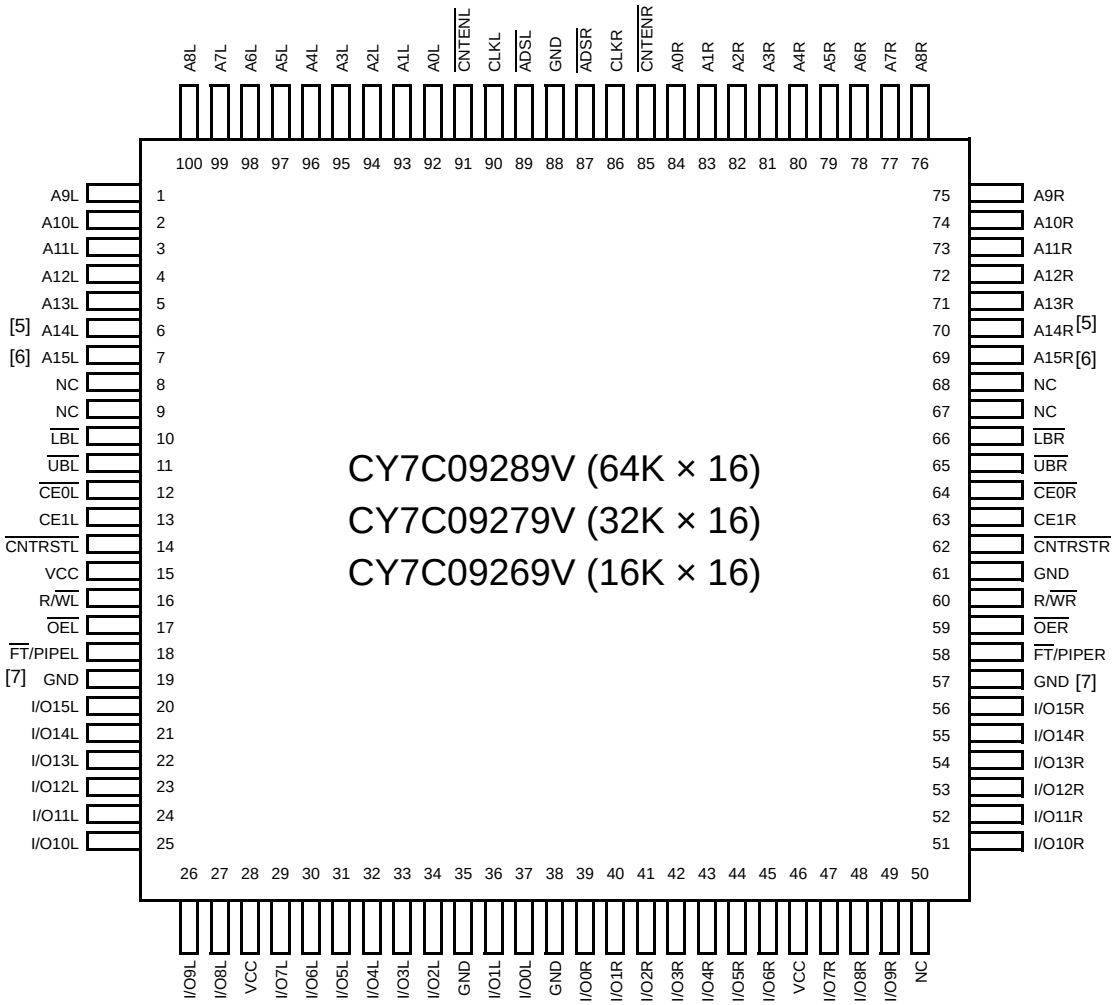



**Notes**
1. See Figure 4 on page 8 for Load Conditions.
2. $I/O_8$–$I/O_{15}$ for × 16 devices; $I/O_9$–$I/O_{17}$ for × 18 devices.
3. $I/O_0$–$I/O_7$ for × 16 devices. $I/O_0$–$I/O_8$ for × 18 devices.
4. $A_0$–$A_{13}$ for 16K; $A_0$–$A_{14}$ for 32K; $A_0$–$A_{15}$ for 64K devices.

## Contents

## Pin Configurations

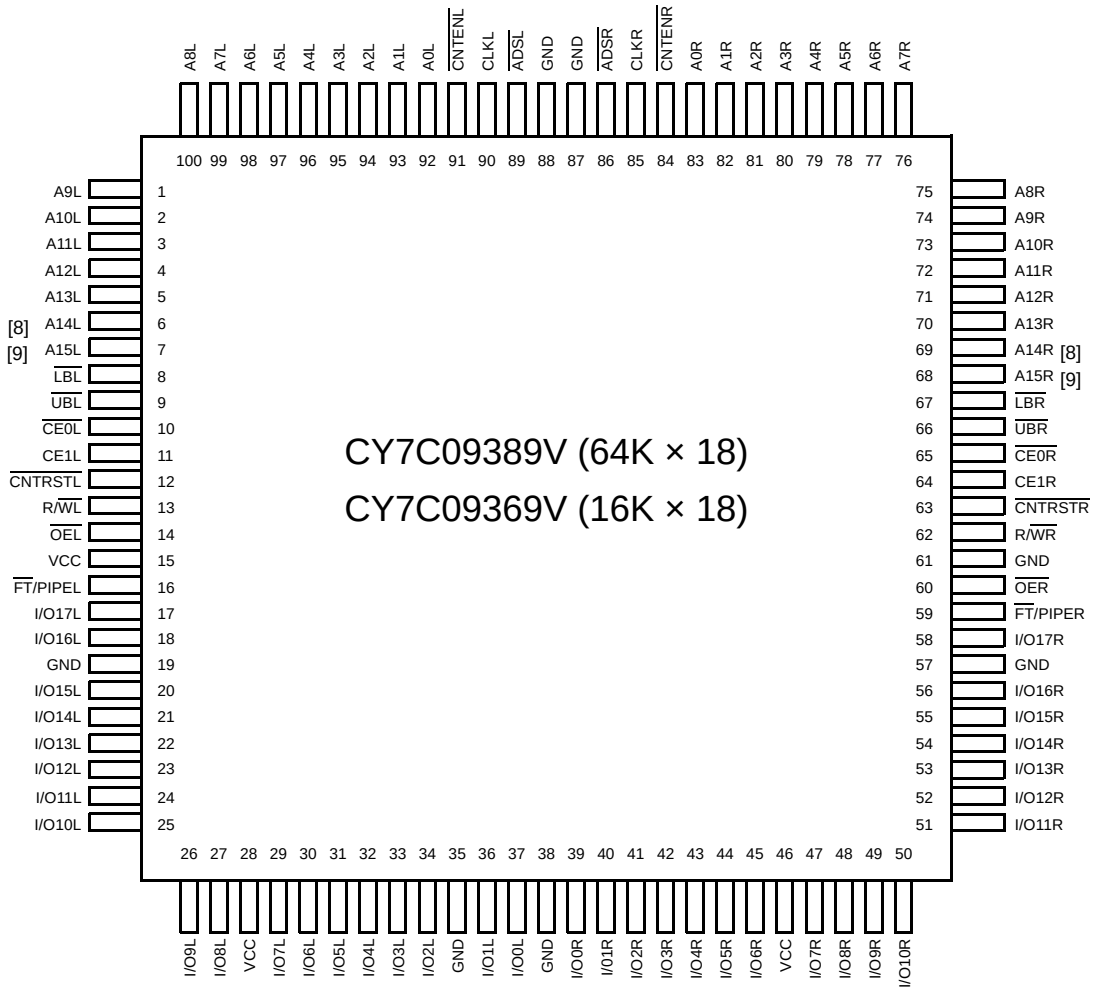
**Figure 1. 100-pin TQFP pinout (Top View)**




**Notes**
5. This pin is NC for CY7C09269V.
6. This pin is NC for CY7C09269V and CY7C09279V.
7. For CY7C09269V and CY7C09279V, pin #18 connected to $V_{CC}$ is pin compatible to an IDT 5 V × 16 pipelined device; connecting pin #18 and #58 to GND is pin compatible to an IDT 5 V × 16 flow through device.

## Pin Configurations (continued)

**Figure 2. 100-pin TQFP pinout (Top View)**




**Notes**
8. This pin is NC for CY7C09369V.
9. This pin is NC for CY7C09369V.

## Selection Guide

| Specifications | CY7C09269V/79V/89V CY7C09369V/89V -7[10] | CY7C09269V/79V/89V CY7C09369V/89V -9 | CY7C09269V/79V/89V CY7C09369V/89V -12 |
|---|---|---|---|
| $f_{MAX2}$ (MHz) (Pipelined) | 83 | 67 | 50 |
| Max. Access Time (ns) (Clock to Data, Pipelined) | 7.5 | 9 | 12 |
| Typical Operating Current $I_{CC}$ (mA) | 155 | 135 | 115 |
| Typical Standby Current for $I_{SB1}$ (mA) (Both Ports TTL Level) | 25 | 20 | 20 |
| Typical Standby Current for $I_{SB3}$ (µA) (Both Ports CMOS Level) | 10 | 10 | 10 |

## Pin Definitions

| Left Port | Right Port | Description |
|---|---|---|
| $A_{0L}$–$A_{15L}$ | $A_{0R}$–$A_{15R}$ | **Address Inputs** ($A_0$–$A_{14}$ for 32K, $A_0$–$A_{13}$ for 16K devices). |
| $\overline{ADS}_L$ | $\overline{ADS}_R$ | **Address Strobe Input.** Used as an address qualifier. This signal must be asserted LOW to access the part using an externally supplied address. Asserting this signal LOW also loads the burst counter with the address present on the address pins. |
| $\overline{CE}_{0L}$, $CE_{1L}$ | $\overline{CE}_{0R}$,$CE_{1R}$ | **Chip Enable Input.** To select either the left or right port, both $\overline{CE}_0$ AND $CE_1$ must be asserted to their active states ($\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$). |
| $CLK_L$ | $CLK_R$ | **Clock Signal.** This input can be free running or strobed. Maximum clock input rate is $f_{MAX}$. |
| $\overline{CNTEN}_L$ | $\overline{CNTEN}_R$ | **Counter Enable Input.** Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. CNTEN is disabled if ADS or CNTRST are asserted LOW. |
| $\overline{CNTRST}_L$ | $\overline{CNTRST}_R$ | **Counter Reset Input.** Asserting this signal LOW resets the burst address counter of its respective port to zero. CNTRST is not disabled by asserting ADS or CNTEN. |
| $I/O_{0L}$–$I/O_{17L}$ | $I/O_{0R}$–$I/O_{17R}$ | **Data Bus Input/Output** ($I/O_0$–$I/O_{15}$ for × 16 devices). |
| $\overline{LB}_L$ | $\overline{LB}_R$ | **Lower Byte Select Input**. Asserting this signal LOW enables read and write operations to the lower byte. ($I/O_0$–$I/O_8$ for × 18, $I/O_0$–$I/O_7$ for × 16) of the memory array. For read operations both the $\overline{LB}$ and $\overline{OE}$ signals must be asserted to drive output data on the lower byte of the data pins. |
| $\overline{UB}_L$ | $\overline{UB}_R$ | **Upper Byte Select Input.** Same function as $\overline{LB}$, but to the upper byte ($I/O_{8/9L}$–$I/O_{15/17L}$). |
| $\overline{OE}_L$ | $\overline{OE}_R$ | **Output Enable Input.** This signal must be asserted LOW to enable the I/O data pins during read operations. |
| $R/\overline{W}_L$ | $R/\overline{W}_R$ | **Read/Write Enable Input**. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH. |
| $\overline{FT}/PIPE_L$ | $\overline{FT}/PIPE_R$ | **Flow Through/Pipelined Select Input.** For flow through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH. |
| GND | | **Ground Input**. |
| NC | | **No Connect**. |
| $V_{CC}$ | | **Power Input**. |

**Note**
10. See Figure 4 on page 8 for Load Conditions.

## Functional Overview

The CY7C09269V/79V/89V and CY7C09369V/89V are high speed 3.3 V synchronous CMOS 16K, 32K, and 64K × 16 and 16K and 64K × 18 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory [11]. Registers on control, address, and data lines allow for minimal setup and hold times. In pipelined output mode, data is registered for decreased cycle time and clock to data valid $t_{CD2}$ = 7.5 ns [12] (pipelined). Flow through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow through mode, data is available $t_{CD1}$ = 18 ns after the address is clocked into the device. Pipelined output or flow through mode is selected through the $\overline{FT}$/Pipe pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW to HIGH transition of the clock signal. The internal write pulse is self timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE}_0$ or LOW on $CE_1$ for one clock cycle powers down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables enables easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with $\overline{CE}_0$ LOW and $CE_1$ HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and use the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe ($\overline{ADS}$). When the port's Count Enable ($\overline{CNTEN}$) is asserted, the address counter increments on each LOW to HIGH transition of that port's clock signal. This reads/writes one word from or into each successive address location, until $\overline{CNTEN}$ is deasserted. The counter can address the entire memory array and loop back to the start. Counter Reset ($\overline{CNTRST}$) is used to reset the burst counter.

All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages.

**Notes**
11. When writing simultaneously to the same location, the final value cannot be guaranteed.
12. See Figure 4 on page 8 for Load Conditions.

## Maximum Ratings

Exceeding maximum ratings [13] may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential ..... –0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State ..... –0.5 V to $V_{CC}$ + 0.5 V

DC Input Voltage ..... –0.5 V to $V_{CC}$ + 0.5 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 1100 V

Latch up Current ..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0 °C to +70 °C | 3.3 V ± 300 mV |
| Industrial | –40 °C to +85 °C | 3.3 V ± 300 mV |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | | CY7C09269V/79V/89V CY7C09369V/89V | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -7[14] | | | -9 | | | -12 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage ($V_{CC}$ = Min, $I_{OH}$ = –4.0 mA) | | 2.4 | – | – | 2.4 | – | – | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW Voltage ($V_{CC}$ = Min, $I_{OH}$ = +4.0 mA) | | – | – | 0.4 | – | – | 0.4 | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | – | – | 2.0 | – | – | 2.0 | – | – | V |
| $V_{IL}$ | Input LOW Voltage | | – | – | 0.8 | – | – | 0.8 | – | – | 0.8 | V |
| $I_{OZ}$ | Output Leakage Current | | –10 | – | 10 | –10 | – | 10 | –10 | – | 10 | µA |
| $I_{CC}$ | Operating Current ($V_{CC}$ = Max, $I_{OUT}$ = 0 mA) Outputs Disabled | Commercial | – | 155 | 275 | – | 135 | 230 | – | 115 | 180 | mA |
| | | Industrial | – | 275 | 390 | – | 185 | 300 | – | – | – | mA |
| $I_{SB1}$ | Standby Current (Both Ports TTL Level) [15] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Commercial | – | 25 | 85 | – | 20 | 75 | – | 20 | 70 | mA |
| | | Industrial | – | 85 | 120 | – | 35 | 85 | – | – | – | mA |
| $I_{SB2}$ | Standby Current (One Port TTL Level) [15] $\overline{CE}_L$ \| $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Commercial | – | 105 | 165 | – | 95 | 155 | – | 85 | 140 | mA |
| | | Industrial | – | 165 | 210 | – | 105 | 165 | – | – | – | mA |
| $I_{SB3}$ | Standby Current (Both Ports CMOS Level) [15] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ – 0.2 V, f = 0 | Commercial | – | 10 | 250 | – | 10 | 250 | – | 10 | 250 | µA |
| | | Industrial | – | 10 | 250 | – | 10 | 250 | – | – | – | µA |
| $I_{SB4}$ | Standby Current (One Port CMOS Level) [15] $\overline{CE}_L$ \| $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Commercial | – | 95 | 125 | – | 85 | 115 | – | 75 | 100 | mA |
| | | Industrial | – | 125 | 170 | – | 95 | 125 | – | – | – | mA |

## Capacitance

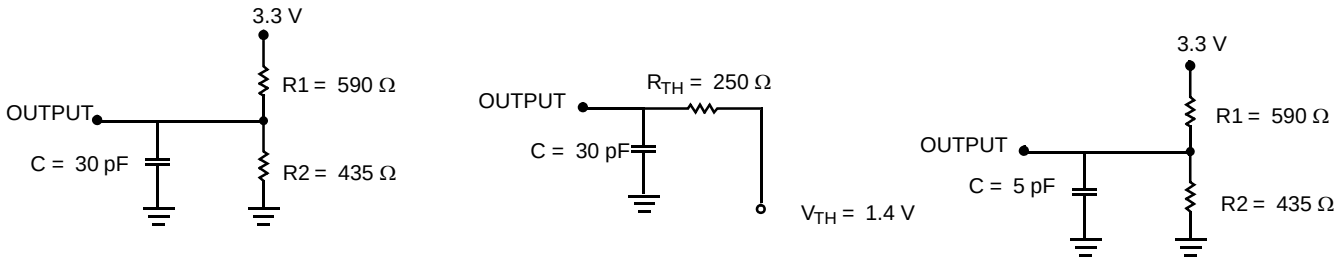
| Parameter [16] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = 3.3 V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

**Notes**

13. The voltage on any input or I/O pin can not exceed the power pin during power up.
14. See Figure 4 on page 8 for Load Conditions.
15. $\overline{CE}_L$ and $\overline{CE}_R$ are internal signals. To select either the left or right port, both $\overline{CE}_0$ and $CE_1$ must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).
16. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

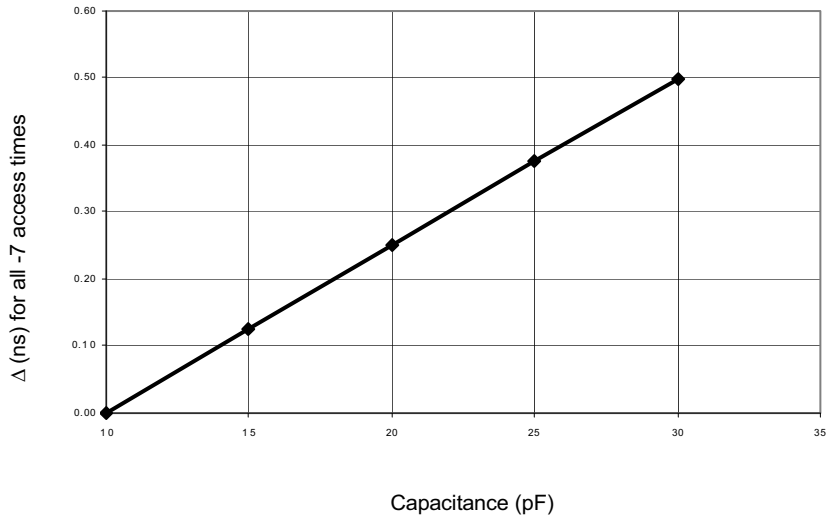
**Figure 3. AC Test Loads and Waveforms**




**(a) Normal Load (Load 1)** **(b) Thévenin Equivalent (Load 1)** **(c) Three-State Delay (Load 2)**
(Used for $t_{CKLZ}$, $t_{OLZ}$, and $t_{OHZ}$ including scope and jig)

**Figure 4. AC Test Loads (Applicable to -7 only)** [17]


**(a) Load 1 (-7 only)**




**(b) Load Derating Curve**

**Note**
17. Test Conditions: C = 10 pF.

## Switching Characteristics

Over the Operating Range

| Parameter | Description | CY7C09269V/79V/89V CY7C09369V/89V | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -7 [18] | | -9 | | -12 | | |
| | | Min | Max | Min | Max | Min | Max | |
| $f_{MAX1}$ | $f_{Max}$ Flow Through | – | 45 | – | 40 | – | 33 | MHz |
| $f_{MAX2}$ | $f_{Max}$ Pipelined | – | 83 | – | 67 | – | 50 | MHz |
| $t_{CYC1}$ | Clock Cycle Time - Flow Through | 22 | – | 25 | – | 30 | – | ns |
| $t_{CYC2}$ | Clock Cycle Time - Pipelined | 12 | – | 15 | – | 20 | – | ns |
| $t_{CH1}$ | Clock HIGH Time - Flow Through | 7.5 | – | 12 | – | 12 | – | ns |
| $t_{CL1}$ | Clock LOW Time - Flow Through | 7.5 | – | 12 | – | 12 | – | ns |
| $t_{CH2}$ | Clock HIGH Time - Pipelined | 5 | – | 6 | – | 8 | – | ns |
| $t_{CL2}$ | Clock LOW Time - Pipelined | 5 | – | 6 | – | 8 | – | ns |
| $t_R$ | Clock Rise Time | – | 3 | – | 3 | – | 3 | ns |
| $t_F$ | Clock Fall Time | – | 3 | – | 3 | – | 3 | ns |
| $t_{SA}$ | Address Set-Up Time | 4 | – | 4 | – | 4 | – | ns |
| $t_{HA}$ | Address Hold Time | 0 | – | 1 | – | 1 | – | ns |
| $t_{SC}$ | Chip Enable Setup Time | 4 | – | 4 | – | 4 | – | ns |
| $t_{HC}$ | Chip Enable Hold Time | 0 | – | 1 | – | 1 | – | ns |
| $t_{SW}$ | R/$\overline{W}$ Set-Up Time | 4 | – | 4 | – | 4 | – | ns |
| $t_{HW}$ | R/$\overline{W}$ Hold Time | 0 | – | 1 | – | 1 | – | ns |
| $t_{SD}$ | Input Data Setup Time | 4 | – | 4 | – | 4 | – | ns |
| $t_{HD}$ | Input Data Hold Time | 0 | – | 1 | – | 1 | – | ns |
| $t_{SAD}$ | $\overline{ADS}$ Set-Up Time | 4 | – | 4 | – | 4 | – | ns |
| $t_{HAD}$ | $\overline{ADS}$ Hold Time | 0 | – | 1 | – | 1 | – | ns |
| $t_{SCN}$ | $\overline{CNTEN}$ Setup Time | 4.5 | – | 5 | – | 5 | – | ns |
| $t_{HCN}$ | $\overline{CNTEN}$ Hold Time | 0 | – | 1 | – | 1 | – | ns |
| $t_{SRST}$ | $\overline{CNTRST}$ Setup Time | 4 | – | 4 | – | 4 | – | ns |
| $t_{HRST}$ | $\overline{CNTRST}$ Hold Time | 0 | – | 1 | – | 1 | – | ns |
| $t_{OE}$ | Output Enable to Data Valid | – | 9 | – | 10 | – | 12 | ns |
| $t_{OLZ}$ [19, 20] | $\overline{OE}$ to Low Z | 2 | – | 2 | – | 2 | – | ns |
| $t_{OHZ}$ [19, 20] | $\overline{OE}$ to High Z | 1 | 7 | 1 | 7 | 1 | 7 | ns |
| $t_{CD1}$ | Clock to Data Valid - Flow Through | – | 18 | – | 20 | – | 25 | ns |
| $t_{CD2}$ | Clock to Data Valid - Pipelined | – | 7.5 | – | 9 | – | 12 | ns |
| $t_{DC}$ | Data Output Hold After Clock HIGH | 2 | – | 2 | – | 2 | – | ns |
| $t_{CKHZ}$ [19, 20] | Clock HIGH to Output High Z | 2 | 9 | 2 | 9 | 2 | 9 | ns |
| $t_{CKLZ}$ [19, 20] | Clock HIGH to Output Low Z | 2 | – | 2 | – | 2 | – | ns |
| **Port to Port Delays** | | | | | | | | |
| $t_{CWDD}$ | Write Port Clock HIGH to Read Data Delay | – | 35 | – | 40 | – | 40 | ns |
| $t_{CCS}$ | Clock to Clock Setup Time | – | 10 | – | 15 | – | 15 | ns |

**Notes**
18. See Figure 4 on page 8 for Load Conditions.
19. Test conditions used are Load 2.
20. This parameter is guaranteed by design, but it is not production tested.

## Switching Waveforms

**Figure 5. Read Cycle for Flow Through Output ($\overline{FT}$/PIPE = $V_{IL}$) [21, 22, 23, 24]**

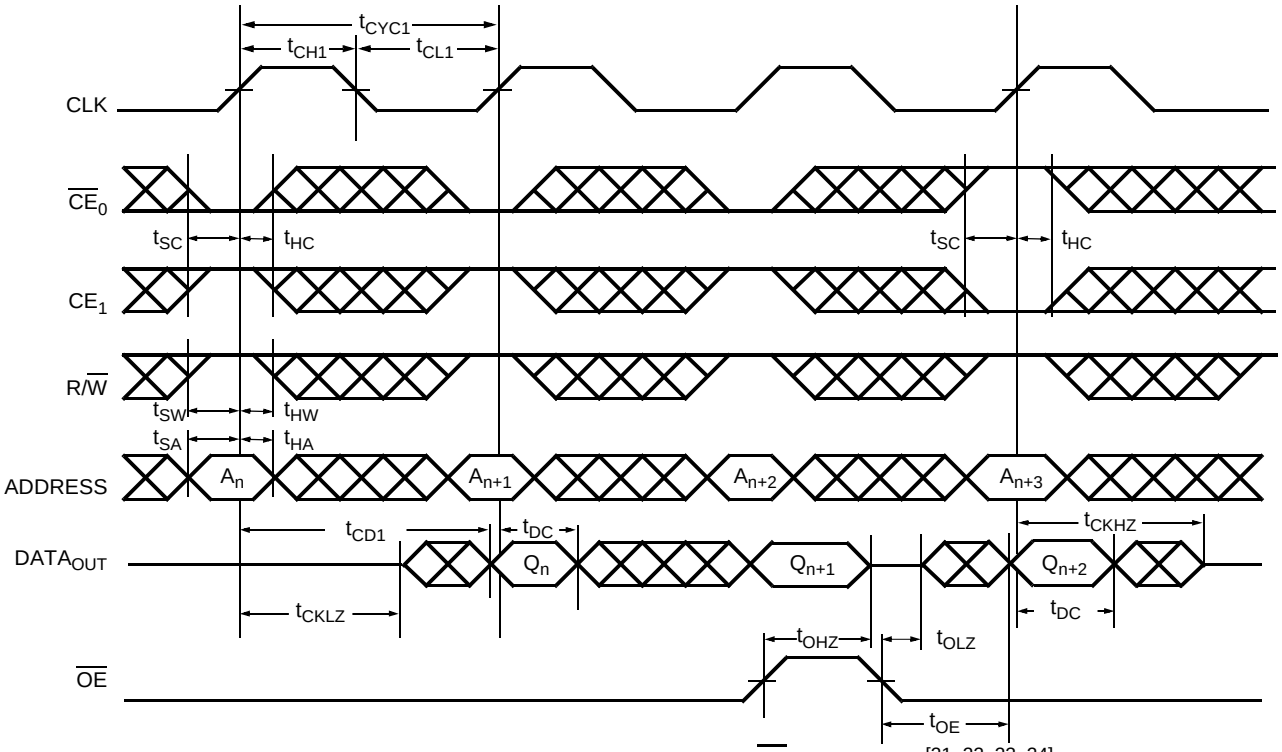
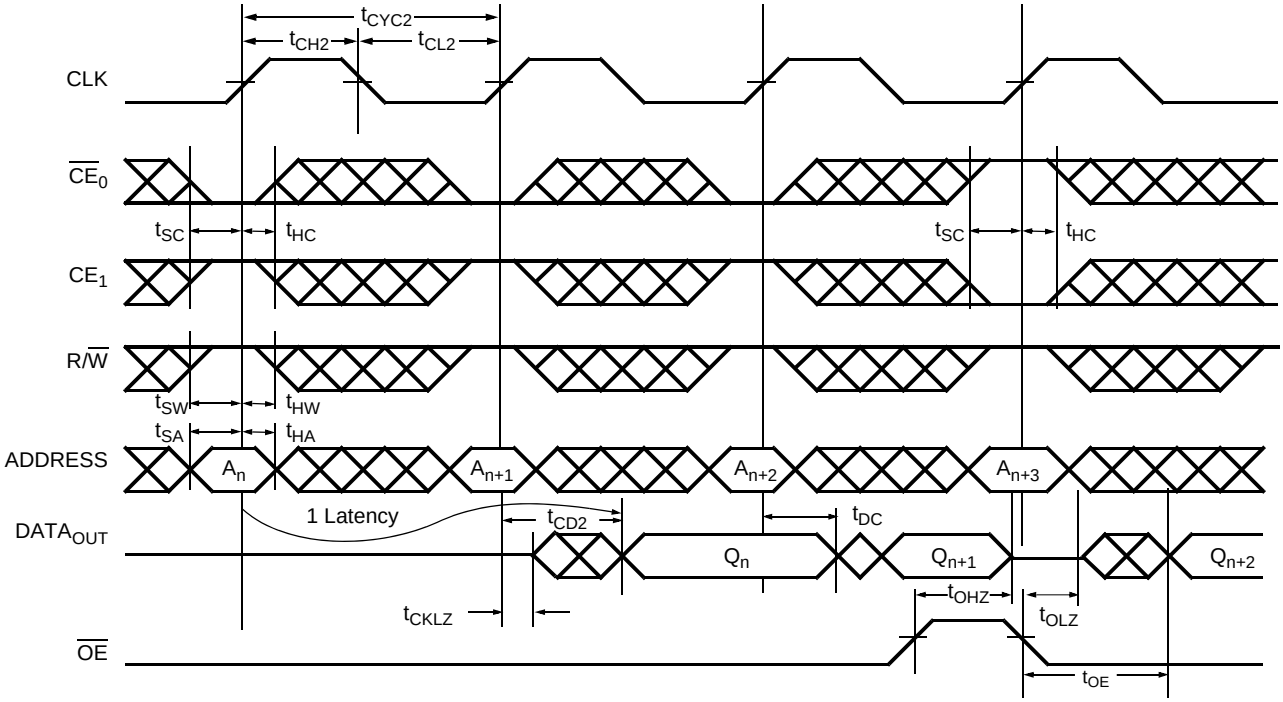



**Figure 6. Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE = $V_{IH}$) [21, 22, 23, 24]**




**Notes**

21. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
22. ADS = $V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = $V_{IH}$.
23. The output is disabled (high impedance state) by $\overline{CE}_0$=$V_{IH}$ or $CE_1$ = $V_{IL}$ following the next rising edge of the clock.
24. Addresses do not have to be accessed sequentially since ADS = $V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

## Switching Waveforms (continued)

**Figure 7. Bank Select Pipelined Read** [25, 26]

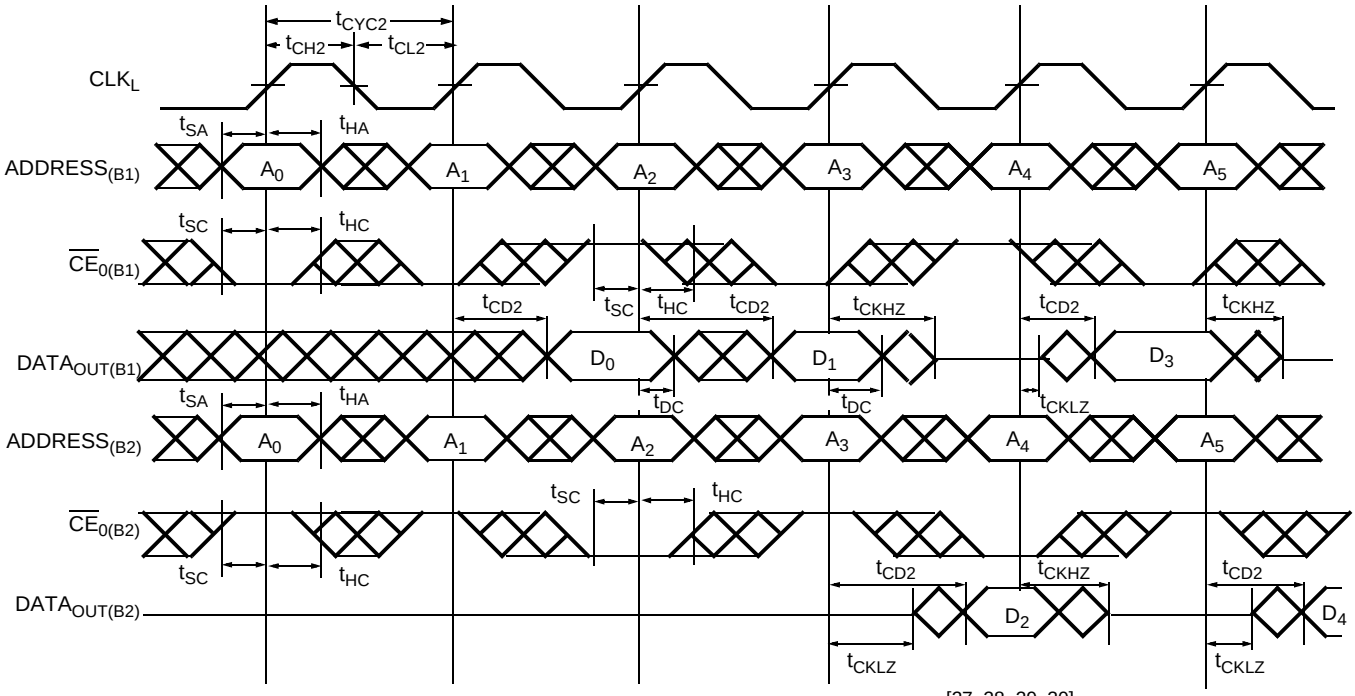
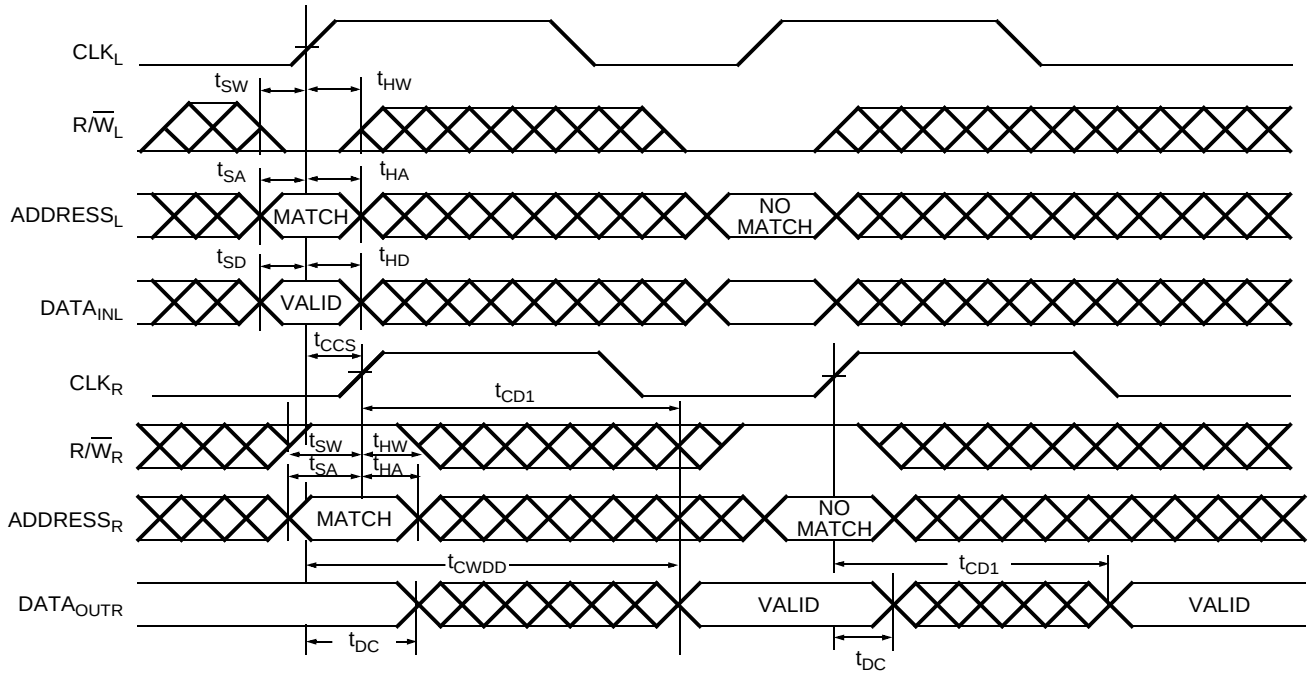



**Figure 8. Left Port Write to Flow Through Right Port Read** [27, 28, 29, 30]




**Notes**

25. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this datasheet. $\overline{ADDRESS}_{(B1)} = \overline{ADDRESS}_{(B2)}$.
26. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$ and $\overline{ADS} = V_{IL}$; $\overline{CE}_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
27. The same waveforms apply for a right port write to flow through left port read.
28. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
29. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
30. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for $t_{CWDD}$. If $t_{CCS}$>maximum specified, then data is not valid until $t_{CCS} + t_{CD1}$. $t_{CWDD}$ does not apply in this case.

## Switching Waveforms (continued)

**Figure 9. Pipelined Read-to-Write-to-Read ($\overline{OE}$ = $V_{IL}$)** [31, 32, 33, 34]

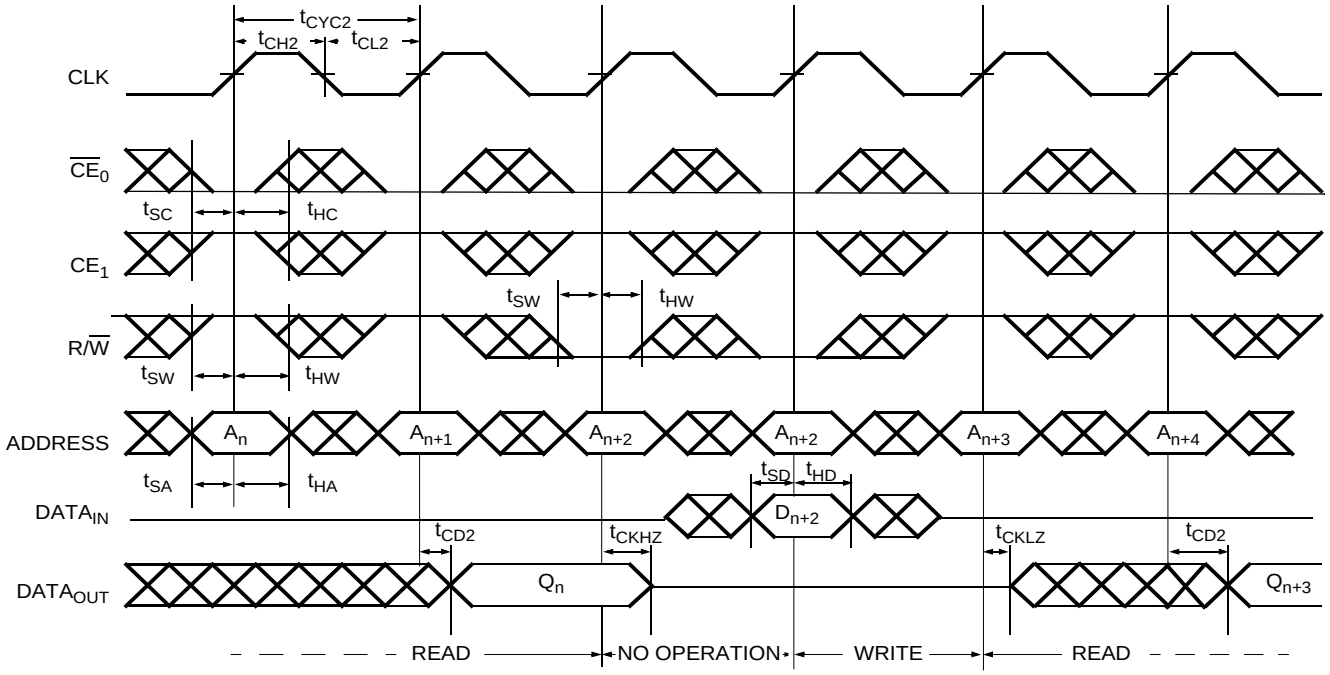
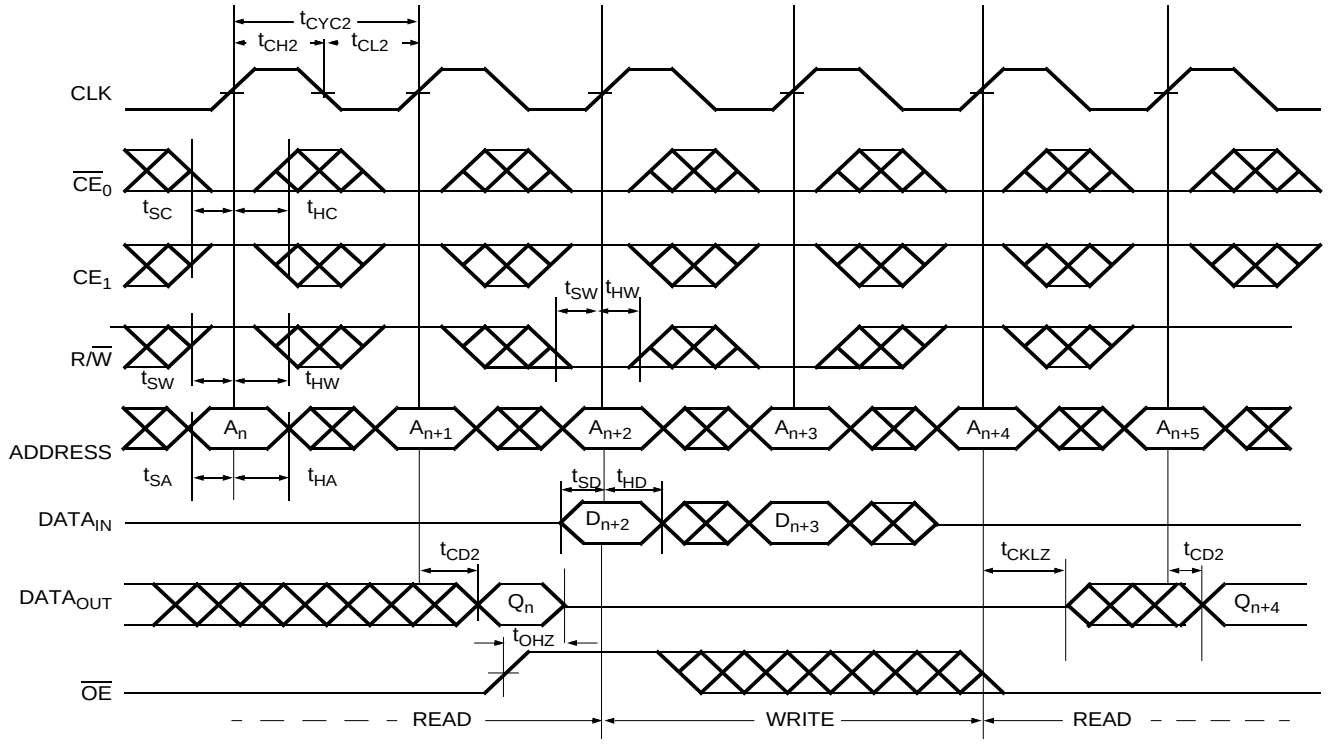



**Figure 10. Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)** [31, 32, 33, 34]

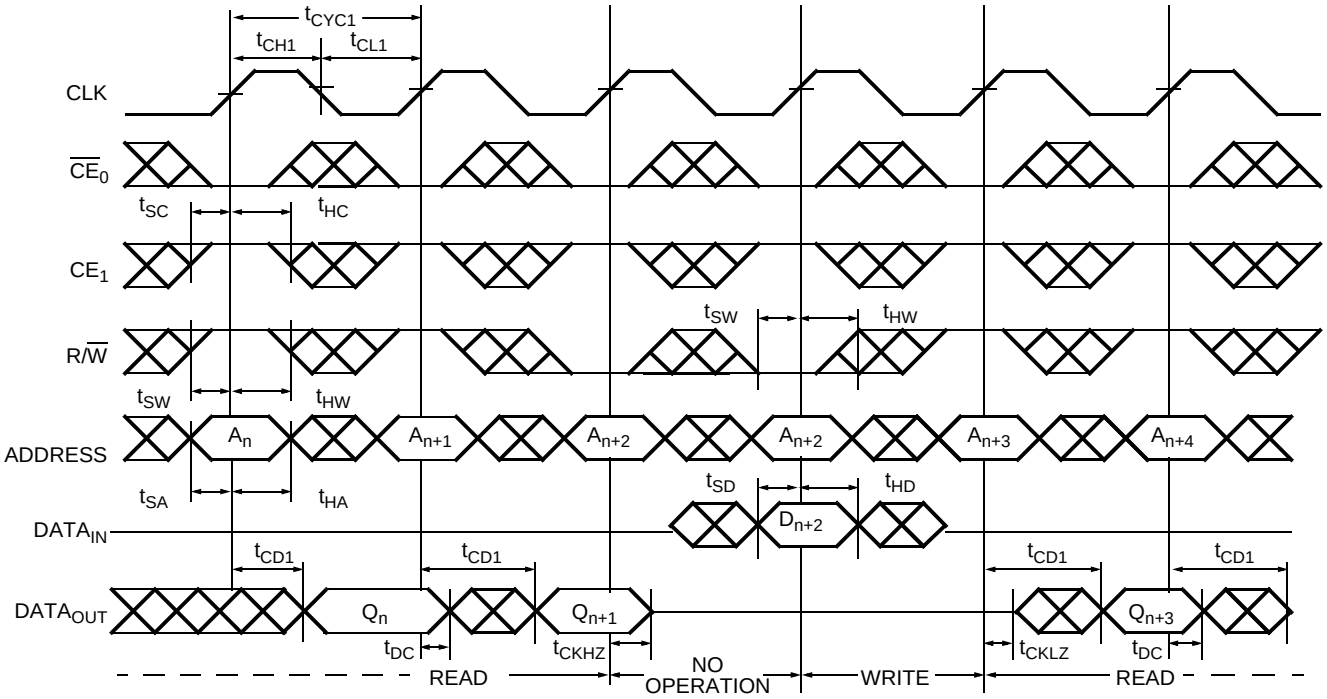



**Notes**

31. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
32. Output state (High, LOW, or high impedance) is determined by the previous cycle control signals.
33. $\overline{CE_0}$ and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = $V_{IH}$.
34. During “No Operation”, data in memory at the selected address may be corrupted and must be rewritten to ensure data integrity.

## Switching Waveforms (continued)

**Figure 11. Flow Through Read-to-Write-to-Read ($\overline{OE}$ = $V_{IL}$) [35, 36, 37, 38]**

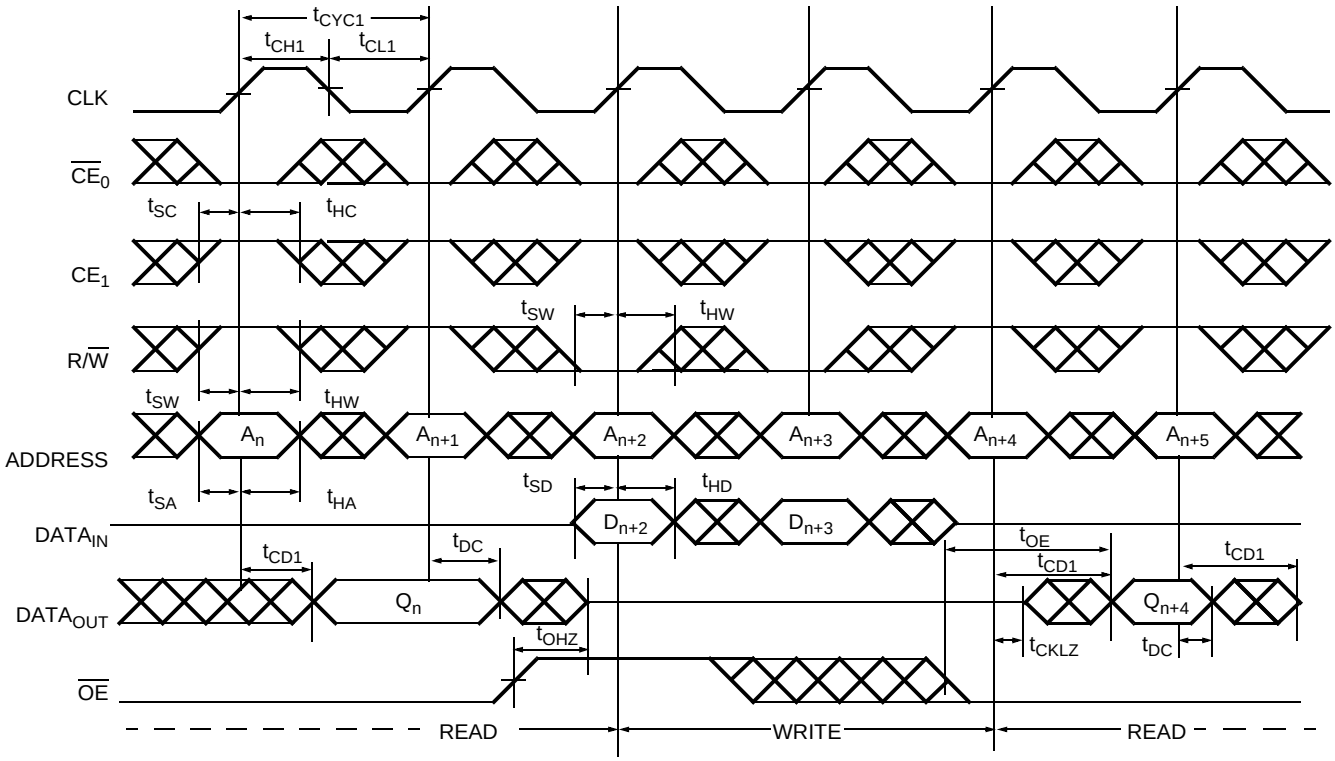



**Notes**

35. $\overline{ADS}$ = $V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = $V_{IH}$.
36. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
37. $\overline{CE}_0$ and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = $V_{IH}$.
38. During “No Operation”, data in memory at the selected address may be corrupted and must be rewritten to ensure data integrity.

## Switching Waveforms (continued)

**Figure 12. Flow Through Read-to-Write-to-Read ($\overline{OE}$ Controlled) [39, 40, 41, 42, 43]**




**Notes**
39. $\overline{ADS}$ = $V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = $V_{IH}$.
40. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
41. $\overline{CE_0}$ and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = $V_{IH}$.
42. During “No Operation”, data in memory at the selected address may be corrupted and must be rewritten to ensure data integrity.
43. Output state (High, LOW, or high impedance) is determined by the previous cycle control signals.

## Switching Waveforms (continued)

**Figure 13. Pipelined Read with Address Counter Advance [44]**

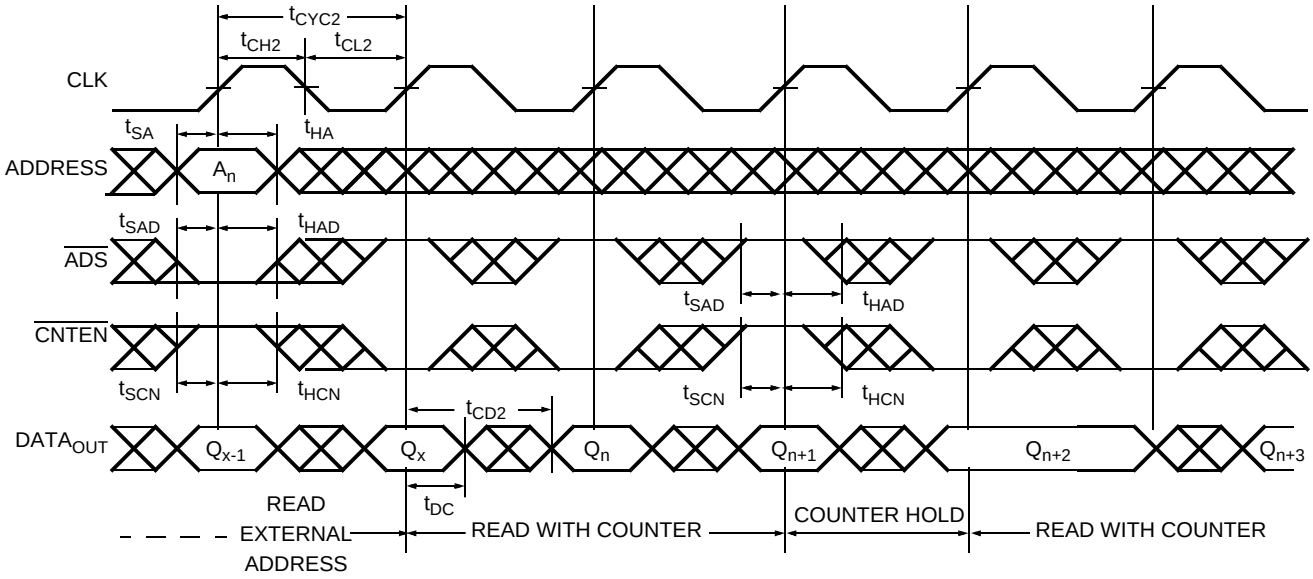
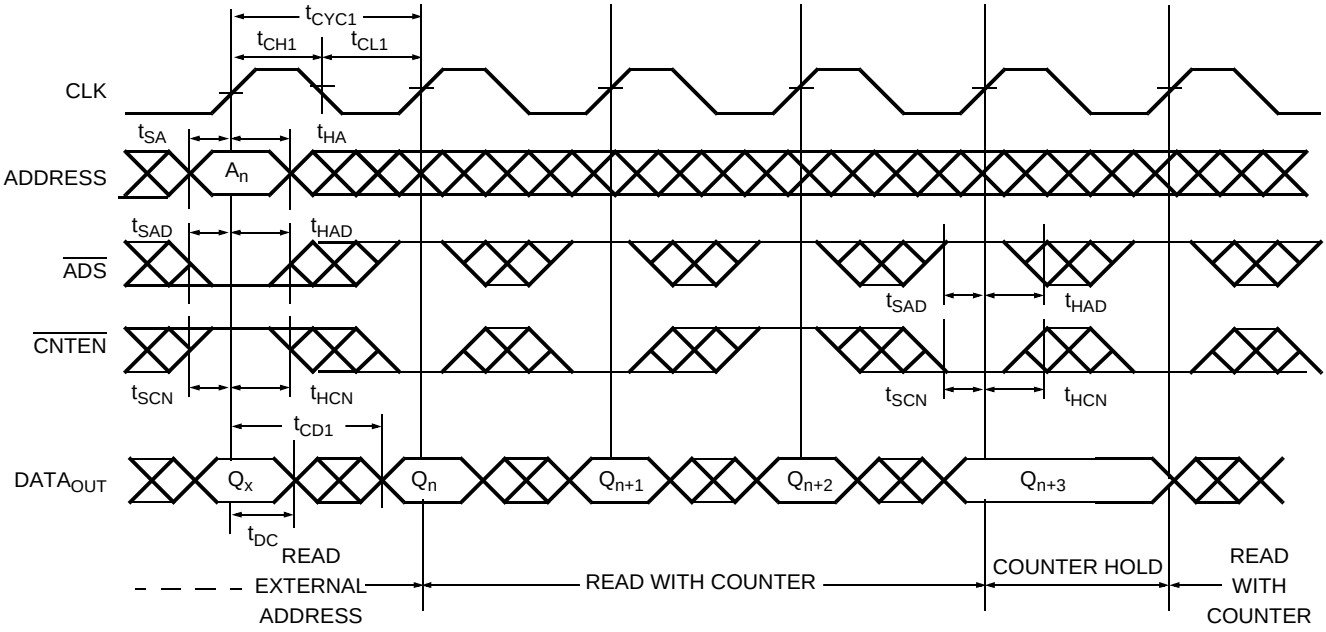


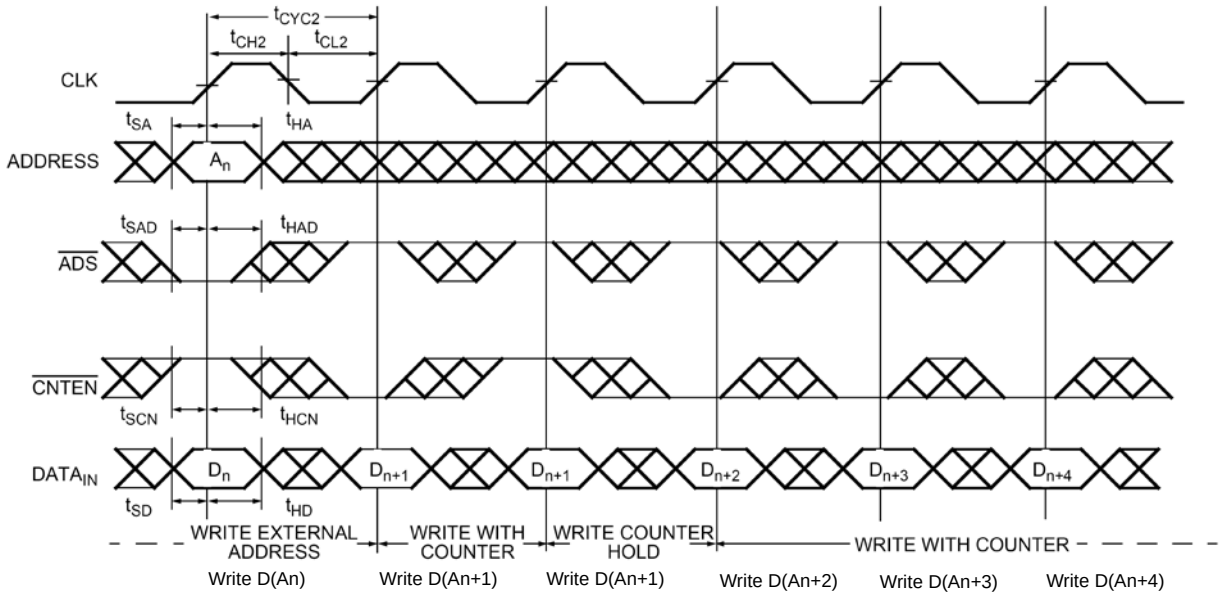

**Figure 14. Flow Through Read with Address Counter Advance [44]**




**Note**
44. $\overline{CE_0}$ and $\overline{OE}$ = $V_{IL}$; $CE_1$, R/$\overline{W}$ and $\overline{CNTRST}$ = $V_{IH}$.

## Switching Waveforms (continued)

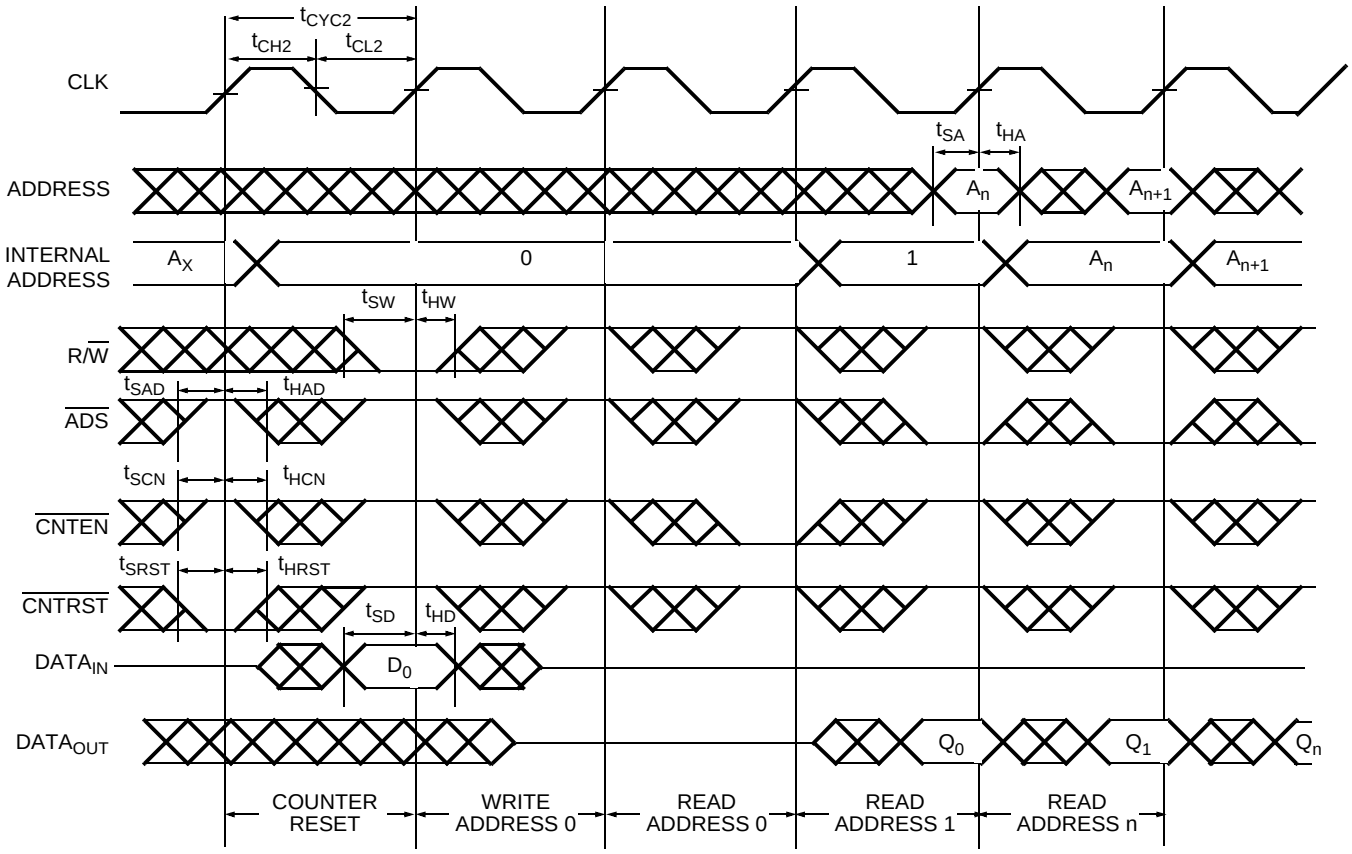
**Figure 15. Write with Address Counter Advance (Flow Through or Pipelined Outputs) [45, 46]**




**Notes**
45. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = $V_{IL}$; $CE_1$ and $\overline{CNTRST}$ = $V_{IH}$.
46. The “Internal Address” is equal to the “External Address” when $\overline{ADS}$ = $V_{IL}$ and equals the counter output when $\overline{ADS}$ = $V_{IH}$.

## Switching Waveforms (continued)

**Figure 16. Counter Reset (Pipelined Outputs)** [47, 48, 49, 50]




**Notes**
47. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
48. Output state (High, LOW, or high impedance) is determined by the previous cycle control signals.
49. $\overline{CE_0}$, $\overline{UB}$, and $\overline{LB}$ = $V_{IL}$; $CE_1$ = $V_{IH}$.
50. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

## Read/Write and Enable Operation

The Read/Write and Enable Operation is described as follows. [51, 52, 53]

| Inputs | | | | | Outputs | Operation |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | CLK | $\overline{CE_0}$ | $CE_1$ | R/$\overline{W}$ | $I/O_0$–$I/O_{17}$ | |
| X | ↑ | H | X | X | High Z | Deselected [54] |
| X | ↑ | X | L | X | High Z | Deselected [54] |
| X | ↑ | L | H | L | $D_{IN}$ | Write |
| L | ↑ | L | H | H | $D_{OUT}$ | Read [55] |
| H | X | L | H | X | High Z | Outputs Disabled |

## Address Counter Control Operation

The Address Counter Control Operation is described as follows. [51, 56, 57, 58]

| Address | Previous Address | CLK | $\overline{ADS}$ | $\overline{CNTEN}$ | $\overline{CNTRST}$ | I/O | Mode | Operation |
|---|---|---|---|---|---|---|---|---|
| X | X | ↑ | X | X | L | $D_{out(0)}$ | Reset | Counter Reset to Address 0 |
| $A_n$ | X | ↑ | L | X | H | $D_{out(n)}$ | Load | Address Load into Counter |
| X | $A_n$ | ↑ | H | H | H | $D_{out(n)}$ | Hold | External Address Blocked — Counter Disabled |
| X | $A_n$ | ↑ | H | L | H | $D_{out(n+1)}$ | Increment | Counter Enabled — Internal Address Generation |

**Notes**
51. "X" = "Don't Care", "H" = $V_{IH}$, "L" = $V_{IL}$.
52. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = "Don't Care".
53. $\overline{OE}$ is an asynchronous input signal.
54. When $\overline{CE}$ changes state in the pipelined mode, deselection and read happen in the following clock cycle.
55. $\overline{ADS}$ = $V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = $V_{IH}$.
56. $\overline{CE_0}$ and $\overline{OE}$ = $V_{IL}$; $CE_1$ and R/$\overline{W}$ = $V_{IH}$.
57. Data shown for flow through mode; pipelined mode output is delayed by one cycle.
58. Counter operation is independent of $\overline{CE_0}$ and $CE_1$.

## Ordering Information

### 16K × 16 3.3 V Synchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 9 | CY7C09269V-9AXC | 51-85048 | 100-pin TQFP (Pb-free) | Commercial |

### 32K × 16 3.3 V Synchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 7.5 [59] | CY7C09279V-7AXC | 51-85048 | 100-pin TQFP (Pb-free) | Commercial |
| 12 | CY7C09279V-12AXC | 51-85048 | 100-pin TQFP (Pb-free) | Commercial |

### 64K × 16 3.3 V Synchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 9 | CY7C09289V-9AXC | 51-85048 | 100-pin TQFP (Pb-free) | Commercial |
| | CY7C09289V-9AXI | 51-85048 | 100-pin TQFP (Pb-free) | Industrial |
| 12 | CY7C09289V-12AXC | 51-85048 | 100-pin TQFP (Pb-free) | Commercial |

### 16K × 18 3.3 V Synchronous Dual-Port SRAM

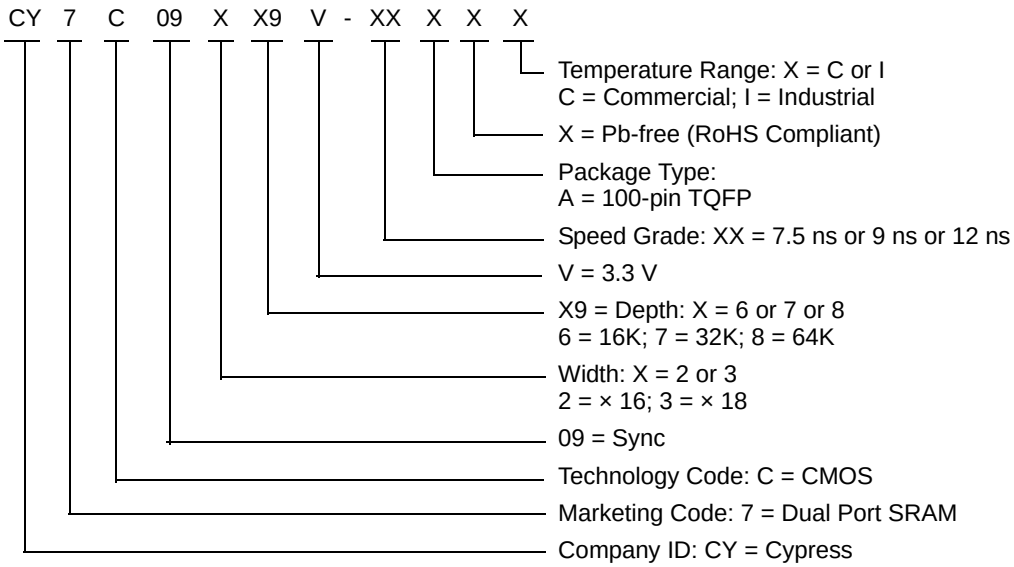
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 12 | CY7C09369V-12AXC | 51-85048 | 100-pin TQFP (Pb-free) | Commercial |

### 64K × 18 3.3 V Synchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 9 | CY7C09389V-9AI | 51-85048 | 100-pin TQFP | Industrial |

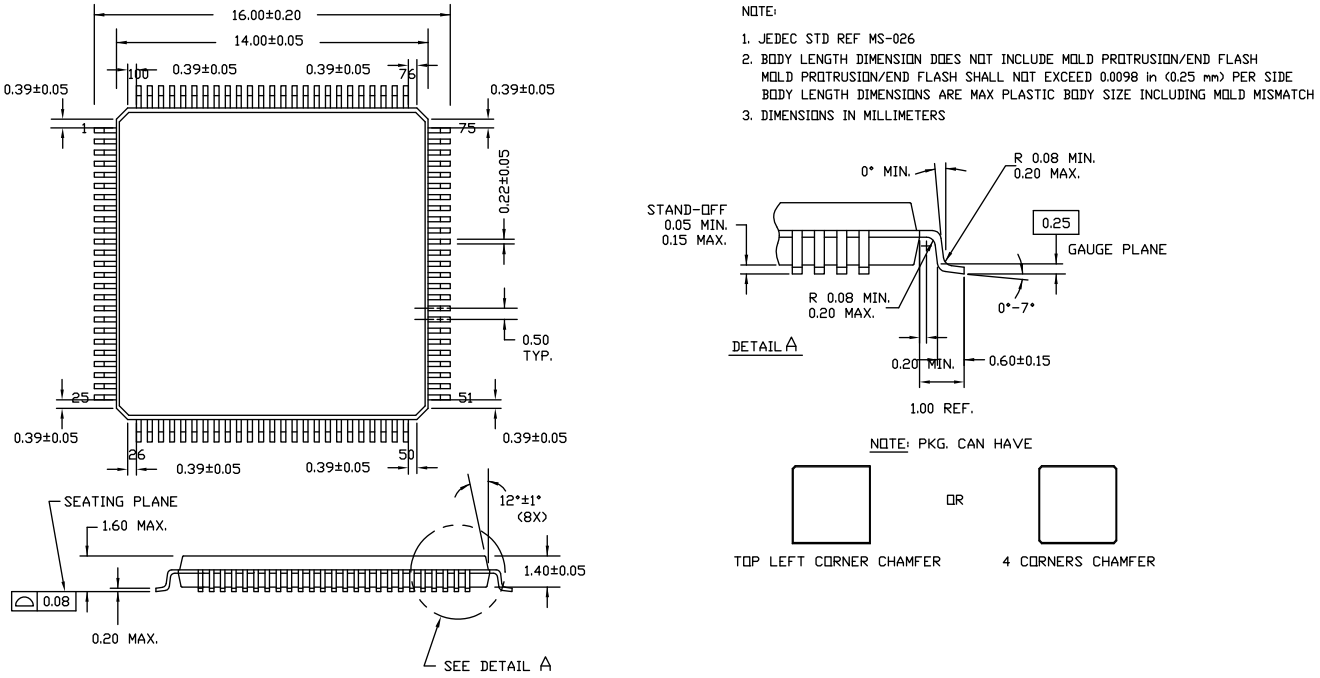
**Note**
59. See page 6 for Load Conditions.

## Ordering Code Definitions



## Package Diagrams

**Figure 17. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048**




51-85048 *J

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |

## Document History Page

| Document Title: CY7C09269V/79V/89V/CY7C09369V/89V, 3.3 V 16K / 32K / 64K × 16 / 18 Synchronous Dual-Port Static RAM<br>Document Number: 38-06056 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 110215 | 12/18/01 | SZV | Change from Spec number: 38-00668 to 38-06056 |
| *A | 122306 | 12/27/02 | RBI | Updated Maximum Ratings:<br>Added Power up requirements. |
| *B | 344354 | See ECN | PCX | Updated Ordering Information (Added Pb-Free Parts). |
| *C | 2678221 | 03/25/2009 | VKN / AESA | Updated Ordering Information (Added CY7C09379V-12AXCT part).<br>Updated Package Diagrams (updated spec 51-85048 to *C). |
| *D | 2896210 | 03/22/2010 | RAME | Updated Ordering Information.<br>Updated Package Diagrams. |
| *E | 3111417 | 12/15/2010 | ADMU | Updated Ordering Information.<br>Added Ordering Code Definitions. |
| *F | 3124048 | 12/30/2010 | ADMU | No technical updates. |
| *G | 3352110 | 08/23/2011 | ADMU | Updated Features (Removed CY7C09379V information and also removed -6 speed bin information).<br>Updated Pin Configurations (Removed CY7C09379V information).<br>Updated Selection Guide (Removed CY7C09379V information and also removed -6 speed bin information).<br>Updated Functional Overview (Removed CY7C09379V information).<br>Updated Electrical Characteristics (Removed CY7C09379V information and also removed -6 speed bin information).<br>Updated AC Test Loads and Waveforms (Removed -6 speed bin information).<br>Updated Switching Characteristics (Removed CY7C09379V information and also removed -6 speed bin information).<br>Updated Ordering Information (Removed part CY7C09279V-7AC).<br>Updated Package Diagrams.<br>Added Acronyms and Units of Measure.<br>Updated to new template. |
| *H | 3402091 | 10/12/2011 | ADMU | Updated Ordering Information (Removed pruned part CY7C09289V-9AI).<br>Updated Package Diagrams. |
| *I | 3680923 | 08/01/2012 | ADMU / SMCH | Updated Pin Configurations (Updated Figure 2).<br>Updated Switching Characteristics (Changed name of parameter from $t_{CKZ}$ to $t_{CKHZ}$, changed name of parameter from $t_{CKZ}$ to $t_{CKLZ}$ in the next corresponding row).<br>Updated Switching Waveforms (Updated Figure 15).<br>Updated Address Counter Control Operation.<br>Updated Ordering Information (Removed pruned part CY7C09289V-9AC).<br>Updated Package Diagrams (spec 51-85048 (Changed revision from *E to *G)). |
| *J | 3859909 | 01/07/2013 | SMCH | Updated Ordering Information (Updated part numbers). |
| *K | 4580622 | 11/27/2014 | SMCH | Updated Functional Description:<br>Added “For a complete list of related documentation, click here.” at the end.<br>Updated Package Diagrams:<br>spec 51-85048 – Changed revision from *G to *I. |
| *L | 4918880 | 09/14/2015 | VINI | Updated Ordering Information (Updated part numbers).<br>Updated to new template.<br>Completing Sunset Review. |

## Document History Page (continued)

| Document Title: CY7C09269V/79V/89V/CY7C09369V/89V, 3.3 V 16K / 32K / 64K × 16 / 18 Synchronous Dual-Port Static RAM<br>Document Number: 38-06056 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| *M | 5183282 | 03/21/2016 | VINI | Updated Pin Configurations:<br>Updated Figure 1 (Fixed typo error in pin number 50).<br>Updated Package Diagrams:<br>spec 51-85048 – Changed revision from *I to *J.<br>Updated to new template.<br>Completing Sunset Review. |

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