

## Features

- Pin- and function-compatible with CY7C1019CV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low Active Power
  - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS Standby Power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0 V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- Available in Pb-free 32-pin 400-Mil wide Molded SOJ, 32-pin TSOP II and 48-ball VFBGA packages

## Functional Description

The CY7C1019DV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

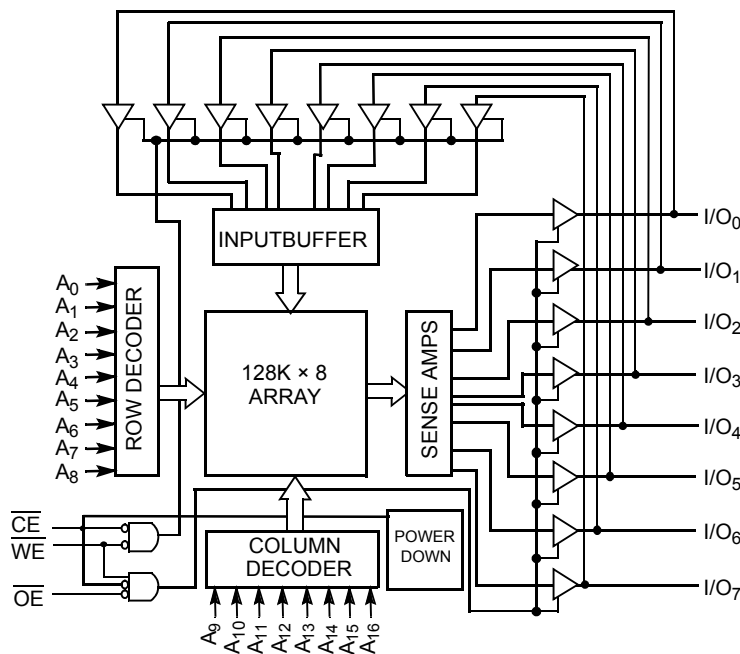
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1019DV33 is available in Pb-free 32-pin 400-Mil wide Molded SOJ, 32-pin TSOP II and 48-ball VFBGA packages.

## Logic Block Diagram



## Contents

<b>Selection Guide</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>11</b>
<b>Pin Configurations</b> .....	<b>3</b>	Ordering Code Definitions .....	11
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>12</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>14</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>14</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	14
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>15</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>16</b>
<b>Switching Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	16
<b>Data Retention Characteristics</b> .....	<b>7</b>	Products .....	16
<b>Data Retention Waveform</b> .....	<b>7</b>	PSoC Solutions .....	16
<b>Switching Waveforms</b> .....	<b>7</b>		
<b>Truth Table</b> .....	<b>10</b>		

### Selection Guide

	-10 (Industrial)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	60	mA
Maximum Standby Current	3	mA

### Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1 mm) (Top View) [1]

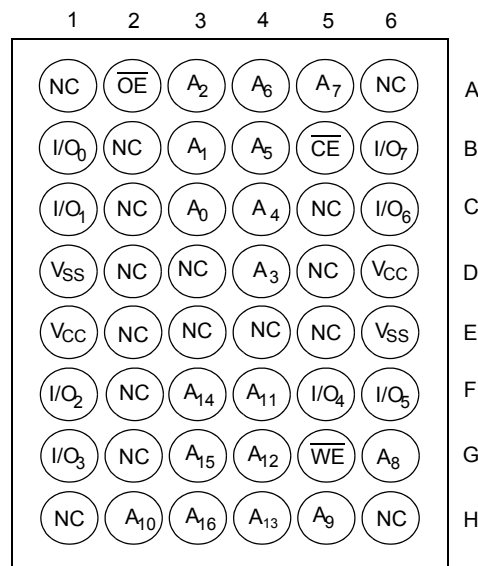
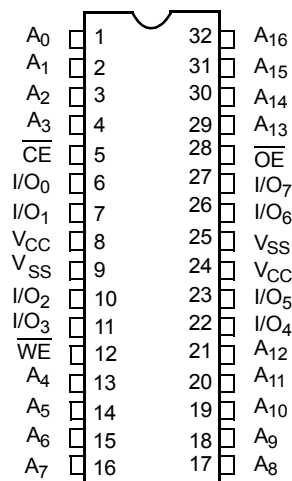


Figure 2. 32-pin SOJ / TSOP II (Top View)



**Note**

- 1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage on $V_{CC}$ to Relative GND <sup>[2]</sup> .....	-0.3 V to +4.6 V
DC Voltage Applied to Outputs in High Z State <sup>[2]</sup> .....	-0.3 V to $V_{CC} + 0.3$ V

DC Input Voltage <sup>[2]</sup> .....	-0.3 V to $V_{CC} + 0.3$ V
Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015) .....	> 2001 V
Latch-up Current .....	> 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$	Speed
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V	10 ns

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10 (Industrial)		Unit	
			Min	Max		
$V_{OH}$	Output HIGH voltage	Min $V_{CC}$ , $I_{OH} = -4.0$ mA	2.4	-	V	
$V_{OL}$	Output LOW voltage	Min $V_{CC}$ , $I_{OL} = 8.0$ mA	-	0.4	V	
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V	
$V_{IL}$	Input LOW voltage <sup>[2]</sup>		-0.3	0.8	V	
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	+1	μA	
$I_{OZ}$	Output leakage current	$GND \leq V_{IN} \leq V_{CC}$ , output disabled	-1	+1	μA	
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}$ , $I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{RC}$	100 MHz	-	60	mA
			83 MHz	-	55	mA
			66 MHz	-	45	mA
			40 MHz	-	30	mA
$I_{SB1}$	Automatic CE power-down current – TTL inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	-	10	mA	
$I_{SB2}$	Automatic CE power-down current – CMOS inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$	-	3	mA	

### Note

2.  $V_{IL(min)}$  = -2.0 V and  $V_{IH(max)}$  =  $V_{CC} + 1$  V for pulse durations of less than 5 ns.

### Capacitance

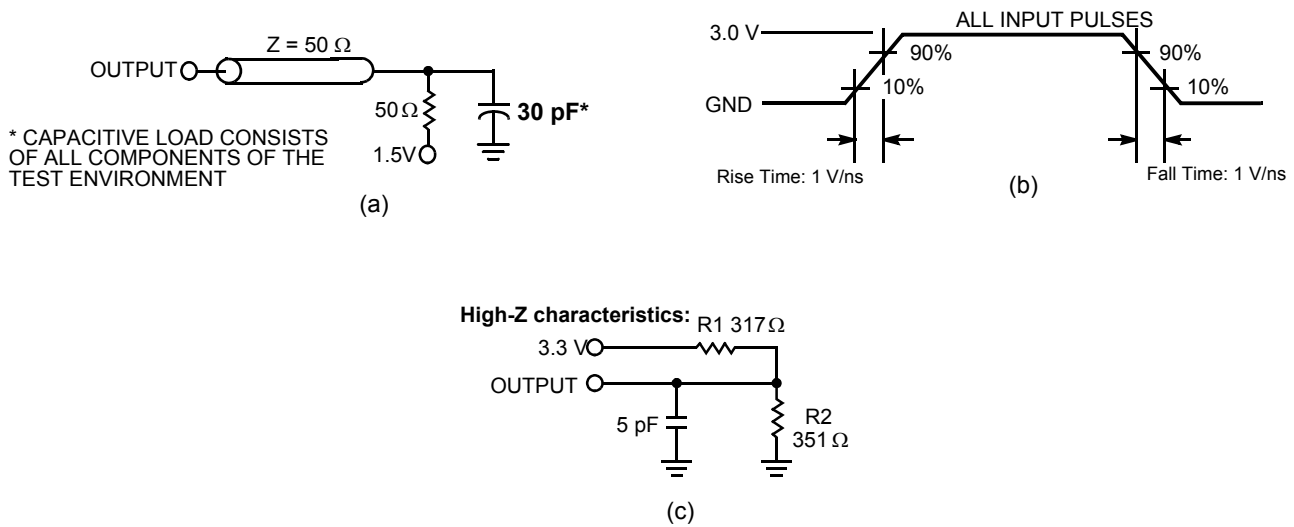
Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

### Thermal Resistance

Parameter <sup>[3]</sup>	Description	Test Conditions	32-pin SOJ	32-pin TSOP II	48-ball VFBGA	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	56.29	62.22	36	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		38.14	21.43	9	°C/W

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[4]</sup>



**Notes**

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

## Switching Characteristics

Over the Operating Range

Parameter <sup>[5]</sup>	Description	-10 (Industrial)		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}^{[6]}$	$V_{CC}$ (typical) to the first access	100	–	$\mu s$
$t_{RC}$	Read cycle time	10	–	ns
$t_{AA}$	Address to data valid	–	10	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[7]</sup>	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[7, 8]</sup>	–	5	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[7]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[7, 8]</sup>	–	5	ns
$t_{PU}^{[9]}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}^{[9]}$	$\overline{CE}$ HIGH to power-down	–	10	ns
<b>Write Cycle <sup>[10, 11]</sup></b>				
$t_{WC}$	Write cycle time	10	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	8	–	ns
$t_{AW}$	Address set-up to write end	8	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address set-up to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	ns
$t_{SD}$	Data set-up to write end	5	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[7]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[7, 8]</sup>	–	5	ns

### Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
6.  $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
7. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
8.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in [Figure 3 on page 5 \(c\)](#). Transition is measured when the outputs enter a high impedance state.
9. This parameter is guaranteed by design and is not tested.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

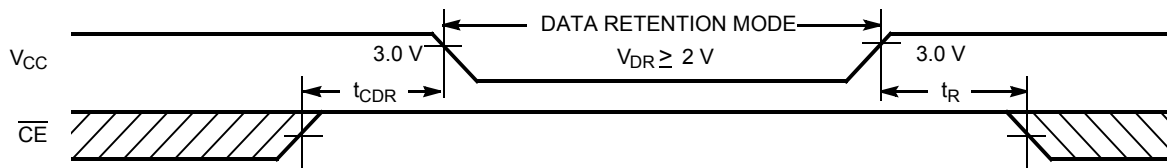
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[12]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[13]}$	Operation recovery time		$t_{RC}$	–	ns

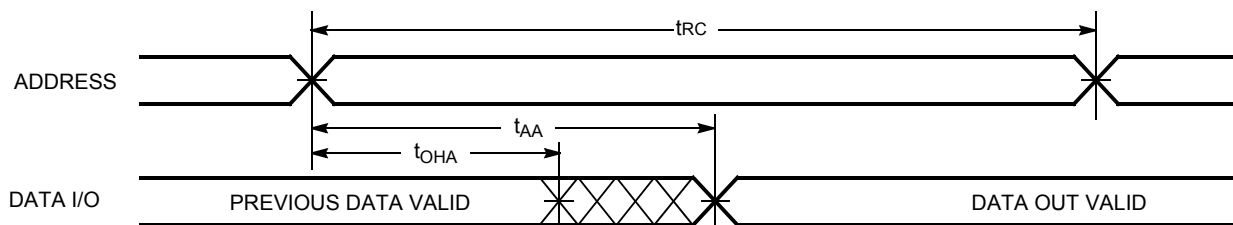
## Data Retention Waveform

Figure 4. Data Retention Waveform



## Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) <sup>[14, 15]</sup>



### Notes

- 12. Tested initially and after any design or process changes that may affect these parameters.
- 13. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min.)} \geq 50\ \mu\text{s}$ .
- 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- 15. WE is HIGH for Read cycle.

Switching Waveforms (continued)

Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [16, 17]

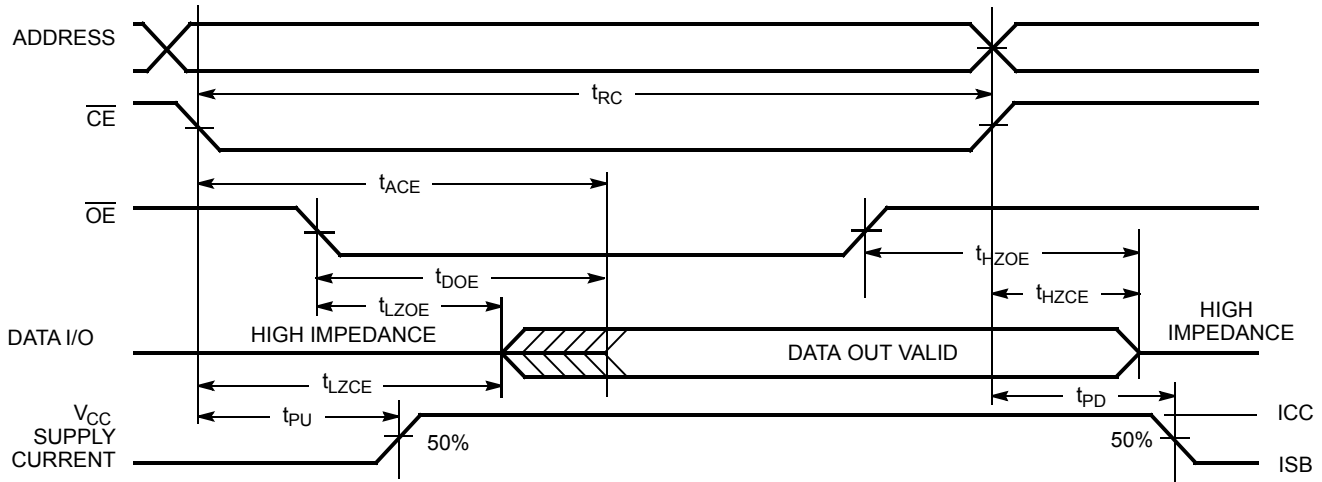
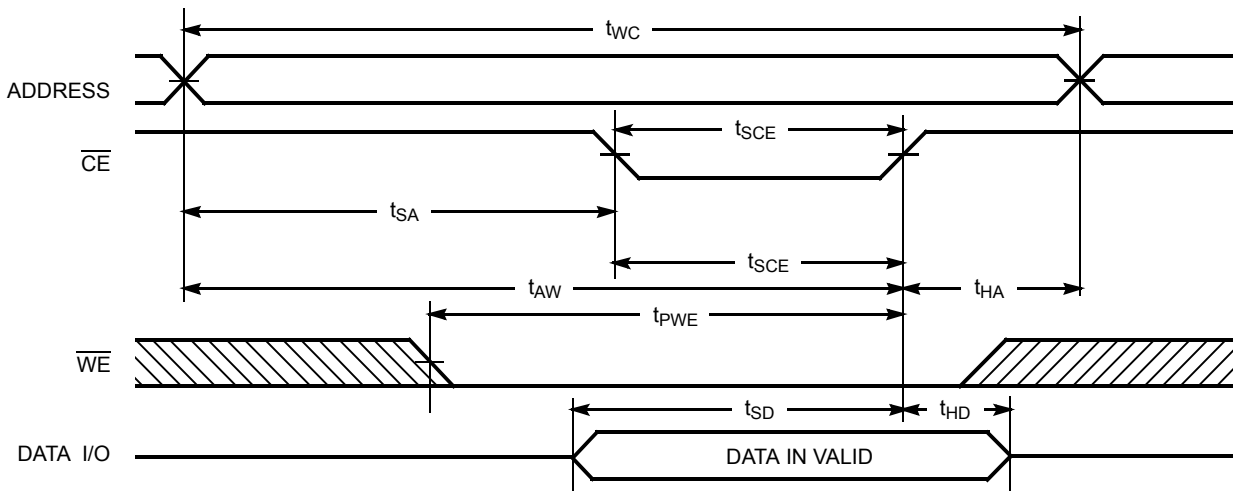


Figure 7. Write Cycle No. 1 ( $\overline{CE}$  Controlled) [18, 19]



Notes

- 16.  $\overline{WE}$  is HIGH for Read cycle.
- 17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 18. Data I/O is high impedance if  $OE = V_{IH}$ .
- 19. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write) [20, 21]

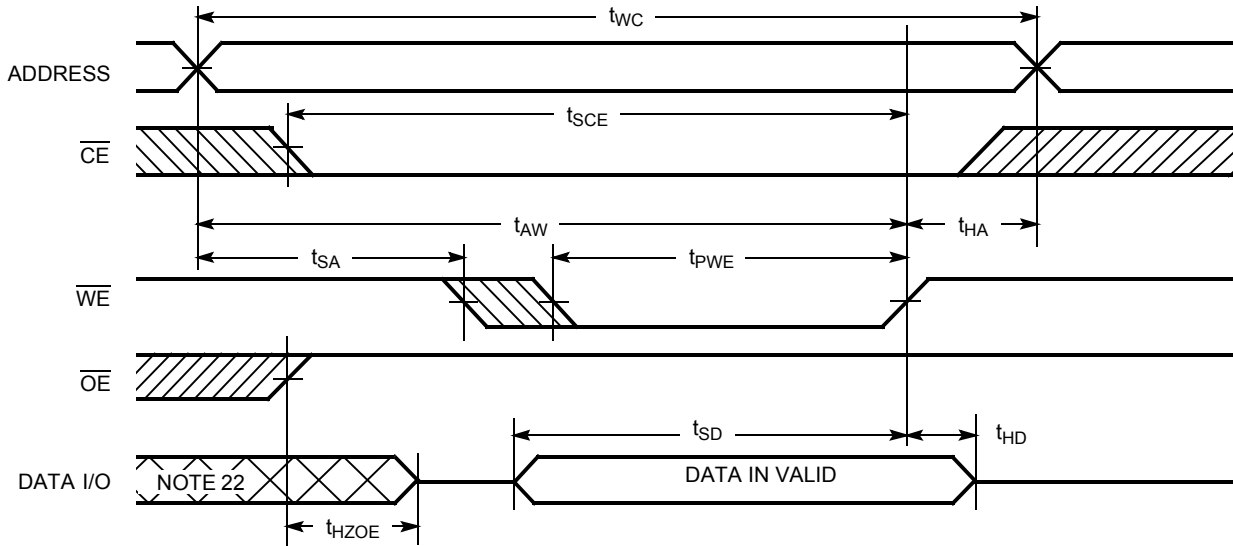
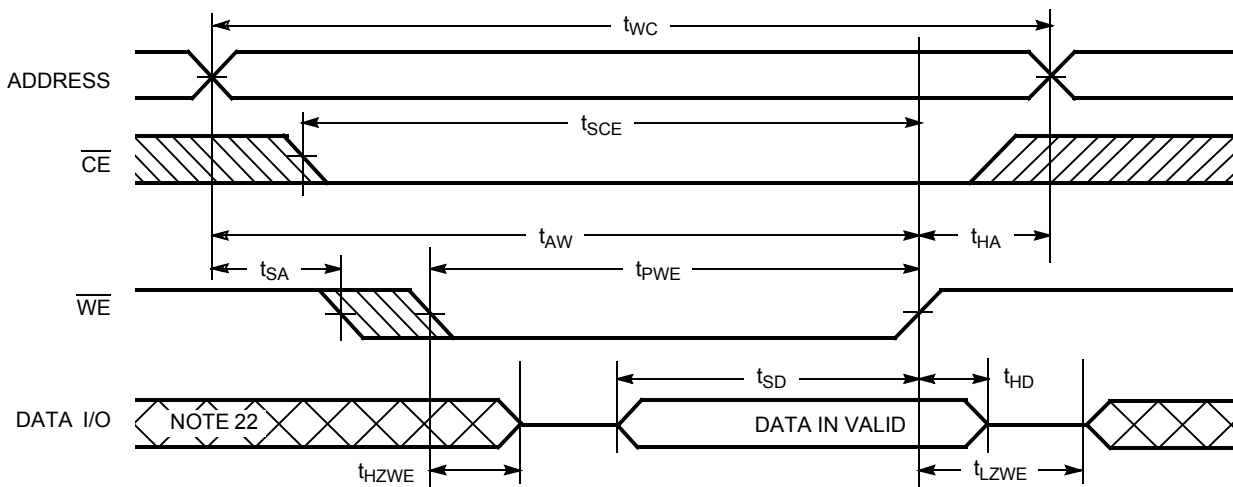


Figure 9. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [21, 23]



Notes

- 20. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 21. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 22. During this period the I/Os are in the output state and input signals should not be applied.
- 23. The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

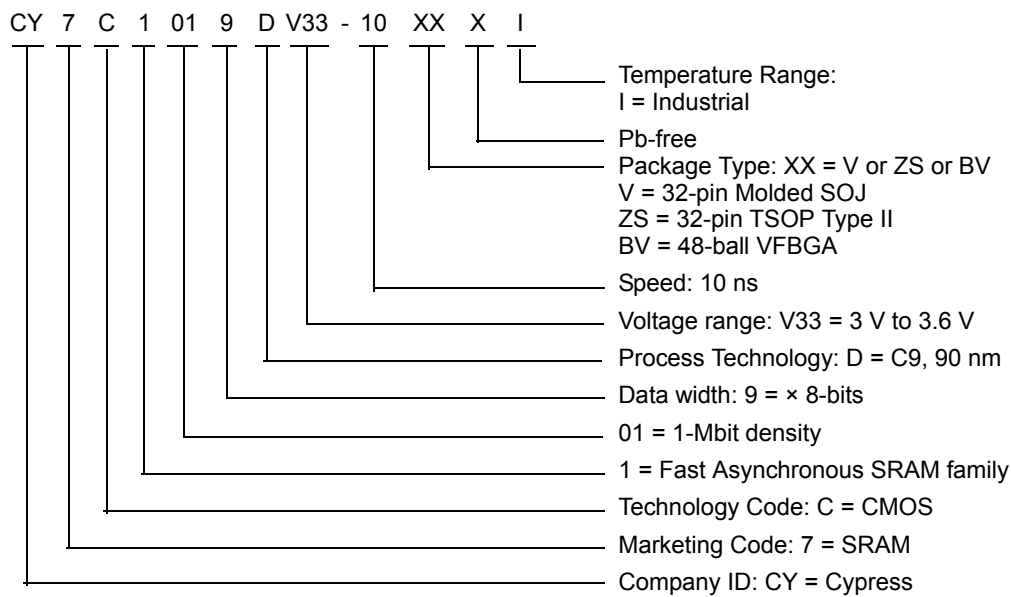
**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1019DV33-10VXI	51-85033	32-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1019DV33-10ZSXI	51-85095	32-pin TSOP Type II (Pb-free)	
	CY7C1019DV33-10BVXI	51-85150	48-ball VFBGA (Pb-free)	

**Ordering Code Definitions**



Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

Figure 10. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033

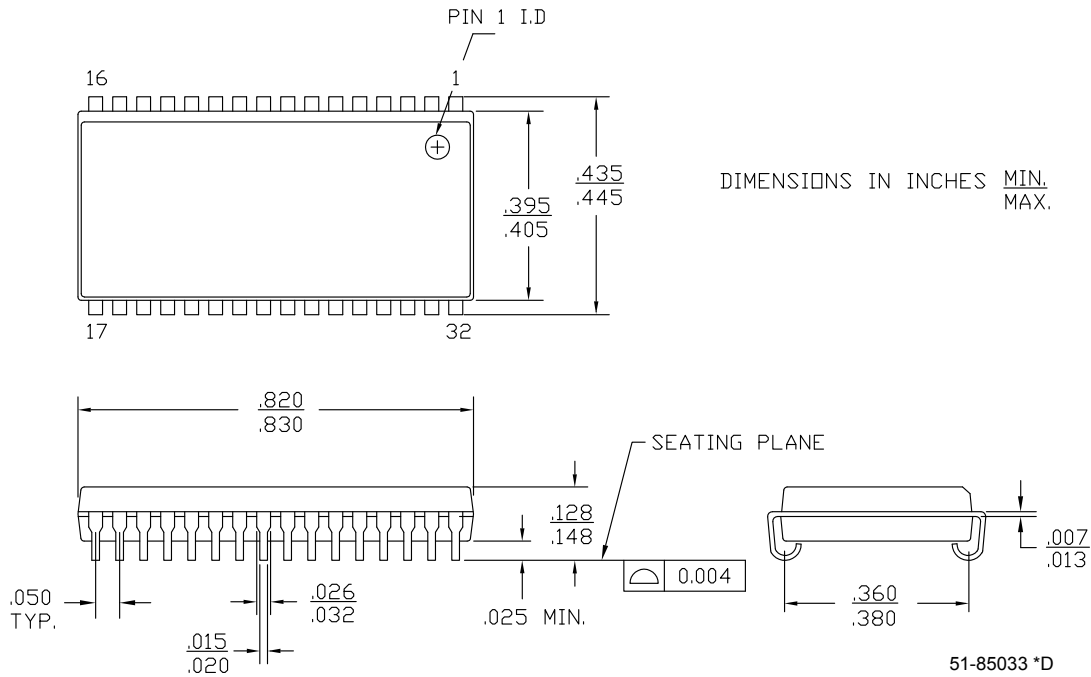
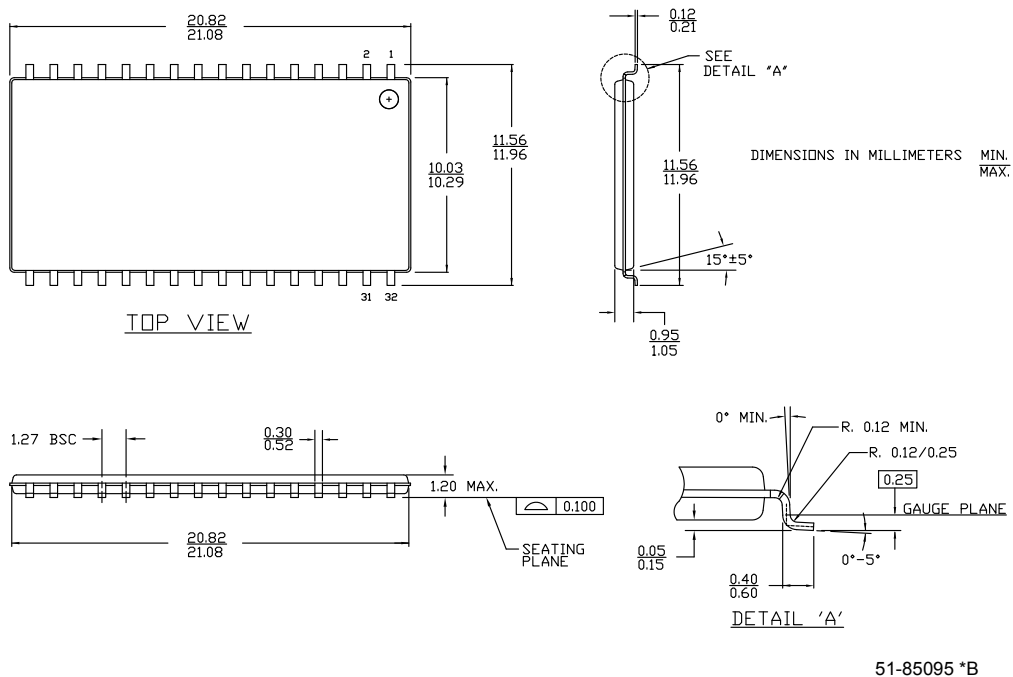
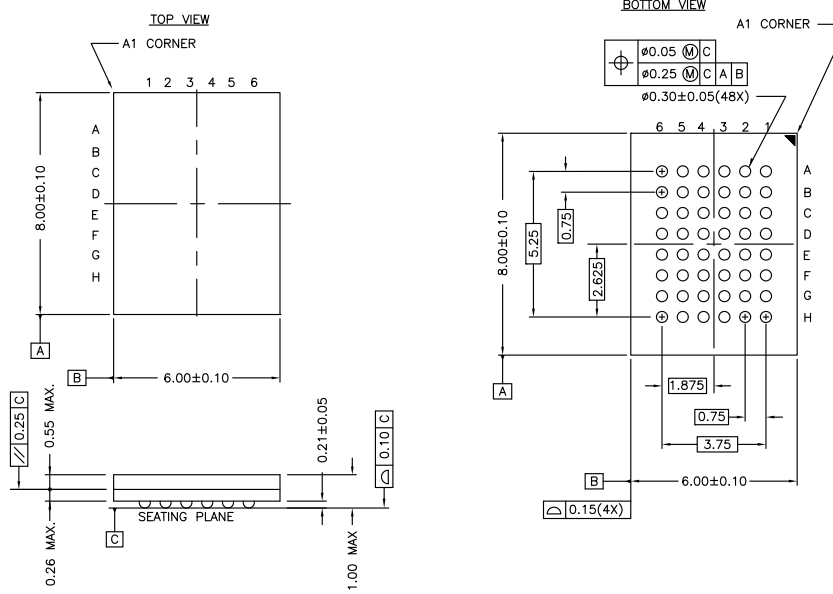


Figure 11. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



Package Diagrams (continued)

Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



51-85150 \*G

### Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball gird array
$\overline{WE}$	write enable

### Document Conventions

#### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1019DV33, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05481				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233750	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165 Rev *A) Pb-free Offering in Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics table Shaded Ordering Information
*C	307598	See ECN	RKF	Reduced Speed bins to -8 and -10 ns
*D	520652	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 8 ns speed bin Added I <sub>CC</sub> values for the frequencies 83 MHz, 66 MHz and 40 MHz Added 48-ball VFBGA package Updated Thermal Resistance table Updated Ordering Information table Changed Overshoot spec from V <sub>CC</sub> + 2 V to V <sub>CC</sub> + 1 V in footnote #3
*E	3110052	12/14/2010	AJU	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*F	3416342	10/20/2011	TAVA	Updated <a href="#">Functional Description</a> (Removed the Note “For guidelines on SRAM system design, please refer to the ‘System Design Guidelines’ Cypress application note, available on the internet at <a href="http://www.cypress.com">www.cypress.com</a> .” and its reference in <a href="#">Functional Description</a> ). Updated <a href="#">Electrical Characteristics</a> . Updated <a href="#">Switching Waveforms</a> . Updated <a href="#">Package Diagrams</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.

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[IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#) [70V639S10BCG](#) [IS66WVE4M16EALL-70BLI](#) [IS62WV6416DBLL-45BLI](#)  
[IS61WV102416DBLL-10TLI](#) [CY7C1381KV33-100AXC](#) [CY7C1381KVE33-133AXI](#) [8602501XA](#) [5962-3829425MUA](#) [5962-3829430MUA](#)  
[5962-8855206YA](#) [5962-8866201YA](#) [5962-8866204TA](#) [5962-8866206MA](#) [5962-8866208UA](#) [5962-8872502XA](#) [5962-9062007MXA](#) [5962-](#)  
[9161705MXA](#) [70V3579S6BFI](#) [GS882Z18CD-150I](#) [M38510/28902BVA](#) [8413202RA](#) [5962-9161708MYA](#) [5962-8971203XA](#) [5962-](#)  
[8971202ZA](#) [5962-8872501LA](#) [5962-8866208YA](#) [5962-8866205YA](#) [5962-8866205UA](#) [5962-8866203YA](#) [5962-8855202YA](#)