

512-Kbit (32 K × 16) Static RAM

Features

- Pin- and function-compatible with CY7C1020B
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low complementary metal oxide semiconductor (CMOS) standby power
 - $I_{SB2} = 3 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin thin small outline package (TSOP) II packages

Functional Description

The CY7C1020D [1] is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The input and output pins (IO₀ through IO₁₅) are placed in a high-impedance state when:

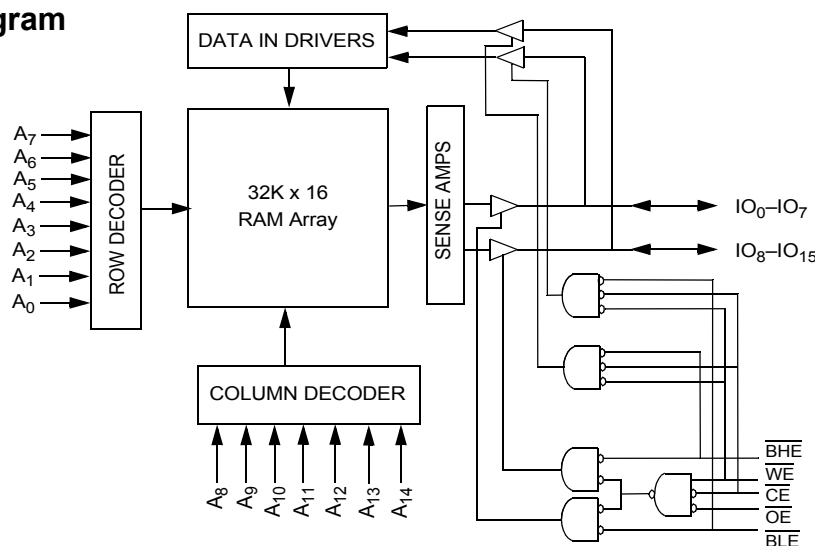
- Deselected (\overline{CE} HIGH)
 - Outputs are disabled (\overline{OE} HIGH)
 - \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH)
 - When the write operation is active (\overline{CE} LOW, and \overline{WE} LOW)
- Write to the device by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from IO pins (IO₀ through IO₇), is written into the location specified on the address pins (A₀ through A₁₄). If Byte High Enable (\overline{BHE}) is LOW, then data from IO pins (IO₈ through IO₁₅) is written into the location specified on the address pins (A₀ through A₁₄).

Reading from the device by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on IO₀ to IO₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on IO₈ to IO₁₅. See the "Truth Table" on page 11 for a complete description of read and write modes.

The CY7C1020D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Note

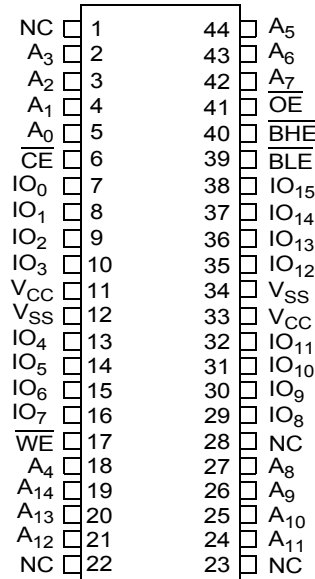
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

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Pin Configurations

Figure 1. 44-pin SOJ/TSOP II pinout (Top View) [2]



Selection Guide

| Description | -10 (Industrial) | Unit |
|------------------------------|------------------|------|
| Maximum access time | 10 | ns |
| Maximum operating current | 80 | mA |
| Maximum CMOS standby current | 3 | mA |

Note

2. NC pins are not connected on the die.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

| | |
|--|-----------------------------------|
| Storage temperature | -65 °C to +150 °C |
| Ambient temperature with power applied | -55 °C to +125 °C |
| Supply voltage on V _{CC} to Relative GND ^[3] | -0.5 V to +6.0 V |
| DC voltage applied to outputs in High Z State ^[3] | -0.5 V to V _{CC} + 0.5 V |

| | |
|---|-----------------------------------|
| DC input voltage ^[3] | -0.5 V to V _{CC} + 0.5 V |
| Current into outputs (LOW) | 20 mA |
| Static discharge voltage (per MIL-STD-883, Method 3015) | >2001 V |
| Latch-up current | >200 mA |

Operating Range

| Range | Ambient Temperature | V _{CC} | Speed |
|------------|---------------------|-----------------|-------|
| Industrial | -40 °C to +85 °C | 5 V ± 0.5 V | 10 ns |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | -10 (Industrial) | | Unit | |
|------------------|---|---|------------------|-----------------------|------|----|
| | | | Min | Max | | |
| V _{OH} | Output HIGH voltage | I _{OH} = -4.0 mA | 2.4 | - | V | |
| | | I _{OH} = -0.1 mA | - | 3.4 ^[4] | | |
| V _{OL} | Output LOW voltage | I _{OL} = 8.0 mA | - | 0.4 | V | |
| V _{IH} | Input HIGH voltage | - | 2.2 | V _{CC} + 0.5 | V | |
| V _{IL} | Input LOW voltage ^[3] | - | -0.5 | 0.8 | V | |
| I _{IX} | Input load current | GND ≤ V _I ≤ V _{CC} | -1 | +1 | μA | |
| I _{OZ} | Output leakage current | GND ≤ V _I ≤ V _{CC} , output disabled | -1 | +1 | μA | |
| I _{CC} | V _{CC} operating supply current | V _{CC} = Max, I _{OUT} = 0 mA, f = f _{max} = 1/t _{RC} | 100 MHz | - | 80 | mA |
| | | | 83 MHz | - | 72 | mA |
| | | | 66 MHz | - | 58 | mA |
| | | | 40 MHz | - | 37 | mA |
| I _{SB1} | Automatic CE power-down current – TTL inputs | Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{max} | - | 10 | mA | |
| I _{SB2} | Automatic CE Power-Down current – CMOS inputs | Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3 V$, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0 | - | 3 | mA | |

Note

- V_{IL} (min) = -2.0 V and V_{IH} (max) = V_{CC} + 1 V for pulse durations of less than 5 ns.
- Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5V. If you are interfacing this SRAM with 5V legacy processors that require a minimum V_{IH} of 3.5V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

Capacitance

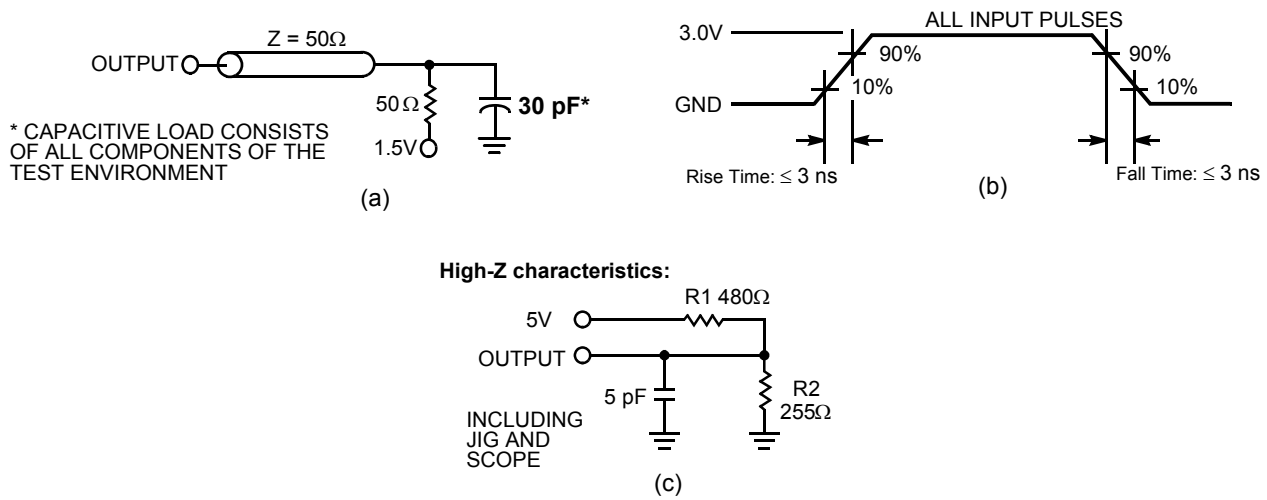
| Parameter ^[5] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V | 8 | pF |
| C _{OUT} | Output capacitance | | 8 | pF |

Thermal Resistance

| Parameter ^[5] | Description | Test Conditions | SOJ | TSOP II | Unit |
|--------------------------|--|---|-------|---------|------|
| θ _{JA} | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 59.52 | 53.91 | °C/W |
| θ _{JC} | Thermal resistance (junction to case) | | 36.75 | 21.24 | °C/W |

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[6]



Notes

- 5. Tested initially and after any design or process changes that may affect these parameters.
- 6. AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

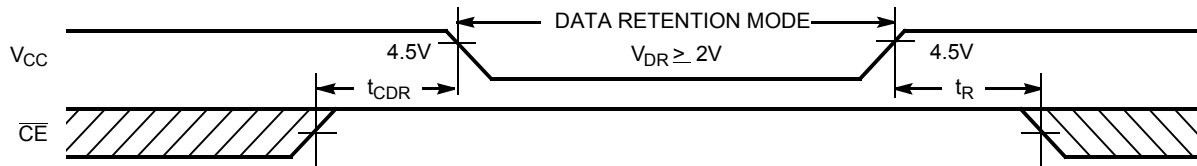
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Max | Unit |
|-----------------|--------------------------------------|--|----------|-----|------|
| V_{DR} | V_{CC} for data retention | – | 2.0 | – | V |
| I_{CCDR} | Data retention current | $V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | – | 3 | mA |
| $t_{CDR}^{[7]}$ | Chip deselect to data retention time | – | 0 | – | ns |
| $t_R^{[8]}$ | Operation recovery time | – | t_{RC} | – | ns |

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\min)} \geq 50\ \mu\text{s}$ or stable at $V_{CC(\min)} \geq 50\ \mu\text{s}$.

Switching Characteristics

Over the Operating Range

| Parameter ^[9] | Description | -10 (Industrial) | | Unit |
|--|--|------------------|-----|---------|
| | | Min | Max | |
| Read Cycle | | | | |
| $t_{power}^{[10]}$ | V_{CC} (typical) to the first access | 100 | – | μ s |
| t_{RC} | Read cycle time | 10 | – | ns |
| t_{AA} | Address to data valid | – | 10 | ns |
| t_{OHA} | Data hold from address change | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to data valid | – | 10 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 5 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[12] | 0 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[11, 12] | – | 5 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[12] | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[11, 12] | – | 5 | ns |
| $t_{PU}^{[13]}$ | \overline{CE} LOW to power-up | 0 | – | ns |
| $t_{PD}^{[13]}$ | \overline{CE} HIGH to power-down | – | 10 | ns |
| t_{DBE} | Byte enable to data valid | – | 5 | ns |
| t_{LZBE} | Byte enable to Low Z | 0 | – | ns |
| t_{HZBE} | Byte disable to High Z | – | 5 | ns |
| Write Cycle ^[14, 15] | | | | |
| t_{WC} | Write cycle time | 10 | – | ns |
| t_{SCE} | \overline{CE} LOW to write end | 7 | – | ns |
| t_{AW} | Address set-up to write end | 7 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| t_{SA} | Address set-up to write start | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 7 | – | ns |
| t_{SD} | Data set-up to write end | 6 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[12] | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[11, 12] | – | 5 | ns |
| t_{BW} | Byte enable to end of write | 7 | – | ns |

Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
10. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
11. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
13. This parameter is guaranteed by design and is not tested.
14. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
15. The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No.1 (Address Transition Controlled) [16, 17]

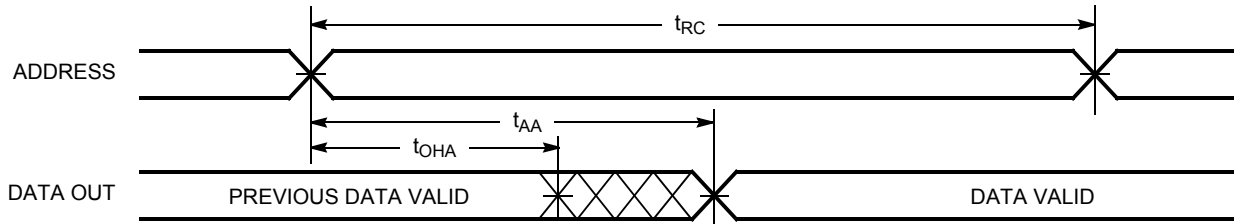
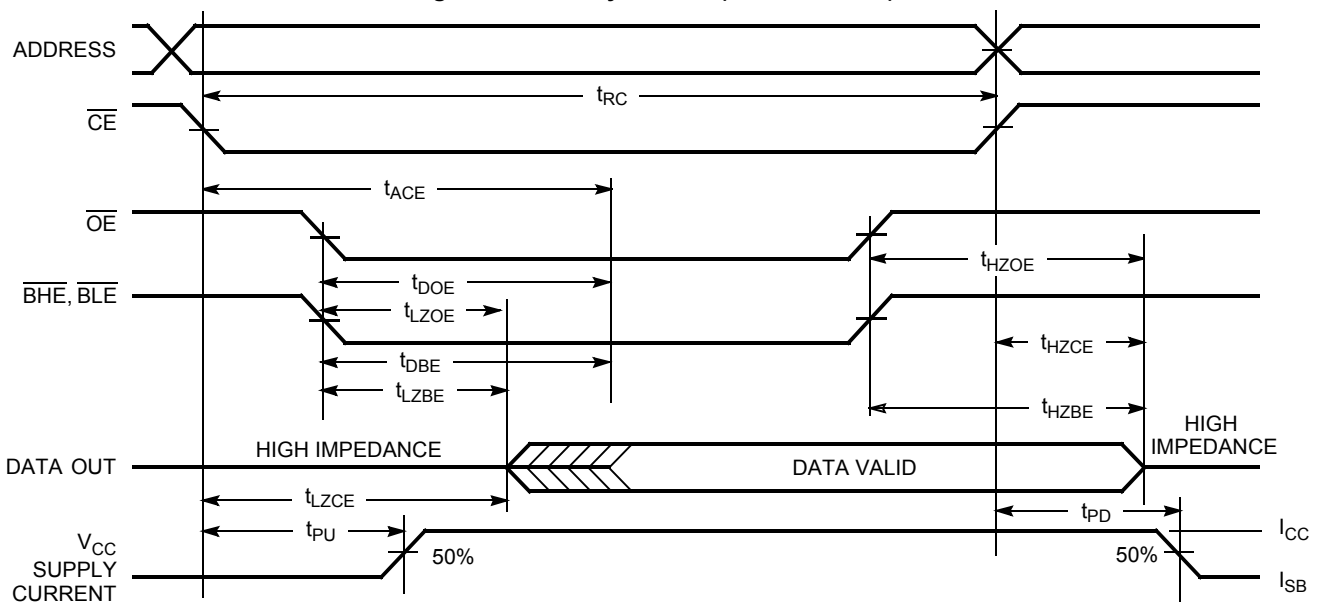


Figure 5. Read Cycle No.2 (\overline{OE} Controlled) [17, 18]



Notes

- 16. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
- 17. \overline{WE} is HIGH for read cycle.
- 18. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [19, 20]

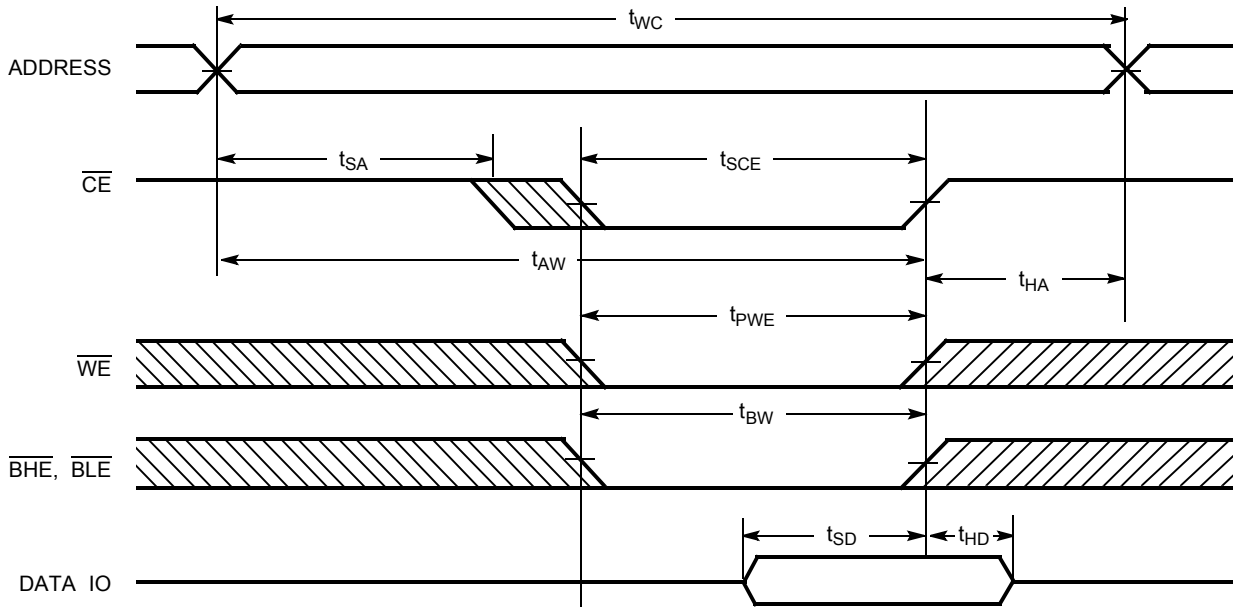
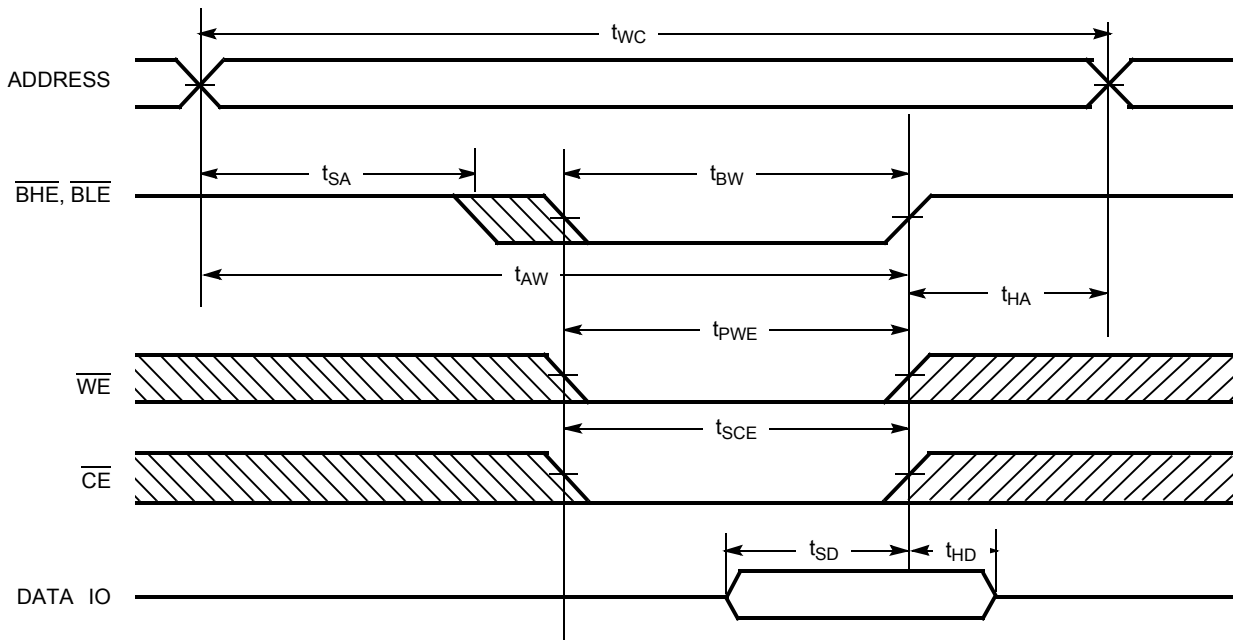


Figure 7. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled) [19, 20]

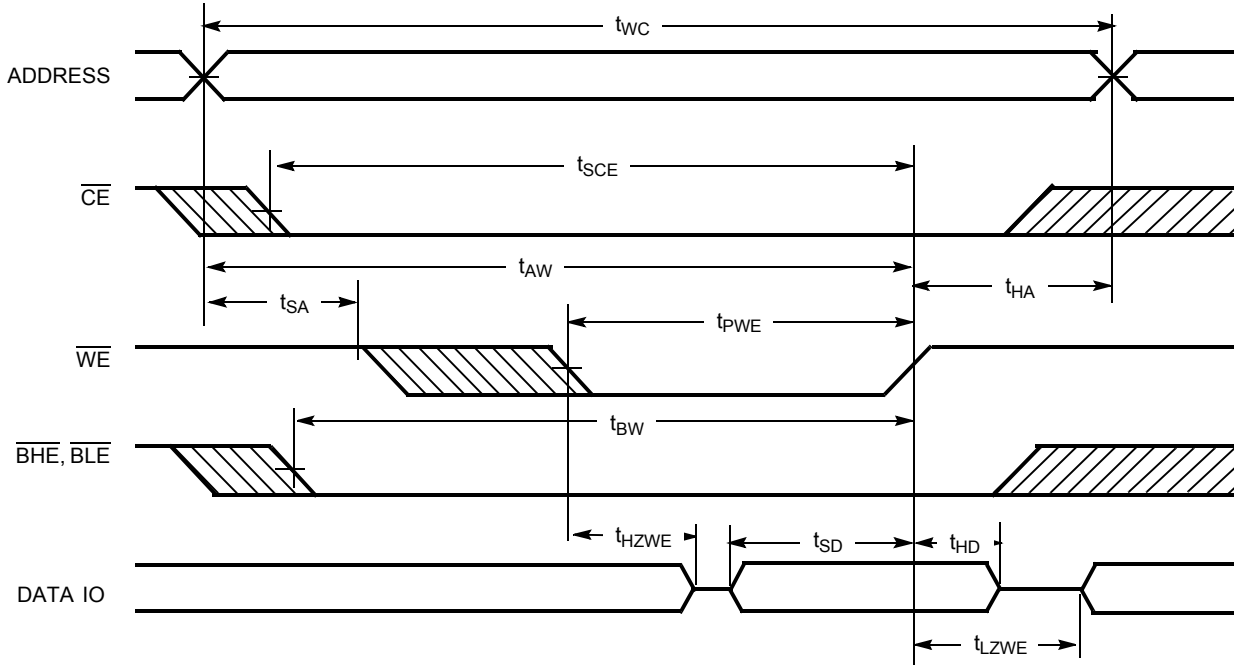


Notes

- 19. Data IO is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
- 20. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms(continued)

Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [21, 22]



Notes

- 21. The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .
- 22. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Truth Table

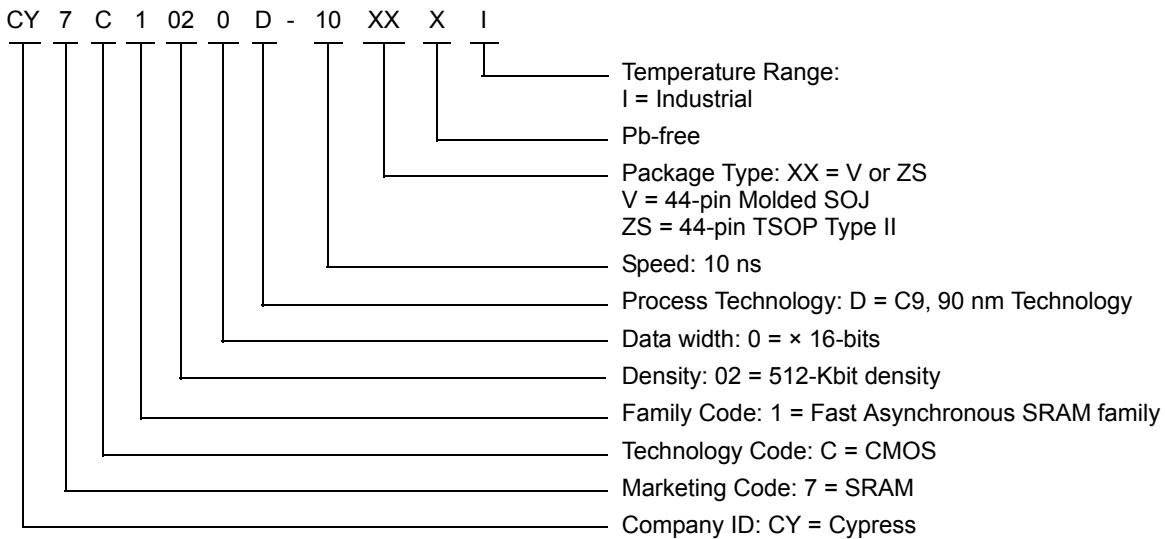
| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | IO_0 - IO_7 | IO_8 - IO_{15} | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|-----------------|--------------------|----------------------------|----------------------|
| H | X | X | X | X | High Z | High Z | Power-down | Standby (I_{SB}) |
| L | L | H | L | L | Data out | Data out | Read – All bits | Active (I_{CC}) |
| | | | L | H | Data out | High Z | Read – Lower bits only | Active (I_{CC}) |
| | | | H | L | High Z | Data out | Read – Upper bits only | Active (I_{CC}) |
| L | X | L | L | L | Data in | Data in | Write – All bits | Active (I_{CC}) |
| | | | L | H | Data in | High Z | Write – Lower bits only | Active (I_{CC}) |
| | | | H | L | High Z | Data in | Write – Upper bits only | Active (I_{CC}) |
| L | H | H | X | X | High Z | High Z | Selected, outputs disabled | Active (I_{CC}) |
| L | X | X | H | H | High Z | High Z | selected, outputs disabled | Active (I_{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|------------------|-----------------|-------------------------------|-----------------|
| 10 | CY7C1020D-10VXI | 51-85082 | 44-pin SOJ (400 Mils) Pb-free | Industrial |
| | CY7C1020D-10ZSXI | 51-85087 | 44-pin TSOP (Type II) Pb-free | |

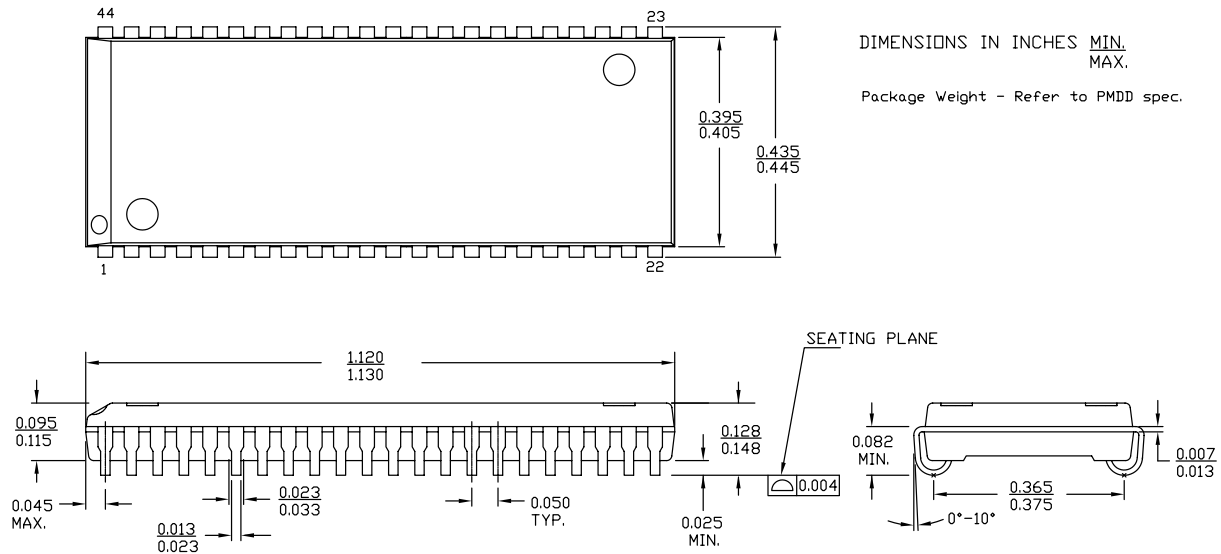
Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

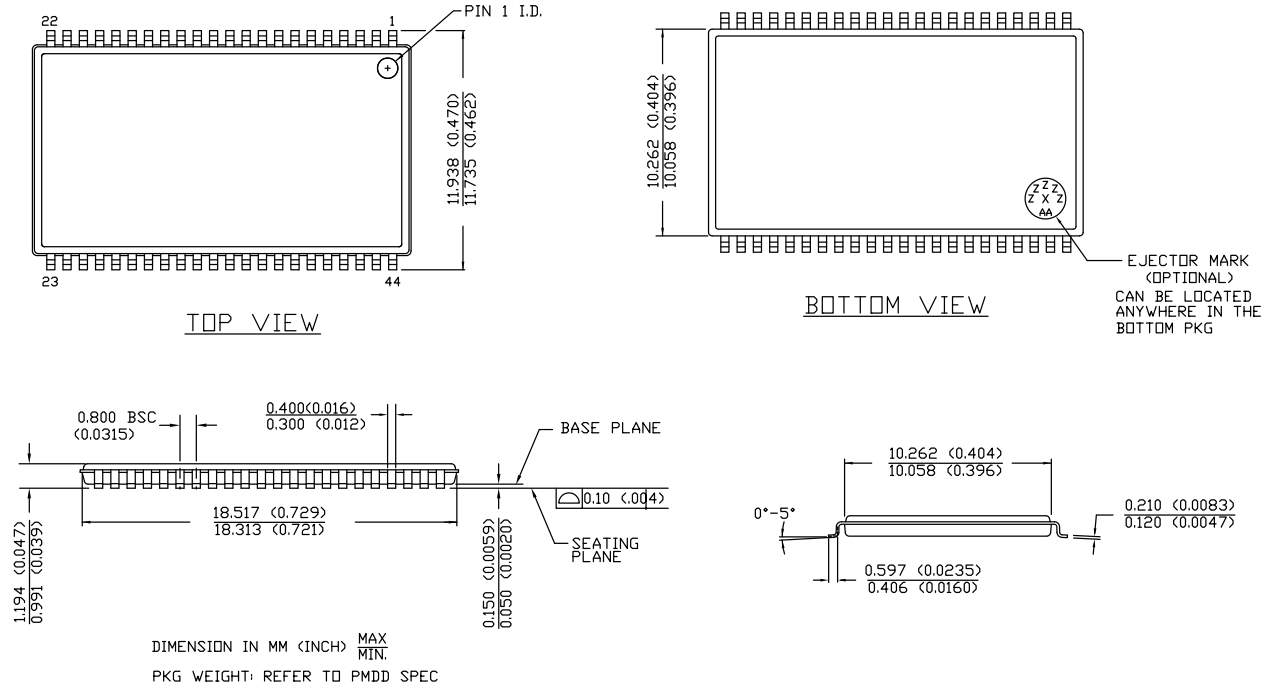
Figure 9. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



51-85082 *E

Package Diagrams(continued)

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

| Acronym | Description |
|---------|---|
| BGA | Ball Grid Array |
| CMOS | Complementary Metal Oxide Semiconductor |
| FBGA | Fine-Pitch Ball Grid Array |
| I/O | Input/Output |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| TTL | Transistor-Transistor Logic |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY7C1020D, 512-Kbit (32 K × 16) Static RAM Document Number: 38-05463 | | | | |
|---|---------|------------|-----------------|--|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 201560 | See ECN | SWI | Advance Data sheet for C9 IPP |
| *A | 233695 | See ECN | RKF | 1) DC parameters modified as per EROS (Spec # 01-0216) 2) Pb-free Offering in the 'Ordering Information' |
| *B | 263769 | See ECN | RKF | 1) Corrected pin #18 on SOJ/TSOPII Pinout (Page #1) from A ₁₅ to A ₄ 2) Changed IO ₁ - IO ₁₆ to IO ₀ - IO ₁₅ on the Pin-out diagram 3) Added T _{power} Spec in Switching Characteristics Table 4) Added Data Retention Characteristics Table and Waveforms 5) Shaded 'Ordering Information' |
| *C | 307594 | See ECN | RKF | Reduced Speed bins to -10, -12 and -15 ns |
| *D | 560995 | See ECN | VKN | Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #3 |
| *E | 802877 | See ECN | VKN | Changed I _{CC} specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz |
| *F | 3109992 | 12/14/2010 | AJU | Added Ordering Code Definitions . Updated Package Diagrams . |
| *G | 3219056 | 04/07/2011 | PRAS | Added TOC Added Acronyms and Units of Measure table. Updated Datasheet as per template. |
| *H | 4033925 | 06/19/2013 | MEMJ | Updated Functional Description . Updated Electrical Characteristics : Added one more Test Condition "I _{OH} = -0.1mA" for V _{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 4 and referred the same note in maximum value for V _{OH} parameter corresponding to Test Condition "I _{OH} = -0.1mA". Updated Package Diagrams : spec 51-85082 – Changed revision from *C to *E. spec 51-85087 – Changed revision from *C to *E. |
| *I | 4385769 | 05/21/2014 | MEMJ | No technical updates. Completing Sunset Review. |
| *J | 4576526 | 11/21/2014 | MEMJ | Added related documentation hyperlink in page 1. |

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[IDT70V5388S166BG](#) [IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#)
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[IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#) [IS66WVE4M16EALL-70BLI](#) [IS61WV102416DBLL-10TLI](#) [CY7C1381KV33-](#)
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[8866204TA](#) [5962-8866206MA](#) [5962-8866208UA](#) [5962-8872502XA](#) [5962-9062007MXA](#) [5962-9161705MXA](#) [GS882Z18CD-150I](#)
[M38510/28902BVA](#) [8413202RA](#) [5962-9161708MYA](#) [5962-8971203XA](#) [5962-8971202ZA](#) [5962-8872501LA](#) [5962-8866208YA](#) [5962-](#)
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