CY7C1021BNV33

64K × 16 Static RAM

Features

- 3.3 V operation (3.0 V–3.6 V)
- High speed
  - t_{AA} = 15 ns
- CMOS for optimum speed/power
- Low Active Power
  - 576 mW (max)
- Low CMOS Standby Power
  - 1.80 mW (max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 44-pin TSOP II and 48-ball Mini BGA package

Functional Description

The CY7C1021BNV33[1] is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

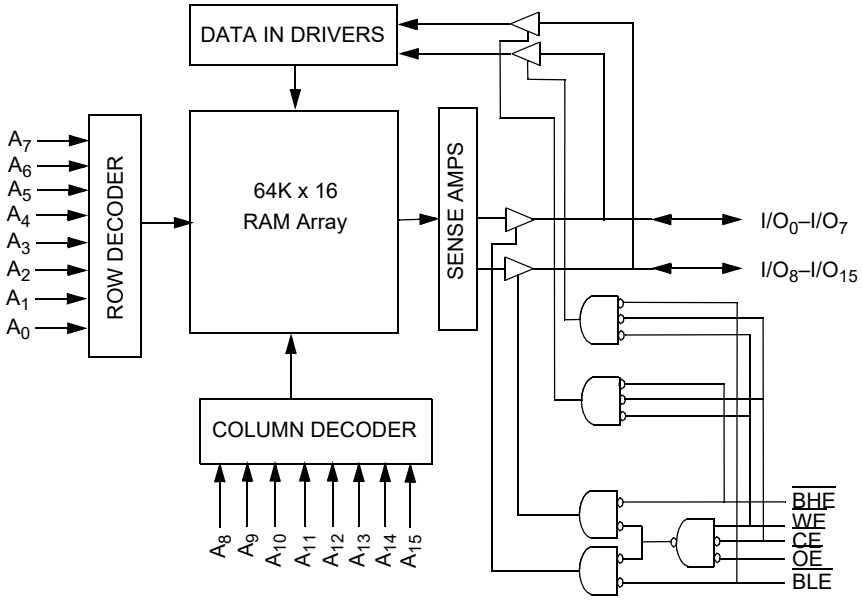
The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021BNV33 is available in standard 44-pin TSOP Type II and 48-ball mini BGA packages.

For a complete list of related documentation, click here.

Note
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Logic Block Diagram



Selection Guide

	-15
Maximum Access Time (ns)	15
Maximum Operating Current (mA)	160
Maximum CMOS Standby Current (mA)	0.5

Contents

Pin Configurations

Figure 1. 44-pin TSOP Type II pinout

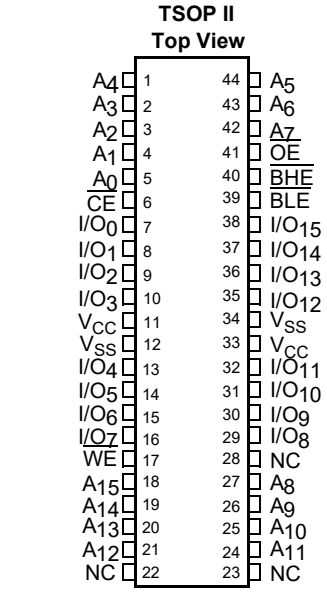
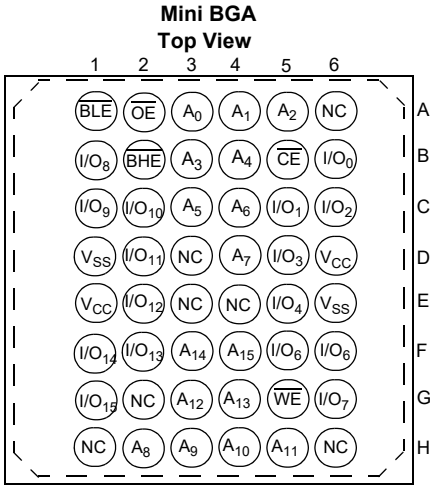


Figure 2. 48-ball mini BGA pinout



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} to Relative GND [2] .....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State [2] .....–0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2] .....–0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

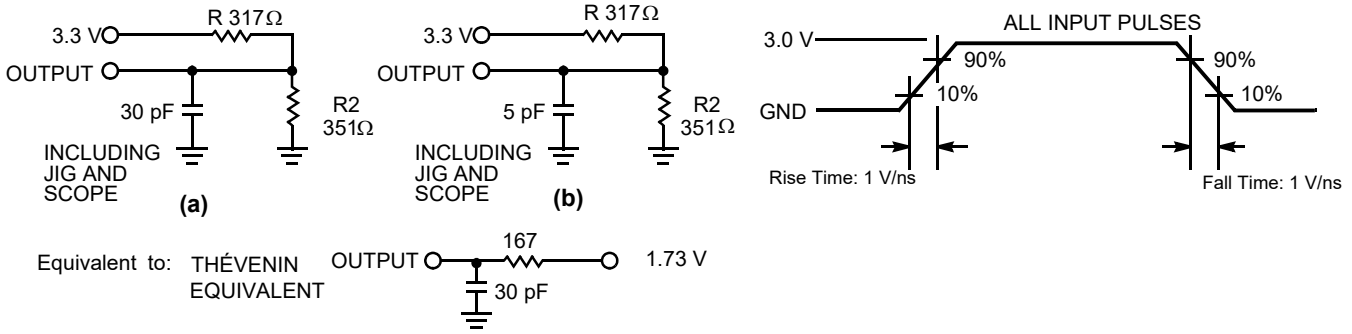
Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage [2]		–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	–	160	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	40	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0	–	500	µA

Capacitance

Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz	6	pF
C_{OUT}	Output capacitance		8	pF

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Notes
2. Minimum voltage is –2.0 V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

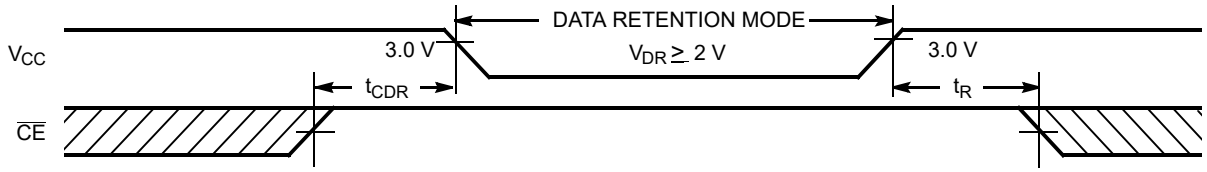
Data Retention Characteristics

Over the Operating Range (L version only)

Parameter	Description	Conditions [4]	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	100	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0	–	ns
t_R[6]	Operation Recovery Time		15	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes
4. No input may exceed V_{CC} + 0.5 V.
5. Tested initially and after any design or process changes that may affect these parameters.
6. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.

Switching Characteristics

Over the Operating Range

Parameter [7]	Description	-15		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read Cycle Time	15	–	ns
t_{AA}	Address to Data Valid	–	15	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [8, 9]	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [9]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [8, 9]	–	7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down	–	15	ns
t_{DBE}	Byte Enable to Data Valid	–	7	ns
t_{LZBE}	Byte Enable to Low Z	0	–	ns
t_{HZBE}	Byte Disable to High Z	–	7	ns
WRITE CYCLE [10, 11]				
t_{WC}	Write Cycle Time	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10	–	ns
t_{AW}	Address Set-Up to Write End	10	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-Up to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	10	–	ns
t_{SD}	Data Set-Up to Write End	8	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [9]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [8, 9]	–	7	ns
t_{BW}	Byte Enable to End of Write	9	–	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of Figure 3 on page 5. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write, and LOW to HIGH transition on any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 [12, 13]

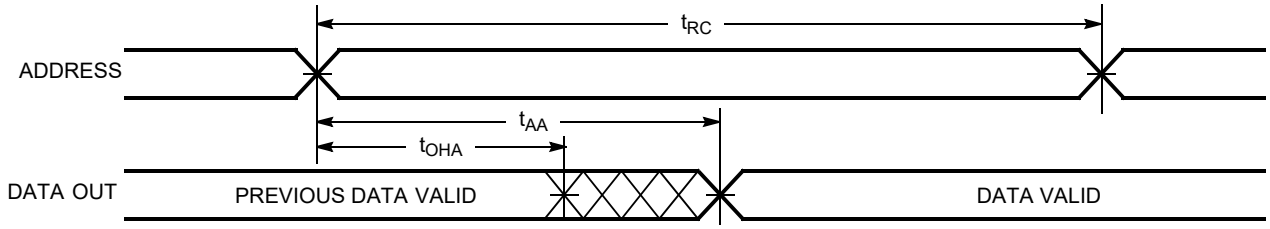
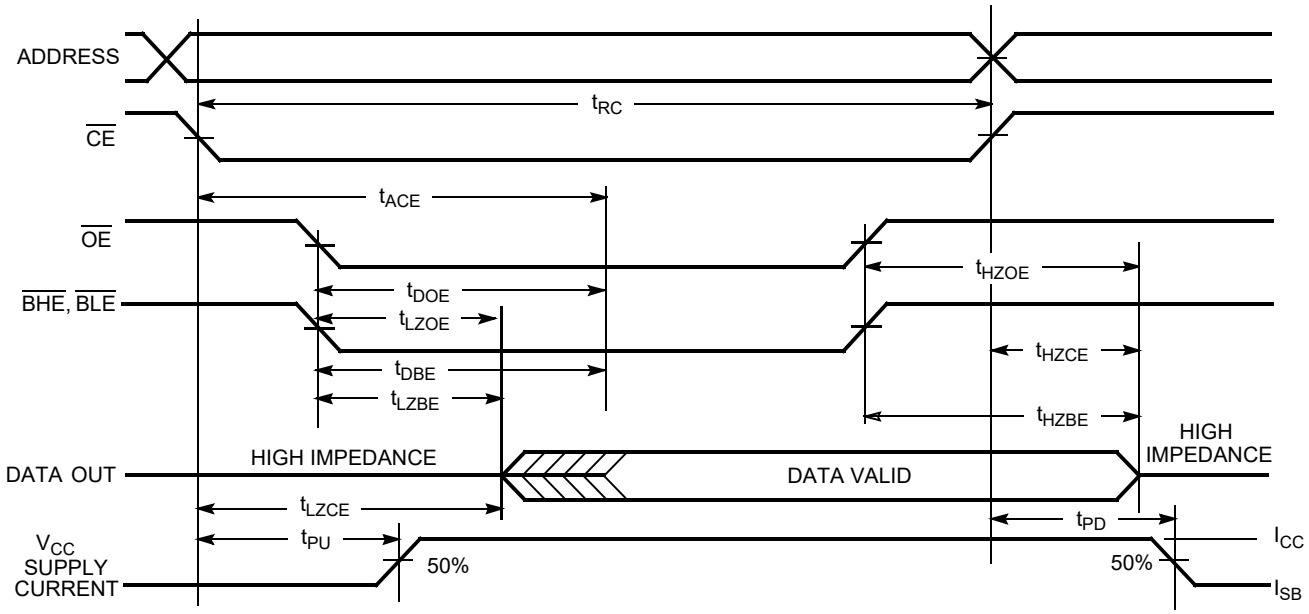


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [13, 14]



Notes
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms(continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [15, 16, 17]

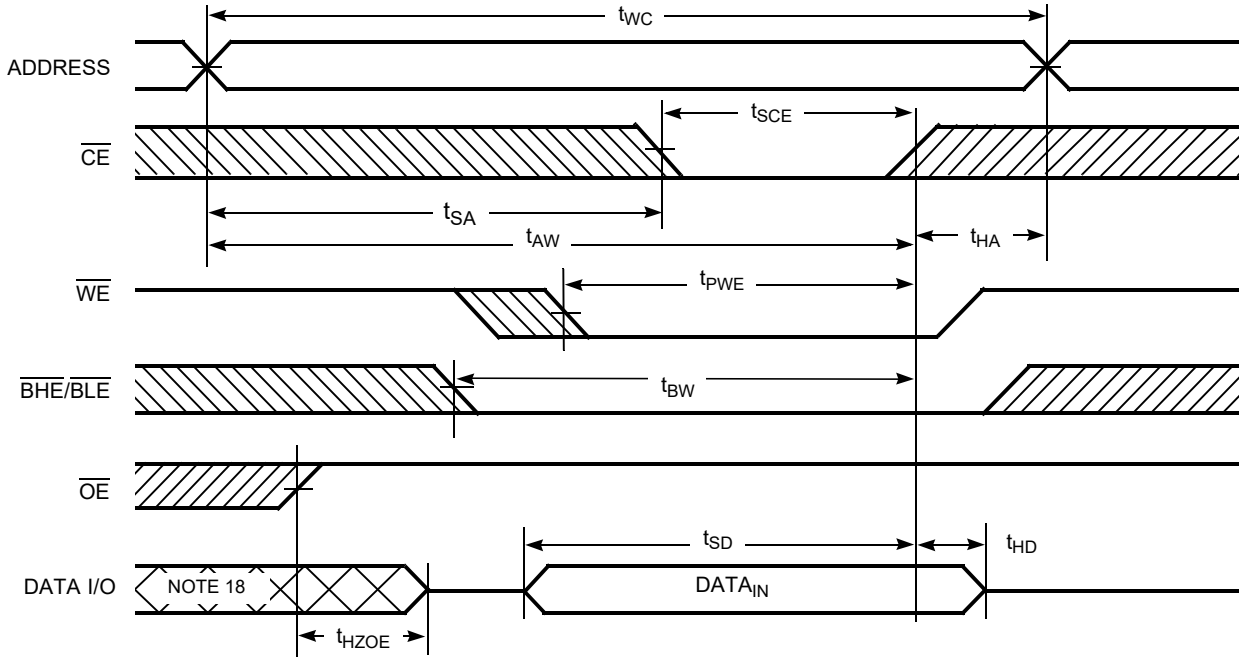
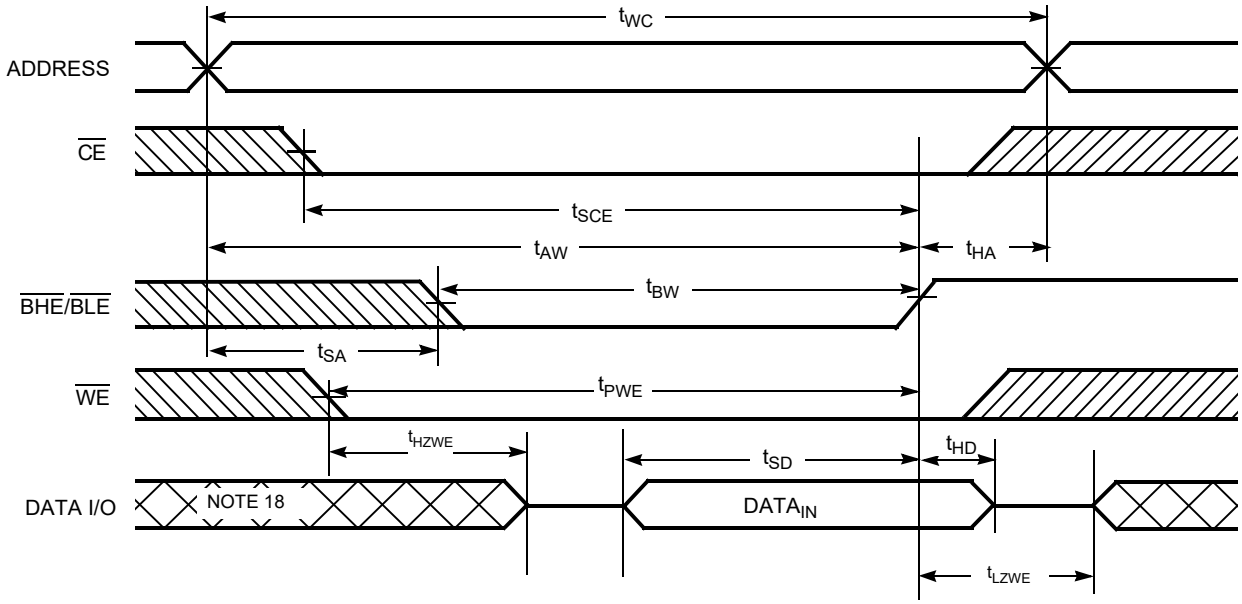


Figure 8. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [15, 16, 17]

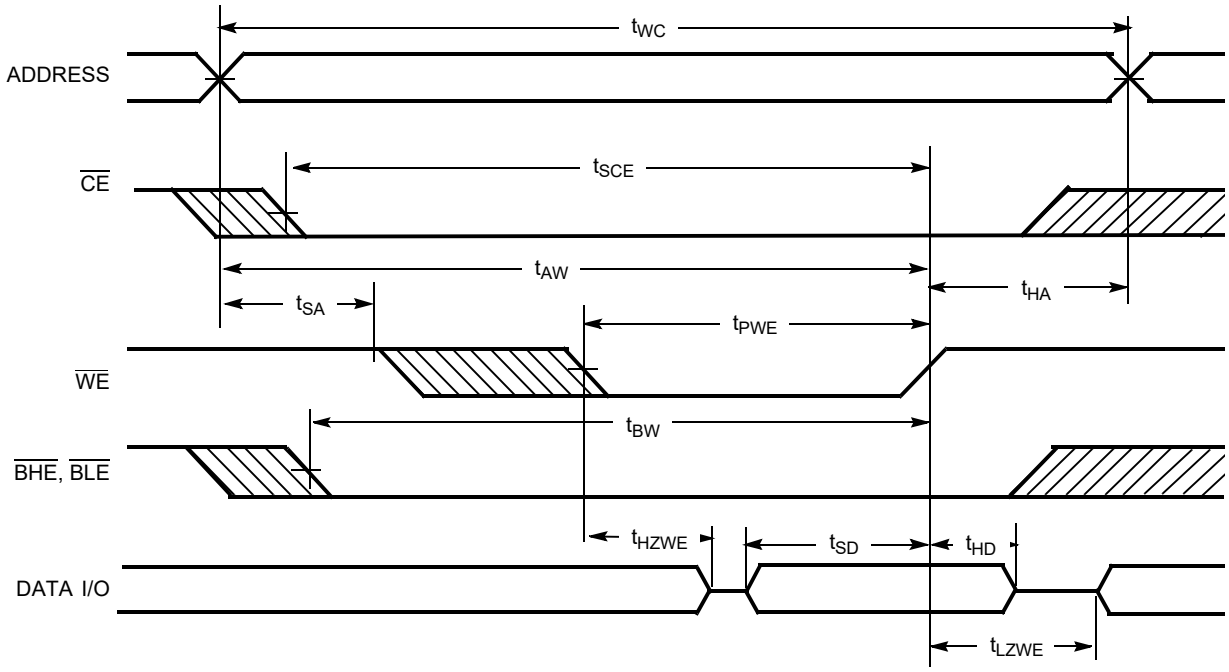


Notes

15. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
16. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms(continued)

Figure 9. Write Cycle No. 3 (WE Controlled, OE LOW) [19, 20, 21]



Notes

19. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE, BLE, or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
20. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
21. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

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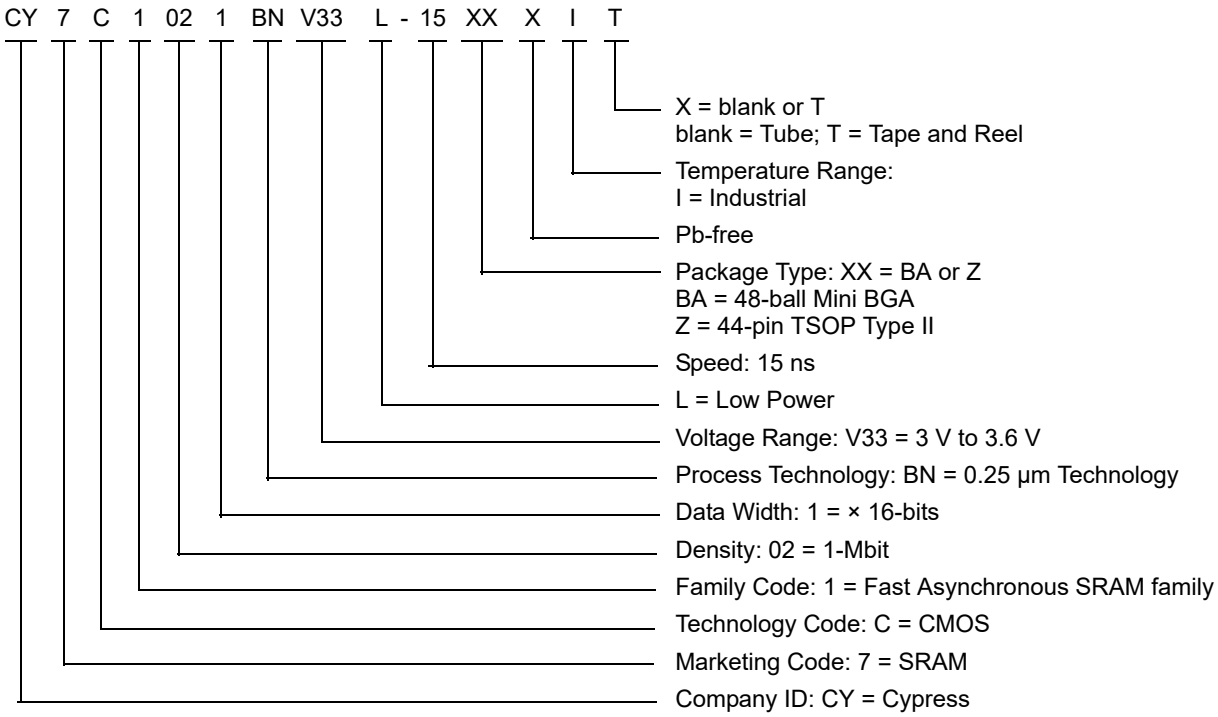
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1021BNV33L-15BAI	51-85096	48-ball Mini BGA (7 mm × 7 mm)	Industrial
	CY7C1021BNV33L-15BAIT	51-85096	48-ball Mini BGA (7 mm × 7 mm) Tape and Reel	
	CY7C1021BNV33L-15ZXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021BNV33L-15ZXIT	51-85087	44-pin TSOP Type II (Pb-free) Tape and Reel	

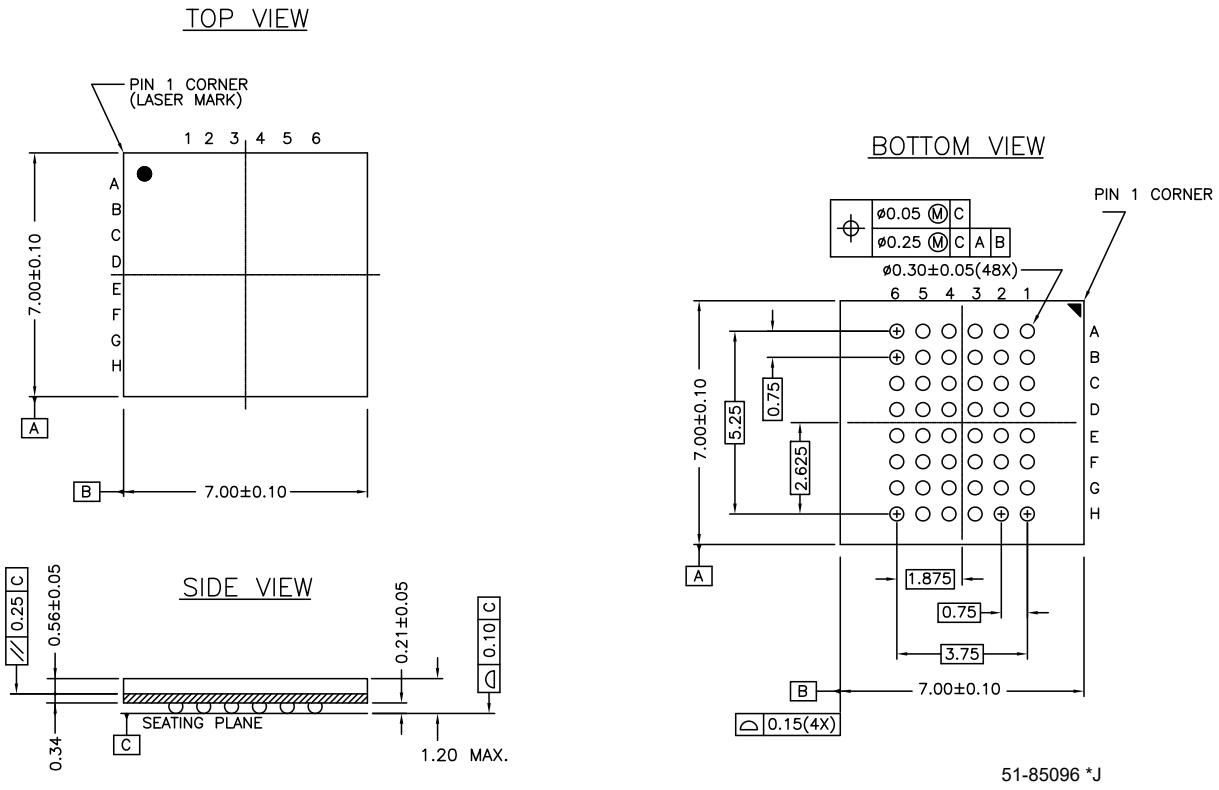
Please contact local sales representative regarding availability of these parts.

Ordering Code Definitions



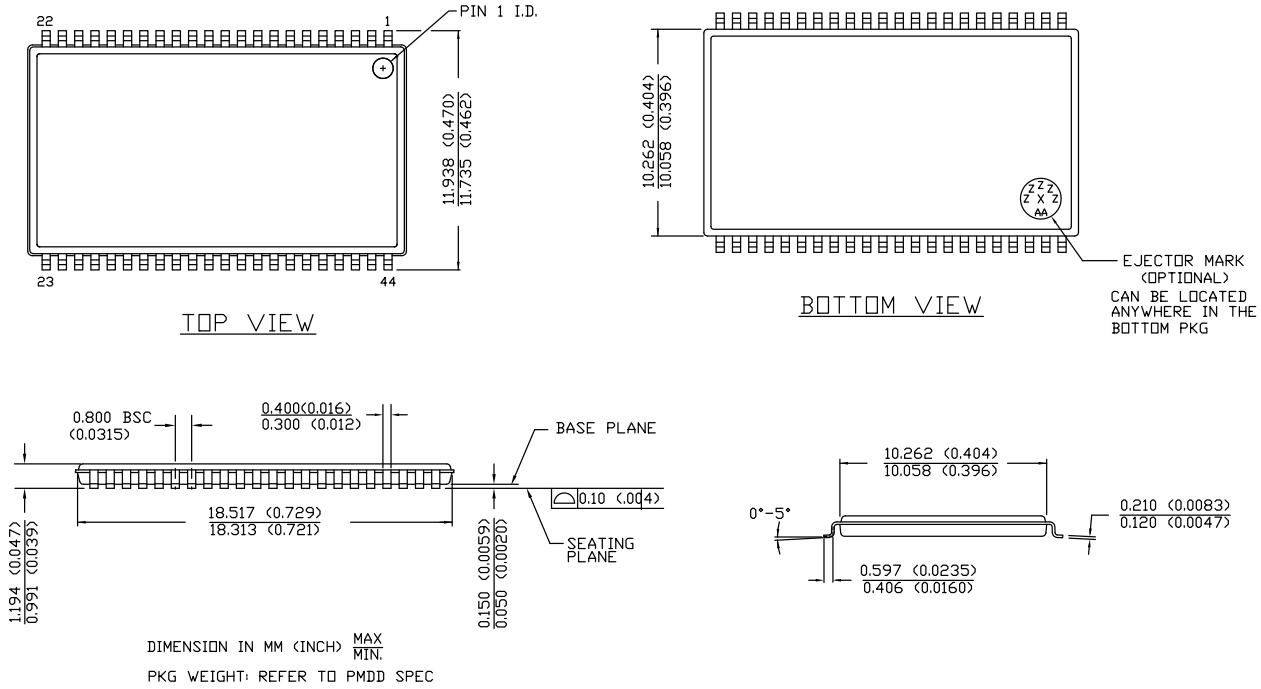
Package Diagrams

Figure 10. 48-ball FBGA (7 mm × 7 mm × 1.2 mm) BA48 Package Outline, 51-85096



Package Diagrams(continued)

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
BGA	Ball Grid Array
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021BNV33, 64K × 16 Static RAM Document Number: 001-06433				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	423847	NXR	02/02/2006	New data sheet.
*A	2897061	AJU	03/22/2010	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85096 – Changed revision from *F to *H. spec 51-85082 – Changed revision from *B to *C. spec 51-85087 – Changed revision from *A to *C.
*B	3109897	AJU	12/14/2010	Added Ordering Code Definitions under Ordering Information.
*C	3103073	PRAS	03/08/2011	Updated Package Diagrams: spec 51-85096 – Changed revision from *H to *I. Added Acronyms and Units of Measure. Updated to new template.
*D	3403051	AJU	10/12/2011	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85082 – Changed revision from *C to *D spec 51-85087 – Changed revision from *C to *D.
*E	3937949	MEMJ	03/19/2013	Removed all references of 400-mil SOJ package in the document. Updated Switching Characteristics: Updated Note 10. Updated Switching Waveforms: Updated Figure 7, Figure 8. Added Note 15, 18 and referred the same notes in Figure 7, Figure 8. Referred Note 16, 17 in Figure 8. Referred Note 19, 20 in Figure 9. Updated Package Diagrams: spec 51-85087 – Changed revision from *D to *E.
*F	4578447	MEMJ	01/16/2015	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Switching Characteristics: Added Note 11 and referred the same note in “WRITE CYCLE”. Updated Switching Waveforms: Added Note 21 and referred the same note in Figure 9. Updated Package Diagrams: spec 51-85096 – Changed revision from *I to *J.
*G	5989860	NILE	12/13/2017	Updated Ordering Information: Updated part numbers. Updated to new template.

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