

3-Mbit (128K × 24) Static RAM

Features

- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 175 \text{ mA}$ at $f = 100 \text{ MHz}$
- Low CMOS standby power
 - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{CE}_3 features
- Available in Pb-free standard 119-ball PBGA

Functional Description

The CY7C1024DV33 is a high performance CMOS static RAM organized as 128 K words by 24 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

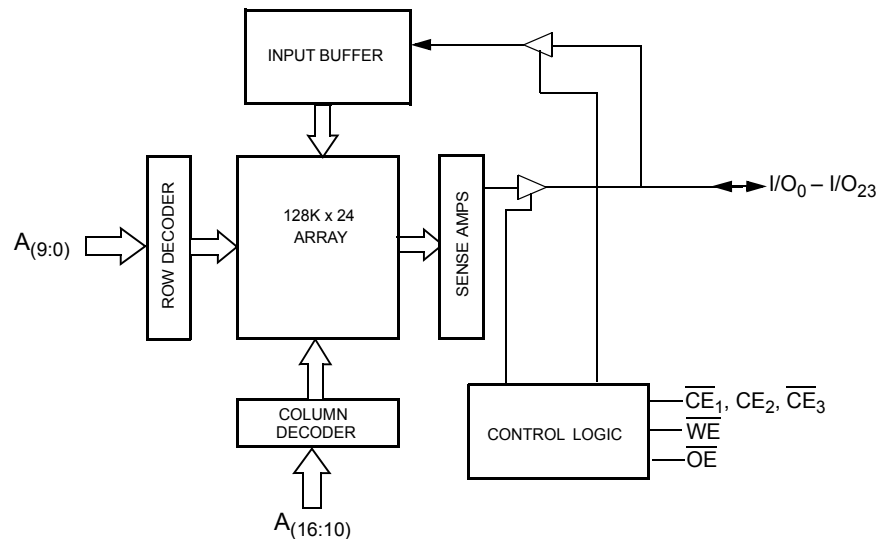
To write to the device, enable the chip (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{CE}_3 LOW), while forcing the Write Enable (\overline{WE}) input LOW.

To read from the device, enable the chip by taking \overline{CE}_1 LOW, CE_2 HIGH, and \overline{CE}_3 LOW while forcing the Output Enable (\overline{OE}) LOW and the Write Enable (\overline{WE}) HIGH. See the [Truth Table on page 7](#) for a complete description of Read and Write modes.

The 24 I/O pins (I/O_0 to I/O_{23}) are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH, CE_2 LOW, or \overline{CE}_3 HIGH) or when the output enable (\overline{OE}) is HIGH during a write operation. (\overline{CE}_1 LOW, CE_2 HIGH, \overline{CE}_3 LOW, and \overline{WE} LOW).

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	175	mA
Maximum CMOS standby current	25	mA

Pin Configuration

Figure 1. 119-Ball PBGA Top View ^[1]

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	\overline{CE}_1	A	A	NC
C	I/O ₁₂	NC	CE ₂	NC	\overline{CE}_3	NC	I/O ₀
D	I/O ₁₃	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁
E	I/O ₁₄	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₂
F	I/O ₁₅	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₃
G	I/O ₁₆	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₄
H	I/O ₁₇	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₅
J	NC	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	NC
K	I/O ₁₈	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₆
L	I/O ₁₉	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₇
M	I/O ₂₀	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₈
N	I/O ₂₁	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₉
P	I/O ₂₂	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₀
R	I/O ₂₃	NC	NC	NC	NC	NC	I/O ₁₁
T	NC	A	A	\overline{WE}	A	A	NC
U	NC	A	A	\overline{OE}	A	A	NC

Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage temperature -65 °C to +150 °C
- Ambient temperature with power applied -55 °C to +125 °C
- Supply Voltage on V_{CC} Relative to GND [2]...-0.5 V to +4.6 V
- DC Voltage Applied to Outputs in high Z state [2].....-0.5 V to V_{CC} + 0.5 V

- DC input voltage [2].....-0.5 V to V_{CC} + 0.5 V
- Current into outputs (LOW) 20 mA
- Static discharge voltage.....>2001 V (MIL-STD-883, method 3015)
- Latch-up current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions [3]	-10		Unit
			Min	Max	
V _{OH}	Output HIGH voltage	Min V _{CC} , I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW voltage	Min V _{CC} , I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH voltage		2.0	V _{CC} + 0.3	V
V _{IL} [2]	Input LOW voltage		-0.3	0.8	V
I _{IX}	Input leakage current	GND ≤ V _{IN} ≤ V _{CC}	-1	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _{OUT} ≤ V _{CC} , output disabled	-1	+1	μA
I _{CC}	V _{CC} operating supply current	Max V _{CC} , f = f _{MAX} = 1/t _{RC} I _{OUT} = 0 mA CMOS levels		175	mA
I _{SB1}	Automatic CE power-down current —TTL inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30	mA
I _{SB2}	Automatic CE power-down current — CMOS inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3 V$, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0		25	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	pF
C _{OUT}	I/O capacitance		10	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	119-Ball PBGA	Unit
θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	20.31	°C/W
θ _{JC}	Thermal resistance (junction to case)		8.35	°C/W

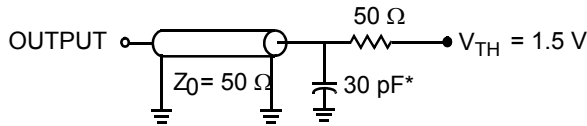
Notes

2. V_{IL} (min) = -2.0 V and V_{IH}(max) = V_{CC} + 2 V for pulse durations of less than 20 ns.
3. \overline{CE} refers to a combination of \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 . \overline{CE} is LOW when \overline{CE}_1 , \overline{CE}_3 are LOW and \overline{CE}_2 is HIGH. \overline{CE} is HIGH when \overline{CE}_1 is HIGH, or \overline{CE}_2 is LOW, or \overline{CE}_3 is HIGH.

AC Test Loads and Waveforms

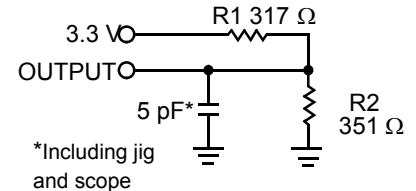
The AC test loads and waveform diagram follows.

Figure 2. AC Test Loads and Waveform^[4]



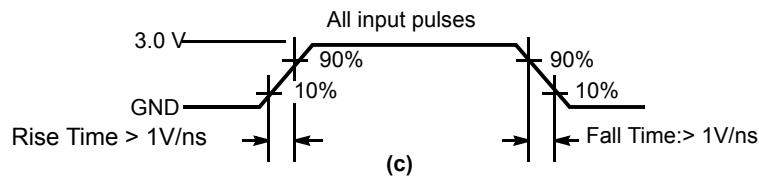
(a)

*Capacitive Load consists of all components of the test environment



(b)

*Including jig and scope



AC Switching Characteristics

Over the Operating Range^[5]

Parameter	Description	-10		Unit
		Min	Max	
Read Cycle				
$t_{power}^{[6]}$	V_{CC} (Typical) to the first access	100	–	μs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	\overline{CE} active LOW to data valid ^[3]	–	10	ns
t_{DOE}	\overline{OE} LOW to data valid	–	5	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[7]	1	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[7]	–	5	ns
t_{LZCE}	\overline{CE} active LOW to low Z ^[3, 7]	3	–	ns
t_{HZCE}	\overline{CE} deselect HIGH to high Z ^[3, 7]	–	5	ns
t_{PU}	\overline{CE} active LOW to power-up ^[3, 8]	0	–	ns
t_{PD}	\overline{CE} deselect HIGH to power-down ^[3, 8]	–	10	ns

Notes

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 μs (t_{power}) after reaching the minimum operating V_{DD} , normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR} , 2.0 V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading as shown in part a) of Figure 2, unless specified otherwise.
- t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{LZOE} , t_{LZCE} , and t_{LZWE} are specified with a load capacitance of 5 pF as in part (b) of Figure 2. Transition is measured ± 200 mV from steady state voltage.
- These parameters are guaranteed by design and are not tested.

AC Switching Characteristics (continued)

Over the Operating Range ^[5]

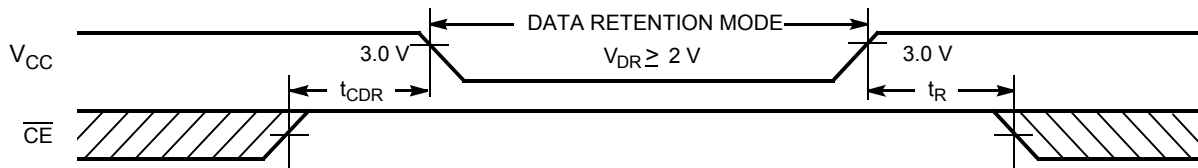
Parameter	Description	-10		Unit
		Min	Max	
Write Cycle ^[9, 10]				
t _{WC}	Write cycle time	10	–	ns
t _{SCE}	\overline{CE} active LOW to write end ^[3]	7	–	ns
t _{AW}	Address setup to write end	7	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	\overline{WE} pulse width	7	–	ns
t _{SD}	Data setup to write end	5.5	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	\overline{WE} HIGH to low Z ^[7]	3	–	ns
t _{HZWE}	\overline{WE} LOW to high Z ^[7]	–	5	ns

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions ^[3]	Min	Typ	Max	Unit
V _{DR}	V _{CC} for data retention		2	–	–	V
I _{CCDR}	Data retention current	V _{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V	–	–	25	mA
t _{CDR} ^[11]	Chip deselect to data retention time		0	–	–	ns
t _R ^[12]	Operation recovery time		t _{RC}	–	–	ns

Data Retention Waveform



Notes

- 9. The internal write time of the memory is defined by the overlap of \overline{CE}_1 and \overline{CE}_2 and \overline{CE}_3 LOW and \overline{WE} LOW. Chip enables must be active and \overline{WE} must be LOW to initiate a write. The transition of any of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- 10. The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.
- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 50 μs or stable at V_{CC(min)} ≥ 50 μs.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [13, 14]

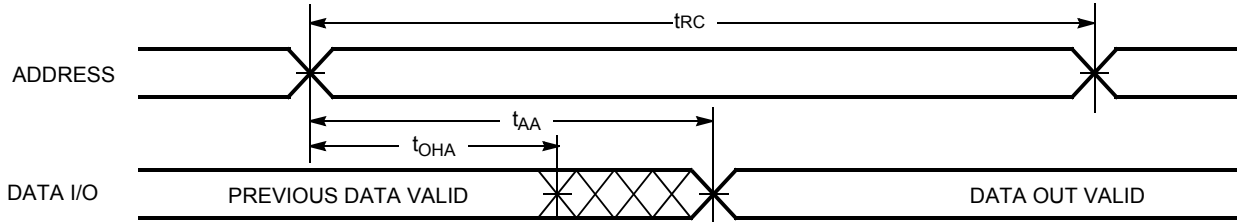


Figure 4. Read Cycle No. 2 (\overline{OE} Controlled) [3, 14, 15]

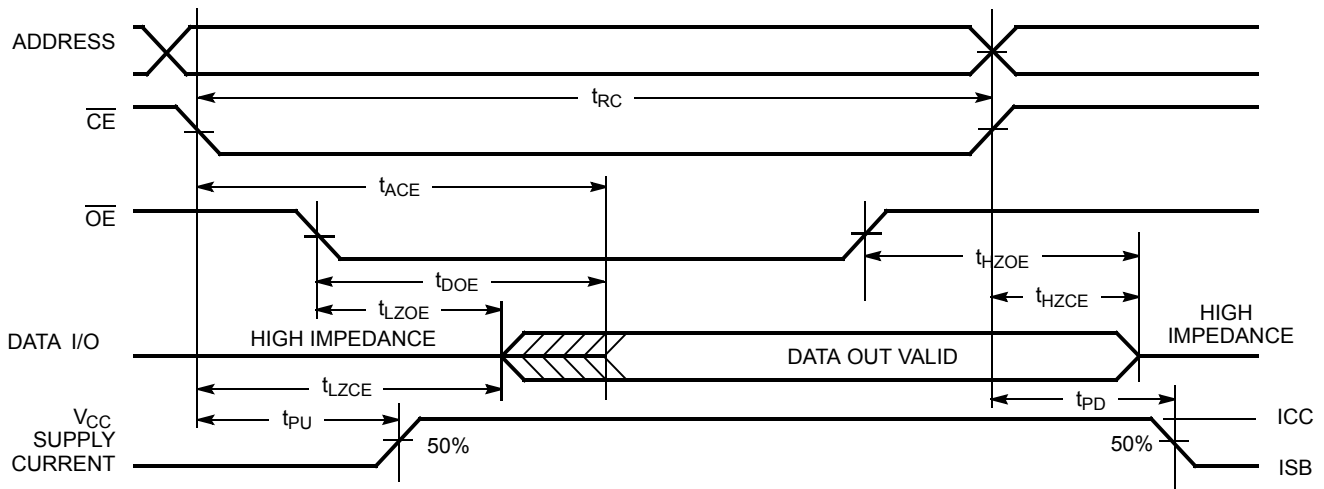
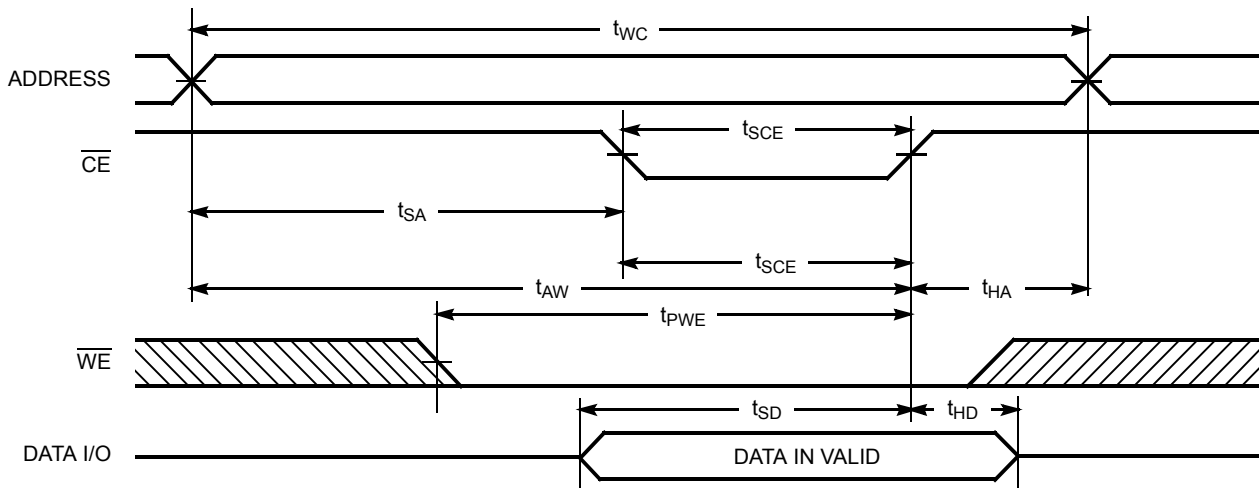


Figure 5. Write Cycle No. 1 (\overline{CE} Controlled) [3, 16, 17]



Notes

- 13. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .
- 14. \overline{WE} is HIGH for read cycle.
- 15. Address valid before or similar to \overline{CE} transition LOW.
- 16. Data I/O is high impedance if \overline{OE} = V_{IH} .
- 17. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [3, 16, 17]

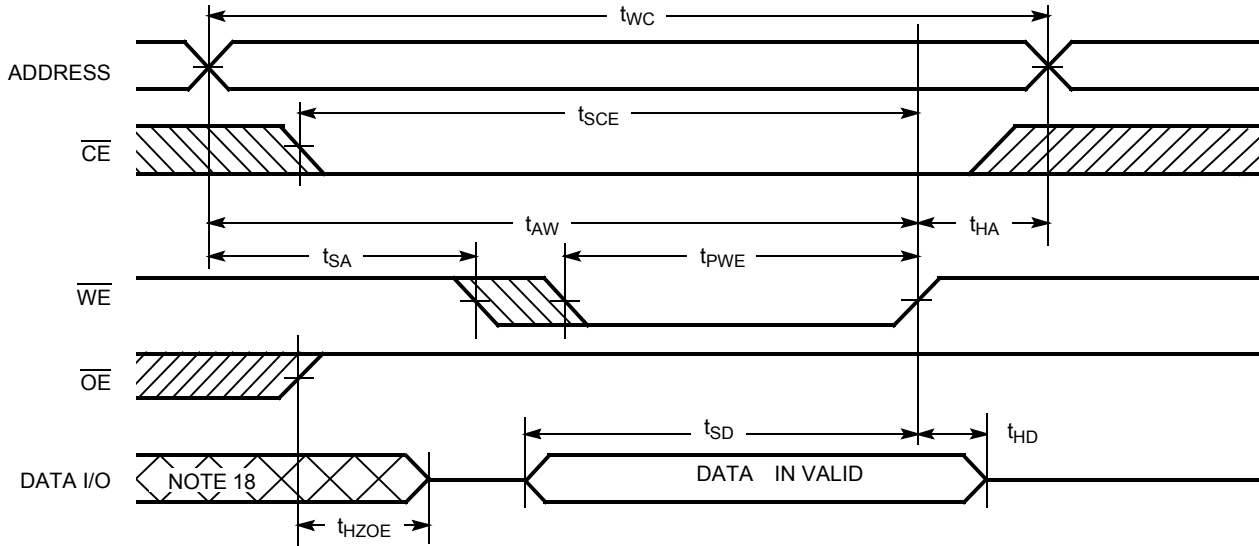
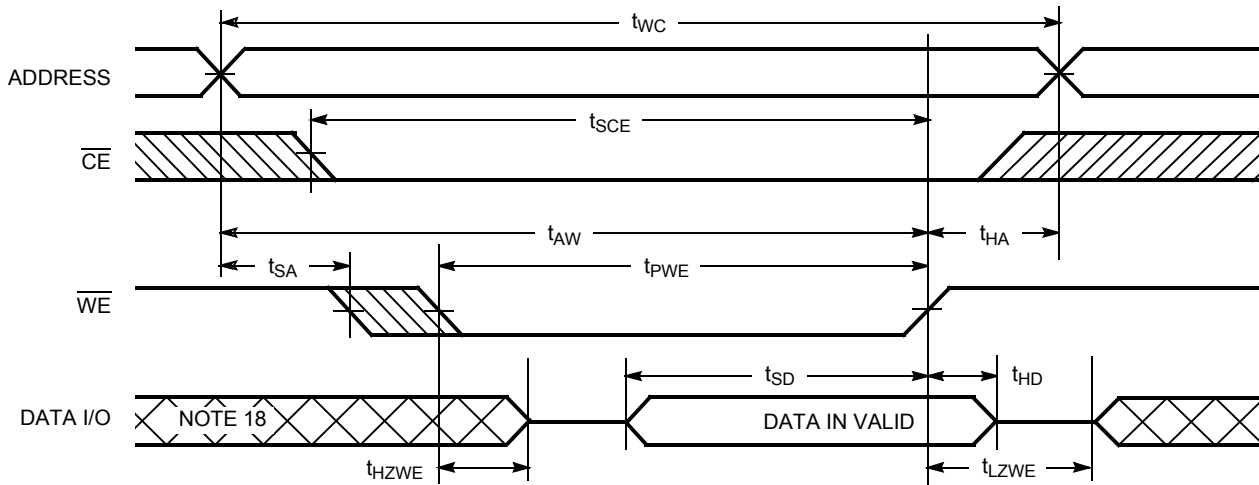


Figure 7. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [3, 17, 19]



Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{CE}_3	\overline{OE}	\overline{WE}	I/O ₀ – I/O ₂₃	Mode	Power
H	X	X	X	X	High Z	Power-down	Standby (I _{SB})
X	L	X	X	X	High Z	Power-down	Standby (I _{SB})
X	X	H	X	X	High Z	Power-down	Standby (I _{SB})
L	H	L	L	H	Full Data Out	Read	Active (I _{CC})
L	H	L	X	L	Full Data In	Write	Active (I _{CC})
L	H	L	H	H	High Z	Selected, outputs disabled	Active (I _{CC})

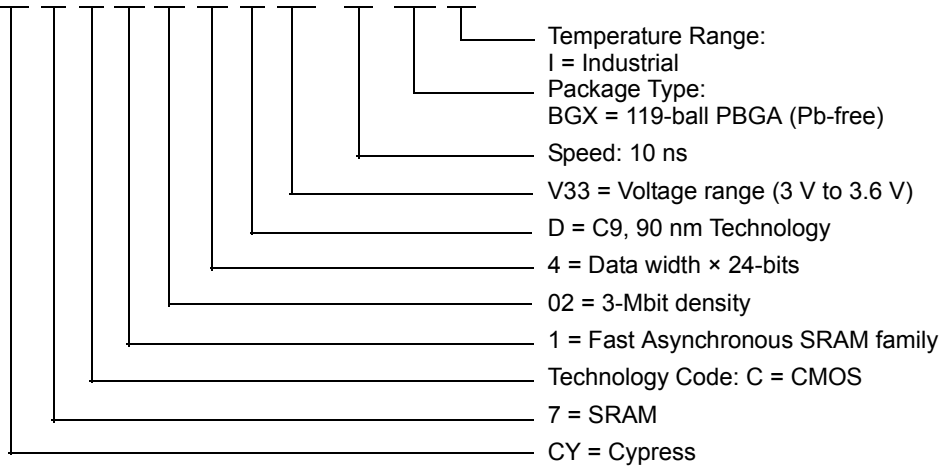
Note
 18. During this period, the I/Os are in the output state and input signals are not applied.
 19. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1024DV33-10BGXI	51-85115	119-ball Plastic Ball Grid Array (14 x 22 x 2.4 mm) (Pb-free)	Industrial

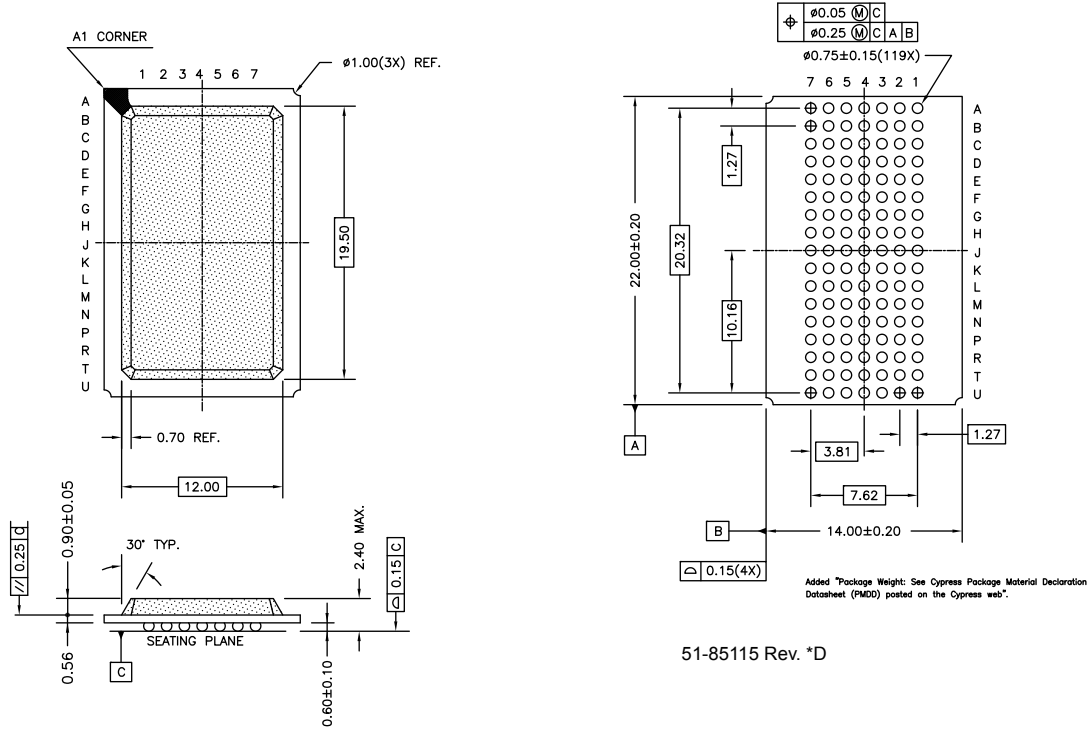
Ordering Code Definitions

CY 7 C 1 02 4 D V33 - 10 BGX I



Package Diagram

Figure 8. 119-ball PBGA (14 x 22 x 2.4 mm)



51-85115 Rev. *D

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
TSOP	thin small outline package
TTL	Transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY7C1024DV33, 3-Mbit (128K × 24) Static RAM Document Number: 001-08353				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	469517	NXR	See ECN	New data sheet
*A	499604	NXR	See ECN	Added note 1 for NC pins Changed I _{CC} specification from 150 mA to 185 mA Updated Test Condition for I _{CC} in DC Electrical Characteristics table Added note for t _{ACE} , t _{LZCE} , t _{HZCE} , t _{PU} , t _{PD} , t _{SCE} in AC Switching Characteristics Table on page 4
*B	1462586	VKN/SFV	See ECN	Converted from preliminary to final Updated block diagram Changed I _{CC} specification from 185 mA to 225 mA Updated thermal specs
*C	2604677	VKN/PYRS	11/12/08	Removed Commercial operating range, Added Industrial operating range Removed 8 ns speed bin, Added 10 ns speed bin
*D	3109199	PRAS	12/13/2010	Added Ordering Code Definitions . Updated Package Diagram .
*E	3388080	TAVA	09/29/2011	Minor technical edits. Added Acronyms and Document Conventions . Updated template.
*F	4548836	MEMJ	10/22/2014	Updated Package Diagram spec 51-85115 – Changed revision from *C to *D Completing Sunset Review.
*G	4576478	MEMJ	11/21/2014	Added related documentation hyperlink in page 1. Added Note 19 in Switching Waveforms . Added note reference 19 in Figure 7 .

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