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## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 110 \text{ mA}$  at  $f = 100 \text{ MHz}$
- Low CMOS standby power
  - $I_{SB2} = 20 \text{ mA}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 44-pin TSOP-II package
- Offered in standard and high reliability (Q) grades

## Functional Description

The CY7C1059DV33 is a high performance CMOS Static RAM organized as 1M words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

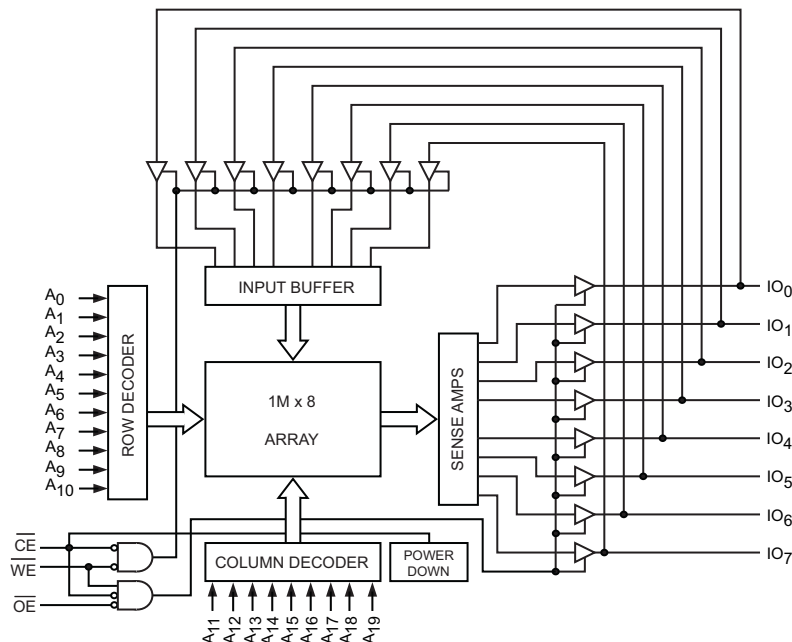
To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input or output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

The CY7C1059DV33 is available in 44-pin TSOP-II package with center power and ground (revolutionary) pinout.

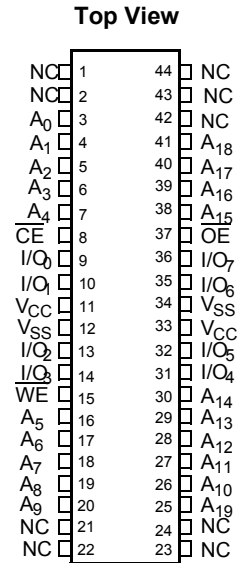
For a complete list of related documentation, click [here](#).

## Logic Block Diagram



## Pin Configuration

Figure 1. 44-Pin TSOP II



## Selection Guide

Description	-10	-12	Unit
Maximum access time	10	12	ns
Maximum operating current	110	100	mA
Maximum CMOS standby current	20	20	mA

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage on  $V_{CC}$  to relative GND<sup>[1]</sup> ..... -0.5 V to + 4.6 V  
 DC voltage applied to outputs in high-Z state<sup>[1]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

DC input voltage<sup>[1]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V  
 Current into outputs (LOW) ..... 20 mA  
 Static discharge voltage ..... >2001 V (MIL-STD-883, Method 3015)  
 Latch-up current ..... >200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		Unit
			Min	Max	Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	2.4	-	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	-	0.4	-	0.4	V
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	+1	-1	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , output disabled	-1	+1	-1	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$	-	110	-	100	mA
$I_{SB1}$	Automatic CE power-down current — TTL inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	-	40	-	35	mA
$I_{SB2}$	Automatic CE power-down current — CMOS inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ , or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$	-	20	-	20	mA

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$	12	pF
$C_{OUT}$	I/O capacitance		12	pF

## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
$\theta_{JA}$	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.43	°C/W
$\theta_{JC}$	Thermal resistance (Junction to case)		15.8	°C/W

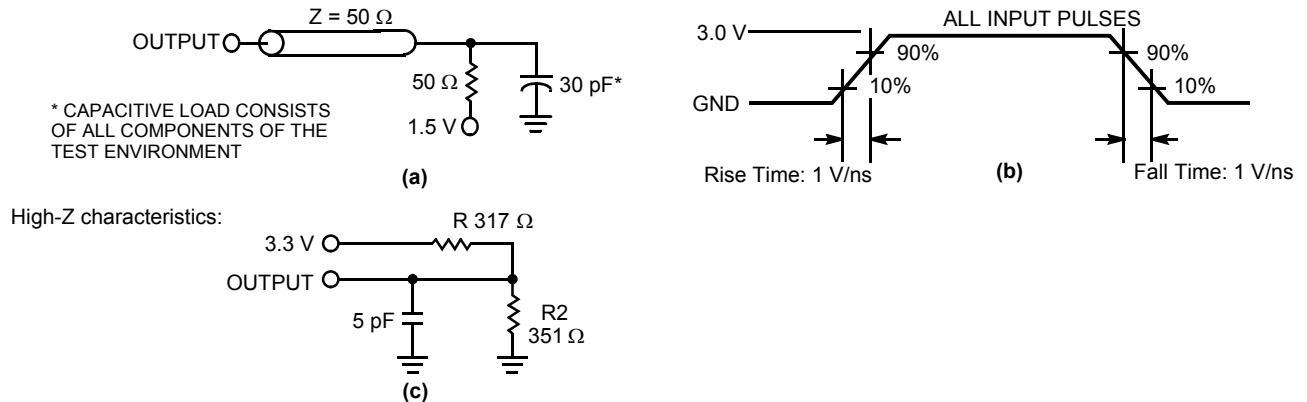
### Notes

- $V_{IL(\text{min})} = -2.0 \text{ V}$  and  $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

Figure 2. AC Test Loads and Waveforms

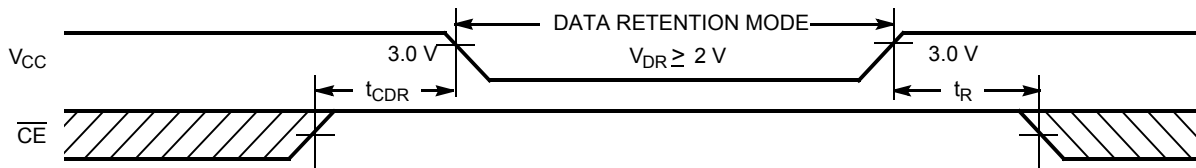


### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions <sup>[3]</sup>	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	20	mA
$t_{CDR}^{[2]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[4]}$	Operation recovery time		$t_{RC}$	–	ns

Figure 3. Data Retention Waveform



**Notes**

- 3. No inputs may exceed  $V_{CC} + 0.3\text{ V}$ .
- 4. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\ \mu\text{s}$ .

## AC Switching Characteristics

Over the Operating Range<sup>[5]</sup>

Parameter	Description	-10		-12		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{\text{power}}^{[6]}$	$V_{\text{CC}}$ (typical) to the first access	100	–	100	–	$\mu\text{s}$
$t_{\text{RC}}$	Read cycle time	10	–	12	–	ns
$t_{\text{AA}}$	Address to data valid	–	10	–	12	ns
$t_{\text{OHA}}$	Data hold from address change	2.5	–	2.5	–	ns
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to data valid	–	10	–	12	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to data valid	–	5	–	6	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to low-Z	0	–	0	–	ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to high-Z <sup>[7, 8]</sup>	–	5	–	6	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to low-Z <sup>[8]</sup>	3	–	3	–	ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to high-Z <sup>[7, 8]</sup>	–	5	–	6	ns
$t_{\text{PU}}$	$\overline{\text{CE}}$ LOW to power-up	0	–	0	–	ns
$t_{\text{PD}}$	$\overline{\text{CE}}$ HIGH to power-down	–	10	–	12	ns
<b>Write Cycle<sup>[9, 10]</sup></b>						
$t_{\text{WC}}$	Write cycle time	10	–	12	–	ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to write end	7	–	8	–	ns
$t_{\text{AW}}$	Address setup to write end	7	–	8	–	ns
$t_{\text{HA}}$	Address hold from write end	0	–	0	–	ns
$t_{\text{SA}}$	Address setup to write start	0	–	0	–	ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ pulse width	7	–	8	–	ns
$t_{\text{SD}}$	Data setup to write end	5	–	6	–	ns
$t_{\text{HD}}$	Data hold from write end	0	–	0	–	ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to low-Z <sup>[8]</sup>	3	–	3	–	ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to high-Z <sup>[7, 8]</sup>	–	5	–	6	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- $t_{\text{POWER}}$  is the minimum amount of time that the power supply must be at stable, typical  $V_{\text{CC}}$  values until the first memory access can be performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms" on page 4. Transition is measured when the outputs enter a high impedance state.
- At any temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any device.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must refer to the leading edge of the signal that terminates the Write.
- The minimum write cycle time for Write Cycle No. 2 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

### Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled)<sup>[11, 12]</sup>

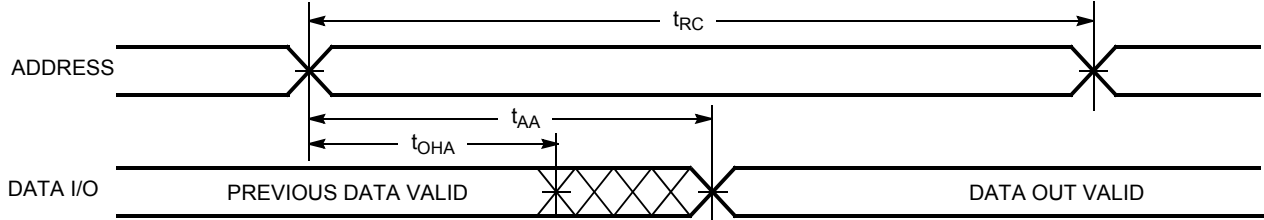
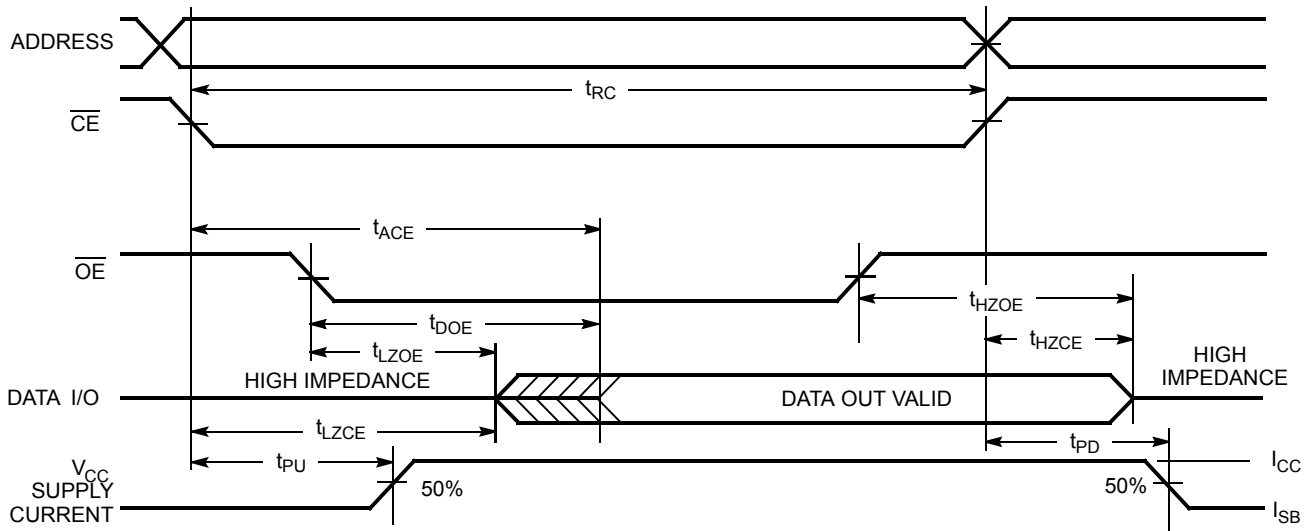


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[12, 13]</sup>



**Notes**

- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- 12.  $\overline{WE}$  is HIGH for Read cycle.
- 13. Address valid before or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  High During Write)<sup>[14, 15]</sup>

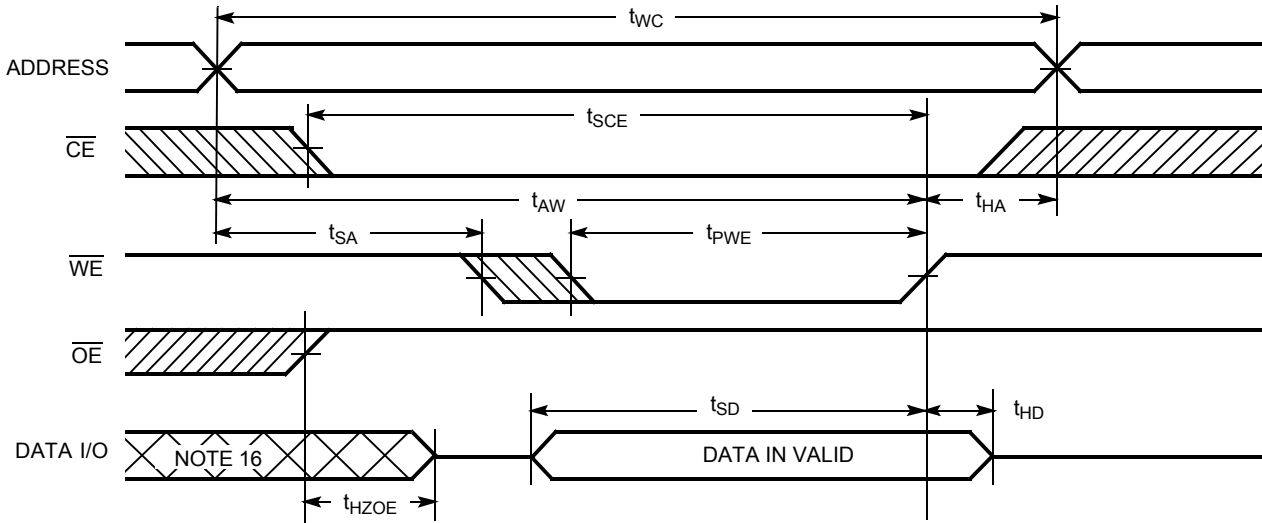
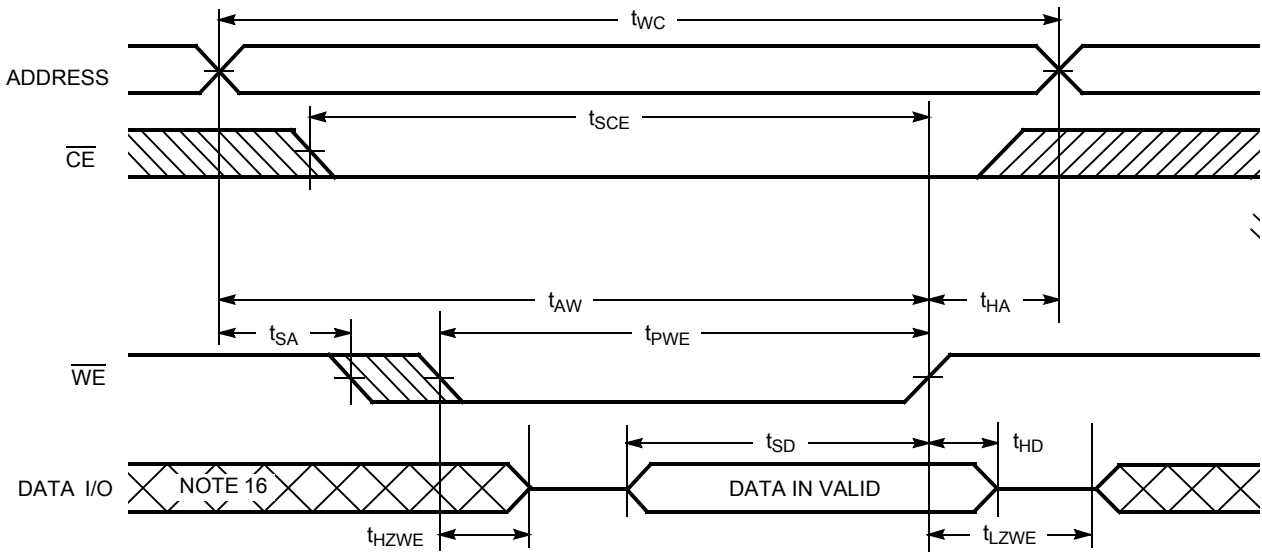


Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  Low)<sup>[15, 17]</sup>



Notes

- 14. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 16. During this period the I/Os are in the output state and input signals must not be applied.
- 17. The minimum write cycle time for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .



**Truth Table**

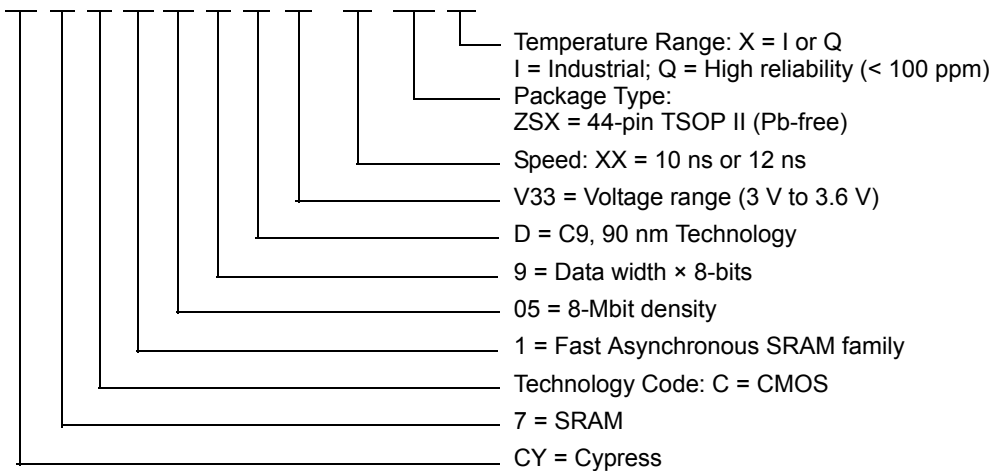
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	Data out	Read	Active (I <sub>CC</sub> )
L	X	L	Data in	Write	Active (I <sub>CC</sub> )
L	H	H	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range	Grade
10	CY7C1059DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial	Standard
12	CY7C1059DV33-12ZSXQ	51-85087	44-pin TSOP II (Pb-free)	Industrial	High reliability (< 100 ppm)

**Ordering Code Definitions**

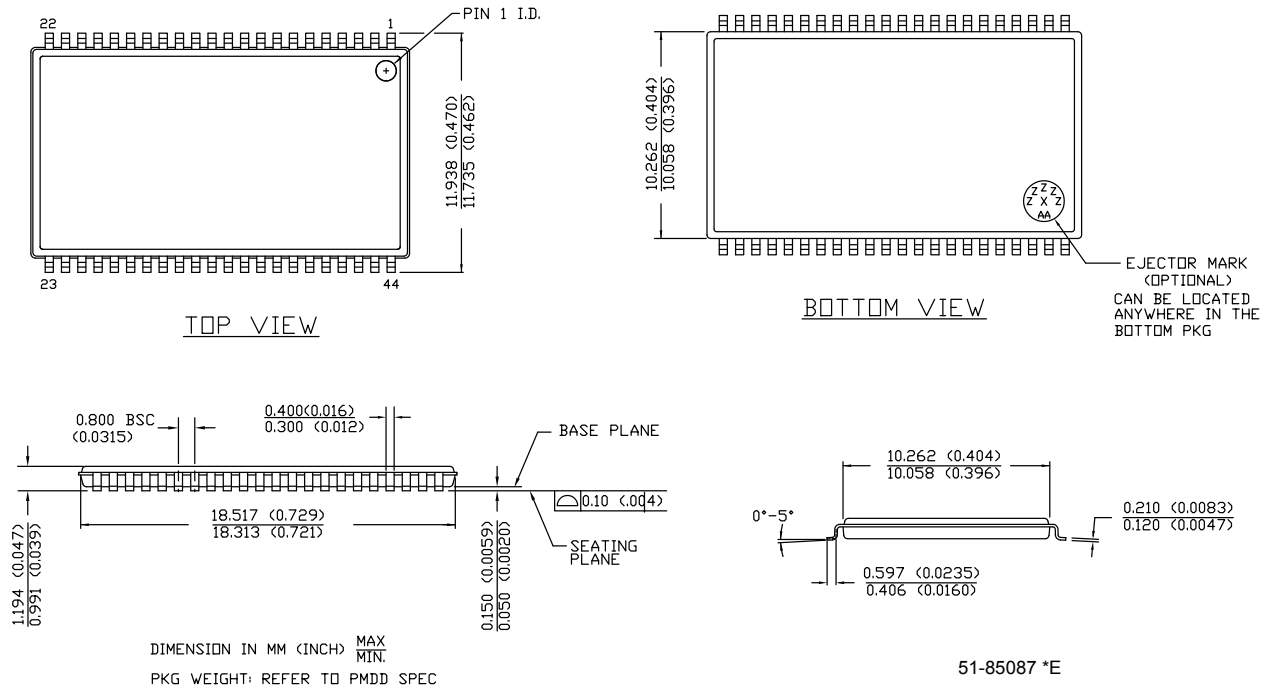
CY 7 C 1 05 9 D V33 - XX ZSX X



Contact your local Cypress sales representative for availability of these parts.

Package Diagram

Figure 8. 44-Pin TSOP II (51-85087)



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
CMOS	complementary metal-oxide-semiconductor
SRAM	static random-access memory
TSOP	thin small-outline package
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad

Document History Page

Document Title: CY7C1059DV33, 8-Mbit (1M × 8) Static RAM				
Document Number: 001-00061				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	342195	PCI	See ECN	New data sheet
*A	380574	SYT	See ECN	Redefined I <sub>CC</sub> values for Com'I and Ind'I temperature ranges I <sub>CC</sub> (Com'I): Changed from 110, 90 and 80 mA to 110, 100 and 95 mA for 8, 10 and 12 ns speed bins respectively I <sub>CC</sub> (Ind'I): Changed from 110, 90 and 80 mA to 120, 110 and 105 mA for 8, 10 and 12 ns speed bins respectively Changed the Capacitance values from 8 pF to 10 pF on Page # 3
*B	485796	NXR	See ECN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed -8 and -12 Speed bins from product offering, Removed Commercial Operating Range option, Modified Maximum Ratings for DC input voltage from -0.5 V to -0.3 V and V <sub>CC</sub> + 0.5 V to V <sub>CC</sub> + 0.3 V Updated footnote #7 on High-Z parameter measurement Added footnote #11 Changed the Description of I <sub>IX</sub> from Input Load Current to Input Leakage Current. Updated the Ordering Information table and Replaced Package Name column with Package Diagram.
*C	1513285	VKN/AESA	See ECN	Converted from preliminary to final Added 12 ns speed bin Changed C <sub>IN</sub> and C <sub>OUT</sub> specs from 16 pF to 12 pF Changed t <sub>OHA</sub> spec from 3 ns to 2.5 ns Updated Ordering information table
*D	2594352	NXR/PYRS	10/21/08	Added Q-Grade part
*E	2764423	AJU	09/16/2009	Corrected typo in the ordering information table
*F	2902563	AJU	03/31/2010	Removed inactive part from Ordering Information table. Updated package diagram.
*G	3109147	AJU	12/13/2010	Added <a href="#">Ordering Code Definitions</a> .
*H	3369075	TAVA	09/12/2011	Changed <a href="#">Features</a> section: "I <sub>CC</sub> = 110 mA at 10 ns" to "110 mA at f = 100 MHz". Removed reference to "AN1064, SRAM System Guidelines" on page 1. Removed reference to 36-ball FBGA from <a href="#">Functional Description</a> section. Updated figures under <a href="#">Switching Waveforms</a> section. Updated package diagram revision to *D. Added acronyms and units of measure.
*I	4530384	MEMJ	10/09/2014	Updated <a href="#">Switching Waveforms</a> : Added Note 17 and referred the same note in <a href="#">Figure 7</a> . Updated <a href="#">Package Diagram</a> : spec 51-85087 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.
*J	4578447	MEMJ	01/16/2015	Added related documentation hyperlink in page 1.

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