CY7C1062GN

16-Mbit (512 K words × 32 bits) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active and standby current
  - I_{CC} = 90 mA typical
  - I_{SB2} = 20 mA typical
- Operating voltage range: 2.2 V to 3.6 V
- 1.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 119-ball plastic ball grid array (PBGA) package

Functional Description

CY7C1062GN is a high-performance CMOS fast static RAM device. This device has three chip enables, giving easy memory expansion features.

To write to the device, take Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) and Write Enable ($\overline{WE}$) input LOW. If Byte Enable A ($\overline{B}_A$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If Byte Enable B ($\overline{B}_B$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}). Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond with the I/O pins I/O_{16} to I/O_{23} and I/O_{24} to I/O_{31}, respectively.

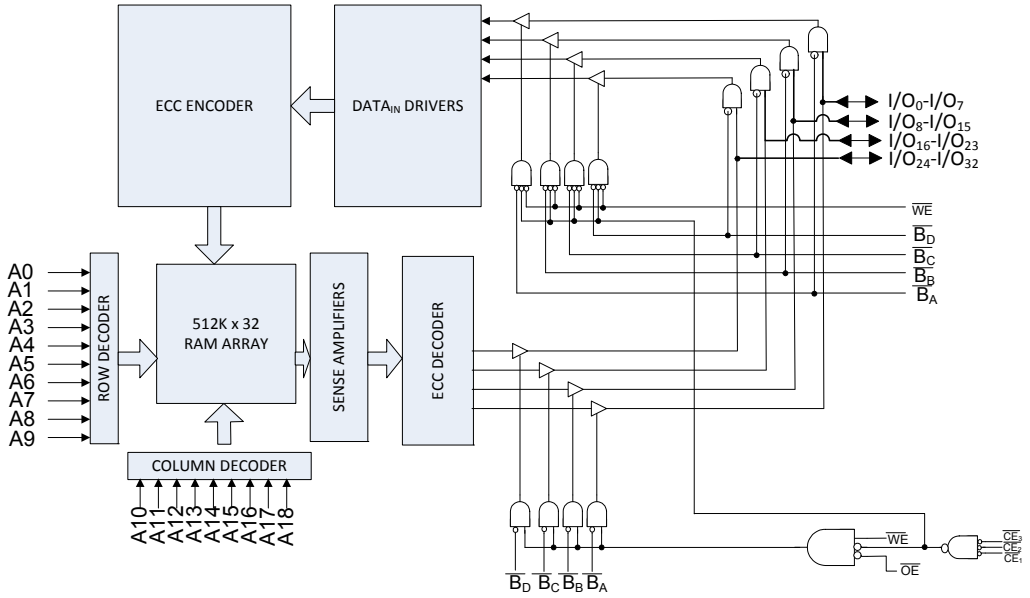
To read from the device, take Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If the first $\overline{B}_A$ is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If $\overline{B}_B$ is LOW, then data from memory appears on I/O_8 to I/O_{15}. Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond to the third and fourth bytes. See Truth Table – CY7C1062GN on page 14 for a complete description of read and write modes.

The input and output pins (I/O_0 through I/O_{31}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the byte selects are disabled ($\overline{B}_{A\text{-}D}$ HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$ LOW and $\overline{WE}$ LOW).

CY7C1062GN is available in Pb-free 119-ball plastic ball grid array (PBGA) package.

For a complete list of related documentation, click here.

Logic Block Diagram – CY7C1062GN



Contents

Pin Configurations

Figure 1. 119-ball PBGA Pinout (Top View) - CY7C1062GN[1]

	1	2	3	4	5	6	7
A	I/O_{16}	A_4	A_3	A_2	A_1	A_0	I/O_0
B	I/O_{17}	A_{18}	A_{17}	$\overline{CE}_1$	A_{16}	A_{15}	I/O_1
C	I/O_{18}	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O_2
D	I/O_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
E	I/O_{20}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
F	I/O_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
G	I/O_{22}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_6
H	I/O_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_7
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O_{24}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
L	I/O_{25}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
M	I/O_{26}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
N	I/O_{27}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_{11}
P	I/O_{28}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{12}
R	I/O_{29}	A_{14}	$\overline{B}_d$	NC	$\overline{B}_b$	A_{13}	I/O_{13}
T	I/O_{30}	A_{12}	A_{11}	$\overline{WE}$	A_{10}	A_9	I/O_{14}
U	I/O_{31}	A_8	A_7	$\overline{OE}$	A_6	A_5	I/O_{15}

Figure 2. 119-ball PBGA Pinout (Top View) - CY7C1062GE[1]

	1	2	3	4	5	6	7
A	I/O_{16}	A_4	A_3	A_2	A_1	A_0	I/O_0
B	I/O_{17}	A_{18}	A_{17}	$\overline{CE}_1$	A_{16}	A_{15}	I/O_1
C	I/O_{18}	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O_2
D	I/O_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
E	I/O_{20}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
F	I/O_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
G	I/O_{22}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_6
H	I/O_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_7
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O_{24}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
L	I/O_{25}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
M	I/O_{26}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
N	I/O_{27}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_{11}
P	I/O_{28}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{12}
R	I/O_{29}	A_{14}	$\overline{B}_d$	NC	$\overline{B}_b$	A_{13}	I/O_{13}
T	I/O_{30}	A_{12}	A_{11}	$\overline{WE}$	A_{10}	A_9	I/O_{14}
U	I/O_{31}	A_8	A_7	$\overline{OE}$	A_6	A_5	I/O_{15}

Note
1. NC pins are not connected internally to the die.

Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I_{CC}, (mA) $f = f_{max}$		Standby, I_{SB2} (mA)	
				Typ[2]	Max	Typ[2]	Max
CY7C1062GN30	Industrial	2.2 V–3.6 V	10	90	110	20	30

Notes
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V and (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND ..... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in High Z State[3] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage[3] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter	Description		Test Conditions		10 ns			Unit
					Min	Typ[4]	Max	
V_{OH}	Output HIGH Voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.0	–	–	V
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2			
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
V_{OL}	Output LOW Voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}	Input HIGH Voltage	2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
V_{IL}	Input LOW Voltage[3]							
		2.2 V to 2.7 V	–		–0.3	–	0.6	
		2.7 V to 3.6 V	–		–0.3	–	0.8	
I_{IX}	Input Leakage Current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output Leakage Current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	
I_{CC}	Operating Supply Current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	110.0	mA
				f = 66.7 MHz	–	70.0	80.0	
I_{SB1}	Automatic CE Power-down Current – TTL Inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH}[5], V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	40.0	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V[5], V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0	30.0	

Notes

3. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and T_A = 25 °C.
5. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, or $\overline{CE_3}$ HIGH.

Capacitance

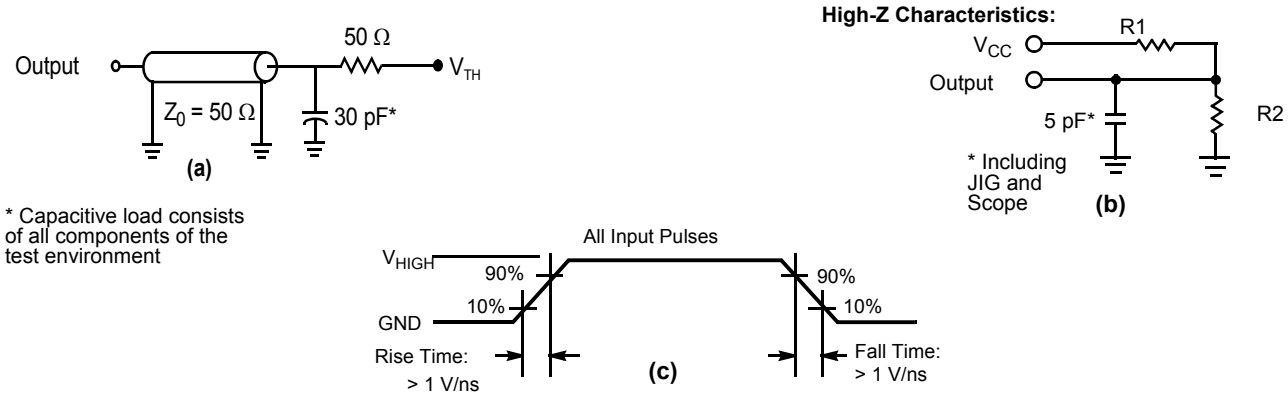
Parameter[6]	Description	Test Conditions	119-ball PBGA	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	I/O Capacitance			

Thermal Resistance

Parameter[6]	Description	Test Conditions	119-ball PBGA	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	20.92	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		15.84	

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms[7]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	
V_{TH}	1.5	V
V_{HIGH}	3.0	

Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 100-µs wait time after V_{CC} stabilizes to its operational value.

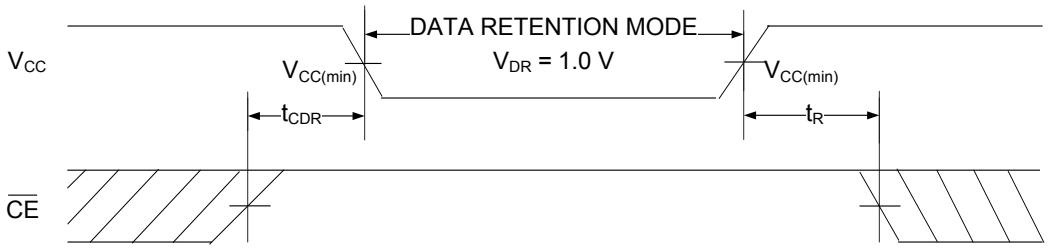
Data Retention Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	–	1.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V [8], $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30.0	mA
t_{CDR}[9]	Chip Deselect to Data Retention Time	–	0.0	–	ns
t_R[9, 10]	Operation Recovery Time	$V_{CC} \geq 2.2$ V	10.0	–	

Data Retention Waveform

Figure 4. Data Retention Waveform[8]



Notes

8. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

AC Switching Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter[11]	Description	10 ns		Unit
		Min	Max	
Read Cycle				
t_{POWER}	V_{CC} (stable) to the first access[12, 13]	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	ns
t_{AA}	Address to data valid	–	10.0	
t_{OHA}	Data hold from address change	3.0	–	
t_{ACE}	$\overline{CE}$ LOW to data valid[14]	–	10.0	
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5.0	
t_{LZOE}	$\overline{OE}$ LOW to low Z[15, 16]	0.0	–	
t_{HZOE}	$\overline{OE}$ HIGH to high Z[15, 16]	–	5.0	
t_{LZCE}	$\overline{CE}$ LOW to low Z[14, 15, 16]	3.0	–	
t_{HZCE}	$\overline{CE}$ HIGH to high Z[14, 15, 16]	–	5.0	
t_{PU}	$\overline{CE}$ LOW to power-up[13, 14]	0.0	–	
t_{PD}	$\overline{CE}$ HIGH to power-down[13, 14]	–	10.0	
t_{DBE}	Byte enable to data valid	–	5.0	
t_{LZBE}	Byte enable to low Z	0.0	–	
t_{HZBE}	Byte disable to high Z	–	6.0	
Write Cycle[17, 18]				
t_{WC}	Write cycle time	10.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end[14]	7.0	–	
t_{AW}	Address setup to write end	7.0	–	
t_{HA}	Address hold from write end	0.0	–	
t_{SA}	Address setup to write start	0.0	–	
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	
t_{SD}	Data setup to write end	5.0	–	
t_{HD}	Data hold from write end	0.0	–	
t_{LZWE}	$\overline{WE}$ HIGH to low Z [15, 16]	3.0	–	
t_{HZWE}	$\overline{WE}$ LOW to high Z [15, 16]	–	5.0	
t_{BW}	Byte Enable to write end	7.0	–	

Notes

11. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 7, unless specified otherwise.
12. t_{POWER} gives minimum amount of time that the power supply is at stable Vcc until first memory access is performed.
13. These parameters are guaranteed by design and are not tested.
14. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.
15. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 7. Transition is measured ±200 mV from steady state voltage.
16. Tested initially and after any design or process changes that may affect these parameters.
17. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ Low) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY7C1062GN (Address Transition Controlled)[19, 20]

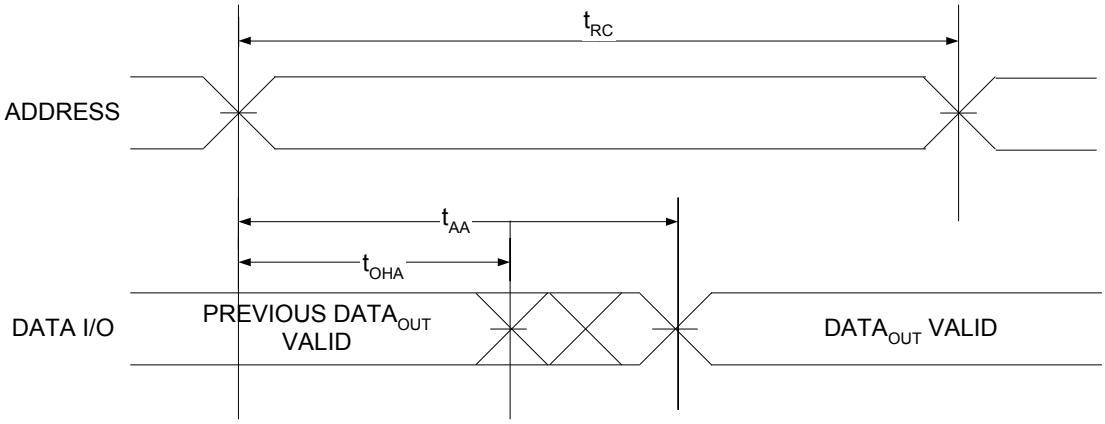
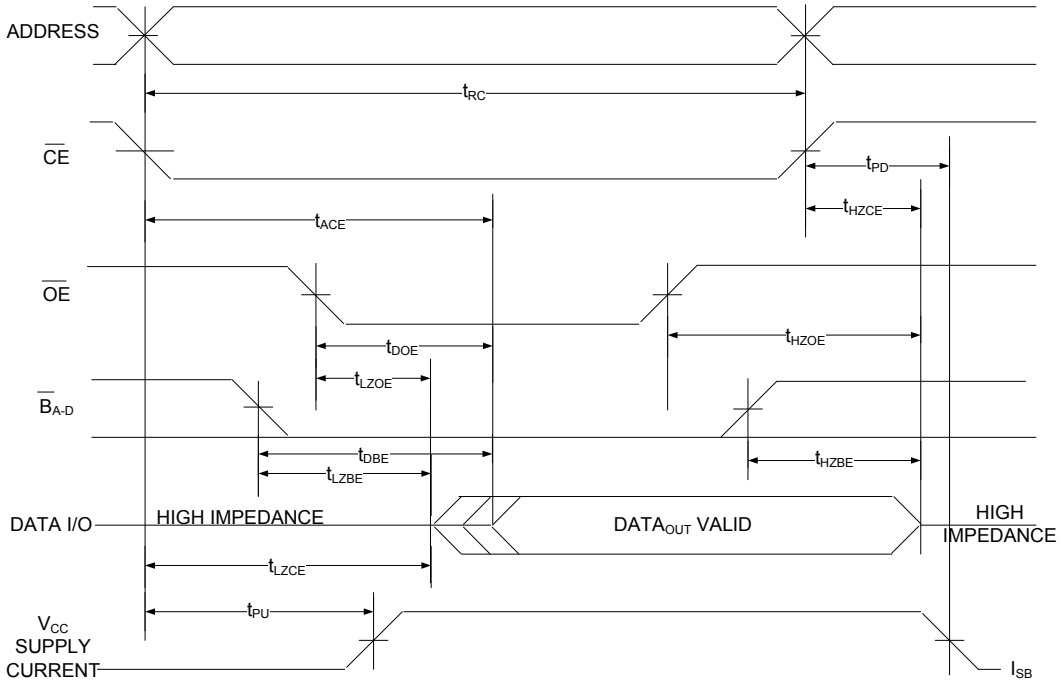


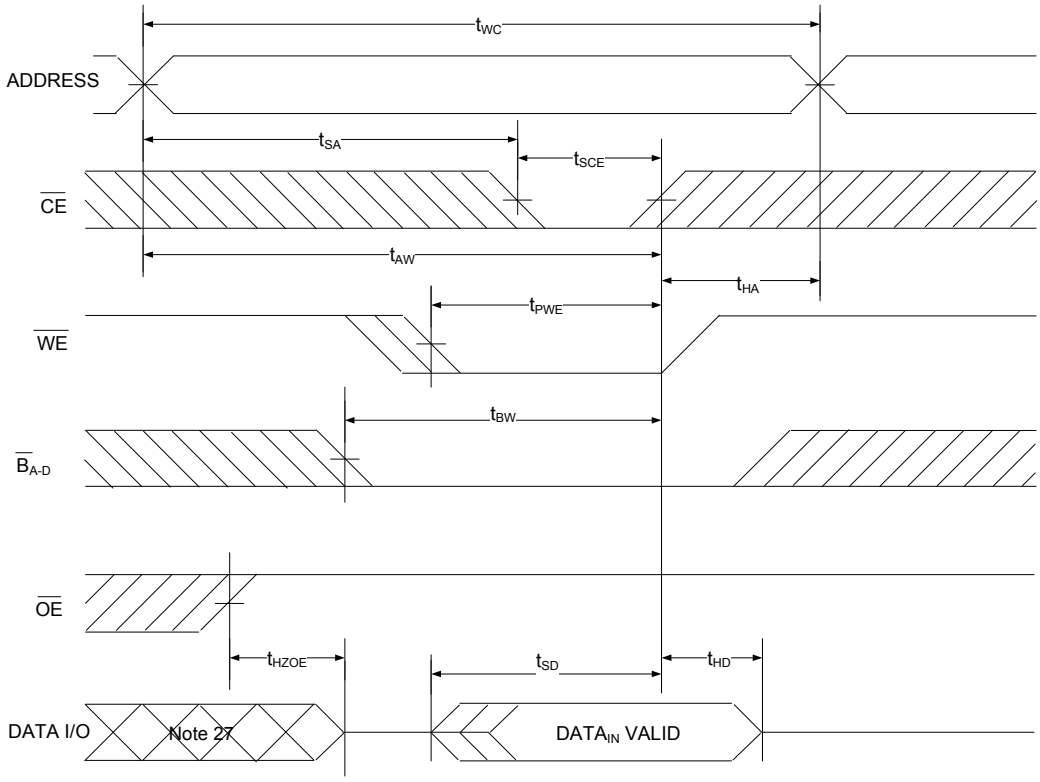
Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)[21, 22, 23]



Notes

19. The device is continuously selected, $\overline{OE}$, $\overline{CE}$, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ = V_{IL}.
20. $\overline{WE}$ is HIGH for read cycle.
21. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.
22. $\overline{WE}$ is HIGH for read cycle.
23. Address valid before or similar to $\overline{CE}$ transition LOW.

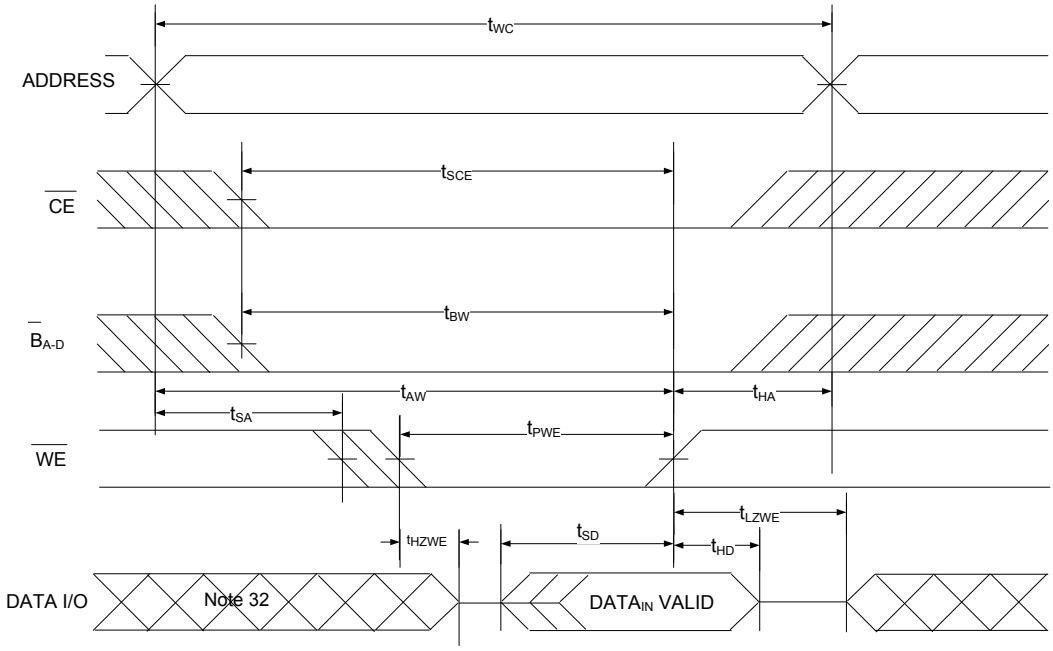
Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled)[24, 25, 26]



Notes

24. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{CE}$ or $\overline{OE}$ or $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ = V_{IH}.
27. During this period I/O are in output state. Do not apply input signals.

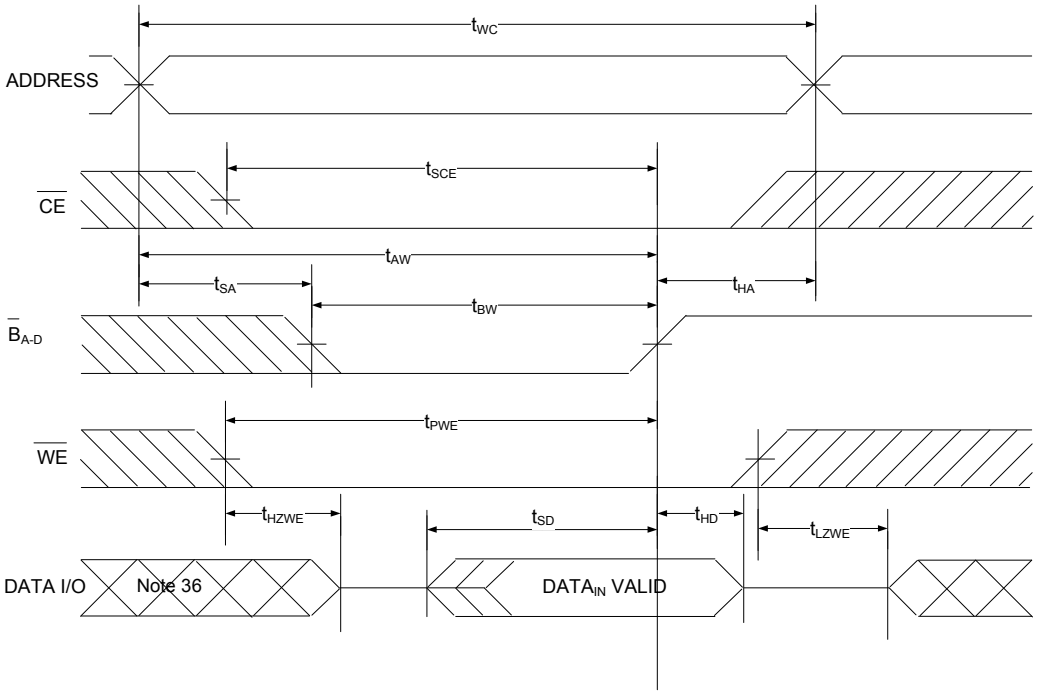
Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ Low)[28, 29, 30, 31]



Notes

28. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
30. Data I/O is high impedance if $\overline{OE}$ or $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ = V_{IH}.
31. The minimum write cycle pulse width should be equal to sum of t_{HZWE} and t_{SD}.
32. During this period I/O are in output state. Do not apply input signals.

Figure 9. Write Cycle No. 3 ($\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$ Controlled)[33, 34, 35]



Notes

33. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, or $\overline{CE_3}$ HIGH.
34. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
35. Data I/O is high impedance if $\overline{OE}$ or $\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$ = V_{IH}.
36. During this period I/O are in output state. Do not apply input signals.

Truth Table – CY7C1062GN

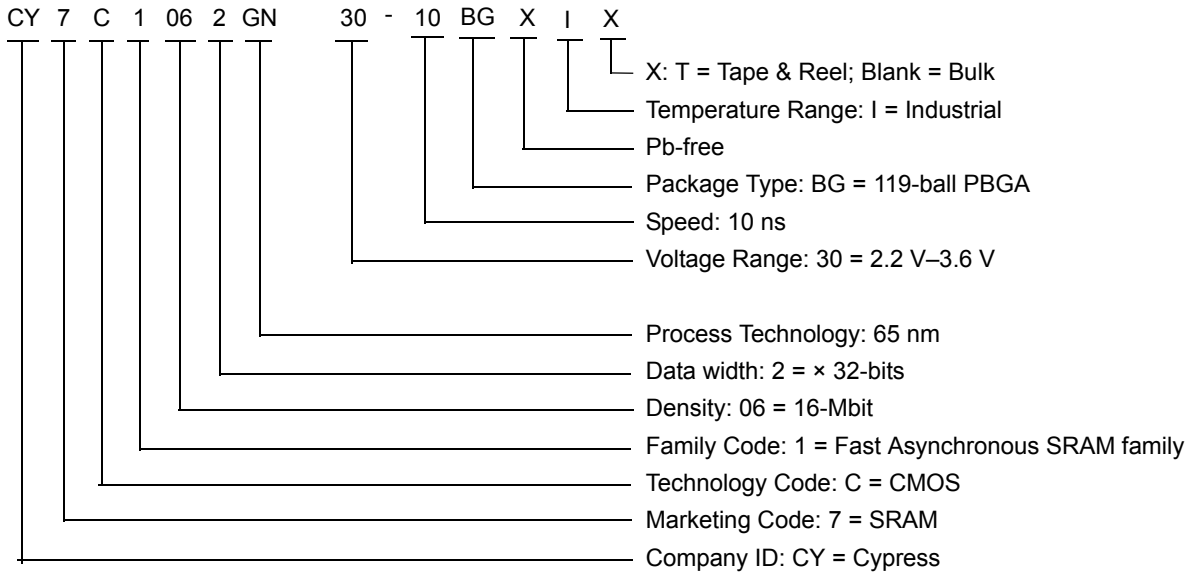
$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	$\overline{OE}$	$\overline{WE}$	$\overline{B_A}$	$\overline{B_B}$	$\overline{B_C}$	$\overline{B_D}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	$I/O_{16}–I/O_{23}$	$I/O_{24}–I/O_{31}$	Mode	Power
H	X[37]	X[37]	X[37]	X[37]	X[37]	X[37]	X[37]	X[37]	High Z	High Z	High Z	High Z	power-down	(I_{SB})
X[37]	H	X[37]	X[37]	X[37]	X[37]	X[37]	X[37]	X[37]	High Z	High Z	High Z	High Z	power-down	(I_{SB})
X[37]	X[37]	H	X[37]	X[37]	X[37]	X[37]	X[37]	X[37]	High Z	High Z	High Z	High Z	power-down	(I_{SB})
L	L	L	L	H	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	(I_{CC})
L	L	L	L	H	L	H	H	H	Data out	High Z	High Z	High Z	Read byte A bits only	(I_{CC})
L	L	L	L	H	H	L	H	H	High Z	Data out	High Z	High Z	Read byte B bits only	(I_{CC})
L	L	L	L	H	H	H	L	H	High Z	High Z	Data out	High Z	Read byte C bits only	(I_{CC})
L	L	L	L	H	H	H	H	L	High Z	High Z	High Z	Data out	Read Byte D bits only	(I_{CC})
L	L	L	X[37]	L	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	(I_{CC})
L	L	L	X[37]	L	L	H	H	H	Data in	High Z	High Z	High Z	Write byte A bits only	(I_{CC})
L	L	L	X[37]	L	H	L	H	H	High Z	Data in	High Z	High Z	Write byte B bits only	(I_{CC})
L	L	L	X[37]	L	H	H	L	H	High Z	High Z	Data in	High Z	Write byte C bits only	(I_{CC})
L	L	L	X[37]	L	H	H	H	L	High Z	High Z	High Z	Data in	Write byte D bits only	(I_{CC})
L	L	L	H	H	X[37]	X[37]	X[37]	X[37]	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I_{CC})
L	L	L	X[37]	X[37]	H	H	H	H	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I_{CC})

Notes
37. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

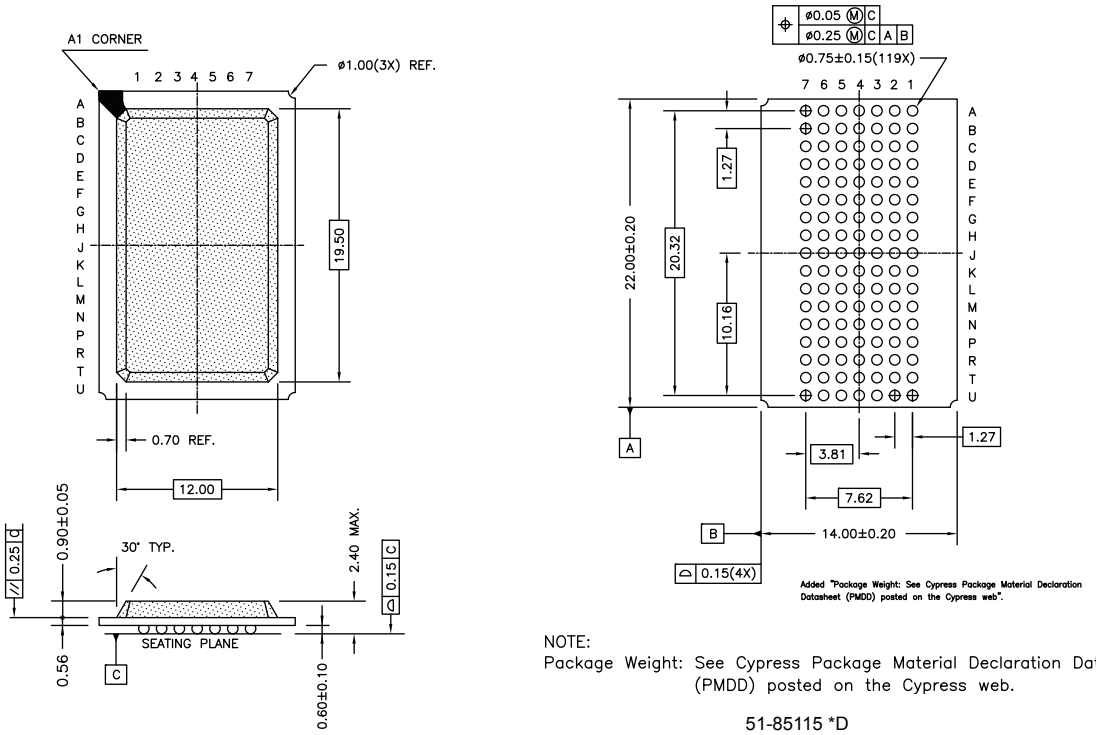
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1062GN30-10BGXI	51-85115	119-ball PBGA	Industrial
		CY7C1062GN30-10BGXIT		119-ball PBGA, Tape & Reel	

Ordering Code Definitions



Package Diagram

Figure 10. 119-pin PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 *D

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
PBGA	Plastic Ball Grid Array
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1062GN, 16-Mbit (512 K words × 32 bits) Static RAM Document Number: 002-13563				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5435066	NILE	09/16/2016	New datasheet
*A	5978656	AESATMP9	11/28/2017	Updated logo and copyright.

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