CY7C130, CY7C130A
CY7C131, CY7C131A

1 K × 8 Dual-Port Static RAM

Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 1 K × 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power: I_{CC} = 110 mA (maximum)
- Fully asynchronous operation
- Automatic power-down
- Master CY7C130/130A/CY7C131/131A easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141
- $\overline{BUSY}$ output flag on CY7C130/130A/CY7C131/131A; $\overline{BUSY}$ input on CY7C140/CY7C141
- $\overline{INT}$ flag for port-to-port communication
- Available in 48-pin DIP (CY7C130/130A/140), 52-pin PLCC, 52-pin TQFP
- Pb-free packages available

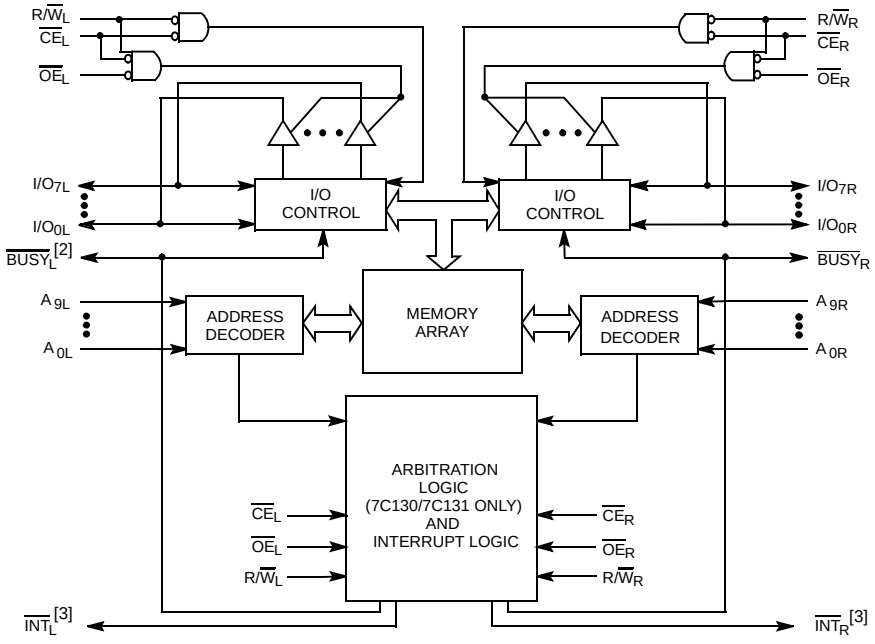
Functional Description

The CY7C130/130A/CY7C131/131A/CY7C140[1] and CY7C141 are high speed CMOS 1 K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/130A/CY7C131/131A can be used as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multi-processor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, BUSY and $\overline{INT}$. BUSY signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data is placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130/130A and CY7C140 are available in 48-pin DIP. The CY7C131/131A and CY7C141 are available in 52-pin PLCC, 52-pin Pb-free PLCC, 52-pin PQFP, and 52-pin Pb-free PQFP.

Logic Block Diagram



Notes
1. CY7C130 and CY7C130A are functionally identical; CY7C131 and CY7C131A are functionally identical.
2. CY7C130/130A/CY7C131/131A (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): BUSY is input.
3. Open drain outputs: pull-up resistor required.

Contents

Pin Configurations

Figure 1. Pin Diagram - DIP (Top View)

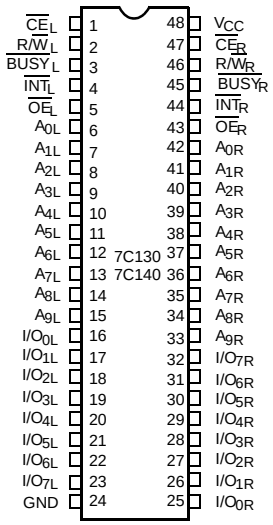


Figure 2. Pin Diagram - PLCC (Top View)

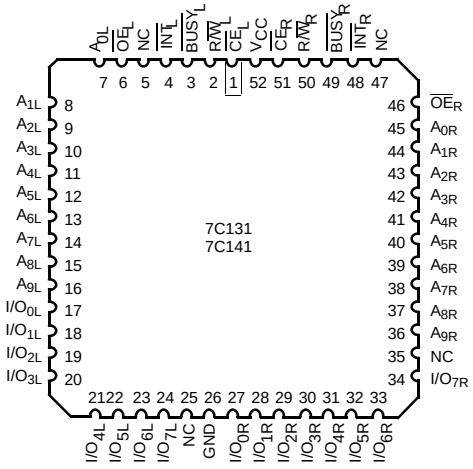
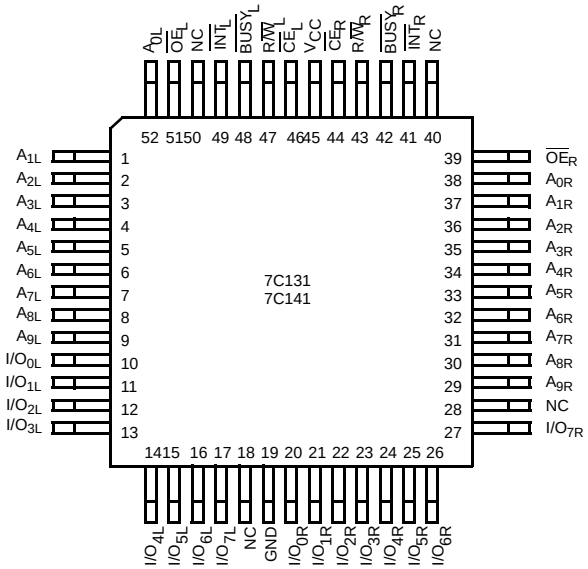


Figure 3. Pin Diagram - PQFP (Top View)



Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/write enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
A_{0L}–$A_{11/12L}$	A_{0R}–$A_{11/12R}$	Address
I/O_{0L}–$I/O_{15/17L}$	I/O_{0R}–$I/O_{15/17R}$	Data bus input/output
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
V_{CC}		Power
GND		Ground

Selection Guide

Parameter		7C131-15[4] 7C131A-15 7C141-15	7C131-25[4] 7C141-25	7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55	Unit
Maximum access time		15	25	30	35	45	55	ns
Maximum operating current	Commercial/ Industrial	190	170	170	120	120	110	mA
Maximum standby current	Commercial/ Industrial	75	65	65	45	45	35	mA

Shaded areas contain preliminary information.

Note
4. 15 and 25 ns version available only in PLCC/PQFP packages.

Maximum Ratings[5]

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential (pin 48 to pin 24).....–0.5 V to +7.0 V

DC voltage applied to outputs in high Z State.....–0.5 V to +7.0 V

DC input voltage .....–3.5 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%
Military[6]	–55 °C to +125 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range[7]

Parameter	Description	Test Conditions		7C131-15[4] 7C131A-15 7C141-15		7C130-30[4] 7C130A-30 7C131-25,30 7C140-30 7C141-25,30		7C130-35,45 7C131-35,45 7C140-35,45 7C141-35,45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	I_{OL} = 4.0 mA		–	0.4	–	0.4	–	0.4	–	0.4	V
		I_{OL} = 16.0 mA[8]		–	0.5	–	0.5	–	0.5	–	0.5	V
V_{IH}	Input HIGH voltage			2.2	–	2.2	–	2.2	–	2.2	–	V
V_{IL}	Input LOW voltage			–	0.8	–	0.8	–	0.8	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–5	+5	–5	+5	–5	+5	–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–5	+5	–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output short circuit current[9, 10]	V_{CC} = Max, V_{OUT} = GND		–	–350	–	–350	–	–350	–	–350	mA
I_{CC}	V_{CC} operating supply current	CE = V_{IL}, outputs open, f = f_{MAX}[11]	Commercial	–	190	–	170	–	120	–	110	mA
I_{SB1}	Standby current both ports, TTL inputs	CE_L and CE_R ≥ V_{IH}, f = f_{MAX}[11]	Commercial	–	75	–	65	–	45	–	35	mA
I_{SB2}	Standby current one port, TTL inputs	CE_L or CE_R ≥ V_{IH}, active port outputs open, f = f_{MAX}[11]	Commercial	–	135	–	115	–	90	–	75	mA
I_{SB3}	Standby current both ports, CMOS inputs	Both ports CE_L and CE_R ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0	Commercial	–	15	–	15	–	15	–	15	mA
I_{SB4}	Standby current one port, CMOS inputs	One port CE_L or CE_R ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, active port outputs open, f = f_{MAX}[11]	Commercial	–	125	–	105	–	85	–	70	mA

Shaded areas contain preliminary information.

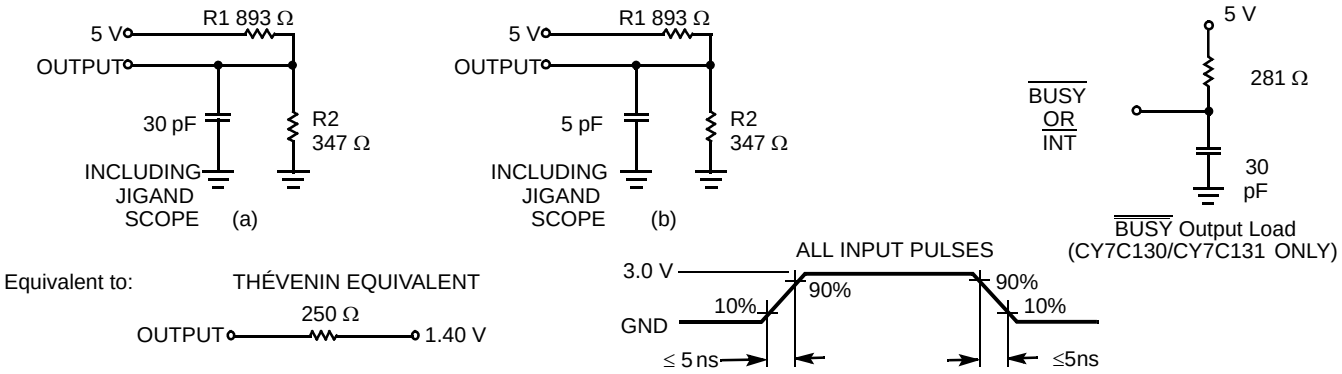
Notes

5. The voltage on any input or I/O pin cannot exceed the power pin during power up.
6. T_A is the "instant on" case temperature
7. See the last page of this specification for Group A subgroup testing information.
8. BUSY and INT pins only.
9. Duration of the short circuit should not exceed 30 seconds.
10. This parameter is guaranteed but not tested.
11. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3 V.

Capacitance[10]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	15	pF
C_{OUT}	Output capacitance		10	pF

Figure 4. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range[12, 13]

Parameter	Description	7C131-15[14] 7C131A-15 7C141-15		7C130-25[14] 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read cycle time	15	–	25	–	30	–	ns
t_{AA}	Address to data valid[15]	–	15	–	25	–	30	ns
t_{OHA}	Data hold from address change	0	–	0	–	0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid[15]	–	15	–	25	–	30	ns
t_{DOE}	$\overline{OE}$ LOW to data valid[15]	–	10	–	15	–	20	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[16, 17, 18]	3	–	3	–	3	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[16, 17, 18]	–	10	–	15	–	15	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[16, 17, 18]	3	–	5	–	5	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[16, 17, 18]	–	10	–	15	–	15	ns
t_{PU}	$\overline{CE}$ LOW to power-up[16]	0	–	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down[16]	–	15	–	25	–	25	ns
Write Cycle[19]								
t_{WC}	Write cycle time	15	–	25	–	30	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	12	–	20	–	25	–	ns
t_{AW}	Address setup to write end	12	–	20	–	25	–	ns
t_{HA}	Address hold from write end	2	–	2	–	2	–	ns
t_{SA}	Address setup to write start	0	–	0	–	0	–	ns
t_{PWE}	R/$\overline{W}$ pulse width	12	–	15	–	25	–	ns
t_{SD}	Data setup to write end	10	–	15	–	15	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{HZWE}	R/$\overline{W}$ LOW to high Z[18]	–	10	–	15	–	15	ns
t_{LZWE}	R/$\overline{W}$ HIGH to low Z[18]	0	–	0	–	0	–	ns

Shaded areas contain preliminary information.

Notes

12. See the last page of this specification for Group A subgroup testing information.
13. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH}, and 30 pF load capacitance.
14. 15 and 25 ns version available only in PLCC/PQFP packages.
15. AC Test Conditions use V_{OH} = 1.6 V and V_{OL} = 1.4 V.
16. This parameter is guaranteed but not tested.
17. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
18. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
19. The internal write time of the memory is defined by the overlap of CS LOW and R/W LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics

Over the Operating Range[12, 13] *(continued)*

Parameter	Description	7C131-15[14] 7C131A-15 7C141-15		7C130-25[14] 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
Busy/Interrupt Timing								
t_{BLA}	$\overline{BUSY}$ LOW from address match	–	15	–	20	–	20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from address mismatch[20]	–	15	–	20	–	20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	15	–	20	–	20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[20]	–	15	–	20	–	20	ns
t_{PS}	Port set-up for priority	5	–	5	–	5	–	ns
t_{WB}[21]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0	–	0	–	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13	–	20	–	30	–	ns
t_{BDD}	$\overline{BUSY}$ HIGH to valid data	–	15	–	25	–	30	ns
t_{DDD}	Write data valid to read data valid	–	Note 22	–	Note 22	–	Note 22	ns
t_{WDD}	Write pulse to data delay	–	Note 22	–	Note 22	–	Note 22	ns
Interrupt Timing								
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ set time	–	15	–	25	–	25	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ set time	–	15	–	25	–	25	ns
t_{INS}	Address to $\overline{INTERRUPT}$ set time	–	15	–	25	–	25	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ reset time[20]	–	15	–	25	–	25	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ reset time[20]	–	15	–	25	–	25	ns
t_{INR}	Address to $\overline{INTERRUPT}$ reset time[20]	–	15	–	25	–	25	ns

Shaded areas contain preliminary information.

Notes

20. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
21. CY7C140/CY7C141 only.
22. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    $\overline{BUSY}$ on Port B goes HIGH.
    Port B's address is toggled.
    $\overline{CE}$ for Port B is toggled.
    R/$\overline{W}$ for Port B is toggled during valid read.

Switching Characteristics

Over the Operating Range[23, 24]

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read cycle time	35	–	45	–	55	–	ns
t_{AA}	Address to data valid[25]	–	35	–	45	–	55	ns
t_{OHA}	Data hold from address change	0	–	0	–	0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid[25]	–	35	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid[25]	–	20	–	25	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[26, 27, 28]	3	–	3	–	3	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[26, 27, 28]	–	20	–	20	–	25	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[26, 27, 28]	5	–	5	–	5	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[26, 27, 28]	–	20	–	20	–	25	ns
t_{PU}	$\overline{CE}$ LOW to power-up[26]	0	–	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down[26]	–	35	–	35	–	35	ns
Write Cycle[29]								
t_{WC}	Write cycle time	35	–	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	30	–	35	–	40	–	ns
t_{AW}	Address set-up to write end	30	–	35	–	40	–	ns
t_{HA}	Address hold from write end	2	–	2	–	2	–	ns
t_{SA}	Address set-up to write start	0	–	0	–	0	–	ns
t_{PWE}	R/$\overline{W}$ pulse width	25	–	30	–	30	–	ns
t_{SD}	Data set-up to write end	15	–	20	–	20	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{HZWE}	R/$\overline{W}$ LOW to high Z[28]	–	20	–	20	–	25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to low Z[28]	0	–	0	–	0	–	ns

Notes
23. See the last page of this specification for Group A subgroup testing information.
24. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH}, and 30 pF load capacitance.
25. AC Test Conditions use V_{OH} = 1.6 V and V_{OL} = 1.4 V.
26. This parameter is guaranteed but not tested.
27. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
28. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
29. The internal write time of the memory is defined by the overlap of CS LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics

Over the Operating Range[23, 24] *(continued)*

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min	Max	Min	Max	Min	Max	
Busy/Interrupt Timing								
t_{BLA}	$\overline{BUSY}$ LOW from address match	–	20	–	25	–	30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from address mismatch[30]	–	20	–	25	–	30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	20	–	25	–	30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[30]	–	20	–	25	–	30	ns
t_{PS}	Port set-up for priority	5	–	5	–	5	–	ns
t_{WB}[31]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0	–	0	–	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	30	–	35	–	35	–	ns
t_{BDD}	$\overline{BUSY}$ HIGH to valid data	–	35	–	45	–	45	ns
t_{DDD}	Write data valid to read data valid	–	Note 32	–	Note 32	–	Note 32	ns
t_{WDD}	Write pulse to data delay	–	Note 32	–	Note 32	–	Note 32	ns
Interrupt Timing								
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ set time	–	25	–	35	–	45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ set time	–	25	–	35	–	45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ set time	–	25	–	35	–	45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ reset time[20]	–	25	–	35	–	45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ reset time[20]	–	25	–	35	–	45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ reset time[20]	–	25	–	35	–	45	ns

Notes
30. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
31. CY7C140/CY7C141 only.
32. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    BUSY on Port B goes HIGH.
    Port B's address is toggled.
    CE for Port B is toggled.
    R/W for Port B is toggled during valid read.

Switching Waveforms

Figure 5. Read Cycle No. 1[33, 34]

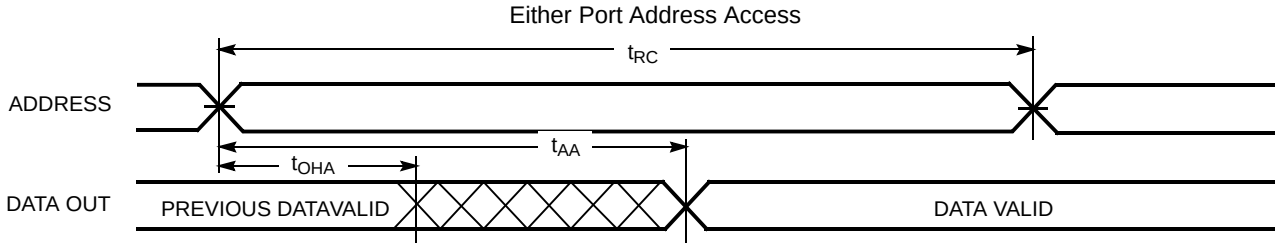


Figure 6. Read Cycle No. 2[33, 35]

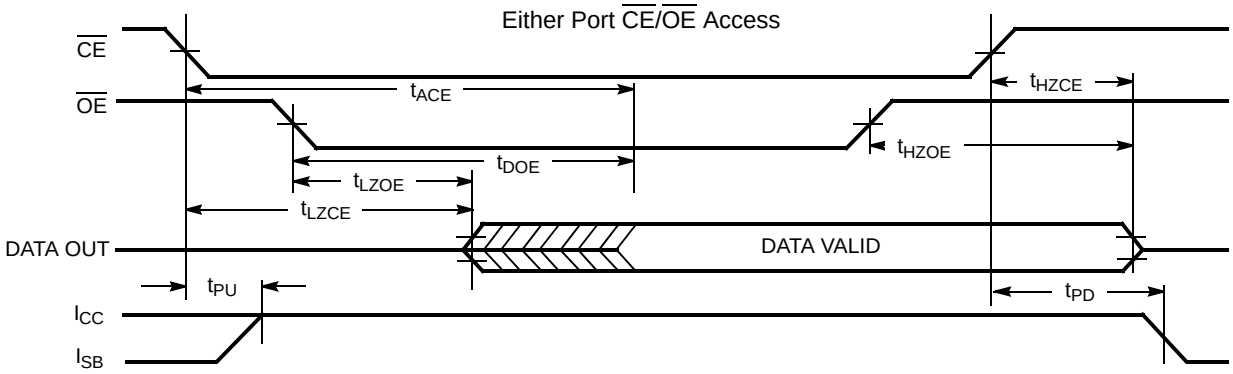
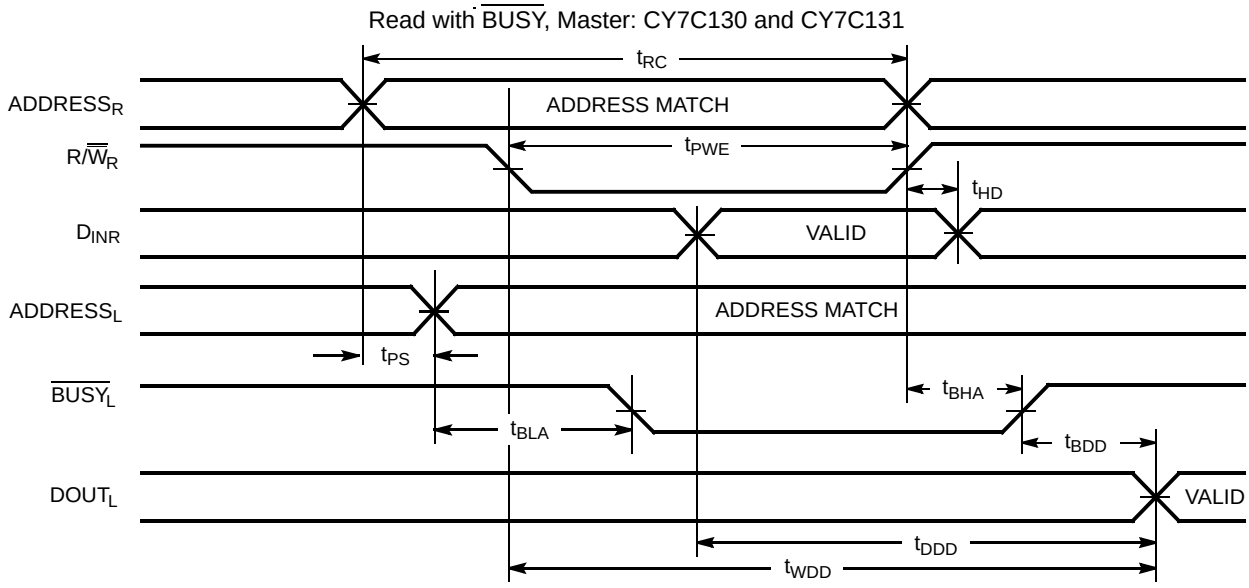


Figure 7. Read Cycle No. 3[34]



Notes
33. R/W is HIGH for read cycle.
34. Device is continuously selected, CE = V_{IL} and OE = V_{IL}.
35. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 1 (OE Three-States Data I/Os—Either Port[36, 37]

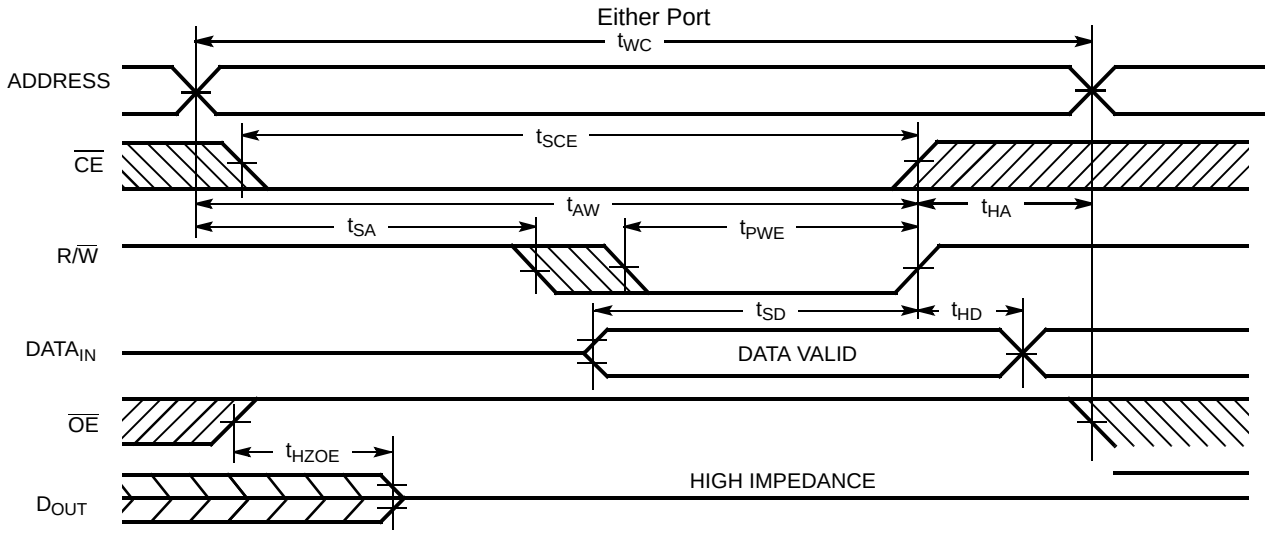
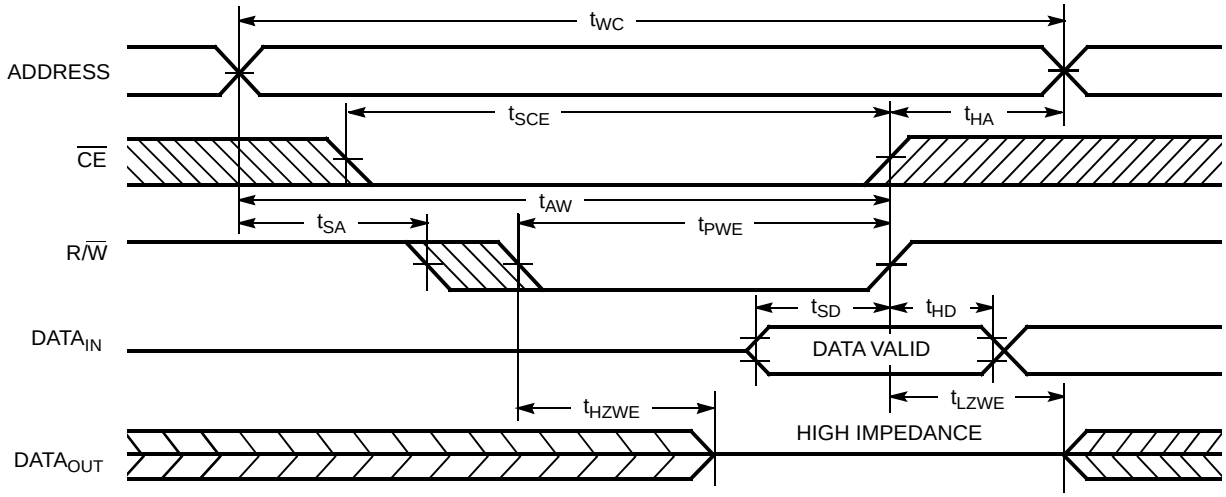


Figure 9. Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port)[38, 39]



Notes

36. The internal write time of the memory is defined by the overlap of CS LOW and R/W LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
37. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
38. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
39. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high impedance state.

Switching Waveforms *(continued)*

Figure 10. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

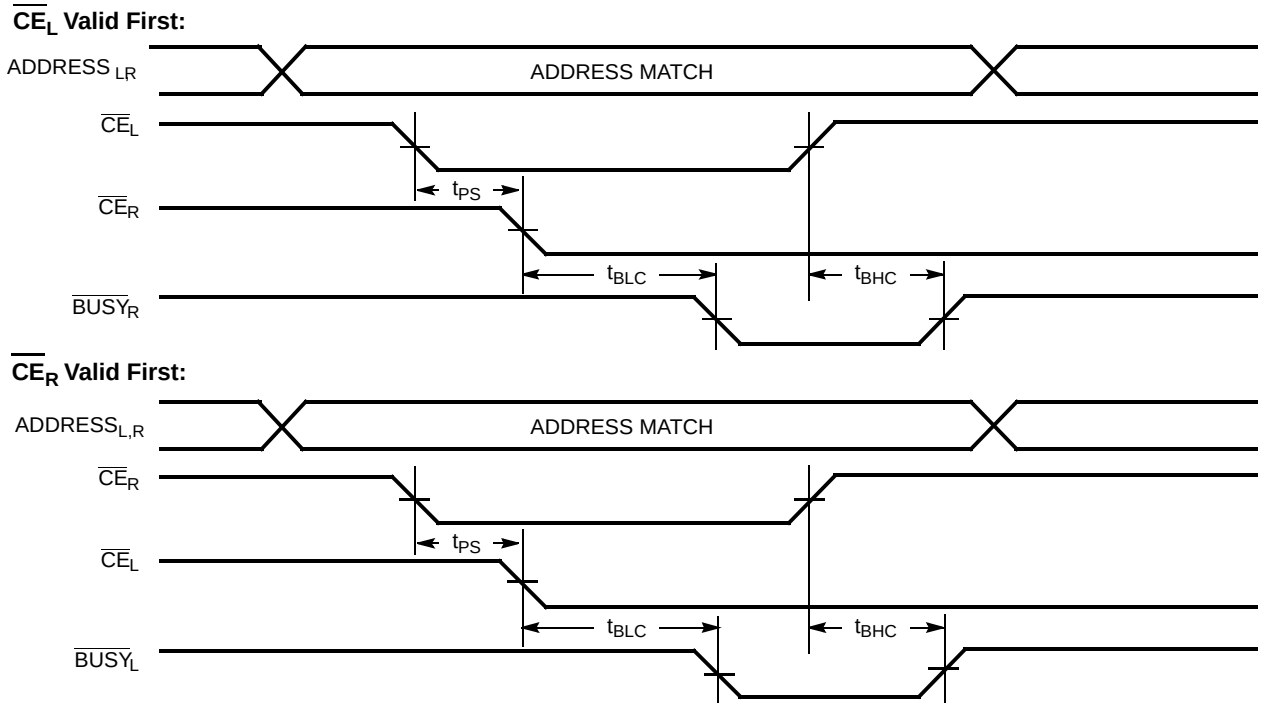
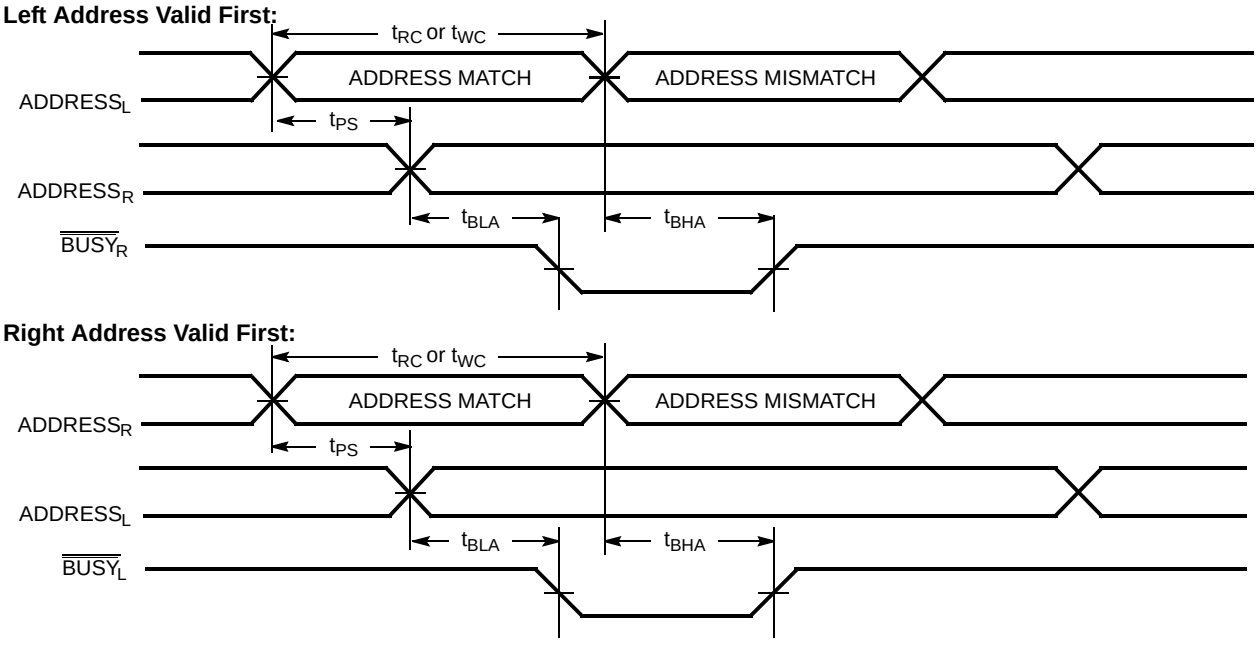
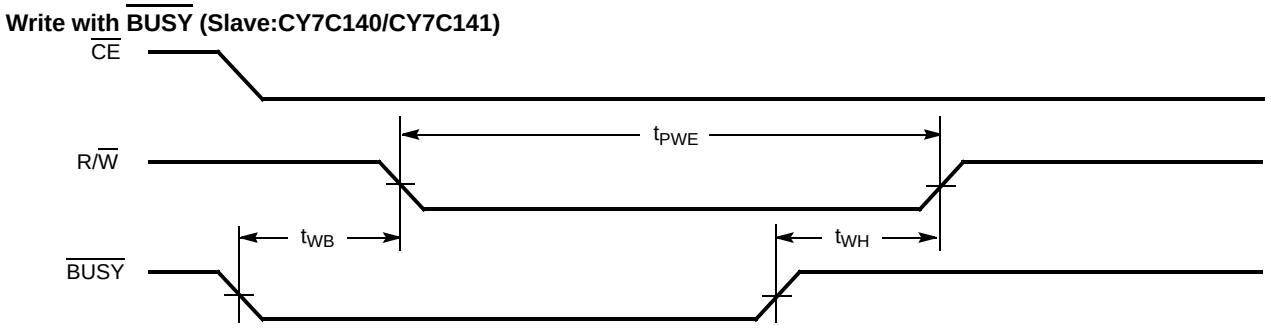


Figure 11. Busy Timing Diagram No. 2 (Address Arbitration)



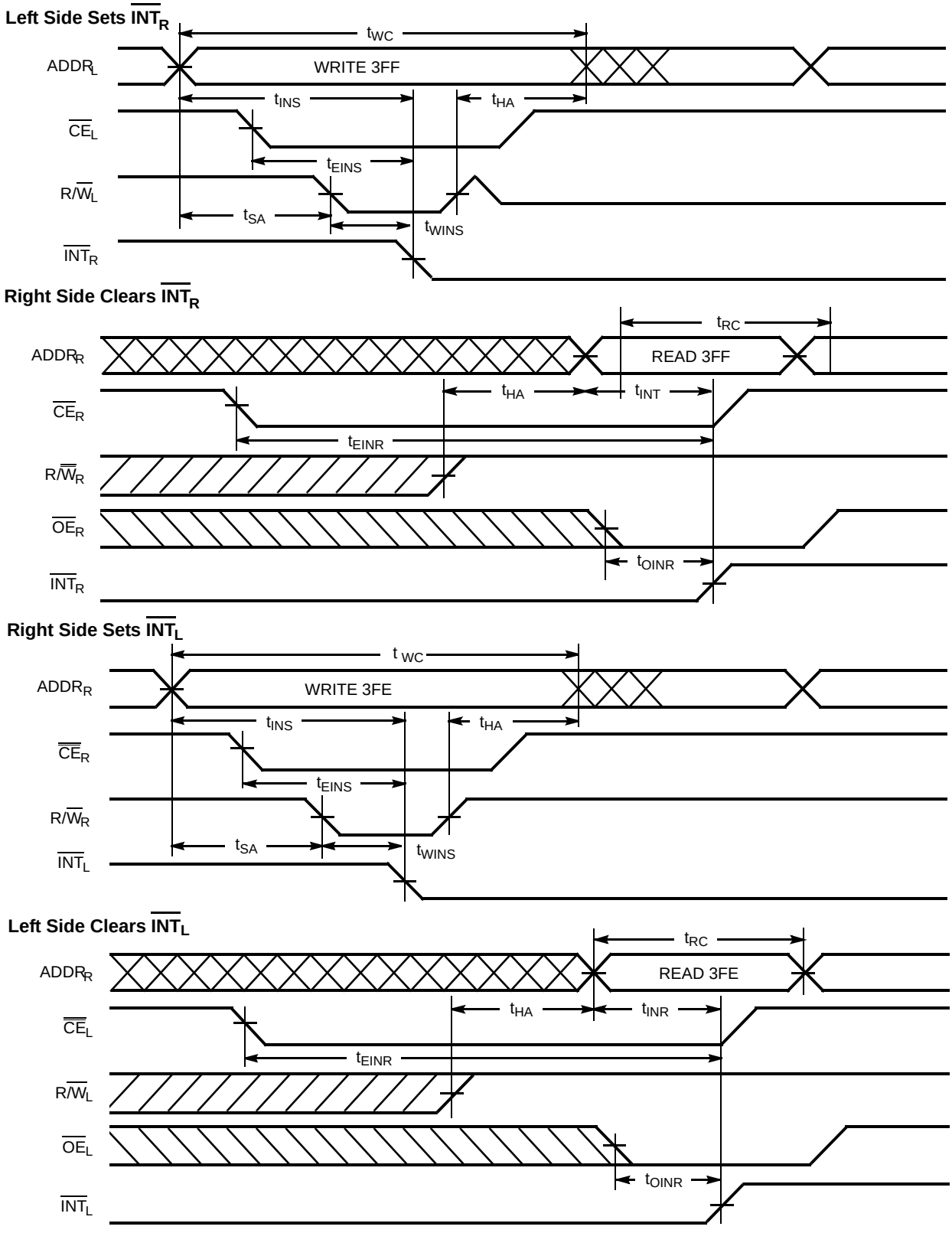
Switching Waveforms *(continued)*

Figure 12. Busy Timing Diagram No. 3



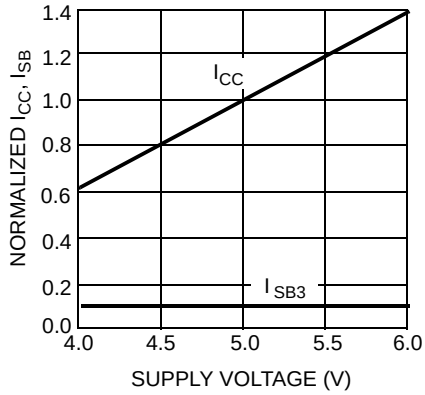
Switching Waveforms *(continued)*

Figure 13. Interrupt Timing Diagrams

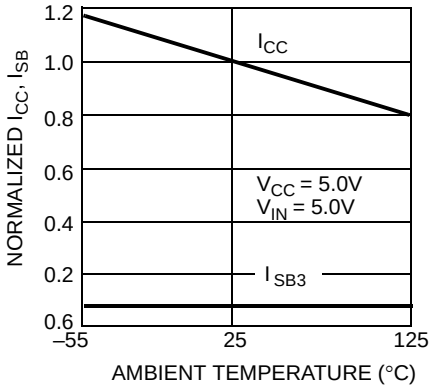


Typical DC and AC Characteristics

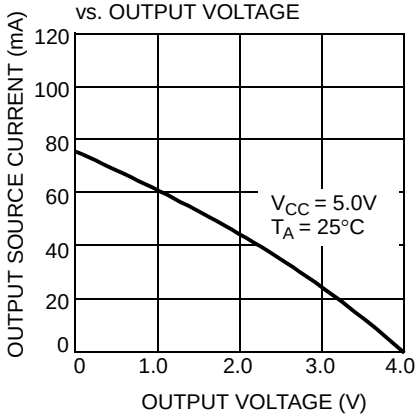
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



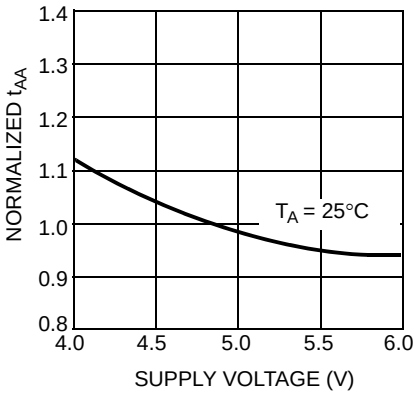
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



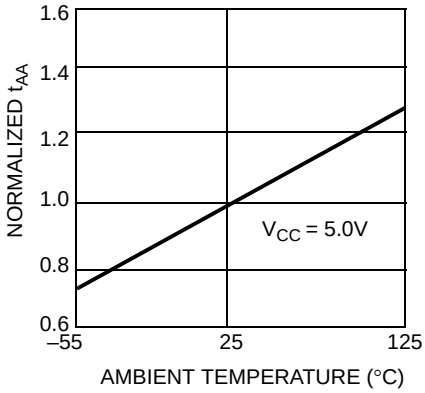
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



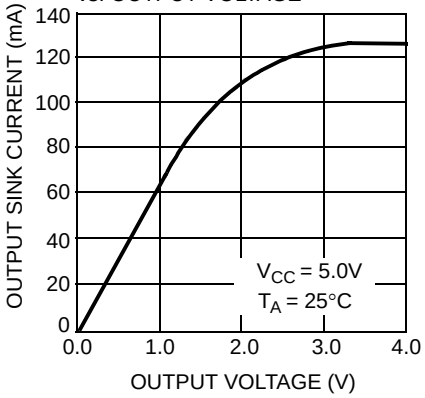
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



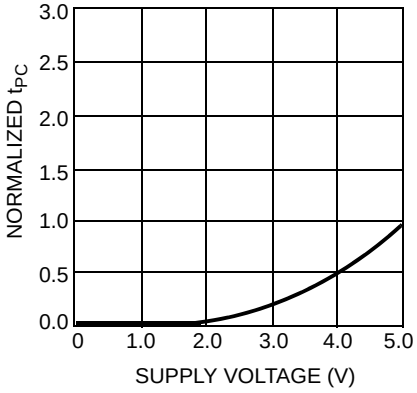
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



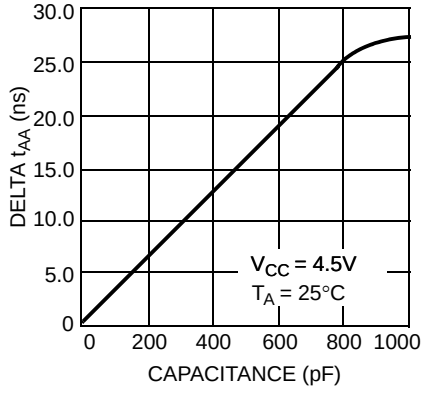
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



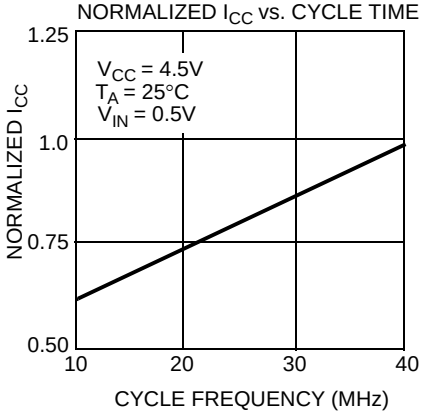
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



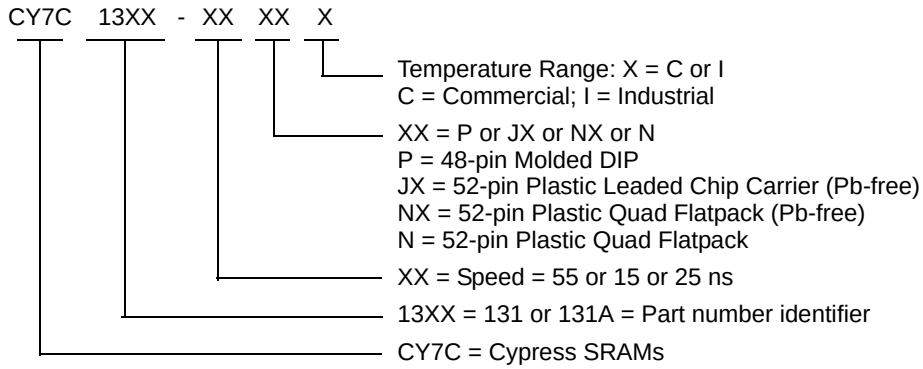
NORMALIZED ICC vs. CYCLE TIME



Ordering Information

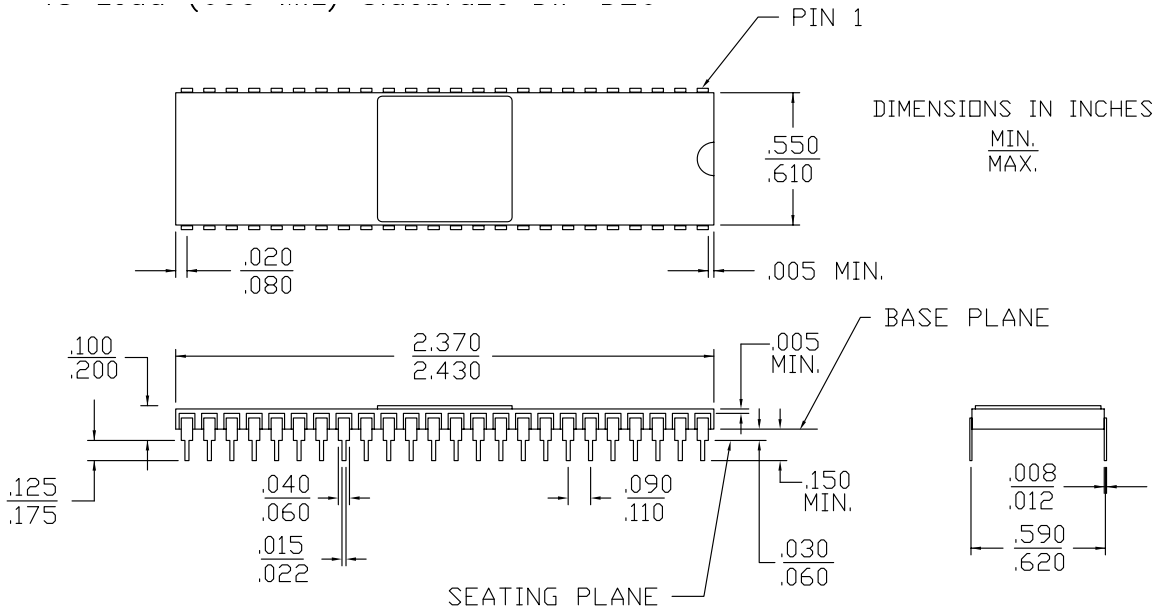
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY7C130-55PC	P25	48-pin (600 Mil) Molded DIP	Commercial
15	CY7C131A-15JXI	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
	CY7C131-15NXI	N52	52-pin Pb-free Plastic Quad Flatpack	
25	CY7C131-25JXC	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C131-25NXC	N52	52-pin Pb-free Plastic Quad Flatpack	
55	CY7C131-55JXC	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C131-55NXC	N52	52-pin Pb-free Plastic Quad Flatpack	
	CY7C131-55JXI	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
	CY7C131-55NXI	N52	52-pin Pb-free Plastic Quad Flatpack	

Ordering Code Definitions



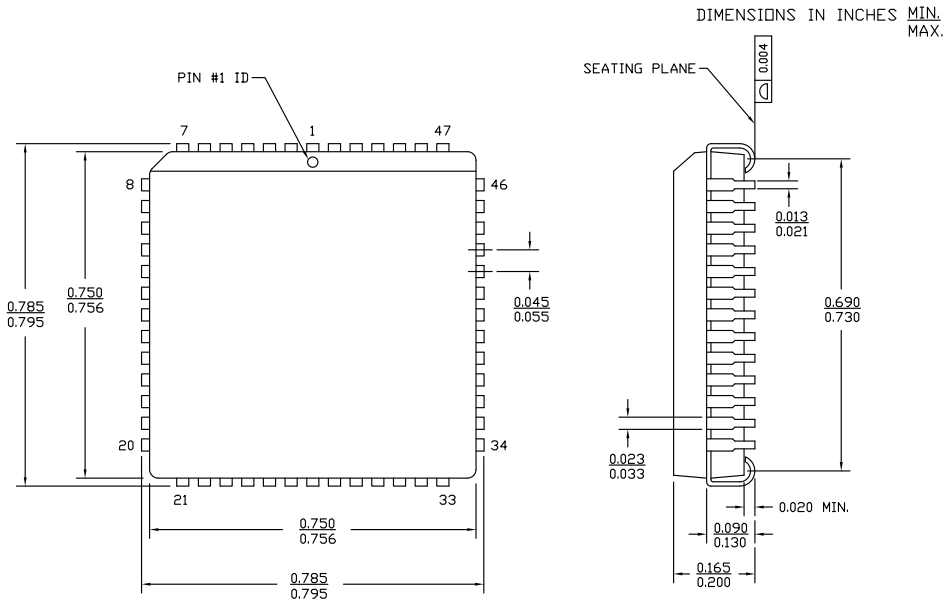
Package Diagrams

Figure 14. 48-pin (600 Mil) Sidebraze DIP D26



51-80044 *B

Figure 15. 52-pin Pb-free Plastic Leaded Chip Carrier J69



51-85004 *C

Package Diagrams *(continued)*

Figure 16. 48-pin (600 Mil) Molded DIP P25

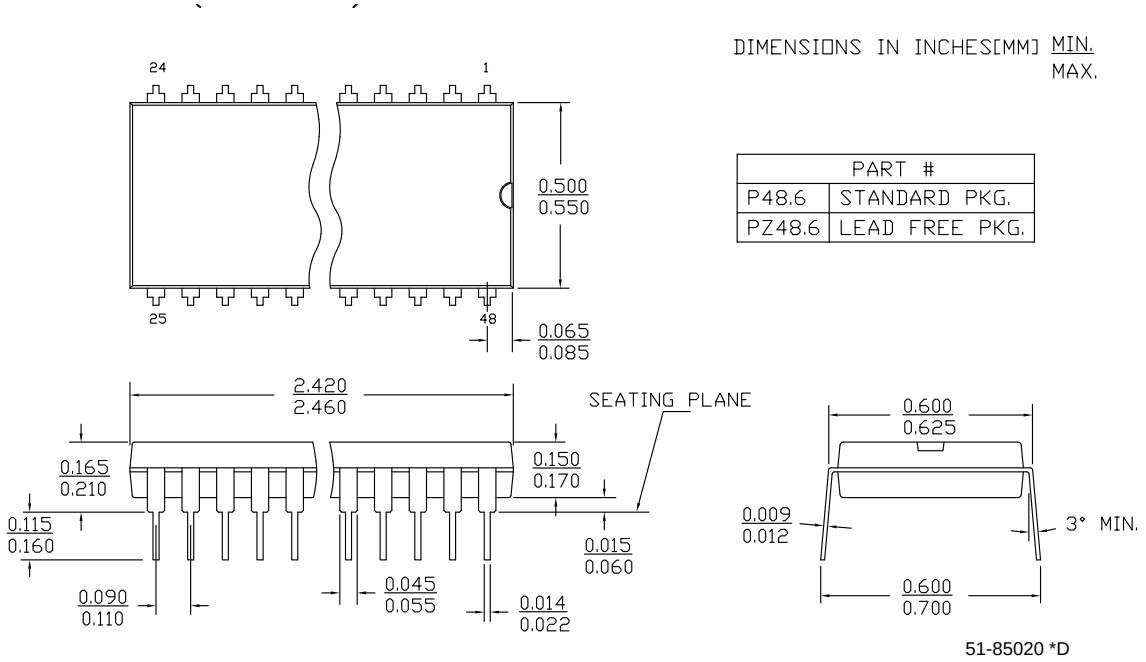
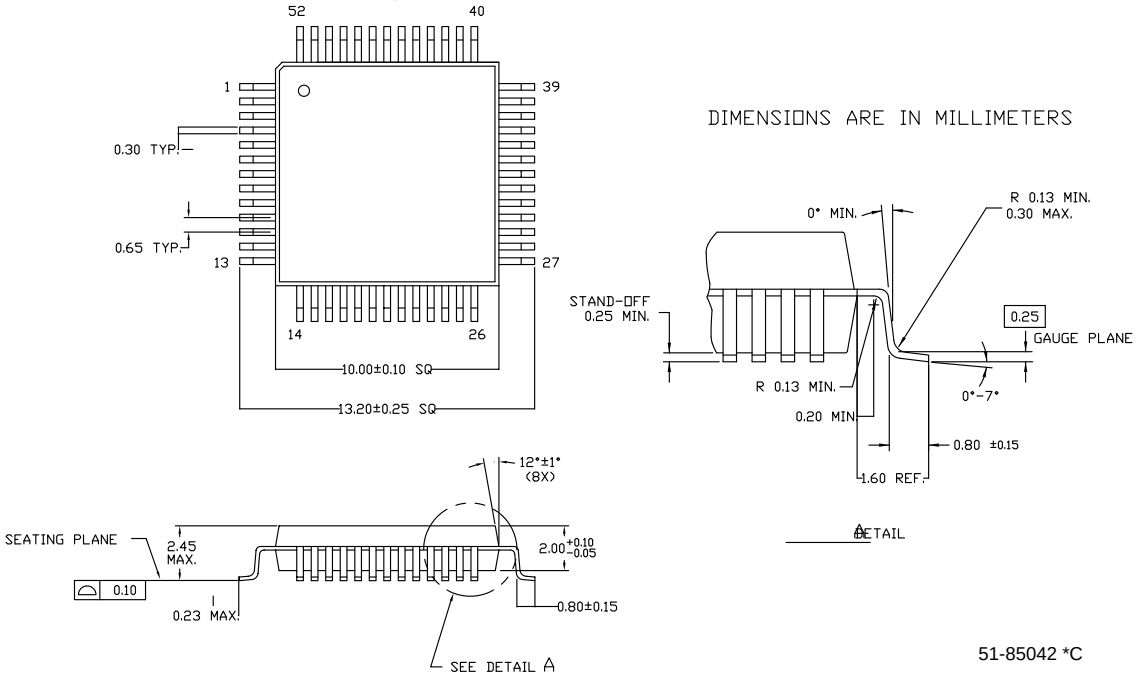


Figure 17. 52-pin Pb-free Plastic Quad Flatpack N52



Acronyms

Acronym	Description
CE	chip enable
CMOS	complementary metal oxide semiconductor
DIP	dual in-line package
I/O	input/output
OE	output enable
PLCC	plastic leaded chip carrier
PQFP	plastic quad flat pack
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	Transistor–transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celcius
MHz	megahertz
µA	microamperes
mA	milliamperes
ms	milliseconds
mV	millivolts
ns	nanoseconds
pF	picofarad
V	volts
W	watts

Document History Page

Document Title: CY7C130/CY7C130A/CY7C131/CY7C131A 1K x 8 Dual-Port Static RAM Document Number: 38-06002				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110169	SZV	09/29/01	Change from Spec number: 38-00027 to 38-06002
*A	122255	RBI	12/26/02	Power up requirements added to Maximum Ratings Information
*B	236751	YDT	See ECN	Removed cross information from features section
*C	325936	RUY	See ECN	Added pin definitions table, 52-pin PQFP package diagram and Pb-free information
*D	393153	YIM	See ECN	Added CY7C131-15JI to ordering information Added Pb-Free parts to ordering information: CY7C131-15JXI
*E	2623540	VKN/PYRS	12/17/08	Added CY7C130A and CY7C131A parts Removed military information Updated ordering information table
*F	2897217	RAME	03/22/2010	Updated Ordering Information Updated Package Diagrams
*G	3054633	ADMU	10/11/2010	Updated Ordering Information and added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Minor edits and updated in new template.
*H	3402163	ADMU	10/12/2011	Removed pruned part CY7C131-25NC from Ordering Information Updated Package Diagrams.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for SRAM ***category:***

Click to view products by Cypress ***manufacturer:***

Other Similar products are found below :

5962-8855206XA CY6116A-35DMB CY7C128A-45DMB CY7C1461KV33-133AXI CY7C199-45LMB CYDM128B16-55BVXIT GS8161Z36DD-200I GS88237CB-200I R1QDA7236ABB-20IB0 RMLV0408EGSB-4S2#AA0 IS64WV3216BLL-15CTLA3 IS66WVE4M16ECLL-70BLI PCF8570P K6T4008C1B-GB70 CY7C1353S-100AXC AS6C8016-55BIN 515712X IS62WV51216EBLL-45BLI IS63WV1288DBLL-10HLI IS66WVE2M16ECLL-70BLI 47L16-E/SN IS66WVE4M16EALL-70BLI IS62WV6416DBLL-45BLI IS61WV102416DBLL-10TLI CY7C1381KV33-100AXC CY7C1381KV33-100BZXI CY7C1373KV33-100AXC CY7C1381KVE33-133AXI CY7C4042KV13-933FCXC 8602501XA 5962-3829425MUA 5962-8855206YA 5962-8866201XA 5962-8866201YA 5962-8866204TA 5962-8866206MA 5962-8866207NA 5962-8866208UA 5962-8872502XA 5962-8959836MZA 5962-8959841MZA 5962-9062007MXA 5962-9161705MXA N08L63W2AB7I 7130LA100PDG GS81284Z36B-250I M38510/28902BVA IS62WV12816ALL-70BLI 5962-8971203XA 5962-8971202ZA