

1 K / 2 K × 8 Dual-port Static RAM

Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 1 K / 2 K × 8 organization
- 0.35 micron complementary metal oxide semiconductor (CMOS) for optimum speed and power
- High speed access: 15 ns
- Low operating power: $I_{CC} = 110$ mA (typical), Standby: $I_{SB3} = 0.05$ mA (typical)
- Fully asynchronous operation
- Automatic power-down
- \overline{BUSY} output flag to indicate access to the same location by both ports
- \overline{INT} flag for port-to-port communication
- Available in 52-pin plastic leaded chip carrier (PLCC), 52-pin plastic quad flat package (PQFP)
- Pb-free packages available

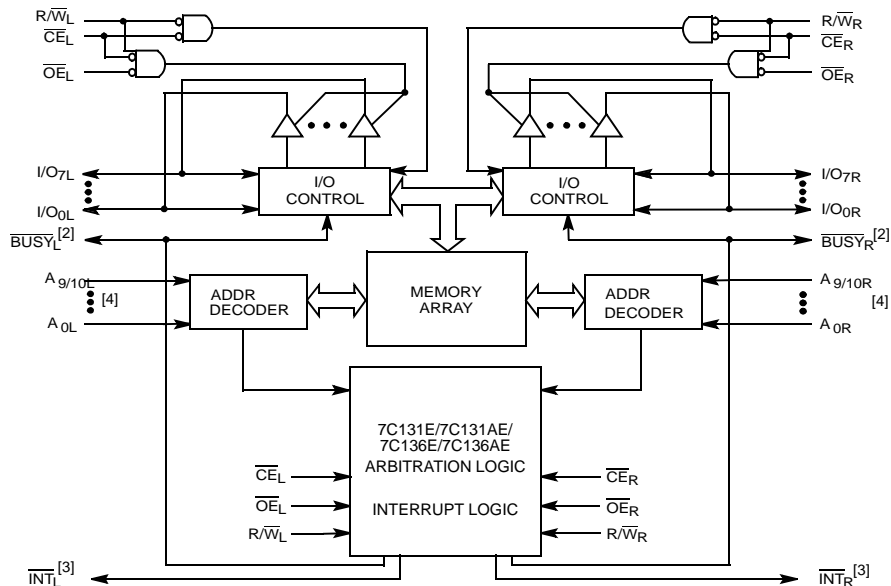
Functional Description

CY7C131E / CY7C131AE / CY7C136E / CY7C136AE are high-speed, low-power CMOS 1 K / 2 K × 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C131E / CY7C131AE / CY7C136E / CY7C136AE can be used as a standalone dual-port static RAM. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multi-processor designs.

Each port has independent control pins; chip enable (\overline{CE}), write enable (R/W), and output enable (\overline{OE}). Two flags are provided on each port, \overline{BUSY} and \overline{INT} . The \overline{BUSY} flag signals that the port is trying to access the same location, which is currently being accessed by the other port. The \overline{INT} is an interrupt flag indicating that data is placed in a unique location^[1]. The \overline{BUSY} and \overline{INT} flags are push pull outputs. An automatic power-down feature is controlled independently on each port by the chip enable (CE) pins.

The CY7C131E / CY7C131AE / CY7C136E / CY7C136AE are available in 52-pin Pb-free PLCC and 52-pin Pb-free PQFP.

Logic Block Diagram



Notes

1. Unique location used by interrupt flag: 1 K × 8: Left port reads from 3FE, Right port reads from 3FF; 2 K × 8: Left port reads from 7FE, Right port reads from 7FF.
2. \overline{BUSY} is a push-pull output. No pull-up resistor required.
3. \overline{INT} : push-pull output. No pull-up resistor required.
4. 1 K × 8: A0–A9, 2 K × 8: A0–A10, address lines are for both left and right ports.

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Pin Configurations

Figure 1. Pin Diagram - 52-pin PLCC (Top View)

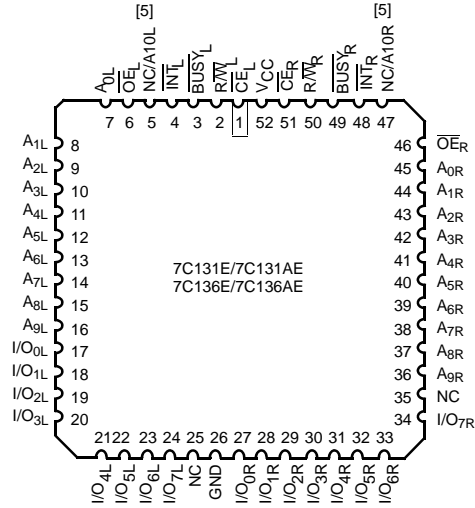
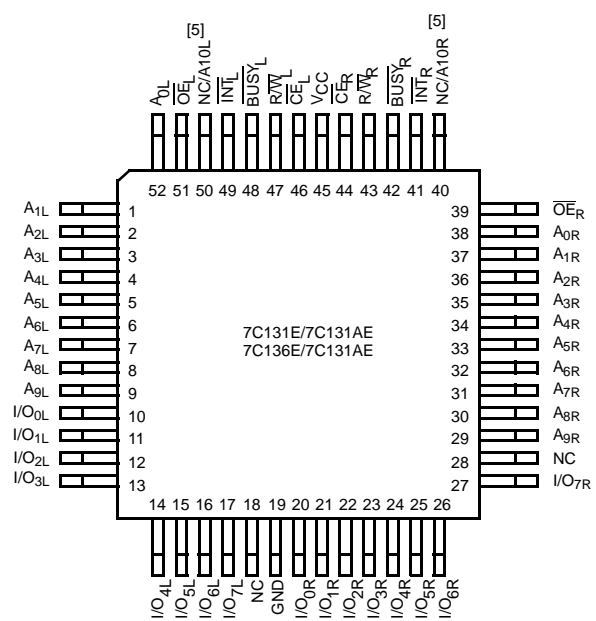


Figure 2. Pin Diagram - 52-pin PQFP (Top View)



Pin Definitions

Left Port	Right Port	Description
\overline{CE}_L	\overline{CE}_R	Chip Enable
$\overline{R/W}_L$	$\overline{R/W}_R$	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
$A_{0L}-A_{9/10L}^{[5]}$	$A_{0R}-A_{9/10R}^{[5]}$	Address
$I/O_{0L}-I/O_{7L}$	$I/O_{0R}-I/O_{7R}$	Data Bus Input/Output
\overline{INT}_L	\overline{INT}_R	Interrupt Flag
\overline{BUSY}_L	\overline{BUSY}_R	Busy Flag
V_{CC}		Power
GND		Ground

Selection Guide

Parameter	7C131E-15 7C131AE-15	7C131E-25 7C136E-25	7C131E-55 7C136E-55 7C136AE-55	Unit
Maximum Access Time	15	25	55	ns
Typical Operating Current	110	100	95	mA
Typical Standby Current for I_{SB1} (both ports TTL level)	50	45	45	mA
Typical Standby Current for I_{SB3} (Both ports CMOS level)	0.05	0.05	0.05	mA

Note

5. 1 K x 8: A0-A9, 2 K x 8: A0-A10, address lines are for both left and right ports.

Maximum Ratings

Exceeding maximum ratings ^[6] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage to ground potential -0.3 V to +7.0 V
 DC voltage applied to outputs in High Z State -0.5 V to +7.0 V

DC input voltage^[8] -0.5 V to +7.0 V
 Output current into outputs (LOW) 20 mA
 Static discharge voltage >1100 V
 Latch up current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	-40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C131E-15 7C131AE-15			7C131E-25 7C136E-25			7C131E-55 7C136E-55 7C136AE-55			Unit
			Min	Typ ^[9]	Max	Min	Typ ^[9]	Max	Min	Typ ^[9]	Max	
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = -4.0 mA	2.4	-	-	2.4	-	-	2.4	-	-	V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 4.0 mA	-	-	0.4	-	-	0.4	-	-	0.4	V
V _{IH}	Input HIGH Voltage		2.2	-	-	2.2	-	-	2.2	-	-	V
V _{IL}	Input LOW Voltage		-	-	0.8	-	-	0.8	-	-	0.8	V
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output disabled	-20	-	+20	-20	-	+20	-20	-	+20	µA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, I _{OUT} = 0 mA Outputs disabled	-	110 115	190 200	-	100 110	170 180	-	95 105	160 170	mA
I _{SB1}	Standby Current, Both Ports, TTL Inputs	CE _L and CE _R ≥ V _{IH} , f = f _{MAX} ^[7]	-	50 65	70 95	-	45 65	65 95	-	45 65	65 95	mA
I _{SB2}	Standby Current, One Port, TTL Inputs	CE _L or CE _R ≥ V _{IH} , Active Port Outputs Open, f = f _{MAX} ^[7]	-	120 135	180 205	-	110 135	160 205	-	110 135	160 205	mA
I _{SB3}	Standby Current, Both Ports, CMOS Inputs	<u>Both Ports</u> CE _L and CE _R ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0	-	0.05 0.05	0.5 0.5	-	0.05 0.05	0.5 0.5	-	0.05 0.05	0.5 0.5	mA
I _{SB4}	Standby Current, One Port, CMOS Inputs	<u>One Port</u> CE _L or CE _R ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, Active Port Outputs Open, f = f _{MAX} ^[7]	-	110 125	160 175	-	100 125	140 175	-	100 125	140 175	mA

Notes

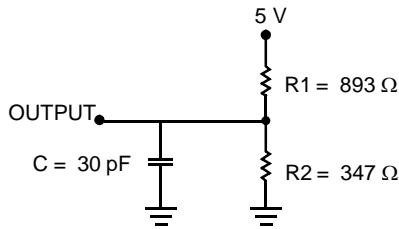
- The voltage on any I/O pin cannot exceed the power pin during power-up.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{RC} and using AC Test Waveforms input levels of GND to 3 V.
- Pulse width < 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ.), T_A = 25 °C.

Capacitance^[10]

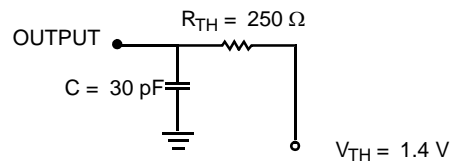
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$	15	pF
C_{OUT}	Output capacitance		10	pF

AC Test Loads and Waveforms

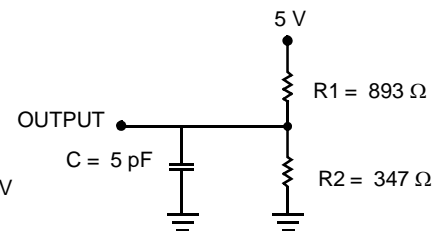
Figure 3. AC Test Loads and Waveforms



(a) Normal Load (Load 1)

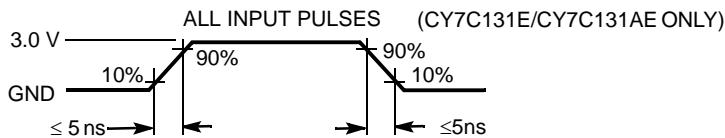


(b) Thévenin Equivalent (Load 1)



(c) Three-State Delay (Load 2)

(Used for t_{LZ} , t_{HZ} , t_{HZWE} , and t_{LZWE} including scope and jig)



Note

10. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter ^[11]	Description	7C131E-15/7C131AE-15		7C131E-25/7C136E-25		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	15	–	25	–	ns
t_{AA}	Address to data valid ^[12]	–	15	–	25	ns
t_{OHA}	Data hold from Address change	3	–	3	–	ns
t_{ACE}	\overline{CE} LOW to data valid ^[12]	–	15	–	25	ns
t_{DOE}	\overline{OE} LOW to data valid ^[12]	–	10	–	15	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[13, 14, 15]	3	–	3	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[13, 14, 15]	–	10	–	15	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[13, 14, 15]	3	–	5	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[13, 14, 15]	–	10	–	15	ns
t_{PU}	\overline{CE} LOW to power-up ^[13]	0	–	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down ^[13]	–	15	–	25	ns
Write Cycle ^[16]						
t_{WC}	Write cycle time	15	–	25	–	ns
t_{SCE}	\overline{CE} LOW to write end	12	–	20	–	ns
t_{AW}	Address setup to write end	12	–	20	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	R/ \overline{W} pulse width	10	–	12	–	ns
t_{SD}	Data setup to write end	10	–	15	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
$t_{HZWE}^{[13]}$	R/ \overline{W} LOW to High Z ^[15]	–	10	–	15	ns
$t_{LZWE}^{[13]}$	R/ \overline{W} HIGH to Low Z ^[15]	3	–	3	–	ns

Notes

11. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
12. AC Test Conditions use $V_{OH} = 1.6$ V and $V_{OL} = 1.4$ V.
13. This parameter is guaranteed but not tested.
14. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE} .
15. Parameters t_{LZCE} , t_{LZWE} , t_{HZOE} , t_{LZOE} , t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in part (c) of [Figure 3 on page 5](#). Transition is measured ± 500 mV from steady state voltage.
16. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and R/ \overline{W} LOW. Both signals must be low to initiate a write and either signal can terminate

Switching Characteristics (continued)

Over the Operating Range

Parameter ^[11]	Description	7C131E-15/7C131AE-15		7C131E-25/7C136E-25		Unit
		Min	Max	Min	Max	
Busy/Interrupt Timing^[17]						
t _{BLA}	BUSY LOW from Address match	–	15	–	20	ns
t _{BHA}	BUSY HIGH from Address mismatch ^[18]	–	15	–	20	ns
t _{BLC}	BUSY LOW from CE LOW	–	15	–	20	ns
t _{BHC}	BUSY HIGH from CE HIGH ^[18]	–	15	–	20	ns
t _{PS}	Port setup for priority	5	–	5	–	ns
t _{BDD}	BUSY HIGH to valid data	–	15	–	25	ns
t _{DDD}	Write data valid to read data valid ^[19]	–	25	–	30	ns
t _{WDD}	Write pulse to data delay ^[19]	–	30	–	45	ns
Interrupt Timing						
t _{WINS}	R/W to INTERRUPT set time	–	15	–	25	ns
t _{EINS}	CE to INTERRUPT set time	–	15	–	25	ns
t _{INS}	Address to INTERRUPT set time	–	15	–	25	ns
t _{OINR}	OE to INTERRUPT reset time ^[18]	–	15	–	25	ns
t _{EINR}	CE to INTERRUPT reset time ^[18]	–	15	–	25	ns
t _{INR}	Address to INTERRUPT reset time ^[18]	–	15	–	25	ns

Notes

17. Test conditions used are Load 2.

18. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

19. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
 BUSY on Port B goes HIGH.
 Port B's address toggled.
 CE for Port B is toggled.

Switching Characteristics

Over the Operating Range

Parameter	Description	7C131E-55 7C136E-55 7C136AE-55		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	55	–	ns
t _{AA}	Address to data valid ^[21]	–	55	ns
t _{OHA}	Data hold from Address change	3	–	ns
t _{ACE}	CE LOW to data valid ^[21]	–	55	ns
t _{DOE}	OE LOW to data valid ^[21]	–	25	ns
t _{LZOE}	OE LOW to Low Z ^[21, 22, 23]	3	–	ns
t _{HZOE}	OE HIGH to High Z ^[21, 22, 23]	–	25	ns
t _{LZCE}	CE LOW to Low Z ^[21, 22, 23]	5	–	ns
t _{HZCE}	CE HIGH to High Z ^[21, 22, 23]	–	25	ns
t _{PU}	CE LOW to power-up ^[22]	0	–	ns
t _{PD}	CE HIGH to power-down ^[22]	–	35	ns
Write Cycle				
t _{WC}	Write cycle time	55	–	ns
t _{SCE}	CE LOW to write end	40	–	ns
t _{AW}	Address setup to write end	40	–	ns
t _{HA}	Address hold from write end	2	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	R/W pulse width	30	–	ns
t _{SD}	Data setup to write end	20	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	R/W LOW to High Z ^[24]	–	25	ns
t _{LZWE}	R/W HIGH to Low Z ^[24]	3	–	ns
Busy/Interrupt Timing ^[20]				
t _{BLA}	BUSY LOW from Address match	–	30	ns
t _{BHA}	BUSY HIGH from Address mismatch ^[25]	–	30	ns
t _{BLC}	BUSY LOW from CE LOW	–	30	ns
t _{BHC}	BUSY HIGH from CE HIGH ^[25]	–	30	ns
t _{PS}	Port setup for priority	5	–	ns
t _{BDD}	BUSY HIGH to valid data	–	45	ns

Notes

20. Test conditions used are Load 2.

21. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and $\overline{R/W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

22. AC Test Conditions use $V_{OH} = 1.6$ V and $V_{OL} = 1.4$ V.

23. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

24. Parameters t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C = 5 pF as in part (b) of Figure 3 on page 5. Transition is measured ±500 mV from steady state voltage.

25. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:

BUSY on Port B goes HIGH.

Port B's address toggled.

Switching Characteristics (continued)

Over the Operating Range

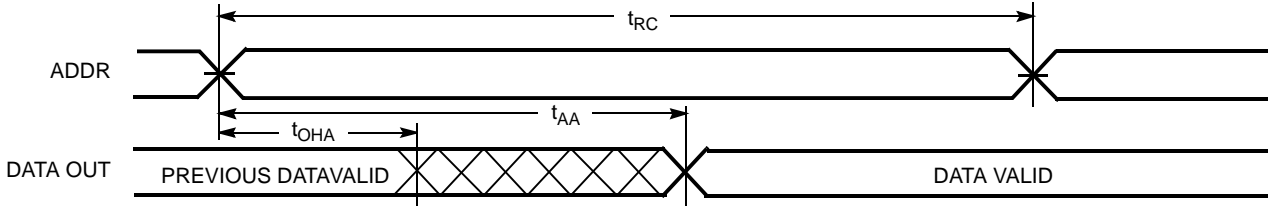
Parameter	Description	7C131E-55 7C136E-55 7C136AE-55		Unit
		Min	Max	
t_{DDD}	Write data valid to read data valid ^[26]	–	30	ns
t_{WDD}	Write pulse to data delay ^[26]	–	45	ns
Interrupt Timing				
t_{WINS}	R/W to INTERRUPT set time	–	45	ns
t_{EINS}	CE to INTERRUPT set time	–	45	ns
t_{INS}	Address to INTERRUPT set time	–	45	ns
t_{OINR}	OE to INTERRUPT reset time ^[27]	–	45	ns
t_{EINR}	CE to INTERRUPT reset time ^[27]	–	45	ns
t_{INR}	Address to INTERRUPT reset time ^[27]	–	45	ns

Notes

26. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
 BUSY on Port B goes HIGH.
 Port B's address toggled.
 CE for Port B is toggled.
 R/W for Port B is toggled during valid read.
27. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

Switching Waveforms

**Figure 4. Read Cycle No. 1 [28, 29]
Either Port ADDR Access**



**Figure 5. Read Cycle No. 2 [28, 30]
Either Port $\overline{CE}/\overline{OE}$ Access**

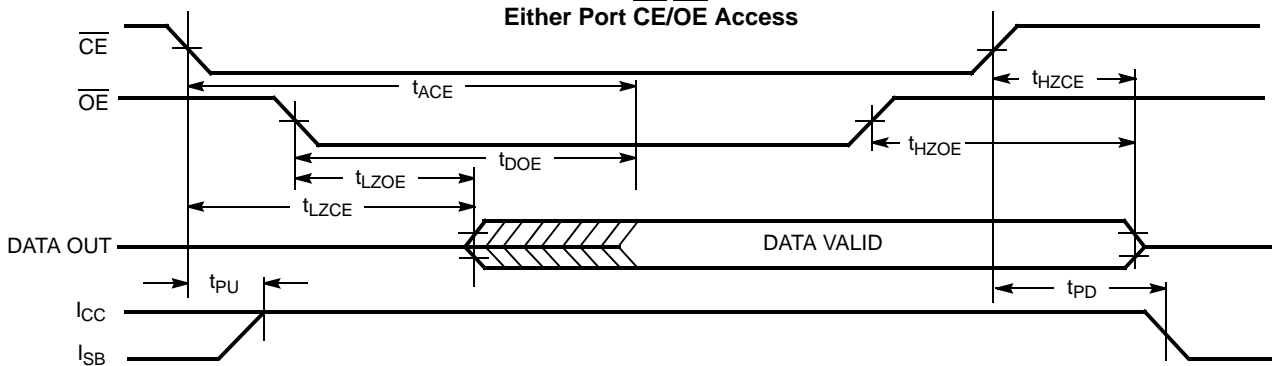
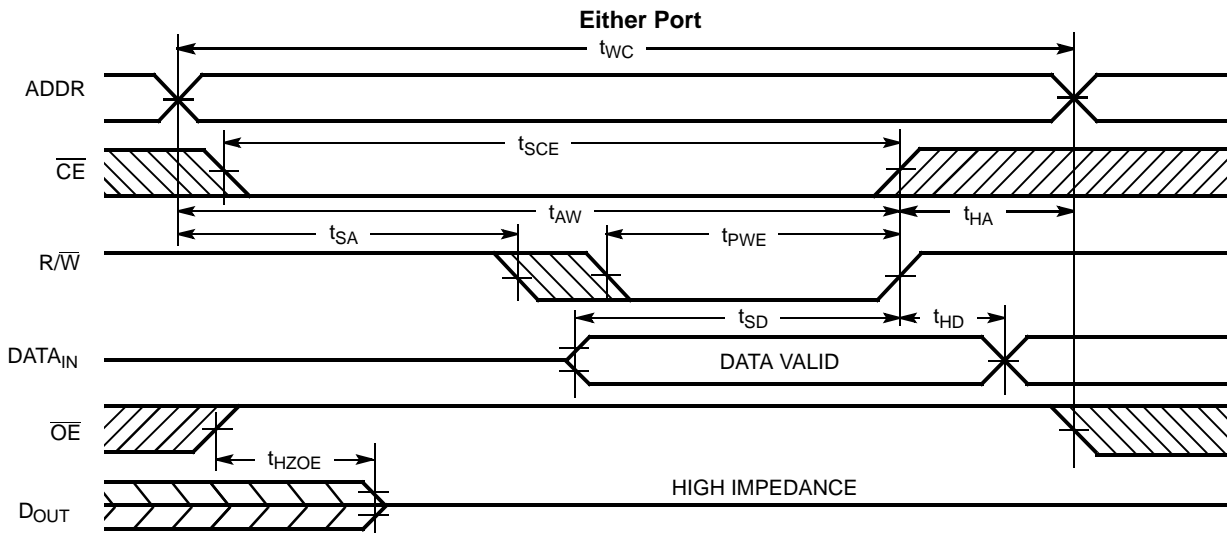


Figure 6. Write Cycle No. 1 (\overline{OE} Three-States Data I/Os – Either Port) [31, 32]



Notes

- 28. R/ \overline{W} is HIGH for read cycle.
- 29. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
- 30. Address valid prior to or coincident with CE transition LOW.
- 31. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and R/ \overline{W} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.
- 32. If \overline{OE} is LOW during a R/ \overline{W} controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZOE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD} .

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 (R/W Three-States Data I/Os – Either Port) [33, 34]

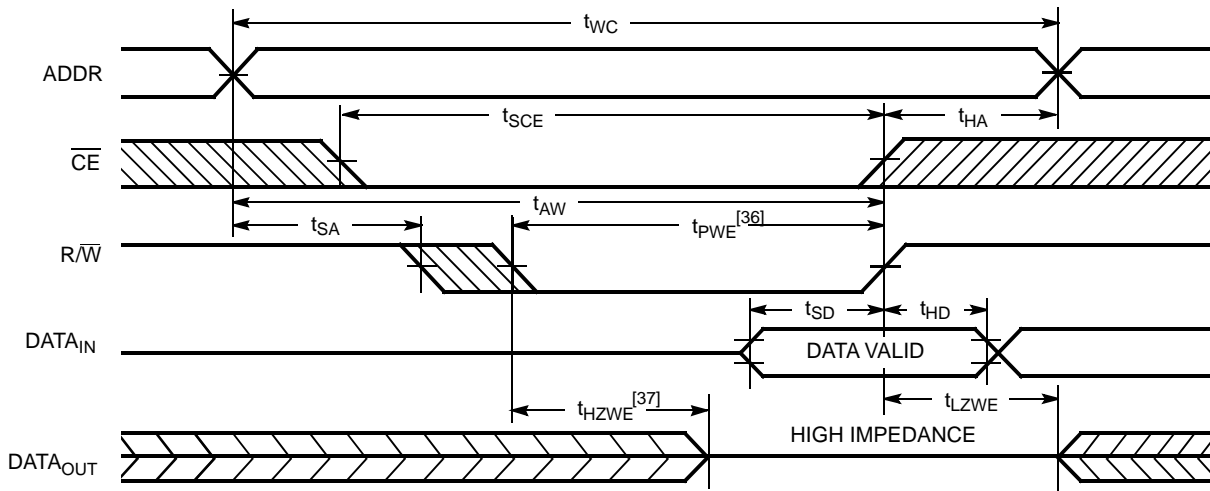
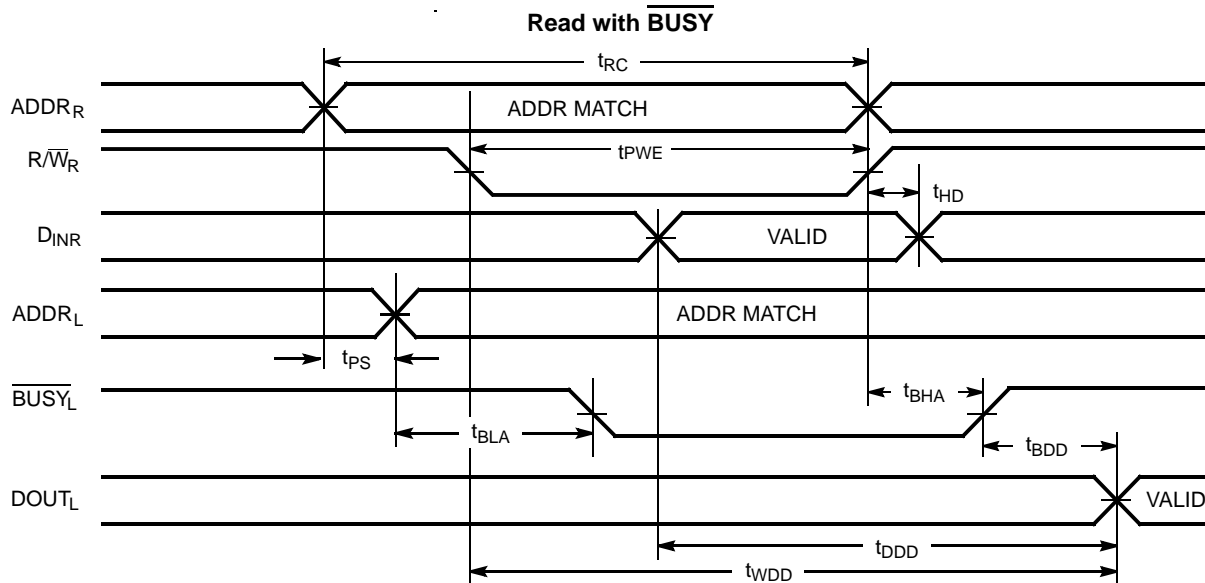


Figure 8. Read Cycle No. 3 [35]



Notes

- 33. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.
- 34. If the \overline{CE} LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high impedance state.
- 35. $CEL = CER = LOW$.
- 36. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If OE is HIGH during a R/Wn controlled write cycle, this requirements does not apply and the write pulse can be as short as the specified t_{PWE}.
- 37. Transition is measured ± 500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.

Switching Waveforms (continued)

Figure 9. Busy Timing Diagram No. 1 (\overline{CE} Arbitration)^[38]

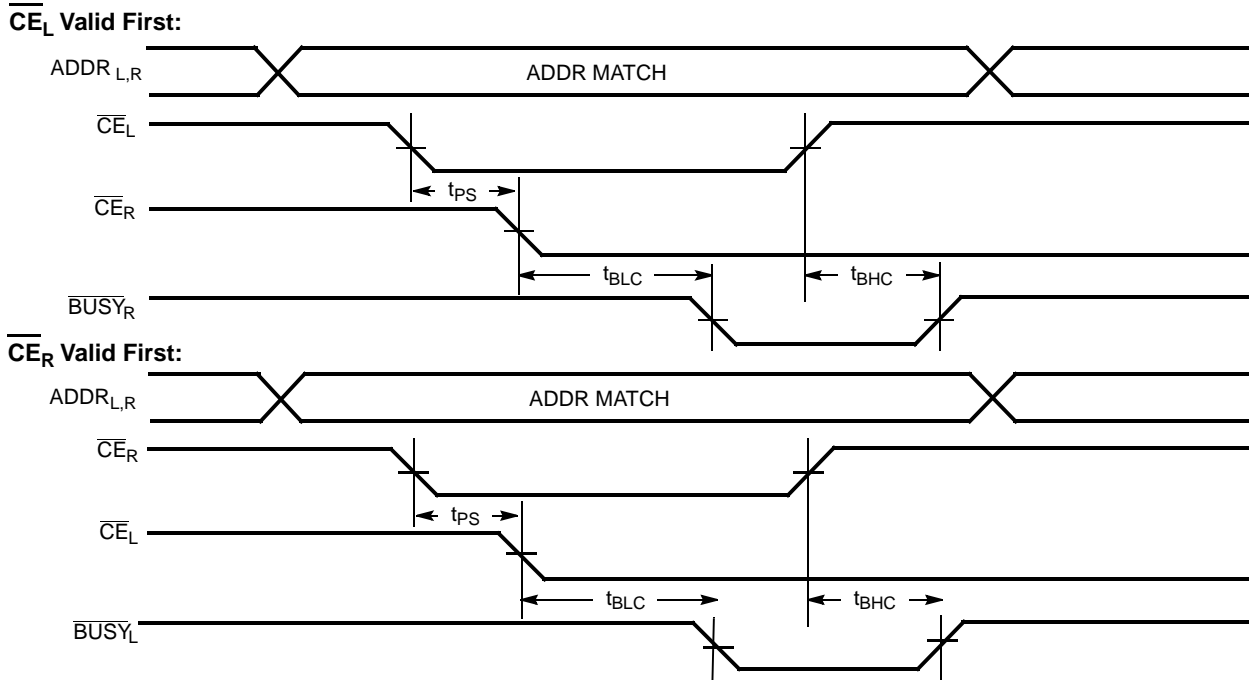
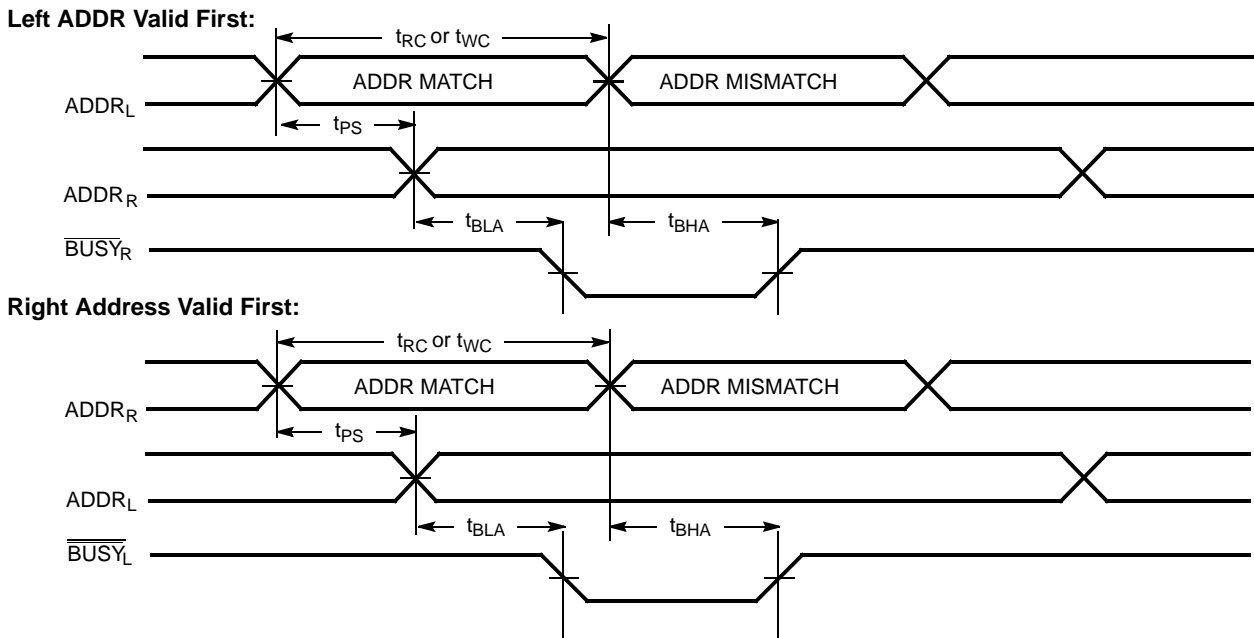


Figure 10. Busy Timing Diagram No. 2 (ADDR Arbitration)^[38]

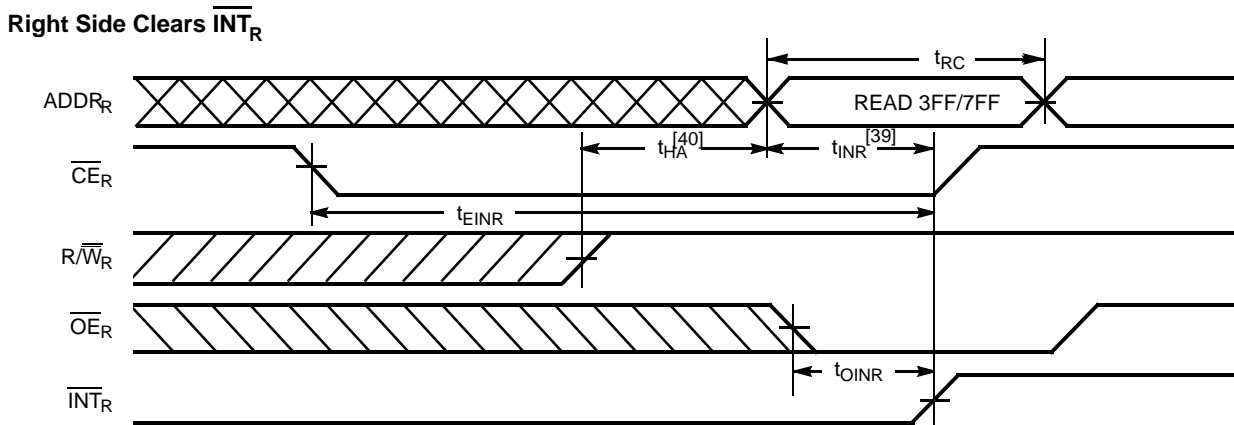
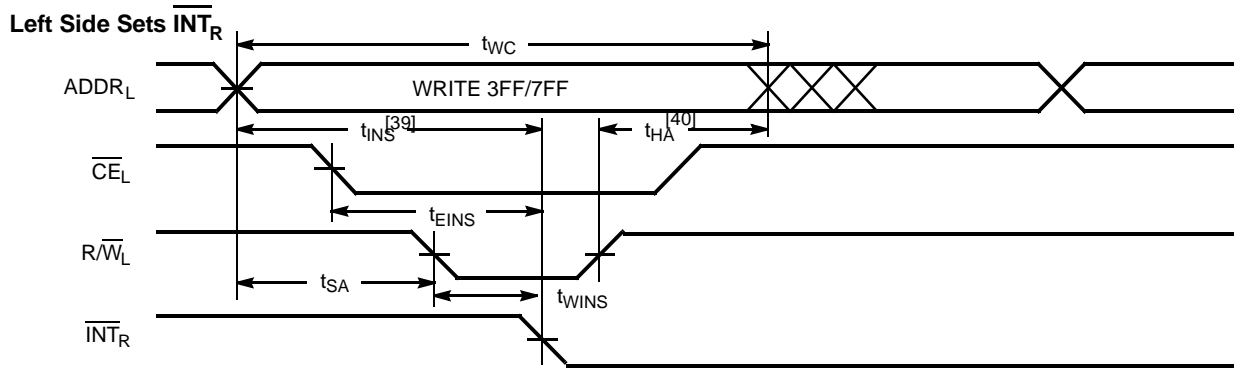


Note

38. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side \overline{BUSY} will be asserted.

Switching Waveforms (continued)

Figure 11. Interrupt Timing Diagrams

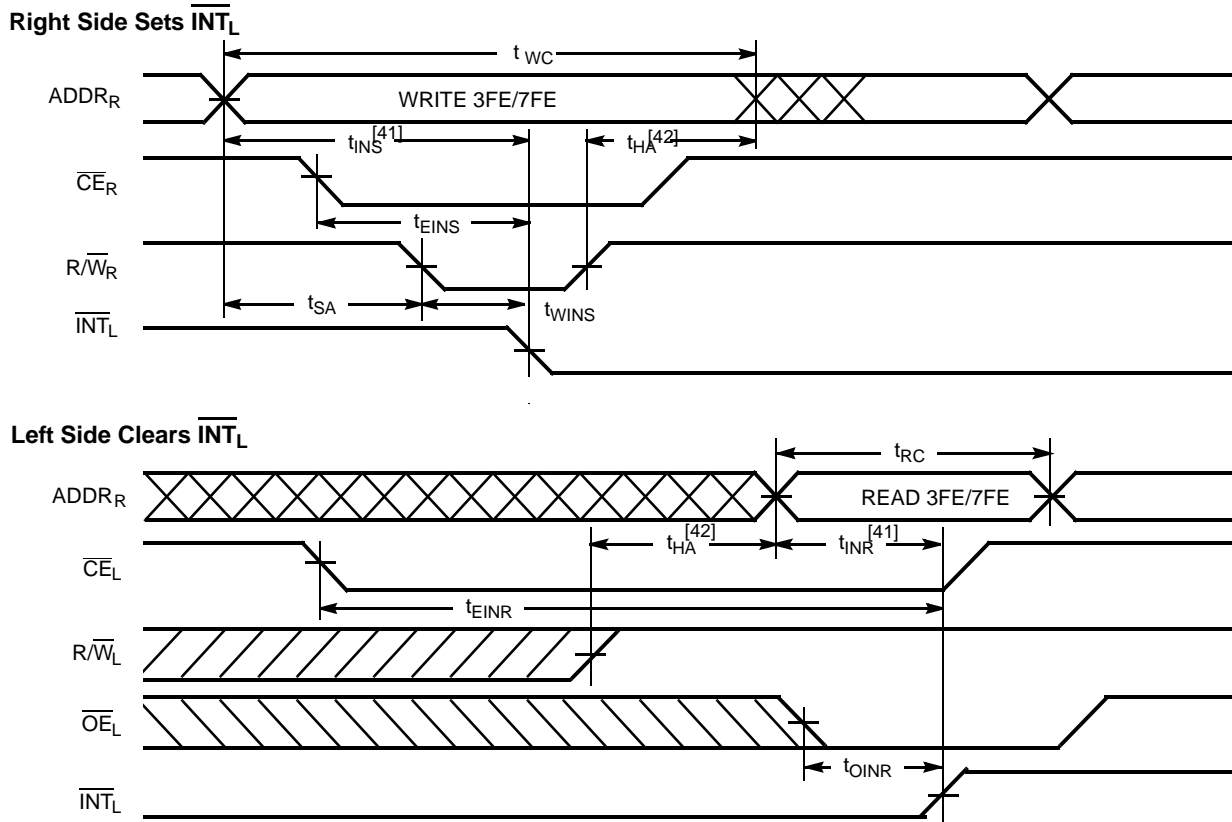


Notes

- 39. Parameter t_{INS} or t_{INR} depends on which enable pin ($\overline{\text{CE}}_L$ or $\overline{\text{R}}/\overline{\text{W}}_L$) is asserted last.
- 40. Parameter t_{HA} depends on which enable pin ($\overline{\text{CE}}_L$ or $\overline{\text{R}}/\overline{\text{W}}_L$) is deasserted first.

Switching Waveforms (continued)

Figure 12. Interrupt Timing Diagrams



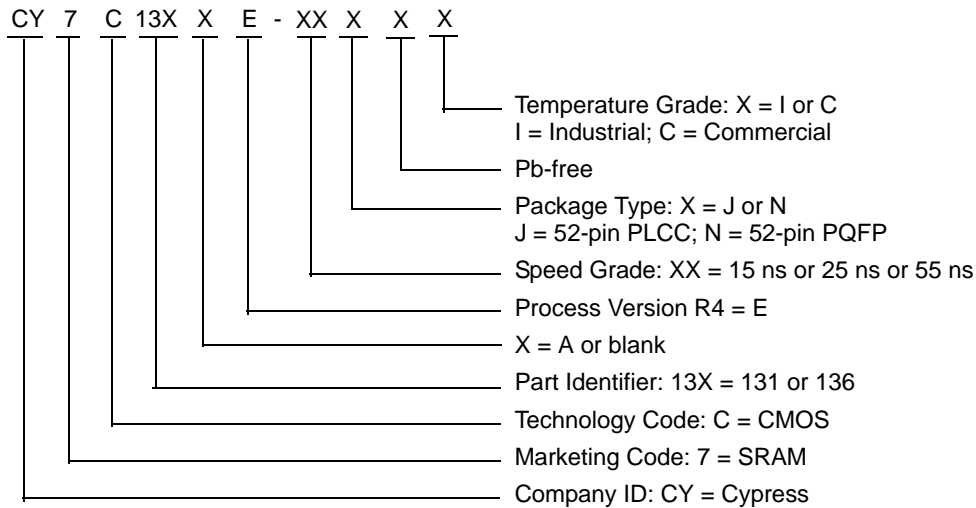
Notes

- 41. Parameter t_{INS} or t_{INR} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is asserted last.
- 42. Parameter t_{HA} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is deasserted first.

Ordering Information

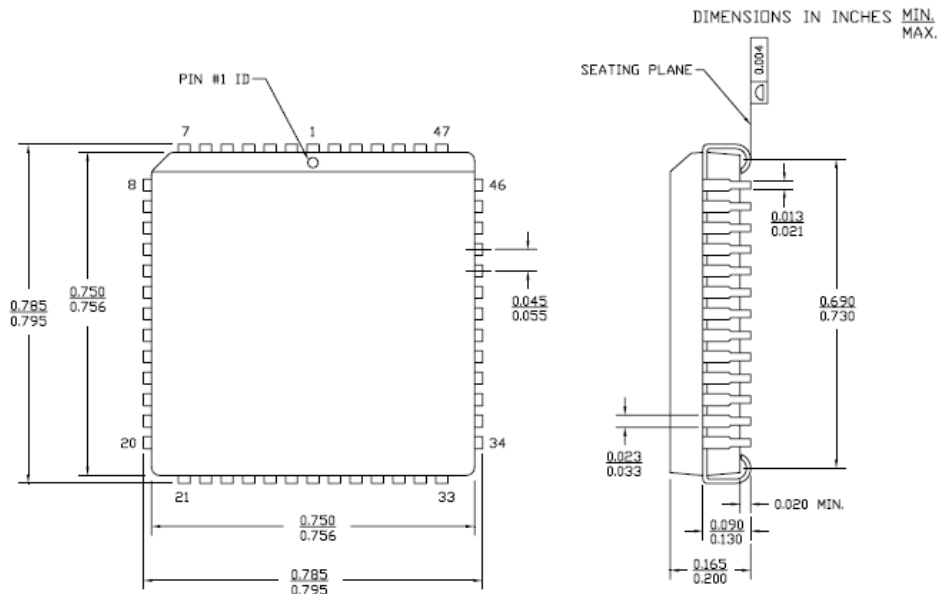
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
1 K x 8 Dual-port SRAM				
15	CY7C131AE-15JXI	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
	CY7C131E-15NXI	51-85042	52-pin Pb-free Plastic Quad Flatpack	
25	CY7C131E-25JXC	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C131E-25NXC	51-85042	52-pin Pb-free Plastic Quad Flatpack	
55	CY7C131E-55JXC	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C131E-55NXC	51-85042	52-pin Pb-free Plastic Quad Flatpack	
	CY7C131E-55JXI	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
	CY7C131E-55NXI	51-85042	52-pin Pb-free Plastic Quad Flatpack	
2 K x 8 Dual-port SRAM				
25	CY7C136E-25JXC	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C136E-25NXC	51-85042	52-pin Pb-free Plastic Quad Flatpack	
	CY7C136E-25JXI	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
55	CY7C136E-55JXC	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C136E-55NXC	51-85042	52-pin Pb-free Plastic Quad Flatpack	
	CY7C136AE-55JXI	51-85004	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
	CY7C136AE-55NXI	51-85042	52-pin Pb-free Plastic Quad Flatpack	

Ordering Code Definitions



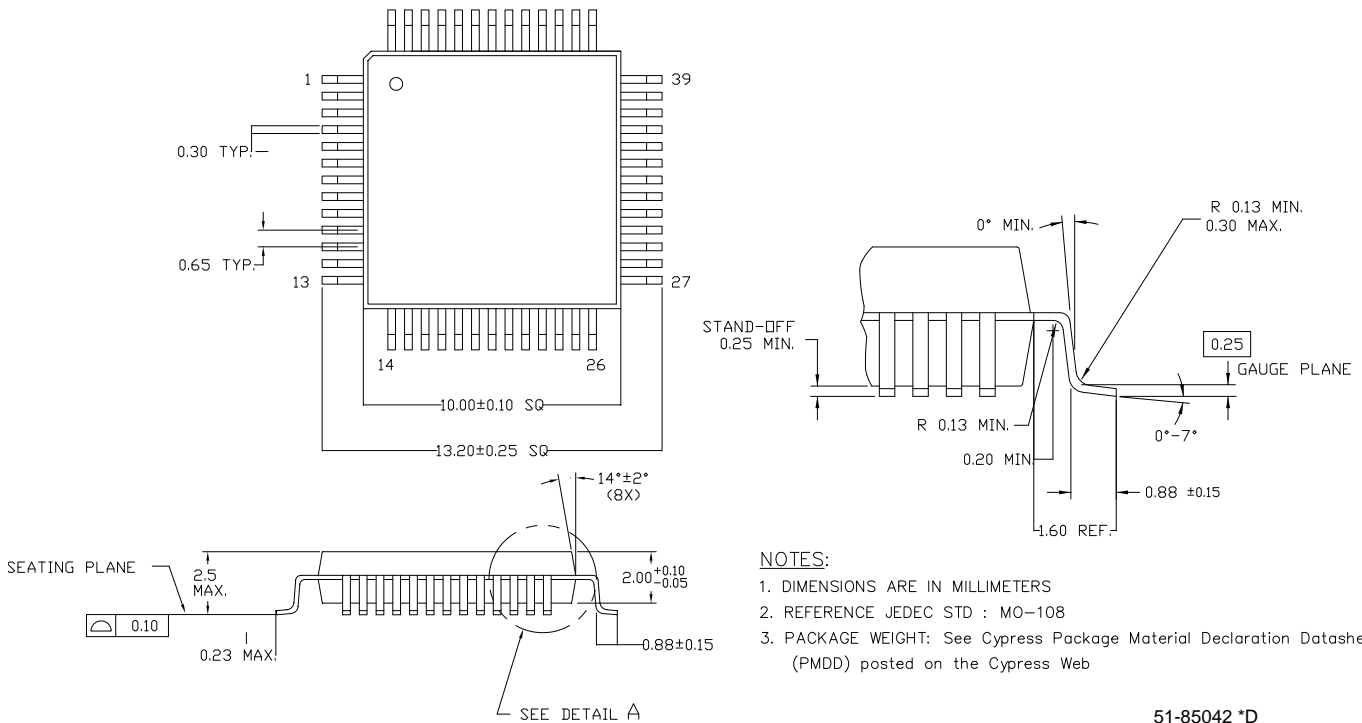
Package Diagrams

Figure 13. 52-pin PLCC (0.756 x 0.756 Inches) J52 Package Outline, 51-85004



51-85004 *C

Figure 14. 52-pin PQFP (10 x 10 x 2.0 mm) N5210 Package Outline, 51-85042



51-85042 *D

Acronyms

Acronym	Description
\overline{CE}	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
\overline{OE}	output enable
PLCC	plastic leaded chip carrier
PQFP	plastic quad flat package
SRAM	static random access memory
TTL	transistor-transistor logic
\overline{WE}	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
mA	milliampere
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C131E/CY7C131AE/CY7C136E/CY7C136AE, 1 K / 2 K × 8 Dual-port Static RAM				
Document Number: 001-64231				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3038037	ADMU	09/24/2010	New data sheet
*A	3394800	ADMU	10/04/2011	<p>Changed status from Preliminary to Final.</p> <p>Updated Maximum Ratings (Removed (Pin 48 to Pin 24)).</p> <p>Updated Electrical Characteristics (changed minimum value of I_{OZ} parameter from -10 μA to -20 μA, changed maximum value of I_{OZ} parameter from +10 μA to +20 μA and changed maximum value of I_{SB3} from 0.5 mA to 15 mA for both Commercial and Industrial temperature ranges).</p> <p>Updated Package Diagrams (Updated revision of 51-85004 from *B to *C and revision of 51-85042 from *A to *C).</p> <p>Updated in new template.</p>
*B	3403147	ADMU	10/12/2011	No technical updates.
*C	3435230	ADMU	11/17/2011	<p>Updated Features (Removed a feature “Expandable data bus width to 16 bits or more using Master/Slave chip select when using more than one device.” and updated another feature to read as “BUSY output flag to indicate access to the same location by both ports.”).</p> <p>Updated Functional Description (Updated the sentence in the first paragraph to read as “The CY7C131E / CY7C131AE / CY7C136E / CY7C136AE can be used as a standalone dual-port static RAM.”).</p> <p>Updated Note 2 to read as “BUSY is a push-pull output. No pull-up resistor required.”.</p> <p>Updated Note 3 to read as “Interrupt: push-pull output. No pull-up resistor required.”.</p> <p>Updated Maximum Ratings (Removed “(per MIL-STD-883, Method 3015)”).</p> <p>Updated Electrical Characteristics (Removed the Note “See the last page of this specification for Group A subgroup testing information.” and its reference in Parameter column.).</p> <p>Updated Capacitance[10] (Changed maximum value of C_{IN} parameter from 10 pF to 15 pF).</p> <p>Updated AC Test Loads and Waveforms.</p> <p>Updated Switching Characteristics (Removed the Note “See the last page of this specification for Group A subgroup testing information.” and its reference in Parameter column.).</p> <p>Updated Switching Characteristics (Changed the minimum value of t_{OHA} from 0 ns to 3 ns).</p> <p>Removed the section “Typical DC and AC Characteristics”.</p> <p>Removed the section “Reference Documents”.</p>
*D	3620277	ADMU	06/15/2012	<p>Added footnotes 9, 13, 17, 20, 36, 37, 39, 40, 41, and 42.</p> <p>Missing overbars updated.</p> <p>Removed “Slave Diagrams”.</p> <p>Updated Figure 3 with value 5 ns.</p> <p>Updated Maximum Ratings (updated Static discharge voltage from 2001 V to 1100 V).</p> <p>Corrected the typo in Electrical Characteristics.</p> <p>Updated Package Diagrams (51-85042 from Rev *C to *D).</p> <p>Updated I_{CC} parameters in Electrical Characteristics table.</p> <p>Updated Typical Operating Current parameters in Selection Guide.</p>

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