36-Mbit (2 M × 18) Flow-Through SRAM with NoBL™ Architecture

Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133-MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin-compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow through operation
- Byte Write capability
- 3.3 V/2.5 V I/O power supply
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock Enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable
- CY7C1463BV33 available in JEDEC-standard Pb-free 100-pin TQFP package
- Three chip enables for simple depth expansion
- Automatic Power down feature available using ZZ mode or CE deselect
- Burst Capability — linear or interleaved burst order
- Low standby power

Functional Description

The CY7C1463BV33 is a 3.3 V, 2 M × 18 Synchronous Flow -through Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1463BV33 is equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write-Read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by the two or four Byte Write Select ($\overline{BW_X}$) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

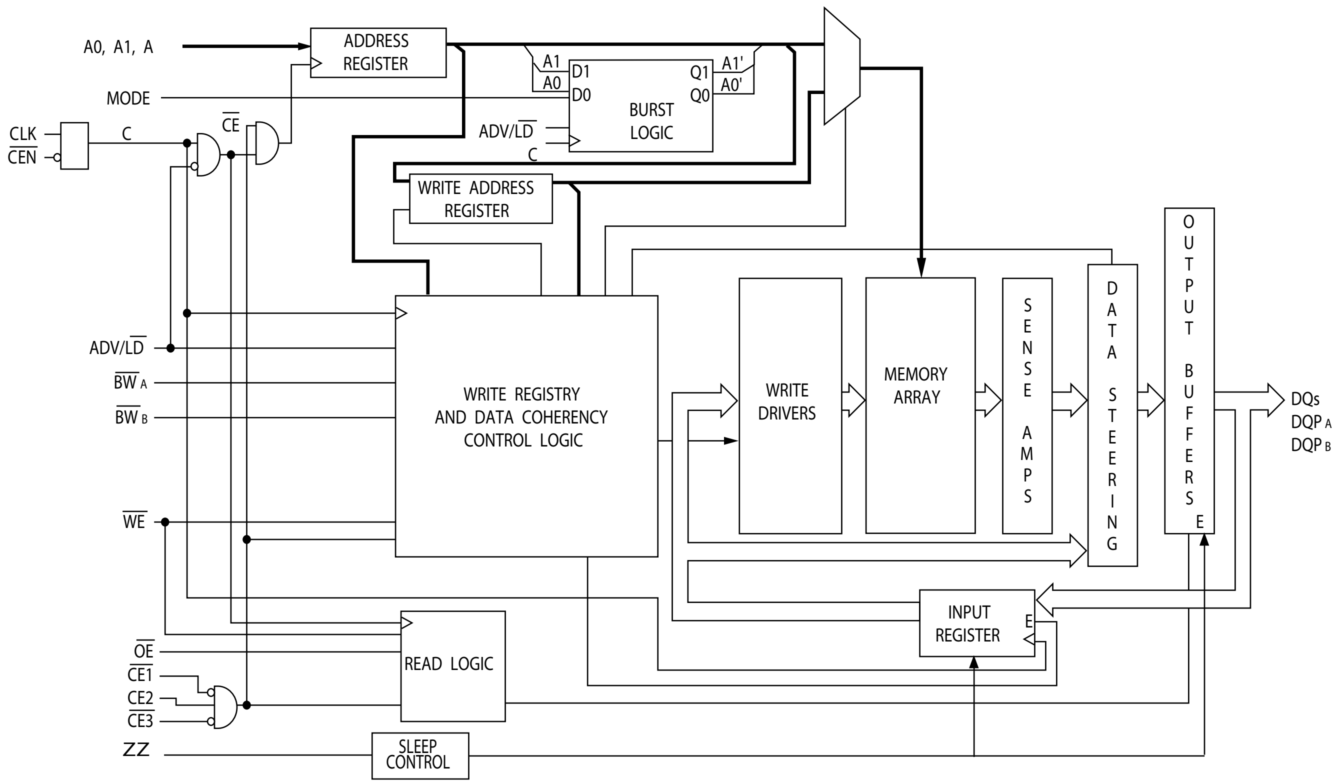
Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

For a complete list of related documentation, click here.

Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	310	mA
Maximum CMOS Standby Current	120	mA

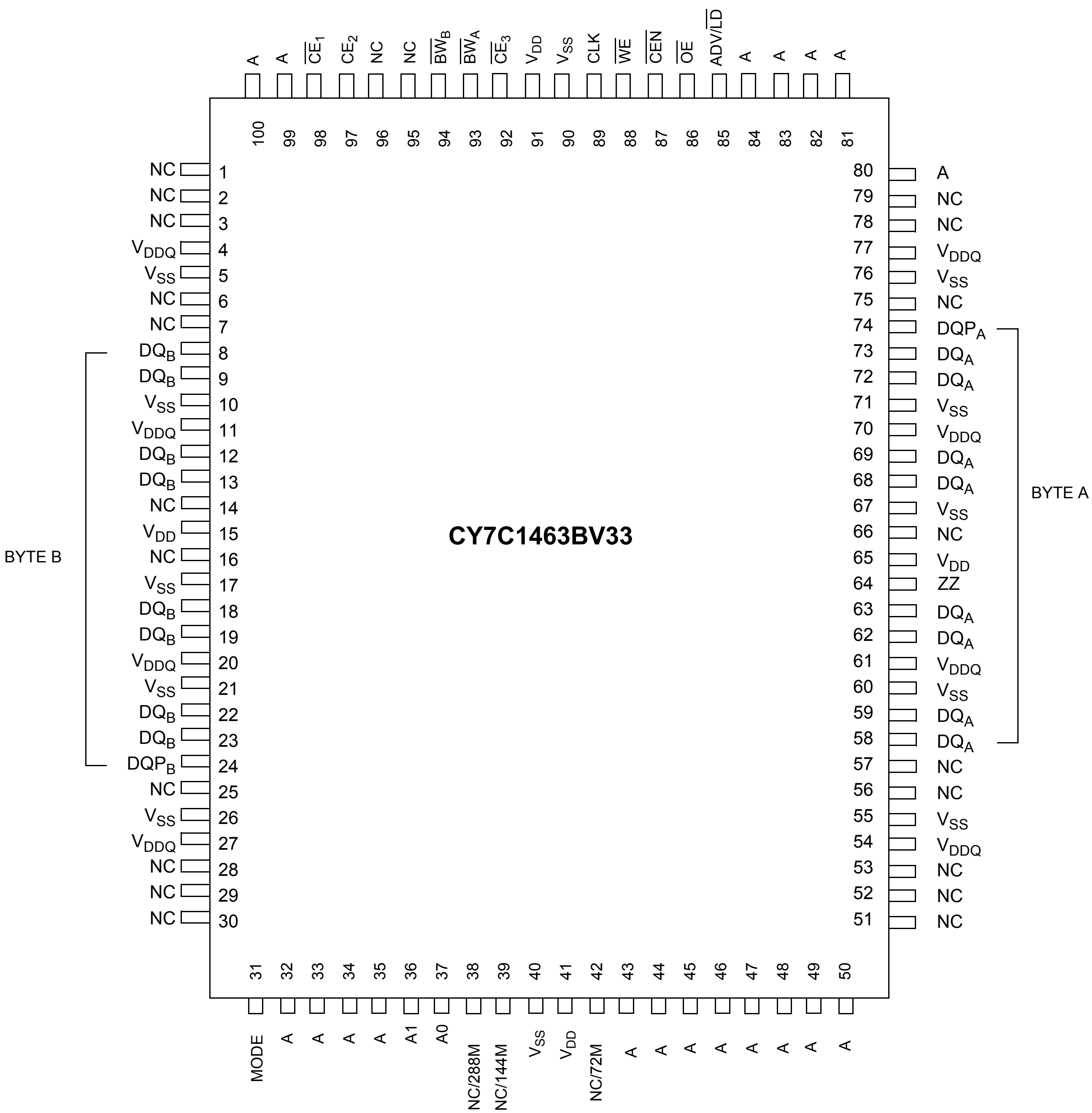
Logic Block Diagram – CY7C1463BV33



Contents

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select one of the Address Locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_A$, $\overline{BW}_B$	Input-Synchronous	**Byte Write Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ must be driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device is deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, use $\overline{CEN}$ to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and $DQP_{[A:B]}$ are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_X is controlled by $\overline{BW}_X$ correspondingly.
MODE	Input Strap Pin	**Mode Input. Selects the Burst Order of the Device**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**.
NC	N/A	**No Connects**. Not internally connected to the die.
NC/72M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.

Pin Definitions (continued)

Name	I/O	Description
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/576M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/1G	N/A	**Not Connected to the Die**. Can be tied to any voltage level.

Functional Overview

The CY7C1463BV33 is a synchronous flow through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BW}_X$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ must be driven LOW after the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active
- The Write Enable input signal $\overline{WE}$ is deasserted HIGH
- ADV/$\overline{LD}$ is asserted LOW.

The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

Burst Read Accesses

The CY7C1463BV33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in Single Read Accesses. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enable inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to the address bus is loaded into the Address Register. The write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and DQP_X.

On the next clock rise the data presented to DQs and DQP_X (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (Read/Write/Deselect) can be initiated on this cycle.

The data written during the Write operation is controlled by $\overline{BW}_X$ signals. The CY7C1463BV33 provides byte write capability that is described in the truth table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte write capability has been included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1463BV33 is a common I/O device, data must not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQs and DQP_X inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and DQP_X are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1463BV33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in Single Write Accesses on page 6. When ADV/LD is driven HIGH on the subsequent clock rise, the Chip Enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}_X$ inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	100	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1463BV33 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	–
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

Truth Table for Read/Write

The read/write truth table for CY7C1463BV33 follows.[1, 8]

Function (CY7C1463BV33)	$\overline{WE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	L
Write Byte b – (DQ_b and DQP_b)	L	L	H
Write Both Bytes	L	L	L

Notes
1. X = "Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{BWx}$ = L signifies at least one Byte Write Select is active, $\overline{BWx}$ = Valid signifies that the desired byte write selects are asserted, see truth table for details.
2. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See truth table for Read/Write.
3. When a write cycle is detected, all I/Os are tri-stated, even during byte writes.
4. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. $\overline{CEN}$ = H, inserts wait states.
6. Device powers up deselected and the I/Os in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = Tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and DQP_X = data when OE is active.
8. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{BW_X}$ is valid Appropriate write is done based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with
Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to +V_{DD}

DC Voltage Applied to Outputs
in Tri-State ....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) .... > 2001 V

Latch-up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Industrial	–40 °C to +85 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25 °C	197	216	FIT/ Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single Event Latch-up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Electrical Characteristics

Over the Operating Range

Parameter [9, 10]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [9]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [9]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD} [11]	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	7.5 ns cycle, 133 MHz	–	310	mA

Notes
9. Overshoot: $V_{IH(AC)} < V_{DD}$ + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than $t_{CYC}/2$).
10. $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
11. The operation current is calculated with 50% read cycle and 50% write cycle.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [9, 10]	Description	Test Conditions		Min	Max	Unit
I_{SB1}	Automatic CE Power down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	180	mA
I_{SB2}	Automatic CE Power down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DD} - 0.3$ V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	120	mA
I_{SB3}	Automatic CE Power down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	180	mA
I_{SB4}	Automatic CE Power down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	135	mA

Capacitance

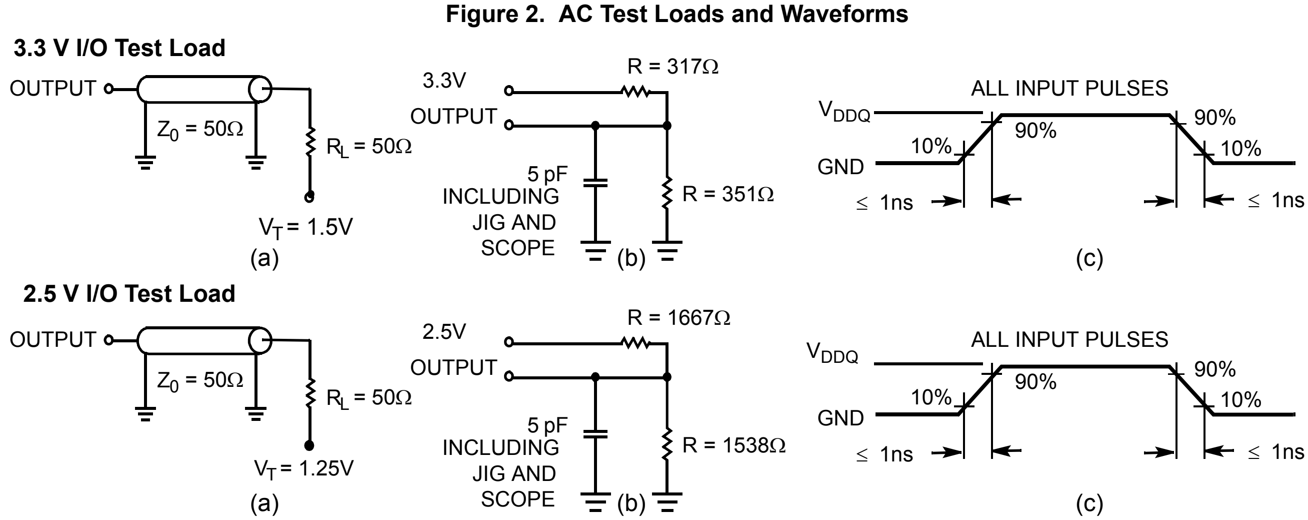
Parameter [12]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	6.5	pF
C_{CLK}	Clock Input Capacitance		3	pF
C_{IO}	Input/Output Capacitance		5.5	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	25.21	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.28	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
12. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

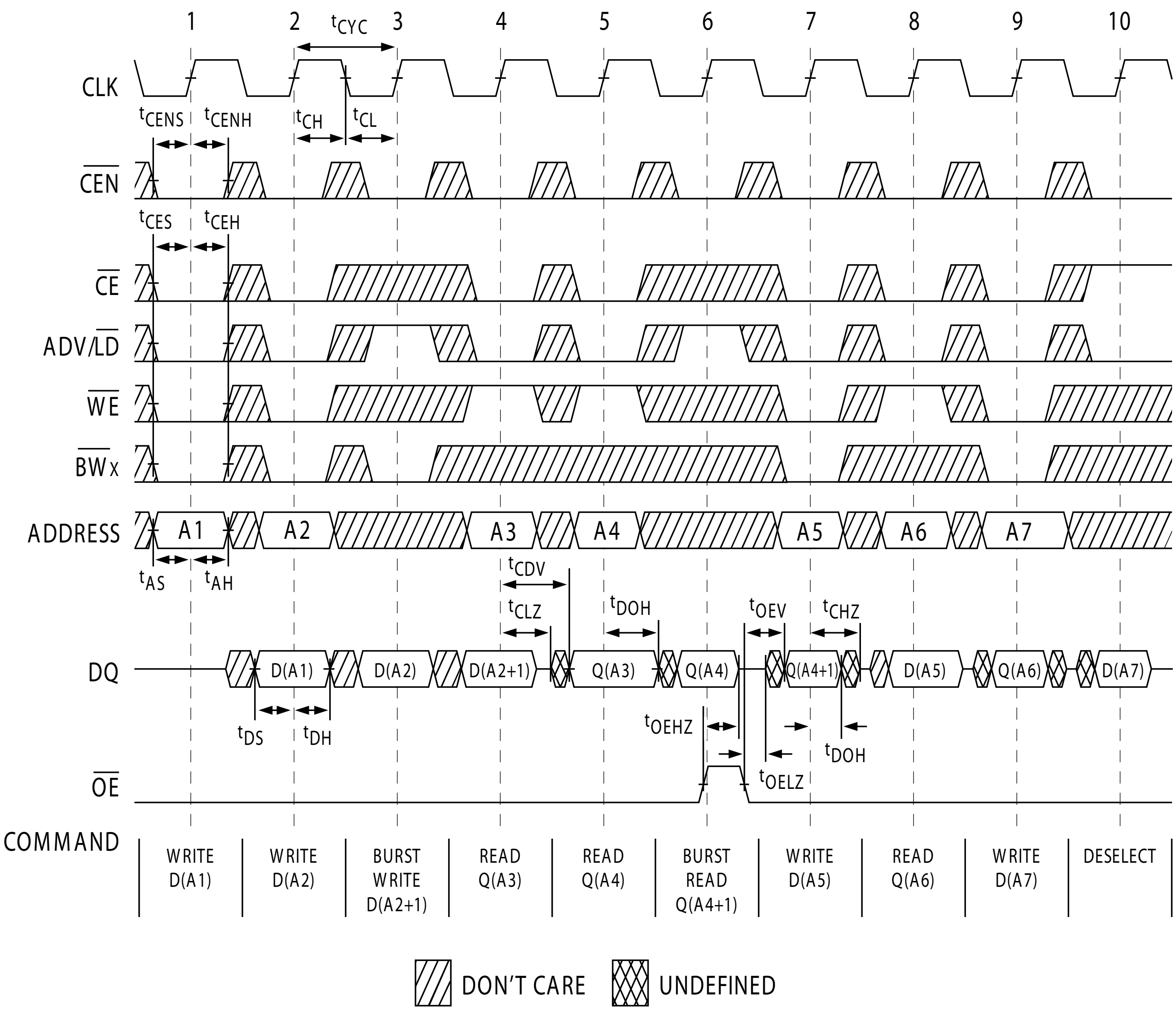
Parameter [13, 14]	Description	133 MHz		Unit
		Min	Max	
t_{POWER}[15]	V_{DD}(typical) to the First Access	1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	7.5	–	ns
t_{CH}	Clock HIGH	2.5	–	ns
t_{CL}	Clock LOW	2.5	–	ns
Output Times				
t_{CDV}	Data Output Valid After CLK Rise	–	6.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.5	–	ns
t_{CLZ}	Clock to Low Z [16, 17, 18]	2.5	–	ns
t_{CHZ}	Clock to High Z [16, 17, 18]	–	3.8	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	3.0	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z [16, 17, 18]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z [16, 17, 18]	–	3.0	ns
Setup Times				
t_{AS}	Address Setup Before CLK Rise	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ Setup Before CLK Rise	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ Setup Before CLK Rise	1.5	–	ns
t_{CENS}	$\overline{CEN}$ Setup Before CLK Rise	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.5	–	ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.5	–	ns
Hold Times				
t_{AH}	Address Hold After CLK Rise	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ Hold After CLK Rise	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ Hold After CLK Rise	0.5	–	ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5	–	ns

Notes

13. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
14. Test conditions shown in (a) of Figure 2 on page 10 unless otherwise noted.
15. This part has a voltage regulator internally; t_{POWER} is the time that the power is supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
16. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 10. Transition is measured ±200 mV from steady-state voltage.
17. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

Switching Waveforms

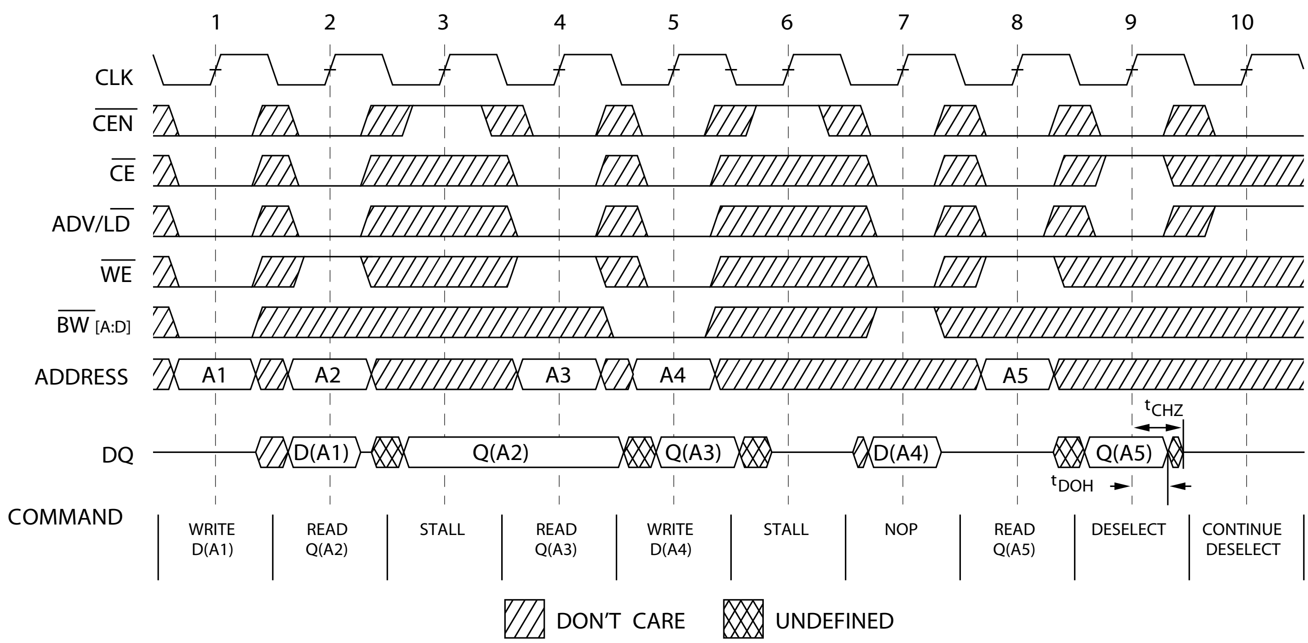
Figure 3. Read/Write Waveforms [19, 20, 21]



Notes
19. For this waveform ZZ is tied LOW.
20. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

Figure 4. NOP, STALL and DESELECT Cycles [22, 23, 24]

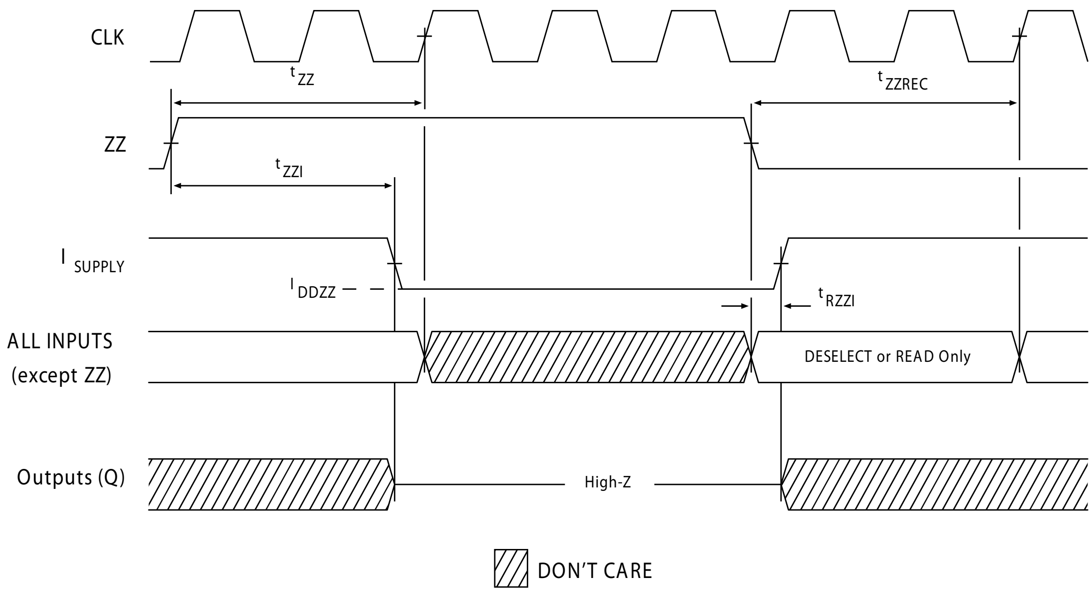


Notes

22. For this waveform ZZ is tied LOW.
23. When CE is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When CE is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
24. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates CEN being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 5. ZZ Mode Timing [25, 26]



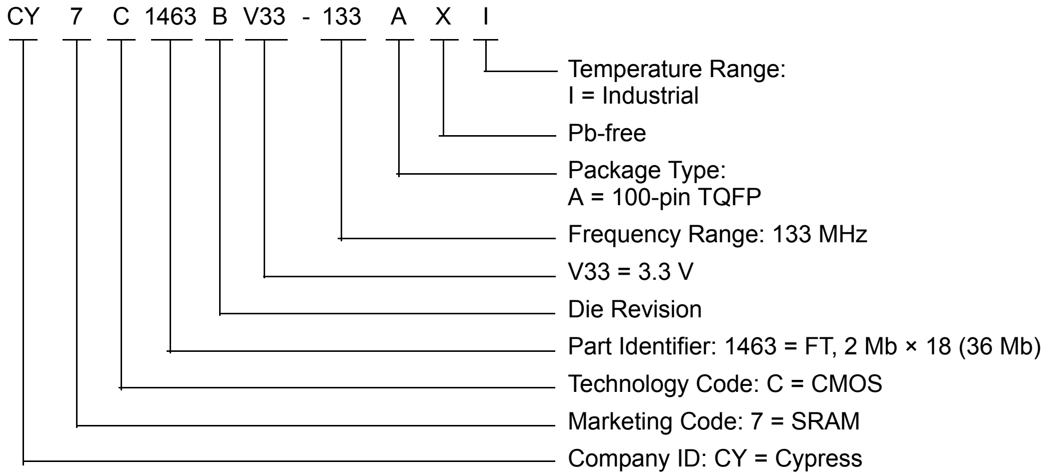
Notes
25. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
26. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.
Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

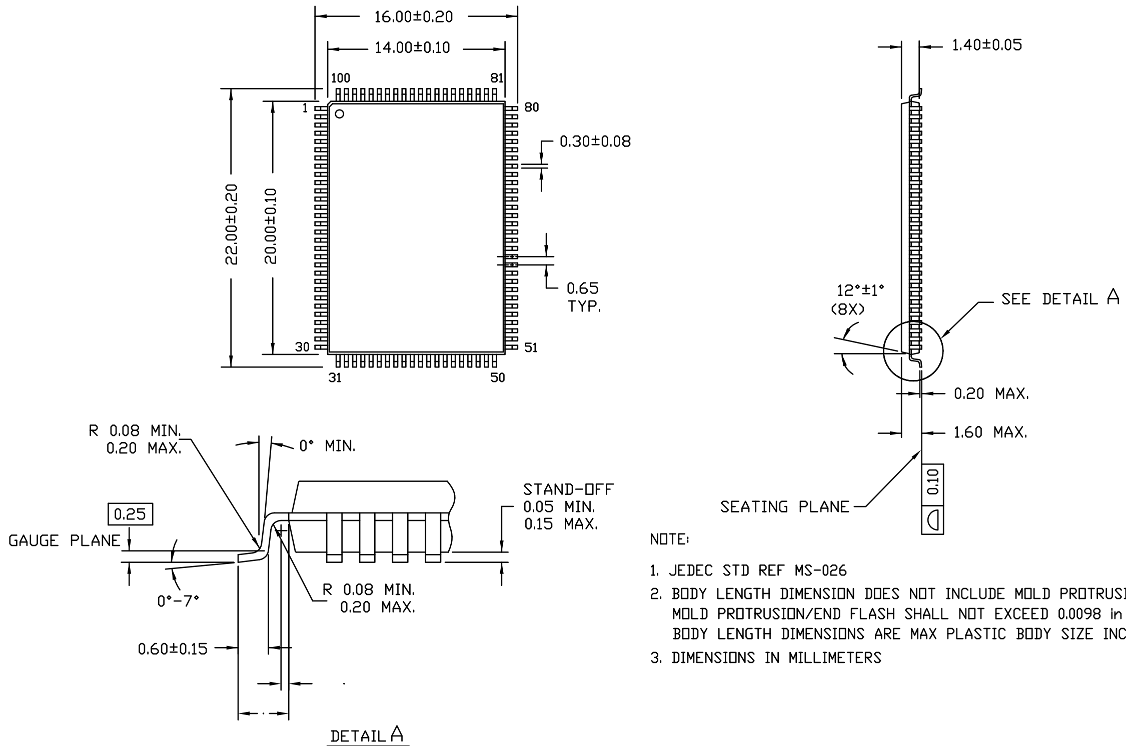
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1463BV33-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagram

Figure 6. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *E

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
$\overline{CEN}$	Clock Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LMBU	Logical Multiple Bit Upset
LSBU	Logical Single Bit Upset
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1463BV33, 36-Mbit (2 M × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 001-75212				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	3488155	01/09/2012	NJY	New data sheet.
*A	3534581	02/28/2012	NJY	Changed status from Preliminary to Final.
*B	4575228	11/20/2014	NJY	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagram: spec 51-85050 – Changed revision from *D to *E.
*C	5072986	01/05/2016	PRIT	Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support