CY7C199D

256-Kbit (32 K × 8) Static RAM

Features

- Temperature ranges
  - –40 °C to 85 °C
- Pin and function compatible with CY7C199C
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 80 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 3 mA
- 2.0 V data retention
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 28-pin 300-Mil-wide molded small outline J-lead package (SOJ) and 28-pin thin small outline package (TSOP) I packages

Functional Description

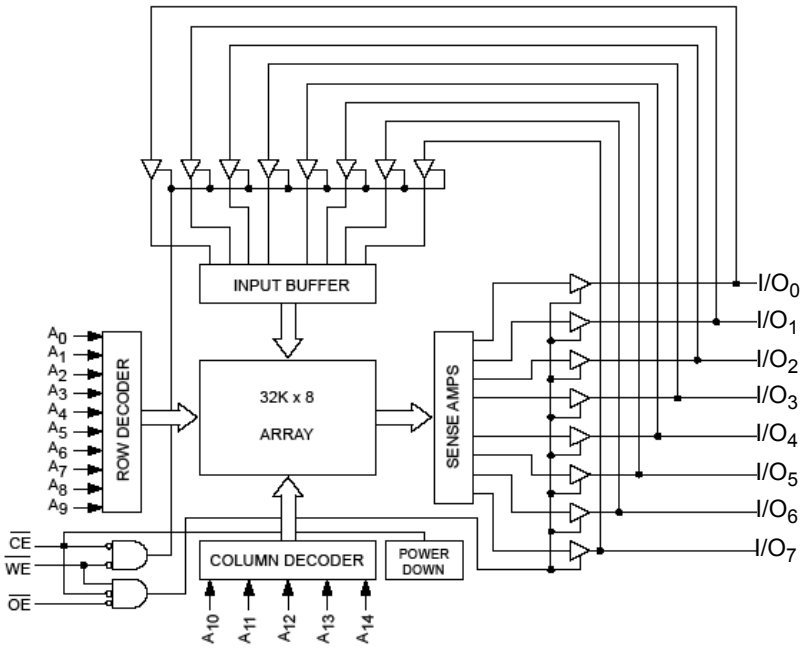
The CY7C199D is a high performance CMOS static RAM organized as 32,768 words by 8-bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$) and tri-state drivers. This device has an automatic power-down feature, reducing the power consumption when deselected. The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Write to the device by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{14}).

Read from the device by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the I/O pins.

The CY7C199D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 28-pin SOJ pinout (Top View)

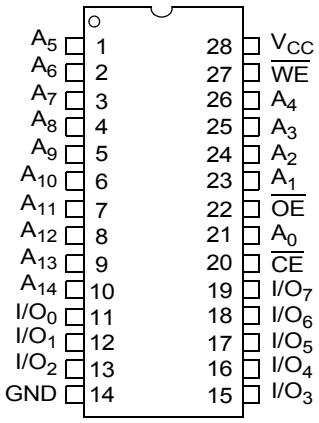
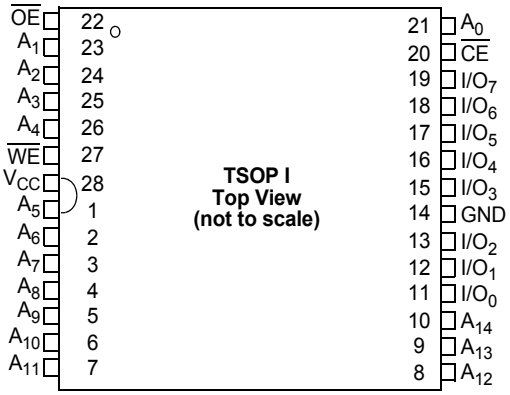


Figure 2. 28-pin TSOP I pinout (Top View)



Selection Guide

Description	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current	3	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND [1] .....–0.5 V to +6.0 V

DC voltage applied to outputs in high Z State [1] .....–0.5 V to V_{CC} + 0.5 V

DC input voltage [1] .....–0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2,001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	5 V ± 0.5 V	10 ns

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		CY7C199D-10		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –4.0 mA		2.4	–	V
		I_{OH} = –0.1mA		–	3.4 [2]	
V_{OL}	Output LOW voltage	I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage [1]			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage [1]			–0.5	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, f = f_{max} = $1/t_{RC}$	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I_{SB1}	Automatic CE power-down current — TTL Inputs	V_{CC} = $V_{CC(max)}$, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{max}		–	10	mA
I_{SB2}	Automatic CE power-down current — CMOS Inputs	V_{CC} = $V_{CC(max)}$, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0		–	3	mA

Note
1. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 1 V for pulse durations of less than 5 ns.
2. Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.

Capacitance

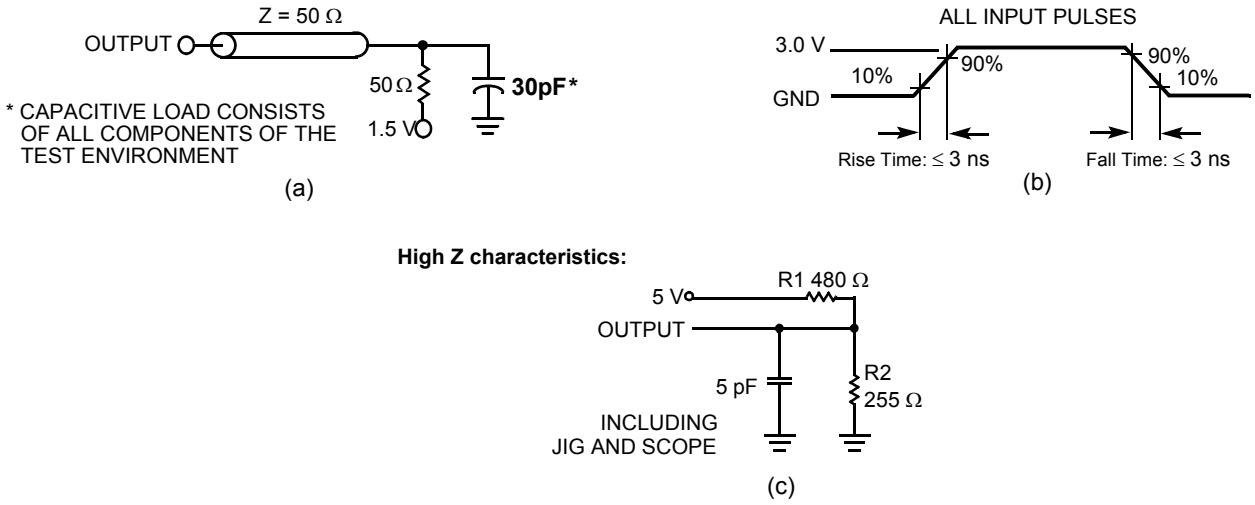
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	28-pin SOJ	28-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.16	54.65	°C/W
Θ_{JC}	Thermal resistance (junction to case)		40.84	21.49	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [4]



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except high Z) are tested using the load conditions shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

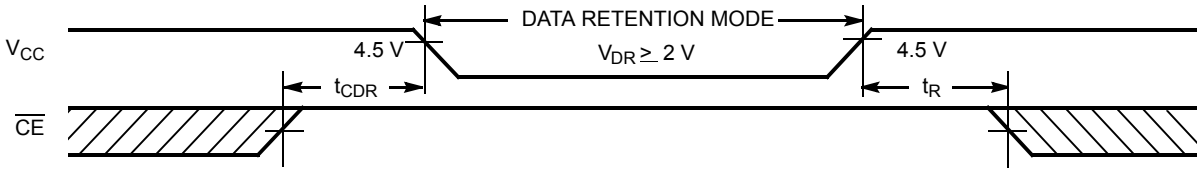
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	3	mA
t_{CDR} [5]	Chip deselect to data retention time		0	–	ns
t_R [6]	Operation recovery time		15	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes
5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

Switching Characteristics

Over the operating range

Parameter [7]	Description	CY7C199D-10		Unit
		Min	Max	
Read Cycle				
t_{power} [8]	$V_{CC(typical)}$ to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE} [9]	$\overline{OE}$ LOW to low Z	0	–	ns
t_{HZOE} [9, 10]	$\overline{OE}$ HIGH to high Z	–	5	ns
t_{LZCE} [9]	$\overline{CE}$ LOW to low Z	3	–	ns
t_{HZCE} [9, 10]	$\overline{CE}$ HIGH to high Z	–	5	ns
t_{PU} [11]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD} [11]	$\overline{CE}$ HIGH to power-down	–	10	ns
Write Cycle [12, 13]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data setup to write end	6	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE} [9]	$\overline{WE}$ LOW to high Z	–	5	ns
t_{LZWE} [9, 10]	$\overline{WE}$ HIGH to low Z	3	–	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less for all speeds, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of Figure 3 on page 5. Transition is measured ±200 mV from steady-state voltage.
11. This parameter is guaranteed by design and is not tested.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1: Address Transition Controlled [14, 15]

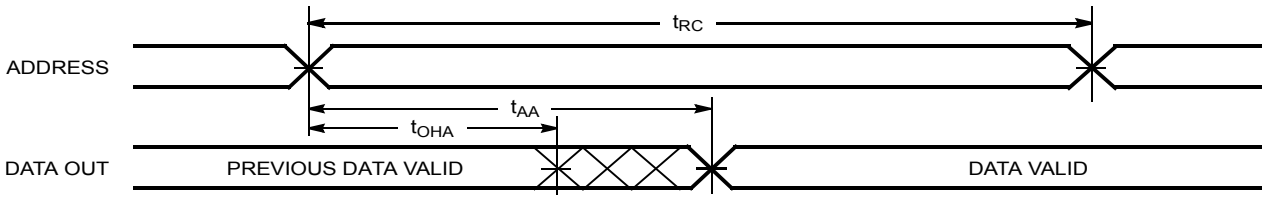
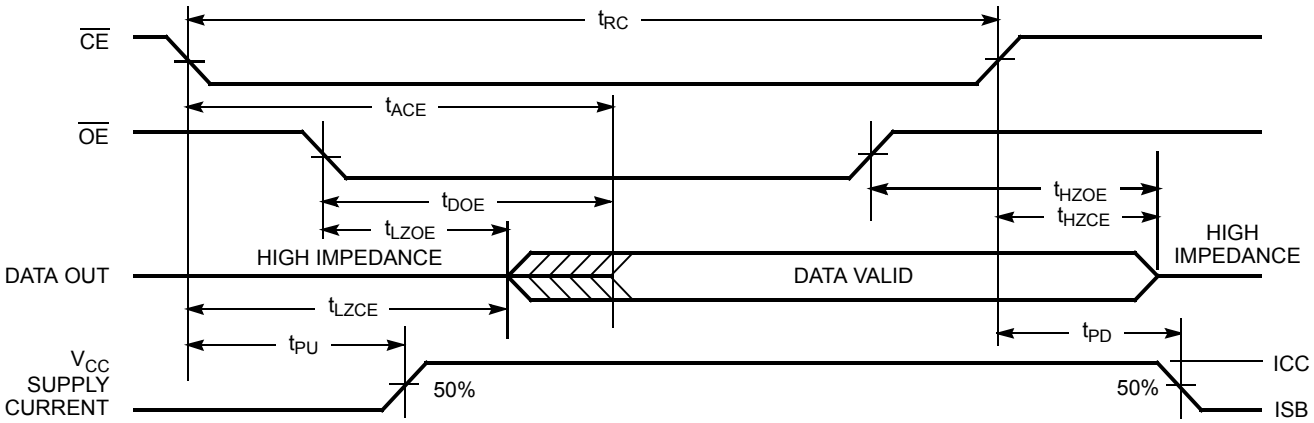


Figure 6. Read Cycle No. 2 $\overline{OE}$ Controlled [15, 16]



Notes
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 7. Write Cycle No. 1: $\overline{CE}$ Controlled [17, 18, 19]

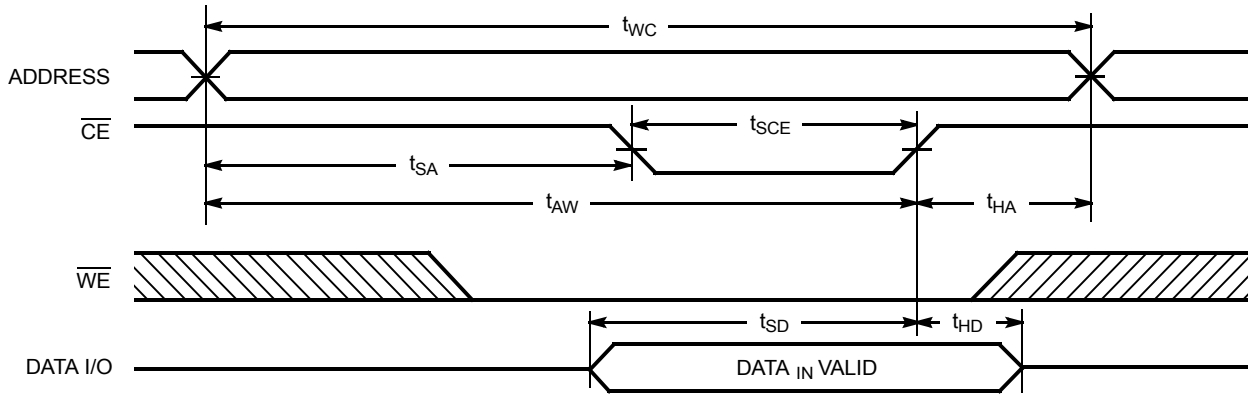
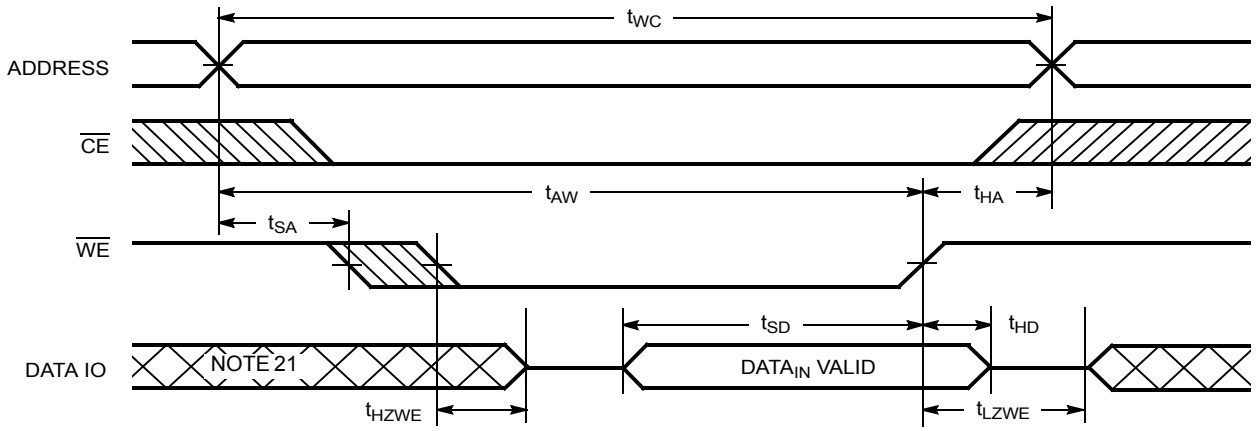


Figure 8. Write Cycle No. 3 $\overline{WE}$ Controlled, $\overline{OE}$ LOW [19, 20]



Notes

17. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
20. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
21. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Deselect, output disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at http://www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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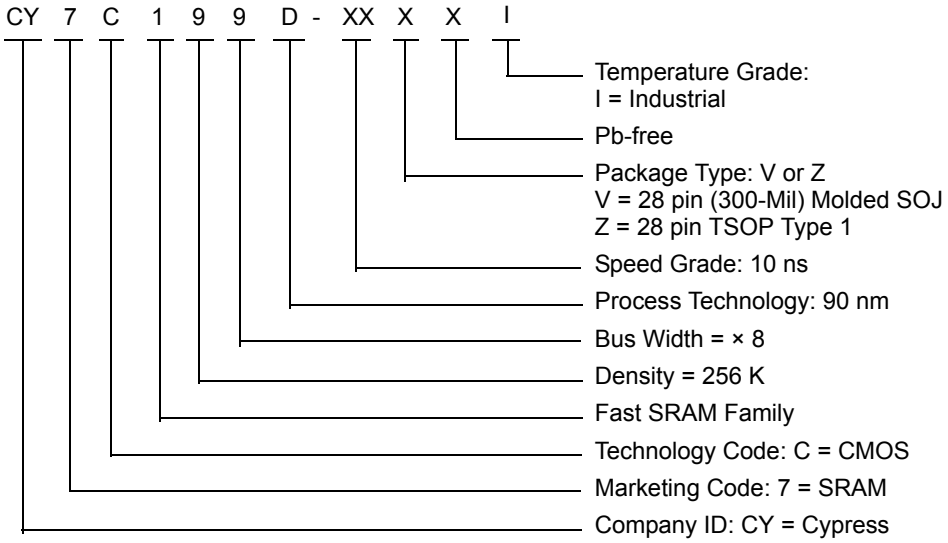
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C199D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C199D-10ZXI	51-85071	28-pin TSOP Type I (Pb-free)	

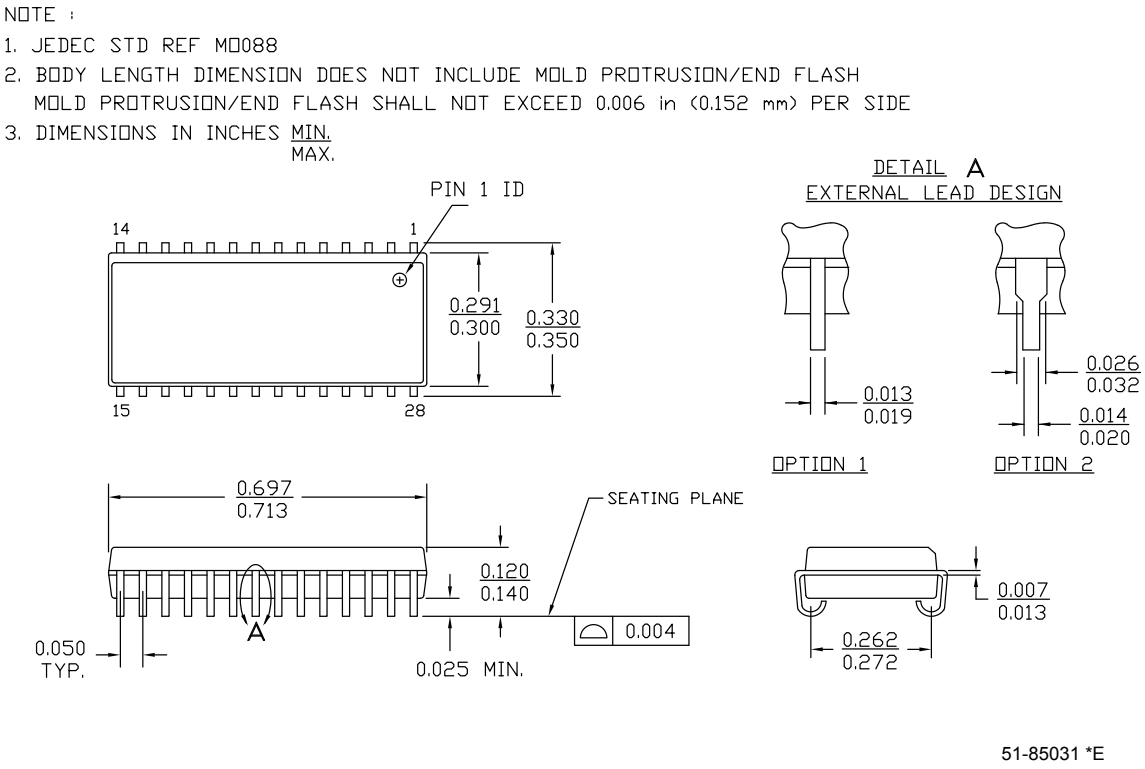
Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



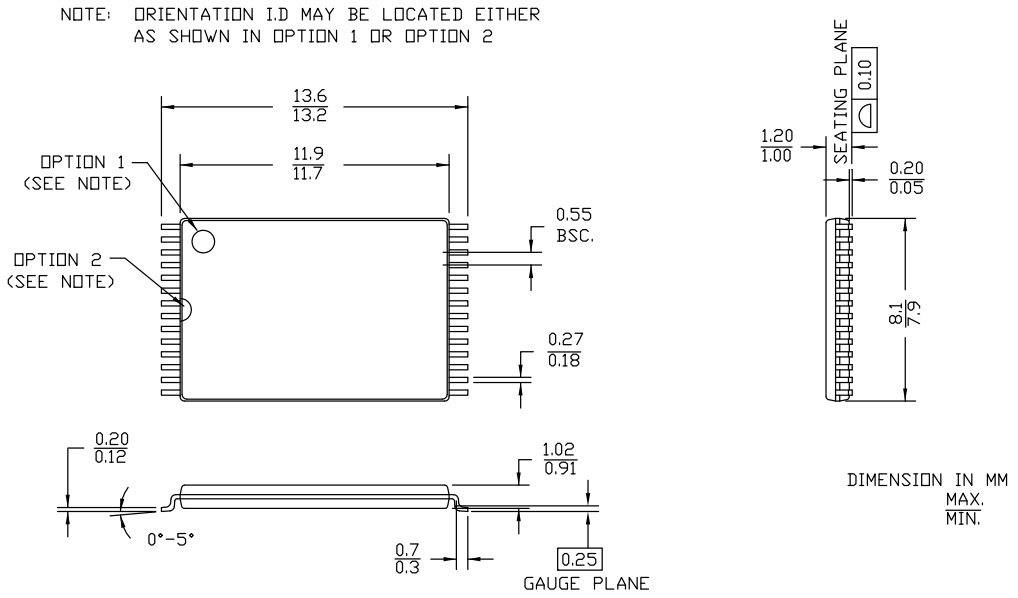
Package Diagrams

Figure 9. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031



Package Diagrams *(continued)*

Figure 10. 28-pin TSOP Type 1 (8 × 13.4 × 1.2 mm) Z28 (Standard) Package Outline, 51-85071



51-85071 *I

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C199D, 256-Kbit (32 K × 8) Static RAM Document Number: 38-05471				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	201560	SWI	See ECN	Advance Information datasheet for C9 IPP
*A	233728	RKF	See ECN	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information
*B	262950	RKF	See ECN	Removed 28-LCC Pinout and Package Diagrams Added Data Retention Characteristics table Added T_{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307594	RKF	See ECN	Reduced Speed bins to -10, -12 and -15 ns
*D	820660	VKN	See ECN	Converted from Preliminary to Final Removed 12 ns and 15 ns speed bin Removed Commercial Operating range Removed “L” part Removed 28-pin PDIP and 28-pin SOIC package Changed Overshoot spec from V_{CC}+2V to V_{CC}+1V in footnote #2 Changed I_{CC} spec from 60 mA to 80 mA for 100 MHz speed bin Added I_{CC} specs for 83 MHz, 66 MHz and 40 MHz speed bins Updated Thermal Resistance table Updated Ordering Information Table
*E	2745093	VKN	See ECN	Included 28-Pin SOIC package Changed V_{IH} level from 2.0V to 2.2V For Industrial grade, changed t_{SD} from 5 ns to 6 ns, and t_{HZWE} from 6 ns to 5 ns Included Automotive-E information
*F	2897087	AJU	03/22/10	Removed obsolete parts from ordering information table Updated package diagrams
*G	3023234	RAME	09/06/2010	Added Auto-E SOIC package related info Changed TDOE spec from 10 ns to 11 ns in CY7C199D-25. Added Ordering Code Definitions. Added Acronyms and Units of Measure.
*H	3130763	PRAS	01/07/11	Dislodged Automotive information to a new datasheet (001-65530)
*I	3271782	PRAS	06/02/2011	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Package Diagrams. Updated in new template.
*J	4033580	MEMJ	06/19/2013	Updated Functional Description. Updated Electrical Characteristics. Added one more Test Condition “I_{OH} = –0.1 mA” for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 2 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition “I_{OH} = –0.1 mA”. Updated Package Diagrams: spec 51-85031 – Changed revision from *D to *E.

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