CY7C4201V/4211V

Low Voltage 256/512 × 9 Synchronous FIFOs

Features

- High-speed, low-power, first-in, first-out (FIFO) memories
  - 256 × 9 (CY7C4201V)
  - 512 × 9 (CY7C4211V)
- High-speed 66-MHz operation (15-ns read/write cycle time)
- Low power (I_{CC} = 20 mA)
- 3.3 V operation for low power consumption and easy integration into low-voltage systems
- 5V-tolerant inputs $V_{IH(max)}$ = 5 V
- Fully asynchronous and simultaneous read and write operation
- Empty, full, and programmable almost empty and almost full status flags
- TTL compatible
- Output Enable ($\overline{OE}$) pin
- Independent read and write enable pins
- Center power and ground pins for reduced noise
- Width expansion capability
- Space saving 32-pin 7 mm × 7 mm TQFP
- 32-pin PLCC available in Pb-free Packages

Functional Description

The CY7C42X1V are high-speed, low-power, FIFO memories with clocked read and write interfaces. All are nine bits wide. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

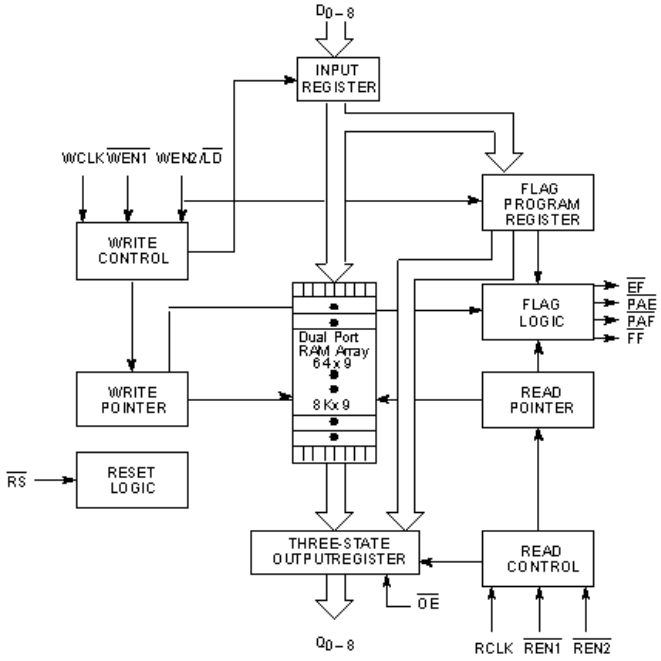
These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a Free-Running Clock (WCLK) and two Write Enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a Free-Running Read Clock (RCLK) and two Read Enable Pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C42X1V has an Output Enable Pin ($\overline{OE}$). The Read (RCLK) and Write (WCLK) clocks may be tied together for single clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 66 MHz are achievable.

Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

For a complete list of related documentation, click here.

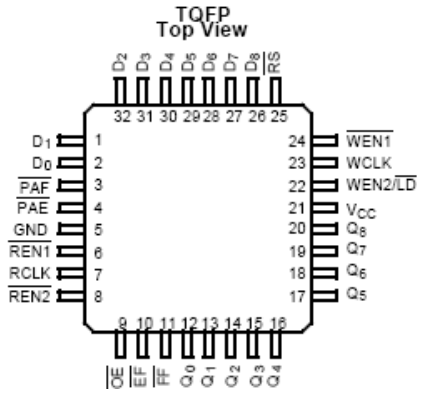
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 32-pin TQFP pinout



Pin Definitions

Signal Name		I/O	Description
D_{0-8}	Data Inputs	I	**Data Inputs for 9-bit bus**.
Q_{0-8}	Data Outputs	O	**Data Outputs for 9-bit bus**.
$\overline{WEN1}$	Write Enable 1	I	**The only write enable when device is configured to have programmable flags**. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ and $\overline{FF}$ are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2	I	**If HIGH at reset, this pin operates as a second write enable**. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
	Load	I	
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	**Enables the device for Read operation**.
WCLK	Write Clock	I	**The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH and the FIFO is not Full**. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	**The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty**. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag offset register.
$\overline{EF}$	Empty Flag	O	**When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK**.
$\overline{FF}$	Full Flag	O	**When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK**.
$\overline{PAE}$	Programmable Almost Empty	O	**When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO**.
$\overline{PAF}$	Programmable Almost Full	O	**When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO**.
$\overline{RS}$	Reset	I	**Resets device to empty condition**. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	**When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected**. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

Selection Guide

Description		CY7C42X1V-15	Unit
Maximum Frequency		66.7	MHz
Maximum Access Time		11	ns
Minimum Cycle Time		15	ns
Minimum Data or Enable Set-up		4	ns
Minimum Data or Enable Hold		1	ns
Maximum Flag Delay		10	ns
Active Power Supply Current	Commercial	20	mA

Architecture

The CY7C42X1V consists of an array of 64 to 8K words of nine bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN1}$, $\overline{REN2}$, WEN1, WEN2, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{FF}$.)

Functional Overview

The CY7C42X1V provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty-7 and Full-7.

The flags are synchronous, that is, they change state relative to either the Read Clock (RCLK) or the Write Clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle

All configurations are fabricated using an advanced 0.65µ P-Well CMOS technology. Input ESD protection is greater than 2001 V, and latch-up is prevented by the use of guard rings.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs (Q_{0-8}) go LOW t_{RSF} after the rising edge of $\overline{RS}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

FIFO Operation

When the $\overline{WEN1}$ signal is active LOW and WEN2 is active HIGH, data present on the D_{0-8} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN1}$ and $\overline{REN2}$ signals are active LOW, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN1}$ and $\overline{REN2}$ are active. $\overline{REN1}$ and $\overline{REN2}$ must set up t_{ENS} before RCLK for it to be a valid read function. WEN1 and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An Output Enable ($\overline{OE}$) pin is provided to three-state the Q_{0-8} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-8} outputs after t_{OE}.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Write Enable 1 ($\overline{WEN1}$). If the FIFO is configured for programmable flags, Write Enable 1 (WEN1) is the only write enable control pin. In this configuration, when Write Enable 1 (WEN1) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load ($\overline{WEN2/LD}$). This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set active HIGH at Reset ($\overline{RS}$=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable (WEN1) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK.) Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

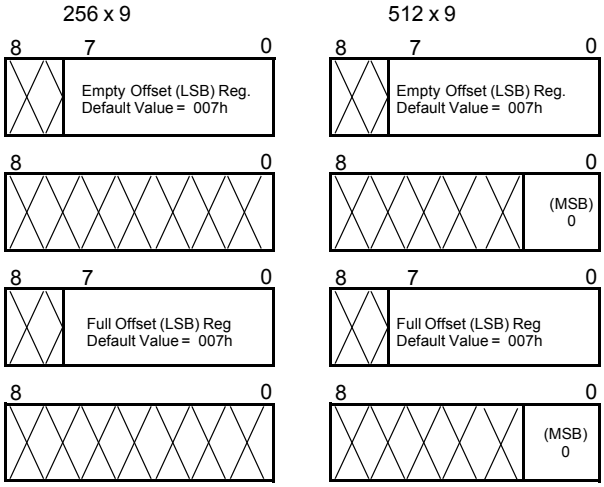
When WEN2/$\overline{LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1V for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset Least Significant Bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset Most Significant Bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW writes data to the empty LSB register again. Figure 2 shows the register sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/$\overline{LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{LD}$ is LOW and both $\overline{REN1}$ and $\overline{REN2}$ are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers.

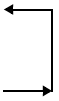
Figure 2. Offset Register Location and Default Values



Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in Table 1 or the default values are used, the programmable Almost Empty Flag ($\overline{PAE}$) and programmable Almost Full Flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers

LD	WEN	WCLK[1]	Selection
0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB) 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAF}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4201V (256 – m) and CY7C4211V (512 – m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 2. Status Flags

Number of Words in FIFO		$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
CY7C4201V	CY7C4211V				
0	0	H	H	L	L
1 to n[2]	1 to n[2]	H	H	L	H
(n+1) to 128	(n+1) to 256	H	H	H	H
129 to (256–(m+1))	257 to (512–(m+1))	H	H	H	H
(256–m)[3] to 255	(512–m)[3] to 511	H	L	H	H
256	512	L	L	H	H

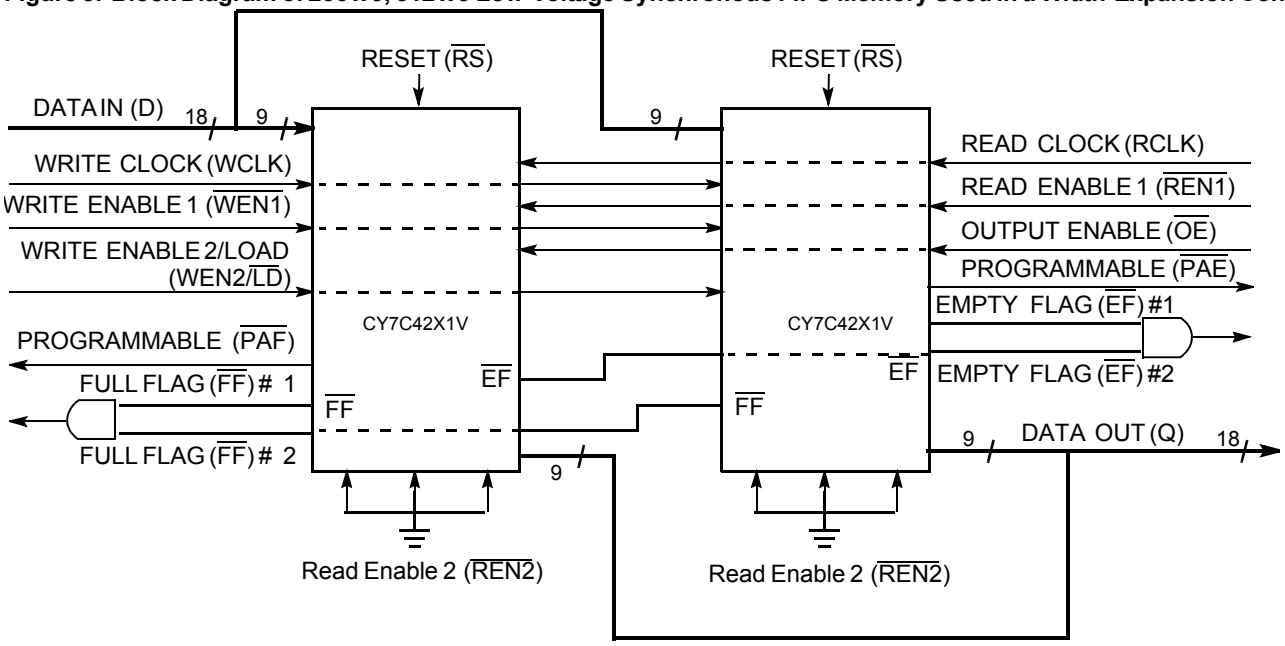
Notes
1. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
2. n = Empty Offset (n=7 default value).
3. m = Full Offset (m=7 default value).

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. Figure 3 demonstrates a 18-bit word width by using two CY7C42X1Vs. Any word width can be attained by adding additional CY7C42X1Vs.

When the CY7C42X1V is in a width expansion configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (see Figure 3). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Figure 3. Block Diagram of 256 x 9, 512 x 9 Low-Voltage Synchronous FIFO Memory Used in a Width-Expansion Configuration



Flag Operation

The CY7C42X1 devices provide four flag pins to indicate the condition of the FIFO contents. Empty, Full, $\overline{PAE}$, and $\overline{PAF}$ are synchronous.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN1}$ and WEN2/$\overline{LD}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –-55 °C to +125 °C

Supply Voltage to Ground Potential ..... –0.5 V to +5.0 V

DC Voltage Applied to Outputs in High-Z State ..... –0.5 V to +5.0 V

DC Input Voltage ..... –0.5 V to +5.0 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 300 mV
Industrial	–40 °C to +85 °C	3.3 V ± 300 mV

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C42X1V-15		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage		2.0	5.0	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.	–10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$	–10	+10	µA
I_{CC}[4]	Active Power Supply Current	Commercial	–	20	mA
I_{SB}[5]	Average Standby Current	Commercial	–	6	mA

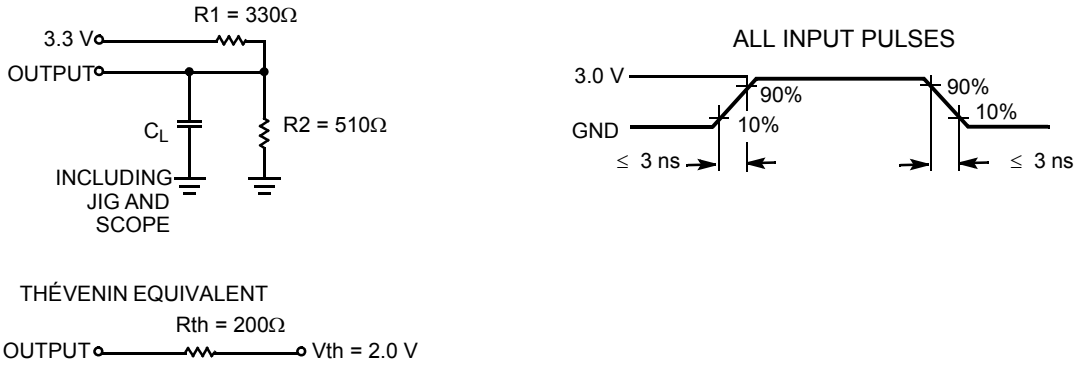
Notes
4. Outputs open. Tested at Frequency = 20 MHz.
5. All inputs = V_{CC} – 0.2 V, except WCLK and RCLK, which are switching at 20 MHz.

Capacitance

Parameter [6]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	5	pF
C_{OUT}	Output capacitance		7	pF

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [7, 8]



Equivalent to: THÉVENIN EQUIVALENT

Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. C_L = 30 pF for all AC parameters except for t_{OHZ}.
8. C_L = 5 pF for t_{OHZ}.

Switching Characteristics

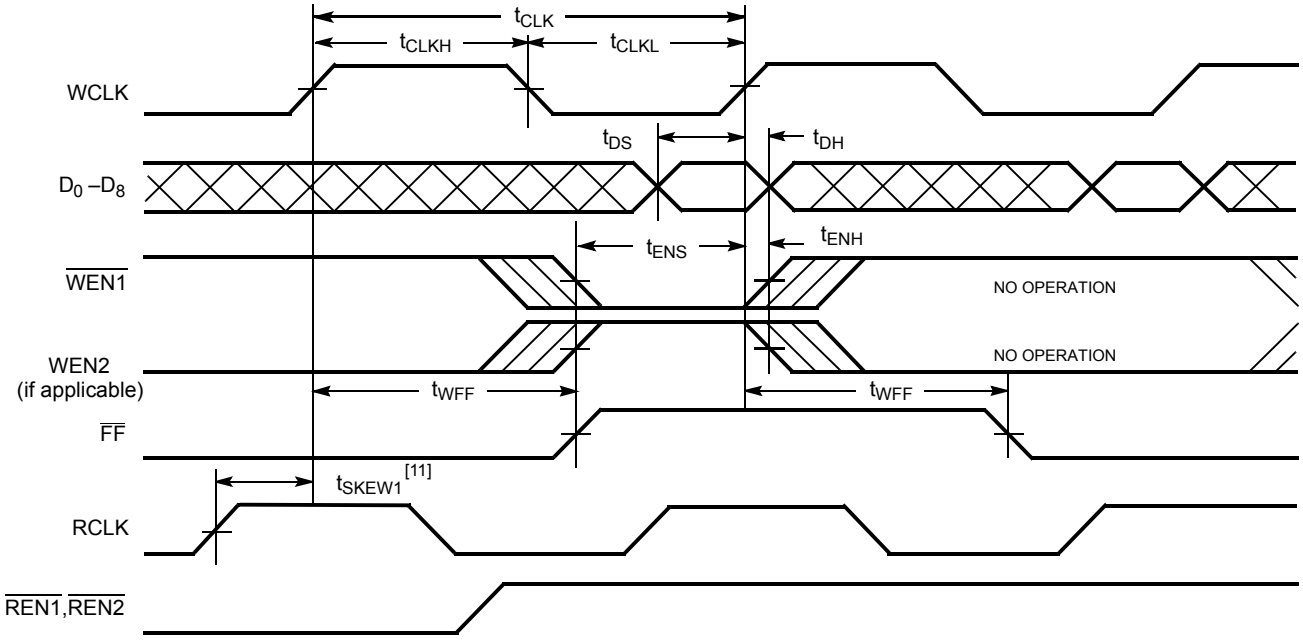
Over the Operating Range

Parameter	Description	7C42X1V-15		Unit
		Min	Max	
t_S	Clock Cycle Frequency	–	66.7	MHz
t_A	Data Access Time	2	11	ns
t_{CLK}	Clock Cycle Time	15	–	ns
t_{CLKH}	Clock HIGH Time	6	–	ns
t_{CLKL}	Clock LOW Time	6	–	ns
t_{DS}	Data Set-Up Time	4	–	ns
t_{DH}	Data Hold Time	1	–	ns
t_{ENS}	Enable Set-Up Time	4	–	ns
t_{ENH}	Enable Hold Time	1	–	ns
t_{RS}	Reset Pulse Width[9]	15	–	ns
t_{RSS}	Reset Set-Up Time	10	–	ns
t_{RSR}	Reset Recovery Time	10	–	ns
t_{RSF}	Reset to Flag and Output Time	–	18	ns
t_{OLZ}	Output Enable to Output in Low Z[10]	0	–	ns
t_{OE}	Output Enable to Output Valid	3	8	ns
t_{OHZ}	Output Enable to Output in High Z[10]	3	8	ns
t_{WFF}	Write Clock to Full Flag	–	11	ns
t_{REF}	Read Clock to Empty Flag	–	11	ns
t_{PAF}	Clock to Programmable Almost-Full Flag	–	16	ns
t_{PAE}	Clock to Programmable Almost-Full Flag	–	16	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	6	–	ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	15	–	ns

Notes
9. Pulse widths less than minimum values are not allowed.
10. Values guaranteed by design, not currently tested.

Switching Waveforms

Figure 5. Write Cycle Timing

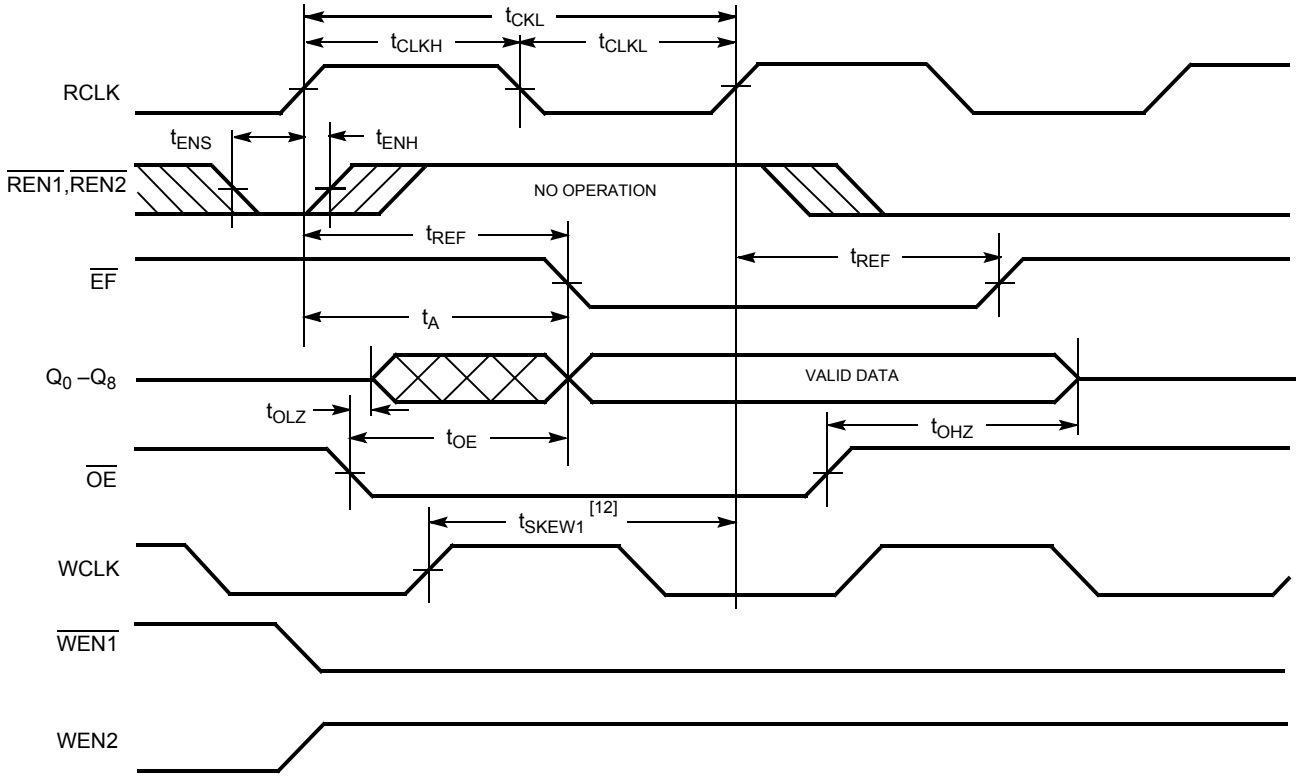


Note

11. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

Figure 6. Read Cycle Timing

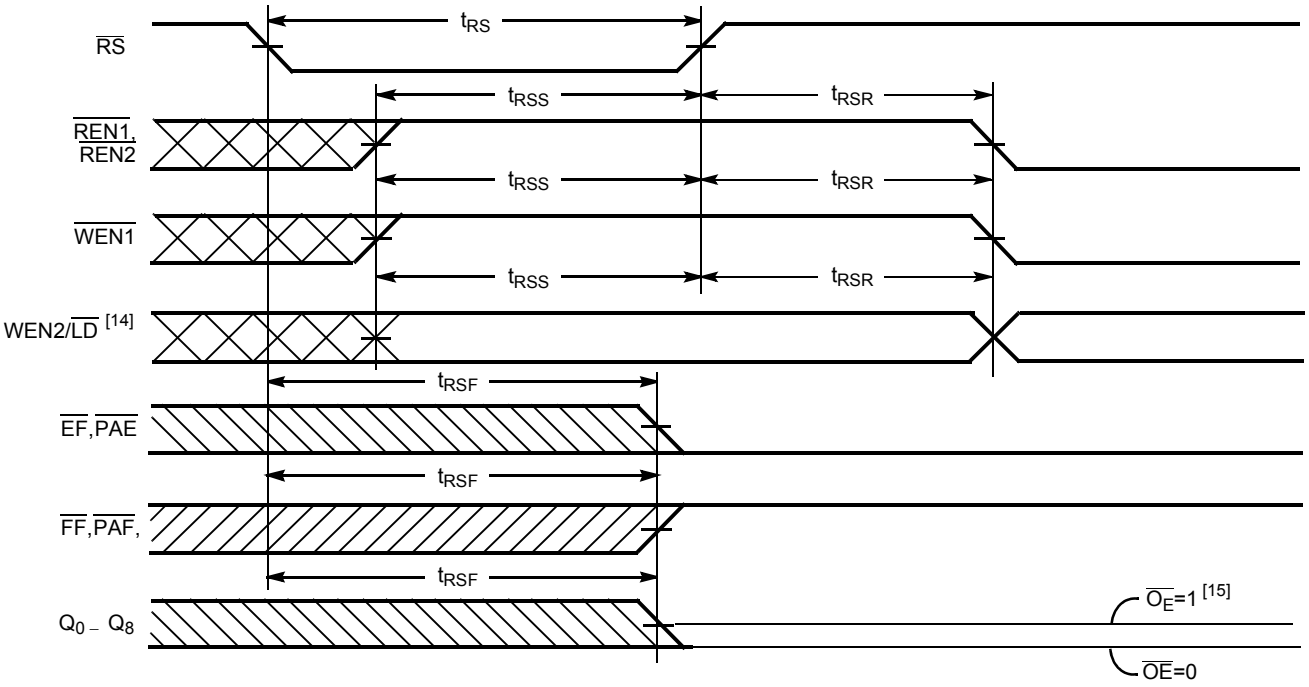


Note

12. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

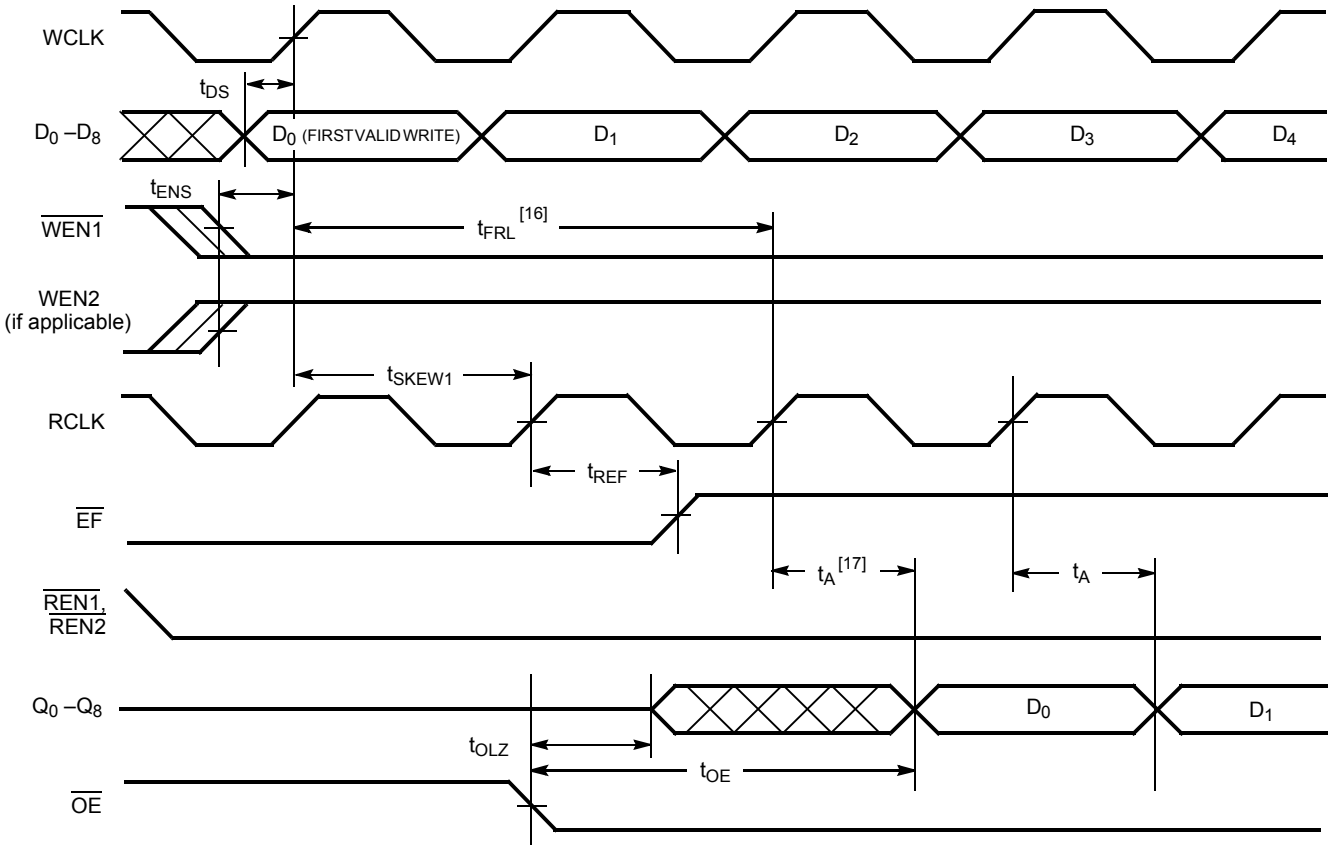
Figure 7. Reset Timing [13]



Notes
13. The clocks (RCLK, WCLK) can be free-running during reset.
14. Holding WEN2/LD HIGH during reset will make the pin act as a second enable pin. Holding WEN2/LD LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
15. After reset, the outputs will be LOW if OE = 0 and three-state if OE = 1.

Switching Waveforms (continued)

Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

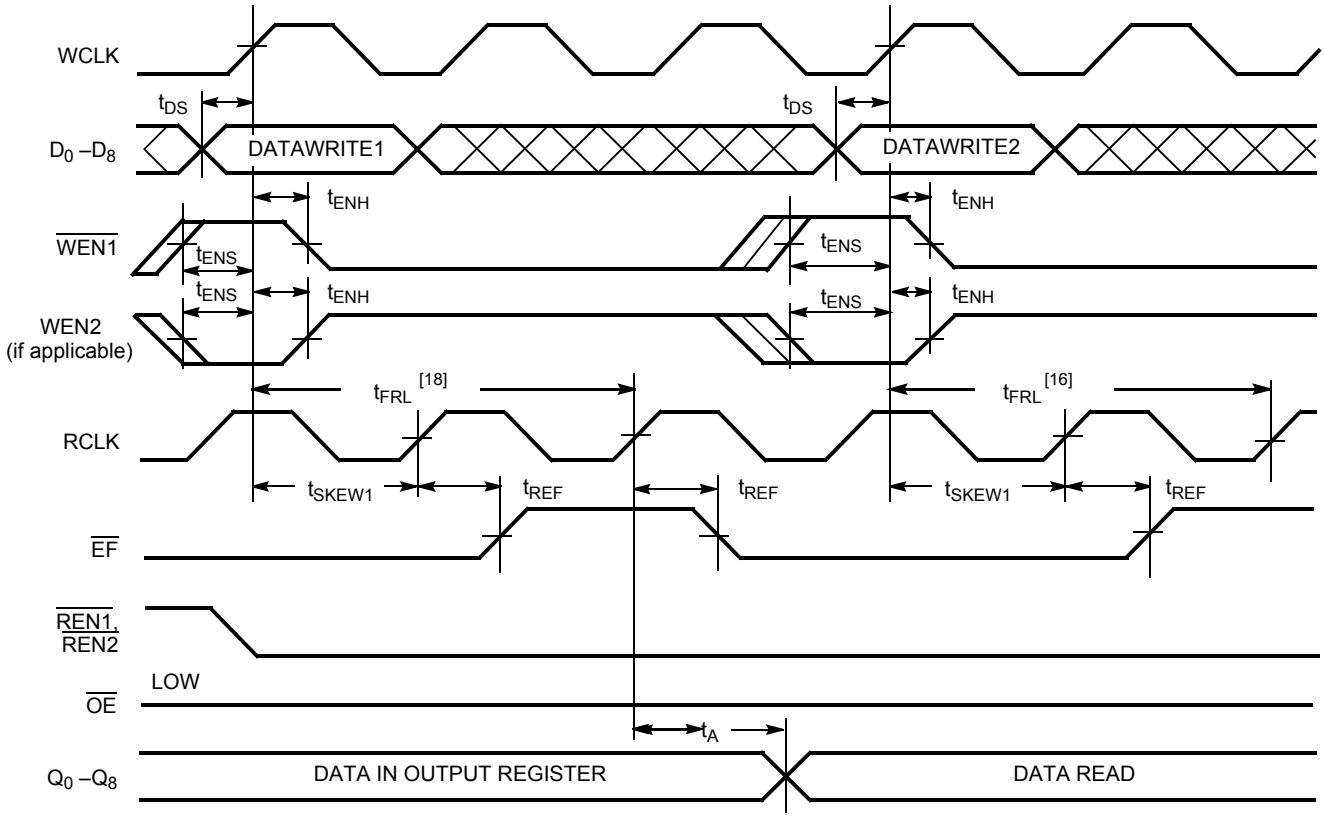


Notes

16. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW1}. When t_{SKEW1} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW1} or t_{CLK} + t_{SKEW1}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
17. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Switching Waveforms (continued)

Figure 9. Empty Flag Timing

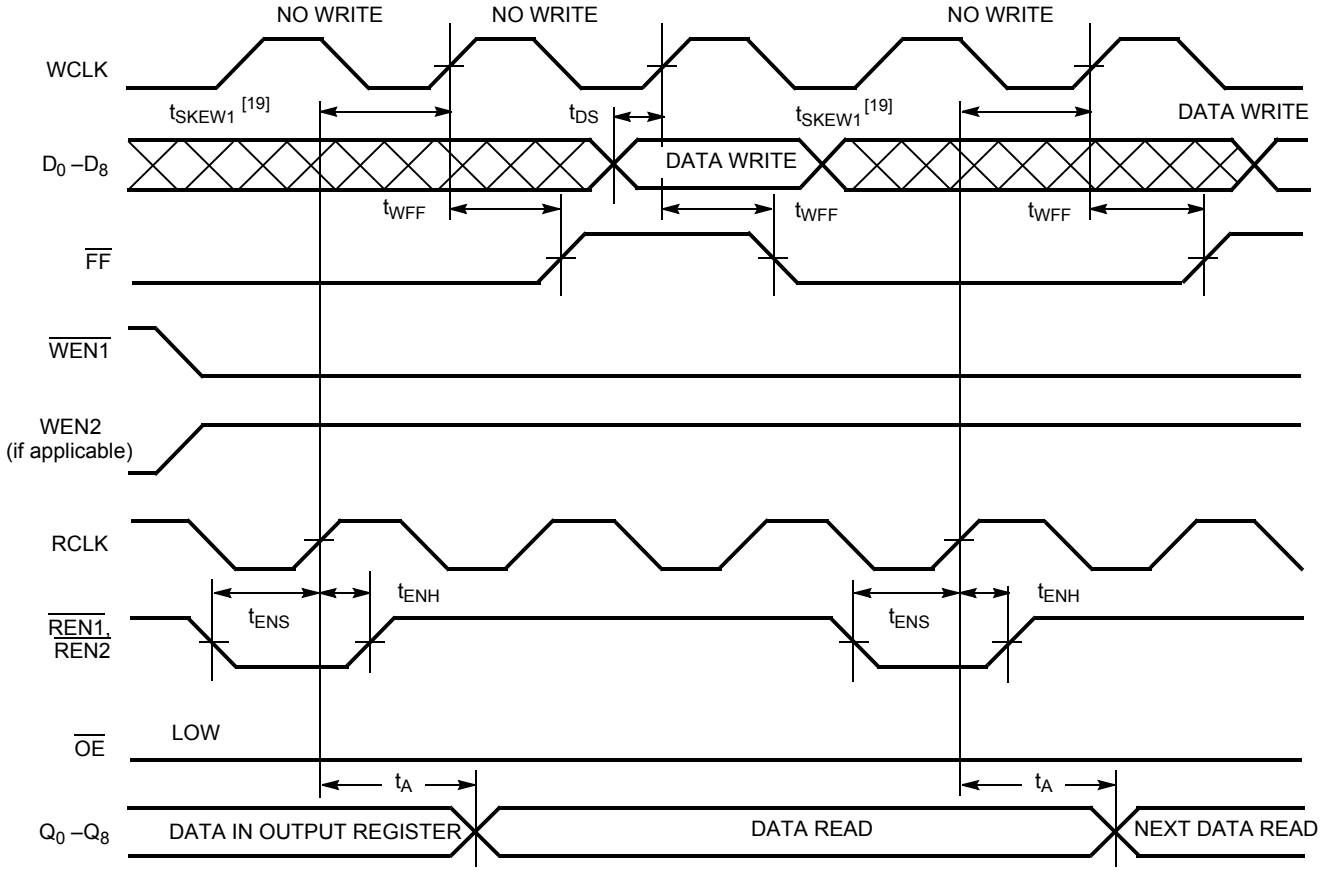


Note

18. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW1}. When t_{SKEW1} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW1} or t_{CLK} + t_{SKEW1}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

Switching Waveforms (continued)

Figure 10. Full Flag Timing



Note

19. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

Figure 11. Programmable Almost Empty Flag Timing

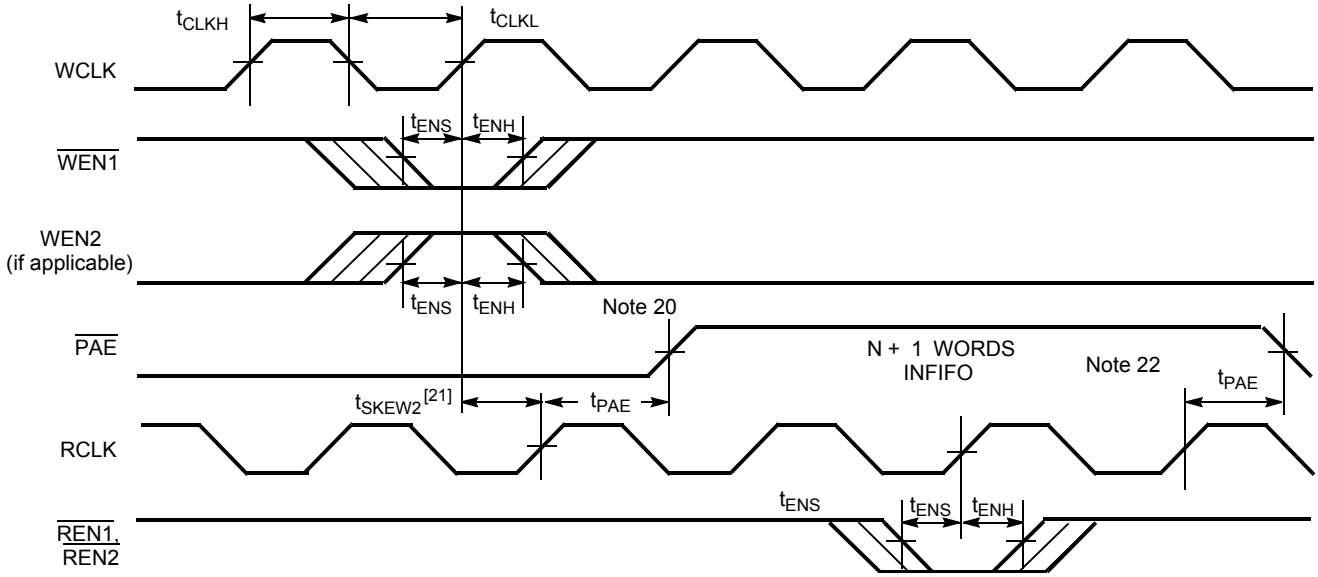
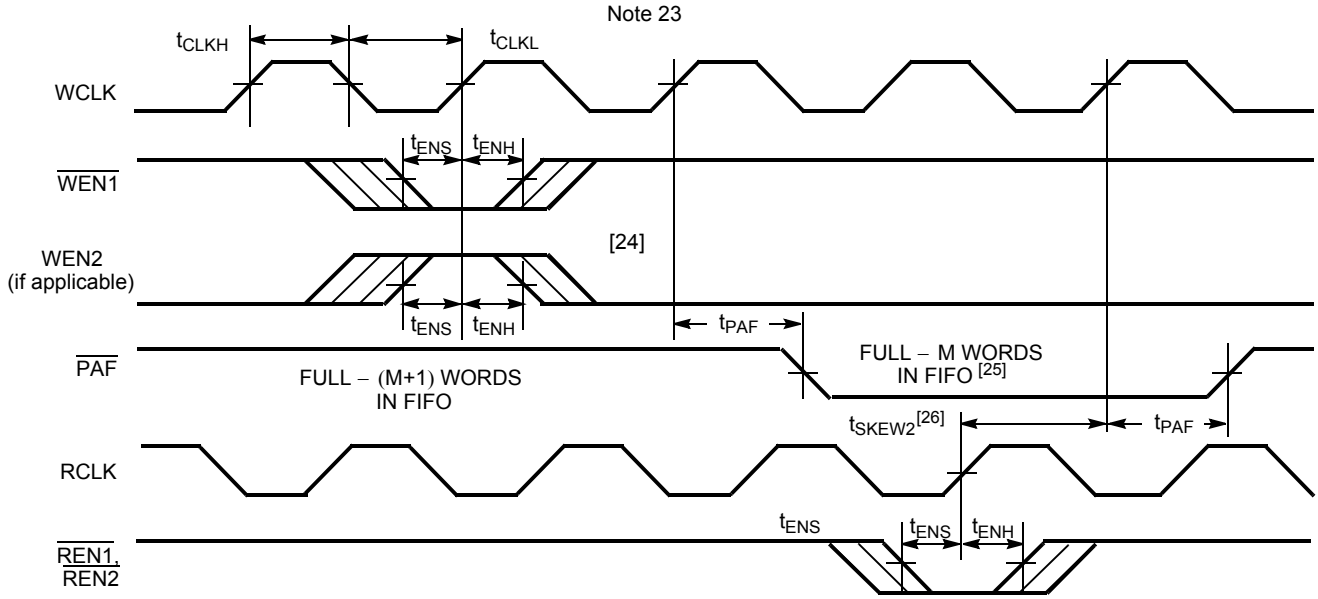


Figure 12. Programmable Almost Full Flag Timing



Notes

20. PAE offset = n.
21. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
22. If a read is performed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.
23. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
24. PAF offset = m.
25. 256-m words in FIFO for CY7C4201V, 512–m words for CY7C4211V
26. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

Switching Waveforms (continued)

Figure 13. Write Programmable Registers

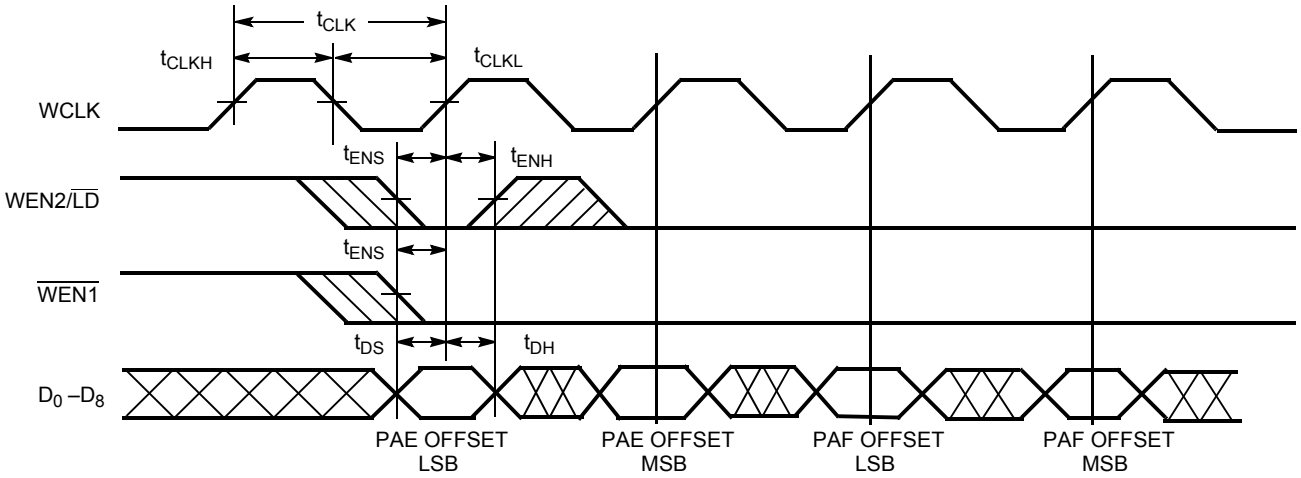
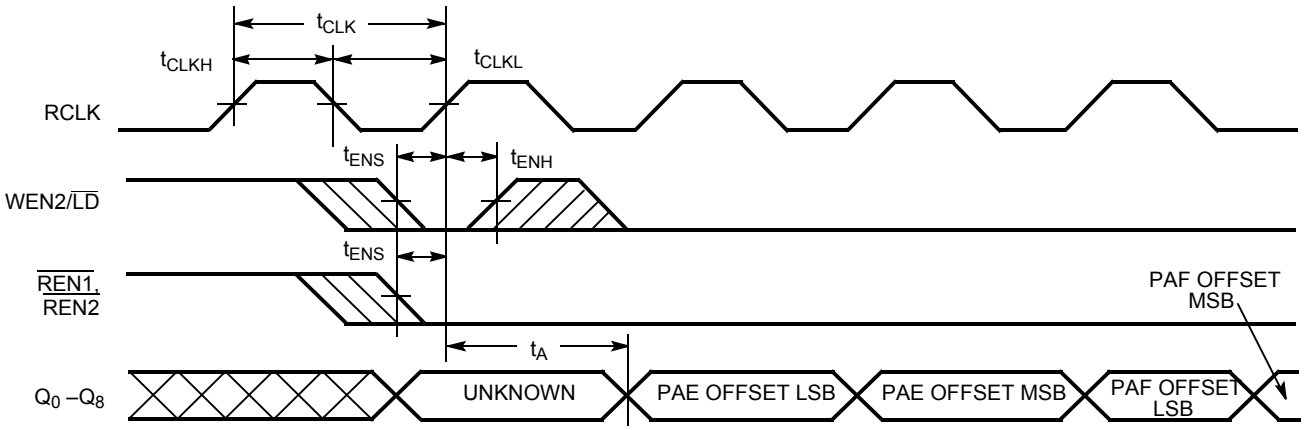


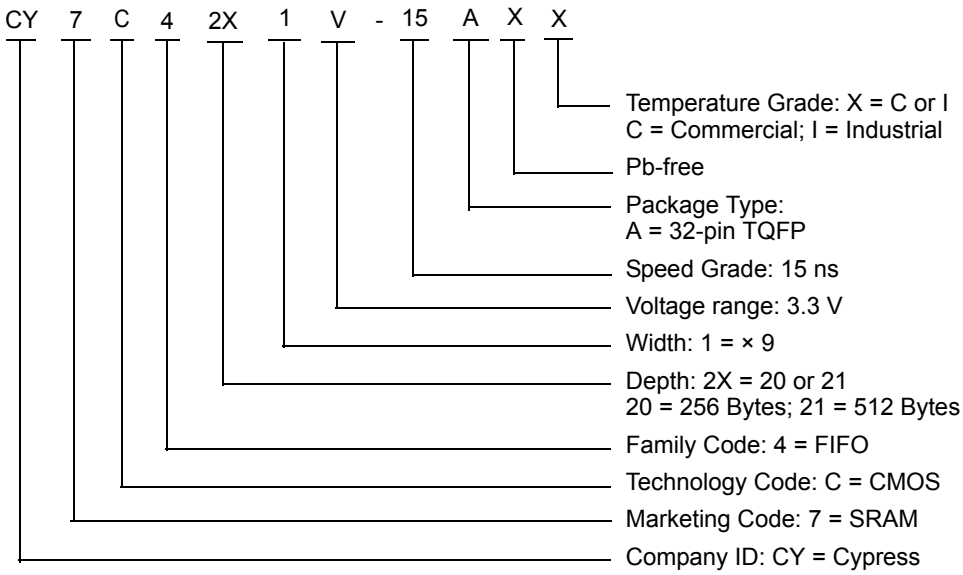
Figure 14. Read Programmable Registers



Ordering Information

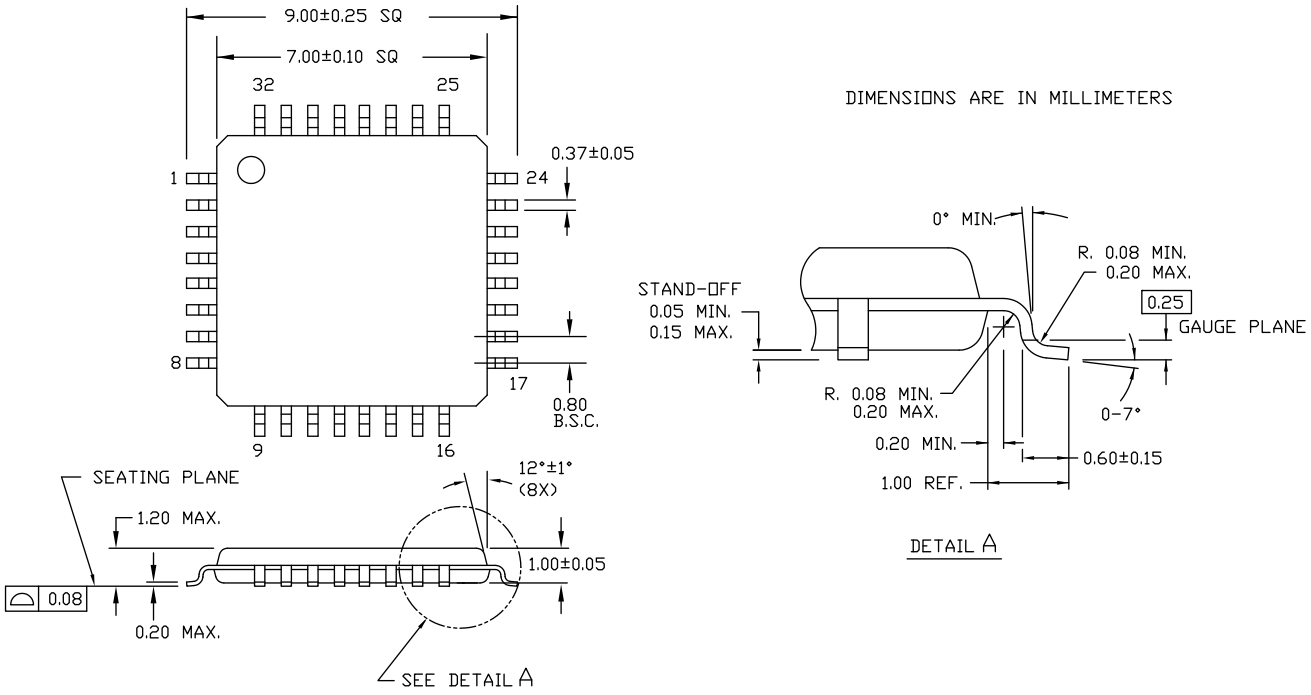
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
256 × 9 Low Voltage Synchronous FIFO				
15	CY7C4201V-15AXC	A32	32-pin TQFP (Pb-free)	Commercial
512 × 9 Low Voltage Synchronous FIFO				
15	CY7C4211V-15AXI	A32	32-pin TQFP (Pb-free)	Industrial

Ordering Code Definitions



Package Diagrams

Figure 15. 32-pin TQFP (7 × 7 × 1.0 mm) Package Outline, 51-85063



51-85063 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{EF}$	Empty Flag
ESD	Electrostatic Discharge
$\overline{FF}$	Full Flag
FIFO	First-In First-Out
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
$\overline{PAE}$	Programmable Almost Empty
$\overline{PAF}$	Programmable Almost Full
RCLK	Read Clock
$\overline{RS}$	Reset
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
WCLK	Write Clock

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C4201V/4211V, Low Voltage 256/512 × 9 Synchronous FIFOs Document Number: 38-06010				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	106471	SZV	09/10/01	Change from Spec number: 38-00622 to 38-06010
*A	127857	FSG	08/25/03	Updated Switching Waveforms: Updated Figure 9. Fixed typos in all figures in the section.
*B	384573	ESH	See ECN	Added Pb-free logo to top of front page. Added industrial Temperature Range related information in all instances across the document. Updated Ordering Information: Added MPNs CY7C4251V-25AXC, CY7C4251V-15AXC, CY7C4241V-15AXC, CY7C4241V-15JXC, CY7C4241V-25XC, CY7C4231V-25AXC, CY7C4221V-15AI, CY7C4211V-15AXI, CY7C4201V-15AXC.
*C	2896039	RAME	03/19/2010	Removed CY7C4421V and CY7C4231V parts related information in all instances across the document. Updated Ordering Information: Removed inactive parts. Updated Package Diagrams.
*D	2965557	RAME	06/30/2010	Removed CY7C4421V, CY7C4221V, CY7C4231V, CY7C4241V and CY7C4251V part related information in all instances across the document. Removed 25 ns and 35 ns speed bins related information in all instances across the document. Updated Ordering Information: Removed inactive parts.
*E	3094385	ADMU	11/24/10	Corrections to the PAE and PAF flags had been done in all instances across the document. Added Ordering Code Definitions.
*F	3847934	ADMU	12/20/2012	Updated Ordering Information (Updated part numbers). Updated Package Diagrams: spec 51-85063 – Changed revision from *C to *D.
*G	4215930	SMCH	12/10/2013	Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*H	4581652	SMCH	11/26/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*I	5018894	NILE	11/18/2015	Updated Package Diagrams: spec 51-85063 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

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