



**CY7C68013A, CY7C68014A  
CY7C68015A, CY7C68016A**

## **EZ-USB<sup>®</sup> FX2LP<sup>™</sup> USB Microcontroller High-Speed USB Peripheral Controller**

### **Features**

- USB 2.0 USB IF high speed certified (TID # 40460272)
- Single chip integrated USB 2.0 transceiver, smart SIE, and enhanced 8051 microprocessor
- Fit, form, and function compatible with the FX2
  - Pin compatible
  - Object code compatible
  - Functionally compatible (FX2LP is a superset)
- Ultra low power: I<sub>CC</sub> No more than 85 mA in any mode
  - Ideal for bus and battery powered applications
- Software: 8051 code runs from:
  - Internal RAM, which is downloaded through USB
  - Internal RAM, which is loaded from EEPROM
  - External memory device (128 pin package)
- 16 KB of on-chip code/data RAM
- Four programmable BULK, INTERRUPT, and ISOCHRONOUS endpoints
  - Buffering options: Double, triple, and quad
- Additional programmable (BULK/INTERRUPT) 64-byte endpoint
- 8-bit or 16-bit external data interface
- Smart media standard ECC generation
- GPIF (general programmable interface)
  - Enables direct connection to most parallel interfaces
  - Programmable waveform descriptors and configuration registers to define waveforms
  - Supports multiple ready (RDY) inputs and Control (CTL) outputs
- Integrated, industry standard enhanced 8051
  - 48 MHz, 24 MHz, or 12 MHz CPU operation
  - Four clocks per instruction cycle
  - Two USARTs
  - Three counter/timers
  - Expanded interrupt system
  - Two data pointers

- 3.3 V operation with 5 V tolerant inputs
- Vectored USB interrupts and GPIF/FIFO interrupts
- Separate data buffers for the setup and data portions of a CONTROL transfer
- Integrated I<sup>2</sup>C controller, runs at 100 or 400 kHz
- Four integrated FIFOs
  - Integrated glue logic and FIFOs lower system cost
  - Automatic conversion to and from 16-bit buses
  - Master or slave operation
  - Uses external clock or asynchronous strobes
  - Easy interface to ASIC and DSP ICs
- Available in commercial and industrial temperature grade (all packages except VFBGA)

### **Features (CY7C68013A/14A only)**

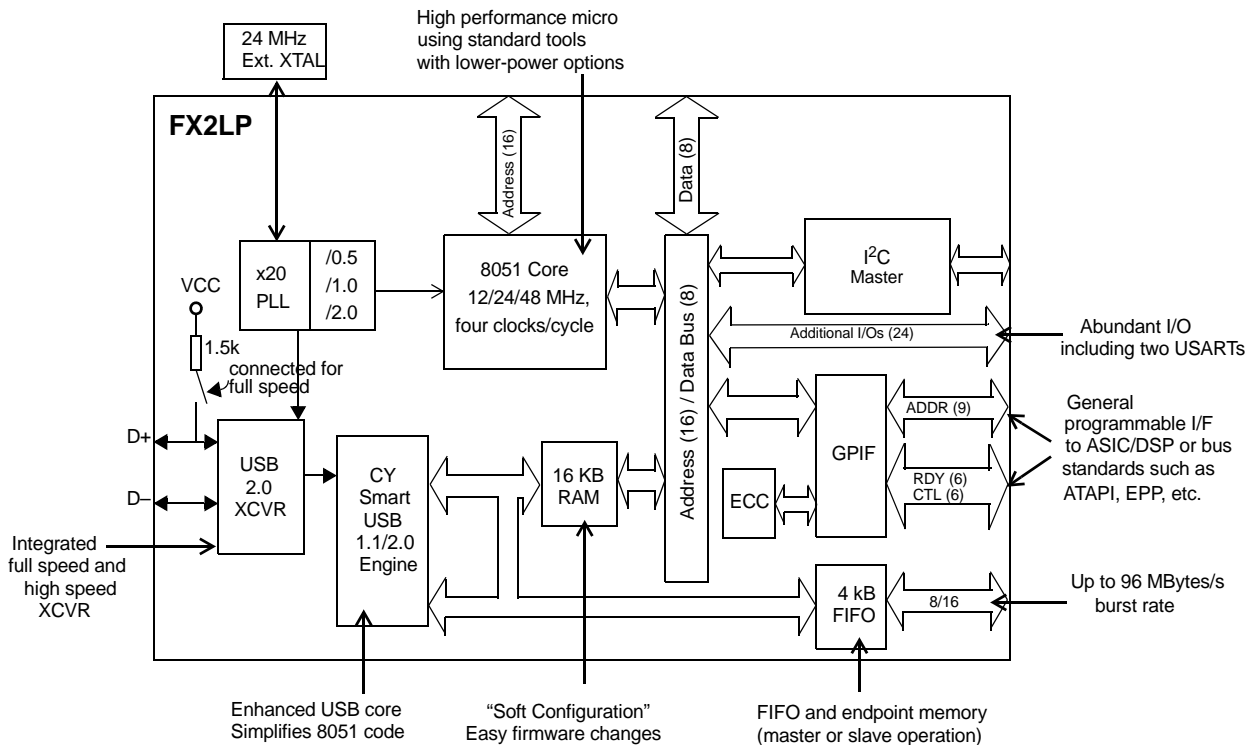
- CY7C68014A: Ideal for Battery Powered Applications
  - Suspend current: 100 μA (typ)
- CY7C68013A: Ideal for Non Battery Powered Applications
  - Suspend current: 300 μA (typ)
- Available in Five Pb-free Packages with Up to 40 GPIOs
  - 128-pin TQFP (40 GPIOs), 100-pin TQFP (40 GPIOs), 56-pin QFN (24 GPIOs), 56-pin SSOP (24 GPIOs), and 56-pin VFBGA (24 GPIOs)

### **Features (CY7C68015A/16A only)**

- CY7C68016A: Ideal for Battery Powered Applications
  - Suspend current: 100 μA (typ)
- CY7C68015A: Ideal for Non Battery Powered Applications
  - Suspend current: 300 μA (typ)
- Available in Pb-free 56-pin QFN Package (26 GPIOs)
- Two more GPIOs than CY7C68013A/14A enabling additional features in same footprint

**Errata:** For information on silicon errata, see "Errata" on page 64. Details include trigger conditions, devices affected, and proposed workaround.

## Logic Block Diagram



Cypress's EZ-USB<sup>®</sup> FX2LP™ (CY7C68013A/14A) is a low power version of the EZ-USB FX2™ (CY7C68013), which is a highly integrated, low power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip,

Cypress has created a cost effective solution that provides superior time-to-market advantages with low power to enable bus powered applications.

The ingenious architecture of FX2LP results in data transfer rates of over 53 Mbytes per second, the maximum allowable USB 2.0 bandwidth, while still using a low cost 8051 microcontroller in a package as small as a 56 VFBGA (5 mm x 5 mm). Because it incorporates the USB 2.0 transceiver, the FX2LP is more economical, providing a smaller footprint solution

than USB 2.0 SIE or external transceiver implementations. With EZ-USB FX2LP, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application specific functions and decreasing development time to ensure USB compatibility.

The General Programmable Interface (GPIF) and Master/Slave Endpoint FIFO (8-bit or 16-bit data bus) provides an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

The FX2LP draws less current than the FX2 (CY7C68013), has double the on-chip code/data RAM, and is fit, form and function compatible with the 56, 100, and 128 pin FX2.

Five packages are defined for the family: 56 VFBGA, 56 SSOP, 56 QFN, 100 TQFP, and 128 TQFP.

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## 1. Applications

- Portable video recorder
- MPEG/TV conversion
- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Cameras
- Scanners
- Wireless LAN
- MP3 players
- Networking

The “Reference Designs” section of the [Cypress web site](http://www.cypress.com) provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Visit [www.cypress.com](http://www.cypress.com) for more information.

## 2. Functional Overview

### 2.1 USB Signaling Speed

FX2LP operates at two of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2LP does not support the low speed signaling mode of 1.5 Mbps.

### 2.2 8051 Microprocessor

The 8051 microprocessor embedded in the FX2LP family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

#### 2.2.1 8051 Clock Frequency

FX2LP has an on-chip oscillator circuit that uses an external 24 MHz ( $\pm 100$  ppm) crystal with the following characteristics:

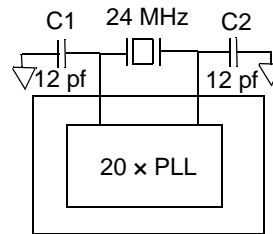
- Parallel resonant
- Fundamental mode
- 500  $\mu$ W drive level
- 12 pF (5% tolerance) load capacitors

An on-chip PLL multiplies the 24 MHz oscillator up to 480 MHz, as required by the transceiver/PHY and internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 can be changed by the 8051 through the CPUCS register, dynamically.

#### Note

1. 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a “1” for UART0, UART1, or both respectively.

**Figure 2-1. Crystal Configuration**



12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four-layer FR4 PCA

The CLKOUT pin, which can be three-stated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency: 48 MHz, 24 MHz, or 12 MHz.

#### 2.2.2 USARTs

FX2LP contains two standard 8051 USARTs, addressed through Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230 KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48 MHz, 24 MHz, and 12 MHz) such that it always presents the correct frequency for 230 KBaud operation.<sup>[1]</sup>

#### 2.2.3 Special Function Registers

Certain 8051 SFR addresses are populated to provide fast access to critical FX2LP functions. These SFR additions are shown in [Table 1 on page 5](#). Bold type indicates non standard, enhanced 8051 registers. The two SFR rows that end with “0” and “8” contain bit addressable registers. The four I/O ports A to D use the SFR addresses used in the standard 8051 for ports 0 to 3, which are not implemented in FX2LP. Because of the faster and more efficient SFR addressing, the FX2LP I/O ports are not addressable in external RAM space (using the MOVX instruction).

### 2.3 I<sup>2</sup>C Bus

FX2LP supports the I<sup>2</sup>C bus as a master only at 100/400 KHz. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to 3.3V, even if no I<sup>2</sup>C device is connected.

### 2.4 Buses

All packages, 8-bit or 16-bit “FIFO” bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output-only 8051 address bus, 8-bit bidirectional data bus.

**Table 1. Special Function Registers**

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	IOA	IOB	IOC	IOD	SCON1	PSW	ACC	B
1	SP	EXIF	INT2CLR	IOE	SBUF1	–	–	–
2	DPL0	MPAGE	INT4CLR	OEA	–	–	–	–
3	DPH0	–	–	OEB	–	–	–	–
4	DPL1	–	–	OEC	–	–	–	–
5	DPH1	–	–	OED	–	–	–	–
6	DPS	–	–	OEE	–	–	–	–
7	PCON	–	–	–	–	–	–	–
8	TCON	SCON0	IE	IP	T2CON	EICON	EIE	EIP
9	TMOD	SBUF0	–	–	–	–	–	–
A	TL0	AUTOPTRH1	EP2468STAT	EP01STAT	RCAP2L	–	–	–
B	TL1	AUTOPTRL1	EP24FIFOFLGS	GPIFTRIG	RCAP2H	–	–	–
C	TH0	reserved	EP68FIFOFLGS		TL2	–	–	–
D	TH1	AUTOPTRH2	–	GPIFSGLDATH	TH2	–	–	–
E	CKCON	AUTOPTRL2	–	GPIFSGLDATLX	–	–	–	–
F	–	reserved	AUTOPTRSET-UP	GPIFSGLDATLNOX	–	–	–	–

**2.5 USB Boot Methods**

During the power up sequence, internal logic checks the I<sup>2</sup>C port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0), or it boot-loads the EEPROM contents into internal RAM (0xC2). If no EEPROM is detected, FX2LP enumerates using internally stored descriptors. The default ID values for FX2LP are VID/PID/DID (0x04B4, 0x8613, 0xAxxx where xxx = Chip revision).<sup>[2]</sup>

**Table 2. Default ID Values for FX2LP**

Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Product ID	0x8613	EZ-USB FX2LP
Device release	0xAxxx	Depends on chip revision (nnn = chip revision where first silicon = 001)

**2.6 ReNumeration**

Because the FX2LP’s configuration is soft, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, the FX2LP enumerates automatically and downloads firmware and USB descriptor tables over the USB cable. Next, the FX2LP enumerates again, this time as a device defined by the downloaded information. This patented two step process called ReNumeration™ happens instantly when the device is plugged in, without a hint that the initial download step has occurred.

**Note**

2. The I<sup>2</sup>C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

Two control bits in the USBCS (USB Control and Status) register, control the ReNumeration process: DISCON and RENUM. To simulate a USB disconnect, the firmware sets DISCON to 1. To reconnect, the firmware clears DISCON to 0.

Before reconnecting, the firmware sets or clears the RENUM bit to indicate whether the firmware or the Default USB Device handles device requests over endpoint zero: if RENUM = 0, the Default USB Device handles device requests; if RENUM = 1, the firmware services the requests.

**2.7 Bus-Powered Applications**

The FX2LP fully supports bus powered designs by enumerating with less than 100 mA as required by the USB 2.0 specification.

**2.8 Interrupt System**

*2.8.1 INT2 Interrupt Request and Enable Registers*

FX2LP implements an autovector feature for INT2 and INT4. There are 27 INT2 (USB) vectors, and 14 INT4 (FIFO/GPIF) vectors. See EZ-USB Technical Reference Manual (TRM) for more details.

*2.8.2 USB Interrupt Autovectors*

The main USB interrupt is shared by 27 interrupt sources. To save the code and processing time that is required to identify the individual USB interrupt source, the FX2LP provides a second level of interrupt vectoring, called Autovectoring. When a USB interrupt is asserted, the FX2LP pushes the program counter to its stack, and then jumps to the address 0x0043 where it expects to find a “jump” instruction to the USB Interrupt service routine.

The FX2LP jump instruction is encoded as follows:

**Table 3. INT2 USB Interrupts**

USB INTERRUPT TABLE FOR INT2			
Priority	INT2VEC Value	Source	Notes
1	00	SUDAV	Setup data available
2	04	SOF	Start of frame (or microframe)
3	08	SUTOK	Setup token received
4	0C	SUSPEND	USB suspend request
5	10	USB RESET	Bus reset
6	14	HISPEED	Entered high speed operation
7	18	EP0ACK	FX2LP ACK'd the CONTROL Handshake
8	1C		reserved
9	20	EP0-IN	EP0-IN ready to be loaded with data
10	24	EP0-OUT	EP0-OUT has USB data
11	28	EP1-IN	EP1-IN ready to be loaded with data
12	2C	EP1-OUT	EP1-OUT has USB data
13	30	EP2	IN: buffer available. OUT: buffer has data
14	34	EP4	IN: buffer available. OUT: buffer has data
15	38	EP6	IN: buffer available. OUT: buffer has data
16	3C	EP8	IN: buffer available. OUT: buffer has data
17	40	IBN	IN-Bulk-NAK (any IN endpoint)
18	44		reserved
19	48	EP0PING	EP0 OUT was pinged and it NAK'd
20	4C	EP1PING	EP1 OUT was pinged and it NAK'd
21	50	EP2PING	EP2 OUT was pinged and it NAK'd
22	54	EP4PING	EP4 OUT was pinged and it NAK'd
23	58	EP6PING	EP6 OUT was pinged and it NAK'd
24	5C	EP8PING	EP8 OUT was pinged and it NAK'd
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64	–	–
27	68	–	Reserved
28	6C	–	Reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

If Autovectoring is enabled (AV2EN = 1 in the INTSET-UP register), the FX2LP substitutes its INT2VEC byte. Therefore, if the high byte (“page”) of a jump table address is preloaded at the location 0x0044, the automatically inserted INT2VEC byte at 0x0045 directs the jump to the correct address out of the 27 addresses within the page.

### 2.8.3 FIFO/GPIF Interrupt (INT4)

Just as the USB Interrupt is shared among 27 individual USB interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, similar to the USB Interrupt, can employ autovectoring. [Table 4 on page 7](#) shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources.

**Table 4. Individual FIFO/GPIF Interrupt Sources**

Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 programmable flag
2	84	EP4PF	Endpoint 4 programmable flag
3	88	EP6PF	Endpoint 6 programmable flag
4	8C	EP8PF	Endpoint 8 programmable flag
5	90	EP2EF	Endpoint 2 empty flag <sup>[3]</sup>
6	94	EP4EF	Endpoint 4 empty flag
7	98	EP6EF	Endpoint 6 empty flag
8	9C	EP8EF	Endpoint 8 empty flag
9	A0	EP2FF	Endpoint 2 full flag
10	A4	EP4FF	Endpoint 4 full flag
11	A8	EP6FF	Endpoint 6 full flag
12	AC	EP8FF	Endpoint 8 full flag
13	B0	GPIFDONE	GPIF operation complete
14	B4	GPIFWF	GPIF waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSET-UP register), the FX 2LP substitutes its INT4VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14

addresses within the page. When the ISR occurs, the FX2LP pushes the program counter to its stack then jumps to address 0x0053, where it expects to find a “jump” instruction to the ISR Interrupt service routine.

**Note**

- Errata:** In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction. For more information, see the “Errata” on page 64.

## 2.9 Reset and Wakeup

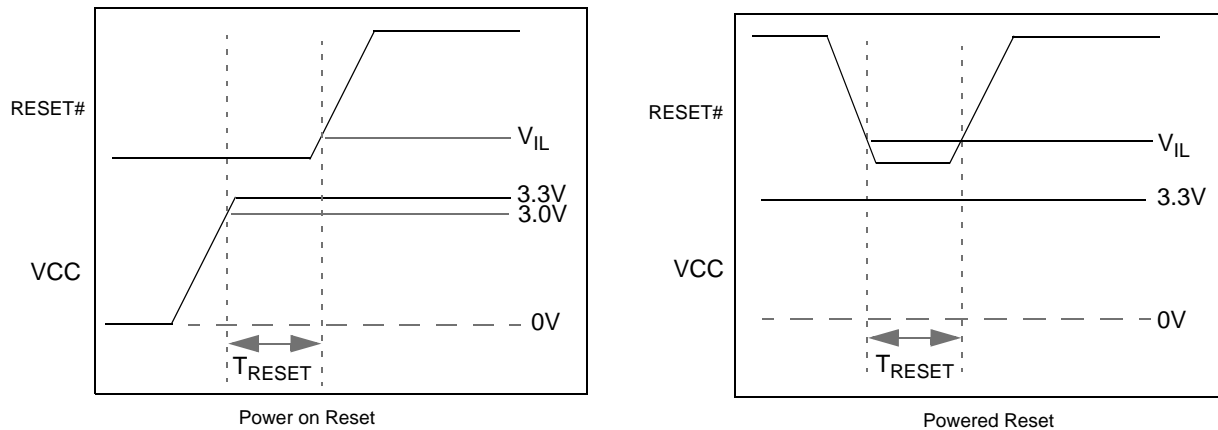
### 2.9.1 Reset Pin

The input pin, RESET#, resets the FX2LP when asserted. This pin has hysteresis and is active LOW. When a crystal is used with the CY7C680xxA the reset period must enable stabilization of the crystal and the PLL. This reset period must be approximately 5 ms after VCC reaches 3.0V. If the crystal input pin is driven by a clock signal the internal PLL stabilizes in 200  $\mu$ s after VCC has reached 3.0V.<sup>[4]</sup>

Figure 2-2 on page 8 shows a power on reset condition and a reset applied during operation. A power on reset is defined as the time reset that is asserted while power is being applied to the circuit. A powered reset is when the FX2LP powered on and operating and the RESET# pin is asserted.

Cypress provides an application note which describes and recommends power on reset implementation. For more information about reset implementation for the FX2 family of products visit <http://www.cypress.com>.

**Figure 2-2. Reset Timing Plots**



**Table 2-1. Reset Timing Values**

Condition	$T_{\text{RESET}}$
Power on reset with crystal	5 ms
Power on reset with external clock	200 $\mu$ s + Clock stability time
Powered Reset	200 $\mu$ s

### 2.9.2 Wakeup Pins

The 8051 puts itself and the rest of the chip into a power down mode by setting PCON.0 = 1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic the oscillator restarts after the PLL stabilizes, and the 8051 receives a wakeup

interrupt. This applies whether or not FX2LP is connected to the USB.

The FX2LP exits the power down (USB suspend) state using one of the following methods:

- USB bus activity (if D+/D- lines are left floating, noise on these lines may indicate activity to the FX2LP and initiate a wakeup)
- External logic asserts the WAKEUP pin
- External logic asserts the PA3/WU2 pin

The second wakeup pin, WU2, can also be configured as a general purpose I/O pin. This enables a simple external R-C network to be used as a periodic wakeup source. WAKEUP is by default active LOW.

**Note**

4. If the external clock is powered at the same time as the CY7C680xxA and has a stabilization wait period, it must be added to the 200  $\mu$ s.



## 2.10 Program/Data RAM

### 2.10.1 Size

The FX2LP has 16 KBytes of internal program/data RAM, where PSEN#/RD# signals are internally ORed to enable the 8051 to access it as both program and data memory. No USB control registers appear in this space.

Two memory maps are shown in the following diagrams:

Figure 2-3 on page 9 shows the Internal Code Memory, EA = 0

Figure 2-4 on page 10 shows the External Code Memory, EA = 1.

### 2.10.2 Internal Code Memory, EA = 0

This mode implements the internal 16 KByte block of RAM (starting at 0) as combined code and data memory. When external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the

chip. This enables the user to connect a 64 KByte memory without requiring address decodes to keep clear of internal memory spaces.

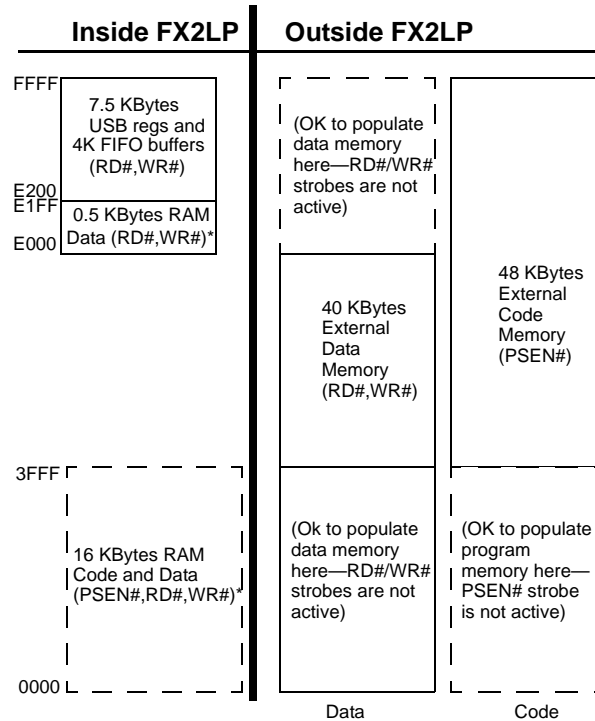
Only the internal 16 KBytes and scratch pad 0.5 KBytes RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- I<sup>2</sup>C interface boot load.

### 2.10.3 External Code Memory, EA = 1

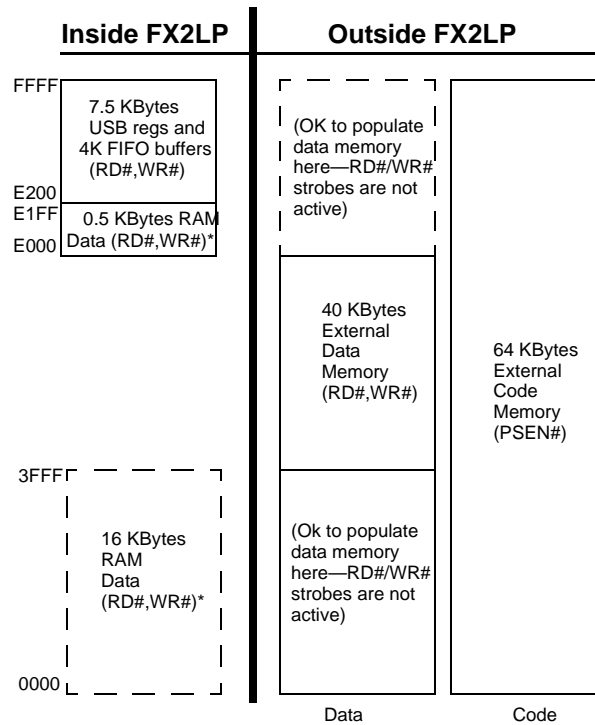
The bottom 16 KBytes of program memory is external and therefore the bottom 16 KBytes of internal RAM is accessible only as a data memory.

**Figure 2-3. Internal Code Memory, EA = 0**



\*SUDPTR, USB upload/download, I<sup>2</sup>C interface boot access

Figure 2-4. External Code Memory, EA = 1



\*SUDPTR, USB upload/download, I<sup>2</sup>C interface boot access

## 2.11 Register Addresses

FFFF	4 KBytes EP2-EP8 buffers (8 x 512)
F000	2 KBytes RESERVED
EFFF	
E800	64 Bytes EP1IN
E7FF	
E7C0	64 Bytes EP1OUT
E7BF	
E780	64 Bytes EP0 IN/OUT
E77F	
E740	64 Bytes RESERVED
E73F	
E700	8051 Addressable Registers (512)
E6FF	
E500	Reserved (128)
E4FF	
E480	128 bytes GPIF Waveforms
E47F	
E400	Reserved (512)
E3FF	
E200	512 bytes 8051 xdata RAM
E1FF	
E000	

## 2.12 Endpoint RAM

### 2.12.1 Size

- 3 × 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

### 2.12.2 Organization

- EP0
- Bidirectional endpoint zero, 64 byte buffer
- EP1IN, EP1OUT
- 64 byte buffers, bulk or interrupt
- EP2, 4, 6, 8
- Eight 512 byte buffers, bulk, interrupt, or isochronous. EP4 and EP8 can be double buffered; EP2 and 6 can be either double, triple, or quad buffered. For high speed endpoint configuration options, see [Figure 2-5](#).

### 2.12.3 Setup Data Buffer

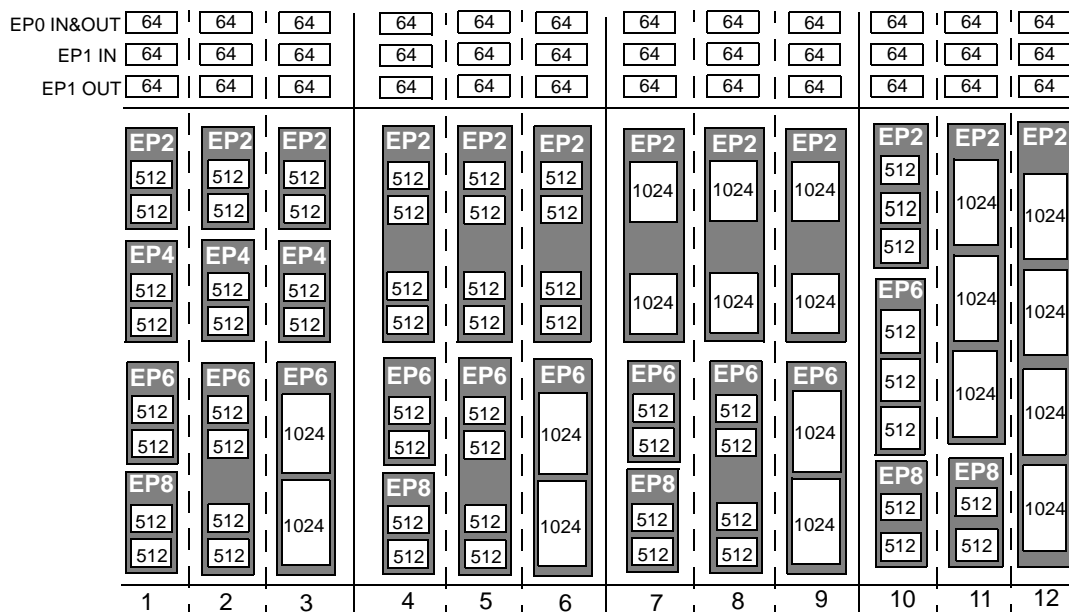
A separate 8 byte buffer at 0xE6B8-0xE6BF holds the setup data from a CONTROL transfer.

### 2.12.4 Endpoint Configurations (High Speed Mode)

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT.

The endpoint buffers can be configured in any 1 of the 12 configurations shown in the vertical columns. When operating in the full speed BULK mode only the first 64 bytes of each buffer are used. For example, in high speed, the max packet size is 512 bytes but in full speed it is 64 bytes. Even though a buffer is configured to a 512 byte buffer, in full speed only the first 64 bytes are used. The unused endpoint buffer space is not available for other operations. An example endpoint configuration is the EP2–1024 double buffered; EP6–512 quad buffered (column 8).

**Figure 2-5. Endpoint Configuration**



2.12.5 Default Full Speed Alternate Settings

**Table 5. Default Full Speed Alternate Settings<sup>[5, 6]</sup>**

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	64 bulk	64 int	64 int
ep1in	0	64 bulk	64 int	64 int
ep2	0	64 bulk out (2x)	64 int out (2x)	64 iso out (2x)
ep4	0	64 bulk out (2x)	64 bulk out (2x)	64 bulk out (2x)
ep6	0	64 bulk in (2x)	64 int in (2x)	64 iso in (2x)
ep8	0	64 bulk in (2x)	64 bulk in (2x)	64 bulk in (2x)

2.12.6 Default High Speed Alternate Settings

**Table 6. Default High Speed Alternate Settings<sup>[5, 6]</sup>**

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	512 bulk <sup>[7]</sup>	64 int	64 int
ep1in	0	512 bulk <sup>[7]</sup>	64 int	64 int
ep2	0	512 bulk out (2x)	512 int out (2x)	512 iso out (2x)
ep4	0	512 bulk out (2x)	512 bulk out (2x)	512 bulk out (2x)
ep6	0	512 bulk in (2x)	512 int in (2x)	512 iso in (2x)
ep8	0	512 bulk in (2x)	512 bulk in (2x)	512 bulk in (2x)

**2.13 External FIFO Interface**

2.13.1 Architecture

The FX2LP slave FIFO architecture has eight 512 byte blocks in the endpoint RAM that directly serve as FIFO memories and are controlled by FIFO control signals (such as IFCLK, SLCS#, SLRD, SLWR, SLOE, PKTEND, and flags).

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms, the GPIF for internally generated control signals and the slave FIFO interface for externally controlled transfers.

2.13.2 Master/Slave Control Signals

The FX2LP endpoint FIFOs are implemented as eight physically distinct 256x16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains, the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done virtually instantaneously, giving essentially zero transfer time between “USB FIFOs” and “Slave FIFOs.” Because they are physically the same memory no bytes are actually transferred between buffers.

At any time, some RAM blocks are filling/emptying with USB data under SIE control, while other RAM blocks are available to the 8051, the I/O control unit or both. The RAM blocks operate as single port in the USB domain, and dual port in the 8051-I/O

domain. The blocks can be configured as single, double, triple, or quad buffered as previously shown.

The I/O control unit implements either an internal master (M for master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) can be used as flag inputs from an external FIFO or other logic if desired. The GPIF can be run from either an internally derived clock or externally supplied clock (IFCLK), at a rate that transfers data up to 96 Megabytes/s (48 MHz IFCLK with 16-bit interface).

In Slave (S) mode, the FX2LP accepts either an internally derived clock or externally supplied clock (IFCLK, max frequency 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. When using an external IFCLK, the external clock must be present before switching to the external clock with the IFCLKSRC bit. Each endpoint can individually be selected for byte or word operation by an internal configuration bit and a Slave FIFO Output Enable signal SLOE enables data of the selected width. External logic must ensure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in synchronous mode. The signals SLRD, SLWR, SLOE and PKTEND are gated by the signal SLCS#.

**Notes**

- 5. “0” means “not implemented.”
- 6. “2x” means “double buffered.”
- 7. Even though these buffers are 64 bytes, they are reported as 512 for USB 2.0 compliance. The user must never transfer packets larger than 64 bytes to EP1.

### 2.13.3 GPIF and FIFO Clock Rates

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 MHz–48 MHz feeding the IFCLK pin can be used as the interface clock. IFCLK can be configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register inverts the IFCLK signal whether internally or externally sourced.

## 2.14 GPIF

The GPIF is a flexible 8-bit or 16-bit parallel interface driven by a user programmable finite state machine. It enables the CY7C68013A/15A to perform local bus mastering and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADR<sub>x</sub>), and six general-purpose ready inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a ready input (or multiple inputs) must be before proceeding. The GPIF vector can be programmed to advance a FIFO to the next data value, advance an address, etc. A sequence of the GPIF vectors make up a single waveform that is executed to perform the desired data move between the FX2LP and the external device.

### 2.14.1 Six Control OUT Signals

The 100-pin and 128-pin packages bring out all six Control Output pins (CTL0–CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals, CTL0–CTL2. CTL<sub>x</sub> waveform edges can be programmed to make transitions as fast as once per clock (20.8 ns using a 48 MHz clock).

### 2.14.2 Six Ready IN Signals

The 100-pin and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56-pin package brings out two of these signals, RDY0–1.

### 2.14.3 Nine GPIF Address OUT Signals

Nine GPIF address lines are available in the 100-pin and 128-pin packages, GPIFADR[8..0]. The GPIF address lines enable indexing through up to a 512 byte block of RAM. If more address lines are needed I/O port pins are used.

### 2.14.4 Long Transfer Mode

In the master mode, the 8051 appropriately sets GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to 2<sup>32</sup> transactions. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

## Notes

8. To use the ECC logic, the GPIF or Slave FIFO interface must be configured for byte-wide operation.
9. After the data is downloaded from the host, a "loader" can execute from internal RAM to transfer downloaded data to external memory.

## 2.15 ECC Generation<sup>[8]</sup>

The EZ-USB can calculate ECCs (Error Correcting Codes) on data that passes across its GPIF or Slave FIFO interfaces. There are two ECC configurations: Two ECCs, each calculated over 256 bytes (SmartMedia Standard); and one ECC calculated over 512 bytes.

The ECC can correct any one-bit error or detect any two-bit error.

### 2.15.1 ECC Implementation

The two ECC configurations are selected by the ECCM bit:

#### ECCM = 0

Two 3 byte ECCs, each calculated over a 256 byte block of data. This configuration conforms to the SmartMedia Standard.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 256 bytes of data is calculated and stored in ECC1. The ECC for the next 256 bytes is stored in ECC2. After the second ECC is calculated, the values in the ECC<sub>x</sub> registers do not change until ECCRESET is written again, even if more data is subsequently passed across the interface.

#### ECCM = 1

One 3 byte ECC calculated over a 512 byte block of data.

Write any value to ECCRESET then pass data across the GPIF or Slave FIFO interface. The ECC for the first 512 bytes of data is calculated and stored in ECC1; ECC2 is unused. After the ECC is calculated, the values in ECC1 do not change even if more data is subsequently passed across the interface, till ECCRESET is written again.

## 2.16 USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 16 KByte RAM and of the internal 512 byte scratch pad RAM via a vendor specific command. This capability is normally used when soft downloading user code and is available only to and from internal RAM, only when the 8051 is held in reset. The available RAM spaces are 16 KBytes from 0x0000–0x3FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad data RAM).<sup>[9]</sup>

## 2.17 Autopointer Access

FX2LP provides two identical autopointers. They are similar to the internal 8051 data pointers but with an additional feature: they can optionally increment after every memory access. This capability is available to and from both internal and external RAM. The autopointers are available in external FX2LP registers under control of a mode bit (AUTOPTRSET-UP.0). Using the external FX2LP autopointer access (at 0xE67B – 0xE67C) enables the autopointer to access all internal and external RAM to the part.

Also, the autopointers can point to any FX2LP register or endpoint buffer space. When autopointer access to external memory is enabled, location 0xE67B and 0xE67C in XDATA and code space cannot be used.

## 2.18 I<sup>2</sup>C Controller

FX2LP has one I<sup>2</sup>C port that is driven by two internal controllers, one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051 uses when running to control external I<sup>2</sup>C devices. The I<sup>2</sup>C port operates in master mode only.

### 2.18.1 I<sup>2</sup>C Port Pins

The I<sup>2</sup>C pins SCL and SDA must have external 2.2 kΩ pull up resistors even if no EEPROM is connected to the FX2LP. External EEPROM device address pins must be configured properly. See [Table 7](#) for configuring the device address pins.

**Table 7. Strap Boot EEPROM Address Lines to These Values**

Bytes	Example EEPROM	A2	A1	A0
16	24LC00 <sup>[10]</sup>	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1
16K	24LC128	0	0	1

### 2.18.2 I<sup>2</sup>C Interface Boot Load Access

At power on reset the I<sup>2</sup>C interface boot loader loads the VID/PID/DID configuration bytes and up to 16 KBytes of program/data. The available RAM spaces are 16 KBytes from 0x0000–0x3FFF and 512 bytes from 0xE000–0xE1FF. The 8051 is in reset. I<sup>2</sup>C interface boot loads only occur after power on reset.

### 2.18.3 I<sup>2</sup>C Interface General-Purpose Access

The 8051 can control peripherals connected to the I<sup>2</sup>C bus using the I<sup>2</sup>CTL and I2DAT registers. FX2LP provides I<sup>2</sup>C master control only, it is never an I<sup>2</sup>C slave.

## 2.19 Compatible with Previous Generation EZ-USB FX2

The EZ-USB FX2LP is form, fit and with minor exceptions functionally compatible with its predecessor, the EZ-USB FX2. This makes for an easy transition for designers wanting to upgrade their systems from the FX2 to the FX2LP. The pinout and package selection are identical and a vast majority of firmware previously developed for the FX2 functions in the FX2LP.

For designers migrating from the FX2 to the FX2LP a change in the bill of material and review of the memory allocation (due to increased internal memory) is required. For more information about migrating from EZ-USB FX2 to EZ-USB FX2LP, see the application note titled *Migrating from EZ-USB FX2 to EZ-USB FX2LP* available in the [Cypress web site](#).

**Table 8. Part Number Conversion Table**

EZ-USB FX2 Part Number	EZ-USB FX2LP Part Number	Package Description
CY7C68013-56PVC	CY7C68013A-56PVXC or CY7C68014A-56PVXC	56-pin SSOP
CY7C68013-56PVCT	CY7C68013A-56PVXCT or CY7C68014A-56PVXCT	56-pin SSOP – Tape and Reel
CY7C68013-56LFC	CY7C68013A-56LFXC or CY7C68014A-56LFXC	56-pin QFN
CY7C68013-100AC	CY7C68013A-100AXC or CY7C68014A-100AXC	100-pin TQFP
CY7C68013-128AC	CY7C68013A-128AXC or CY7C68014A-128AXC	128-pin TQFP

## 2.20 CY7C68013A/14A and CY7C68015A/16A Differences

CY7C68013A is identical to CY7C68014A in form, fit, and functionality. CY7C68015A is identical to CY7C68016A in form, fit, and functionality. CY7C68014A and CY7C68016A have a lower suspend current than CY7C68013A and CY7C68015A respectively and are ideal for power sensitive battery applications.

CY7C68015A and CY7C68016A are available in 56-pin QFN package only. Two additional GPIO signals are available on the CY7C68015A and CY7C68016A to provide more flexibility when neither IFCLK or CLKOUT are needed in the 56-pin package.

USB developers wanting to convert their FX2 56-pin application to a bus-powered system directly benefit from these additional signals. The two GPIOs give developers the signals they need for the power control circuitry of their bus-powered application without pushing them to a high pincount version of FX2LP.

The CY7C68015A is only available in the 56-pin QFN package

**Table 9. CY7C68013A/14A and CY7C68015A/16A Pin Differences**

CY7C68013A/CY7C68014A	CY7C68015A/CY7C68016A
IFCLK	PE0
CLKOUT	PE1

**Note**

10. This EEPROM does not have address pins.

### 3. Pin Assignments

Figure 3-1 on page 16 identifies all signals for the five package types. The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 128-pin, 100-pin, and 56-pin packages.

The signals on the left edge of the 56-pin package in Figure 3-1 on page 16 are common to all versions in the FX2LP family with the noted differences between the CY7C68013A/14A and the CY7C68015A/16A.

Three modes are available in all package versions: Port, GPIF master, and Slave FIFO. These modes define the signals on the right edge of the diagram. The 8051 selects the interface mode using the IFCONFIG[1:0] register bits. Port mode is the power on default configuration.

The 100-pin package adds functionality to the 56-pin package by adding these pins:

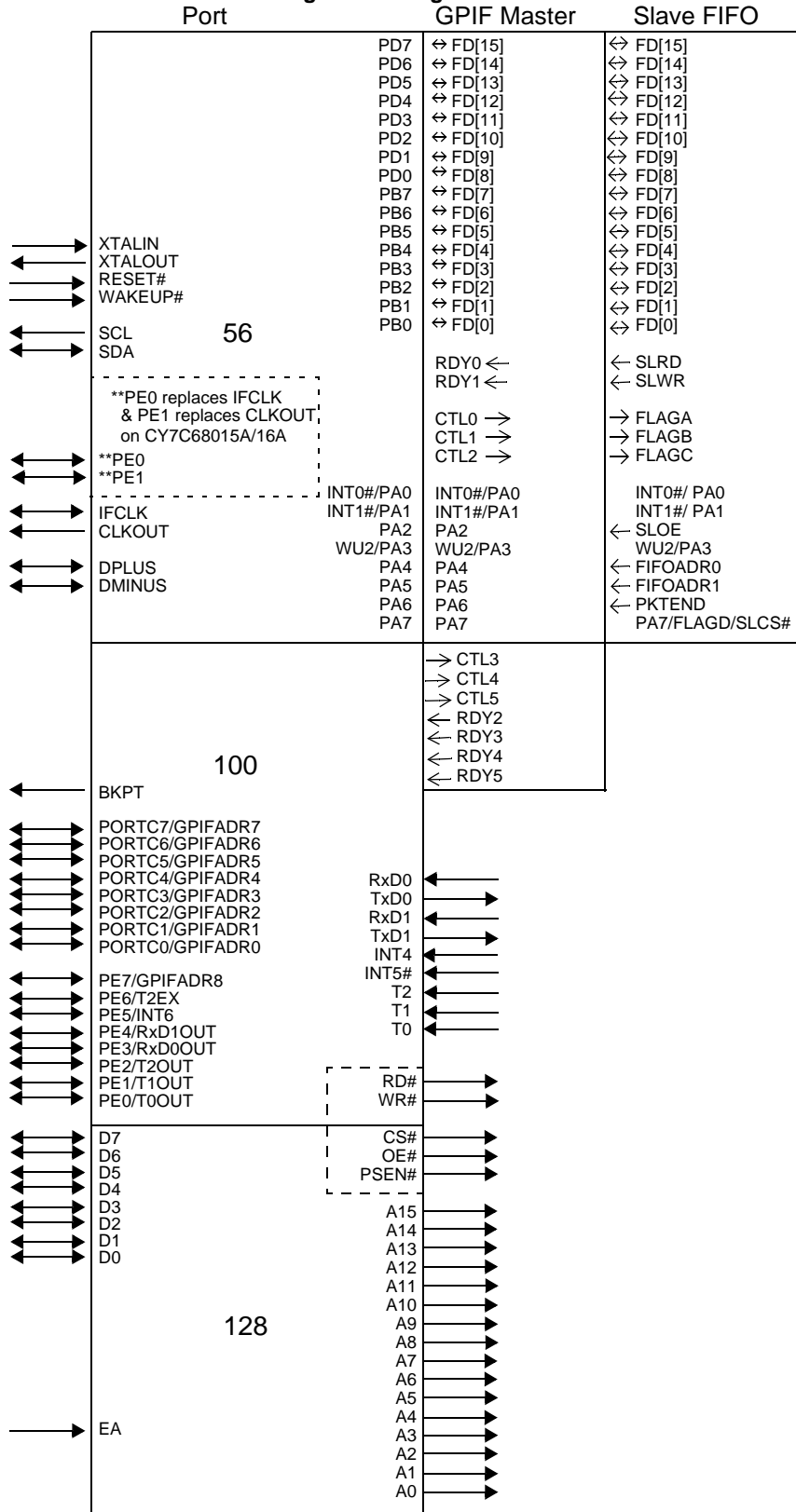
- PORTC or alternate GPIFADR[7:0] address signals
- PORTE or alternate GPIFADR[8] address signal and seven additional 8051 signals
- Three GPIF Control signals
- Four GPIF Ready signals
- Nine 8051 signals (two USARTs, three timer inputs, INT4, and INT5#)
- BKPT, RD#, WR#.

The 128-pin package adds the 8051 address and data buses plus control signals. Note that two of the required signals, RD# and WR#, are present in the 100-pin version.

In the 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from/writes to PORTC. This feature is enabled by setting PORTCSTB bit in CPUCS register.

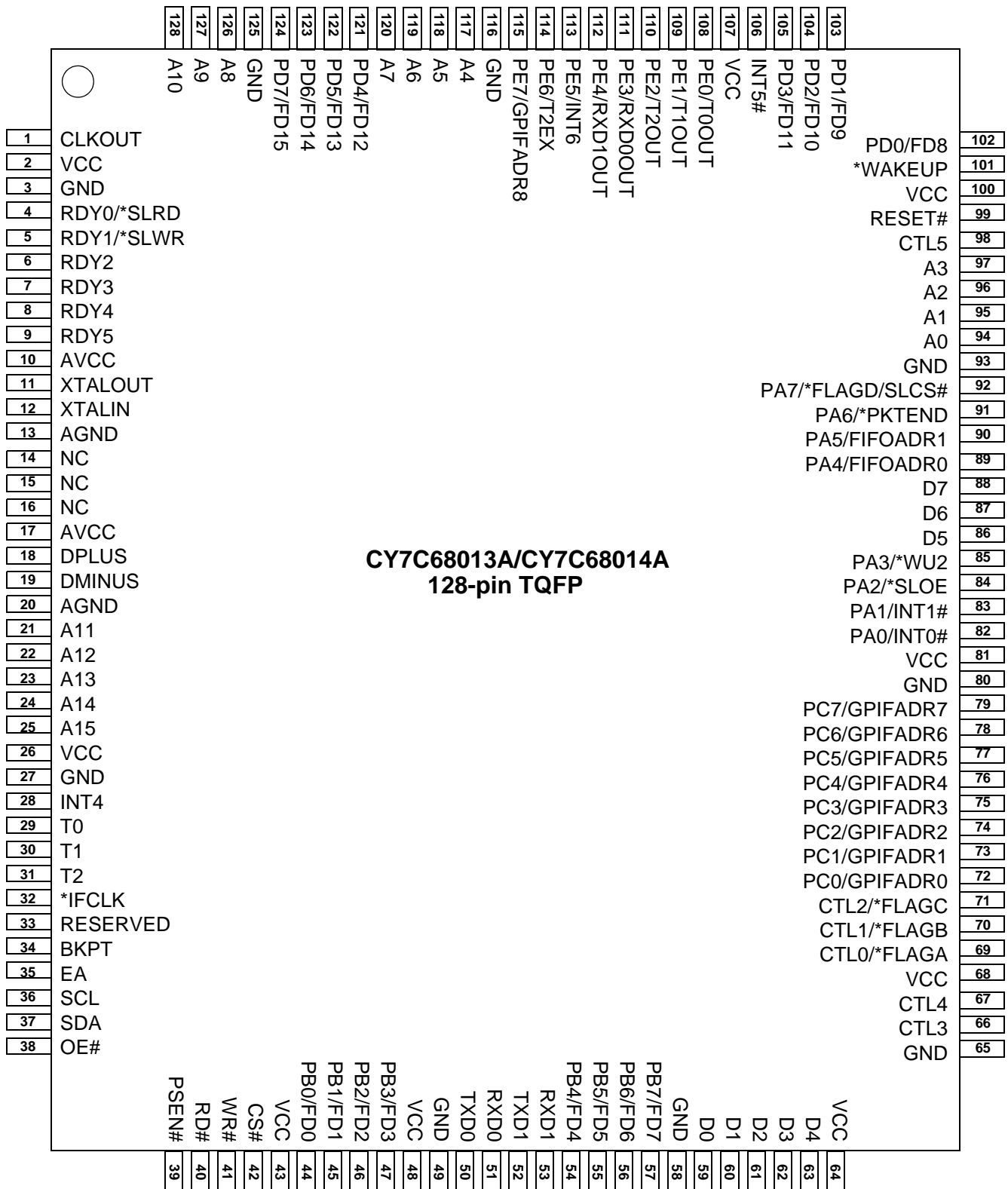
Section 9.5 displays the timing diagram of the read and write strobing function on accessing PORTC.

Figure 3-1. Signal





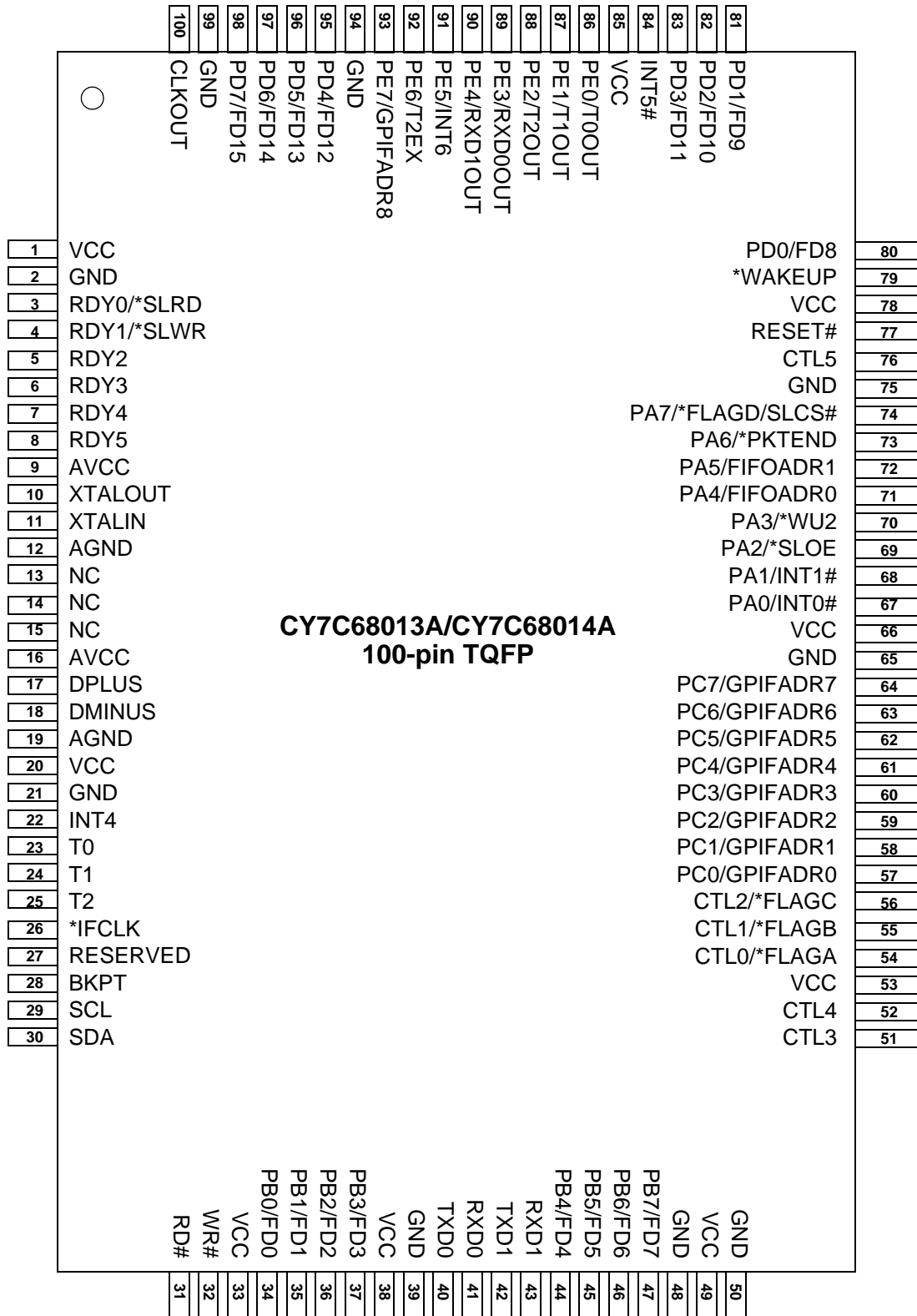
**Figure 3-2. CY7C68013A/CY7C68014A 128-Pin TQFP Pin Assignment**



**CY7C68013A/CY7C68014A  
128-pin TQFP**

\* denotes programmable polarity

**Figure 3-3. CY7C68013A/CY7C68014A 100-Pin TQFP Pin Assignment**



\* denotes programmable polarity

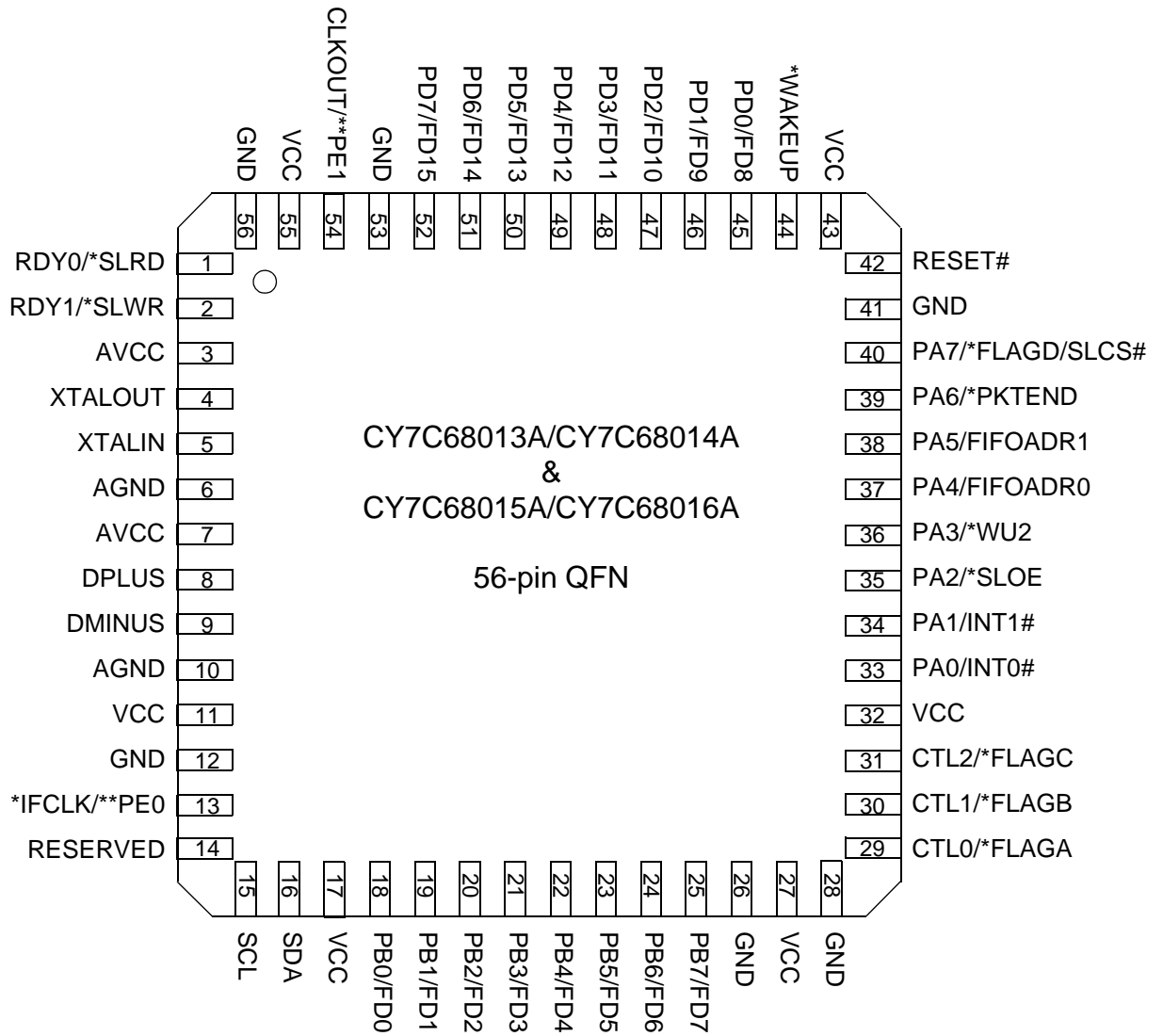
Figure 3-4. CY7C68013A/CY7C68014A 56-Pin SSOP Pin Assignment

**CY7C68013A/CY7C68014A  
56-pin SSOP**

1	PD5/FD13	PD4/FD12	56
2	PD6/FD14	PD3/FD11	55
3	PD7/FD15	PD2/FD10	54
4	GND	PD1/FD9	53
5	CLKOUT	PD0/FD8	52
6	VCC	*WAKEUP	51
7	GND	VCC	50
8	RDY0/*SLRD	RESET#	49
9	RDY1/*SLWR	GND	48
10	AVCC	PA7/*FLAGD/SLCS#	47
11	XTALOUT	PA6/PKTEND	46
12	XTALIN	PA5/FIFOADR1	45
13	AGND	PA4/FIFOADR0	44
14	AVCC	PA3/*WU2	43
15	DPLUS	PA2/*SLOE	42
16	DMINUS	PA1/INT1#	41
17	AGND	PA0/INT0#	40
18	VCC	VCC	39
19	GND	CTL2/*FLAGC	38
20	*IFCLK	CTL1/*FLAGB	37
21	RESERVED	CTL0/*FLAGA	36
22	SCL	GND	35
23	SDA	VCC	34
24	VCC	GND	33
25	PB0/FD0	PB7/FD7	32
26	PB1/FD1	PB6/FD6	31
27	PB2/FD2	PB5/FD5	30
28	PB3/FD3	PB4/FD4	29

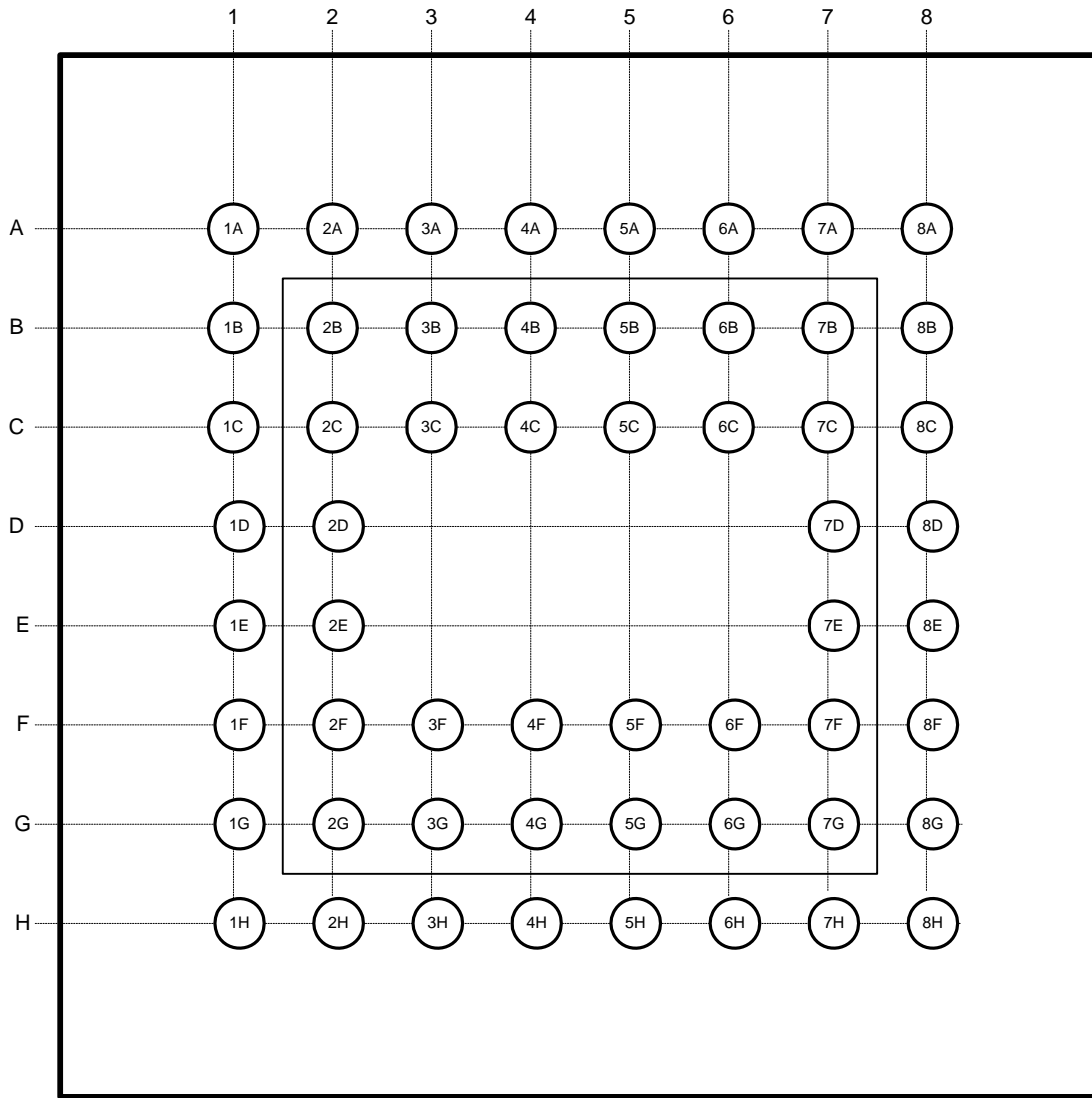
\* denotes programmable polarity

**Figure 3-5. CY7C68013A/14A/15A/16A 56-Pin QFN Pin Assignment**



\* denotes programmable polarity  
\*\* denotes CY7C68015A/CY7C68016A pinout

**Figure 3-6. CY7C68013A 56-pin VFBGA Pin Assignment – Top View**



### 3.1 CY7C68013A/15A Pin Descriptions

The FX2LP pin descriptions follow.<sup>[11]</sup>

**Table 10. FX2LP Pin Descriptions**

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
10	9	10	3	2D	AVCC	Power	N/A	<b>Analog VCC.</b> Connect this pin to 3.3V power source. This signal provides power to the analog section of the chip.
17	16	14	7	1D	AVCC	Power	N/A	<b>Analog VCC.</b> Connect this pin to 3.3V power source. This signal provides power to the analog section of the chip.
13	12	13	6	2F	AGND	Ground	N/A	<b>Analog Ground.</b> Connect to ground with as short a path as possible.
20	19	17	10	1F	AGND	Ground	N/A	<b>Analog Ground.</b> Connect to ground with as short a path as possible.
19	18	16	9	1E	DMINUS	I/O/Z	Z	<b>USB D- Signal.</b> Connect to the USB D- signal.
18	17	15	8	2E	DPLUS	I/O/Z	Z	<b>USB D+ Signal.</b> Connect to the USB D+ signal.
94	–	–	–	–	A0	Output	L	<b>8051 Address Bus.</b> This bus is driven at all times. When the 8051 is addressing internal RAM it reflects the internal address.
95	–	–	–	–	A1	Output	L	
96	–	–	–	–	A2	Output	L	
97	–	–	–	–	A3	Output	L	
117	–	–	–	–	A4	Output	L	
118	–	–	–	–	A5	Output	L	
119	–	–	–	–	A6	Output	L	
120	–	–	–	–	A7	Output	L	
126	–	–	–	–	A8	Output	L	
127	–	–	–	–	A9	Output	L	
128	–	–	–	–	A10	Output	L	
21	–	–	–	–	A11	Output	L	
22	–	–	–	–	A12	Output	L	
23	–	–	–	–	A13	Output	L	
24	–	–	–	–	A14	Output	L	
25	–	–	–	–	A15	Output	L	
59	–	–	–	–	D0	I/O/Z	Z	<b>8051 Data Bus.</b> This bidirectional bus is high impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is active only for external bus accesses, and is driven LOW in suspend.
60	–	–	–	–	D1	I/O/Z	Z	
61	–	–	–	–	D2	I/O/Z	Z	
62	–	–	–	–	D3	I/O/Z	Z	
63	–	–	–	–	D4	I/O/Z	Z	
86	–	–	–	–	D5	I/O/Z	Z	
87	–	–	–	–	D6	I/O/Z	Z	
88	–	–	–	–	D7	I/O/Z	Z	
39	–	–	–	–	PSEN#	Output	H	<b>Program Store Enable.</b> This active-LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x4000–0xFFFF when the EA pin is LOW, or from 0x0000–0xFFFF when the EA pin is HIGH.

**Note**

11. Unused inputs must not be left floating. Tie either HIGH or LOW as appropriate. Outputs should only be pulled up or down to ensure signals at power up and in standby. Note also that no pins should be driven while the device is powered down.

**Table 10. FX2LP Pin Descriptions (continued)**

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
34	28	–	–		BKPT	Output	L	<b>Breakpoint.</b> This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48 MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register.
99	77	49	42	8B	RESET#	Input	N/A	<b>Active LOW Reset.</b> Resets the entire chip. See section 2.9 "Reset and Wakeup" on page 8 for more details.
35	–	–	–	–	EA	Input	N/A	<b>External Access.</b> This pin determines where the 8051 fetches code between addresses 0x0000 and 0x3FFF. If EA = 0 the 8051 fetches this code from its internal RAM. If EA = 1 the 8051 fetches this code from external memory.
12	11	12	5	1C	XTALIN	Input	N/A	<b>Crystal Input.</b> Connect this signal to a 24 MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. It is also correct to drive XTALIN with an external 24-MHz square wave derived from another clock source. When driving from an external source, the driving signal should be a 3.3V square wave.
11	10	11	4	2C	XTALOUT	Output	N/A	<b>Crystal Output.</b> Connect this signal to a 24 MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
1	100	5	54	2B	CLKOUT on CY7C68013A and CY7C68014A	O/Z	12 MHz	<b>CLKOUT:</b> 12-, 24- or 48 MHz clock, phase locked to the 24 MHz input clock. The 8051 defaults to 12 MHz operation. The 8051 may three-state this output by setting CPUCS.1 = 1.
					PE1 on CY7C68015A and CY7C68016A	I/O/Z	I	<b>PE1</b> is a bidirectional I/O port pin.
<b>Port A</b>								
82	67	40	33	8G	PA0 or INT0#	I/O/Z	I (PA0)	Multiplexed pin whose function is selected by PORTACFG.0 <b>PA0</b> is a bidirectional I/O port pin. <b>INT0#</b> is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
83	68	41	34	6G	PA1 or INT1#	I/O/Z	I (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 <b>PA1</b> is a bidirectional I/O port pin. <b>INT1#</b> is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0).
84	69	42	35	8F	PA2 or SLOE or	I/O/Z	I (PA2)	Multiplexed pin whose function is selected by two bits: IFCONFIG[1:0]. <b>PA2</b> is a bidirectional I/O port pin. <b>SLOE</b> is an input-only output enable with programmable polarity (FIFOPINPOLAR.4) for the slave FIFOs connected to FD[7..0] or FD[15..0].

**Table 10. FX2LP Pin Descriptions (continued)**

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
85	70	43	36	7F	PA3 or WU2	I/O/Z	I (PA3)	Multiplexed pin whose function is selected by: WAKEUP.7 and OEA.3 <b>PA3</b> is a bidirectional I/O port pin. <b>WU2</b> is an alternate source for <b>USB Wakeup</b> , enabled by WU2EN bit (WAKEUP.1) and polarity set by WU2POL (WAKEUP.4). If the 8051 is in suspend and WU2EN = 1, a transition on this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Asserting this pin inhibits the chip from suspending, if WU2EN = 1.
89	71	44	37	6F	PA4 or FIFOADR0	I/O/Z	I (PA4)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. <b>PA4</b> is a bidirectional I/O port pin. <b>FIFOADR0</b> is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
90	72	45	38	8C	PA5 or FIFOADR1	I/O/Z	I (PA5)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. <b>PA5</b> is a bidirectional I/O port pin. <b>FIFOADR1</b> is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
91	73	46	39	7C	PA6 or PKTEND	I/O/Z	I (PA6)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. <b>PA6</b> is a bidirectional I/O port pin. <b>PKTEND</b> is an input used to commit the FIFO packet data to the endpoint and whose polarity is programmable via FIFOPINPOLAR.5.
92	74	47	40	6C	PA7 or FLAGD or SLCS#	I/O/Z	I (PA7)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. <b>PA7</b> is a bidirectional I/O port pin. <b>FLAGD</b> is a programmable slave-FIFO output status flag signal. <b>SLCS#</b> gates all other slave FIFO enable/strobes
<b>Port B</b>								
44	34	25	18	3H	PB0 or FD[0]	I/O/Z	I (PB0)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB0</b> is a bidirectional I/O port pin. <b>FD[0]</b> is the bidirectional FIFO/GPIF data bus.
45	35	26	19	4F	PB1 or FD[1]	I/O/Z	I (PB1)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB1</b> is a bidirectional I/O port pin. <b>FD[1]</b> is the bidirectional FIFO/GPIF data bus.
46	36	27	20	4H	PB2 or FD[2]	I/O/Z	I (PB2)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB2</b> is a bidirectional I/O port pin. <b>FD[2]</b> is the bidirectional FIFO/GPIF data bus.
47	37	28	21	4G	PB3 or FD[3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB3</b> is a bidirectional I/O port pin. <b>FD[3]</b> is the bidirectional FIFO/GPIF data bus.
54	44	29	22	5H	PB4 or FD[4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB4</b> is a bidirectional I/O port pin. <b>FD[4]</b> is the bidirectional FIFO/GPIF data bus.



**Table 10. FX2LP Pin Descriptions (continued)**

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
55	45	30	23	5G	PB5 or FD[5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB5</b> is a bidirectional I/O port pin. <b>FD[5]</b> is the bidirectional FIFO/GPIF data bus.
56	46	31	24	5F	PB6 or FD[6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB6</b> is a bidirectional I/O port pin. <b>FD[6]</b> is the bidirectional FIFO/GPIF data bus.
57	47	32	25	6H	PB7 or FD[7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>PB7</b> is a bidirectional I/O port pin. <b>FD[7]</b> is the bidirectional FIFO/GPIF data bus.
<b>PORT C</b>								
72	57	–	–	–	PC0 or GPIFADR0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by PORTCCFG.0 <b>PC0</b> is a bidirectional I/O port pin. <b>GPIFADR0</b> is a GPIF address output pin.
73	58	–	–	–	PC1 or GPIFADR1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by PORTCCFG.1 <b>PC1</b> is a bidirectional I/O port pin. <b>GPIFADR1</b> is a GPIF address output pin.
74	59	–	–	–	PC2 or GPIFADR2	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by PORTCCFG.2 <b>PC2</b> is a bidirectional I/O port pin. <b>GPIFADR2</b> is a GPIF address output pin.
75	60	–	–	–	PC3 or GPIFADR3	I/O/Z	I (PC3)	Multiplexed pin whose function is selected by PORTCCFG.3 <b>PC3</b> is a bidirectional I/O port pin. <b>GPIFADR3</b> is a GPIF address output pin.
76	61	–	–	–	PC4 or GPIFADR4	I/O/Z	I (PC4)	Multiplexed pin whose function is selected by PORTCCFG.4 <b>PC4</b> is a bidirectional I/O port pin. <b>GPIFADR4</b> is a GPIF address output pin.
77	62	–	–	–	PC5 or GPIFADR5	I/O/Z	I (PC5)	Multiplexed pin whose function is selected by PORTCCFG.5 <b>PC5</b> is a bidirectional I/O port pin. <b>GPIFADR5</b> is a GPIF address output pin.
78	63	–	–	–	PC6 or GPIFADR6	I/O/Z	I (PC6)	Multiplexed pin whose function is selected by PORTCCFG.6 <b>PC6</b> is a bidirectional I/O port pin. <b>GPIFADR6</b> is a GPIF address output pin.
79	64	–	–	–	PC7 or GPIFADR7	I/O/Z	I (PC7)	Multiplexed pin whose function is selected by PORTCCFG.7 <b>PC7</b> is a bidirectional I/O port pin. <b>GPIFADR7</b> is a GPIF address output pin.
<b>PORT D</b>								
102	80	52	45	8A	PD0 or FD[8]	I/O/Z	I (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[8]</b> is the bidirectional FIFO/GPIF data bus.
103	81	53	46	7A	PD1 or FD[9]	I/O/Z	I (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[9]</b> is the bidirectional FIFO/GPIF data bus.

**Table 10. FX2LP Pin Descriptions** (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
104	82	54	47	6B	PD2 or FD[10]	I/O/Z	I (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[10]</b> is the bidirectional FIFO/GPIF data bus.
105	83	55	48	6A	PD3 or FD[11]	I/O/Z	I (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[11]</b> is the bidirectional FIFO/GPIF data bus.
121	95	56	49	3B	PD4 or FD[12]	I/O/Z	I (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[12]</b> is the bidirectional FIFO/GPIF data bus.
122	96	1	50	3A	PD5 or FD[13]	I/O/Z	I (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[13]</b> is the bidirectional FIFO/GPIF data bus.
123	97	2	51	3C	PD6 or FD[14]	I/O/Z	I (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[14]</b> is the bidirectional FIFO/GPIF data bus.
124	98	3	52	2A	PD7 or FD[15]	I/O/Z	I (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. <b>FD[15]</b> is the bidirectional FIFO/GPIF data bus.
<b>Port E</b>								
108	86	–	–	–	PE0 or T0OUT	I/O/Z	I (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. <b>PE0</b> is a bidirectional I/O port pin. <b>T0OUT</b> is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87	–	–	–	PE1 or T1OUT	I/O/Z	I (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. <b>PE1</b> is a bidirectional I/O port pin. <b>T1OUT</b> is an active-HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.
110	88	–	–	–	PE2 or T2OUT	I/O/Z	I (PE2)	Multiplexed pin whose function is selected by the PORTECFG.2 bit. <b>PE2</b> is a bidirectional I/O port pin. <b>T2OUT</b> is the active-HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows.
111	89	–	–	–	PE3 or RXD0OUT	I/O/Z	I (PE3)	Multiplexed pin whose function is selected by the PORTECFG.3 bit. <b>PE3</b> is a bidirectional I/O port pin. <b>RXD0OUT</b> is an active-HIGH signal from 8051 UART0. If RXD0OUT is selected and UART0 is in Mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1.

**Table 10. FX2LP Pin Descriptions** (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
112	90	–	–	–	PE4 or RXD1OUT	I/O/Z	I (PE4)	Multiplexed pin whose function is selected by the PORTECFG.4 bit. <b>PE4</b> is a bidirectional I/O port pin. <b>RXD1OUT</b> is an active-HIGH output from 8051 UART1. When RXD1OUT is selected and UART1 is in Mode 0, this pin provides the output data for UART1 only when it is in sync mode. In Modes 1, 2, and 3, this pin is HIGH.
113	91	–	–	–	PE5 or INT6	I/O/Z	I (PE5)	Multiplexed pin whose function is selected by the PORTECFG.5 bit. <b>PE5</b> is a bidirectional I/O port pin. <b>INT6</b> is the 8051 INT6 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH.
114	92	–	–	–	PE6 or T2EX	I/O/Z	I (PE6)	Multiplexed pin whose function is selected by the PORTECFG.6 bit. <b>PE6</b> is a bidirectional I/O port pin. <b>T2EX</b> is an active-HIGH input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON.
115	93	–	–	–	PE7 or GPIFADR8	I/O/Z	I (PE7)	Multiplexed pin whose function is selected by the PORTECFG.7 bit. <b>PE7</b> is a bidirectional I/O port pin. <b>GPIFADR8</b> is a GPIF address output pin.
4	3	8	1	1A	RDY0 or SLRD	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>RDY0</b> is a GPIF input signal. <b>SLRD</b> is the input-only read strobe with programmable polarity (FIFOPINPOLAR.3) for the slave FIFOs connected to FD[7..0] or FD[15..0].
5	4	9	2	1B	RDY1 or SLWR	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>RDY1</b> is a GPIF input signal. <b>SLWR</b> is the input-only write strobe with programmable polarity (FIFOPINPOLAR.2) for the slave FIFOs connected to FD[7..0] or FD[15..0].
6	5	–	–	–	RDY2	Input	N/A	<b>RDY2</b> is a GPIF input signal.
7	6	–	–	–	RDY3	Input	N/A	<b>RDY3</b> is a GPIF input signal.
8	7	–	–	–	RDY4	Input	N/A	<b>RDY4</b> is a GPIF input signal.
9	8	–	–	–	RDY5	Input	N/A	<b>RDY5</b> is a GPIF input signal.
69	54	36	29	7H	CTL0 or FLAGA	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>CTL0</b> is a GPIF control output. <b>FLAGA</b> is a programmable slave-FIFO output status flag signal. Defaults to programmable for the FIFO selected by the FIFOADR[1:0] pins.

**Table 10. FX2LP Pin Descriptions (continued)**

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
70	55	37	30	7G	CTL1 or FLAGB	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>CTL1</b> is a GPIF control output. <b>FLAGB</b> is a programmable slave-FIFO output status flag signal. Defaults to FULL for the FIFO selected by the FIFOADR[1:0] pins.
71	56	38	31	8H	CTL2 or FLAGC	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. <b>CTL2</b> is a GPIF control output. <b>FLAGC</b> is a programmable slave-FIFO output status flag signal. Defaults to EMPTY for the FIFO selected by the FIFOADR[1:0] pins.
66	51	–	–	–	CTL3	O/Z	H	<b>CTL3</b> is a GPIF control output.
67	52	–	–	–	CTL4	Output	H	<b>CTL4</b> is a GPIF control output.
98	76	–	–	–	CTL5	Output	H	<b>CTL5</b> is a GPIF control output.
32	26	20	13	2G	IFCLK on CY7C68013A and CY7C68014A	I/O/Z	Z	Interface Clock, used for synchronously clocking data into or out of the slave FIFOs. IFCLK also serves as a timing reference for all slave FIFO control signals and GPIF. When internal clocking is used (IFCONFIG.7 = 1) the IFCLK pin can be configured to output 30/48 MHz by bits IFCONFIG.5 and IFCONFIG.6. IFCLK may be inverted, whether internally or externally sourced, by setting the bit IFCONFIG.4 = 1.
					PE0 on CY7C68015A and CY7C68016A	I/O/Z	I	<b>PE0</b> is a bidirectional I/O port pin.
28	22	–	–	–	INT4	Input	N/A	<b>INT4</b> is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH.
106	84	–	–	–	INT5#	Input	N/A	<b>INT5#</b> is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW.
31	25	–	–	–	T2	Input	N/A	<b>T2</b> is the active-HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2 = 1. When C/T2 = 0, Timer2 does not use this pin.
30	24	–	–	–	T1	Input	N/A	<b>T1</b> is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit.
29	23	–	–	–	T0	Input	N/A	<b>T0</b> is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit.
53	43	–	–	–	RXD1	Input	N/A	<b>RXD1</b> is an active-HIGH input signal for 8051 UART1, which provides data to the UART in all modes.
52	42	–	–	–	TXD1	Output	H	<b>TXD1</b> is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode.
51	41	–	–	–	RXD0	Input	N/A	<b>RXD0</b> is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes.

**Table 10. FX2LP Pin Descriptions (continued)**

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Description
50	40	–	–	–	TXD0	Output	H	<b>TXD0</b> is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode.
42		–	–	–	CS#	Output	H	<b>CS#</b> is the active-LOW chip select for external memory.
41	32	–	–	–	WR#	Output	H	<b>WR#</b> is the active-LOW write strobe output for external memory.
40	31	–	–	–	RD#	Output	H	<b>RD#</b> is the active-LOW read strobe output for external memory.
38		–	–	–	OE#	Output	H	<b>OE#</b> is the active-LOW output enable for external memory.
33	27	21	14	2H	Reserved	Input	N/A	<b>Reserved.</b> Connect to ground.
101	79	51	44	7B	WAKEUP	Input	N/A	<b>USB Wakeup.</b> If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB <sup>®</sup> chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	15	3F	SCL	OD	Z	<b>Clock</b> for the I <sup>2</sup> C interface. Connect to VCC with a 2.2K resistor, even if no I <sup>2</sup> C peripheral is attached.
37	30	23	16	3G	SDA	OD	Z	<b>Data for I<sup>2</sup>C compatible interface.</b> Connect to VCC with a 2.2K resistor, <b>even if no I<sup>2</sup>C compatible peripheral is attached.</b>
2	1	6	55	5A	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
26	20	18	11	1G	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
43	33	24	17	7E	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
48	38	–	–	–	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
64	49	34	27	8E	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
68	53	–	–	–	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
81	66	39	32	5C	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
100	78	50	43	5B	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
107	85	–	–	–	VCC	Power	N/A	<b>VCC.</b> Connect to 3.3 V power source.
3	2	7	56	4B	GND	Ground	N/A	<b>Ground.</b>
27	21	19	12	1H	GND	Ground	N/A	<b>Ground.</b>
49	39	–	–	–	GND	Ground	N/A	<b>Ground.</b>
58	48	33	26	7D	GND	Ground	N/A	<b>Ground.</b>
65	50	35	28	8D	GND	Ground	N/A	<b>Ground.</b>
80	65	–	–	–	GND	Ground	N/A	<b>Ground.</b>
93	75	48	41	4C	GND	Ground	N/A	<b>Ground.</b>
116	94	–	–	–	GND	Ground	N/A	<b>Ground.</b>
125	99	4	53	4A	GND	Ground	N/A	<b>Ground.</b>
14	13	–	–	–	NC	N/A	N/A	<b>No Connect.</b> This pin must be left open.
15	14	–	–	–	NC	N/A	N/A	<b>No Connect.</b> This pin must be left open.
16	15	–	–	–	NC	N/A	N/A	<b>No Connect.</b> This pin must be left open.















**Table 11. FX2LP Register Summary (continued)**

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
BE	1	GPIFSGLDATLX <sup>[14]</sup>	GPIF Data L w/ Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
BF	1	GPIFSGLDATL-NOX <sup>[14]</sup>	GPIF Data L w/ No Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
C0	1	SCON1 <sup>[14]</sup>	Serial Port 1 Control (bit addressable)	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00000000	RW
C1	1	SBUF1 <sup>[14]</sup>	Serial Port 1 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
C2	6	reserved											
C8	1	T2CON	Timer/Counter 2 Control (bit addressable)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00000000	RW
C9	1	reserved											
CA	1	RCAP2L	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CB	1	RCAP2H	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CC	1	TL2	Timer 2 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CD	1	TH2	Timer 2 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
CE	2	reserved											
D0	1	PSW	Program Status Word (bit addressable)	CY	AC	F0	RS1	RS0	OV	F1	P	00000000	RW
D1	7	reserved											
D8	1	EICON <sup>[14]</sup>	External Interrupt Control	SMOD1	1	ERESI	RESI	INT6	0	0	0	01000000	RW
D9	7	reserved											
E0	1	ACC	Accumulator (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
E1	7	reserved											
E8	1	EIE <sup>[14]</sup>	External Interrupt Enable(s)	1	1	1	EX6	EX5	EX4	EIPC	EUSB	11100000	RW
E9	7	reserved											
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
F1	7	reserved											
F8	1	EIP <sup>[14]</sup>	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	PIPC	PUSB	11100000	RW
F9	7	reserved											

R = all bits read-only  
W = all bits write-only  
r = read-only bit  
w = write-only bit  
b = both read/write bit

## 5. Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power supplied (commercial).....	0 °C to +70 °C
Ambient temperature with power supplied (industrial).....	-40 °C to + 105 °C
Supply voltage to ground potential .....	-0.5 V to +4.0 V
DC input voltage to any input pin <sup>[16]</sup> .....	5.25 V
DC voltage applied to outputs in high Z state .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Power dissipation .....	300 mW
Static discharge voltage.....	>2000 V
Max output current, per I/O port .....	10 mA
Max output current, all five I/O ports (128-pin and 100-pin packages).....	50 mA

## 7. Thermal Characteristics

The following table displays the thermal characteristics of various packages:

**Table 12. Thermal Characteristics**

Package	Ambient Temperature (°C)	$\theta_{Jc}$ Junction to Case Thermal Resistance (°C/W)	$\theta_{Ja}$ Junction to Ambient Thermal Resistance (°C/W)
56 SSOP	70	24.4	47.7
100 TQFP	70	11.9	45.9
128 TQFP	70	15.5	43.2
56 QFN	70	10.6	25.2
56 VFBGA	70	30.9	58.6

The junction temperature  $\theta_j$ , can be calculated using the following equation:  $\theta_j = P \cdot \theta_{Ja} + \theta_a$

Where,

P = Power

$\theta_{Ja}$  = Junction to ambient temperature ( $\theta_{Jc} + \theta_{Ca}$ )

$\theta_a$  = Ambient temperature (70 °C)

The case temperature  $\theta_c$ , can be calculated using the following equation:  $\theta_c = P \cdot \theta_{Ca} + \theta_a$

where,

P = Power

$\theta_{Ca}$  = Case to ambient temperature

$\theta_a$  = Ambient temperature (70 °C)

**Note**

16. Do not power I/O with chip power off.

## 6. Operating Conditions

T <sub>A</sub> (ambient temperature under bias)	Commercial .....	0 °C to +70 °C
T <sub>A</sub> (ambient temperature under bias)	Industrial .....	-40 °C to +105 °C
Supply voltage .....		+3.00 V to +3.60 V
Ground voltage .....		0 V
F <sub>OSC</sub> (oscillator or crystal frequency) .....		24 MHz ± 100 ppm, parallel resonant

## 8. DC Characteristics

Table 13. DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
VCC	Supply voltage	–	3.00	3.3	3.60	V
VCC Ramp Up	0 to 3.3 V	–	200	–	–	μs
V <sub>IH</sub>	Input HIGH voltage	–	2	–	5.25	V
V <sub>IL</sub>	Input LOW voltage	–	–0.5	–	0.8	V
V <sub>IH_X</sub>	Crystal input HIGH voltage	–	2	–	5.25	V
V <sub>IL_X</sub>	Crystal input LOW voltage	–	–0.5	–	0.8	V
I <sub>I</sub>	Input leakage current	0 < V <sub>IN</sub> < VCC	–	–	±10	μA
V <sub>OH</sub>	Output voltage HIGH	I <sub>OUT</sub> = 4 mA	2.4	–	–	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OUT</sub> = –4 mA	–	–	0.4	V
I <sub>OH</sub>	Output current HIGH	–	–	–	4	mA
I <sub>OL</sub>	Output current LOW	–	–	–	4	mA
C <sub>IN</sub>	Input pin capacitance	Except D+/D–	–	–	10	pF
		D+/D–	–	–	15	pF
I <sub>SUSP</sub>	Suspend current CY7C68014/CY7C68016	Connected	–	300	380 <sup>[17]</sup>	μA
		Disconnected	–	100	150 <sup>[17]</sup>	μA
	Suspend current CY7C68013/CY7C68015	Connected	–	0.5	1.2 <sup>[17]</sup>	mA
		Disconnected	–	0.3	1.0 <sup>[17]</sup>	mA
I <sub>CC</sub>	Supply current	8051 running, connected to USB HS	–	50	85	mA
		8051 running, connected to USB FS	–	35	65	mA
T <sub>RESET</sub>	Reset time after valid power	V <sub>CC</sub> min = 3.0 V	5.0	–	–	mS
	Pin reset after powered on		200	–	–	μS

### 8.1 USB Transceiver

USB 2.0 compliant in full speed and high speed modes.

**Note**

17. Measured at Max VCC, 25 °C.

## 9. AC Electrical Characteristics

### 9.1 USB Transceiver

USB 2.0 compliant in full speed and high speed modes.

### 9.2 Program Memory Read

Figure 9-1. Program Memory Read Timing Diagram

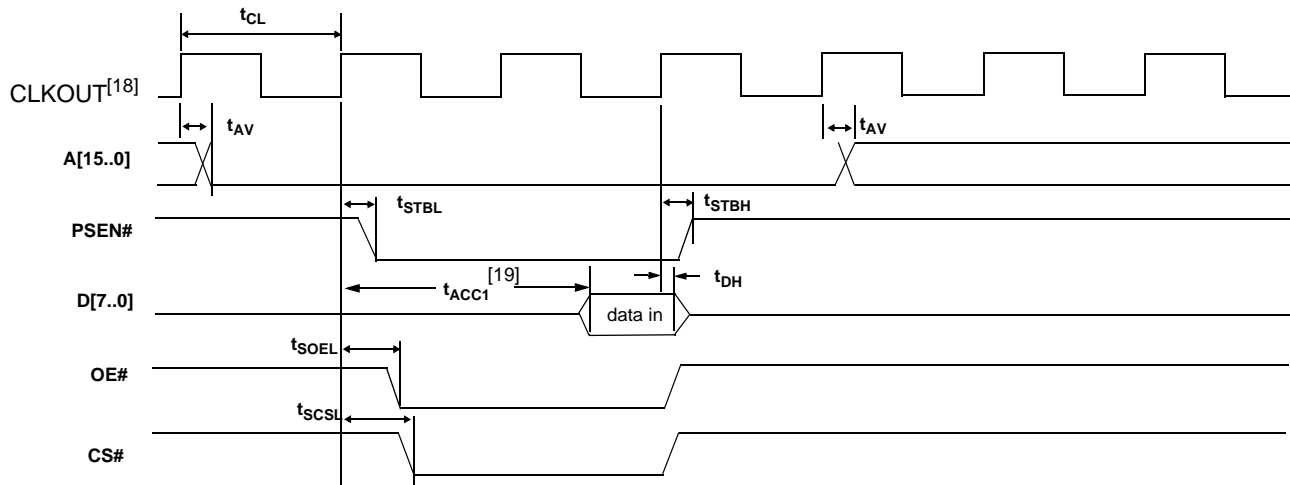


Table 14. Program Memory Read Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$t_{CL}$	1/CLKOUT Frequency	–	20.83	–	ns	48 MHz
		–	41.66	–	ns	24 MHz
		–	83.2	–	ns	12 MHz
$t_{AV}$	Delay from Clock to Valid Address	0	–	10.7	ns	–
$t_{STBL}$	Clock to PSEN Low	0	–	8	ns	–
$t_{STBH}$	Clock to PSEN High	0	–	8	ns	–
$t_{SOEL}$	Clock to OE Low	–	–	11.1	ns	–
$t_{SCSL}$	Clock to CS Low	–	–	13	ns	–
$t_{DSU}$	Data Setup to Clock	9.6	–	–	ns	–
$t_{DH}$	Data Hold Time	0	–	–	ns	–

#### Notes

18. CLKOUT is shown with positive polarity.  
 19.  $t_{ACC1}$  is computed from these parameters as follows:  
 $t_{ACC1}(24\text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 106\text{ ns}$ .  
 $t_{ACC1}(48\text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 43\text{ ns}$ .

### 9.3 Data Memory Read

Figure 9-2. Data Memory Read Timing Diagram

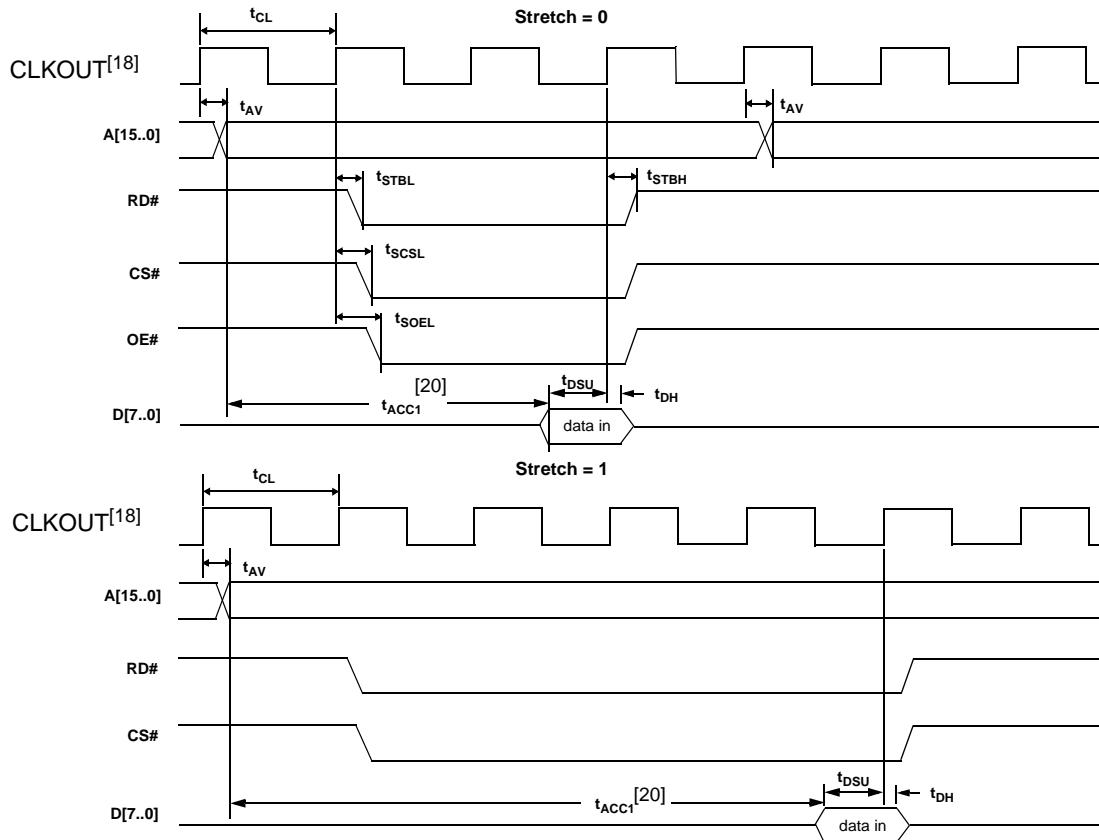


Table 15. Data Memory Read Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$t_{CL}$	1/CLKOUT frequency	–	20.83	–	ns	48 MHz
		–	41.66	–	ns	24 MHz
		–	83.2	–	ns	12 MHz
$t_{AV}$	Delay from clock to valid address	–	–	10.7	ns	–
$t_{STBL}$	Clock to RD LOW	–	–	11	ns	–
$t_{STBH}$	Clock to RD HIGH	–	–	11	ns	–
$t_{SCSL}$	Clock to CS LOW	–	–	13	ns	–
$t_{SOEL}$	Clock to OE LOW	–	–	11.1	ns	–
$t_{DSU}$	Data setup to clock	9.6	–	–	ns	–
$t_{DH}$	Data hold time	0	–	–	ns	–

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value

**Note**

20.  $t_{ACC2}$  and  $t_{ACC3}$  are computed from these parameters as follows:  
 $t_{ACC2}(24\text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 106\text{ ns.}$   
 $t_{ACC2}(48\text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 43\text{ ns.}$   
 $t_{ACC3}(24\text{ MHz}) = 5 \cdot t_{CL} - t_{AV} - t_{DSU} = 190\text{ ns.}$   
 $t_{ACC3}(48\text{ MHz}) = 5 \cdot t_{CL} - t_{AV} - t_{DSU} = 86\text{ ns.}$



### 9.4 Data Memory Write

Figure 9-3. Data Memory Write Timing Diagram

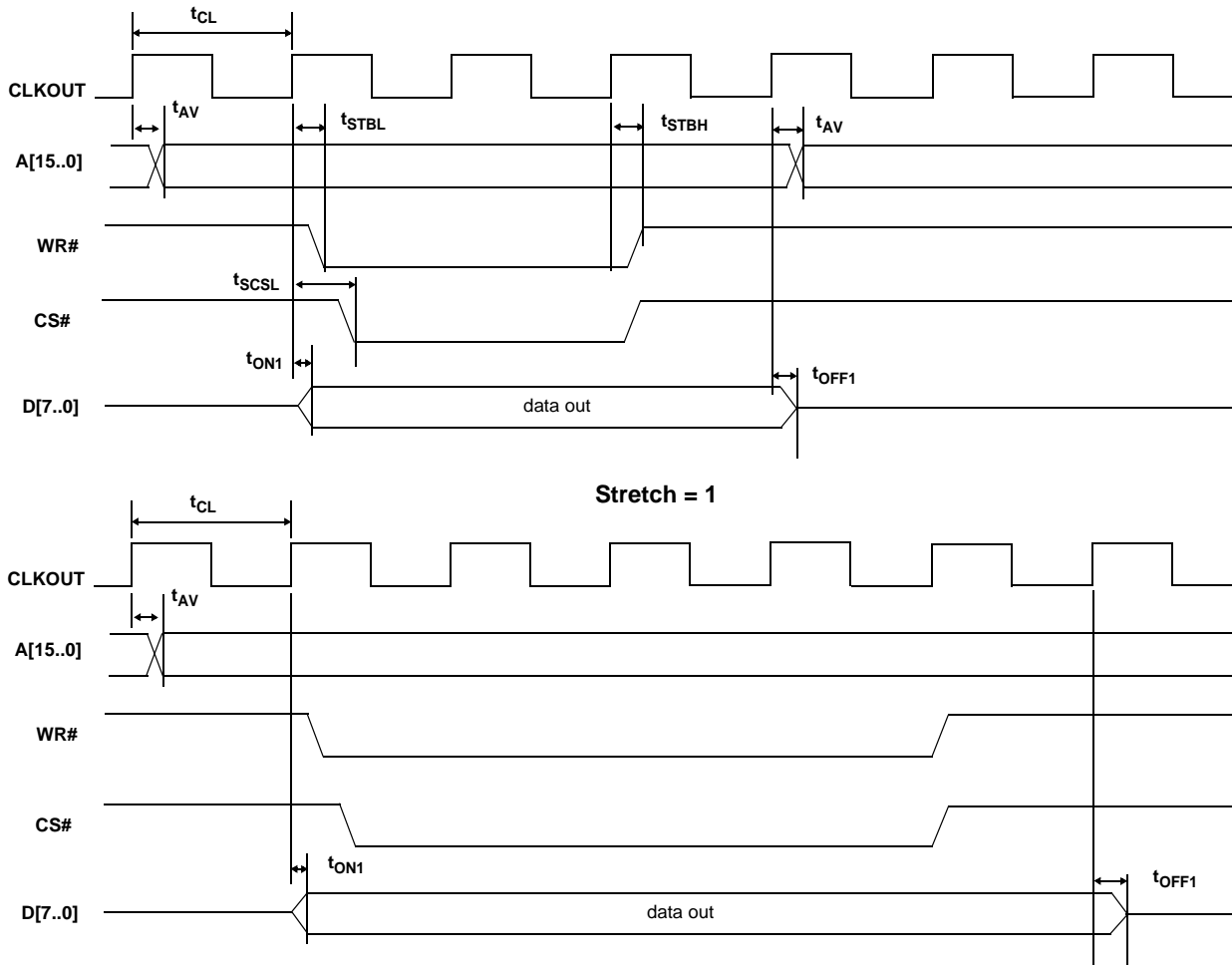


Table 16. Data Memory Write Parameters

Parameter	Description	Min	Max	Unit	Notes
$t_{AV}$	Delay from clock to valid address	0	10.7	ns	–
$t_{STBL}$	Clock to WR pulse LOW	0	11.2	ns	–
$t_{STBH}$	Clock to WR pulse HIGH	0	11.2	ns	–
$t_{SCSL}$	Clock to CS pulse LOW	–	13.0	ns	–
$t_{ON1}$	Clock to data turn-on	0	13.1	ns	–
$t_{OFF1}$	Clock to data hold time	0	13.1	ns	–

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

### 9.5 PORTC Strobe Feature Timings

The RD# and WR# are present in the 100-pin version and the 128-pin package. In these 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from or writes to PORTC. This feature is enabled by setting PORTCSTB bit in CPUCS register.

The RD# and WR# strobes are asserted for two CLKOUT cycles when PORTC is accessed.

The WR# strobe is asserted two clock cycles after PORTC is updated and is active for two clock cycles after that, as shown in Figure 9-4.

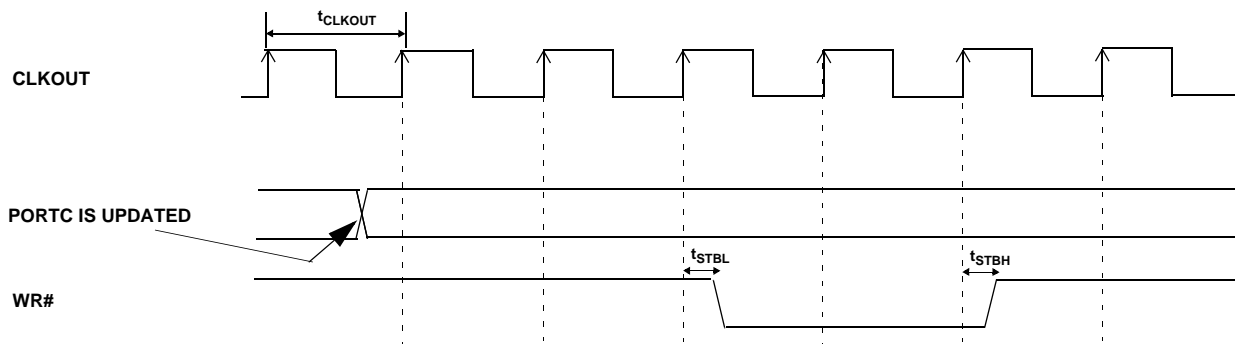
As for read, the value of PORTC three clock cycles before the assertion of RD# is the value that the 8051 reads in. The RD# is pulsed for 2 clock cycles after 3 clock cycles from the point when the 8051 has performed a read function on PORTC.

The RD# signal prompts the external logic to prepare the next data byte. Nothing gets sampled internally on assertion of the RD# signal itself, it is just a prefetch type signal to get the next data byte prepared. So, using it with that in mind easily meets the setup time to the next read.

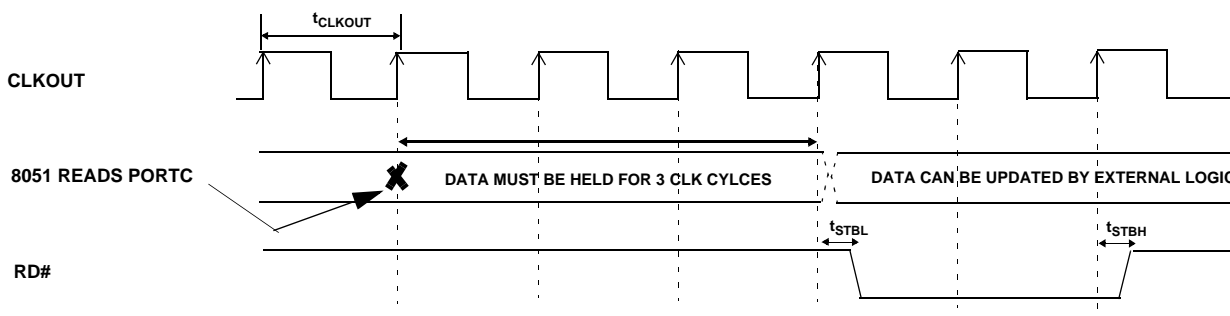
The purpose of this pulsing of RD# is to allow the external peripheral to know that the 8051 is done reading PORTC and the data was latched into PORTC three CLKOUT cycles before asserting the RD# signal. After the RD# is pulsed, the external logic can update the data on PORTC.

Following is the timing diagram of the read and write strobing function on accessing PORTC. Refer to Section 9.3 and Section 9.4 for details on propagation delay of RD# and WR# signals.

**Figure 9-4. WR# Strobe Function when PORTC is Accessed by 8051**



**Figure 9-5. RD# Strobe Function when PORTC is Accessed by 8051**



## 9.6 GPIF Synchronous Signals

Figure 9-6. GPIF Synchronous Signals Timing Diagram<sup>[21]</sup>

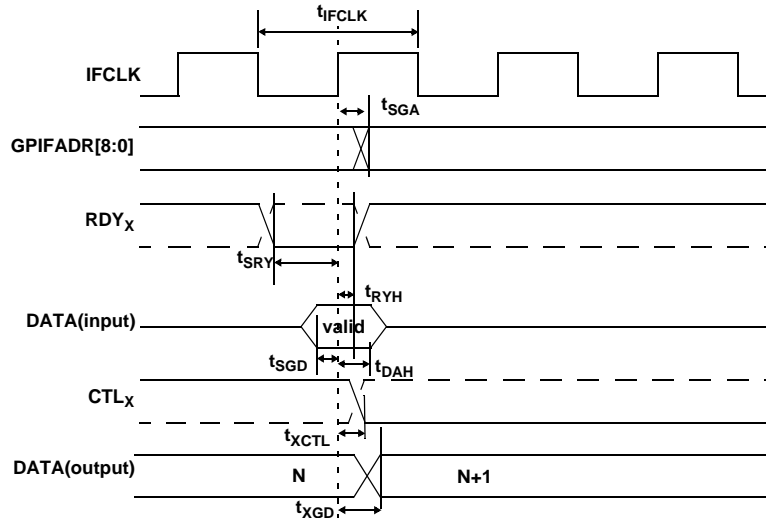


Table 17. GPIF Synchronous Signals Parameters with Internally Sourced IFCLK<sup>[21, 22]</sup>

Parameter	Description	Min	Max	Typ		Unit
				Min	Max	
$t_{IFCLK}$	IFCLK Period	20.83	–	–	–	ns
$t_{SRY}$	RDY <sub>x</sub> to Clock Setup Time	8.9	–	–	–	ns
$t_{RYH}$	Clock to RDY <sub>x</sub>	0	–	–	–	ns
$t_{SGD}$	GPIF Data to Clock Setup Time	9.2	–	–	–	ns
$t_{DAH}$	GPIF Data Hold Time	0	–	–	–	ns
$t_{SGA}$	Clock to GPIF Address Propagation Delay	–	7.5	–	–	ns
$t_{XGD}$	Clock to GPIF Data Output Propagation Delay	–	11	–	–	ns
$t_{XCTL}$	Clock to CTL <sub>x</sub> Output Propagation Delay	–	6.7	–	–	ns
$t_{IFCLKR}$	IFCLK rise time	–	–	–	900	ps
$t_{IFCLKF}$	IFCLK fall time	–	–	–	900	ps
$t_{IFCLKOD}$	IFCLK Output duty cycle	–	–	49	51	%
$t_{IFCLKJ}$	IFCLK jitter peak to peak	–	–	–	300	ps

Table 18. GPIF Synchronous Signals Parameters with Externally Sourced IFCLK<sup>[22]</sup>

Parameter	Description	Min	Max	Unit
$t_{IFCLK}$	IFCLK Period <sup>[23]</sup>	20.83	200	ns
$t_{SRY}$	RDY <sub>x</sub> to Clock Setup Time	2.9	–	ns
$t_{RYH}$	Clock to RDY <sub>x</sub>	3.7	–	ns
$t_{SGD}$	GPIF Data to Clock Setup Time	3.2	–	ns
$t_{DAH}$	GPIF Data Hold Time	4.5	–	ns
$t_{SGA}$	Clock to GPIF Address Propagation Delay	–	11.5	ns
$t_{XGD}$	Clock to GPIF Data Output Propagation Delay	–	15	ns
$t_{XCTL}$	Clock to CTL <sub>x</sub> Output Propagation Delay	–	10.7	ns

### Notes

21. Dashed lines denote signals with programmable polarity.

22. GPIF asynchronous RDY<sub>x</sub> signals have a minimum setup time of 50 ns when using internal 48 MHz IFCLK.

23. IFCLK must not exceed 48 MHz.

### 9.1 Slave FIFO Synchronous Read

Figure 9-7. Slave FIFO Synchronous Read Timing Diagram<sup>[21]</sup>

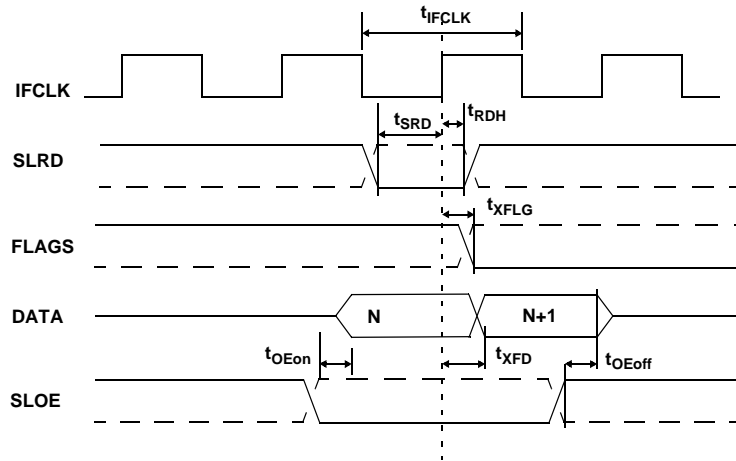


Table 19. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK<sup>[22]</sup>

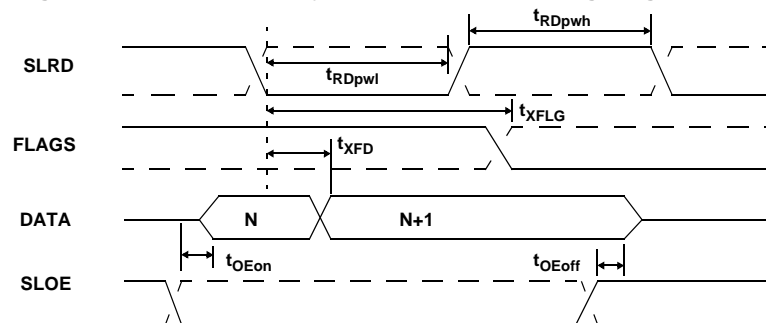
Parameter	Description	Min	Max	Typ		Unit
				Min	Max	
$t_{IFCLK}$	IFCLK period	20.83	–	–	–	ns
$t_{SRD}$	SLRD to clock setup time	18.7	–	–	–	ns
$t_{RDH}$	Clock to SLRD hold time	0	–	–	–	ns
$t_{OEon}$	SLOE turn on to FIFO data valid	–	10.5	–	–	ns
$t_{OEoff}$	SLOE turn off to FIFO data hold	–	10.5	–	–	ns
$t_{XFLG}$	Clock to FLAGS output propagation delay	–	9.5	–	–	ns
$t_{XFD}$	Clock to FIFO data output propagation delay	–	11	–	–	ns
$t_{IFCLKR}$	IFCLK rise time	–	–	–	900	ps
$t_{IFCLKF}$	IFCLK fall time	–	–	–	900	ps
$t_{IFCLKOD}$	IFCLK Output duty cycle	–	–	49	51	%
$t_{IFCLKJ}$	IFCLK jitter peak to peak	–	–	–	300	ps

**Table 20. Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK<sup>[22]</sup>**

Parameter	Description	Min	Max	Unit
$t_{IFCLK}$	IFCLK period	20.83	200	ns
$t_{SRD}$	SLRD to clock setup time	12.7	–	ns
$t_{RDH}$	Clock to SLRD hold time	3.7	–	ns
$t_{OEon}$	SLOE turn on to FIFO data valid	–	10.5	ns
$t_{OEoff}$	SLOE turn off to FIFO data hold	–	10.5	ns
$t_{XFLG}$	Clock to FLAGS output propagation delay	–	13.5	ns
$t_{XFD}$	Clock to FIFO data output propagation delay	–	15	ns

### 9.8 Slave FIFO Asynchronous Read

**Figure 9-8. Slave FIFO Asynchronous Read Timing Diagram<sup>[21]</sup>**



**Table 21. Slave FIFO Asynchronous Read Parameters<sup>[24]</sup>**

Parameter	Description	Min	Max	Unit
$t_{RDpwl}$	SLRD pulse width LOW	50	–	ns
$t_{RDpwh}$	SLRD pulse width HIGH	50	–	ns
$t_{XFLG}$	SLRD to FLAGS output propagation delay	–	70	ns
$t_{XFD}$	SLRD to FIFO data output propagation delay	–	15	ns
$t_{OEon}$	SLOE turn-on to FIFO data valid	–	10.5	ns
$t_{OEoff}$	SLOE turn-off to FIFO data hold	–	10.5	ns

**Note**

24. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

### 9.9 Slave FIFO Synchronous Write

Figure 9-9. Slave FIFO Synchronous Write Timing Diagram<sup>[21]</sup>

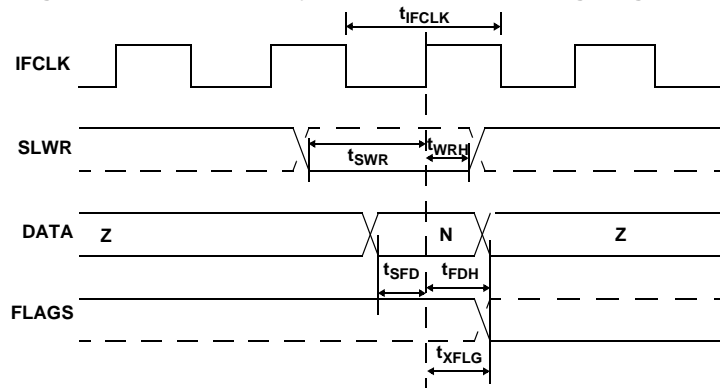


Table 22. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK<sup>[22]</sup>

Parameter	Description	Min	Max	Unit
$t_{IFCLK}$	IFCLK period	20.83	–	ns
$t_{SWR}$	SLWR to clock setup time	10.4	–	ns
$t_{WRH}$	Clock to SLWR hold time	0	–	ns
$t_{SFD}$	FIFO data to clock setup time	9.2	–	ns
$t_{FDH}$	Clock to FIFO data hold time	0	–	ns
$t_{XFLG}$	Clock to FLAGS output propagation time	–	9.5	ns

Table 23. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK<sup>[22]</sup>

Parameter	Description	Min	Max	Unit
$t_{IFCLK}$	IFCLK Period	20.83	200	ns
$t_{SWR}$	SLWR to clock setup time	12.1	–	ns
$t_{WRH}$	Clock to SLWR hold time	3.6	–	ns
$t_{SFD}$	FIFO data to clock setup time	3.2	–	ns
$t_{FDH}$	Clock to FIFO data hold time	4.5	–	ns
$t_{XFLG}$	Clock to FLAGS output propagation time	–	13.5	ns

### 9.10 Slave FIFO Asynchronous Write

Figure 9-10. Slave FIFO Asynchronous Write Timing Diagram<sup>[21]</sup>

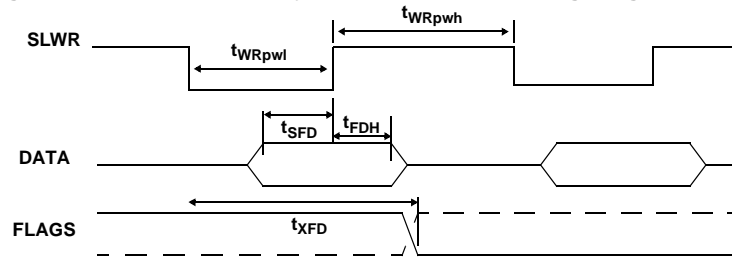


Table 24. Slave FIFO Asynchronous Write Parameters with Internally Sourced IFCLK<sup>[24]</sup>

Parameter	Description	Min	Max	Unit
$t_{WRpwl}$	SLWR pulse LOW	50	–	ns
$t_{WRpwh}$	SLWR pulse HIGH	70	–	ns
$t_{SFD}$	SLWR to FIFO DATA setup time	10	–	ns
$t_{FDH}$	FIFO DATA to SLWR hold time	10	–	ns
$t_{XFD}$	SLWR to FLAGS output propagation delay	–	70	ns

### 9.11 Slave FIFO Synchronous Packet End Strobe

Figure 9-11. Slave FIFO Synchronous Packet End Strobe Timing Diagram<sup>[21]</sup>

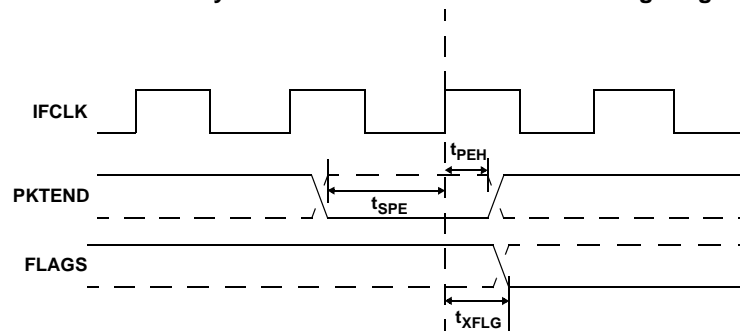


Table 25. Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK<sup>[22]</sup>

Parameter	Description	Min	Max	Unit
$t_{IFCLK}$	IFCLK period	20.83	–	ns
$t_{SPE}$	PKTEND to clock setup time	14.6	–	ns
$t_{PEH}$	Clock to PKTEND hold time	0	–	ns
$t_{XFLG}$	Clock to FLAGS output propagation delay	–	9.5	ns

Table 26. Slave FIFO Synchronous Packet End Strobe Parameters with Externally Sourced IFCLK<sup>[22]</sup>

Parameter	Description	Min	Max	Unit
$t_{IFCLK}$	IFCLK period	20.83	200	ns
$t_{SPE}$	PKTEND to clock setup time	8.6	–	ns
$t_{PEH}$	Clock to PKTEND hold time	2.5	–	ns
$t_{XFLG}$	Clock to FLAGS output propagation delay	–	13.5	ns

There is no specific timing requirement that should be met for asserting PKTEND pin to asserting SLWR. PKTEND can be asserted with the last data value clocked into the FIFOs or thereafter. The setup time  $t_{SPE}$  and the hold time  $t_{PEH}$  must be met.

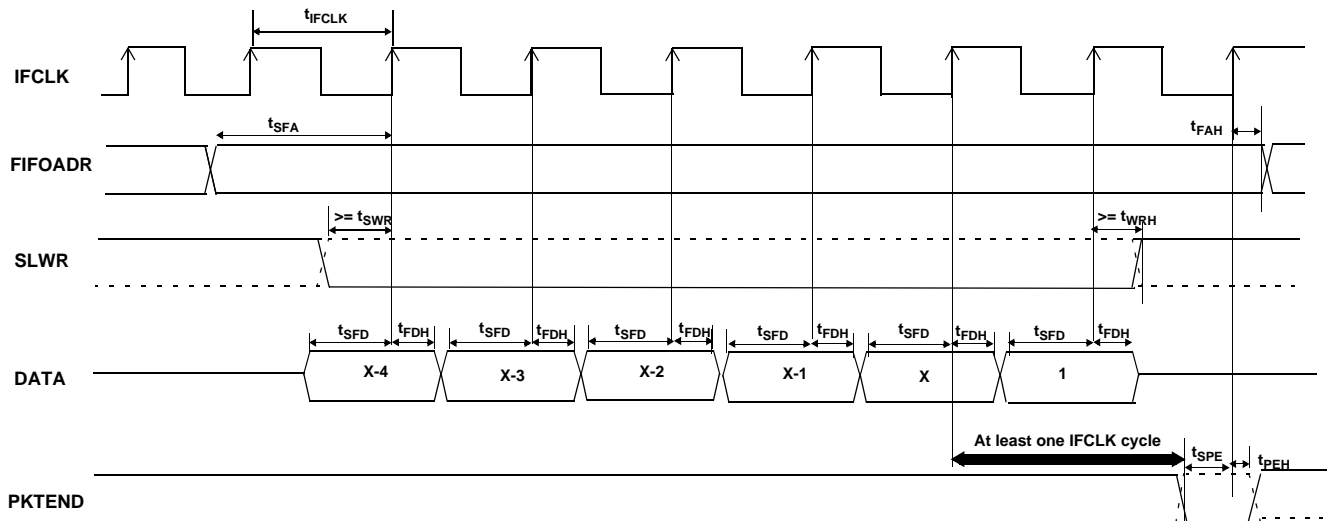
Although there are no specific timing requirements for the PKTEND assertion, there is a specific corner case condition that needs attention while using the PKTEND to commit a one byte or word packet. There is an additional timing requirement that needs to be met when the FIFO is configured to operate in auto mode and it is required to send two packets back to back: a full packet (full defined as the number of bytes in the FIFO meeting the level set in AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin. In this scenario, the user must ensure to assert PKTEND at least one clock cycle after the rising edge that

caused the last byte or word to be clocked into the previous auto committed packet. Figure 9-12 shows this scenario. X is the value the AUTOINLEN register is set to when the IN endpoint is configured to be in auto mode.

Figure 9-12 shows a scenario where two packets are committed. The first packet gets committed automatically when the number of bytes in the FIFO reaches X (value set in AUTOINLEN register) and the second one byte/word short packet being committed manually using PKTEND.

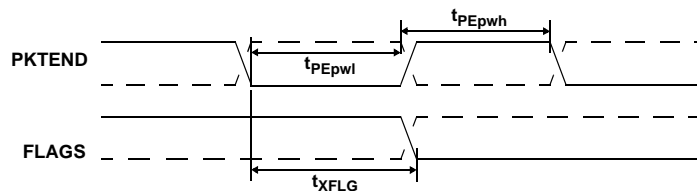
Note that there is at least one IFCLK cycle timing between the assertion of PKTEND and clocking of the last byte of the previous packet (causing the packet to be committed automatically). Failing to adhere to this timing results in the FX2 failing to send the one byte or word short packet.

**Figure 9-12. Slave FIFO Synchronous Write Sequence and Timing Diagram<sup>[21]</sup>**



## 9.12 Slave FIFO Asynchronous Packet End Strobe

**Figure 9-13. Slave FIFO Asynchronous Packet End Strobe Timing Diagram<sup>[21]</sup>**



**Table 27. Slave FIFO Asynchronous Packet End Strobe Parameters<sup>[24]</sup>**

Parameter	Description	Min	Max	Unit
$t_{PEpwl}$	PKTEND pulse width LOW	50	–	ns
$t_{PEpwh}$	PKTEND pulse width HIGH	50	–	ns
$t_{XFLG}$	PKTEND to FLAGS output propagation delay	–	115	ns



### 9.13 Slave FIFO Output Enable

Figure 9-14. Slave FIFO Output Enable Timing Diagram<sup>[21]</sup>

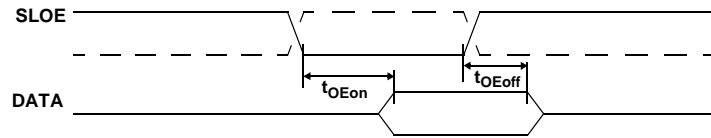


Table 28. Slave FIFO Output Enable Parameters

Parameter	Description	Min	Max	Unit
$t_{OEon}$	SLOE assert to FIFO DATA output		10.5	ns
$t_{OEoff}$	SLOE deassert to FIFO DATA hold		10.5	ns

### 9.14 Slave FIFO Address to Flags/Data

Figure 9-15. Slave FIFO Address to Flags/Data Timing Diagram<sup>[21]</sup>

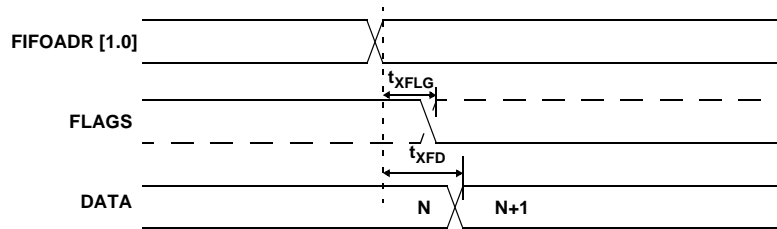


Table 29. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Min	Max	Unit
$t_{XFLG}$	FIFOADR[1:0] to FLAGS output propagation delay	–	10.7	ns
$t_{XFD}$	FIFOADR[1:0] to FIFODATA output propagation delay	–	14.3	ns

### 9.15 Slave FIFO Synchronous Address

Figure 9-16. Slave FIFO Synchronous Address Timing Diagram<sup>[21]</sup>

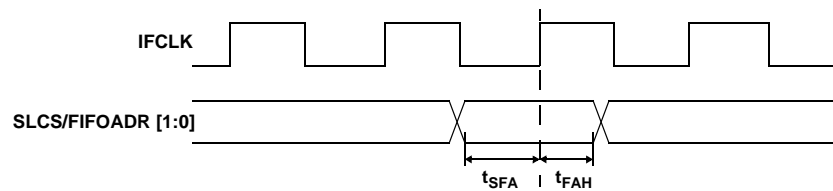


Table 30. Slave FIFO Synchronous Address Parameters<sup>[22]</sup>

Parameter	Description	Min	Max	Unit
$t_{IFCLK}$	Interface clock period	20.83	200	ns
$t_{SFA}$	FIFOADR[1:0] to clock setup time	25	–	ns
$t_{FAH}$	Clock to FIFOADR[1:0] hold time	10	–	ns

### 9.16 Slave FIFO Asynchronous Address

Figure 9-17. Slave FIFO Asynchronous Address Timing Diagram<sup>[21]</sup>

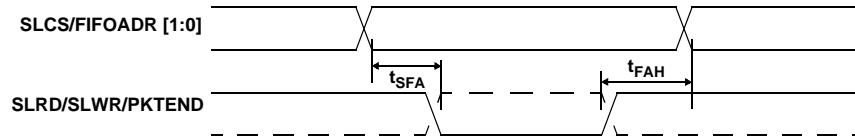


Table 31. Slave FIFO Asynchronous Address Parameters<sup>[24]</sup>

Parameter	Description	Min	Max	Unit
$t_{SFA}$	FIFOADR[1:0] to SLRD/SLWR/PKTEND setup time	10	–	ns
$t_{FAH}$	RD/WR/PKTEND to FIFOADR[1:0] hold time	10	–	ns

### 9.17 Sequence Diagram

#### 9.17.1 Single and Burst Synchronous Read Example

Figure 9-18. Slave FIFO Synchronous Read Sequence and Timing Diagram<sup>[21]</sup>

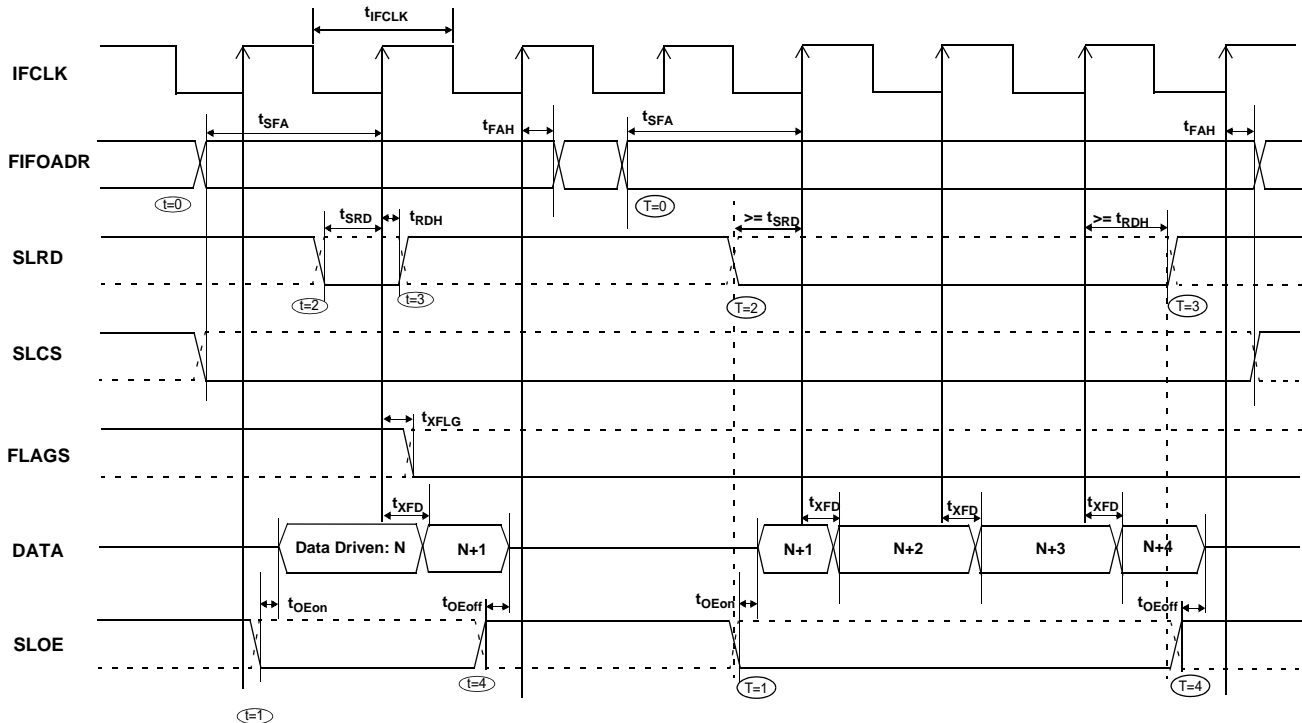


Figure 9-19. Slave FIFO Synchronous Sequence of Events Diagram

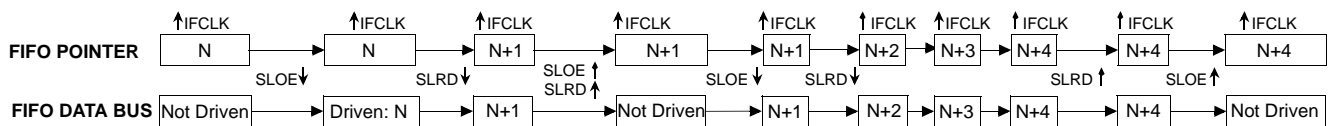


Figure 9-18 on page 50 shows the timing relationship of the SLAVE FIFO signals during a synchronous FIFO read using IFCLK as the synchronizing clock. The diagram illustrates a single read followed by a burst read.

- At  $t = 0$  the FIFO address is stable and the signal SLCS is asserted (SLCS may be tied low in some applications). Note that  $t_{SFA}$  has a minimum of 25 ns. This means when IFCLK is running at 48 MHz, the FIFO address setup time is more than one IFCLK cycle.
- At  $t = 1$ , SLOE is asserted. SLOE is an output enable only, whose sole function is to drive the data bus. The data that is driven on the bus is the data that the internal FIFO pointer is currently pointing to. In this example it is the first data value in the FIFO. Note: the data is pre-fetched and is driven on the bus when SLOE is asserted.
- At  $t = 2$ , SLRD is asserted. SLRD must meet the setup time of  $t_{SRD}$  (time from asserting the SLRD signal to the rising edge of the IFCLK) and maintain a minimum hold time of  $t_{RDH}$  (time from the IFCLK edge to the deassertion of the SLRD signal). If the SLCS signal is used, it must be asserted before SLRD is asserted (The SLCS and SLRD signals must both be asserted to start a valid read condition).

- The FIFO pointer is updated on the rising edge of the IFCLK, while SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of  $t_{XFD}$  (measured from the rising edge of IFCLK) the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE MUST also be asserted.

The same sequence of events are shown for a burst read and are marked with the time indicators of  $T = 0$  through 5.

**Note** For the burst mode, the SLRD and SLOE are left asserted during the entire duration of the read. In the burst read mode, when SLOE is asserted, data indexed by the FIFO pointer is on the data bus. During the first read cycle, on the rising edge of the clock the FIFO pointer is updated and increments to point to address  $N+1$ . For each subsequent rising edge of IFCLK, while the SLRD is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

### 9.17.2 Single and Burst Synchronous Write

Figure 9-20. Slave FIFO Synchronous Write Sequence and Timing Diagram<sup>[21]</sup>

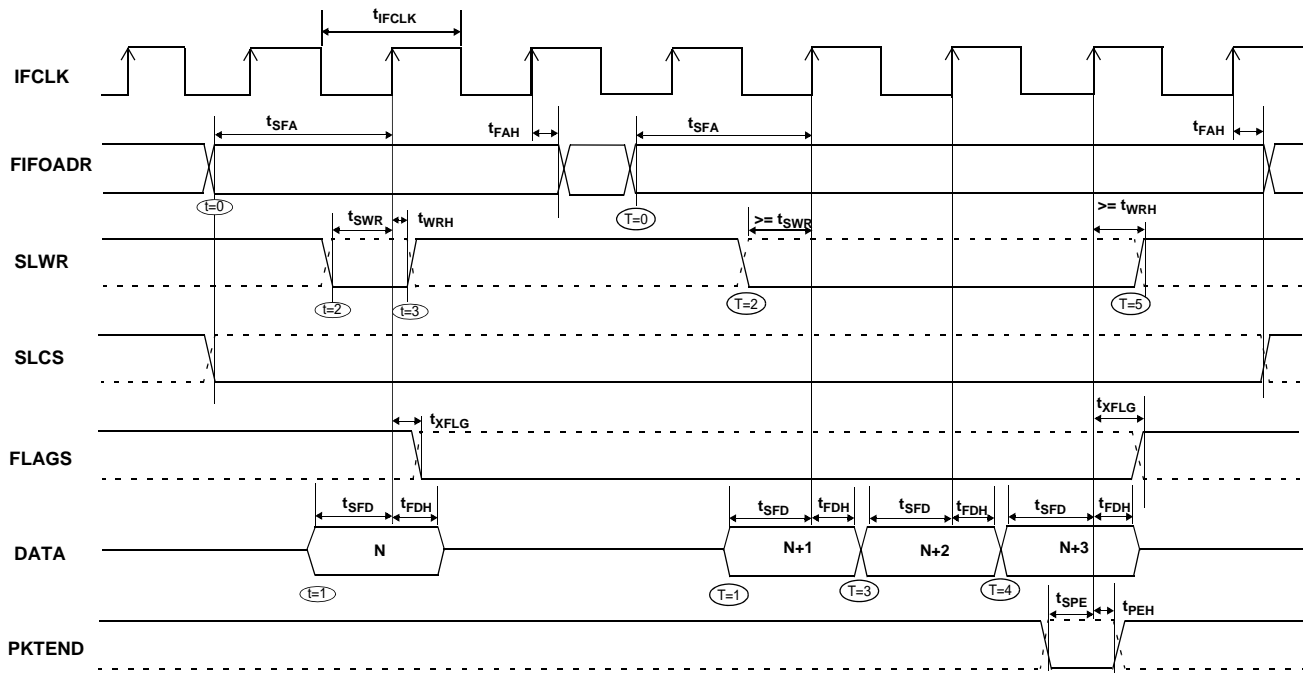


Figure 9-20 shows the timing relationship of the SLAVE FIFO signals during a synchronous write using IFCLK as the synchronizing clock. The diagram illustrates a single write followed by burst write of 3 bytes and committing all 4 bytes as a short packet using the PKTEND pin.

- At  $t = 0$  the FIFO address is stable and the signal SLCS is asserted. (SLCS may be tied low in some applications) Note that  $t_{SFA}$  has a minimum of 25 ns. This means when IFCLK is running at 48 MHz, the FIFO address setup time is more than one IFCLK cycle.
- At  $t = 1$ , the external master/peripheral must output the data value onto the data bus with a minimum set up time of  $t_{SFD}$  before the rising edge of IFCLK.
- At  $t = 2$ , SLWR is asserted. The SLWR must meet the setup time of  $t_{SWR}$  (time from asserting the SLWR signal to the rising edge of IFCLK) and maintain a minimum hold time of  $t_{WRH}$  (time from the IFCLK edge to the deassertion of the SLWR signal). If the SLCS signal is used, it must be asserted with SLWR or before SLWR is asserted (The SLCS and SLWR signals must both be asserted to start a valid write condition).
- While the SLWR is asserted, data is written to the FIFO and on the rising edge of the IFCLK, the FIFO pointer is incremented. The FIFO flag is also updated after a delay of  $t_{XFLG}$  from the rising edge of the clock.

The same sequence of events are also shown for a burst write and are marked with the time indicators of  $T = 0$  through 5.

**Note** For the burst mode, SLWR and SLCS are left asserted for the entire duration of writing all the required data values. In this burst write mode, after the SLWR is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of IFCLK. The FIFO pointer is updated on each rising edge of IFCLK. In Figure 9-20, after the four bytes are written to the FIFO, SLWR is deasserted. The short 4 byte packet can be committed to the host by asserting the PKTEND signal.

There is no specific timing requirement that should be met for asserting PKTEND signal with regards to asserting the SLWR signal. PKTEND can be asserted with the last data value or thereafter. The only requirement is that the setup time  $t_{SPE}$  and the hold time  $t_{PEH}$  must be met. In the scenario of Figure 9-20, the number of data values committed includes the last value written to the FIFO. In this example, both the data value and the PKTEND signal are clocked on the same rising edge of IFCLK. PKTEND can also be asserted in subsequent clock cycles. The FIFOADDR lines should be held constant during the PKTEND assertion.

Although there are no specific timing requirement for the PKTEND assertion, there is a specific corner case condition that needs attention while using the PKTEND to commit a one byte/word packet. Additional timing requirements exists when the FIFO is configured to operate in auto mode and it is desired to send two packets: a full packet (full defined as the number of bytes in the FIFO meeting the level set in AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin.

In this case, the external master must ensure to assert the PKTEND pin at least one clock cycle after the rising edge that caused the last byte or word that needs to be clocked into the previous auto committed packet (the packet with the number of bytes equal to what is set in the AUTOINLEN register). Refer to Figure 9-12 on page 48 for further details on this timing.

9.17.3 Sequence Diagram of a Single and Burst Asynchronous Read

Figure 9-21. Slave FIFO Asynchronous Read Sequence and Timing Diagram<sup>[21]</sup>

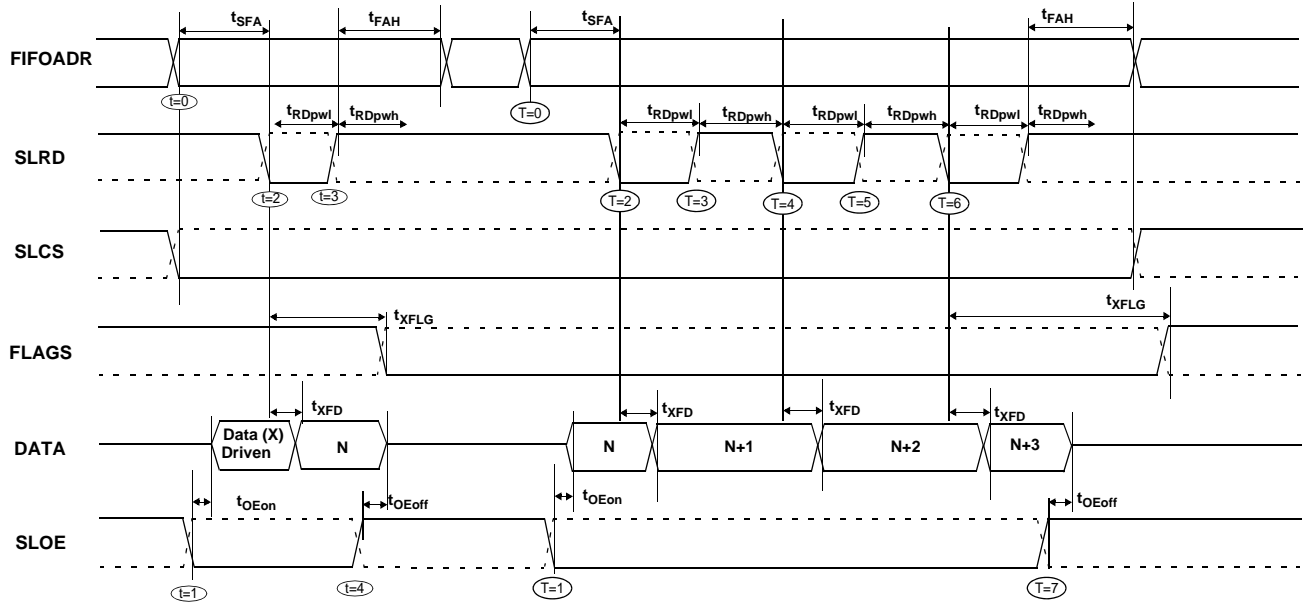


Figure 9-22. Slave FIFO Asynchronous Read Sequence of Events Diagram

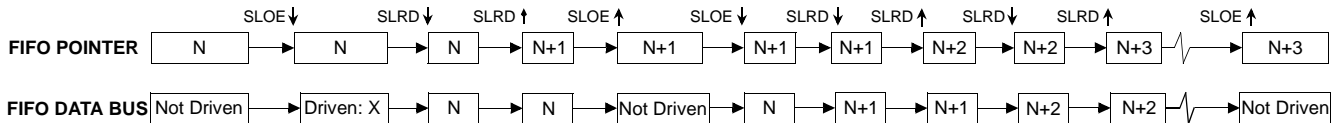


Figure 9-21 shows the timing relationship of the SLAVE FIFO signals during an asynchronous FIFO read. It shows a single read followed by a burst read.

- At  $t = 0$  the FIFO address is stable and the SLCS signal is asserted.
- At  $t = 1$ , SLOE is asserted. This results in the data bus being driven. The data that is driven on to the bus is previous data, it data that was in the FIFO from a prior read cycle.
- At  $t = 2$ , SLRD is asserted. The SLRD must meet the minimum active pulse of  $t_{RDpwl}$  and minimum de-active pulse width of  $t_{RDpwh}$ . If SLCS is used then, SLCS must be asserted before SLRD is asserted (The SLCS and SLRD signals must both be asserted to start a valid read condition.)

- The data that is driven, after asserting SLRD, is the updated data from the FIFO. This data is valid after a propagation delay of  $t_{XFD}$  from the activating edge of SLRD. In Figure 9-21, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle (SLRD is asserted), SLOE must be in an asserted state. SLRD and SLOE can also be tied together.

The same sequence of events is also shown for a burst read marked with T = 0 through 5.

**Note** In burst read mode, during SLOE is assertion, the data bus is in a driven state and outputs the previous data. After SLRD is asserted, the data from the FIFO is driven on the data bus (SLOE must also be asserted) and then the FIFO pointer is incremented.

9.17.4 Sequence Diagram of a Single and Burst Asynchronous Write

Figure 9-23. Slave FIFO Asynchronous Write Sequence and Timing Diagram<sup>[21]</sup>

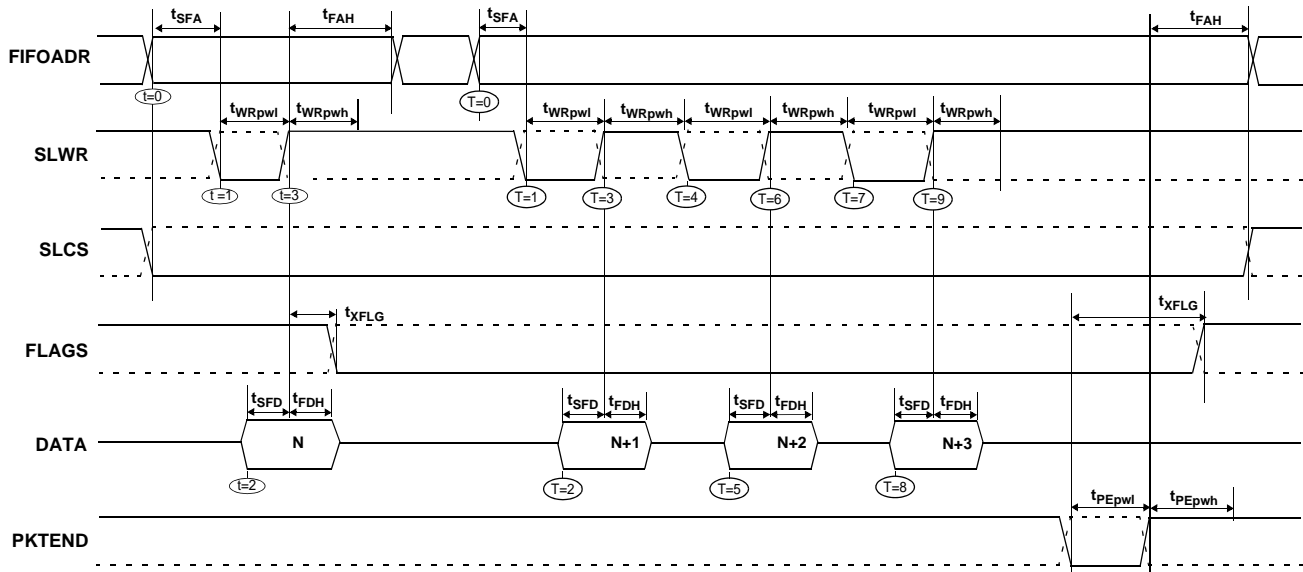


Figure 9-23 shows the timing relationship of the SLAVE FIFO write in an asynchronous mode. The diagram shows a single write followed by a burst write of 3 bytes and committing the 4 byte short packet using PKTEND.

- At  $t = 0$  the FIFO address is applied, insuring that it meets the setup time of  $t_{SFA}$ . If SLCS is used, it must also be asserted (SLCS may be tied low in some applications).
- At  $t = 1$  SLWR is asserted. SLWR must meet the minimum active pulse of  $t_{WRpwl}$  and minimum de-active pulse width of  $t_{WRpwh}$ . If the SLCS is used, it must be asserted with SLWR or before SLWR is asserted.
- At  $t = 2$ , data must be present on the bus  $t_{SFD}$  before the deasserting edge of SLWR.
- At  $t = 3$ , deasserting SLWR causes the data to be written from the data bus to the FIFO and then increments the FIFO pointer. The FIFO flag is also updated after  $t_{XFLG}$  from the deasserting edge of SLWR.

The same sequence of events are shown for a burst write and is indicated by the timing marks of  $T = 0$  through 5.

**Note** In the burst write mode, after SLWR is deasserted, the data is written to the FIFO and then the FIFO pointer is incremented to the next byte in the FIFO. The FIFO pointer is post incremented.

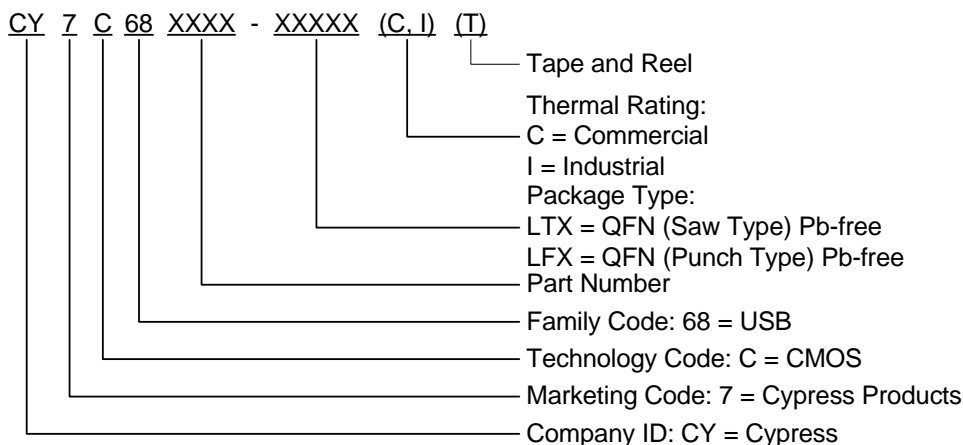
In Figure 9-23 after the four bytes are written to the FIFO and SLWR is deasserted, the short 4 byte packet can be committed to the host using the PKTEND. The external device should be designed to not assert SLWR and the PKTEND signal at the same time. It should be designed to assert the PKTEND after SLWR is deasserted and met the minimum deasserted pulse width. The FIFOADDR lines have to held constant during the PKTEND assertion.

## 10. Ordering Information

Table 32. Ordering Information

Ordering Code	Package Type	RAM Size	# Prog I/Os	8051 Address /Data Busses	Serial Debug <sup>[25]</sup>
<b>Ideal for Battery Powered Applications</b>					
CY7C68014A-128AXC	128 TQFP – Pb-free	16 K	40	16-/8-bit	Y
CY7C68014A-100AXC	100 TQFP – Pb-free	16 K	40	–	Y
CY7C68014A-56PVXC	56 SSOP – Pb-free	16 K	24	–	N
CY7C68014A-56LTXC	56 QFN - Pb-free	16 K	24	–	N
CY7C68016A-56LTXC	56 QFN - Pb-free	16 K	26	–	N
CY7C68016A-56LTXCT	56 QFN - Pb-free	16 K	26	–	N
<b>Ideal for Non Battery Powered Applications</b>					
CY7C68013A-128AXC	128 TQFP – Pb-free	16 K	40	16-/8-bit	Y
CY7C68013A-128AXI	128 TQFP – Pb-free (Industrial)	16 K	40	16-/8-bit	Y
CY7C68013A-100AXC	100 TQFP – Pb-free	16 K	40	–	Y
CY7C68013A-100AXI	100 TQFP – Pb-free (Industrial)	16 K	40	–	Y
CY7C68013A-56PVXC	56 SSOP – Pb-free	16 K	24	–	N
CY7C68013A-56PVXCT	56 SSOP – Pb-free	16 K	24	–	N
CY7C68013A-56PVXI	56 SSOP – Pb-free (Industrial)	16 K	24	–	N
CY7C68013A-56BAXC	56 VFBGA – Pb-free	16 K	24	–	N
CY7C68013A-56BAXCT	56 VFBGA – Pb-free	16 K	24	–	N
CY7C68013A-56LTXC	56 QFN – Pb-free	16 K	24	–	N
CY7C68013A-56LTXCT	56 QFN – Pb-free	16 K	24	–	N
CY7C68013A-56LTXI	56 QFN – Pb-free (Industrial)	16 K	24	–	N
CY7C68015A-56LTXC	56 QFN – Pb-free	16 K	26	–	N
<b>Development Tool Kit</b>					
CY3684	EZ-USB FX2LP development kit				
<b>Reference Design Kit</b>					
CY4611B	USB 2.0 to ATA/ATAPI reference design using EZ-USB FX2LP				

### Ordering Code Definitions



**Note**

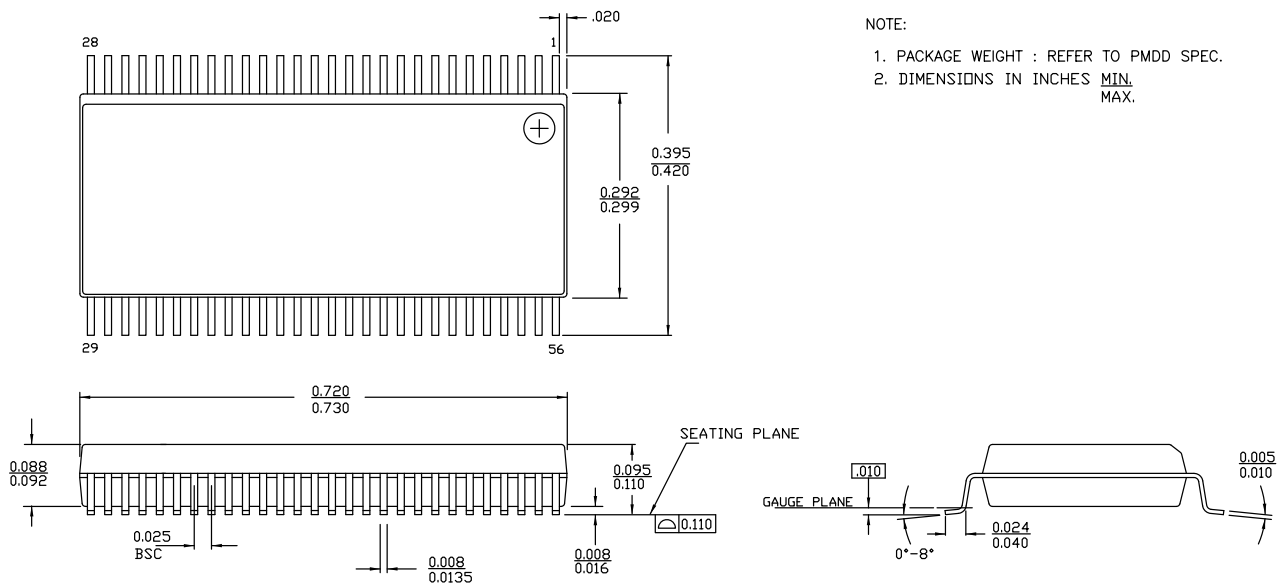
25. As UART is not available in the 56-pin package of CY7C68013A, serial port debugging using Keil Monitor is not possible.

## 11. Package Diagrams

The FX2LP is available in five packages:

- 56-pin SSOP
- 56-pin QFN
- 100-pin TQFP
- 128-pin TQFP
- 56-ball VFBGA

Figure 11-1. 56-Pin Shrink Small Outline Package O56 (51-85062)



NOTE:

1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES MIN.  
MAX.

51-85062 \*F

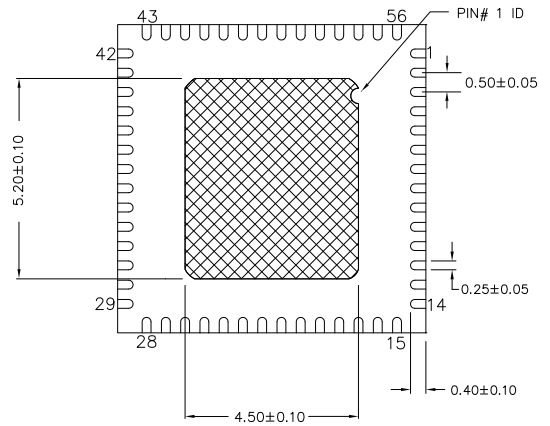
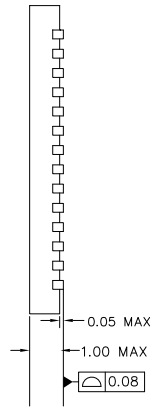
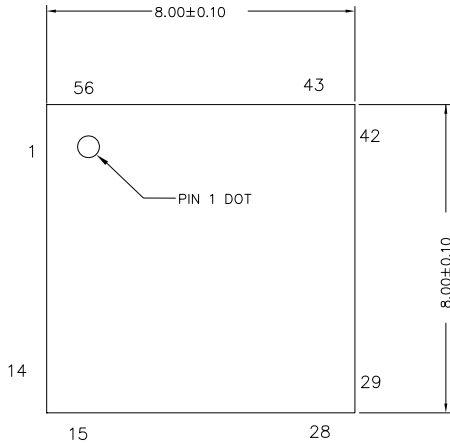


**Figure 11-2. 56-Pin QFN 8 x 8 mm Sawn Version (001-53450)**


TOP VIEW

SIDE VIEW

BOTTOM VIEW



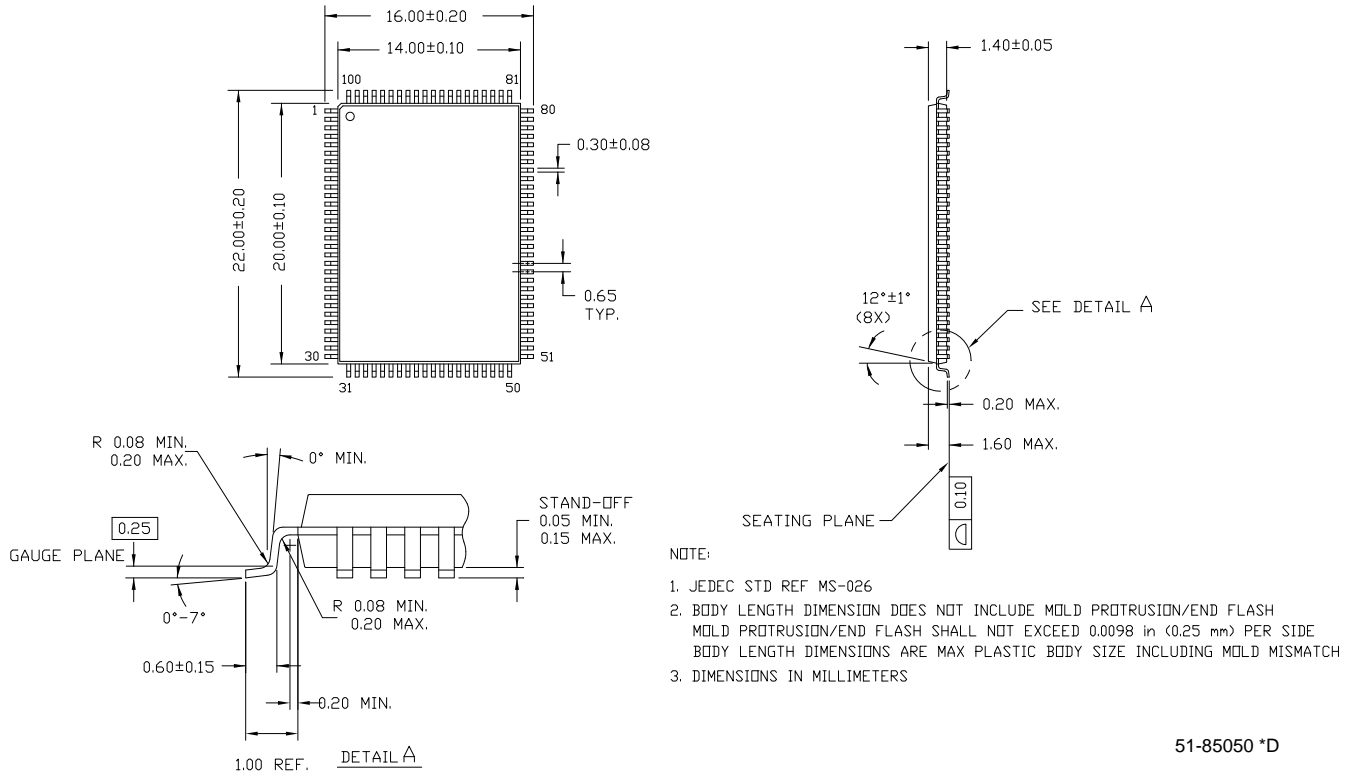
NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT:  $162 \pm 16$  mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-53450 \*C

**Figure 11-3. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A100RA (51-85050)**

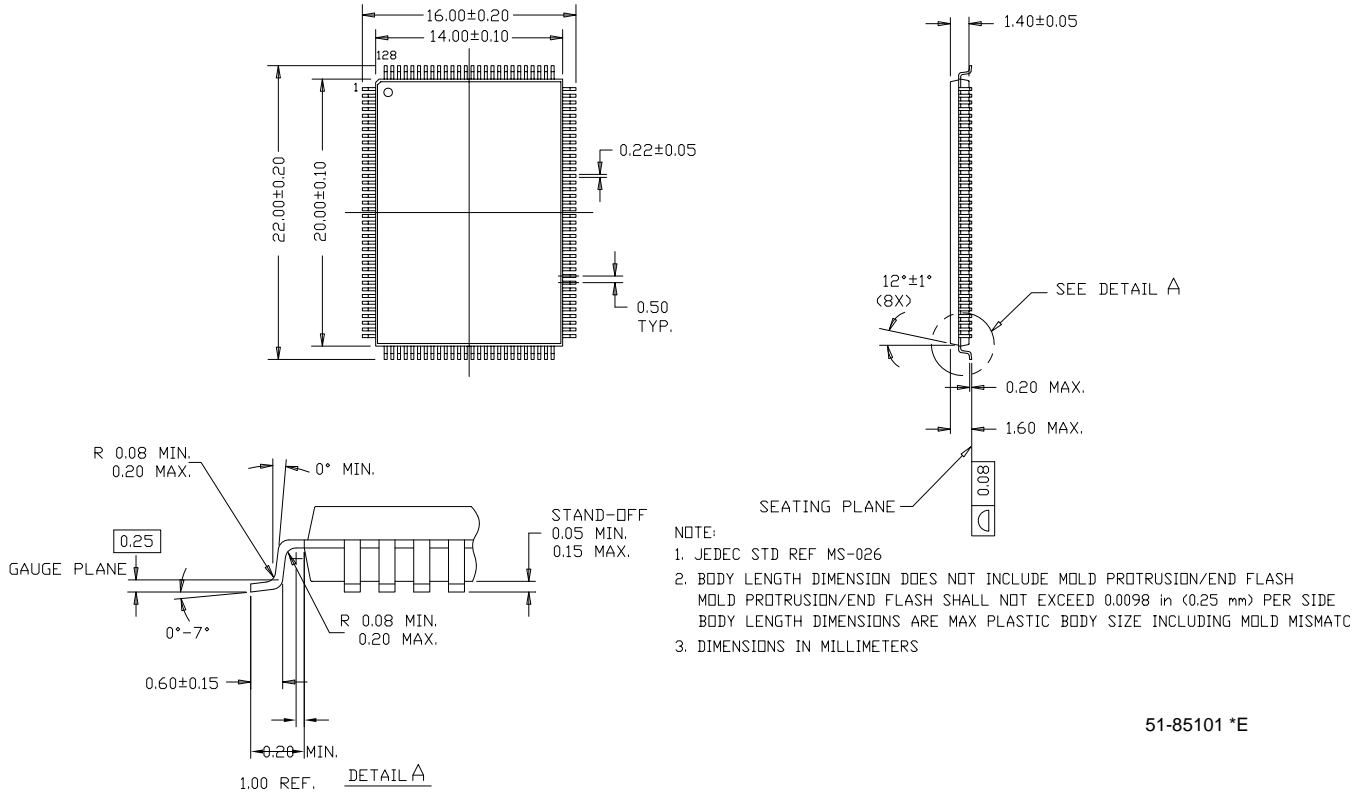
100 Lead Thin Plastic Quad Flatpack 14 X 20 X 1.4mm



51-85050 \*D

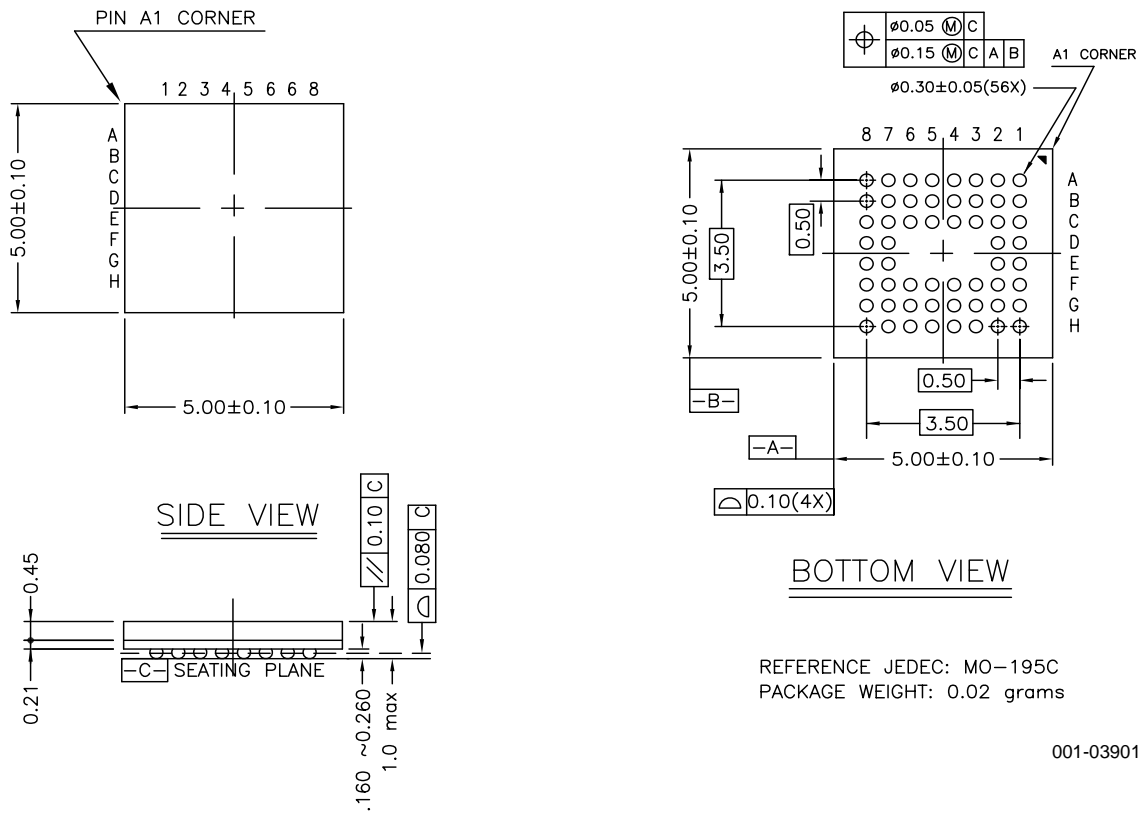
**Figure 11-4. 128-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A128 (51-85101)**

128 Lead Thin Plastic Quad Flatpack 14 X 20 X 1.4mm – A128



51-85101 \*E

**Figure 11-5. 56-Pin VFBGA (5 x 5 x 1.0 mm) 0.50 Pitch, 0.30 Ball BZ56 (001-03901)**



REFERENCE JEDEC: MO-195C  
PACKAGE WEIGHT: 0.02 grams

001-03901 \*E

## 12. PCB Layout Recommendations

Follow these recommendations to ensure reliable high performance operation:<sup>[26]</sup>

- Four layer impedance controlled boards are required to maintain signal quality.
- Specify impedance targets (ask your board vendor what they can achieve).
- To control impedance, maintain trace widths and trace spacing.
- Minimize stubs to minimize reflected signals.
- Connections between the USB connector shell and signal ground must be near the USB connector.
- Bypass and flyback caps on VBus, near connector, are recommended.
- DPLUS and DMINUS trace lengths should be kept to within 2 mm of each other in length, with preferred length of 20 to 30 mm.
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to split under these traces.
- Do not place vias on the DPLUS or DMINUS trace routing.
- Isolate the DPLUS and DMINUS traces from all other signal traces by no less than 10 mm.

### Note

26. Source for recommendations: *EZ-USB FX2™ PCB Design Recommendations*, <http://www.cypress.com> and *High Speed USB Platform Design Guidelines*, [http://www.usb.org/developers/docs/hs\\_usb\\_pdg\\_r1\\_0.pdf](http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf).

### 13. Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the Printed Circuit Board (PCB) is made by soldering the leads on the bottom surface of the package to the PCB. Hence, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. Design a Copper (Cu) fill in the PCB as a thermal pad under the package. Heat is transferred from the FX2LP through the device's metal paddle on the bottom side of the package. Heat from here is conducted to the PCB at the thermal pad. It is then conducted to the PCB inner ground plane by a 5 × 5 array of via. A via is a plated through hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each via to resist solder flow into the via. The mask on the top side also minimizes outgassing during the solder reflow process.

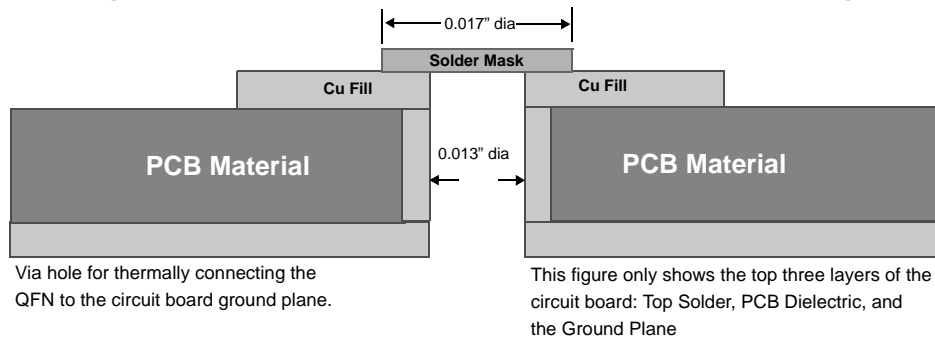
For further information on this package design refer to Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages. You can find this on Amkor's website <http://www.amkor.com>.

The application note provides detailed information about board mounting guidelines, soldering flow, rework process, etc.

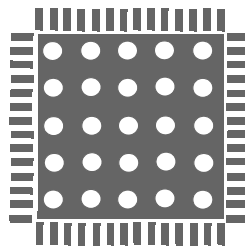
Figure 13-1 shows a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template should be designed to allow at least 50% solder coverage. The thickness of the solder paste template should be 5 mil. Use the No Clean type 3 solder paste for mounting the part. Nitrogen purge is recommended during reflow.

Figure 13-2 is a plot of the solder mask pattern and Figure 13-3 displays an X-Ray image of the assembly (darker areas indicate solder).

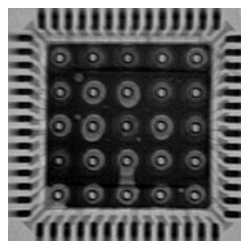
**Figure 13-1. Cross-section of the Area Underneath the QFN Package**



**Figure 13-2. Plot of the Solder Mask (White Area)**



**Figure 13-3. X-ray Image of the Assembly**



## Acronyms

### Acronyms Used in this Document

Acronym	Description
ASIC	application specific integrated circuit
ATA	advanced technology attachment
DID	device identifier
DSL	digital service line
DSP	digital signal processor
ECC	error correction code
EEPROM	electrically erasable programmable read only memory
EPP	enhanced parallel port
FIFO	first in first out
GPIF	general programmable interface
GPIO	general purpose input output
I/O	input output
LAN	local area network
MPEG	moving picture experts group
PCMCIA	personal computer memory card international association
PID	product identifier
PLL	phase locked loop
QFN	quad flat no leads
RAM	random access memory
SIE	serial interface engine
SOF	start of frame
SSOP	super small outline package
TQFP	thin quad flat pack
USARTS	universal serial asynchronous receiver/transmitter
USB	universal serial bus
UTOPIA	universal test and operations physical-layer interface
VFBGA	very fine ball grid array
VID	vendor identifier

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
KHz	kilohertz
mA	milliamperes
Mbps	megabits per second
MBPs	megabytes per second
MHz	megahertz
uA	microamperes
V	volts

## Errata

This section describes the errata for the EZ-USB<sup>®</sup> FX2LP™ CY7C68013A/14A/15A/16A Rev. B silicon. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### Part Numbers Affected

Part Number	Package Type	Operating Range
CY7C68013A	All	Commercial
CY7C68014A	All	Commercial
CY7C68015A	All	Commercial
CY7C68016A	All	Commercial

### CY7C68013A/14A/15A/16A Qualification Status

In production

### CY7C68013A/14A/15A/16A Errata Summary

This table defines the errata for available CY7C68013A/14A/15A/16A family devices. An "X" indicates that the errata pertain to the selected device.

Items	CY7C68013A/14A/15A/16A	Silicon Revision	Fix Status
[1] Empty Flag Assertion	X	B	No silicon fix planned currently. Use workaround

#### 1. Empty Flag Assertion

##### ■ Problem Definition

In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction.

##### ■ Parameters Affected

NA

##### ■ Trigger Condition(S)

In Slave FIFO Asynchronous Word Wide Mode, after firmware boot and initialization, EP2 OUT endpoint empty flag indicates status as 'Empty'. When data is received in EP2, the status changes to 'Not-Empty'. However, if data transferred to EP2 is a single word, then asserting SLRD with FIFOADR pointing to any other endpoint changes 'Not-Empty' status to 'Empty' for EP2 even though there is a word data (or it is untouched). This is noticed only when the single word is sent as the first transaction and not if it follows a multi-word packet as the first transaction.

##### ■ Scope of Impact

External interface does not see data available in EP2 OUT endpoint and can end up waiting for data to be read.

##### ■ Workaround

One of the following workarounds can be used:

- Send a pulse signal to the SLWR pin, with FIFOADR pins pointing to an endpoint other than EP2, after firmware initialization and before or after transferring the data to EP2 from the host
- Set the length of the first data to EP2 to be more than a word
- Prioritize EP2 read from the Master for multiple OUT EPs and single word write to EP2
- Write to an IN EP, if any, from the Master before reading from other OUT EPs (other than EP2) from the Master.

##### ■ Fix Status

There is no silicon fix planned for this currently; use the workarounds provided.



## Document History Page

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	124316	VCS	03/17/03	New datasheet
*A	128461	VCS	09/02/03	Added PN CY7C68015A throughout datasheet Modified <a href="#">Figure 2-1</a> to add ECC block and fix errors Removed word “compatible” where associated with I <sup>2</sup> C Corrected grammar and formatting in various locations Updated Sections 3.2.1, 3.9, 3.11, <a href="#">Table 8</a> , Section 5.0 Added Sections 3.15, 3.18.4, 3.20 Modified <a href="#">Figure 2-5</a> for clarity Updated <a href="#">Figure 11-2</a> to match current spec revision
*B	130335	KKV	10/09/03	Restored PRELIMINARY to header (had been removed in error from rev. *A)
*C	131673	KKU	02/12/04	Section 8.1 changed “certified” to “compliant” <a href="#">Table 13</a> added parameter V <sub>H_X</sub> and V <sub>L_X</sub> Added Sequence diagrams Section 9.16 Updated Ordering information with lead-free parts Updated Registry Summary Section 3.12.4:example changed to column 8 from column 9 Updated <a href="#">Figure 9-3</a> memory write timing Diagram Updated section 3.9 (reset) Updated section 3.15 ECC Generation
*D	230713	KKU	See ECN	Changed Lead free Marketing part numbers in <a href="#">Table 32</a> as per spec change in 28-00054.
*E	242398	TMD	See ECN	Minor Change: datasheet posted to the web,
*F	271169	MON	See ECN	Added USB-IF Test ID number Added USB 2.0 logo Added values for I <sub>susp</sub> , I <sub>cc</sub> , Power Dissipation, V <sub>ih_x</sub> , V <sub>il_x</sub> Changed VCC from ± 10% to ± 5% Changed PKTEND to FLAGS output propagation delay (asynchronous interface) in <a href="#">Table 27</a> from a max value of 70 ns to 115 ns
*G	316313	MON	See ECN	Removed CY7C68013A-56PVXCT part availability Added parts ideal for battery powered applications: CY7C68014A, CY7C68016A Provided additional timing restrictions and requirement about the use of PKETEND pin to commit a short one byte/word packet subsequent to committing a packet automatically (when in auto mode). Added Min Vcc Ramp Up time (0 to 3.3v)
*H	338901	MON	See ECN	Added information about the AUTOPTR1/AUTOPT2 address timing with regards to data memory read/write timing diagram. Removed TBD for Min value of Clock to FIFO Data Output Propagation Delay (t <sub>xFD</sub> ) for Slave FIFO Synchronous Read Changed <a href="#">Table 32</a> to include part CY7C68016A-56LFXC in the part listed for battery powered applications Added register GPCR2 in register summary
*I	371097	MON	See ECN	Added timing for strobing RD#/WR# signals when using PortC strobe feature (Section 9.5)
*J	397239	MON	See ECN	Removed XTALINSRC register from register summary. Changed Vcc margins to ±10% Added 56-pin VFBGA Pin Package Diagram Added 56-pin VFBGA definition in pin listing Added RDK part number to the Ordering Information table

**Document History Page** (continued)

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*K	420505	MON	See ECN	Remove SLCS from figure in Section 9.10. Removed indications that SLRD can be asserted simultaneously with SLCS in Section 9.17.2 and Section 9.17.3 Added Absolute Maximum Temperature Rating for industrial packages in Section 5. Changed number of packages stated in the description in Section 3. to five. Added <a href="#">Table 12</a> on Thermal Coefficients for various packages
*L	2064406	CMCC/PY RS	See ECN	Changed TID number Removed T0OUT and T1OUT from CY7C68015A/16A Updated $t_{SWR}$ Min value in <a href="#">Figure 9-9</a> Updated 56-lead QFN package diagram
*M	2710327	DPT	05/22/2009	Added 56-Pin QFN (8 X 8 mm) package diagram Updated ordering information for CY7C68013A-56LTXC, CY7C68013A-56LTXI, CY7C68014A-56LTXC, CY7C68015A-56LTXC, and CY7C68016A-56LTXC parts.
*N	2727334	ODC	07/01/09	Removed sentence on E-Pad size change from *F revision in the Document History Page Updated 56-Pin Sawn Package Diagram
*O	2756202	ODC	08/26/2009	Updated Ordering Information table and added note 24.
*P	2785207	ODC	10/12/2009	Added information on Pb-free parts in the Ordering information table.
*Q	2811890	ODC	11/20/2009	Updated Program I/Os for the CY7C68016A-56LTXC and CY7C68016A-56LTXCT parts in " <a href="#">Ordering Information</a> " on page 55.
*R	2896281	ODC	03/19/10	Removed inactive parts from the ordering information table. Updated package diagrams. Updated links in Sales, Solutions and Legal Information.
*S	3035980	ODC	09/22/10	Updated template. Changed PPM requirement for the external crystal from +/- 10 ppm to +/- 100 ppm under Electrical specifications. Added table of contents, ordering code definitions, acronym table, and units of measure.
*T	3161410	AAE	02/03/2011	Replaced 56-Pin QFN 8 x 8 mm Punch Version Package Diagram (Figure 11.2) and 56-Pin QFN 8 x 8 mm Sawn Version Package Diagram (Figure 11.3). Updated Package Diagrams (Figure 11.4, Figure 11.5).
*U	3195232	ODC	03/14/2011	Updated table numbering. Added typical values to <a href="#">Table 17 on page 43</a> and <a href="#">Table 19 on page 44</a> based on data obtained from SHAK-63 and SHAK 69. Updated <a href="#">Table 12, "Thermal Characteristics,"</a> on page 37 (CDT 89510) Updated package diagram 001-03901 to *D.
*V	3512313	GAYA	02/01/2012	Removed obsolete part CY7C68014A-56BAXC Removed pruned part CY7C68016A-56LFXC Added parts CY7C68013A-56BAXCT and CY7C68013A-56PVXCT Updated <a href="#">Package Diagrams</a>

**Document History Page** (continued)

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller  
Document Number: 38-08032

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*W	3998554	GAYA	07/19/2013	<p>Added Errata footnote (Note 3).</p> <p>Updated <a href="#">Functional Overview</a>:  Updated <a href="#">Interrupt System</a>:  Updated <a href="#">FIFO/GPIF Interrupt (INT4)</a>:  Added Note 3 and referred the same note in “Endpoint 2 empty flag” in <a href="#">Table 4</a>.</p> <p>Updated <a href="#">Package Diagrams</a>:  spec 51-85062 – Changed revision from *E to *F.  spec 001-53450 – Changed revision from *B to *C.</p> <p>Added <a href="#">Errata</a>.</p> <p>Updated in new template.</p>

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