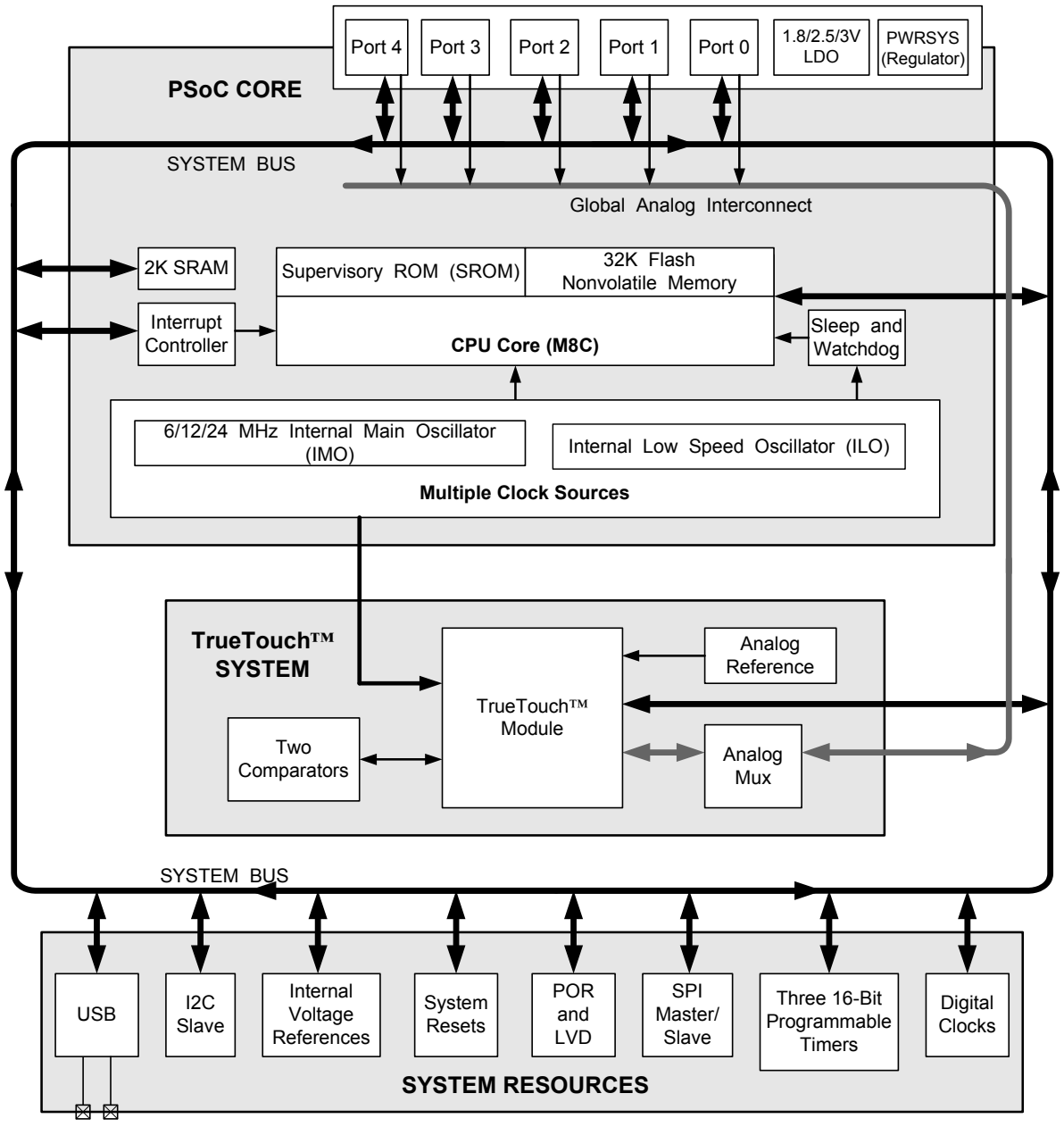
CY7C69356

TrueTouch® Multi-Touch Gesture Full Speed USB Controller

Features

- Powerful Harvard-architecture processor
  - M8C processor speeds running up to 24 MHz
  - Low power at high processing speeds
  - Interrupt controller
  - 1.71 V to 5.5 V operating voltage without USB
  - Commercial temperature range: 0 °C to +70 °C
- TrueTouch™ capacitive touchscreen controller
  - Supports single-touch and multi-touch applications
  - Supports up to 33 X/Y sensor inputs
  - Supports screen sizes 5.6 inch and below (typical)
  - Fast scan rates: Typical 400 µs per sensor
- Includes gesture detection library
- Allows development of customized gestures
- Low-power TrueTouch block
  - 2.5 mA average supply current at 8-ms report rate
  - 1.25 mA average supply current at 16-ms report rate
- Flexible on-chip memory
  - Program and data storage options:
    - 32-KB flash
  - 50,000 erase and write cycles
  - 2048 bytes SRAM data storage
  - Partial flash updates
  - Flexible protection modes
  - In-system serial programming (ISSP)
- Full-speed USB (12 Mbps)
  - Eight uni-directional endpoints
  - One bi-directional control endpoint
  - USB 2.0 compliant
  - Dedicated 512 byte buffer
  - Internal 3.3-V output regulator
  - Available on 48-pin QFN packages only
  - Operating voltage with USB enabled:
    - 3.15 V to 3.45 V when supply voltage is around 3.3 V
    - 4.35 V to 5.25 V when supply voltage is around 5.0 V
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator, and programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128-K trace memory
- Precision, programmable clocking
  - Internal ± 5.0 percent 6, 12, or 24 MHz main oscillator
  - Internal low-speed oscillator at 32 kHz for Watchdog and Sleep
  - Optional external 32-kHz crystal
  - 0.25 percent accuracy for USB with no external components
- Programmable pin configurations
  - 25 mA sink current on all GPIO
  - Pull up, High Z, open drain CMOS drive modes on all GPIO
  - CMOS drive mode on ports 0 and 1
  - Up to 36 analog inputs on GPIO
  - Configurable inputs on all GPIO
  - Selectable, regulated digital I/O on port 1
  - Configurable input threshold for port 1
  - 3.0 V, 20 mA total port 1 source current
  - 5 mA source current mode on ports 0 and 1
  - Hot-swap capable on all Port1GPIO
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
  - High PSRR comparator
  - Low dropout voltage regulator for the analog array
- Additional system resources
  - I^2C slave
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - Implementation requires no clock stretching
    - Implementation during sleep modes with less than 100 µA
    - Hardware address detection
  - SPI master and SPI slave
    - Configurable between 46.9 kHz and 12 MHz
  - Three 16-bit timers
  - Watchdog and sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit
  - 8- to 10-bit Incremental analog-to-digital converter (ADC)
- Package options
  - 48-pin 7 × 7 × 1.0 mm QFN

Logic Block Diagram



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Functional Overview

The Encore-VI from the Encore family of devices is a single-chip solution which provides the fastest and most efficient way to develop and tune a capacitive touchsensing HID application. These devices are designed to replace multiple traditional full-speed USB MCU based components with one, low cost single-chip programmable component. An Encore device includes configurable analog and digital blocks and programmable interconnect. This architecture enables the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in the Logic Block Diagram on page 2, contains three main areas: the Core, the TrueTouch Analog System, and the System Resources (including a full-speed USB port). A common, versatile bus enables connection between I/O and the analog system. Each Encore-VI device includes a dedicated TrueTouch block that provides sensing and scanning control circuitry for capacitive sensing applications. Encore-VI supports 36 general purpose I/O (GPIO) out of which 33 GPIOs can be used for capacitive sensing. The GPIO provides access to the MCU and analog mux.

Refer to the user module data sheet for performance requirements and detailed design process explanations.

The Encore-VI Core

The Encore-VI core encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard architecture microprocessor.

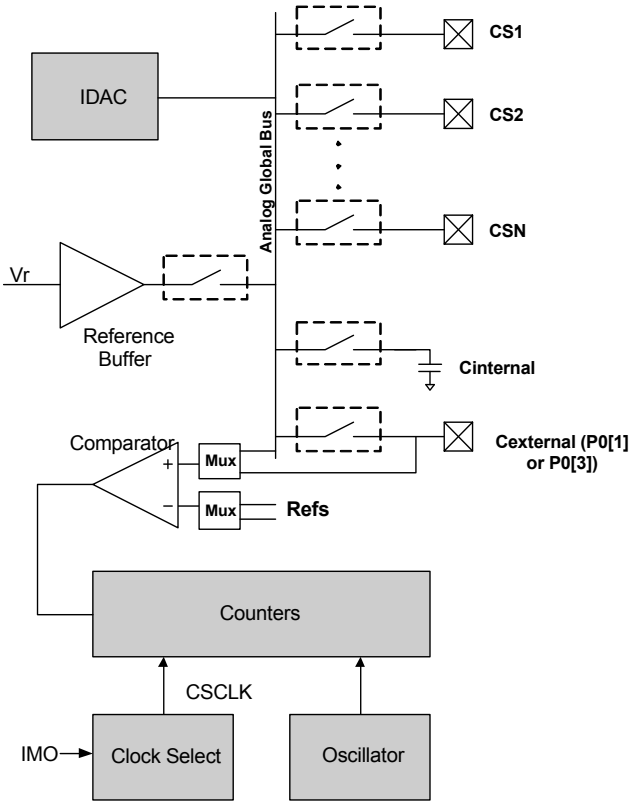
System resources provide additional capability, such as configurable USB and I^2C slave and SPI master-slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

The analog system contains the TrueTouch PSoC® block and an internal 1.2-V analog reference, which together support capacitive sensing of up to 36 inputs.

The TrueTouch Analog System

The analog system contains the capacitive sensing hardware that supports several hardware algorithms. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled TrueTouch capacitive sensing pins are completed easily across multiple ports.

Figure 1. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin, individually or in any combination. The bus also connects to the analog system for analysis with the TrueTouch block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

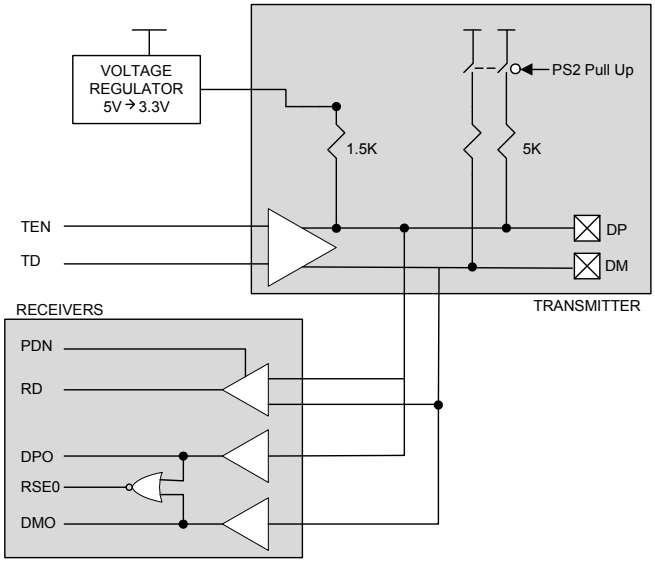
- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that enables analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Full-Speed USB

The Encore-VI USB system resource adheres to the USB 2.0 Specification for full speed devices operating at 12 Mb/second with one upstream port and one USB address. Encore-VI USB consists of these components:

- Serial interface engine (SIE) block.
- PSoC memory arbiter (PMA) block.
- 512 bytes of dedicated SRAM.
- A full-speed USB Transceiver with internal regulator and two dedicated USB pins.

Figure 2. USB Transceiver Regulator



At the Encore-VI system level, the full-speed USB system resource interfaces to the rest of the Encore-VI by way of the M8C's register access instructions and to the outside world by way of the two USB pins. The SIE supports nine endpoints including a bidirectional control endpoint (endpoint 0) and eight unidirectional data endpoints (endpoints 1 to 8). The unidirectional data endpoints are individually configurable as either IN or OUT.

The USB Serial Interface Engine (SIE) allows the Encore-VI device to communicate with the USB host at full speed data rates (12 Mb/s). The SIE simplifies the interface to USB traffic by automatically handling the following USB processing tasks without firmware intervention:

- Translates the encoded received data and formats the data to be transmitted on the bus.
- Generates and checks cyclical redundancy checks (CRCs). Incoming packets failing checksum verification are ignored.
- Checks addresses. Ignores all transactions not addressed to the device.
- Sends appropriate ACK/NAK/Stall handshakes.
- Identifies token type (SETUP, IN, OUT) and sets the appropriate token bit once a valid token in received.
- Identifies Start-of-Frame (SOF) and saves the frame count.
- Sends data to or retrieves data from the USB SRAM, by way of the PSoC Memory Arbiter (PMA).

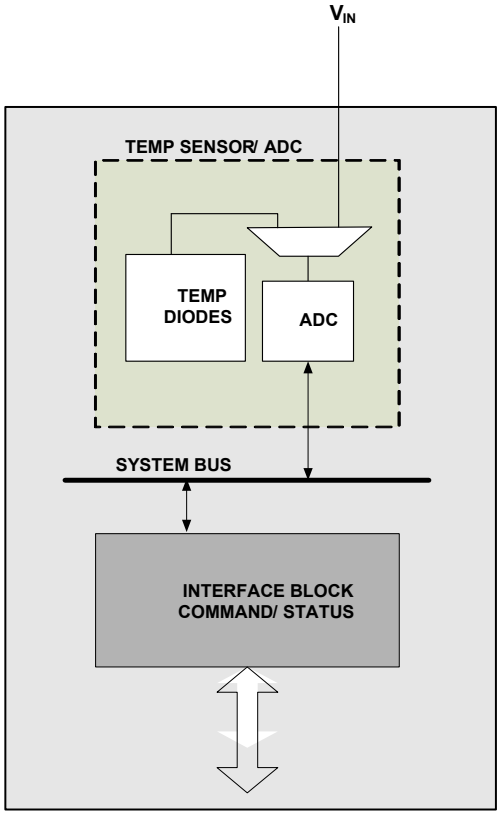
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on Encore-VI device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 3. ADC System Performance Block Diagram



The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes.

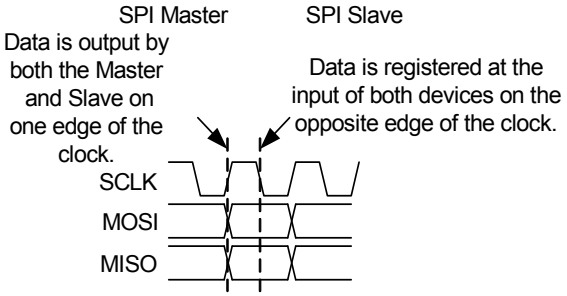
The input to the integrator stage comes from the analog global input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC}.

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

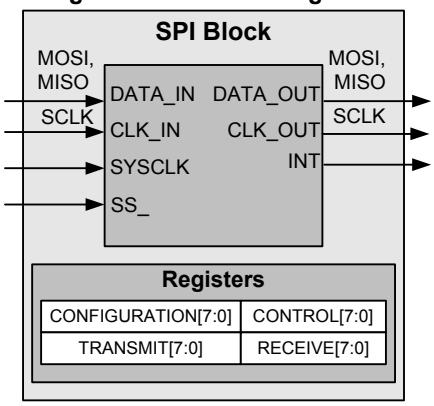
Figure 4. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 5. SPI Block Diagram



SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed, and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is dependent on the application and Encore-VI device and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions:

- To allow for the selection of a given slave in a multi-slave environment.
- To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I^2C Slave

The I^2C slave enhanced communications block is a serial-to-parallel processor, designed to interface the Encore-VI device to a two-wire I^2C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I^2C-specific support for status detection and generation of framing bits. By default, the I^2C slave enhanced module is firmware compatible with the previous generation of I^2C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing. The basic I^2C features include:

- Slave, transmitter, and receiver operation.
- Byte processing for low CPU overhead.
- Interrupt or polling CPU interface.
- Support for clock rates of up to 400 kHz.
- 7- or 10-bit addressing (through firmware support).
- SMBus operation (through firmware support).

Enhanced features of the I^2C Slave Enhanced Module include:

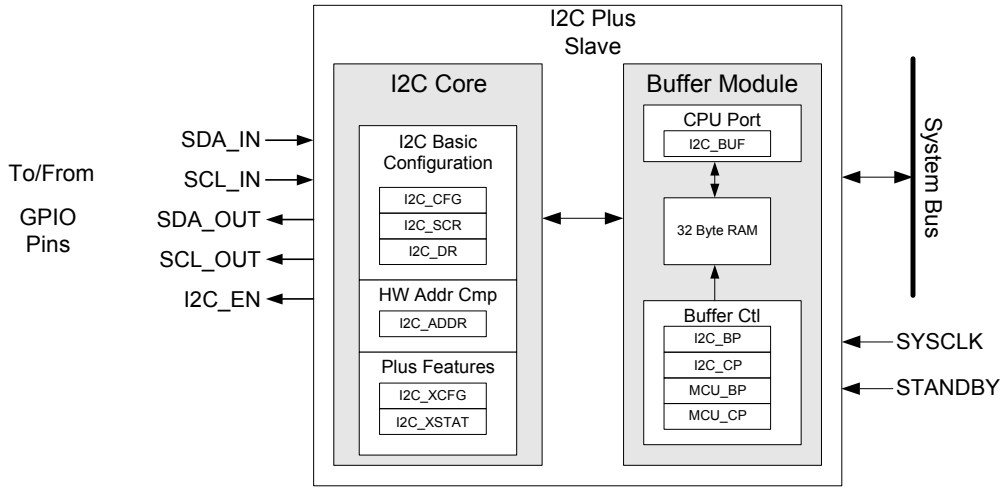
- Support for 7-bit hardware address compare.
- Flexible data buffering schemes.
- A “no bus stalling” operating mode.
- A low power bus monitoring mode.

The I^2C block controls the data (SDA) and the clock (SCL) to the external I^2C interface through direct connections to two dedicated GPIO pins. When I^2C is enabled, these GPIO pins are not available for general purpose use. The Encore-VI CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I^2C slave modules, the I^2C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I^2C bus continues. However, this I^2C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI^2C buffering mode, the I^2C slave interface appears as a

32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Figure 6. I²C Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource.

- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- The 5 V maximum input, 1.8, 2.5, or 3 V selectable output, LDO regulator provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the Encore-VI family of parts.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pin Information

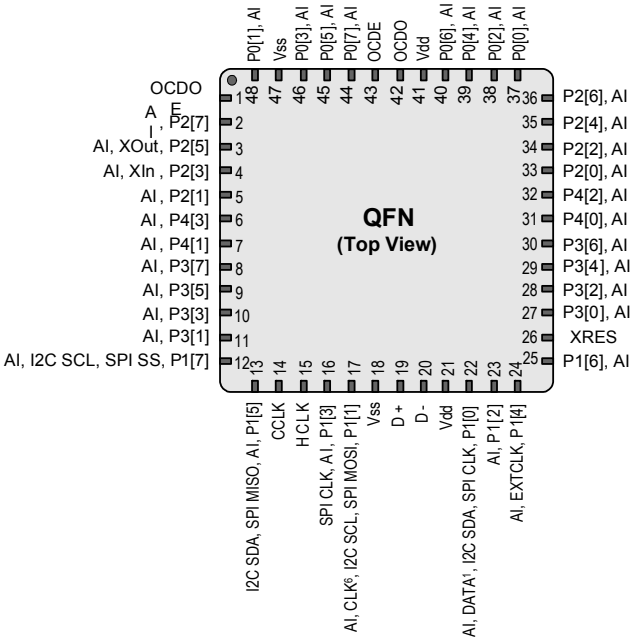
This section describes, lists, and illustrates the CY7C69356 PSoC device pins and pinout configuration.

The CY7C69356 PSoC device is available in a 48-pin QFN package. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of digital I/O.

Table 1. 48-pin QFN Part Pinout [1, 2]

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin.
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut).
4	I/O	I	P2[3]	Crystal input (XIn).
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	I/OHR	I	P1[7]	I2C SCL, SPI SS.
13	I/OHR	I	P1[5]	I2C SDA, SPI MISO.
14			CCLK	OCD CPU clock output.
15			HCLK	OCD high speed clock output.
16	I/OHR	I	P1[3]	SPI CLK.
17	I/OHR	I	P1[1]	ISSP CLK[3], I2C SCL, SPI MOSI.
18	Power		Vss	Ground connection.
19	I/O		D+	
20	I/O		D-	
21	Power		Vdd	Supply voltage.
22	I/OHR	I	P1[0]	ISSP DATA[3], I2C SDA, SPI CLK.
23	I/OHR	I	P1[2]	
24	I/OHR	I	P1[4]	Optional external clock input (EXTCLK).
25	I/OHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down.
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	

CY7C69356 48-pin PSoC Device



Pin No.	Digital	Analog	Name	Description
37	I/OH	I	P0[0]	
38	I/OH	I	P0[2]	
39	I/OH	I	P0[4]	
40	I/OH	I	P0[6]	
41	Power		Vdd	Supply voltage.
42			OCDO	OCD even data I/O.
43			OCDE	OCD odd data output.
44	I/OH	I	P0[7]	
45	I/OH	I	P0[5]	
46	I/OH	I	P0[3]	Integrating input.
47	Power		Vss	Ground connection.
48	I/OH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground.

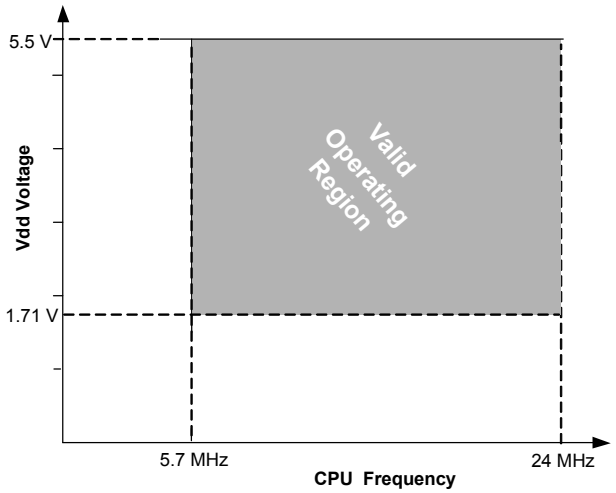
LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Notes
1. During power up or reset event, device P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter any issues.
2. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
3. These are the ISSP pins, which are not High Z at POR.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY7C69356 PSoC devices.

Figure 7. Voltage versus CPU Frequency



Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
Vdd	Supply voltage relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC input voltage		Vss – 0.5	–	Vdd + 0.5	V
V_{IOZ}	DC voltage applied to tristate		Vss – 0.5	–	Vdd + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electro static discharge voltage	Human Body Model ESD.	2000	–	–	V
LU	Latch-up current	In accordance with JESD78 standard.	–	–	200	mA

Operating Temperature

Table 3. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature		0	–	+70	°C
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. See Table 23 on page 26. The user must limit the power consumption to comply with this requirement.	0	–	+85	°C

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 4. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}[4, 5, 6]	Supply voltage	Refer the table DC POR and LVD Specifications on page 16	1.71	–	5.50	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz. No USB/I2C/SPI	–	2.90	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz. No USB/I2C/SPI	–	1.70	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 24 MHz. No USB/I2C/SPI	–	1.20	1.80	mA
I_{SB0}	Deep sleep current	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off	–	0.10	0.50	µA
I_{SB1}	Standby current with POR, LVD and sleep timer	V_{DD} = 3.0 V, T_A = 25 °C, I/O regulator turned off	–	1.1	1.50	µA

Notes

4. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 usec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
5. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
   a. Bring the device out of sleep before powering down.
   b. Assure that V_{DD} falls below 100 mV before powering back up.
   c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
6. For USB mode, the V_{DD} supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application, V_{DD} should be 3.15 V–3.45 V.

DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and 0 °C ≤ T_A ≤ 70 °C, Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 5. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	I_{OH} ≤ 10 µA, maximum of 10 mA source current in all I/Os.	Vdd – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	Vdd – 0.9	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.	Vdd – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	Vdd – 0.9	–	–	V
V_{OH5}	High output voltage Port 1 pins with LDO regulator Enabled for 3 V Out	I_{OH} < 10 µA, Vdd > 3.1 V, maximum of 4 I/Os all sourcing 5 mA.	2.85	3.00	3.3	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator Enabled for 3 V Out	I_{OH} = 5 mA, Vdd > 3.1 V, maximum of 20 mA source current in all I/Os.	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V Out	I_{OH} < 10 µA, Vdd > 2.7 V, maximum of 20 mA source current in all I/Os.	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V Out	I_{OH} = 2 mA, Vdd > 2.7 V, maximum of 20 mA source current in all I/Os.	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V Out	I_{OH} < 10 µA, Vdd > 2.7 V, maximum of 20 mA source current in all I/Os.	1.60	1.80	2.1	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V Out	I_{OH} = 1 mA, Vdd > 2.7 V, maximum of 20 mA source current in all I/Os.	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, Vdd > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.80	V
V_{IH}	Input high voltage		2.00	–	–	V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	1	1000	nA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

Table 6. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high		2.8	–	3.6	V
Volusb	Static output low		–	–	0.3	V
Vdi	Differential input sensitivity		0.2	–	–	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single ended receiver threshold		0.8	–	2.0	V
Cin	Transceiver capacitance		–	–	50	pF
Iio	Hi-Z state data line leakage	On D+ or D- line	–10	–	+10	µA
Rps2	PS/2 pull-up resistance		3000	5000	7000	Ω
Rext	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 7. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus		–	–	800	Ω
R_{GND}	Resistance of initialization switch to Vss		–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V with PUMP on.

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ TA ≤ 85 °C, 3 V ≤ Vdd ≤ 5.5 V.

Table 8. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset			–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage >2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage <2 V	Power supply rejection ratio	–	40	–	dB
Input Range			0	–	1.5	V

ADC Electrical Specifications

Table 9. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range		0	–	V_{REFADC}	V
C_{IIN}	Input capacitance		–	–	5	pF
R_{IN}	Input resistance	Equivalent switched capacitance input resistance for 8-, 9-, or 10-bit resolution	1/(500 fF × data clock)	1/(400 fF × data clock)	1/(300 fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage		1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 18 for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. Sample rate = 0.001/ (2^resolution/data clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. Sample rate = 0.001/ ((2^resolution/data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	Integral nonlinearity		–2	–	+2	LSB
E_{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current		–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR (Vdd > 3.0 V)	–	24	–	dB
		PSRR (Vdd < 3.0 V)	–	30	–	dB

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to Vdd.	0.0	–	1.8	V
I_{LPC}	LPC supply current		–	10	40	µA
V_{OSLPC}	LPC voltage offset		–	2.5	30	mV

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
	V_{DD} value for PPOR trip	V_{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.				
V_{PPOR0}	PORLEV[1:0] = 00b, HPOR = 0		1.61	1.66	1.71	V
V_{PPOR1}	PORLEV[1:0] = 00b, HPOR = 1		–	2.36	2.41	V
V_{PPOR2}	PORLEV[1:0] = 01b, HPOR = 1		–	2.60	2.66	V
V_{PPOR3}	PORLEV[1:0] = 10b, HPOR = 1		–	2.82	2.95	V
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b		2.40 [7]	2.45	2.51	V
V_{LVD1}	VM[2:0] = 001b		2.64 [8]	2.71	2.78	V
V_{LVD2}	VM[2:0] = 010b		2.85 [9]	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b		2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b		3.06	3.13	3.20	V
V_{LVD5}	VM[2:0] = 101b		1.84	1.90	2.32	V
V_{LVD6}	VM[2:0] = 110b		1.75 [10]	1.80	1.84	V
V_{LVD7}	VM[2:0] = 111b		4.62	4.73	4.83	V

Notes

7. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
8. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
9. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
10. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 12. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply voltage for flash write operations		1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify		–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See appropriate DC General Purpose I/O Specifications.	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications.	V_{IH}	–	–	V
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull down resistor.	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull down resistor.	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	Vss + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications. For Vdd > 3 V use V_{OH4} in Table 5 on page 13.	V_{OH}	–	Vdd	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block.	50,000	–	–	Cycles
$Flash_{DR}$	Flash data retention	Following maximum flash write cycles, ambient temperature of 55 °C	20	–	–	Years

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	Internal main oscillator frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F_{IMO12}	Internal main oscillator frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F_{IMO6}	Internal main oscillator frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency	–	5.7	–	25.20	MHz
F_{32K1}	Internal low speed oscillator frequency	–	19	32	50	kHz
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency)	–	13	32	82	kHz
DC_{IMO}	Duty cycle of IMO	–	40	50	60	%
DC_{ILO}	Internal low speed oscillator duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	V_{DD} slew rate during power-up	–	–	250	V/ms
t_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t_{XRST2}	External reset pulse width after power-up[11]	Applies after part has booted	10	–	–	µs

AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, Port 1.	0	–	12 MHz for 3 V < Vdd < 5.5 V	MHz
TRise23	Rise time, strong mode, Cload = 50 pF, Ports 2 or 3	Vdd = 3.0 to 3.6 V, 10%–90%	15	–	80	ns
TRise01	Rise time, strong mode, Cload = 50 pF, Ports 0 or 1	Vdd = 3.0 to 3.6 V, 10%–90%. LDO enabled or disabled.	10	–	50	ns
TFall	Fall time, strong mode, Cload = 50 pF, All ports	Vdd = 3.0 to 3.6 V, 10%–90%	10	–	50	ns

Note

11. The minimum required XRES pulse length is longer when programming the device (see Table 22 on page 24).

Figure 8. GPIO Timing Diagram

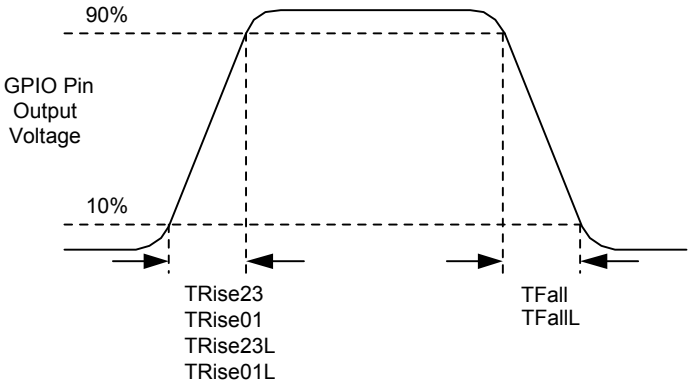


Table 15. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	–18.5	–	18.5	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	–9	–	9	ns
Tudj1	Driver differential jitter	To next transition	–3.5	–	3.5	ns
Tudj2	Driver differential jitter	To pair transition	–4.0	–	4.0	ns
Tfdeop	Source jitter for differential transition	To SE0 transition	–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–		ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns

Table 16. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR	Rise/fall time matching		90.00	–	111.1	%
Vcrs	Output signal crossover voltage		1.3	–	2.0	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{LPC}	Comparator response time, 50 mV Overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

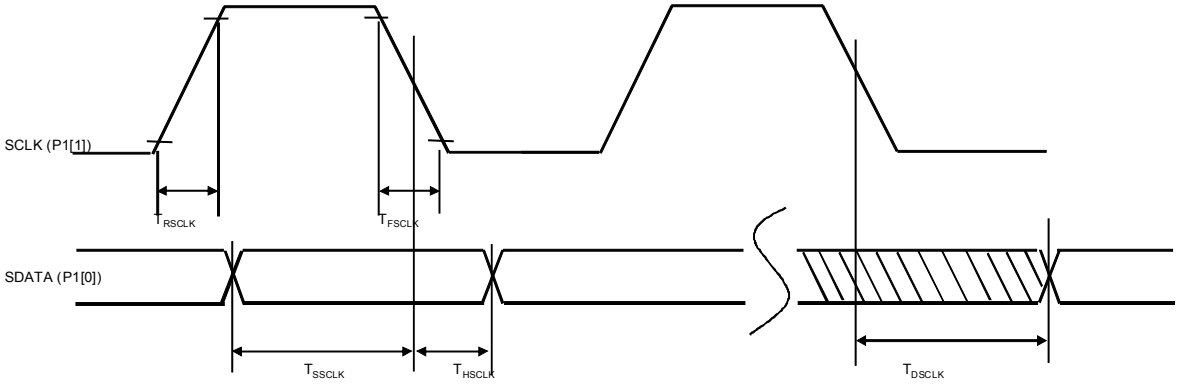
AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.75	–	25.20	MHz
–	High period		20.60	–	5300	ns
–	Low period		20.60	–	–	ns
–	Power up IMO to switch		150	–	–	µs

Figure 9. AC Waveform



AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK		1	–	20	ns
T_{FSCLK}	Fall time of SCLK		1	–	20	ns
T_{SSCLK}	Data setup time to falling edge of SCLK		40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash erase time (block)		–	–	18	ms
T_{WRITE}	Flash block write time		–	–	25	ms
T_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \le V_{DD} \le 3.0$	–	–	130	ns
T_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
T_{XRST3}	External reset pulse width after power up	Required to enter programming mode when coming out of sleep	263	–	–	µs
T_{XRES}	XRES pulse length		300	–	–	µs
$T_{VDDWAIT}$	V_{DD} stable to wait-and-poll hold off		0.1	–	1	ms

Table 19. AC Programming Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{VDDXRES}$	V_{DD} stable to XRES assertion delay		14.27	–	–	ms
T_{POLL}	SDATA high pulse time		0.01	–	200	ms
T_{ACQ}	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.		3.20	–	19.60	ms
$T_{XRESINI}$	“Key window” time after an XRES event, based on 8 ILO clocks		98	–	615	µs

AC SPI Specifications

Table 20. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 3$ V	–		6	MHz
DC	SCLK duty cycle		–	50	–	%
T_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 3$ V	60	–	–	ns
T_{HOLD}	SCLK to MISO hold time		40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
T_{OUT_HIGH}	MOSI high time		40	–	–	ns

Figure 10. SPI Master Mode 0 and 2

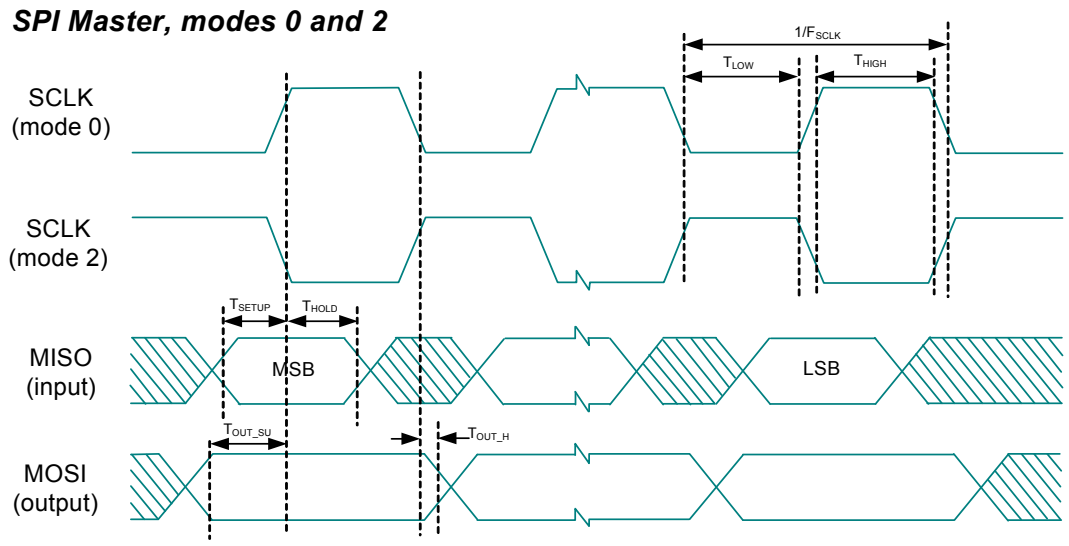


Figure 11. SPI Master Mode 1 and 3

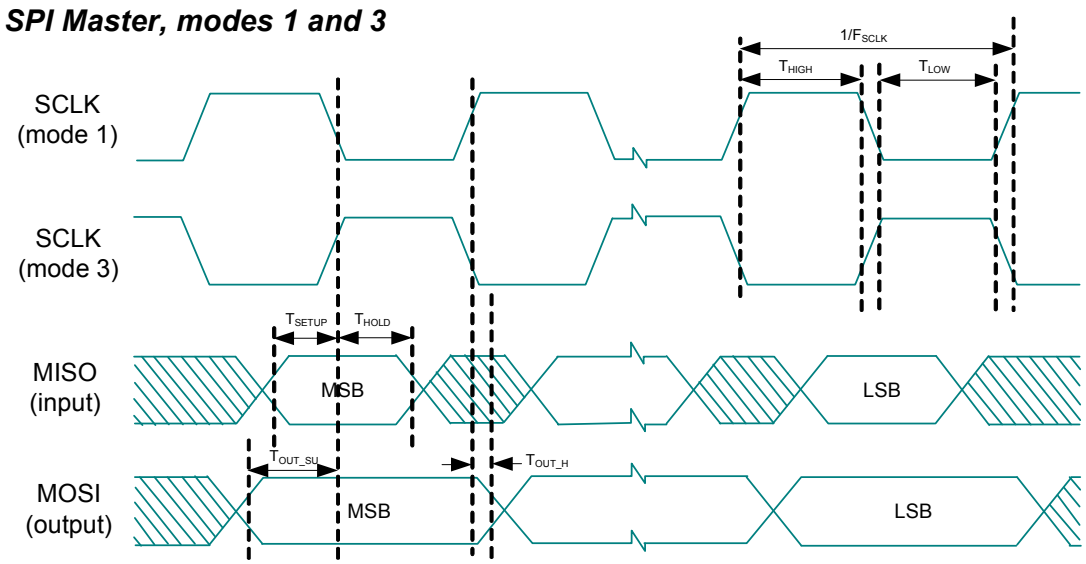


Table 21. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 3$ V	–	–	12	MHz
T_{LOW}	SCLK low time		42	–	–	ns
T_{HIGH}	SCLK high time		42	–	–	ns
T_{SETUP}	MOSI to SCLK setup time		30	–	–	ns
T_{HOLD}	SCLK to MOSI hold time		50	–	–	ns
T_{SS_MISO}	SS high to MISO valid		–	–	153	ns
T_{SCLK_MISO}	SCLK to MISO valid		–	–	125	ns
T_{SS_HIGH}	SS high time		50	–	–	ns
T_{SS_CLK}	Time from SS low to first SCLK		2/SCLK	–	–	ns
T_{CLK_SS}	Time from last SCLK to SS high		2/SCLK	–	–	ns

Figure 12. SPI Slave Mode 0 and 2

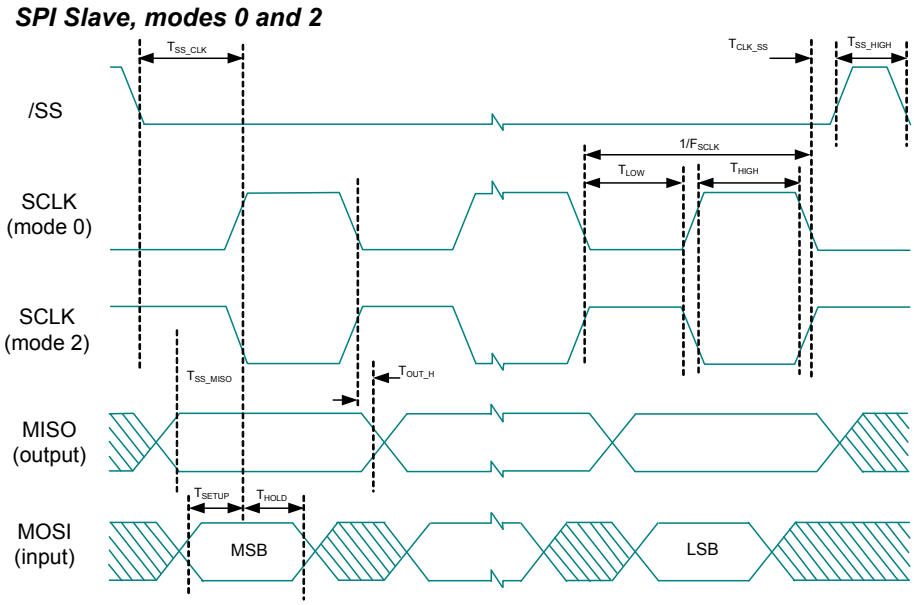
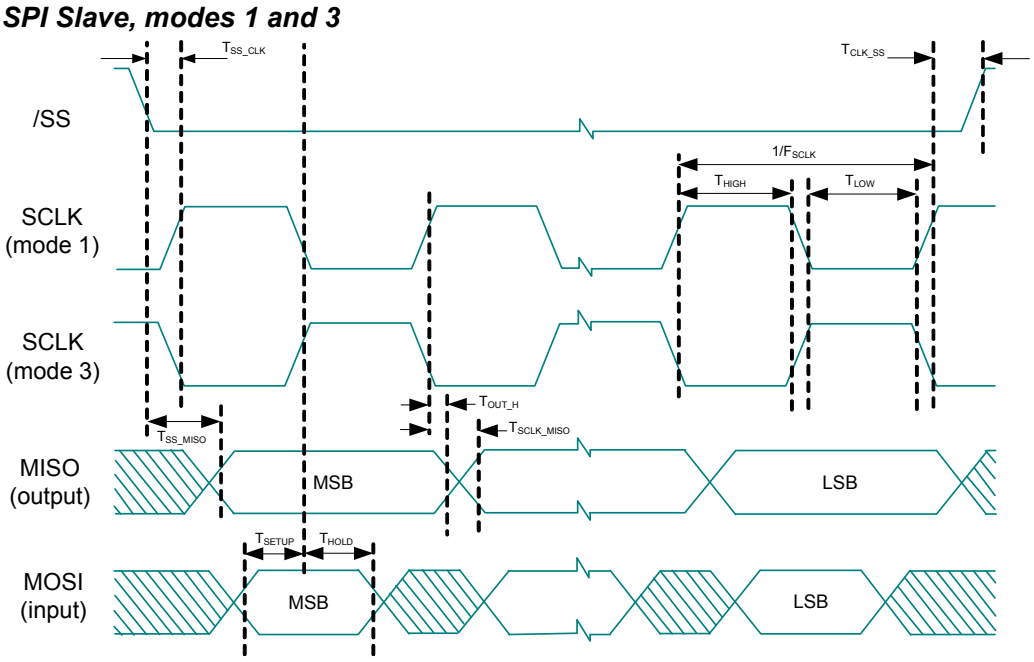


Figure 13. SPI Slave Mode 1 and 3



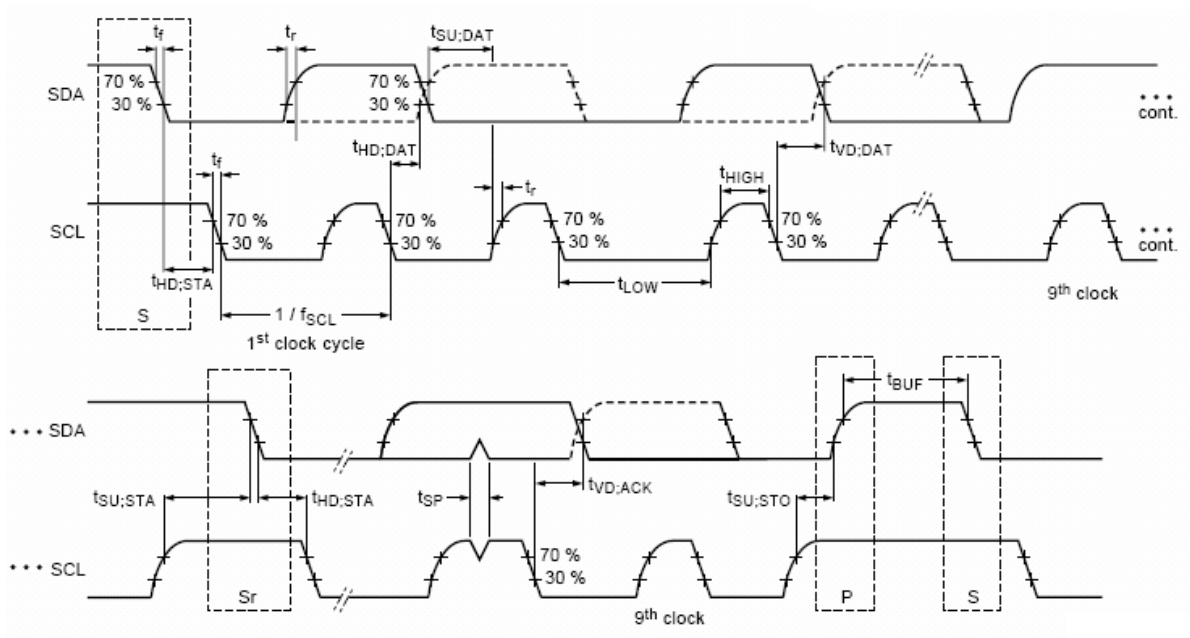
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Conditions	Standard Mode		Fast Mode		Units
			Min	Max	Min	Max	
f_{SCLI2C}	SCL clock frequency		0	100	0	400	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0	–	0.6	–	µs
t_{LOWI2C}	LOW period of the SCL clock		4.7	–	1.3	–	µs
$t_{HIGHI2C}$	HIGH period of the SCL clock		4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition		4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time		0	3.45	0	0.90	µs
$t_{SUDATI2C}$	Data setup time		250	–	100[12]	–	ns
$t_{SUSTOI2C}$	Setup time for STOP Condition		4.0	–	0.6	–	µs
t_{BUFI2C}	Bus free time between a STOP and START Condition		4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.		–	–	0	50	ns

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

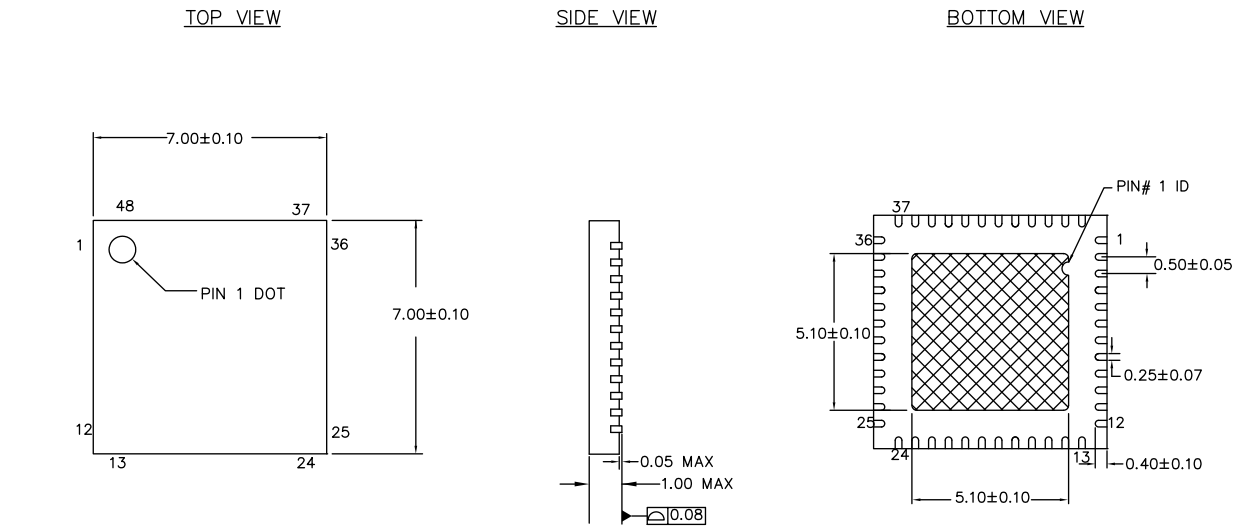
12. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY7C69356 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR1016

Figure 15. 48-pin QFN (7 × 7 × 1.0 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *H

Important Note

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 23. Thermal Impedances per Package

Package	Typical θ_{JA} [13]
48-pin QFN [14]	18 °C/W

Capacitance on Crystal Pins

Table 24. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
48-pin QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 25. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [15]	Maximum Peak Temperature
48-pin QFN	240 °C	260 °C

Notes

13. $T_J = T_A + \text{Power} \times \theta_{JA}$.
14. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
15. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for the CY7C69356 family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Used by thousands of PSoC developers, this robust software has made designing with PSoC easy for half a decade. TrueTouch products require a dedicated PSoC Designer installer. Contact your local sales representative or send your request to tsbusdev@cypress.com.

PSoC Programmer

PSoC Programmer is flexible enough to be used on the bench in development, yet suitable for factory programming. It works as a standalone programming application, or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

Development Kits

Under development.

Device Programmers

All device programmers are available for purchase from The Cypress Store. For programming during development, use:

- MiniProg1 Programming Unit (does not support debug monitor). It is available for purchase through the Cypress online store as part of kit:CY3210-MiniProg1.
- MiniProg3 Programming Unit (supports debug monitor). It is available for purchase through the Cypress online store as part of kit:CY8CKIT-002.

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

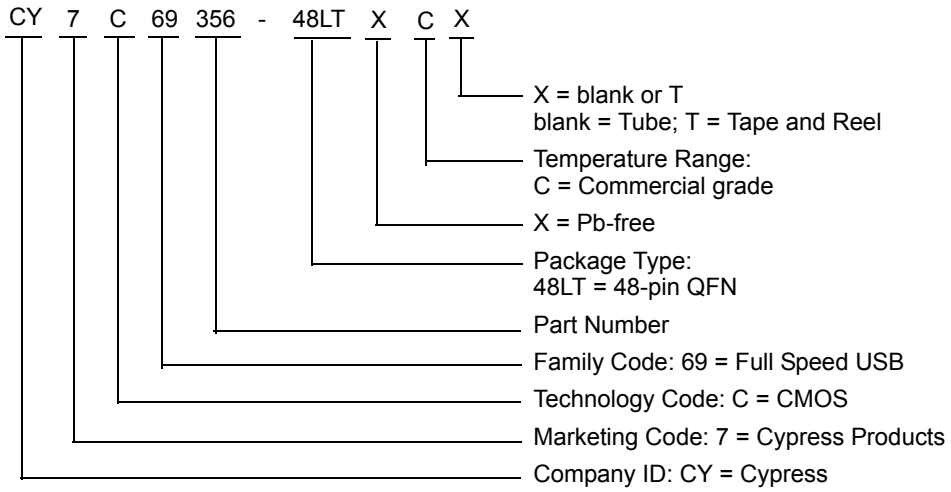
Ordering Information

The following table lists the CY7C69356 PSoC devices key package features and ordering codes.

Table 26. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (KB)	SRAM (Bytes)	TrueTouch Blocks	Digital I/O Pins	Analog Inputs	XRES Pin	USB
48-pin (7 × 7 mm) QFN	CY7C69356-48LTXC	32	2048	1	36	36[16]	Yes	Yes

Ordering Code Definitions



Notes
16. Dual-function Digital I/O pins also connect to the common analog mux.
17. This part may be used for in-circuit debugging. It is NOT available for production.

Acronyms

Table 27. Acronyms used

Acronym	Description
AC	alternating current
API	application programming interface
CPU	central processing unit
DC	direct current
GPIO	general purpose I/O
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip
SLIMO	slow IMO
SRAM	static random access memory
FSR	full scale range

Document Conventions

Units of Measure

Table 28. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolts
µVrms	microvolts root-mean-square
ksps	kilo samples per second
µW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volts

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers are also represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Document History Page

Document Title: CY7C69356, TrueTouch® Multi-Touch Gesture Full Speed USB Controller Document Number: 001-86334				
Revision	**ECN #**	**Origin of Change**	**Submission Date**	**Description of Change**
*B	5222044	SKUV	04/15/2016	Changed status from Preliminary to Final.

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