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General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex™-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC 4000 product family is the smallest member of the PSoC 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CapSense) with best-in-class performance, and general-purpose analog. PSoC 4000 products will be fully upward compatible with members of the PSoC 4 platform for new applications and design needs.

Features

32-bit MCU Subsystem

- 16-MHz Arm Cortex-M0 CPU
- Up to 16 KB of flash with Read Accelerator
- Up to 2 KB of SRAM

Programmable Analog

- Two current DACs (IDACs) for general-purpose or capacitive sensing applications
- One low-power comparator with internal reference
- Limited ADC function provided by capacitance sensing block

Low Power 1.71-V to 5.5-V operation

- Deep Sleep mode with wake-up on interrupt and I²C address detect

Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class signal-to-noise ratio (SNR) and water tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™) over a sensor range of 5 pF to 45 pF

Serial Communication

- Multi-master I²C block with the ability to do address matching during Deep Sleep and generate a wake-up on match

Timing and Pulse-Width Modulation

- One 16-bit timer/counter/pulse-width modulator (TCPWM) block
- Center-aligned, Edge, and Pseudo-Random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Up to 20 Programmable GPIO Pins

- 28-pin SSOP, 24-pin QFN, 16-pin SOIC, 16-pin QFN, 16 ball WLCSP, and 8-pin SOIC packages
- GPIO pins on Ports 0, 1, and 2 can be CapSense or have other functions
- Drive modes, strengths, and slew rates are programmable

PSoC Creator Design Environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API) component for all fixed-function and programmable peripherals

Industry-Standard Tool Compatibility

- After schematic entry, development can be done with Arm-based industry-standard development tools

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
 In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): Arm Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
 - CY8CKIT-040, PSoC 4000 Pioneer Kit, is an easy-to-use and inexpensive development platform with debugging capability. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
 - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

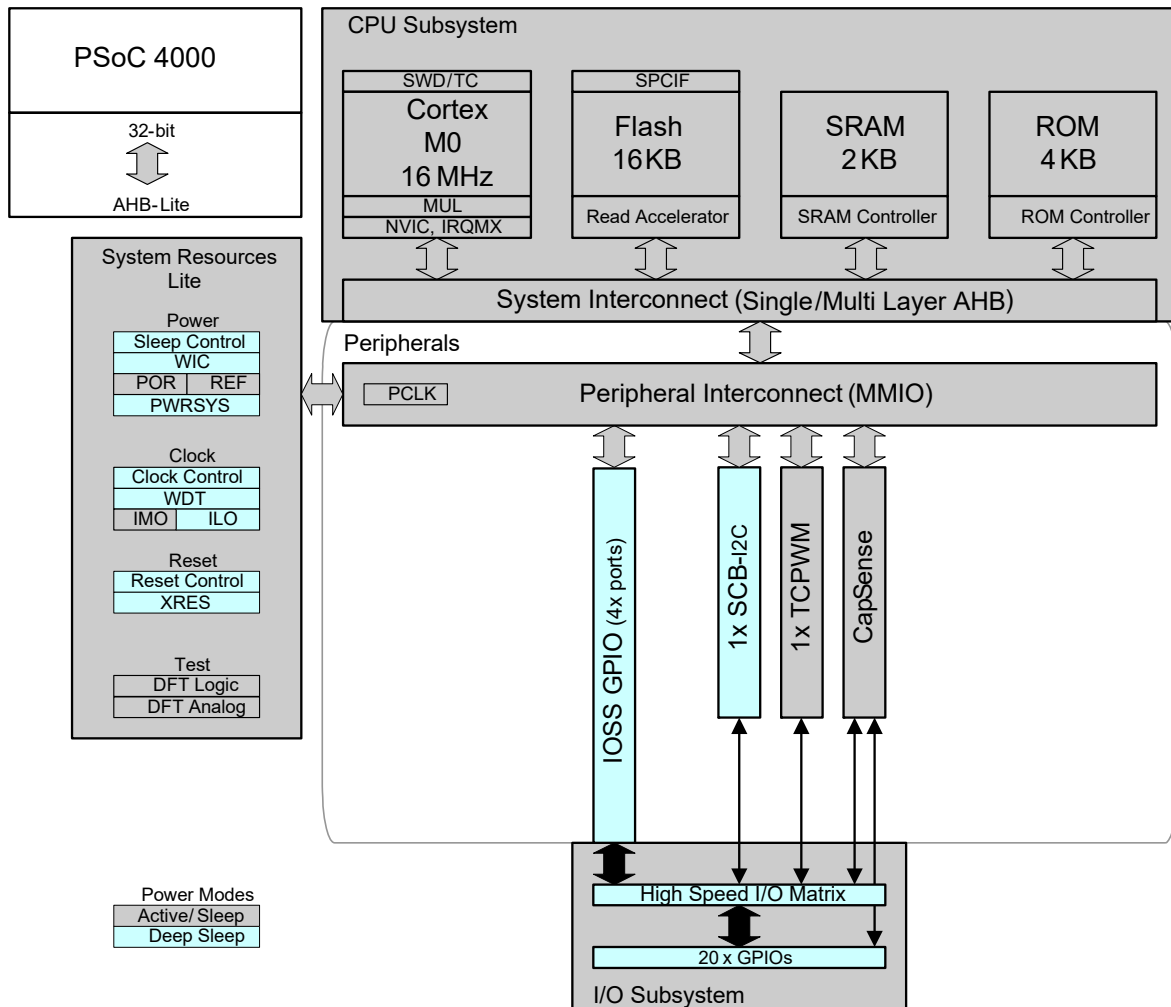
[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Example Project in PSoC Creator

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Figure 2. Block Diagram


PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4000 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. This enables fully compatible, binary, upward migration of the code to higher performance processors, such as the Cortex-M3 and M4. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The CPU subsystem also includes a 24-bit timer called SYSTICK, which can generate an interrupt.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC 4000 has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4000 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver zero wait-state (WS) access time at 16 MHz.

SRAM

Two KB of SRAM are provided with zero wait-state access at 16 MHz.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section on [Power on page 12](#). It provides an assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000 operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000 provides Active, Sleep, and Deep Sleep low-power modes.

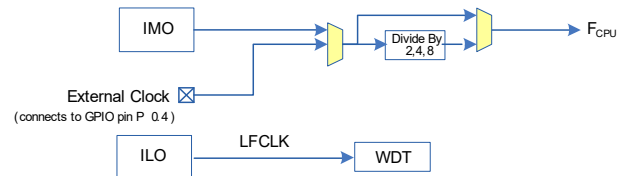
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ S.

Clock System

The PSoC 4000 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000 consists of the internal main oscillator (IMO) and the internal low-frequency oscillator (ILO) and provision for an external clock.

Figure 3. PSoC 4000 MCU Clocking Architecture



The F_{CPU} signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are four clock dividers for the PSoC 4000, each with 16-bit divide capability. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz. It can be adjusted to 24 or 32 MHz. The IMO tolerance with Cypress-provided calibration settings is \pm 2% (24 and 32 MHz).

ILO Clock Source

The ILO is a very low power, 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4000 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset on the 24-pin package. An internal POR is provided on the 16-pin and 8-pin packages. The XRES pin has an internal pull-up resistor that is always enabled. Reset is Active Low.

Voltage Reference

The PSoC 4000 reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a \pm 5% reference.

Analog Blocks

Low-power Comparators

The PSoC 4000 has a low-power comparator, which uses the built-in voltage reference. Any one of up to 16 pins can be used as a comparator input and the output of the comparator can be brought out to a pin. The selected comparator input is connected to the minus input of the comparator with the plus input always connected to the 1.2-V voltage reference. This comparator is also used for CapSense purposes and is not available during CapSense operation.

Current DACs

The PSoC 4000 has two IDACs, which can drive any of up to 16 pins on the chip and have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4000 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on Ports 0, 1, and 2.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention.

Serial Communication Block (SCB)

The PSoC 4000 has a serial communication block, which implements a multi-master I²C interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI²C that creates a mailbox address range in the memory of the PSoC 4000 and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000 is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast-mode minimum fall time is not met in Fast Strong mode; Slow Strong mode can help meet this spec depending on the Bus Load.

GPIO

The PSoC 4000 has up to 20 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for PSoC 4000).

The 28-pin and 24-pin packages have 20 GPIOs. The 16-pin SOIC has 13 GPIOs. The 16-pin QFN and the 16-ball WLCSP have 12 GPIOs. The 8-pin SOIC has 5 GPIOs.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4000 through a CSD block that can be connected to up to 16 pins through an analog mux bus via an analog switch (pins on Port 3 are not available for CapSense purposes). CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block can also be re-purposed to implement a limited ADC function, which is only available when not using the block for capacitive sensing.



Pinouts

All port pins support GPIO. Ports 0, 1, and 2 support CSD CapSense and analog multiplexed bus connections. TCPWM functions and Alternate Functions are supported on port pins as follows for the five PSoc 4000 packages.

Table 1. Pin Descriptions

| 28-Pin SSOP | | 24-Pin QFN | | 16-Pin QFN | | 16-Pin SOIC | | 8-Pin SOIC | | TCPWM |
|-------------|-------------------------------------|------------|-------------------------------------|------------|---------------------------------|-------------|---------------------------------|------------|---------------------------------|-------------------------------------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | |
| 20 | VSS | | | | | | | | | |
| 21 | P0.0/TRIN0 | 1 | P0.0/TRIN0 | | | | | | | TRIN0: Trig 0 |
| 22 | P0.1/TRIN1/CMPO _0 | 2 | P0.1/TRIN1/CMPO _0 | 1 | P0.1/TRIN1/CMPO _0 | 3 | P0.1/TRIN1/CMPO _0 | | | TRIN1: Trig 1 |
| 23 | P0.2/TRIN2 | 3 | P0.2/TRIN2 | 2 | P0.2/TRIN2 | 4 | P0.2/TRIN2 | | | TRIN2: Trig 2 |
| 24 | P0.3/TRIN3 | 4 | P0.3/TRIN3 | | | | | | | TRIN3: Trig 3 |
| 25 | P0.4/TRIN4/CMPO _0/EXT_CLK | 5 | P0.4/TRIN4/CMPO _0/EXT_CLK | 3 | P0.4/TRIN4/CMPO _0/EXT_CLK | 5 | P0.4/TRIN4/CMPO _0/EXT_CLK | 2 | P0.4/TRIN4/CMPO _0/EXT_CLK | TRIN4: Trig 4 |
| 26 | VCCD | 6 | VCCD | 4 | VCCD | 6 | VCCD | 3 | VCCD | |
| 27 | VDD | 7 | VDD | 6 | VDD | 7 | VDD | 4 | VDD | |
| 28 | VSS | 8 | VSS | 7 | VSS | 8 | VSS | 5 | VSS | |
| 1 | P0.5 | 9 | P0.5 | 5 | VDDIO | 9 | P0.5 | | | |
| 2 | P0.6 | 10 | P0.6 | 8 | P0.6 | 10 | P0.6 | | | |
| 3 | P0.7 | 11 | P0.7 | | | | | | | |
| 4 | P1.0 | 12 | P1.0 | | | | | | | |
| 5 | P1.1/OUT0 | 13 | P1.1/OUT0 | 9 | P1.1/OUT0 | 11 | P1.1/OUT0 | 6 | P1.1/OUT0 | OUT0: PW |
| 6 | P1.2/SCL | 14 | P1.2/SCL | 10 | P1.2/SCL | 12 | P1.2/SCL | | | |
| 7 | P1.3/SDA | 15 | P1.3/SDA | 11 | P1.3/SDA | 13 | P1.3/SDA | | | |
| 8 | P1.4/UND0 | 16 | P1.4/UND0 | | | | | | | UND0: Un Ou |
| 9 | P1.5/OVF0 | 17 | P1.5/OVF0 | | | | | | | OVF0: Ove |
| 10 | P1.6/OVF0/UND0/n OUT0 /CMPO_0 | 18 | P1.6/OVF0/UND0/n OUT0 /CMPO_0 | 12 | P1.6/OVF0/UND0/n OUT0/CMPO_0 | 14 | P1.6/OVF0/UND0/n OUT0/CMPO_0 | 7 | P1.6/OVF0/UND0/n OUT0/CMPO_0 | nOU Comple OUT0, U OVF0 as |

Note

1. Must not have load to ground during POR (should be an output).



Table 1. Pin Descriptions (continued)

| 28-Pin SSOP | | 24-Pin QFN | | 16-Pin QFN | | 16-Pin SOIC | | 8-Pin SOIC | | TCPWM 3 |
|-------------|--------------------------------|------------|--------------------|------------|--------------------|-------------|--------------------|------------|------------------|----------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | |
| 11 | VSS | | | | | | | | | |
| 12 | No Connect (NC) ^[2] | | | | | | | | | |
| 13 | P1.7/MATCH/EXT_CLK | 19 | P1.7/MATCH/EXT_CLK | 13 | P1.7/MATCH/EXT_CLK | 15 | P1.7/MATCH/EXT_CLK | | | MATCH: M |
| 14 | P2.0 | 20 | P2.0 | | | 16 | P2.0 | | | |
| 15 | VSS | | | | | | | | | |
| 16 | P3.0/SDA/SWD_IO | 21 | P3.0/SDA/SWD_IO | 14 | P3.0/SDA/SWD_IO | 1 | P3.0/SDA/SWD_IO | 8 | P3.0/SDA/SWD_IO | |
| 17 | P3.1/SCL/SWD_CLK | 22 | P3.1/SCL/SWD_CLK | 15 | P3.1/SCL/SWD_CLK | 2 | P3.1/SCL/SWD_CLK | 1 | P3.1/SCL/SWD_CLK | |
| 18 | P3.2 | 23 | P3.2 | 16 | P3.2 | | | | | OUT0:PW |
| 19 | XRES | 24 | XRES | | | | | | | |

Descriptions of the Pin functions are as follows:

VDD: Power supply for both analog and digital sections.

VDDIO: Where available, this pin provides a separate voltage domain (see the [Power](#) section for details).

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V ±5%).

Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense or shield pins connected to AMUXBUS A or B. They can also be used as the firmware, in addition to their alternate functions listed in the [Table 1](#).

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

The following packages are provided: 28-pin SSOP, 24-pin QFN, 16-pin QFN, 16-pin SOIC, and 8-pin SOIC.

Note

- This pin is not to be used; it must be left floating.

Figure 4. 28-Pin SSOP Pinout

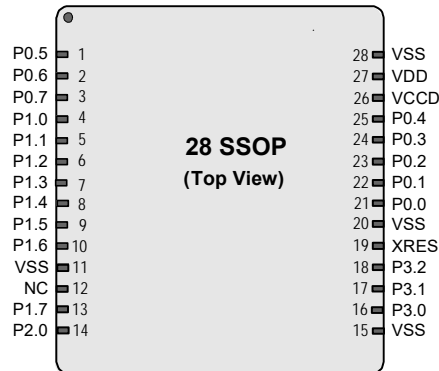


Figure 5. 24-pin QFN Pinout

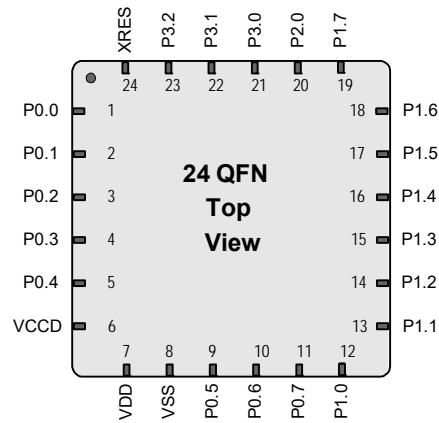


Figure 6. 16-Pin QFN Pinout

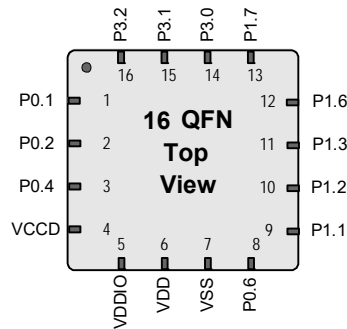


Figure 7. 16-Pin SOIC Pinout

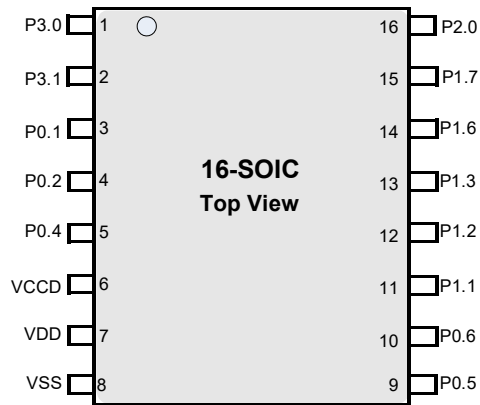


Figure 8. 8-Pin SOIC Pinout

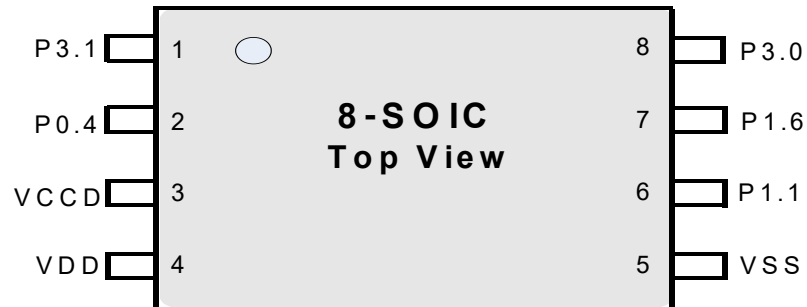
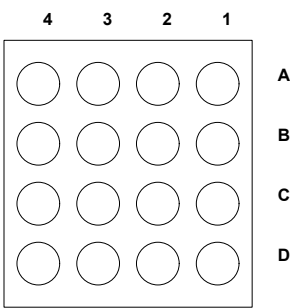
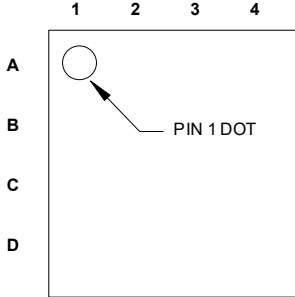


Table 2. 16-ball WLCSP Pin Descriptions and Diagram

| Pin | Name | TCPWM Signal | Alternate Functions | Pin Diagram |
|-----|---------------------------------|--------------------------------------|--|---|
| B4 | P3.2 | OUT0:PWMOUT0 | – | <p style="text-align: center;">Bottom View</p>  <p style="text-align: center;">Top View</p>  |
| C3 | P0.2/TRIN2 | TRIN2:Trigger Input 2 | – | |
| C4 | P0.4/TRIN4/CMPO_0/ EXT_CLK | TRIN4:Trigger Input 4 | CMPO_0: Sense Comp Out, Ext. Clock, CMOD Cap | |
| D4 | VCCD | – | – | |
| D3 | VDD | – | – | |
| D2 | VSS | – | – | |
| C2 | VDDIO | – | – | |
| D1 | P0.6 | – | – | |
| C1 | P1.1/OUT0 | OUT0:PWMOUT0 | – | |
| B1 | P1.2/SCL | – | I ² C Clock | |
| A1 | P1.3/SDA | – | I ² C Data | |
| A2 | P1.6/OVF0/UND0/nO UT0/CMPO_0 | nOUT0:Complement of OUT0, UND0, OVF0 | CMPO_0: Sense Comp Out, Internal Reset function ^[3] | |
| B2 | P1.7/MATCH/ EXT_CLK | MATCH: Match Out | External Clock | |
| A3 | P2.0 | – | – | |
| B3 | P3.0/SDA/SWD_IO | – | I ² C Data, SWD I/O | |
| A4 | P3.1/SCL/SWD_CLK | – | I ² C Clock, SWD Clock | |

Note

3. Must not have load to ground during POR (should be an output).

Power

The following power system diagrams (Figure 9 and Figure 10) show the set of power supply pins as implemented for the PSoC 4000. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V \pm 5% (externally regulated) or 1.8 V to 5.5 V (unregulated externally; regulated internally) with all functions and circuits operating over that range.

The V_{DDIO} pin, available in the 16-pin QFN package, provides a separate voltage domain for the following pins: P3.0, P3.1, and P3.2. P3.0 and P3.1 can be I²C pins and the chip can thus communicate with an I²C system, running at a different voltage (where $V_{DDIO} \leq V_{DD}$). For example, V_{DD} can be 3.3 V and V_{DDIO} can be 1.8 V.

The PSoC 4000 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

Unregulated External Supply

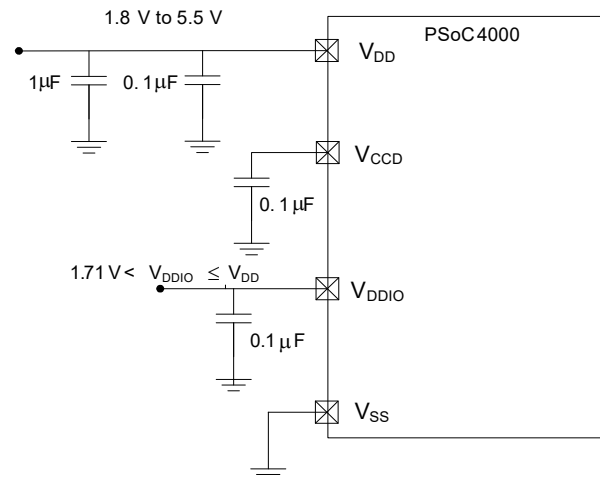
In this mode, the PSoC 4000 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000 supplies the internal logic and the V_{CCD} output of the PSoC 4000 must be bypassed to ground via an external capacitor (0.1 μ F; X5R ceramic or better). The bypass capacitor should be located as close as possible to the V_{CCD} pin.

Bypass capacitors must be used from V_{DD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μ F range, in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 9. 16-pin QFN Bypass Scheme Example - Unregulated External Supply

Power supply connections when $1.8 \leq V_{DD} \leq 5.5$ V



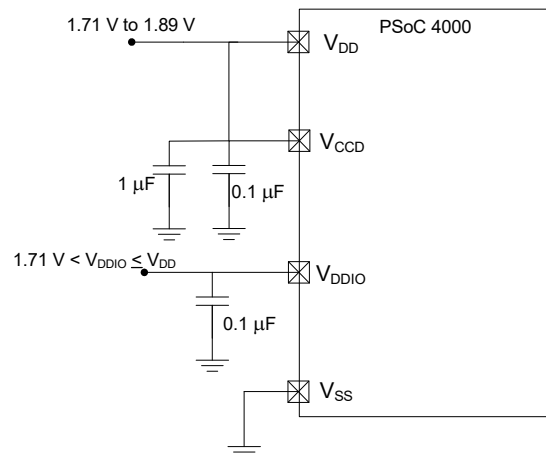
Regulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator should be disabled in the firmware. Note that in this mode V_{DD} (V_{CCD}) should never exceed 1.89 in any condition, including flash programming.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 10. 16-pin QFN Bypass Scheme Example - Regulated External Supply

Power supply connections when $1.71 \leq V_{DD} \leq 1.89$ V



Development Support

The PSoC 4000 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4000 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings^[4]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-----------------------------|---|------|-----|----------------------|-------|--------------------------|
| SID1 | V _{DD_ABS} | Digital supply relative to V _{SS} | -0.5 | - | 6 | V | |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SS} | -0.5 | - | 1.95 | V | |
| SID3 | V _{GPIO_ABS} | GPIO voltage | -0.5 | - | V _{DD} +0.5 | V | |
| SID4 | I _{GPIO_ABS} | Maximum current per GPIO | -25 | - | 25 | mA | |
| SID5 | I _{GPIO_injection} | GPIO injection current, Max for V _{IH} > V _{DD} , and Min for V _{IL} < V _{SS} | -0.5 | - | 0.5 | mA | Current injected per pin |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | - | - | V | |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | - | - | V | |
| BID46 | LU | Pin current for latch-up | -140 | - | 140 | mA | |

Device Level Specifications

All specifications are valid for -40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 4. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|--|--------------------|--|------|-----|-----------------|-------|-------------------------------|
| SID53 | V _{DD} | Power supply input voltage | 1.8 | - | 5.5 | V | With regulator enabled |
| SID255 | V _{DD} | Power supply input voltage (V _{CCD} = V _{DD}) | 1.71 | - | 1.89 | V | Internally unregulated supply |
| SID54 | V _{DDIO} | V _{DDIO} domain supply | 1.71 | - | V _{DD} | V | |
| SID55 | C _{EFC} | External regulator voltage (V _{CCD}) bypass | - | 0.1 | - | μF | X5R ceramic or better |
| SID56 | C _{EXC} | Power supply bypass capacitor | - | 1 | - | μF | X5R ceramic or better |
| Active Mode, V_{DD} = 1.8 to 5.5 V | | | | | | | |
| SID9 | I _{DD5} | Execute from flash; CPU at 6 MHz | - | 2.0 | 2.85 | mA | |
| SID12 | I _{DD8} | Execute from flash; CPU at 12 MHz | - | 3.2 | 3.75 | mA | |
| SID16 | I _{DD11} | Execute from flash; CPU at 16 MHz | - | 4.0 | 4.5 | mA | |
| Sleep Mode, V_{DD} = 1.71 to 5.5 V | | | | | | | |
| SID25 | I _{DD20} | I ² C wakeup, WDT on. 6 MHz | - | 1.1 | - | mA | |
| SID25A | I _{DD20A} | I ² C wakeup, WDT on. 12 MHz | - | 1.4 | - | mA | |
| Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V (Regulator on) | | | | | | | |
| SID31 | I _{DD26} | I ² C wakeup and WDT on | - | 2.5 | 8.2 | μA | |

Note

4. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 4. DC Specifications (continued)

 Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|--------------|------------------------------------|-----|-----|-----|-------|------------------------|
| Deep Sleep Mode, $V_{DD} = 3.6$ to 5.5 V (Regulator on) | | | | | | | |
| SID34 | I_{DD29} | I ² C wakeup and WDT on | – | 2.5 | 12 | μA | |
| Deep Sleep Mode, $V_{DD} = V_{CCD} = 1.71$ to 1.89 V (Regulator bypassed) | | | | | | | |
| SID37 | I_{DD32} | I ² C wakeup and WDT on | – | 2.5 | 9.2 | μA | |
| XRES Current | | | | | | | |
| SID307 | I_{DD_XR} | Supply current while XRES asserted | – | 2 | 5 | mA | |

Table 5. AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------------------|-----------------|-----------------------------|-----|-----|-----|-------|-----------------------------|
| SID48 | F_{CPU} | CPU frequency | DC | – | 16 | MHz | $1.71 \leq V_{DD} \leq 5.5$ |
| SID49 ^[5] | T_{SLEEP} | Wakeup from Sleep mode | – | 0 | – | μs | |
| SID50 ^[5] | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | 35 | – | μs | |

GPIO
Table 6. GPIO DC Specifications (referenced to V_{DDIO} for 16-Pin QFN V_{DDIO} pins)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-------------------------|---|---------------------|-----|---------------------|-------|--|
| SID57 | V_{IH} ^[6] | Input voltage high threshold | $0.7 \times V_{DD}$ | – | – | V | CMOS Input |
| SID58 | V_{IL} | Input voltage low threshold | – | – | $0.3 \times V_{DD}$ | V | CMOS Input |
| SID241 | V_{IH} ^[6] | LVTTL input, $V_{DD} < 2.7\text{ V}$ | $0.7 \times V_{DD}$ | – | – | V | |
| SID242 | V_{IL} | LVTTL input, $V_{DD} < 2.7\text{ V}$ | – | – | $0.3 \times V_{DD}$ | V | |
| SID243 | V_{IH} ^[6] | LVTTL input, $V_{DD} \geq 2.7\text{ V}$ | 2.0 | – | – | V | |
| SID244 | V_{IL} | LVTTL input, $V_{DD} \geq 2.7\text{ V}$ | – | – | 0.8 | V | |
| SID59 | V_{OH} | Output voltage high level | $V_{DD} - 0.6$ | – | – | V | $I_{OH} = 4\text{ mA}$ at $3\text{ V } V_{DD}$ |
| SID60 | V_{OH} | Output voltage high level | $V_{DD} - 0.5$ | – | – | V | $I_{OH} = 1\text{ mA}$ at $1.8\text{ V } V_{DD}$ |
| SID61 | V_{OL} | Output voltage low level | – | – | 0.6 | V | $I_{OL} = 4\text{ mA}$ at $1.8\text{ V } V_{DD}$ |
| SID62 | V_{OL} | Output voltage low level | – | – | 0.6 | V | $I_{OL} = 10\text{ mA}$ at $3\text{ V } V_{DD}$ |
| SID62A | V_{OL} | Output voltage low level | – | – | 0.4 | V | $I_{OL} = 3\text{ mA}$ at $3\text{ V } V_{DD}$ |
| SID63 | R_{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID65 | I_{IL} | Input leakage current (absolute value) | – | – | 2 | nA | $25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$ |
| SID66 | C_{IN} | Input capacitance | – | 3 | 7 | pF | |

Notes

- Guaranteed by characterization.
- V_{IH} must not exceed $V_{DD} + 0.2\text{ V}$.

Table 6. GPIO DC Specifications (referenced to V_{DDIO} for 16-Pin QFN V_{DDIO} pins) (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|-----------------------|------------------|---|----------------------|-----|-----|---------|------------------------|
| SID67 ^[7] | V_{HYSTTL} | Input hysteresis LVTTTL | 15 | 40 | – | mV | $V_{DD} \geq 2.7$ V |
| SID68 ^[7] | $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 \times V_{DD}$ | – | – | mV | $V_{DD} < 4.5$ V |
| SID68A ^[7] | $V_{HYSCMOS5V5}$ | Input hysteresis CMOS | 200 | – | – | mV | $V_{DD} > 4.5$ V |
| SID69 ^[7] | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | – | – | 100 | μ A | |
| SID69A ^[7] | I_{TOT_GPIO} | Maximum total source or sink chip current | – | – | 85 | mA | |

Table 7. GPIO AC Specifications

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|---------------|--|-----|-----|-----|-------|--|
| SID70 | T_{RISEF} | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V V_{DD} , Cload = 25 pF |
| SID71 | T_{FALLF} | Fall time in fast strong mode | 2 | – | 12 | ns | 3.3 V V_{DD} , Cload = 25 pF |
| SID72 | T_{RISES} | Rise time in slow strong mode | 10 | – | 60 | – | 3.3 V V_{DD} , Cload = 25 pF |
| SID73 | T_{FALLS} | Fall time in slow strong mode | 10 | – | 60 | – | 3.3 V V_{DD} , Cload = 25 pF |
| SID74 | $F_{GPIOUT1}$ | GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V. Fast strong mode. | – | – | 16 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | $F_{GPIOUT2}$ | GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V. Fast strong mode. | – | – | 16 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | $F_{GPIOUT3}$ | GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V. Slow strong mode. | – | – | 7 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | $F_{GPIOUT4}$ | GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V. Slow strong mode. | – | – | 3.5 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | F_{GPIOIN} | GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5$ V | – | – | 16 | MHz | 90/10% V_{IO} |

Note

7. Guaranteed by characterization.

XRES

Table 8. XRES DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------------------|----------------------|------------------------------|-----------------------|-----------------------|-----------------------|-------|---|
| SID77 | V _{IH} | Input voltage high threshold | 0.7 × V _{DD} | – | – | V | CMOS Input |
| SID78 | V _{IL} | Input voltage low threshold | – | – | 0.3 × V _{DD} | V | CMOS Input |
| SID79 | R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID80 | C _{IN} | Input capacitance | – | 3 | 7 | pF | |
| SID81 ^[8] | V _{HYSXRES} | Input voltage hysteresis | – | 0.05* V _{DD} | – | mV | Typical hysteresis is 200 mV for V _{DD} > 4.5V |

Table 9. XRES AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|------------------------|-------------------------|---------------------------------|-----|-----|-----|-------|------------------------|
| SID83 ^[8] | T _{RESETWIDTH} | Reset pulse width | 5 | – | – | μs | |
| BID#194 ^[8] | T _{RESETWAKE} | Wake-up time from reset release | – | – | 3 | ms | |

Analog Peripherals

Comparator

Table 10. Comparator DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|-----------------------|-----------------------|---------------------------------------|-------|-----|-------|-------|--|
| SID330 ^[8] | I _{CMP1} | Block current, High Bandwidth mode | – | – | 110 | μA | |
| SID331 ^[8] | I _{CMP2} | Block current, Low Power mode | – | – | 85 | μA | |
| SID332 ^[8] | V _{OFFSET1} | Offset voltage, High Bandwidth mode | – | 10 | 30 | mV | |
| SID333 ^[8] | V _{OFFSET2} | Offset voltage, Low Power mode | – | 10 | 30 | mV | |
| SID334 ^[8] | Z _{CMP} | DC input impedance of comparator | 35 | – | – | MΩ | |
| SID338 ^[8] | V _{INP_COMP} | Comparator input range | 0 | – | 3.6 | V | Max input voltage is lower of 3.6 V or V _{DD} |
| SID339 | V _{REF_COMP} | Comparator internal voltage reference | 1.188 | 1.2 | 1.212 | V | |

Note

8. Guaranteed by characterization.

Table 11. Comparator AC Specifications (Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|-----------------------|--------------------|--|-----|-----|-----|-------|------------------------|
| SID336 ^[8] | T _{COMP1} | Response Time High Bandwidth mode, 50-mV overdrive | – | – | 90 | ns | |
| SID337 ^[8] | T _{COMP2} | Response Time Low Power mode, 50-mV overdrive | – | – | 110 | ns | |

CSD

Table 12. CSD and IDAC Block Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|------------------------------------|--------------------------|--|------|-------|-----------------------|-------|---|
| CSD and IDAC Specifications | | | | | | | |
| SYS.PER#3 | VDD_RIPPLE | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | VDD > 2V (with ripple), 25 °C T _A , Sensitivity = 0.1 pF |
| SYS.PER#16 | VDD_RIPPLE_1.8 | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | VDD > 1.75V (with ripple), 25 °C T _A , Parasitic Capacitance (C _P) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD#15 | VREFHI | Reference Buffer Output | 1.1 | 1.2 | 1.3 | V | |
| SID.CSD#16 | IDAC1IDD | IDAC1 (8-bits) block current | – | – | 1125 | µA | |
| SID.CSD#17 | IDAC2IDD | IDAC2 (7-bits) block current | – | – | 1125 | µA | |
| SID308 | V _{CSD} | Voltage range of operation | 1.71 | – | 5.5 | V | 1.8 V ±5% or 1.8 V to 5.5 V |
| SID308A | VCOMPIDAC | Voltage compliance range of IDAC | 0.8 | – | V _{DD} – 0.8 | V | |
| SID309 | IDAC1 _{DNL} | DNL for 8-bit resolution | –1 | – | 1 | LSB | |
| SID310 | IDAC1 _{INL} | INL for 8-bit resolution | –3 | – | 3 | LSB | |
| SID311 | IDAC2 _{DNL} | DNL for 7-bit resolution | –1 | – | 1 | LSB | |
| SID312 | IDAC2 _{INL} | INL for 7-bit resolution | –3 | – | 3 | LSB | |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | – | – | Ratio | Capacitance range of 9 to 35 pF, 0.1 pF sensitivity |
| SID314 | IDAC1 _{CRT1} | Output current of IDAC1 (8 bits) in high range | – | 612 | – | µA | |
| SID314A | IDAC1 _{CRT2} | Output current of IDAC1(8 bits) in low range | – | 306 | – | µA | |
| SID315 | IDAC2 _{CRT1} | Output current of IDAC2 (7 bits) in high range | – | 304.8 | – | µA | |
| SID315A | IDAC2 _{CRT2} | Output current of IDAC2 (7 bits) in low range | – | 152.4 | – | µA | |
| SID320 | IDAC _{OFFSET} | All zeroes input | – | – | ±1 | LSB | |
| SID321 | IDAC _{GAIN} | Full-scale error less offset | – | – | ±10 | % | |
| SID322 | IDAC _{MISMATCH} | Mismatch between IDACs | – | – | 7 | LSB | |
| SID323 | IDAC _{SET8} | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID324 | IDAC _{SET7} | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

CSD ADC

All characterization is done with a 0.1% tolerance 1-M Ω input resistor (R_{in}), 0.1% tolerance 220-K Ω bleed resistor (R_{bleed}), and 2.2-nF C_{mod} capacitor. Refer to this [page](#) for more details on the circuit.

Table 13. CSD ADC DC Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------|-------------------------|--|-----|-----|--------------------------------------|-------|
| ADC _{Res} | ADC resolution | | 1 | – | – | mV |
| ADC _{MONO} | ADC Monotonicity | Across PVT | – | – | – | Yes |
| ADC _{Error} | ADC gain error | For 0 to 5-V range, 0.1% accurate Rin / Rbleed, 1% accurate Internal Vref and Temp range of 0 to 70 °C | – | – | 1 | % |
| ADC _{Offset} | ADC offset error | | – | – | 50 | mV |
| ADC _{INMAX} | ADC input voltage range | | 0 | – | 5 / V _{DDIO} ^[9] | V |

Note: Inputs applied directly to a pin must not exceed V_{DDIO}, but voltages applied to an input resistor can exceed V_{DDIO}.

Table 14. CSD ADC AC Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---------------------|--------------------------------|-------------------------------|-----|-----|-----|-------|
| ADC _{INL} | ADC integral non-linearity | 0 to 5-V input and 0 to 70 °C | – | – | 18 | mV |
| ADC _{DNL} | ADC differential non-linearity | 0 to 5-V input and 0 to 70 °C | – | – | 12 | mV |
| ADC _{Samp} | ADC Sample rate | - | – | – | 58 | sps |

Note

9. Inputs applied directly to a pin must not exceed V_{DDIO}, but voltages applied to an input resistor can exceed V_{DDIO}.

Digital Peripherals
Timer Counter Pulse-Width Modulator (TCPWM)
Table 15. TCPWM Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|-----------------------|-------------------------------------|------------------|-----|----------------|-------|--|
| SID.TCPWM.1 | ITCPWM1 | Block current consumption at 3 MHz | – | – | 45 | μ A | All modes (TCPWM) |
| SID.TCPWM.2 | ITCPWM2 | Block current consumption at 8 MHz | – | – | 145 | μ A | All modes (TCPWM) |
| SID.TCPWM.2A | ITCPWM3 | Block current consumption at 16 MHz | – | – | 160 | μ A | All modes (TCPWM) |
| SID.TCPWM.3 | TCPWM _{FREQ} | Operating frequency | – | – | F _c | MHz | F _c max = CLK_SYS. Maximum = 16 MHz |
| SID.TCPWM.4 | TPWM _{ENEXT} | Input trigger pulse width | 2/F _c | – | – | ns | For all trigger events ^[10] |
| SID.TCPWM.5 | TPWM _{EXT} | Output trigger pulse widths | 2/F _c | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | TC _{RES} | Resolution of counter | 1/F _c | – | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM resolution | 1/F _c | – | – | ns | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | 1/F _c | – | – | ns | Minimum pulse width between Quadrature phase inputs. |

²C

Table 16. Fixed I²C DC Specifications^[11]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|-------------------|---|-----|-----|-----|-------|--------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | – | 25 | μA | |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 135 | μA | |
| SID.PWR#5 | ISBI2C | I ² C enabled in Deep Sleep mode | – | – | 2.5 | μA | |

Table 17. Fixed I²C AC Specifications^[11]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 400 | Kbps | |

Note

10. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
 11. Guaranteed by characterization.

Memory

Table 18. Flash DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------|---------------------------|------|-----|-----|-------|--------------------|
| SID173 | V _{PE} | Erase and program voltage | 1.71 | – | 5.5 | V | |

Table 19. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------|---|---|-------|-----|-----|---------|------------------------|
| SID174 | T _{ROWWRITE} ^[12] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 64 bytes |
| SID175 | T _{ROWERASE} ^[12] | Row erase time | – | – | 13 | ms | |
| SID176 | T _{ROWPROGRAM} ^[12] | Row program time after erase | – | – | 7 | ms | |
| SID178 | T _{BULKERASE} ^[12] | Bulk erase time (16 KB) | – | – | 15 | ms | |
| SID180 ^[13] | T _{DEVPROG} ^[12] | Total device program time | – | – | 7.5 | seconds | |
| SID181 ^[13] | F _{END} | Flash endurance | 100 K | – | – | cycles | |
| SID182 ^[13] | F _{RET} | Flash retention. T _A ≤ 55 °C, 100 K P/E cycles | 20 | – | – | years | |
| SID182A ^[13] | | Flash retention. T _A ≤ 85 °C, 10 K P/E cycles | 10 | – | – | years | |

System Resources

Power-on Reset (POR)

Table 20. Power On Reset (PRES)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|-----------------------|------------------------|------|-----|-----|-------|----------------------------|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up and power-down |
| SID185 ^[13] | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.5 | V | |
| SID186 ^[13] | V _{FALLIPOR} | Falling trip voltage | 0.70 | – | 1.4 | V | |

Table 21. Brown-out Detect (BOD) for V_{CCD}

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|--|------|-----|------|-------|--------------------|
| SID190 ^[13] | V _{FALLPPOR} | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | |
| SID192 ^[13] | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep | 1.11 | – | 1.5 | V | |

Notes

12. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

13. Guaranteed by characterization.

SWD Interface
Table 22. SWD Interface Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------|--------------|---|--------|-----|-------|-------|--|
| SID213 | F_SWDCCLK1 | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCCLK \leq 1/3 CPU clock frequency |
| SID214 | F_SWDCCLK2 | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | – | – | 7 | MHz | SWDCCLK \leq 1/3 CPU clock frequency |
| SID215 ^[14] | T_SWDI_SETUP | $T = 1/f\text{ SWDCCLK}$ | 0.25*T | – | – | ns | |
| SID216 ^[14] | T_SWDI_HOLD | $T = 1/f\text{ SWDCCLK}$ | 0.25*T | – | – | ns | |
| SID217 ^[14] | T_SWDO_VALID | $T = 1/f\text{ SWDCCLK}$ | – | – | 0.5*T | ns | |
| SID217A ^[14] | T_SWDO_HOLD | $T = 1/f\text{ SWDCCLK}$ | 1 | – | – | ns | |

Internal Main Oscillator
Table 23. IMO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|-----|-------|--------------------|
| SID218 | I _{IMO1} | IMO operating current at 48 MHz | – | – | 250 | μA | |
| SID219 | I _{IMO2} | IMO operating current at 24 MHz | – | – | 180 | μA | |

Table 24. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------------|--|-----|-----|-----|-------|---|
| SID223 | F _{IMOTOL1} | Frequency variation at 24 and 32 MHz (trimmed) | – | – | ±2 | % | $2\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, and $-25\text{ °C} \leq T_A \leq 85\text{ °C}$ |
| SID223A | F _{IMOTOLVCCD} | Frequency variation at 24 and 32 MHz (trimmed) | – | – | ±4 | % | All other conditions |
| SID226 | T _{STARTIMO} | IMO startup time | – | – | 7 | μs | |
| SID228 | T _{JITRMSIMO2} | RMS jitter at 24 MHz | – | 145 | – | ps | |

Internal Low-Speed Oscillator
Table 25. ILO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|----------------------|-----------------------|-----|-----|------|-------|--------------------|
| SID231 ^[14] | I _{ILO1} | ILO operating current | – | 0.3 | 1.05 | μA | |
| SID233 ^[14] | I _{ILOLEAK} | ILO leakage current | – | 2 | 15 | nA | |

Table 26. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|---------------------|-----|-----|-----|-------|--------------------|
| SID234 ^[14] | T _{STARTILO1} | ILO startup time | – | – | 2 | ms | |
| SID236 ^[14] | T _{ILODUTY} | ILO duty cycle | 40 | 50 | 60 | % | |
| SID237 | F _{ILOTRIM1} | ILO frequency range | 20 | 40 | 80 | kHz | |

Note

14. Guaranteed by characterization.

Table 27. External Clock Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------|------------------------------------|-----|-----|-----|-------|--------------------|
| SID305 ^[15] | ExtClkFreq | External clock input frequency | 0 | – | 16 | MHz | |
| SID306 ^[15] | ExtClkDuty | Duty cycle; measured at $V_{DD}/2$ | 45 | – | 55 | % | |

Table 28. Block Specs

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|------------------------------------|-----|-----|-----|---------|--------------------|
| SID262 ^[15] | T _{CLKSWITCH} | System clock source switching time | 3 | – | 4 | Periods | |

Note

15. Guaranteed by characterization.

The Field Values are listed in the following table:

| Field | Description | Values | Meaning |
|-------|-------------------|---------|--|
| CY8C | Cypress prefix | | |
| 4 | Architecture | 4 | PSoC 4 |
| A | Family | 0 | 4000 Family |
| B | CPU speed | 1 | 16 MHz |
| | | 4 | 48 MHz |
| C | Flash capacity | 3 | 8 KB |
| | | 4 | 16 KB |
| | | 5 | 32 KB |
| | | 6 | 64 KB |
| | | 7 | 128 KB |
| DE | Package code | SX | SOIC |
| | | LQ | QFN |
| | | PV | SSOP |
| | | FN | WLCSP |
| F | Temperature range | I | Industrial |
| XYZ | Attributes code | 000-999 | Code of feature set in specific family |

Packaging

Table 29. Package List

| Spec ID# | Package | Description |
|----------|-------------------------------|--|
| BID#47A | 28-Pin SSOP | 28-pin 5 × 10 × 1.65mm SSOP with 0.65-mm pitch |
| BID#26 | 24-Pin QFN | 24-pin 4 × 4 × 0.6 mm QFN with 0.5-mm pitch |
| BID#33 | 16-Pin QFN | 16-pin 3 × 3 × 0.6 mm QFN with 0.5-mm pitch |
| BID#40 | 16-Pin SOIC | 16-pin (150 Mil) SOIC |
| BID#47 | 8-Pin SOIC | 8-pin (150 Mil) SOIC |
| BID#147A | 16-Ball WLCSP (1.47 × 1.58mm) | 16-Ball 1.47 × 1.58 × 0.4 mm |
| | 16-Ball WLCSP (1.45 × 1.56mm) | 16-Ball 1.45 × 1.56 × 0.4 mm |

Table 30. Package Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------------|---|------------|-----|------|-----|---------|
| T _A | Operating ambient temperature | | -40 | 25 | 85 | °C |
| T _J | Operating junction temperature | | -40 | - | 100 | °C |
| T _{JA} | Package θ _{JA} (28-pin SSOP) | | - | 66.6 | - | °C/Watt |
| T _{JC} | Package θ _{JC} (28-pin SSOP) | | - | 34 | - | °C/Watt |
| T _{JA} | Package θ _{JA} (24-pin QFN) | | - | 38 | - | °C/Watt |
| T _{JC} | Package θ _{JC} (24-pin QFN) | | - | 5.6 | - | °C/Watt |
| T _{JA} | Package θ _{JA} (16-pin QFN) | | - | 49.6 | - | °C/Watt |
| T _{JC} | Package θ _{JC} (16-pin QFN) | | - | 5.9 | - | °C/Watt |
| T _{JA} | Package θ _{JA} (16-pin SOIC) | | - | 142 | - | °C/Watt |
| T _{JC} | Package θ _{JC} (16-pin SOIC) | | - | 49.8 | - | °C/Watt |
| T _{JA} | Package θ _{JA} (16-ball WLCSP) | | - | 90 | - | °C/Watt |
| T _{JC} | Package θ _{JC} (16-ball WLCSP) | | - | 0.9 | - | °C/Watt |
| T _{JA} | Package θ _{JA} (8-pin SOIC) | | - | 198 | - | °C/Watt |
| T _{JC} | Package θ _{JC} (8-pin SOIC) | | - | 56.9 | - | °C/Watt |

Table 31. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---------|--------------------------|----------------------------------|
| All | 260 °C | 30 seconds |

Table 32. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

| Package | MSL |
|------------------|-------|
| All except WLCSP | MSL 3 |
| 16-ball WLCSP | MSL1 |

Package Outline Drawings

Figure 11. 28-Pin SSOP Package Outline

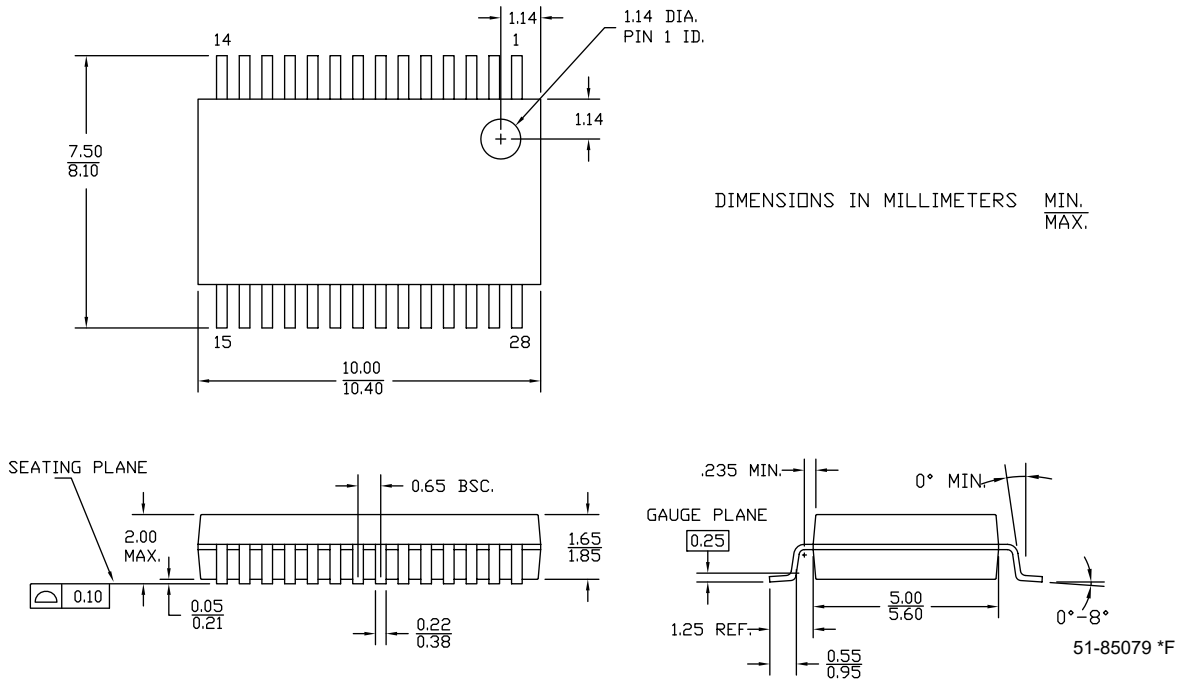
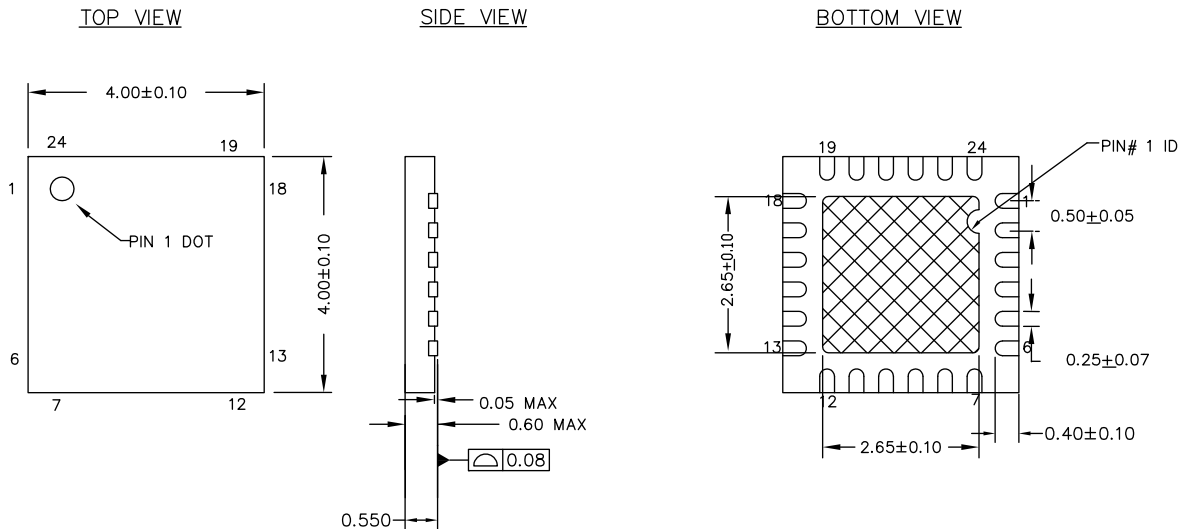


Figure 12. 24-pin QFN EPAD (Sawn) Package Outline



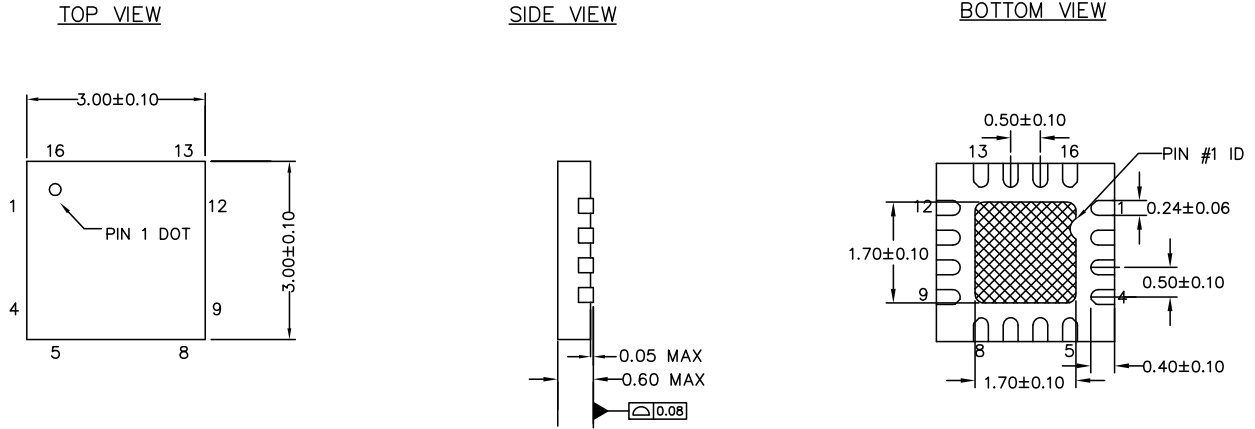
NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *G

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 13. 16-pin QFN Package EPAD (Sawn)

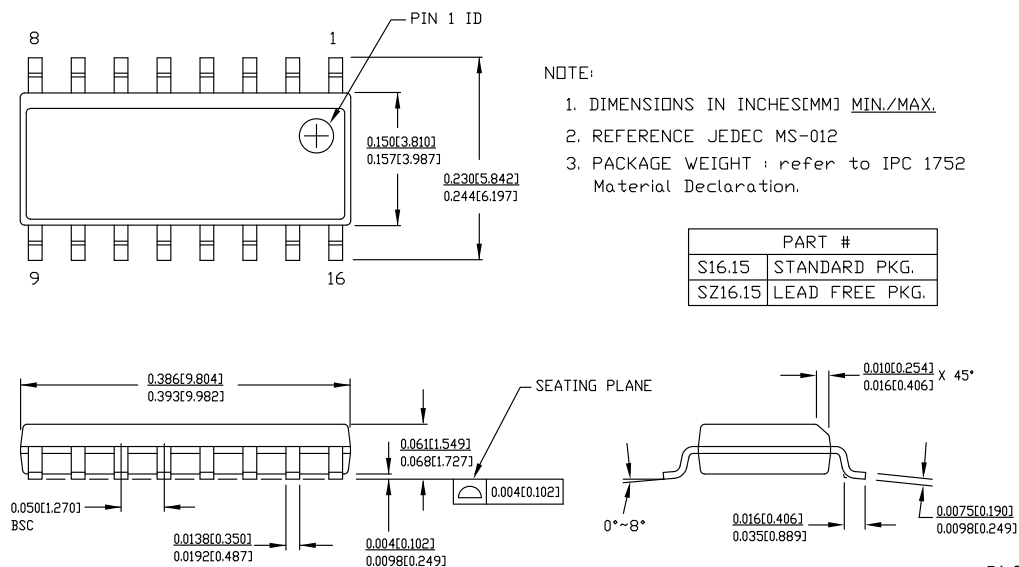


NOTES

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web

001-87187 *A

Figure 14. 16-pin (150-mil) SOIC Package Outline



51-85068 *F

Figure 15. 8-pin (150-mil) SOIC Package Outline

1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

| PART # | |
|---------|---------------|
| S08.15 | STANDARD PKG |
| SZ08.15 | LEAD FREE PKG |
| SW8.15 | LEAD FREE PKG |

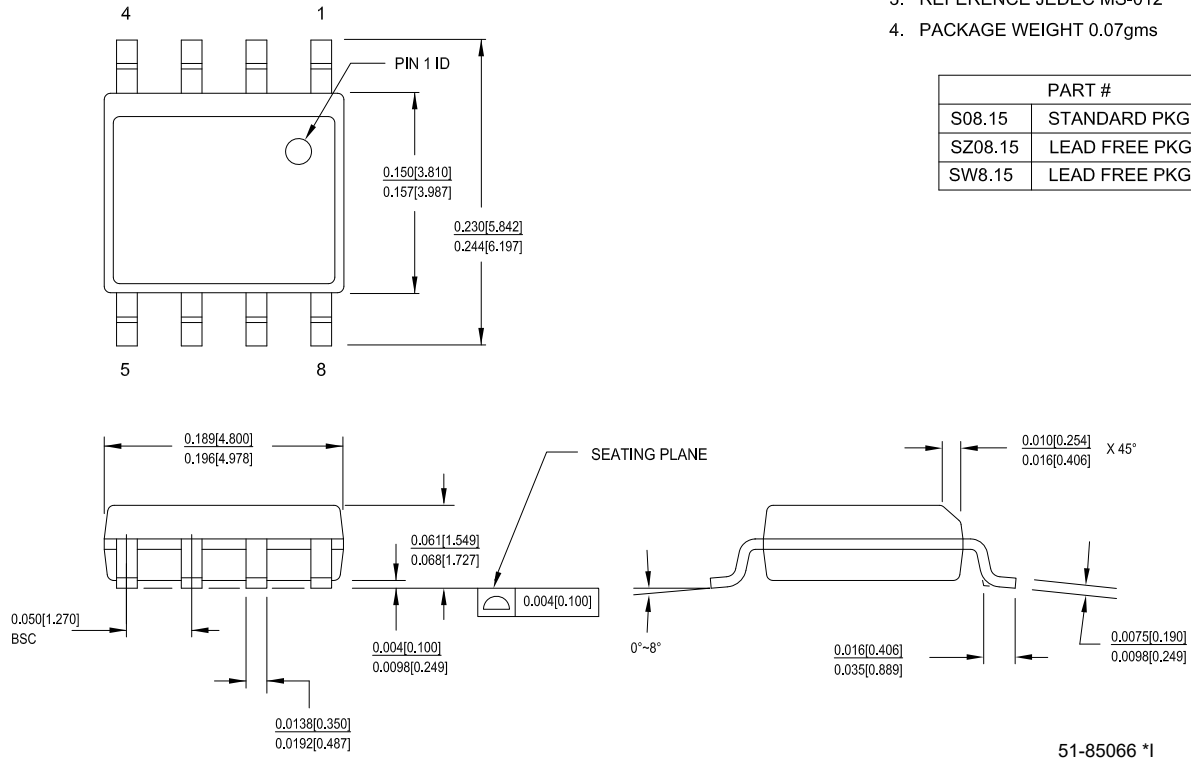
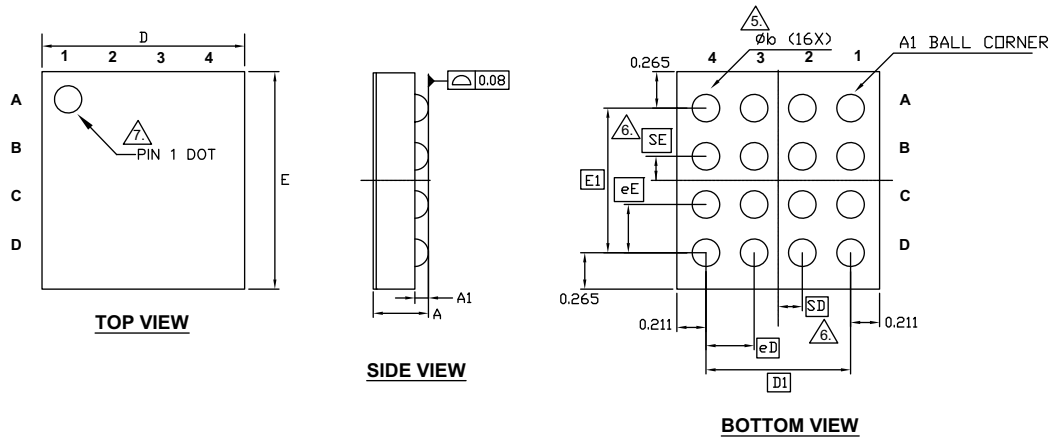


Figure 16. 16-Ball WLCSP 1.47 × 1.58 × 0.42 mm

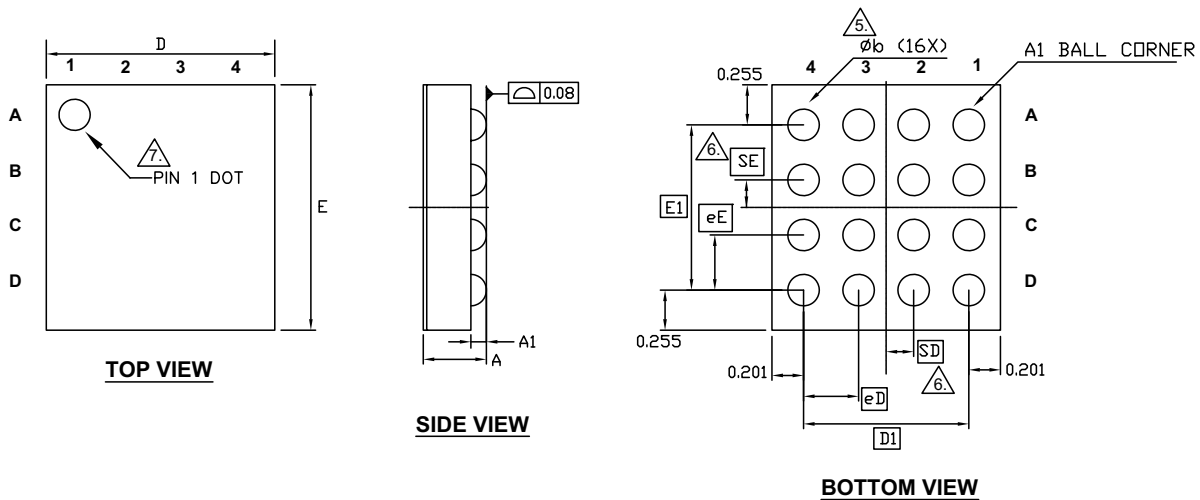


| SYMBOL | DIMENSIONS | | |
|--------|------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | - | - | 0.42 |
| A1 | 0.089 | 0.099 | 0.109 |
| D | 1.447 | 1.472 | 1.497 |
| E | 1.554 | 1.579 | 1.604 |
| D1 | 1.05 BSC | | |
| E1 | 1.05 BSC | | |
| MD | 4 | | |
| ME | 4 | | |
| N | 16 | | |
| ∅ b | 0.17 | 0.20 | 0.23 |
| eD | 0.35 BSC | | |
| eE | 0.35 BSC | | |
| SD | 0.18 BSC | | |
| SE | 0.18 BSC | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : N/A.

002-18598 **

Figure 17. 16-Ball WLCSP 1.45 × 1.56 × 0.42 mm


| SYMBOL | DIMENSIONS | | |
|--------|------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | - | - | 0.42 |
| A1 | 0.089 | 0.099 | 0.109 |
| D | 1.427 | 1.452 | 1.477 |
| E | 1.534 | 1.559 | 1.584 |
| D1 | 1.05 BSC | | |
| E1 | 1.05 BSC | | |
| MD | 4 | | |
| ME | 4 | | |
| N | 16 | | |
| ∅ b | 0.17 | 0.20 | 0.23 |
| eD | 0.35 BSC | | |
| eE | 0.35 BSC | | |
| SD | 0.18 BSC | | |
| SE | 0.18 BSC | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
 - SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
 - "e" REPRESENTS THE SOLDER BALL GRID PITCH.
 - SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- △5 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- △6 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- △7 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
 - JEDEC SPECIFICATION NO. REF. : N/A.

001-95966 *C

Acronyms

Table 33. Acronyms Used in this Document

| Acronym | Description |
|---------|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| Arm® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |

Table 33. Acronyms Used in this Document (continued)

| Acronym | Description |
|--------------------------|--|
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoc pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |

Table 33. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|-------------------|--|
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC [®] | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |

Table 33. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|---------|--|
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

Document Conventions

Units of Measure

Table 34. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |

Table 34. Units of Measure (continued)

| Symbol | Unit of Measure |
|--------|----------------------|
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

Revision History

| Description Title: PSoC [®] 4: PSoC 4000 Family Datasheet Programmable System-on-Chip (PSoC [®]) Document Number: 001-89638 | | | |
|---|---------|-----------------|--|
| Revision | ECN | Submission Date | Description of Change |
| *B | 4348760 | 05/16/2014 | New PSoC 4000 datasheet. |
| *C | 4514139 | 10/27/2014 | Added 28-pin SSOP pin and package details. Updated V _{REF} spec values. Updated conditions for SID174. Updated SID.CSD#15 values and description. Added spec SID339. |
| *D | 4617283 | 01/09/2015 | Corrected Development Kits information and PSoC Creator Example Project figure. Corrected typo in the ordering information table. Updated 28-pin SSOP package diagram. |
| *E | 4735762 | 05/26/2015 | Added 16-ball WLCSP pin and package details. |
| *F | 5466193 | 10/07/2016 | Updated Table 32 . Updated 8-pin SOIC package diagram. Updated the template. |
| *G | 5685079 | 04/05/2017 | Updated 16-ball WLCSP package details. |
| *H | 5807014 | 07/24/2017 | Added Figure 17 (spec 001-95966 *C) in Packaging . Updated Table 29 . Updated Ordering Information . |
| *I | 6189153 | 05/29/2018 | Updated 8-pin SOIC and 24-pin QFN package drawings. |
| *J | 6604429 | 07/02/2019 | Corrected TRM links in More Information . Updated clocking diagram. Updated Pin 26 in 28-pin SSOP pinout. Added CSD ADC DC Specifications and CSD ADC AC Specifications . |
| *K | 7104675 | 03/15/2021 | Updated conditions for SID.CLK#6. |

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