

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90340 Series

MB90F342A(S), MB90F342CA(S), MB90F343A(S), MB90F343CA(S), MB90F345A(S), MB90F345CA(S), MB90F346A(S), MB90F346CA(S), MB90F347A(S), MB90F347CA(S), MB90F349A(S), MB90F349CA(S), MB90341A(S), MB90341CA(S), MB90342A(S), MB90342CA(S), MB90346A(S), MB90346CA(S), MB90347A(S), MB90347CA(S), MB90348A(S), MB90348CA(S), MB90349A(S), MB90349CA(S), MB90V340A-101/102

### ■ DESCRIPTION

The MB90340-series with up to 2 FULL-CAN\* interfaces and FLASH ROM is especially designed for automotive and other industrial applications. Its main feature are the on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35  $\mu\text{m}$  CMOS technology, Fujitsu now offers on-chip FLASH-ROM program memory up to 512 Kbytes.

The power supply (3 V) is supplied to the internal MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

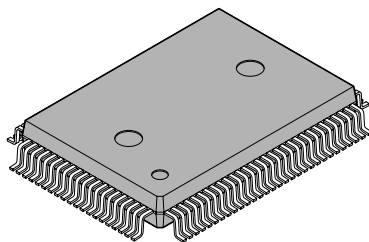
The unit features an 8 channel Output Compare Unit and 8 channel Input Capture Unit with 2 separate 16-bit free running timers. 4 UARTs constitute additional functionality for communication purposes.

\* : Controller Area Network (CAN) - License of Robert Bosch GmbH

Note : F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

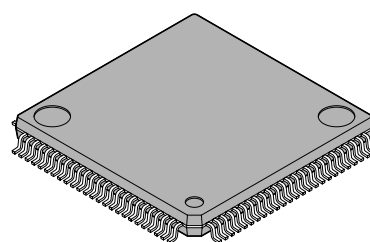
### ■ PACKAGES

100-pin Plastic QFP



(FPT-100P-M06)

100-pin Plastic LQFP



(FPT-100P-M05)

# MB90340 Series

## ■ FEATURES

### ● Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 6 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 24 MHz).
- Operation by sub-clock (up to 50 kHz : 100 kHz oscillation clock divided two) is allowed. (devices without S-suffix only)
- Minimum execution time of instruction : 42 ns (when operating with 4-MHz oscillation clock, and 6-time multiplied PLL clock).
- Built-in Clock Modulation circuit

### ● 16 Mbyte CPU memory space

- 24-bit internal addressing

### ● Instruction system best suited to controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes(23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

### ● Instruction system compatible with high-level language (C language) and multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

### ● Increased processing speed

- 4-byte instruction queue

### ● Powerful interrupt function

- Powerful 8-level, 34-condition interrupt feature
- Up to 16 external interrupts are supported

### ● Automatic data transfer function independent of CPU

- Expanded intelligent I/O service function (EI<sup>2</sup>OS) : up to 16 channels
- DMA : up to 16 channels

### ● Low power consumption (standby) mode

- Sleep mode (a mode that halts CPU operating clock)
- Main timer mode (time-base timer mode that is transferred from main clock mode)
- PLL timer mode (time-base timer mode that is transferred from PLL clock mode)
- Watch mode (a mode that operates sub clock and clock timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

### ● Process

- CMOS technology

### ● I/O port

- General-purpose input/output port (CMOS output)
  - 80 ports (devices without S-suffix)
  - 82 ports (devices with S-suffix)

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- **Timer**

- Time-base timer, clock timer, watchdog timer : 1 channel
- 8/16-bit PPG timer : 8-bit X 16 channels, or 16-bit X 8 channels
- 16-bit reload timer : 4 channels
- 16-bit input/output timer
  - 16-bit free run timer : 2 channel (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
  - 16-bit input capture: (ICU) : 8 channels
  - 16-bit output compare : (OCU) : 8 channels

- **Full-CAN interface : up to 2 channels**

- Compliant with Ver2.0A and Ver2.0B CAN specifications
- Flexible message buffering (mailbox and FIFO buffering can be mixed)
- CAN wake-up function

- **UART (LIN/SCI) : up to 4 channels**

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available

- **I<sup>2</sup>C interface\* : up to 2 channels (devices with C-suffix only)**

- Up to 400 Kbits/s transfer rate

- **DTP/External interrupt : up to 16 channels, CAN wakeup : up to 2 channels**

- Module for activation of expanded intelligent I/O service (EI<sup>2</sup>OS), DMA, and generation of external interrupt.

- **Delay interrupt generator module**

- Generates interrupt request for task switching.

- **8/10-bit A/D converter : 16/24 channels**

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3  $\mu$ s (at 24-MHz machine clock, including sampling time)

- **Program patch function**

- Address matching detection for 6 address pointers.

- **Internal voltage regulator**

- Supports 3 V MCU core, offering low EMI and low power consumption figures

- **Programmable input levels**

- Automotive/CMOS-Schmitt (initial level is Automotive in Single chip mode)
- TTL level (initial level for External bus mode)

- **FLASH memory security function**

- Protects the content of FLASH memory (FLASH memory device only)

- **External bus interface**

- **Clock monitor function**

\* : I<sup>2</sup>C license :

Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use, these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

# MB90340 Series

## ■ PRODUCT LINEUP

Part Number	MB90F342A(S), MB90F342CA(S), MB90F343A(S)*1, MB90F343CA(S)*1, MB90F345A(S), MB90F345CA(S), MB90F346A(S), MB90F346CA(S), MB90F347A(S), MB90F347CA(S), MB90F349A(S), MB90F349CA(S), MB90341A(S)*1, MB90341CA(S)*1, MB90342A(S)*1, MB90342CA(S)*1, MB90346A(S), MB90346CA(S), MB90347A(S), MB90347CA(S), MB90348A(S)*1, MB90348CA(S)*1, MB90349A(S)*1, MB90349CA(S)*1	MB90V340A-101/102
Parameter		
CPU	F <sup>2</sup> MC-16LX CPU	
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)	
ROM	MASK ROM, Flash memory 512 Kbytes : MB90F345A(S), MB90F345CA(S) 384 Kbytes : MB90F343A(S), MB90F343CA(S) 256 Kbytes : MB90F342A(S), MB90F342CA(S), MB90F349A(S), MB90F349CA(S), MB90342A(S), MB90342CA(S), MB90349A(S), MB90349CA(S) 128 Kbytes : MB90F347A(S), MB90F347CA(S), MB90341A(S), MB90341CA(S), MB90348A(S), MB90348CA(S), MB90347A(S), MB90347CA(S) 64 Kbytes : MB90F346A(S), MB90F346CA(S), MB90346A(S), MB90346CA(S)	External
RAM	20 Kbytes : MB90F343A(S), MB90F343CA(S), MB90F345A(S), MB90F345CA(S) 16 Kbytes : MB90F342A(S), MB90F342CA(S), MB90F349A(S), MB90F349CA(S), MB90341A(S), MB90341CA(S), MB90342A(S), MB90342CA(S), MB90348A(S), MB90348CA(S), MB90349A(S), MB90349CA(S) 6 Kbytes : MB90F347A(S), MB90F347CA(S), MB90347A(S), MB90347CA(S) 2 Kbytes : MB90F346A(S), MB90F346CA(S), MB90346A(S), MB90346CA(S)	30 Kbytes
Emulator-specific power supply*2	—	Yes
Technology	0.35 μm CMOS with regulator for internal power supply + Flash memory with Charge pump for programming voltage	0.35 μm CMOS with regulator for internal power supply
Operating voltage range	3.5 V - 5.5 V : at normal operating (not using A/D converter) 4.0 V - 5.5 V : at using A/D converter/Flash programming 4.5 V - 5.5 V : at using external bus	5 V ± 10%
Temperature range	-40 °C to +105 °C	
Package	QFP-100, LQFP-100	PGA-299
UART	4 channels	5 channels
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device	
I <sup>2</sup> C (400 Kbps)	devices with 'C'-suffix : 2ch devices without 'C'-suffix : —	2 channels

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# MB90340 Series

<b>Part Number</b>	MB90F342A(S), MB90F342CA(S), MB90F343A(S)*1, MB90F343CA(S)*1, MB90F345A(S), MB90F345CA(S), MB90F346A(S), MB90F346CA(S), MB90F347A(S), MB90F347CA(S), MB90F349A(S), MB90F349CA(S), MB90341A(S)*1, MB90341CA(S)*1, MB90342A(S)*1, MB90342CA(S)*1, MB90346A(S), MB90346CA(S), MB90347A(S), MB90347CA(S), MB90348A(S)*1, MB90348CA(S)*1, MB90349A(S)*1, MB90349CA(S)*1	MB90V340A-101/102
<b>Parameter</b>		
A/D Converter	<p>devices with 'C'-suffix : 24ch            devices without 'C'-suffix : 16ch</p> <p>10-bit or 8-bit resolution            Conversion time : Min 3 <math>\mu</math>s include sample time (per one channel)</p>	24 input channels
16-bit Reload Timer (4 channels)	<p>Operation clock frequency : <math>f_{sys}/2^1</math>, <math>f_{sys}/2^3</math>, <math>f_{sys}/2^5</math> (<math>f_{sys}</math> = Machine clock frequency)            Supports External Event Count function</p>	
16-bit I/O Timer (2 channels)	<p>Signals an interrupt when overflowing            Supports Timer Clear when a match with Output Compare (Channel 0, 4)            Operation clock freq. : <math>f_{sys}</math>, <math>f_{sys}/2^1</math>, <math>f_{sys}/2^2</math>, <math>f_{sys}/2^3</math>, <math>f_{sys}/2^4</math>, <math>f_{sys}/2^5</math>, <math>f_{sys}/2^6</math>, <math>f_{sys}/2^7</math> (<math>f_{sys}</math> = Machine clock freq.)            I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3            I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7</p>	
16-bit Output Compare (8 channels)	<p>Signals an interrupt when 16-bit I/O Timer match output compare registers.            A pair of compare registers can be used to generate an output signal.</p>	
16-bit Input Capture (8 channels)	<p>Rising edge, falling edge or rising &amp; falling edge sensitive            Signals an interrupt upon external event</p>	
8/16-bit Programmable Pulse Generator (8 channels)	<p>Supports 8-bit and 16-bit operation modes            Sixteen 8-bit reload counters            Sixteen 8-bit reload registers for L pulse width            Sixteen 8-bit reload registers for H pulse width            A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter            Operation clock freq. : <math>f_{sys}</math>, <math>f_{sys}/2^1</math>, <math>f_{sys}/2^2</math>, <math>f_{sys}/2^3</math>, <math>f_{sys}/2^4</math> or 128 <math>\mu</math>s@<math>f_{osc}</math> = 4 MHz (<math>f_{sys}</math> = Machine clock frequency, <math>f_{osc}</math> = Oscillation clock frequency)</p>	
CAN Interface	<p>2 channels : MB90F342A(S), MB90F342CA(S), MB90F345A(S), MB90F345CA(S), MB90341A(S), MB90341CA(S), MB90342A(S), MB90342CA(S)            1 channel : MB90F346A(S), MB90F346CA(S), MB90F347A(S), MB90F347CA(S), MB90F349A(S), MB90F349CA(S), MB90346A(S), MB90346CA(S), MB90347A(S), MB90347CA(S), MB90348A(S), MB90348CA(S), MB90349A(S), MB90349CA(S)</p> <p>Conforms to CAN Specification Version 2.0 Part A and B            Automatic re-transmission in case of error            Automatic transmission responding to Remote Frame            Prioritized 16 message buffers for data and ID's            Supports multiple messages            Flexible configuration of acceptance filtering :                Full bit compare/Full bit mask/Two partial bit masks            Supports up to 1 Mbps</p>	3 channels

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# MB90340 Series

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<b>Part Number</b>	MB90F342A(S), MB90F342CA(S), MB90F343A(S)*1, MB90F343CA(S)*1, MB90F345A(S), MB90F345CA(S), MB90F346A(S), MB90F346CA(S), MB90F347A(S), MB90F347CA(S), MB90F349A(S), MB90F349CA(S), MB90341A(S)*1, MB90341CA(S)*1, MB90342A(S)*1, MB90342CA(S)*1, MB90346A(S), MB90346CA(S), MB90347A(S), MB90347CA(S), MB90348A(S)*1, MB90348CA(S)*1, MB90349A(S)*1, MB90349CA(S)*1	MB90V340A-101/102
<b>Parameter</b>		
External Interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI <sup>2</sup> OS) and DMA	
D/A converter	—	2 channels
Up to 100 kHz Subclock for low power operation	without subclock : devices with 'S'-suffix or MB90V340A-101 with subclock : devices without 'S'-suffix or MB90V340A-102	
I/O Ports	Virtually all external pins can be used as general purpose I/O port All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable in pin-wise of 8 as CMOS schmitt trigger/ automotive inputs (default) TTL input level settable for external bus (32-pin only for external bus)	
Flash Memory	Supports automatic programming, Embedded Algorithm <sup>TM*3</sup> Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (except for MB90F346A(S) and MB90F346CA (S) )	—

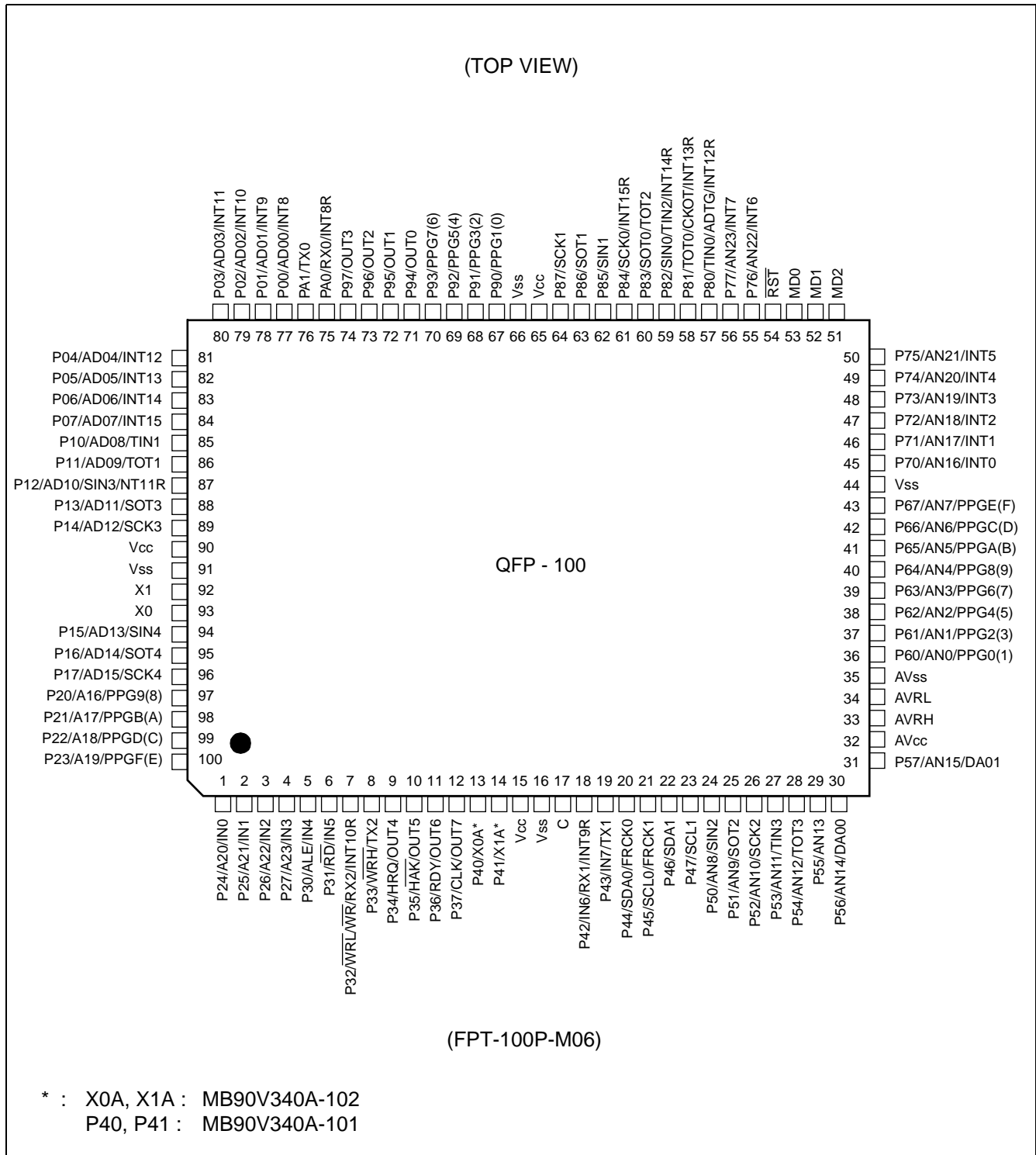
\*1 : These devices are under development.

\*2 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.  
Please refer to the Emulator hardware manual about details.

\*3 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

## PIN ASSIGNMENTS

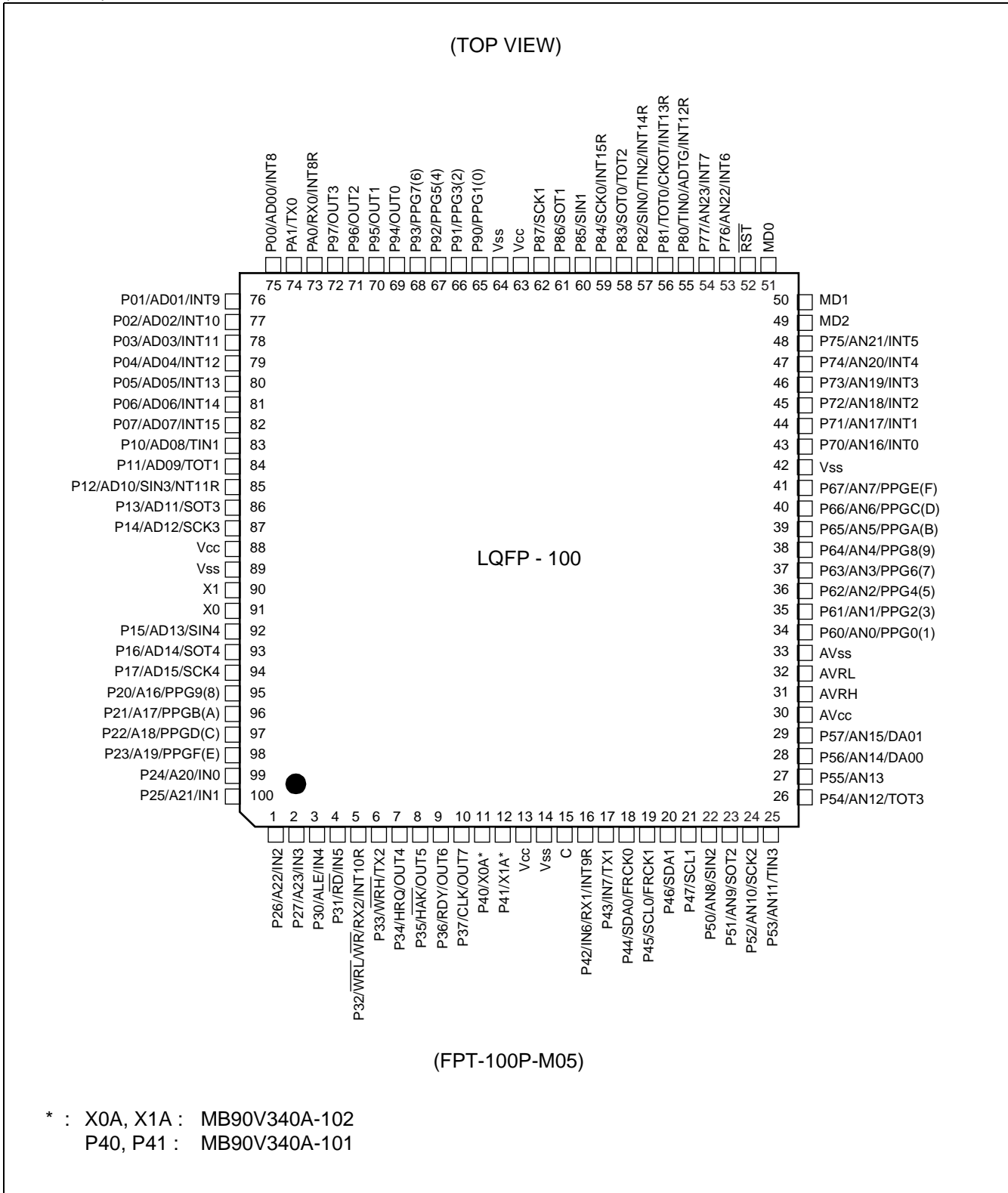
- MB90V340A-101/MB90V340A-102



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# MB90340 Series

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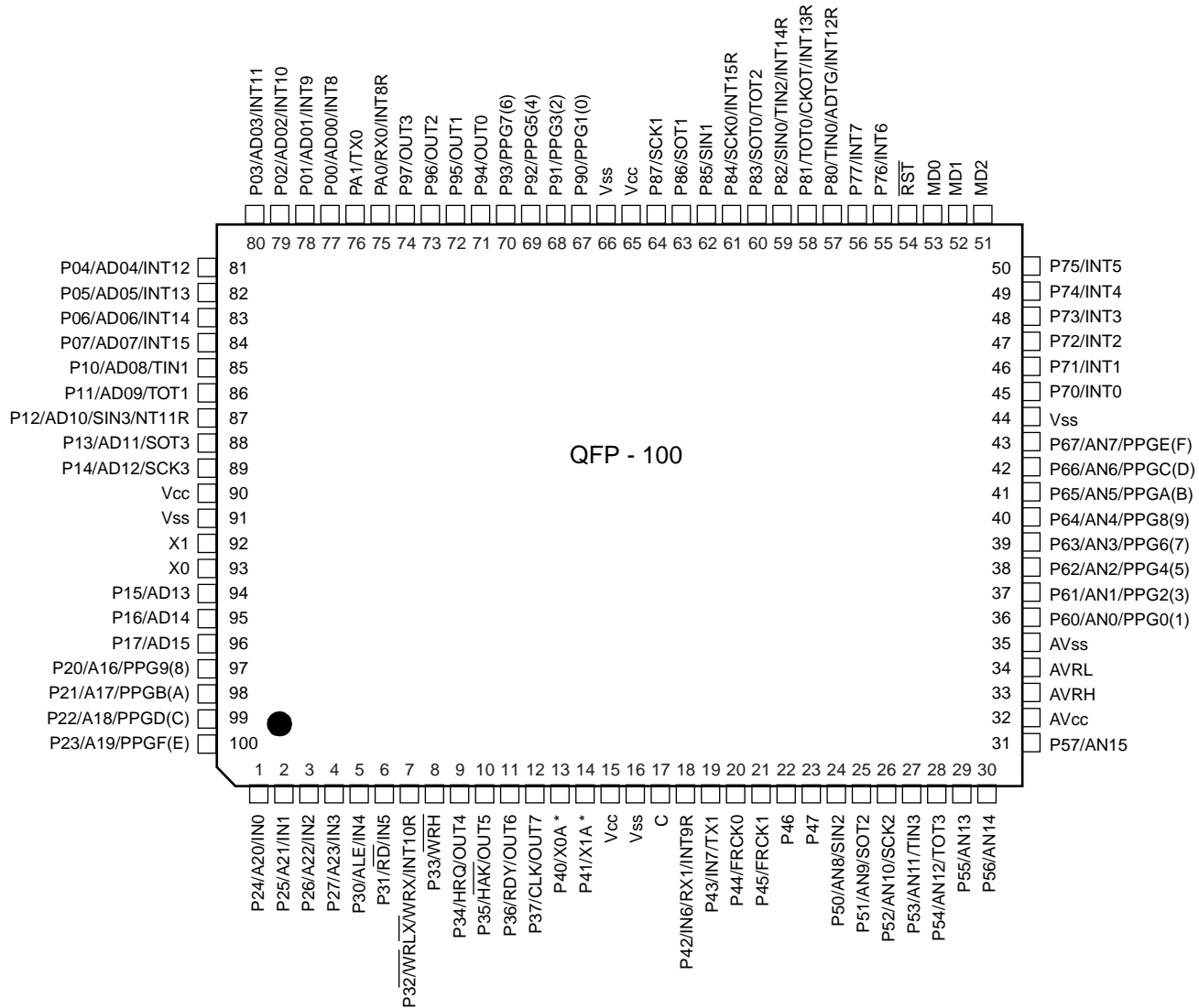




# MB90340 Series

- MB90F342A(S) / MB90F343A(S) / MB90F345A(S) / MB90F346A(S) / MB90F347A(S) / MB90F349A(S) / MB90341A(S) / MB90342A(S) / MB90346A(S) / MB90347A(S) / MB90348A(S) / MB90349A(S)

(TOP VIEW)

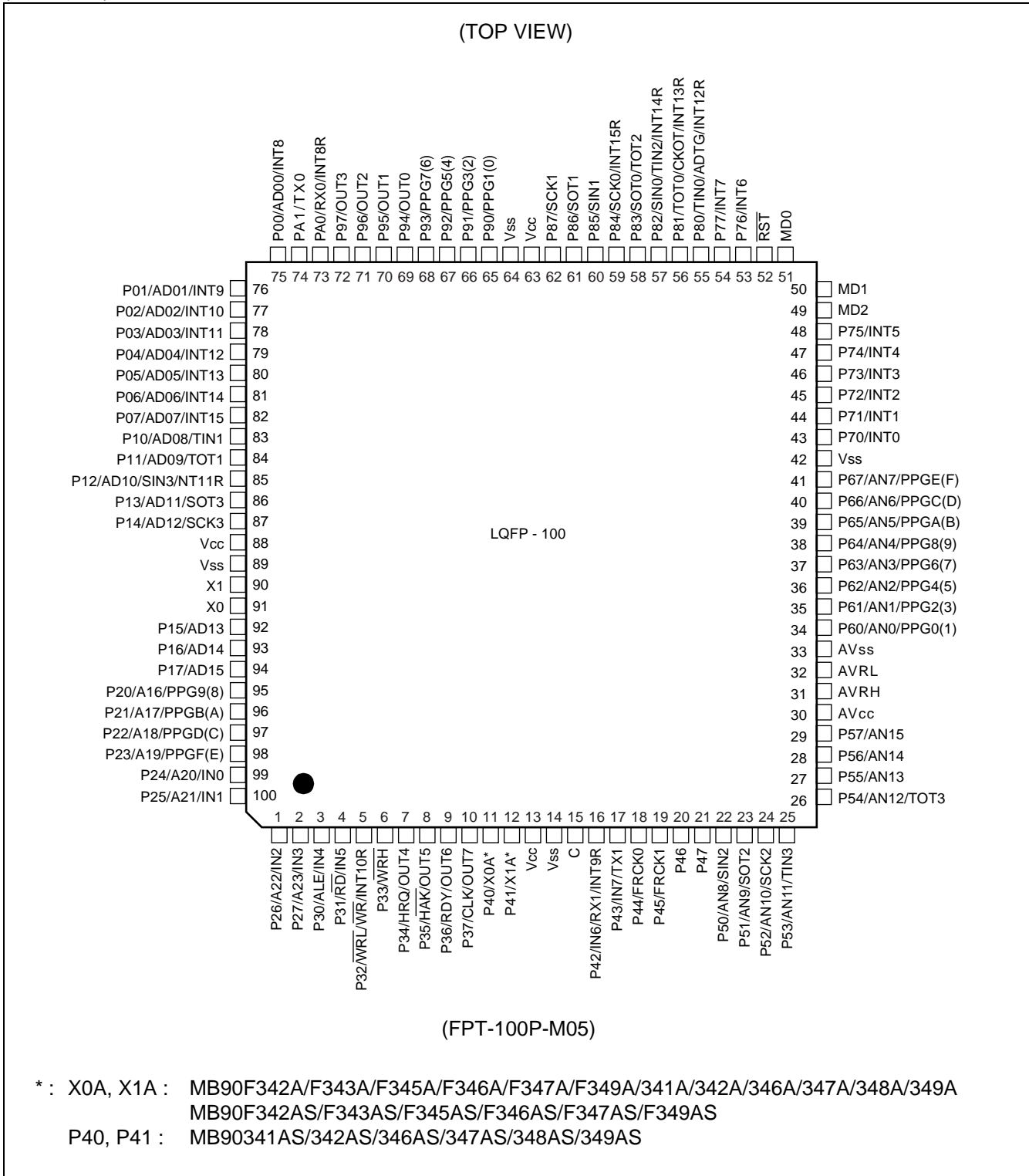


- \* : X0A, X1A : MB90F342A/F343A/F345A/F346A/F347A/F349A/341A/342A/346A/347A/348A/349A  
MB90F342AS/F343AS/F345AS/F346AS/F347AS/F349AS
- P40, P41 : MB90341AS/342AS/346AS/347AS/348AS/349AS

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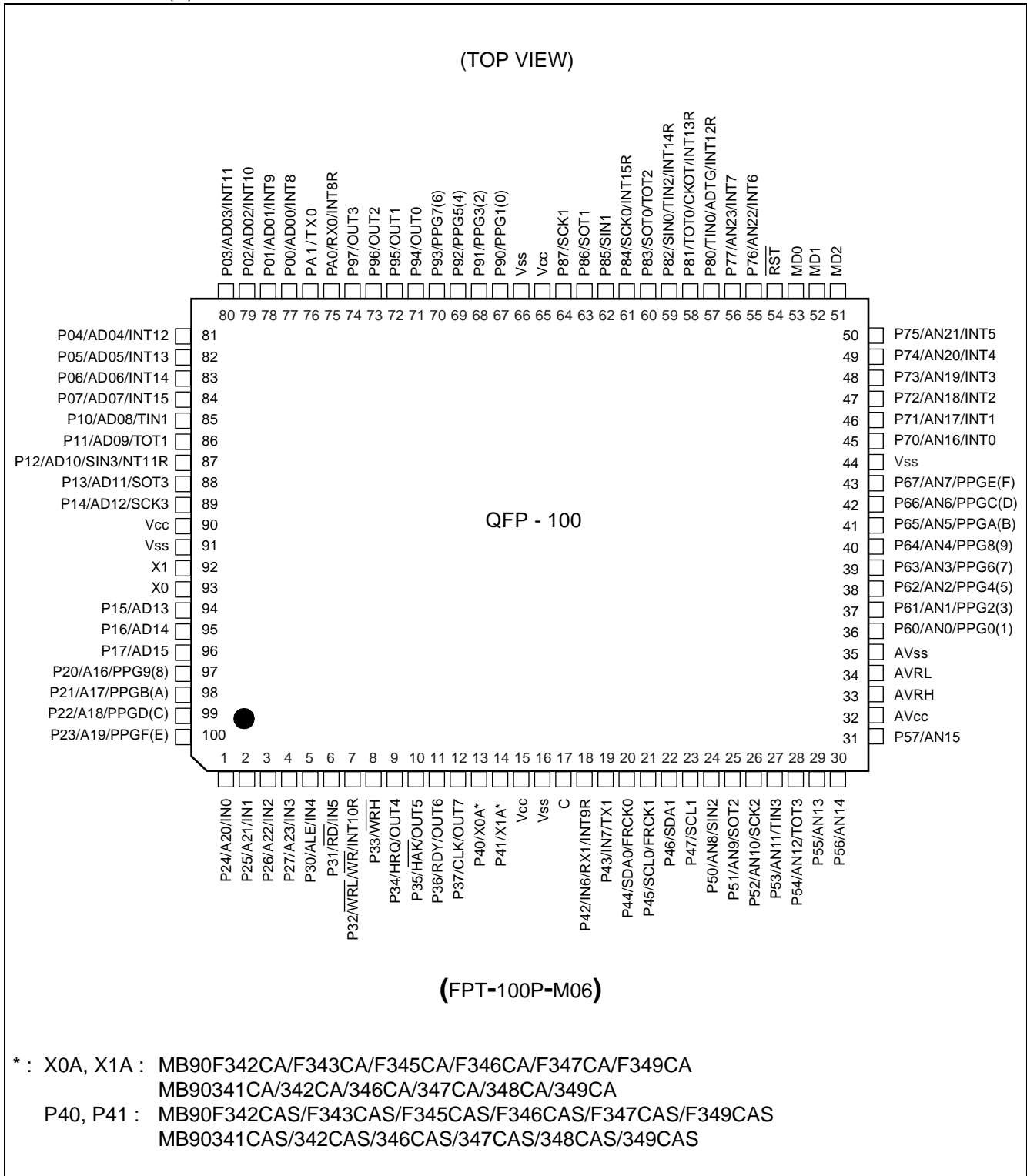
# MB90340 Series

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# MB90340 Series

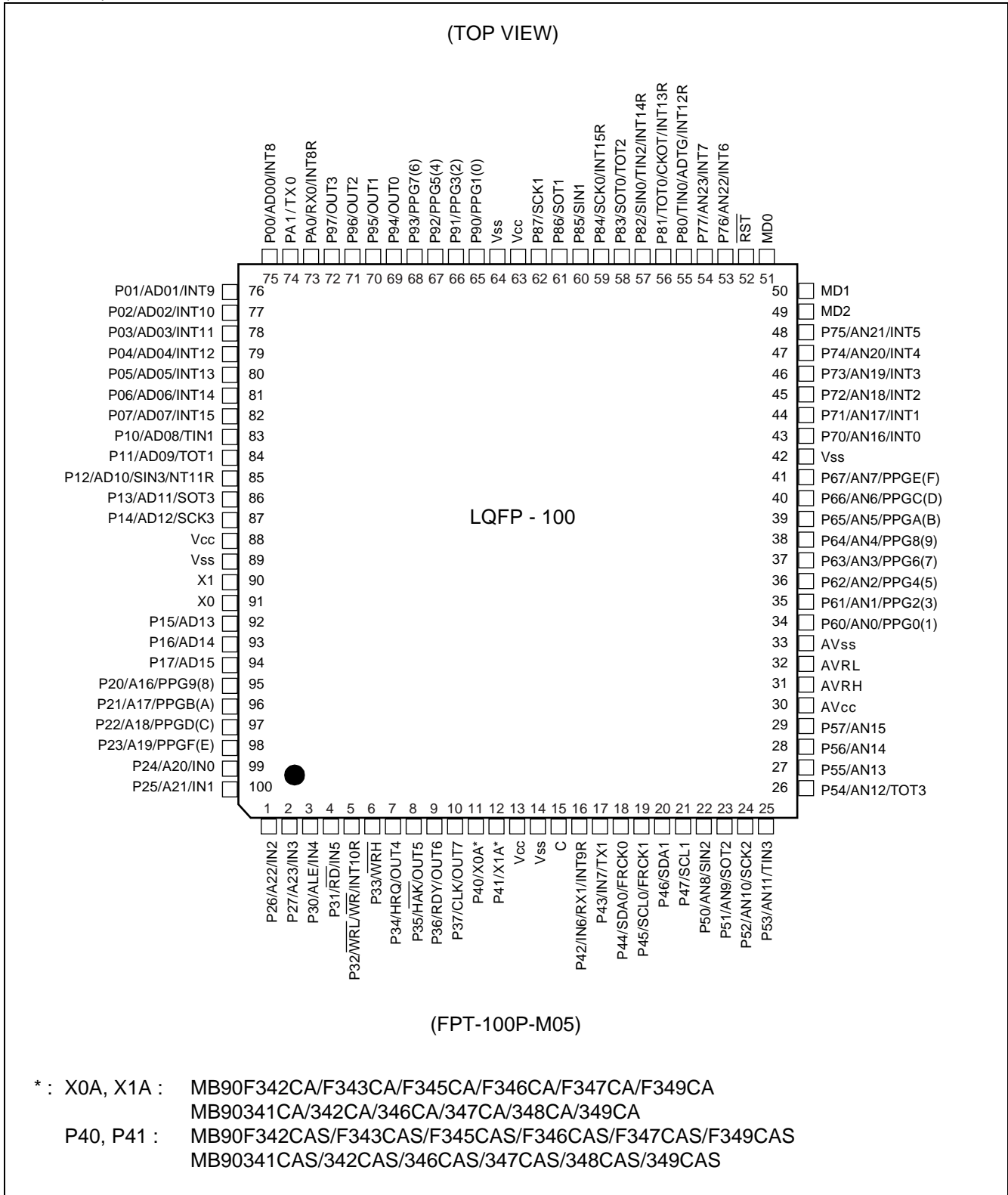
- MB90F342CA(S) / MB90F343CA(S) / MB90F345CA(S) / MB90F346CA(S) / MB90F347CA(S) / MB90F349CA(S) / MB90341CA(S) / MB90342CA(S) / MB90346CA(S) / MB90347CA(S) / MB90348CA(S) / MB90349CA(S)



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# MB90340 Series

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## ■ PIN DESCRIPTION

Pin No.		Pin name	Circuit type	Function
LQFP100*2	QFP100*1			
90	92	X1	A	Oscillation output
91	93	X0		Oscillation input
52	54	$\overline{\text{RST}}$	E	Reset input
75 to 82	77 to 84	P00 to P07	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins for INT8 to INT15.
83	85	P10	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer 1
84	86	P11	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer 1
85	87	P12	N	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin for INT11
86	88	P13	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
87	89	P14	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3

(Continued)

# MB90340 Series

Pin No.		Pin name	Circuit type	Function
LQFP100*2	QFP100*1			
92	94	P15	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN4		Serial data input pin for UART4 (EVA devices)
93	95	P16	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT4		Serial data output pin for UART4 (EVA devices)
94	96	P17	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK4		Clock I/O pin for UART4 (EVA devices only)
95 to 98	97 to 100	P20 to P23	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins for A16 to A19 of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, PPGB, PPGD, PPGF		Output pins for PPGs
99 to 2	1 to 4	P24 to P27	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins for A20 to A23 of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Data sample input pins for input captures ICU0 to ICU3
3	5	P30	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Data sample input pin for input capture ICU4

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# MB90340 Series

Pin No.		Pin name	Circuit type	Function
LQFP100*2	QFP100*1			
4	6	P31	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
		IN5		Data sample input pin for input capture ICU5
5	7	P32	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WR}/\overline{WRL}$ pin output disabled.
		$\overline{WRL} / \overline{WR}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}/\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		RX2		RX input pin for CAN2 Interface (EVA devices)
		INT10R		External interrupt request input pin for INT10
6	8	P33	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WRH}$ pin output disabled.
		$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.
		TX2		TX Output pin for CAN2 (EVA devices)
7	9	P34	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare OCU4
8	10	P35	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
		$\overline{HAK}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare OCU6
9	11	P36	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare OCU5

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# MB90340 Series

Pin No.		Pin name	Circuit type	Function
LQFP100*2	QFP100*1			
10	12	P37	G	General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
		OUT7		Waveform output pin for output compare OCU7
11, 12	13, 14	P40, P41	F	General purpose I/O (devices with S-suffix or MB90V340A-101)
		X0A, X1A	B	Oscillator input pins for sub-clock (devices without S-suffix or MB90V340A-102)
16	18	P42	F	General purpose I/O
		IN6		Data sample input pin for input capture ICU6
		RX1		RX input pin for CAN1 Interface (MB90F342A/F343A/F345A/341A/342A only)
		INT9R		External interrupt request input pin for INT9
17	19	P43	F	General purpose I/O
		IN7		Data sample input pin for input capture ICU7
		TX1		TX Output pin for CAN1 (MB90F342A/F343A/F345A/341A/342A only)
18	20	P44	H	General purpose I/O
		SDA0		Serial data I/O pin for I <sup>2</sup> C 0 (devices with C-suffix)
		FRCK0		Input for the 16-bit I/O Timer 0
19	21	P45	H	General purpose I/O
		SCL0		Serial clock I/O pin for I <sup>2</sup> C 0 (devices with C-suffix)
		FRCK1		Input for the 16-bit I/O Timer 1
20	22	P46	H	General purpose I/O
		SDA1		Serial data I/O pin for I <sup>2</sup> C 1 (devices with C-suffix)
21	23	P47	H	General purpose I/O
		SCL1		Serial clock I/O pin for I <sup>2</sup> C 1 (devices with C-suffix)
22	24	P50	O	General purpose I/O
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
23	25	P51	I	General purpose I/O
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
24	26	P52	I	General purpose I/O
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2

(Continued)



# MB90340 Series

Pin No.		Pin name	Circuit type	Function
LQFP100*2	QFP100*1			
25	27	P53	I	General purpose I/O
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timers 3
26	28	P54	I	General purpose I/O
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer 3
27	29	P55	I	General purpose I/O
		AN13		Analog input pin for the A/D converter
28, 29	30, 31	P56 to P57	J	General purpose I/O
		AN14 to AN15		Analog input pin for the A/D converter
		DA00 to DA01		D/A converter analog output pins (MB90V340 only)
34 to 41	36 to 43	P60 to P67	I	General purpose I/O
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
43 to 48, 53, 54	45 to 50, 55, 56	P70 to P77	I	General purpose I/O
		AN16 to AN23		Analog input pins for the A/D converter (devices with C-suffix)
		INT0 to INT7		External interrupt request input pins for INT0 to INT7
55	57	P80	F	General purpose I/O
		TIN0		Event input pin for the reload timers 0
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin for INT12
56	58	P81	F	General purpose I/O
		TOT0		Output pin for the reload timer 0
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin for INT13
57	59	P82	M	General purpose I/O
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timers 2
		INT14R		External interrupt request input pin for INT14
58	60	P83	F	General purpose I/O
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer 2
59	61	P84	F	General purpose I/O
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin for INT15

(Continued)

# MB90340 Series

(Continued)

Pin No.		Pin name	Circuit type	Function
LQFP100*2	QFP100*1			
60	62	P85	M	General purpose I/O
		SIN1		Serial data input pin for UART1
61	63	P86	F	General purpose I/O
		SOT1		Serial data output pin for UART1
62	64	P87	F	General purpose I/O
		SCK1		Clock I/O pin for UART1
65 to 68	67 to 70	P90 to P93	F	General purpose I/O
		PPG1, 3, 5, 7		Output pins for PPGs
69 to 72	71 to 74	P94 to P97	F	General purpose I/O
		OUT0 to OUT3		Waveform output pins for output compares OCU0 to OCU3. This function is enabled when the OCU enables waveform output.
73	75	PA0	F	General purpose I/O
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin for INT8
74	76	PA1	F	General purpose I/O
		TX0		TX Output pin for CAN0
30	32	AV <sub>cc</sub>	K	V <sub>cc</sub> power input pin for analog circuits
31	33	AVRH	L	Reference voltage input for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV <sub>cc</sub> .
32	34	AVRL	K	Lower reference voltage input for the A/D Converter
33	35	AV <sub>ss</sub>	K	V <sub>ss</sub> power input pin for analog circuits
50, 51	52, 53	MD1, MD0	C	Input pins for specifying the operating mode.
49	51	MD2	D	Input pin for specifying the operating mode.
13 63 88	15 65 90	V <sub>cc</sub>	—	Power (3.5 V to 5.5 V) input pins
14 42 64 89	16 44 66 91	V <sub>ss</sub>	—	Power (0V) input pins
15	17	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor.

\*1 : FPT-100P-M06

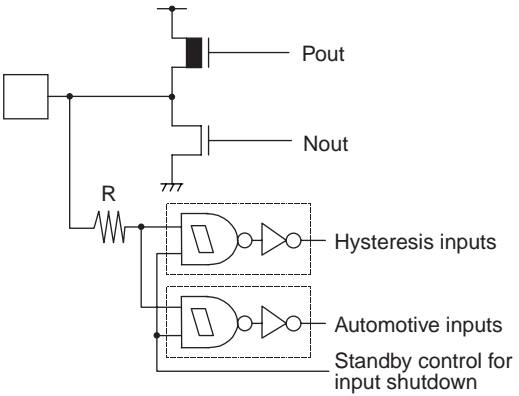
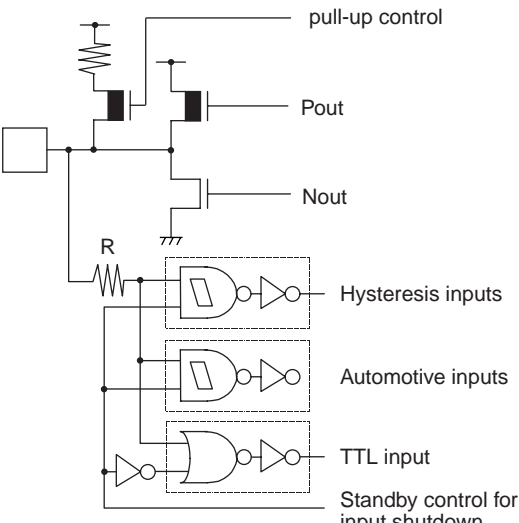
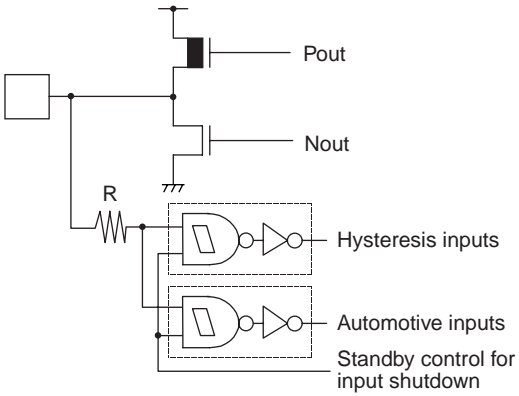
\*2 : FPT-100P-M05

## ■ I/O CIRCUIT TYPE

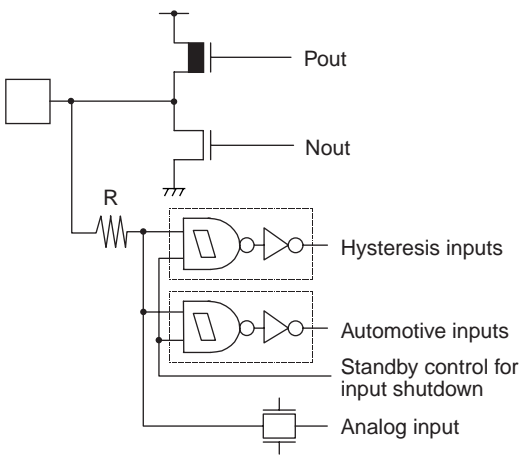
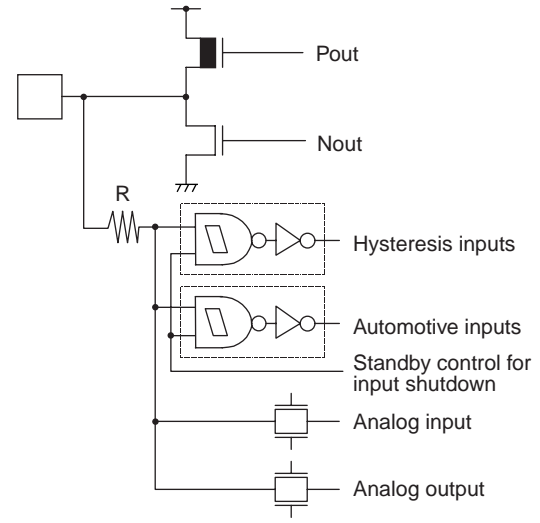
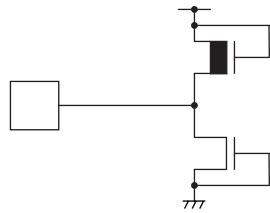
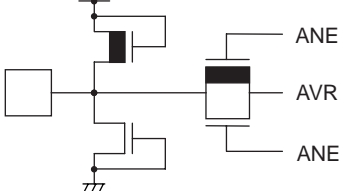
Type	Circuit	Remarks
A		<p>Oscillation circuit</p> <ul style="list-style-type: none"> <li>• High-speed oscillation feedback resistor = approx. 1 MΩ</li> </ul>
B		<p>Oscillation circuit</p> <ul style="list-style-type: none"> <li>• Low-speed oscillation feedback resistor = approx. 10 MΩ</li> </ul>
C		<p>Mask ROM and EVA device:</p> <ul style="list-style-type: none"> <li>• CMOS Hysteresis input pin</li> </ul> <p>Flash device:</p> <ul style="list-style-type: none"> <li>• CMOS input pin</li> </ul>
D		<p>Mask ROM and EVA device:</p> <ul style="list-style-type: none"> <li>• CMOS Hysteresis input pin</li> <li>• Pull-down resistor value: approx. 50 kΩ</li> </ul> <p>Flash device:</p> <ul style="list-style-type: none"> <li>• CMOS input pin</li> <li>• No Pull-down</li> </ul>
E		<p>CMOS Hysteresis input pin</p> <ul style="list-style-type: none"> <li>• Pull-up resistor value: approx. 50 kΩ</li> </ul>

(Continued)

# MB90340 Series

Type	Circuit	Remarks
F	 <p>The circuit diagram for Type F shows a CMOS output stage with a PMOS transistor (Pout) and an NMOS transistor (Nout). A pull-up resistor R is connected to the output node. The input stage consists of three differential pairs: Hysteresis inputs, Automotive inputs, and Standby control for input shutdown.</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> </ul>
G	 <p>The circuit diagram for Type G shows a CMOS output stage with a PMOS transistor (Pout) and an NMOS transistor (Nout). A pull-up control resistor is connected to the output node. A pull-up resistor R is also present. The input stage includes Hysteresis inputs, Automotive inputs, a TTL input, and Standby control for input shutdown.</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• TTL input (With the standby-time input shutdown function)</li> <li>• Programmable pullup resistor: <math>50 \text{ k}\Omega</math> approx.</li> </ul>
H	 <p>The circuit diagram for Type H shows a CMOS output stage with a PMOS transistor (Pout) and an NMOS transistor (Nout). A pull-up resistor R is connected to the output node. The input stage consists of two differential pairs: Hysteresis inputs and Automotive inputs, along with Standby control for input shutdown.</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 3 \text{ mA}</math>, <math>I_{OH} = -3 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> </ul>

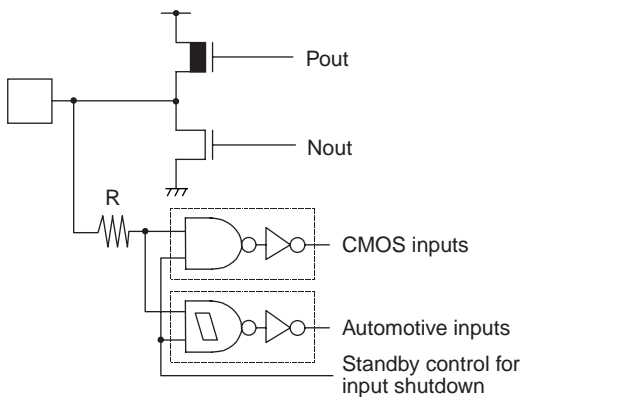
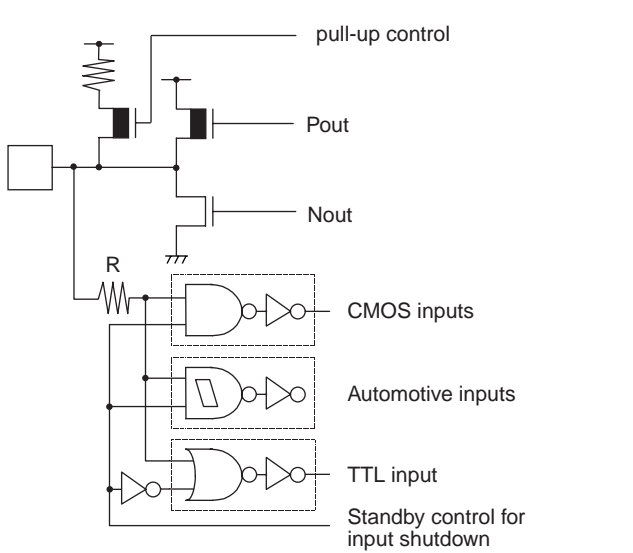
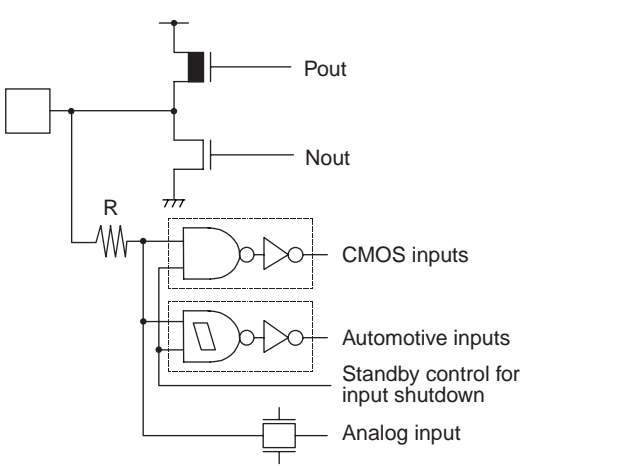
(Continued)

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• A/D analog input</li> </ul>
J		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• D/A analog output</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• A/D analog input</li> </ul>
K		<ul style="list-style-type: none"> <li>• Power supply input protection circuit</li> </ul>
L		<ul style="list-style-type: none"> <li>• A/D converter reference voltage power supply input pin, with the protection circuit</li> <li>• Flash devices do not have a protection circuit against <math>V_{CC}</math> for pin AVRH</li> </ul>

(Continued)

# MB90340 Series

(Continued)

Type	Circuit	Remarks
M		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> </ul>
N		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• TTL input (With the standby-time input shutdown function)</li> </ul> <p>Programmable pullup resistor: 50 k<math>\Omega</math> approx</p>
O		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• A/D analog input</li> </ul>

## ■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Precautions for when not using a sub clock signal
- Notes on during operation of PLL clock mode
- Power supply pins ( $V_{CC}/V_{SS}$ )
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Stabilization of power supply voltage
- Initialization
- Port0 to port3 output during Power-on(**External-bus mode**)
- Notes on using CAN Function
- Flash security Function

### 1. Preventing latch-up

**CMOS IC chips may suffer latch-up under the following conditions :**

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$ .
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AV_{RH}$ ) exceed the digital power-supply voltage.

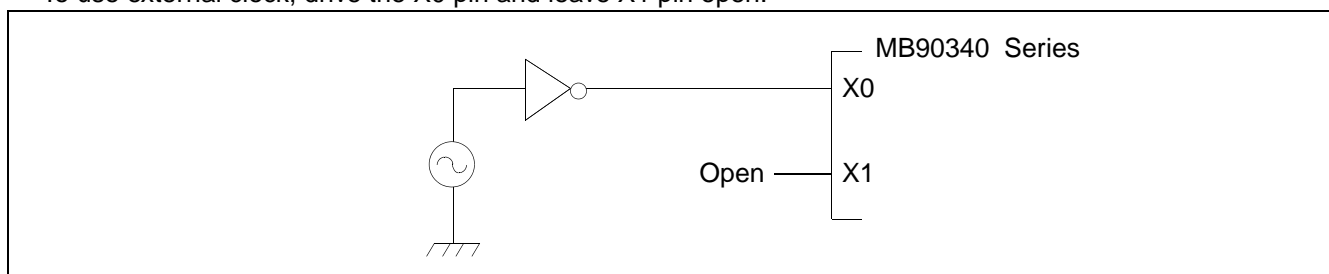
### 2. Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k $\Omega$  .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

### 3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



### 4. Precautions for when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

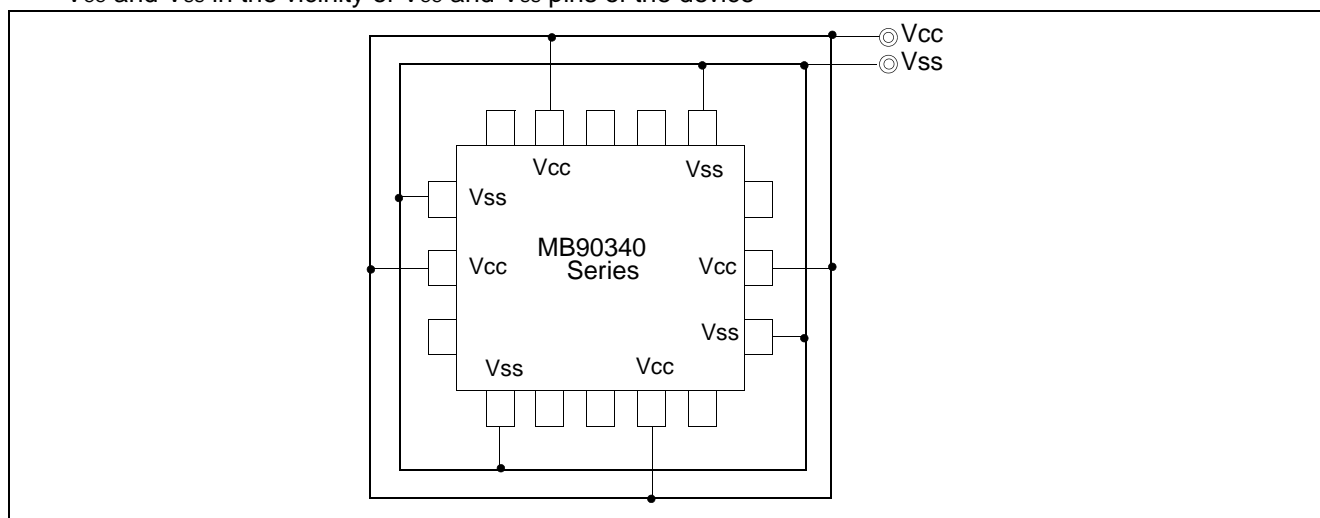
# MB90340 Series

## 5. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## 6. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.  
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally.
- Connect  $V_{CC}$  and  $V_{SS}$  to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1  $\mu\text{F}$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device



## 7. Pull-up/down resistors

The MB90340 Series does not support internal pull-up/down resistors (Port 0 to Port 3: built-in pull-up resistors). Use external components where needed.

## 8. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

## 9. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply ( $AV_{CC}$ ,  $AV_{RH}$ ,  $AV_{RL}$ ) and analog inputs (AN0 to AN23) after turning-on the digital power supply ( $V_{CC}$ ).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed  $AV_{RH}$  or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 10. Connection of Unused Pins of A/D Converter if A/D Converter is used

Connect unused pins of A/D converter to  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$ .



## 11. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more  $\mu\text{s}$  (0.2 V to 2.7 V)

## 12. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified  $V_{\text{CC}}$  supply voltage operating range. Therefore, the  $V_{\text{CC}}$  supply voltage should be stabilized.

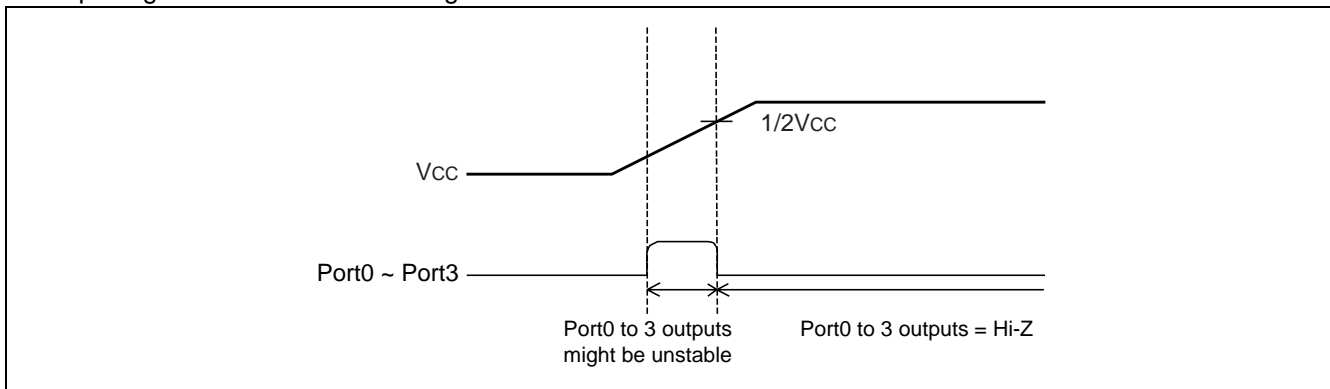
For reference, the supply voltage should be controlled so that  $V_{\text{CC}}$  ripple variations (peak-to-peak value) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard  $V_{\text{CC}}$  supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

## 13. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

## 14. Port 0 to port 3 output during Power-on (External-bus mode)

As shown below, when power is turned on in External-Bus mode, in spite of reset input, there is a possibility that output signal of Port 0 to Port 3 might be unstable.



## 15. Notes on using CAN Function

To use CAN function, please set '1' to DIRECT bit of CAN Direct Mode Register (CDMR).

If DIRECT bit is set to '0' (initial value), wait states will be performed when accessing CAN registers.

Please refer to Hardware Manual of MB90340 series for detail of CAN Direct Mode Register.

## 16. Flash security Function (except for MB90F346A)

The security bit is located in the area of the flash memory.

If protection code 01<sub>H</sub> is written in the security bit, the flash memory is in the protected state by security.

Therefore please do not write 01<sub>H</sub> in this address if you do not use the security function.

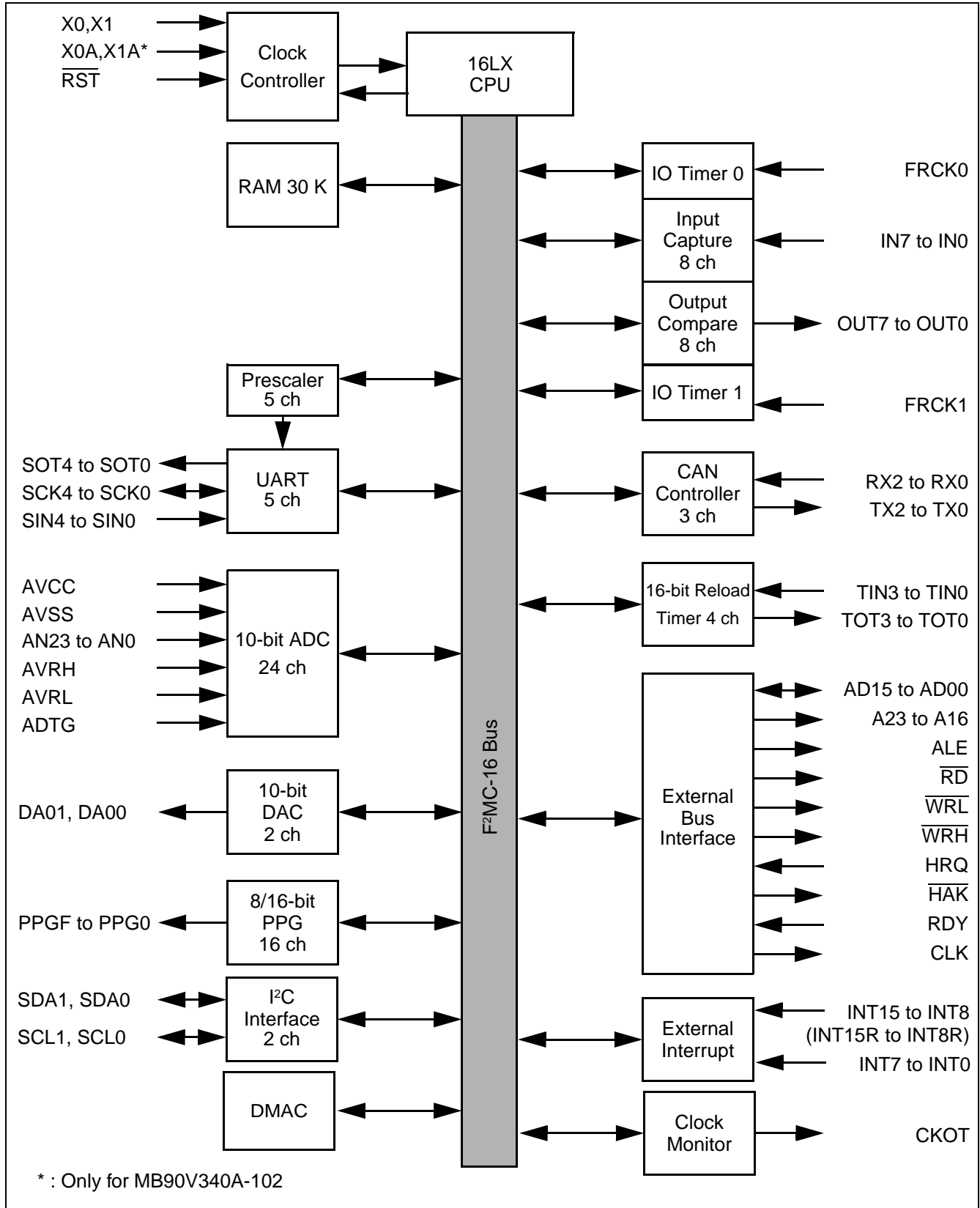
Please refer to following table for the address of the security bit.

	Flash memory size	Address for security bit
MB90F347 MMB90F347A	Embedded 1 Mbit Flash Memory	FE0001 <sub>H</sub>
MB90F342A MB90F349A	Embedded 2 Mbit Flash Memory	FC0001 <sub>H</sub>
MB90F343A	Embedded 3 Mbit Flash Memory	F90001 <sub>H</sub>
MB90F345A	Embedded 4 Mbit Flash Memory	F80001 <sub>H</sub>

# MB90340 Series

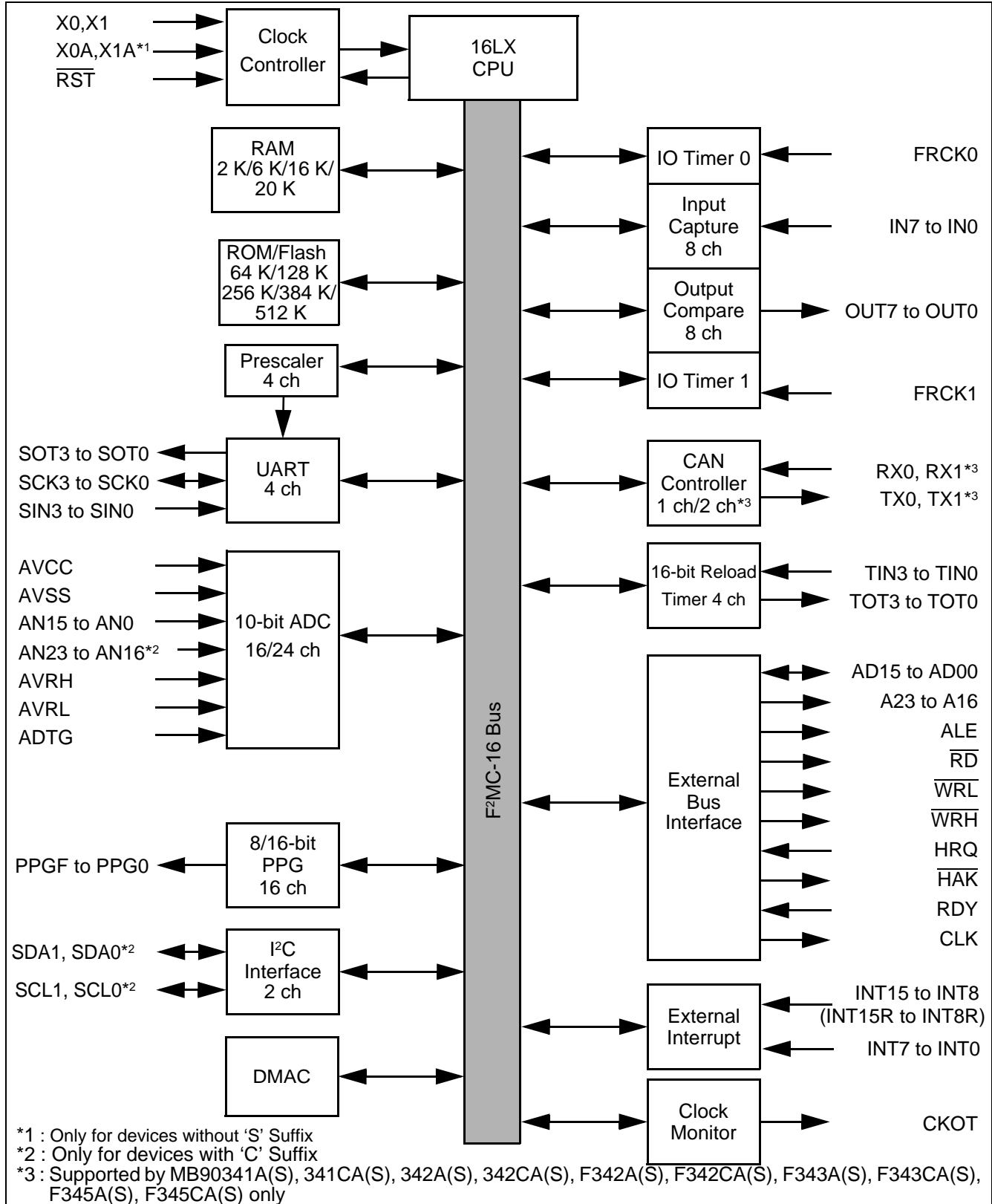
## ■ BLOCK DIAGRAMS

### MB90V340A-101/102



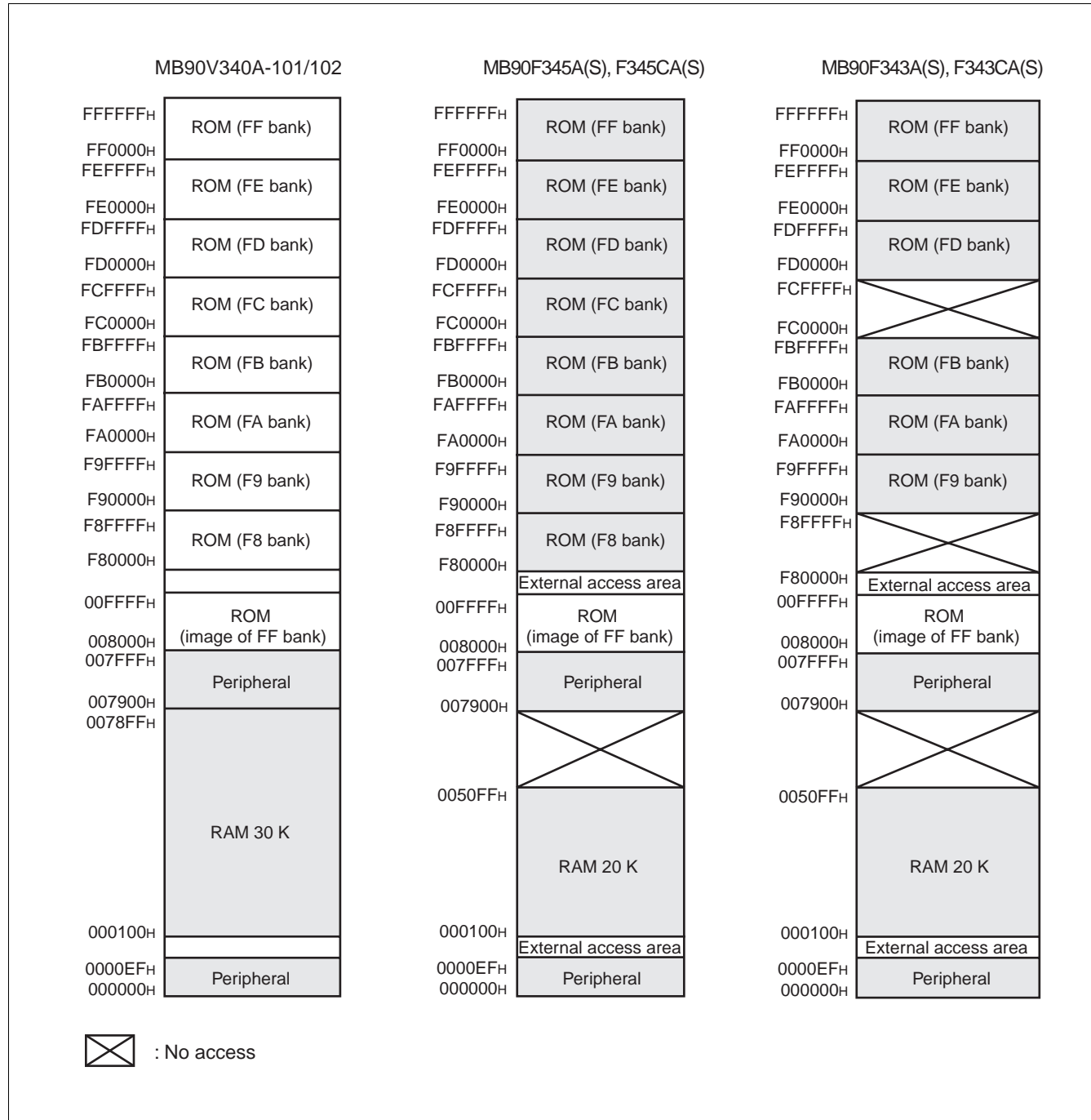
# MB90340 Series

MB90F342A(S), MB90F342CA(S), MB90F343A(S), MB90F343CA(S), MB90F345A(S), MB90F345CA(S), MB90F346A(S), MB90F346CA(S), MB90F347A(S), MB90F347CA(S), MB90F349A(S), MB90F349CA(S), MB90341A(S), MB90341CA(S), MB90342A(S), MB90342CA(S), MB90346A(S), MB90346CA(S), MB90347A(S), MB90347CA(S), MB90348A(S), MB90348CA(S), MB90349A(S), MB90349CA(S)



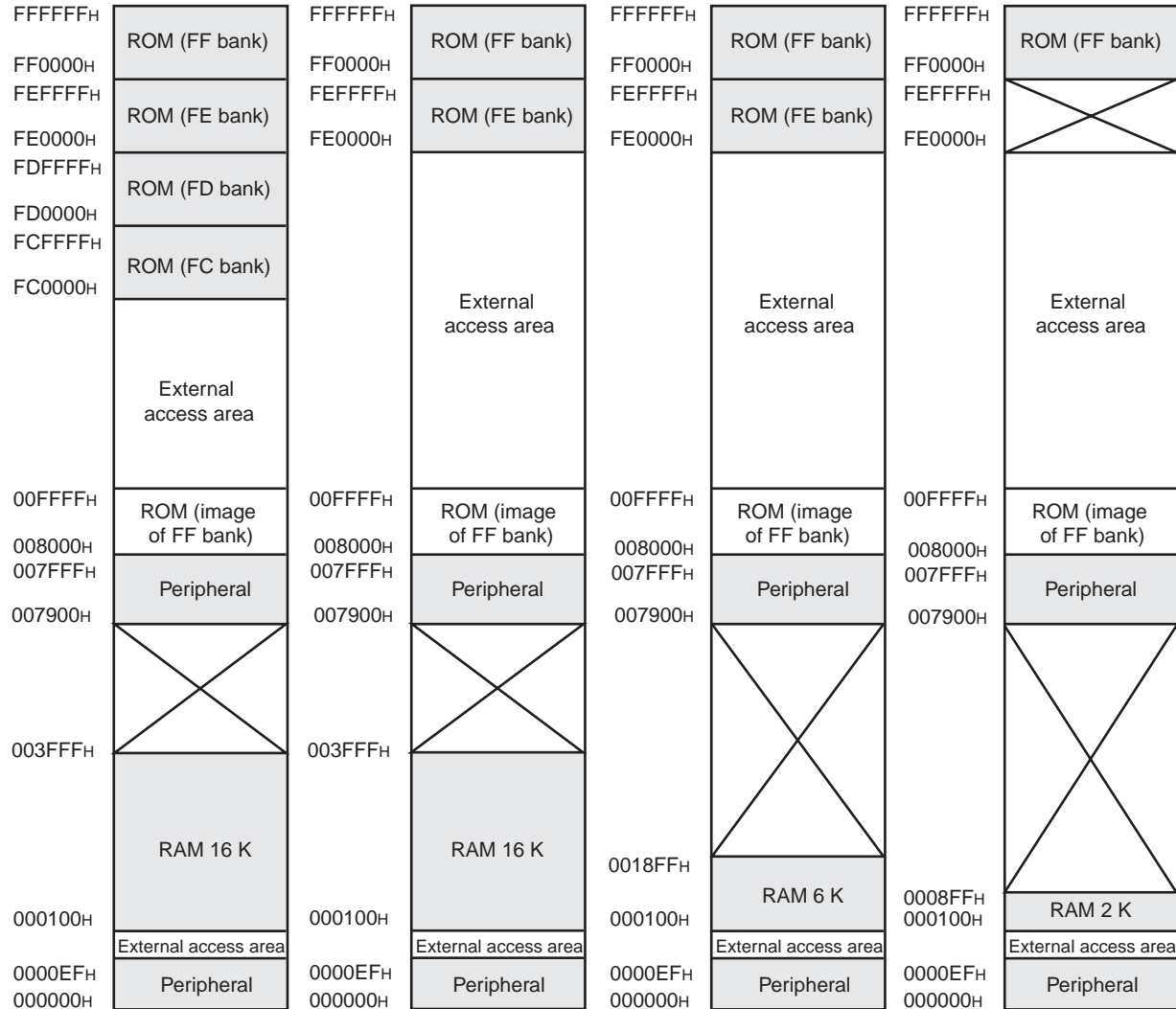
# MB90340 Series

## MEMORY MAP



# MB90340 Series

MB90349A(S), 349CA(S)      MB90348A(S), 348CA(S)      MB90347A(S), 347CA(S)      MB90346A(S), 346CA(S)  
 MB90342A(S), 342CA(S)      MB90341A(S), 341CA(S)      MB90F347(S), F347C(S)      MB90F346A(S), F346CA(S)  
 MB90F349A(S), F349CA(S)      MB90F342A(S), F342CA(S)      MB90F347A(S), F347CA(S)



: No access

Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.

For example, an attempt to access 00C000<sub>H</sub> accesses the value at FFC000<sub>H</sub> in ROM.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

The image between FF8000<sub>H</sub> and FFFFFF<sub>H</sub> is visible in bank 00, while the image between FF0000<sub>H</sub> and FF7FFF<sub>H</sub> is visible only in bank FF.

# MB90340 Series

## ■ I/O MAP

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
00 <sub>H</sub>	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
01 <sub>H</sub>	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
02 <sub>H</sub>	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
03 <sub>H</sub>	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
04 <sub>H</sub>	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
05 <sub>H</sub>	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX
06 <sub>H</sub>	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX
07 <sub>H</sub>	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX
08 <sub>H</sub>	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
09 <sub>H</sub>	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX
0A <sub>H</sub>	Port A data register	PDRA	R/W	Port A	XXXXXXXX
0B <sub>H</sub>	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111
0C <sub>H</sub>	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111
0D <sub>H</sub>	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	11111111
0E <sub>H</sub>	Input level select register 0	ILSR0	R/W	Ports	XXXXXXXX
0F <sub>H</sub>	Input level select register 1	ILSR1	R/W	Ports	XXXX0XXX
10 <sub>H</sub>	Port 0 direction register	DDR0	R/W	Port 0	00000000
11 <sub>H</sub>	Port 1 direction register	DDR1	R/W	Port 1	00000000
12 <sub>H</sub>	Port 2 direction register	DDR2	R/W	Port 2	00000000
13 <sub>H</sub>	Port 3 direction register	DDR3	R/W	Port 3	00000000
14 <sub>H</sub>	Port 4 direction register	DDR4	R/W	Port 4	00000000
15 <sub>H</sub>	Port 5 direction register	DDR5	R/W	Port 5	00000000
16 <sub>H</sub>	Port 6 direction register	DDR6	R/W	Port 6	00000000
17 <sub>H</sub>	Port 7 direction register	DDR7	R/W	Port 7	00000000
18 <sub>H</sub>	Port 8 direction register	DDR8	R/W	Port 8	00000000
19 <sub>H</sub>	Port 9 direction register	DDR9	R/W	Port 9	00000000
1A <sub>H</sub>	Port A direction register	DDRA	R/W	Port A	00000100
1B <sub>H</sub>	Reserved				
1C <sub>H</sub>	Port 0 Pullup control register	PUCR0	R/W	Port 0	00000000
1D <sub>H</sub>	Port 1 Pullup control register	PUCR1	R/W	Port 1	00000000
1E <sub>H</sub>	Port 2 Pullup control register	PUCR2	R/W	Port 2	00000000
1F <sub>H</sub>	Port 3 Pullup control register	PUCR3	W, R/W	Port 3	00000000

(Continued)

# MB90340 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
20 <sub>H</sub>	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000
21 <sub>H</sub>	Serial Control Register 0	SCR0	W,R/W		00000000
22 <sub>H</sub>	Reception/Transmission Data Register 0	RDR0/ TDR0	R/W		00000000
23 <sub>H</sub>	Serial Status Register 0	SSR0	R,R/W		00001000
24 <sub>H</sub>	Extended Communication Control Register 0	ECCR0	R,W,R/ W		000000XX
25 <sub>H</sub>	Extended Status/Control Register 0	ESCR0	R/W		00000100
26 <sub>H</sub>	Baud Rate generator Register 00	BGR00	R/W		00000000
27 <sub>H</sub>	Baud Rate generator Register 01	BGR01	R/W		00000000
28 <sub>H</sub>	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000
29 <sub>H</sub>	Serial Control Register 1	SCR1	W,R/W		00000000
2A <sub>H</sub>	Reception/Transmission Data Register 1	RDR1/ TDR1	R/W		00000000
2B <sub>H</sub>	Serial Status Register 1	SSR1	R,R/W		00001000
2C <sub>H</sub>	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XX
2D <sub>H</sub>	Extended Status/Control Register 1	ESCR1	R/W		00000100
2E <sub>H</sub>	Baud Rate generator Register 10	BGR10	R/W		00000000
2F <sub>H</sub>	Baud Rate generator Register 11	BGR11	R/W		00000000
30 <sub>H</sub>	PPG 0 operation mode control register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1
31 <sub>H</sub>	PPG 1 operation mode control register	PPGC1	W,R/W		0X000001
32 <sub>H</sub>	PPG 0/PPG 1 count clock select register	PPG01	R/W		000000X0
33 <sub>H</sub>	Reserved				
34 <sub>H</sub>	PPG 2 operation mode control register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1
35 <sub>H</sub>	PPG 3 operation mode control register	PPGC3	W,R/W		0X000001
36 <sub>H</sub>	PPG 2/PPG 3 count clock select register	PPG23	R/W		000000X0
37 <sub>H</sub>	Reserved				
38 <sub>H</sub>	PPG 4 operation mode control register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1
39 <sub>H</sub>	PPG 5 operation mode control register	PPGC5	W,R/W		0X000001
3A <sub>H</sub>	PPG 4/PPG 5 clock select register	PPG45	R/W		000000X0
3B <sub>H</sub>	Address detect control register 1	PACSR1	R/W	Address Match Detection 1	00000000
3C <sub>H</sub>	PPG 6 operation mode control register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1
3D <sub>H</sub>	PPG 7 operation mode control register	PPGC7	W,R/W		0X000001
3E <sub>H</sub>	PPG 6/PPG 7 count clock control register	PPG67	R/W		000000X0
3F <sub>H</sub>	Reserved				

(Continued)

# MB90340 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
40H	PPG 8 operation mode control register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1
41H	PPG 9 operation mode control register	PPGC9	W,R/W		0X000001
42H	PPG 8/PPG 9 count clock control register	PPG89	R/W		000000X0
43H	Reserved				
44H	PPG A operation mode control register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1
45H	PPG B operation mode control register	PPGCB	W,R/W		0X000001
46H	PPG A/PPG B count clock select register	PPGAB	R/W		000000X0
47H	Reserved				
48H	PPG C operation mode control register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1
49H	PPG D operation mode control register	PPGCD	W,R/W		0X000001
4AH	PPG C/PPG D count clock select register	PPGCD	R/W		000000X0
4BH	Reserved				
4CH	PPG E operation mode control register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1
4DH	PPG F operation mode control register	PPGCF	W,R/W		0X000001
4EH	PPG E/PPG F count clock select register	PPGEF	R/W		000000X0
4FH	Reserved				
50H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000
51H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX
52H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000
53H	Input Capture Edge 2/3	ICE23	R		XXXXXXXXXX
54H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000
55H	Input Capture Edge 4/5	ICE45	R		XXXXXXXXXX
56H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000
57H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX
58H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00
59H	Output Compare Control Status 1	OCS1	R/W		0XX00000
5AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00
5BH	Output Compare Control Status 3	OCS3	R/W		0XX00000
5CH	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00
5DH	Output Compare Control Status 5	OCS5	R/W		0XX00000
5EH	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00
5FH	Output Compare Control Status 7	OCS7	R/W		0XX00000

(Continued)



# MB90340 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
60H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000
61H	Timer Control Status 0	TMCSR0	R/W		XXXX0000
62H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000
63H	Timer Control Status 1	TMCSR1	R/W		XXXX0000
64H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000
65H	Timer Control Status 2	TMCSR2	R/W		XXXX0000
66H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000
67H	Timer Control Status 3	TMCSR3	R/W		XXXX0000
68H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0
69H	A/D Control Status 1	ADCS1	R/W		0000000X
6AH	A/D Data 0	ADCR0	R		00000000
6BH	A/D Data 1	ADCR1	R		XXXXXXXX00
6CH	ADC Setting 0	ADSR0	R/W		00000000
6DH	ADC Setting 1	ADSR1	R/W		00000000
6EH	Reserved				
6FH	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXXX1
70H to 8FH	Reserved for CAN Interface 0/1. Refer to "■ CAN CONTROLLERS"				
90H to 9AH	Reserved				
9BH	DMA Descriptor Channel Specified	DCSR	R/W	DMA	00000000
9CH	DMA Status L	DSRL	R/W		00000000
9DH	DMA Status H	DSRH	R/W		00000000
9EH	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000
9FH	Delayed Interrupt/release	DIRR	R/W	Delayed Interrupt	XXXXXXXX0
A0H	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000
A1H	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100
A2H, A3H	Reserved				
A4H	DMA Stop Status	DSSR	R/W	DMA	00000000
A5H	Automatic ready function select reg.	ARSR	W	External Memory Access	0011XX00
A6H	External address output control reg.	HACR	W		00000000
A7H	Bus control signal selection register	ECSR	W		0000000X
A8H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111
A9H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100

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# MB90340 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
AA <sub>H</sub>	Watch Timer Control register	WTC	R,R/W	Watch Timer	1X001000
AB <sub>H</sub>	Reserved				
AC <sub>H</sub>	DMA Enable L	DERL	R/W	DMA	00000000
AD <sub>H</sub>	DMA Enable H	DERH	R/W		00000000
AE <sub>H</sub>	Flash Control Status (FlashDevices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000
AF <sub>H</sub>	Reserved				
B0 <sub>H</sub>	Interrupt control register 00	ICR00	W,R/W	Interrupt Control	00000111
B1 <sub>H</sub>	Interrupt control register 01	ICR01	W,R/W		00000111
B2 <sub>H</sub>	Interrupt control register 02	ICR02	W,R/W		00000111
B3 <sub>H</sub>	Interrupt control register 03	ICR03	W,R/W		00000111
B4 <sub>H</sub>	Interrupt control register 04	ICR04	W,R/W		00000111
B5 <sub>H</sub>	Interrupt control register 05	ICR05	W,R/W		00000111
B6 <sub>H</sub>	Interrupt control register 06	ICR06	W,R/W		00000111
B7 <sub>H</sub>	Interrupt control register 07	ICR07	W,R/W		00000111
B8 <sub>H</sub>	Interrupt control register 08	ICR08	W,R/W		00000111
B9 <sub>H</sub>	Interrupt control register 09	ICR09	W,R/W		00000111
BA <sub>H</sub>	Interrupt control register 10	ICR10	W,R/W		00000111
BB <sub>H</sub>	Interrupt control register 11	ICR11	W,R/W		00000111
BC <sub>H</sub>	Interrupt control register 12	ICR12	W,R/W		00000111
BD <sub>H</sub>	Interrupt control register 13	ICR13	W,R/W		00000111
BE <sub>H</sub>	Interrupt control register 14	ICR14	W,R/W		00000111
BF <sub>H</sub>	Interrupt control register 15	ICR15	W,R/W		00000111
C0 <sub>H</sub>	D/A Converter data 0	DAT0	R/W	D/A Converter	XXXXXXXX
C1 <sub>H</sub>	D/A Converter data 1	DAT1	R/W		XXXXXXXX
C2 <sub>H</sub>	D/A Control 0	DACR0	R/W		XXXXXXXX0
C3 <sub>H</sub>	D/A Control 1	DACR1	R/W		XXXXXXXX0
C4 <sub>H</sub> , C5 <sub>H</sub>	Reserved				
C6 <sub>H</sub>	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000
C7 <sub>H</sub>	External Interrupt Source 0	EIRR0	R/W		XXXXXXXX
C8 <sub>H</sub>	External Interrupt Level Setting 0	ELVR0	R/W		00000000
C9 <sub>H</sub>	External Interrupt Level Setting 0	ELVR0	R/W		00000000

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
CA <sub>H</sub>	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000
CB <sub>H</sub>	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX
CC <sub>H</sub>	External Interrupt Level Setting 1	ELVR1	R/W		00000000
CD <sub>H</sub>	External Interrupt Level Setting 1	ELVR1	R/W		00000000
CE <sub>H</sub>	External Interrupt Source Select	EISSR	R/W		00000000
CF <sub>H</sub>	PLL/Subclock Control register	PSCCR	W	PLL	XXXX0000
D0 <sub>H</sub>	DMA Buffer Addrss Pointer L	BAPL	R/W	DMA	XXXXXXXX
D1 <sub>H</sub>	DMA Buffer Addrss Pointer M	BAPM	R/W		XXXXXXXX
D2 <sub>H</sub>	DMA Buffer Addrss Pointer H	BAPH	R/W		XXXXXXXX
D3 <sub>H</sub>	DMA Control	DMACS	R/W		XXXXXXXX
D4 <sub>H</sub>	I/O Register Address Pointer L	IOAL	R/W		XXXXXXXX
D5 <sub>H</sub>	I/O Register Address Pointer H	IOAH	R/W		XXXXXXXX
D6 <sub>H</sub>	Data Counter L	DCTL	R/W		XXXXXXXX
D7 <sub>H</sub>	Data Counter H	DCTH	R/W		XXXXXXXX
D8 <sub>H</sub>	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000
D9 <sub>H</sub>	Serial Control Register 2	SCR2	W,R/W		00000000
DA <sub>H</sub>	Reception/Transmission Data Register 2	RDR2/ TDR2	R/W		00000000
DB <sub>H</sub>	Serial Status Register 2	SSR2	R,R/W		00001000
DC <sub>H</sub>	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX
DD <sub>H</sub>	Extended Status Control Register 2	ESCR2	R/W		00000100
DE <sub>H</sub>	Baud Rate Generator Register 20	BGR20	R/W		00000000
DF <sub>H</sub>	Baud Rate Generator Register 21	BGR21	R/W		00000000
E0 <sub>H</sub> to EF <sub>H</sub>	Reserved for CAN Interface 2. Refer to "■ CAN CONTROLLERS"				
F0 <sub>H</sub> to FF <sub>H</sub>	External				

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
7900 <sub>H</sub>	Reload Register L0	PRL0	R/W	16-bit PPG 0/1	XXXXXXXX
7901 <sub>H</sub>	Reload Register H0	PRLH0	R/W		XXXXXXXX
7902 <sub>H</sub>	Reload Register L1	PRL1	R/W		XXXXXXXX
7903 <sub>H</sub>	Reload Register H1	PRLH1	R/W		XXXXXXXX
7904 <sub>H</sub>	Reload Register L2	PRL2	R/W	16-bit PPG 2/3	XXXXXXXX
7905 <sub>H</sub>	Reload Register H2	PRLH2	R/W		XXXXXXXX
7906 <sub>H</sub>	Reload Register L3	PRL3	R/W		XXXXXXXX
7907 <sub>H</sub>	Reload Register H3	PRLH3	R/W		XXXXXXXX
7908 <sub>H</sub>	Reload Register L4	PRL4	R/W	16-bit PPG 4/5	XXXXXXXX
7909 <sub>H</sub>	Reload Register H4	PRLH4	R/W		XXXXXXXX
790A <sub>H</sub>	Reload Register L5	PRL5	R/W		XXXXXXXX
790B <sub>H</sub>	Reload Register H5	PRLH5	R/W		XXXXXXXX
790C <sub>H</sub>	Reload Register L6	PRL6	R/W	16-bit PPG 6/7	XXXXXXXX
790D <sub>H</sub>	Reload Register H6	PRLH6	R/W		XXXXXXXX
790E <sub>H</sub>	Reload Register L7	PRL7	R/W		XXXXXXXX
790F <sub>H</sub>	Reload Register H7	PRLH7	R/W		XXXXXXXX
7910 <sub>H</sub>	Reload Register L8	PRL8	R/W	16-bit PPG 8/9	XXXXXXXX
7911 <sub>H</sub>	Reload Register H8	PRLH8	R/W		XXXXXXXX
7912 <sub>H</sub>	Reload Register L9	PRL9	R/W		XXXXXXXX
7913 <sub>H</sub>	Reload Register H9	PRLH9	R/W		XXXXXXXX
7914 <sub>H</sub>	Reload Register LA	PRLA	R/W	16-bit PPG A/B	XXXXXXXX
7915 <sub>H</sub>	Reload Register HA	PRLHA	R/W		XXXXXXXX
7916 <sub>H</sub>	Reload Register LB	PRLB	R/W		XXXXXXXX
7917 <sub>H</sub>	Reload Register HB	PRLHB	R/W		XXXXXXXX
7918 <sub>H</sub>	Reload Register LC	PRLC	R/W	16-bit PPG C/D	XXXXXXXX
7919 <sub>H</sub>	Reload Register HC	PRLHC	R/W		XXXXXXXX
791A <sub>H</sub>	Reload Register LD	PRLD	R/W		XXXXXXXX
791B <sub>H</sub>	Reload Register HD	PRLHD	R/W		XXXXXXXX
791C <sub>H</sub>	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX
791D <sub>H</sub>	Reload Register HE	PRLHE	R/W		XXXXXXXX
791E <sub>H</sub>	Reload Register LF	PRLLF	R/W		XXXXXXXX
791F <sub>H</sub>	Reload Register HF	PRLHF	R/W		XXXXXXXX
7920 <sub>H</sub>	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX
7921 <sub>H</sub>	Input Capture 0	IPCP0	R		XXXXXXXX
7922 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX
7923 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX

(Continued)

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
7924 <sub>H</sub>	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXXXX
7925 <sub>H</sub>	Input Capture 2	IPCP2	R		XXXXXXXXXX
7926 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXXXX
7927 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXXXX
7928 <sub>H</sub>	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXXXX
7929 <sub>H</sub>	Input Capture 4	IPCP4	R		XXXXXXXXXX
792A <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXXXX
792B <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXXXX
792C <sub>H</sub>	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXXXX
792D <sub>H</sub>	Input Capture 6	IPCP6	R		XXXXXXXXXX
792E <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXXXX
792F <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXXXX
7930 <sub>H</sub>	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXXX
7931 <sub>H</sub>	Output Compare 0	OCCP0	R/W		XXXXXXXXXX
7932 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXXXX
7933 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXXXX
7934 <sub>H</sub>	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXXX
7935 <sub>H</sub>	Output Compare 2	OCCP2	R/W		XXXXXXXXXX
7936 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXXXX
7937 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXXXX
7938 <sub>H</sub>	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXXXX
7939 <sub>H</sub>	Output Compare 4	OCCP4	R/W		XXXXXXXXXX
793A <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXXXX
793B <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXXXX
793C <sub>H</sub>	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXXXX
793D <sub>H</sub>	Output Compare 6	OCCP6	R/W		XXXXXXXXXX
793E <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXXXX
793F <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXXXX
7940 <sub>H</sub>	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000
7941 <sub>H</sub>	Timer Data 0	TCDT0	R/W		00000000
7942 <sub>H</sub>	Timer Control Status 0	TCCSL0	R/W		00000000
7943 <sub>H</sub>	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXXX
7944 <sub>H</sub>	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000
7945 <sub>H</sub>	Timer Data 1	TCDT1	R/W		00000000
7946 <sub>H</sub>	Timer Control Status 1	TCCSL1	R/W		00000000
7947 <sub>H</sub>	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXXX

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Address	Register	Abbreviation	Access	Resource name	Initial value	
7948 <sub>H</sub>	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX	
7949 <sub>H</sub>			R/W		XXXXXXXX	
794A <sub>H</sub>	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX	
794B <sub>H</sub>			R/W		XXXXXXXX	
794C <sub>H</sub>	Timer 2/Reload 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX	
794D <sub>H</sub>			R/W		XXXXXXXX	
794E <sub>H</sub>	Timer 3/Reload 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX	
794F <sub>H</sub>			R/W		XXXXXXXX	
7950 <sub>H</sub>	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000	
7951 <sub>H</sub>	Serial Control Register 3	SCR3	W,R/W		00000000	
7952 <sub>H</sub>	Reception/Transmission Data Register 3	RDR3/ TDR3	R/W		00000000	
7953 <sub>H</sub>	Serial Status Register 3	SSR3	R,R/W		00001000	
7954 <sub>H</sub>	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX	
7955 <sub>H</sub>	Extended Status Control Register	ESCR3	R/W		00000100	
7956 <sub>H</sub>	Baud Rate Generator Register 30	BGR30	R/W		00000000	
7957 <sub>H</sub>	Baud Rate Generator Register 31	BGR31	R/W		00000000	
7958 <sub>H</sub>	Serial Mode Register 4	SMR4	W,R/W		UART4	00000000
7959 <sub>H</sub>	Serial Control Register 4	SCR4	W,R/W			00000000
795A <sub>H</sub>	Reception/Transmission Data Register 4	RDR4/ TDR4	R/W	00000000		
795B <sub>H</sub>	Serial Status Register 4	SSR4	R,R/W	00001000		
795C <sub>H</sub>	Extended Communication Control Register 4	ECCR4	R,W, R/W	000000XX		
795D <sub>H</sub>	Extended Status Control Register	ESCR4	R/W	00000100		
795E <sub>H</sub>	Baud Rate Generator Register 40	BGR40	R/W	00000000		
795F <sub>H</sub>	Baud Rate generator Register 41	BGR41	R/W	00000000		
7960 <sub>H</sub> to 796B <sub>H</sub>	Reserved					
796C <sub>H</sub>	Clock output enable register	CLKR	R/W	Clock Monitor	XXXX0000	
796D <sub>H</sub>	Reserved					
796E <sub>H</sub>	CAN Direct Mode Register	CDMR	R/W	CAN clock sync	XXXXXXXX0	
796F <sub>H</sub>	CAN switch register	CANSWR	R/W	CAN 0/1	XXXXXXXX00	

(Continued)

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
7970 <sub>H</sub>	I <sup>2</sup> C bus status register 0	IBSR0	R	I <sup>2</sup> C Interface 0	00000000
7971 <sub>H</sub>	I <sup>2</sup> C bus control register 0	IBCR0	W,R/W		00000000
7972 <sub>H</sub>	I <sup>2</sup> C 10 bit slave address register 0	ITBAL0	R/W		00000000
7973 <sub>H</sub>		ITBAH0	R/W		00000000
7974 <sub>H</sub>	I <sup>2</sup> C 10 bit slave address mask register 0	ITMKL0	R/W		11111111
7975 <sub>H</sub>		ITMKH0	R/W		00111111
7976 <sub>H</sub>	I <sup>2</sup> C 7 bit slave address register 0	ISBA0	R/W		00000000
7977 <sub>H</sub>	I <sup>2</sup> C 7 bit slave address mask register 0	ISMK0	R/W		01111111
7978 <sub>H</sub>	I <sup>2</sup> C data register 0	IDAR0	R/W		00000000
7979 <sub>H</sub> , 797A <sub>H</sub>	Reserved				
797B <sub>H</sub>	I <sup>2</sup> C clock control register 0	ICCR0	R/W	I <sup>2</sup> C Interface 0	00011111
797C <sub>H</sub> to 797F <sub>H</sub>	Reserved				
7980 <sub>H</sub>	I <sup>2</sup> C bus status register 1	IBSR1	R	I <sup>2</sup> C Interface 1	00000000
7981 <sub>H</sub>	I <sup>2</sup> C bus control register 1	IBCR1	W,R/W		00000000
7982 <sub>H</sub>	I <sup>2</sup> C 10 bit slave address register 1	ITBAL1	R/W		00000000
7983 <sub>H</sub>		ITBAH1	R/W		00000000
7984 <sub>H</sub>	I <sup>2</sup> C 10 bit slave address mask register 1	ITMKL1	R/W		11111111
7985 <sub>H</sub>		ITMKH1	R/W		00111111
7986 <sub>H</sub>	I <sup>2</sup> C 7 bit slave address register 1	ISBA1	R/W		00000000
7987 <sub>H</sub>	I <sup>2</sup> C 7 bit slave address mask register 1	ISMK1	R/W		01111111
7988 <sub>H</sub>	I <sup>2</sup> C data register 1	IDAR1	R/W		00000000
7989 <sub>H</sub> , 798A <sub>H</sub>	Reserved				
798B <sub>H</sub>	I <sup>2</sup> C clock control register 1	ICCR1	R/W	I <sup>2</sup> C Interface 1	00011111
798C <sub>H</sub> to 79C1 <sub>H</sub>	Reserved				
79C2 <sub>H</sub>	Clock Modulator Control Register	CMCR	R,R/W	Clock Modulator	0001X000
79C3 <sub>H</sub> to 79DF <sub>H</sub>	Reserved				

(Continued)

# MB90340 Series

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
79E0 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX
79E1 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W		XXXXXXXX
79E2 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W		XXXXXXXX
79E3 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX
79E4 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX
79E5 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX
79E6 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX
79E7 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX
79E8 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX
79E9 <sub>H</sub> to 79EF <sub>H</sub>	Reserved				
79F0 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX
79F1 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W		XXXXXXXX
79F2 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W		XXXXXXXX
79F3 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX
79F4 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX
79F5 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX
79F6 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX
79F7 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX
79F8 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX
79F9 <sub>H</sub> to 79FF <sub>H</sub>	Reserved				
7A00 <sub>H</sub> to 7AFF <sub>H</sub>	Reserved for CAN Interface 0. Refer to “■ CAN CONTROLLERS”				
7B00 <sub>H</sub> to 7BFF <sub>H</sub>	Reserved for CAN Interface 0. Refer to “■ CAN CONTROLLERS”				
7C00 <sub>H</sub> to 7CFF <sub>H</sub>	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7D00 <sub>H</sub> to 7DFF <sub>H</sub>	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7E00 <sub>H</sub> to 7EFF <sub>H</sub>	Reserved for CAN Interface 2. Refer to “■ CAN CONTROLLERS”				
7F00 <sub>H</sub> to 7FFF <sub>H</sub>	Reserved for CAN Interface 2. Refer to “■ CAN CONTROLLERS”				

Notes : • Initial value of “X” represents unknown value.

- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.



## ■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbits/s to 2 Mbits/s (when input clock is at 16 MHz)

**List of Control Registers (1)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
000070 <sub>H</sub>	000080 <sub>H</sub>	0000E0 <sub>H</sub>	Message buffer valid register	BVALR	R/W	00000000 00000000
000071 <sub>H</sub>	000081 <sub>H</sub>	0000E1 <sub>H</sub>				
000072 <sub>H</sub>	000082 <sub>H</sub>	0000E2 <sub>H</sub>	Transmit request register	TREQR	R/W	00000000 00000000
000073 <sub>H</sub>	000083 <sub>H</sub>	0000E3 <sub>H</sub>				
000074 <sub>H</sub>	000084 <sub>H</sub>	0000E4 <sub>H</sub>	Transmit cancel register	TCANR	W	00000000 00000000
000075 <sub>H</sub>	000085 <sub>H</sub>	0000E5 <sub>H</sub>				
000076 <sub>H</sub>	000086 <sub>H</sub>	0000E6 <sub>H</sub>	Transmission complete register	TCR	R/W	00000000 00000000
000077 <sub>H</sub>	000087 <sub>H</sub>	0000E7 <sub>H</sub>				
000078 <sub>H</sub>	000088 <sub>H</sub>	0000E8 <sub>H</sub>	Receive complete register	RCR	R/W	00000000 00000000
000079 <sub>H</sub>	000089 <sub>H</sub>	0000E9 <sub>H</sub>				
00007A <sub>H</sub>	00008A <sub>H</sub>	0000EA <sub>H</sub>	Remote request receiving register	RRTRR	R/W	00000000 00000000
00007B <sub>H</sub>	00008B <sub>H</sub>	0000EB <sub>H</sub>				
00007C <sub>H</sub>	00008C <sub>H</sub>	0000EC <sub>H</sub>	Receive overrun register	ROVRR	R/W	00000000 00000000
00007D <sub>H</sub>	00008D <sub>H</sub>	0000ED <sub>H</sub>				
00007E <sub>H</sub>	00008E <sub>H</sub>	0000EE <sub>H</sub>	Reception interrupt enable register	RIER	R/W	00000000 00000000
00007F <sub>H</sub>	00008F <sub>H</sub>	0000EF <sub>H</sub>				

# MB90340 Series

List of Control Registers (2)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007B00 <sub>H</sub>	007D00 <sub>H</sub>	007F00 <sub>H</sub>	Control status register	CSR	R/W, W R/W, R	0XXXX0X1 00XXXX00
007B01 <sub>H</sub>	007D01 <sub>H</sub>	007F01 <sub>H</sub>				
007B02 <sub>H</sub>	007D02 <sub>H</sub>	007F02 <sub>H</sub>	Last event indicator register	LEIR	R/W	000X0000 XXXXXXXX
007B03 <sub>H</sub>	007D03 <sub>H</sub>	007F03 <sub>H</sub>				
007B04 <sub>H</sub>	007D04 <sub>H</sub>	007F04 <sub>H</sub>	Receive and transmit error counter	RTEC	R	00000000 00000000
007B05 <sub>H</sub>	007D05 <sub>H</sub>	007F05 <sub>H</sub>				
007B06 <sub>H</sub>	007D06 <sub>H</sub>	007F06 <sub>H</sub>	Bit timing register	BTR	R/W	11111111 X1111111
007B07 <sub>H</sub>	007D07 <sub>H</sub>	007F07 <sub>H</sub>				
007B08 <sub>H</sub>	007D08 <sub>H</sub>	007F08 <sub>H</sub>	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX
007B09 <sub>H</sub>	007D09 <sub>H</sub>	007F09 <sub>H</sub>				
007B0A <sub>H</sub>	007D0A <sub>H</sub>	007F0A <sub>H</sub>	Transmit RTR register	TRTRR	R/W	00000000 00000000
007B0B <sub>H</sub>	007D0B <sub>H</sub>	007F0B <sub>H</sub>				
007B0C <sub>H</sub>	007D0C <sub>H</sub>	007F0C <sub>H</sub>	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX
007B0D <sub>H</sub>	007D0D <sub>H</sub>	007F0D <sub>H</sub>				
007B0E <sub>H</sub>	007D0E <sub>H</sub>	007F0E <sub>H</sub>	Transmit interrupt enable register	TIER	R/W	00000000 00000000
007B0F <sub>H</sub>	007D0F <sub>H</sub>	007F0F <sub>H</sub>				
007B10 <sub>H</sub>	007D10 <sub>H</sub>	007F10 <sub>H</sub>	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX
007B11 <sub>H</sub>	007D11 <sub>H</sub>	007F11 <sub>H</sub>				
007B12 <sub>H</sub>	007D12 <sub>H</sub>	007F12 <sub>H</sub>				XXXXXXXX XXXXXXXX
007B13 <sub>H</sub>	007D13 <sub>H</sub>	007F13 <sub>H</sub>				
007B14 <sub>H</sub>	007D14 <sub>H</sub>	007F14 <sub>H</sub>	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX
007B15 <sub>H</sub>	007D15 <sub>H</sub>	007F15 <sub>H</sub>				
007B16 <sub>H</sub>	007D16 <sub>H</sub>	007F16 <sub>H</sub>				XXXXXXXX XXXXXXXX
007B17 <sub>H</sub>	007D17 <sub>H</sub>	007F17 <sub>H</sub>				
007B18 <sub>H</sub>	007D18 <sub>H</sub>	007F18 <sub>H</sub>	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX
007B19 <sub>H</sub>	007D19 <sub>H</sub>	007F19 <sub>H</sub>				
007B1A <sub>H</sub>	007D1A <sub>H</sub>	007F1A <sub>H</sub>				XXXXXXXX XXXXXXXX
007B1B <sub>H</sub>	007D1B <sub>H</sub>	007F1B <sub>H</sub>				

List of Message Buffers (ID Registers) (1)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A00H to 007A1FH	007C00H to 007C1FH	007E00H to 007E1FH	General- purpose RAM	—	R/W	XXXXXXXXX to XXXXXXXXX
007A20H	007C20H	007E20H	ID register 0	IDR0	R/W	XXXXXXXXX XXXXXXXXX
007A21H	007C21H	007E21H				
007A22H	007C22H	007E22H				
007A23H	007C23H	007E23H				XXXXXXXXX XXXXXXXXX
007A24H	007C24H	007E24H	ID register 1	IDR1	R/W	XXXXXXXXX XXXXXXXXX
007A25H	007C25H	007E25H				
007A26H	007C26H	007E26H				
007A27H	007C27H	007E27H				XXXXXXXXX XXXXXXXXX
007A28H	007C28H	007E28H	ID register 2	IDR2	R/W	XXXXXXXXX XXXXXXXXX
007A29H	007C29H	007E29H				
007A2AH	007C2AH	007E2AH				
007A2BH	007C2BH	007E2BH				XXXXXXXXX XXXXXXXXX
007A2CH	007C2CH	007E2CH	ID register 3	IDR3	R/W	XXXXXXXXX XXXXXXXXX
007A2DH	007C2DH	007E2DH				
007A2EH	007C2EH	007E2EH				
007A2FH	007C2FH	007E2FH				XXXXXXXXX XXXXXXXXX
007A30H	007C30H	007E30H	ID register 4	IDR4	R/W	XXXXXXXXX XXXXXXXXX
007A31H	007C31H	007E31H				
007A32H	007C32H	007E32H				
007A33H	007C33H	007E33H				XXXXXXXXX XXXXXXXXX
007A34H	007C34H	007E34H	ID register 5	IDR5	R/W	XXXXXXXXX XXXXXXXXX
007A35H	007C35H	007E35H				
007A36H	007C36H	007E36H				
007A37H	007C37H	007E37H				XXXXXXXXX XXXXXXXXX
007A38H	007C38H	007E38H	ID register 6	IDR6	R/W	XXXXXXXXX XXXXXXXXX
007A39H	007C39H	007E39H				
007A3AH	007C3AH	007E3AH				
007A3BH	007C3BH	007E3BH				XXXXXXXXX XXXXXXXXX
007A3CH	007C3CH	007E3CH	ID register 7	IDR7	R/W	XXXXXXXXX XXXXXXXXX
007A3DH	007C3DH	007E3DH				
007A3EH	007C3EH	007E3EH				
007A3FH	007C3FH	007E3FH				XXXXXXXXX XXXXXXXXX

# MB90340 Series

List of Message Buffers (ID Registers) (2)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A40 <sub>H</sub>	007C40 <sub>H</sub>	007E40 <sub>H</sub>	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX
007A41 <sub>H</sub>	007C41 <sub>H</sub>	007E41 <sub>H</sub>				
007A42 <sub>H</sub>	007C42 <sub>H</sub>	007E42 <sub>H</sub>				
007A43 <sub>H</sub>	007C43 <sub>H</sub>	007E43 <sub>H</sub>				XXXXXXXX XXXXXXXX
007A44 <sub>H</sub>	007C44 <sub>H</sub>	007E44 <sub>H</sub>	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX
007A45 <sub>H</sub>	007C45 <sub>H</sub>	007E45 <sub>H</sub>				
007A46 <sub>H</sub>	007C46 <sub>H</sub>	007E46 <sub>H</sub>				
007A47 <sub>H</sub>	007C47 <sub>H</sub>	007E47 <sub>H</sub>				XXXXXXXX XXXXXXXX
007A48 <sub>H</sub>	007C48 <sub>H</sub>	007E48 <sub>H</sub>	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX
007A49 <sub>H</sub>	007C49 <sub>H</sub>	007E49 <sub>H</sub>				
007A4A <sub>H</sub>	007C4A <sub>H</sub>	007E4A <sub>H</sub>				
007A4B <sub>H</sub>	007C4B <sub>H</sub>	007E4B <sub>H</sub>				XXXXXXXX XXXXXXXX
007A4C <sub>H</sub>	007C4C <sub>H</sub>	007E4C <sub>H</sub>	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX
007A4D <sub>H</sub>	007C4D <sub>H</sub>	007E4D <sub>H</sub>				
007A4E <sub>H</sub>	007C4E <sub>H</sub>	007E4E <sub>H</sub>				
007A4F <sub>H</sub>	007C4F <sub>H</sub>	007E4F <sub>H</sub>				XXXXXXXX XXXXXXXX
007A50 <sub>H</sub>	007C50 <sub>H</sub>	007E50 <sub>H</sub>	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX
007A51 <sub>H</sub>	007C51 <sub>H</sub>	007E51 <sub>H</sub>				
007A52 <sub>H</sub>	007C52 <sub>H</sub>	007E52 <sub>H</sub>				
007A53 <sub>H</sub>	007C53 <sub>H</sub>	007E53 <sub>H</sub>				XXXXXXXX XXXXXXXX
007A54 <sub>H</sub>	007C54 <sub>H</sub>	007E54 <sub>H</sub>	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX
007A55 <sub>H</sub>	007C55 <sub>H</sub>	007E55 <sub>H</sub>				
007A56 <sub>H</sub>	007C56 <sub>H</sub>	007E56 <sub>H</sub>				
007A57 <sub>H</sub>	007C57 <sub>H</sub>	007E57 <sub>H</sub>				XXXXXXXX XXXXXXXX
007A58 <sub>H</sub>	007C58 <sub>H</sub>	007E58 <sub>H</sub>	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX
007A59 <sub>H</sub>	007C59 <sub>H</sub>	007E59 <sub>H</sub>				
007A5A <sub>H</sub>	007C5A <sub>H</sub>	007E5A <sub>H</sub>				
007A5B <sub>H</sub>	007C5B <sub>H</sub>	007E5B <sub>H</sub>				XXXXXXXX XXXXXXXX
007A5C <sub>H</sub>	007C5C <sub>H</sub>	007E5C <sub>H</sub>	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX
007A5D <sub>H</sub>	007C5D <sub>H</sub>	007E5D <sub>H</sub>				
007A5E <sub>H</sub>	007C5E <sub>H</sub>	007E5E <sub>H</sub>				
007A5F <sub>H</sub>	007C5F <sub>H</sub>	007E5F <sub>H</sub>				XXXXXXXX XXXXXXXX

List of Message Buffers (DLC Registers and Data Registers) (1)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A60H	007C60H	007E60H	DLC register 0	DLCR0	R/W	XXXXXXXX
007A61H	007C61H	007E61H				
007A62H	007C62H	007E62H	DLC register 1	DLCR1	R/W	XXXXXXXX
007A63H	007C63H	007E63H				
007A64H	007C64H	007E64H	DLC register 2	DLCR2	R/W	XXXXXXXX
007A65H	007C65H	007E65H				
007A66H	007C66H	007E66H	DLC register 3	DLCR3	R/W	XXXXXXXX
007A67H	007C67H	007E67H				
007A68H	007C68H	007E68H	DLC register 4	DLCR4	R/W	XXXXXXXX
007A69H	007C69H	007E69H				
007A6AH	007C6AH	007E6AH	DLC register 5	DLCR5	R/W	XXXXXXXX
007A6BH	007C6BH	007E6BH				
007A6CH	007C6CH	007E6CH	DLC register 6	DLCR6	R/W	XXXXXXXX
007A6DH	007C6DH	007E6DH				
007A6EH	007C6EH	007E6EH	DLC register 7	DLCR7	R/W	XXXXXXXX
007A6FH	007C6FH	007E6FH				
007A70H	007C70H	007E70H	DLC register 8	DLCR8	R/W	XXXXXXXX
007A71H	007C71H	007E71H				
007A72H	007C72H	007E72H	DLC register 9	DLCR9	R/W	XXXXXXXX
007A73H	007C73H	007E73H				
007A74H	007C74H	007E74H	DLC register 10	DLCR10	R/W	XXXXXXXX
007A75H	007C75H	007E75H				
007A76H	007C76H	007E76H	DLC register 11	DLCR11	R/W	XXXXXXXX
007A77H	007C77H	007E77H				
007A78H	007C78H	007E78H	DLC register 12	DLCR12	R/W	XXXXXXXX
007A79H	007C79H	007E79H				
007A7AH	007C7AH	007E7AH	DLC register 13	DLCR13	R/W	XXXXXXXX
007A7BH	007C7BH	007E7BH				
007A7CH	007C7CH	007E7CH	DLC register 14	DLCR14	R/W	XXXXXXXX
007A7DH	007C7DH	007E7DH				
007A7EH	007C7EH	007E7EH	DLC register 15	DLCR15	R/W	XXXXXXXX
007A7FH	007C7FH	007E7FH				

# MB90340 Series

List of Message Buffers (DLC Registers and Data Registers) (2)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A80 <sub>H</sub> to 007A87 <sub>H</sub>	007C80 <sub>H</sub> to 007C87 <sub>H</sub>	007E80 <sub>H</sub> to 007E87 <sub>H</sub>	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX to XXXXXXXX
007A88 <sub>H</sub> to 007A8F <sub>H</sub>	007C88 <sub>H</sub> to 007C8F <sub>H</sub>	007E88 <sub>H</sub> to 007E8F <sub>H</sub>	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX to XXXXXXXX
007A90 <sub>H</sub> to 007A97 <sub>H</sub>	007C90 <sub>H</sub> to 007C97 <sub>H</sub>	007E90 <sub>H</sub> to 007E97 <sub>H</sub>	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX to XXXXXXXX
007A98 <sub>H</sub> to 007A9F <sub>H</sub>	007C98 <sub>H</sub> to 007C9F <sub>H</sub>	007E98 <sub>H</sub> to 007E9F <sub>H</sub>	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX to XXXXXXXX
007AA0 <sub>H</sub> to 007AA7 <sub>H</sub>	007CA0 <sub>H</sub> to 007CA7 <sub>H</sub>	007EA0 <sub>H</sub> to 007EA7 <sub>H</sub>	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX to XXXXXXXX
007AA8 <sub>H</sub> to 007AAF <sub>H</sub>	007CA8 <sub>H</sub> to 007CAF <sub>H</sub>	007EA8 <sub>H</sub> to 007EAF <sub>H</sub>	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX to XXXXXXXX
007AB0 <sub>H</sub> to 007AB7 <sub>H</sub>	007CB0 <sub>H</sub> to 007CB7 <sub>H</sub>	007EB0 <sub>H</sub> to 007EB7 <sub>H</sub>	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX to XXXXXXXX
007AB8 <sub>H</sub> to 007ABF <sub>H</sub>	007CB8 <sub>H</sub> to 007CBF <sub>H</sub>	007EB8 <sub>H</sub> to 007EBF <sub>H</sub>	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX to XXXXXXXX
007AC0 <sub>H</sub> to 007AC7 <sub>H</sub>	007CC0 <sub>H</sub> to 007CC7 <sub>H</sub>	007EC0 <sub>H</sub> to 007EC7 <sub>H</sub>	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX to XXXXXXXX
007AC8 <sub>H</sub> to 007ACF <sub>H</sub>	007CC8 <sub>H</sub> to 007CCF <sub>H</sub>	007EC8 <sub>H</sub> to 007ECF <sub>H</sub>	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX to XXXXXXXX
007AD0 <sub>H</sub> to 007AD7 <sub>H</sub>	007CD0 <sub>H</sub> to 007CD7 <sub>H</sub>	007ED0 <sub>H</sub> to 007ED7 <sub>H</sub>	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX to XXXXXXXX
007AD8 <sub>H</sub> to 007ADF <sub>H</sub>	007CD8 <sub>H</sub> to 007CDF <sub>H</sub>	007ED8 <sub>H</sub> to 007EDF <sub>H</sub>	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX to XXXXXXXX
007AE0 <sub>H</sub> to 007AE7 <sub>H</sub>	007CE0 <sub>H</sub> to 007CE7 <sub>H</sub>	007EE0 <sub>H</sub> to 007EE7 <sub>H</sub>	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX to XXXXXXXX
007AE8 <sub>H</sub> to 007AEF <sub>H</sub>	007CE8 <sub>H</sub> to 007CEF <sub>H</sub>	007EE8 <sub>H</sub> to 007EEF <sub>H</sub>	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX to XXXXXXXX

# MB90340 Series

List of Message Buffers (DLC Registers and Data Registers) (3)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007AF0 <sub>H</sub> to 007AF7 <sub>H</sub>	007CF0 <sub>H</sub> to 007CF7 <sub>H</sub>	007EF0 <sub>H</sub> to 007EF7 <sub>H</sub>	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX to XXXXXXXX
007AF8 <sub>H</sub> to 007AFF <sub>H</sub>	007CF8 <sub>H</sub> to 007CFF <sub>H</sub>	007EF8 <sub>H</sub> to 007EFF <sub>H</sub>	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX to XXXXXXXX

# MB90340 Series

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI <sup>2</sup> OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC <sub>H</sub>	—	—
INT9 instruction	N	—	#09	FFFFD8 <sub>H</sub>	—	—
Exception	N	—	#10	FFFFD4 <sub>H</sub>	—	—
CAN 0 RX	N	—	#11	FFFFD0 <sub>H</sub>	ICR00	0000B0 <sub>H</sub>
CAN 0 TX/NS	N	—	#12	FFFFCC <sub>H</sub>		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 <sub>H</sub>	ICR01	0000B1 <sub>H</sub>
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 <sub>H</sub>		
CAN 2 RX / I <sup>2</sup> C0	N	—	#15	FFFFC0 <sub>H</sub>	ICR02	0000B2 <sub>H</sub>
CAN 2 TX/NS	N	—	#16	FFFFBC <sub>H</sub>		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 <sub>H</sub>	ICR03	0000B3 <sub>H</sub>
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 <sub>H</sub>		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 <sub>H</sub>	ICR04	0000B4 <sub>H</sub>
16-bit Reload Timer 3	Y1	—	#20	FFFFAC <sub>H</sub>		
PPG 0/1/4/5	N	—	#21	FFFFA8 <sub>H</sub>	ICR05	0000B5 <sub>H</sub>
PPG 2/3/6/7	N	—	#22	FFFFA4 <sub>H</sub>		
PPG 8/9/C/D	N	—	#23	FFFFA0 <sub>H</sub>	ICR06	0000B6 <sub>H</sub>
PPG A/B/E/F	N	—	#24	FFFF9C <sub>H</sub>		
Time Base Timer	N	—	#25	FFFF98 <sub>H</sub>	ICR07	0000B7 <sub>H</sub>
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 <sub>H</sub>		
Watch Timer	N	—	#27	FFFF90 <sub>H</sub>	ICR08	0000B8 <sub>H</sub>
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C <sub>H</sub>		
A/D Converter	Y1	5	#29	FFFF88 <sub>H</sub>	ICR09	0000B9 <sub>H</sub>
I/O Timer 0 / I/O Timer 1	N	—	#30	FFFF84 <sub>H</sub>		
Input Capture 4/5 / I <sup>2</sup> C1	Y1	6	#31	FFFF80 <sub>H</sub>	ICR10	0000BA <sub>H</sub>
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C <sub>H</sub>		
Input Capture 0 to 3	Y1	8	#33	FFFF78 <sub>H</sub>	ICR11	0000BB <sub>H</sub>
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 <sub>H</sub>		
UART 0 RX	Y2	10	#35	FFFF70 <sub>H</sub>	ICR12	0000BC <sub>H</sub>
UART 0 TX	Y1	11	#36	FFFF6C <sub>H</sub>		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 <sub>H</sub>	ICR13	0000BD <sub>H</sub>
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 <sub>H</sub>		

(Continued)



(Continued)

Interrupt cause	EI <sup>2</sup> OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	FFFF60H	ICR14	0000BEH
UART 2 TX / UART 4 TX	Y1	15	#40	FFFF5CH		
Flash Memory	N	—	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt	N	—	#42	FFFF54H		

Y1 : Usable

Y2 : Usable, with EI<sup>2</sup>OS stop function

N : Unusable

- Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
  - When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
  - When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

# MB90340 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

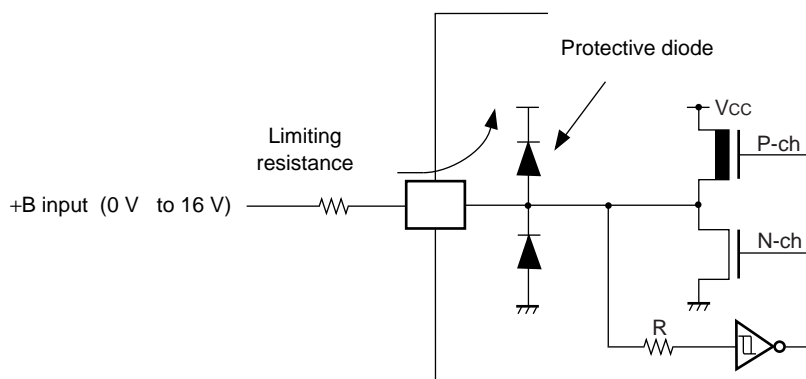
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC} \times 1$
	$AV_{RH}$ , $AV_{RL}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AV_{RH}$ , $AV_{CC} \geq AV_{RL}$ , $AV_{RH} \geq AV_{RL}$
Input voltage	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum Clamp Current	$I_{CLAMP}$	-4.0	+4.0	mA	*4
Total Maximum Clamp Current	$\Sigma I_{CLAMP} $	—	40	mA	*4
"L" level maximum output current	$I_{OL}$	—	15	mA	*3
"L" level average output current	$I_{OLAV}$	—	4	mA	*3
"L" level maximum overall output current	$\Sigma I_{OL}$	—	100	mA	*3
"L" level average overall output current	$\Sigma I_{OLAV}$	—	50	mA	*3
"H" level maximum output current	$I_{OH}$	—	-15	mA	*3
"H" level average output current	$I_{OHAV}$	—	-4	mA	*3
"H" level maximum overall output current	$\Sigma I_{OH}$	—	-100	mA	*3
"H" level average overall output current	$\Sigma I_{OHAV}$	—	-50	mA	*3
Power consumption	$P_D$	—	340	mW	MB90F347
Operating temperature	$T_A$	-40	+105	°C	
Storage temperature	$T_{STG}$	-55	+150	°C	

(Continued)

(Continued)

- \*1: Set  $AV_{CC}$  and  $V_{CC}$  to the same voltage. Make sure that  $AV_{CC}$  does not exceed  $V_{CC}$  and that the voltage at the analog inputs does not exceed  $AV_{CC}$  when the power is switched on.
- \*2:  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3$  V.  $V_I$  should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supercedes the  $V_I$  rating.
- \*3: Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
- \*4:
  - Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (EVA device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
  - Use within recommended operating conditions.
  - Use at DC voltage (current)
  - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
  - Care must be taken not to leave the +B input pin open.
  - Sample recommended circuits:

• Input/output equivalent circuits



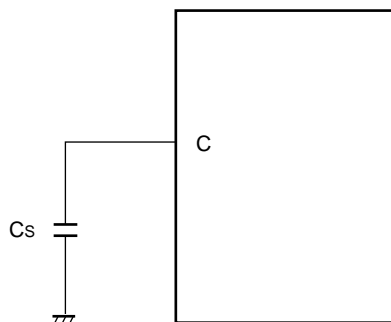
**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB90340 Series

## 2. Recommended Conditions

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}, AV_{CC}$	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	$C_s$	0.1	—	1.0	$\mu\text{F}$	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the $V_{CC}$ should be greater than this capacitor.
Operating temperature	$T_A$	-40	—	+105	$^{\circ}\text{C}$	



**C Pin Connection Diagram**

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB90340 Series

## 3. DC Characteristics

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{IHS}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P83)
	$V_{IHA}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if AUTOMOTIVE input levels are selected
	$V_{IHT}$	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	$V_{IHS}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{IHI}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{IHR}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{RST}$ input pin (CMOS hysteresis)
	$V_{IHM}$	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P83)
	$V_{ILA}$	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if AUTOMOTIVE input levels are selected
	$V_{ILT}$	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{ILI}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{ILR}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{RST}$ input pin (CMOS hysteresis)
	$V_{ILM}$	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	$V_{OH}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	$V_{OHI}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	$V_{OL}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	$V_{OLI}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

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# MB90340 Series

(Continued)

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	$I_{IL}$	—	$V_{CC} = 5.5\text{ V}$ , $V_{SS} < V_i < V_{CC}$	-1	—	1	$\mu\text{A}$	
Pull-up resistance	$R_{UP}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	$R_{DOWN}$	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash devices
Power supply current*	$I_{CC}$	$V_{CC}$	$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At normal operation.	—	55	70	$\text{mA}$	
			$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At writing FLASH memory.	—	70	85	$\text{mA}$	Flash devices
			$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At erasing FLASH memory.	—	75	90	$\text{mA}$	Flash devices
	$I_{CCS}$		$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At Sleep mode.	—	25	35	$\text{mA}$	
	$I_{CTS}$		$V_{CC} = 5.0\text{ V}$ , Internal frequency : 2 MHz, At Main Timer mode	—	0.3	0.8	$\text{mA}$	
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	4	7	$\text{mA}$	
	$I_{CCL}$		$V_{CC} = 5.0\text{ V}$ Internal frequency: 8 kHz, At sub operation $T_A = +25^\circ\text{C}$	—	70	140	$\mu\text{A}$	
	$I_{CCLS}$		$V_{CC} = 5.0\text{ V}$ Internal frequency: 8 kHz, At sub sleep $T_A = +25^\circ\text{C}$	—	20	50	$\mu\text{A}$	
	$I_{CCT}$		$V_{CC} = 5.0\text{ V}$ Internal frequency: 8 kHz, At watch mode $T_A = +25^\circ\text{C}$	—	10	35	$\mu\text{A}$	
	$I_{CCH}$		$V_{CC} = 5.0\text{ V}$ , At Stop mode, $T_A = +25^\circ\text{C}$	—	7	25	$\mu\text{A}$	
Input capacity	$C_{IN}$	Other than C, $AV_{CC}$ , $AV_{SS}$ , $AVRH$ , $AVRL$ , $V_{CC}$ , $V_{SS}$ ,	—	—	5	15	$\text{pF}$	

\* : The power supply current is measured with an external clock.

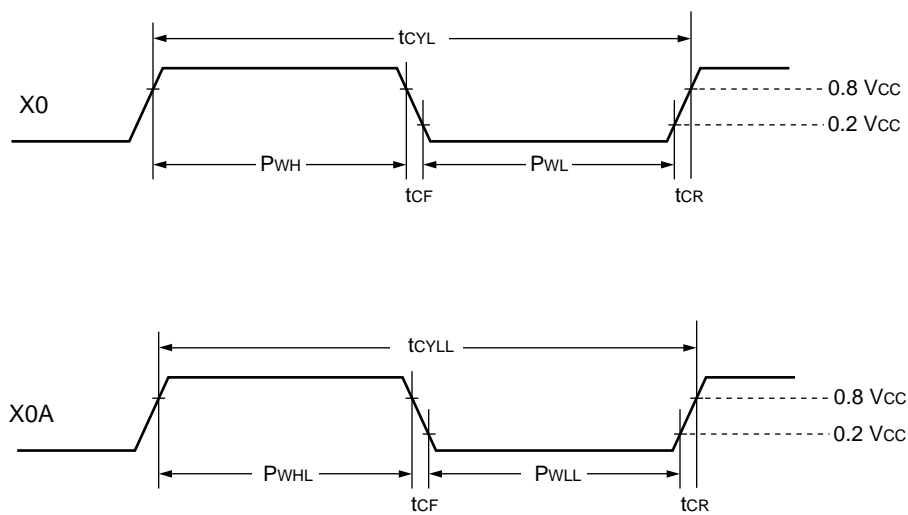
## 4. AC Characteristics

### (1) Clock Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

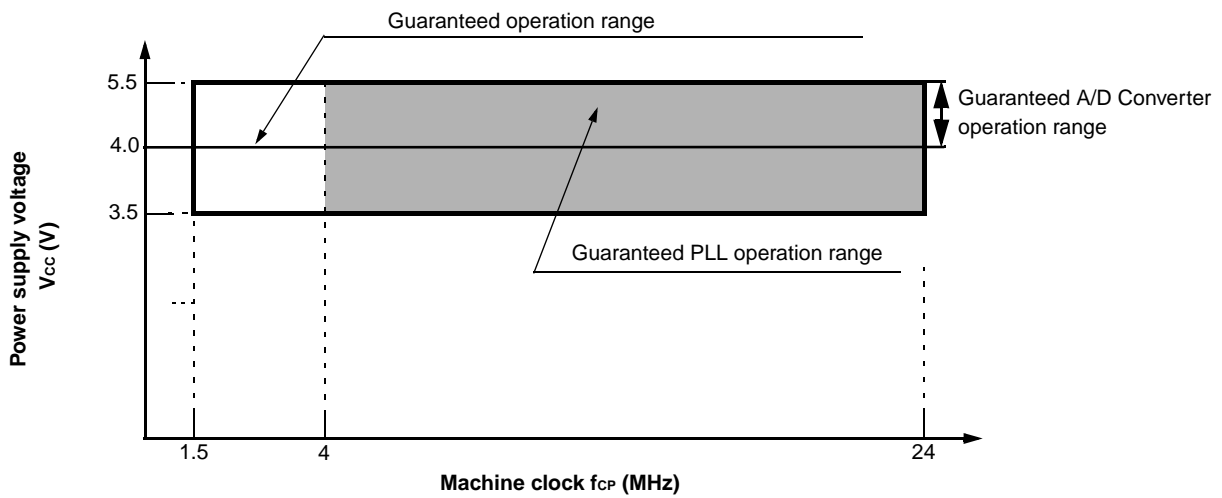
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_c$	X0, X1	3	—	16	MHz	When using an oscillation circuit
		X0, X1	3	—	24	MHz	When using an external clock*
	$f_{CL}$	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	$t_{CYL}$	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	$t_{CYLL}$	X0A, X1A	10	30.5	—	$\mu\text{s}$	
Input clock pulse width	$P_{WH}, P_{WL}$	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	$P_{WHL}, P_{WLL}$	X0A	5	15.2	—	$\mu\text{s}$	
Input clock rise and fall time	$t_{CR}, t_{CF}$	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	$f_{CP}$	—	1.5	—	24	MHz	When using main clock
	$f_{CPL}$	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	$t_{CP}$	—	41.67	—	666	ns	When using main clock
	$t_{CPL}$	—	20	122.1	—	$\mu\text{s}$	When using sub clock

\* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in "Relation among external clock frequency and machine clock frequency".

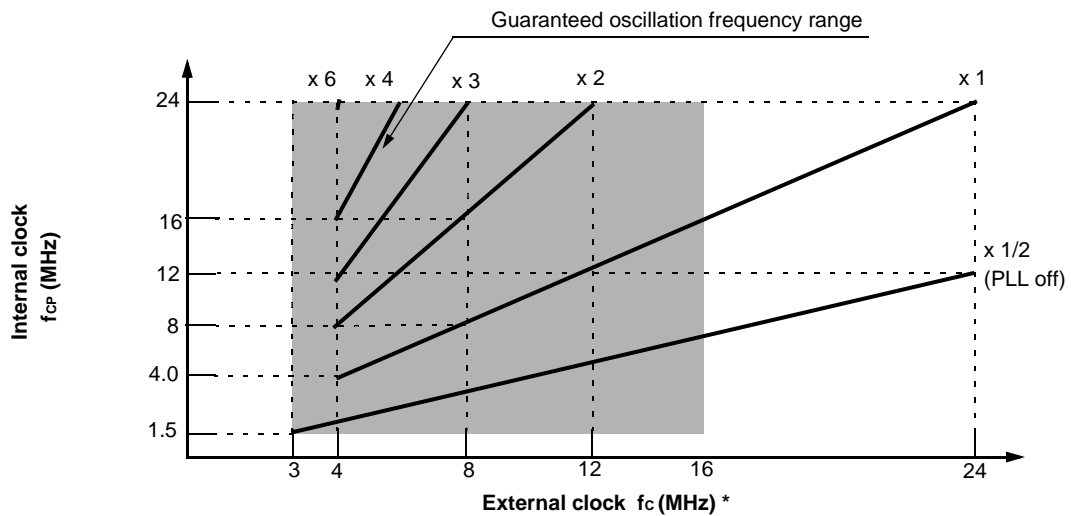


**Clock Timing**

# MB90340 Series



**Guaranteed operation range of MB90340 series**



\* : When using the oscillation circuit, the maximum oscillation clock frequency is 16 MHz

**External clock frequency and Machine clock frequency**



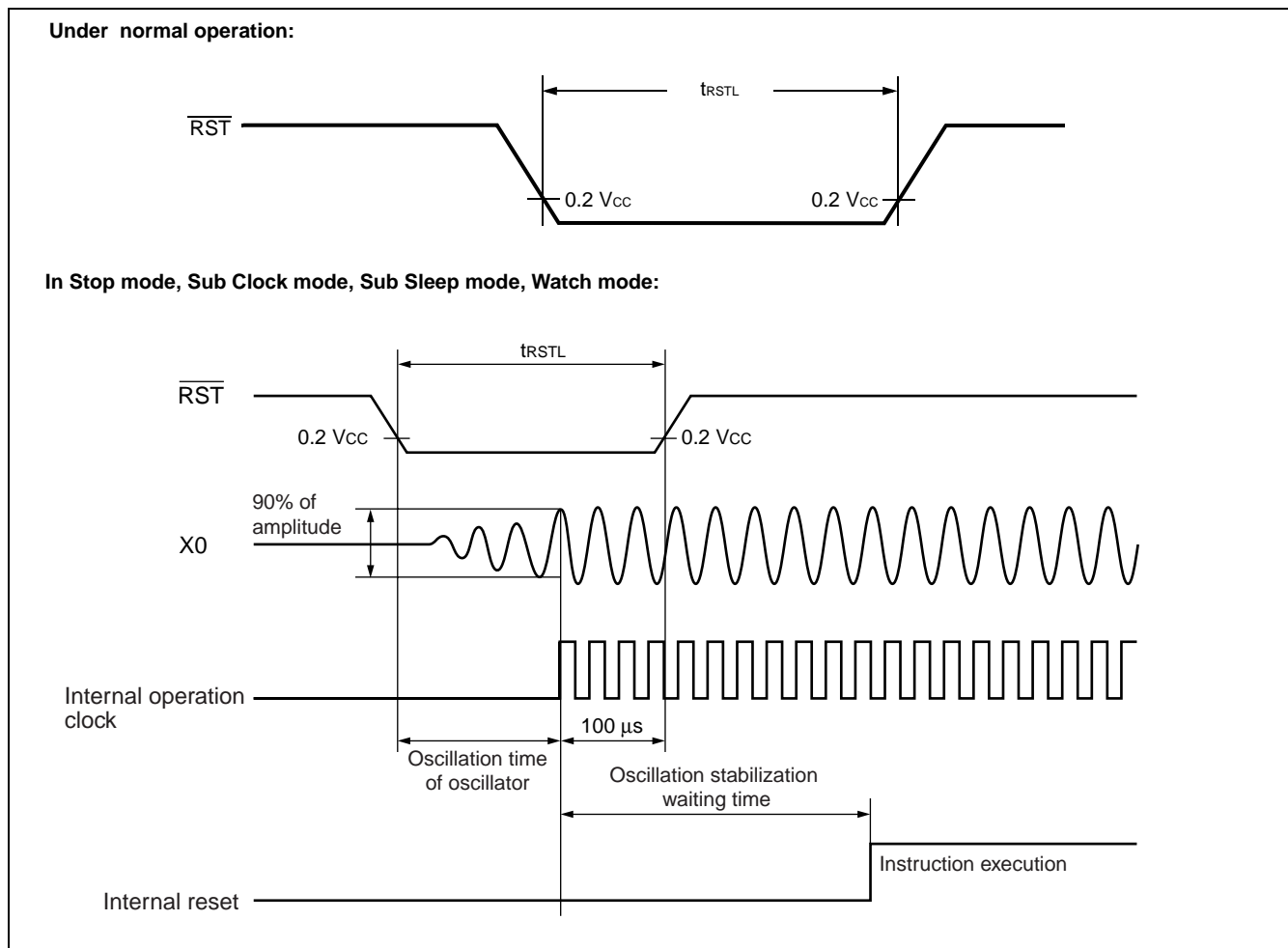
## (2) Reset Standby Input

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Value		Unit	Remarks	
			Min	Max			
Reset input time	$t_{RSTL}$	$\overline{RST}$	500	—	ns	Under normal operation	
			Oscillation time of oscillator* + 100 $\mu\text{s}$		—	ns	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	$\mu\text{s}$	In Time Timer mode	

\* : Oscillation time of oscillator is the time that the amplitude reaches 90%.

In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. With an external clock, the oscillation time is 0 ms.

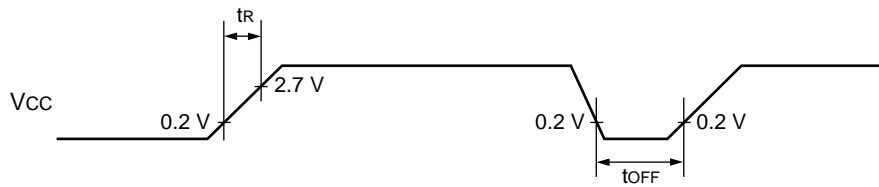


# MB90340 Series

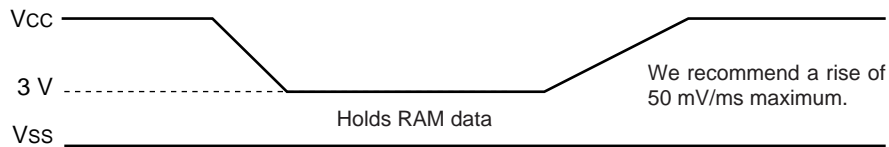
## (3) Power On Reset

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power off time	$t_{OFF}$	$V_{CC}$	—	1	—	ms	Due to repetitive operation



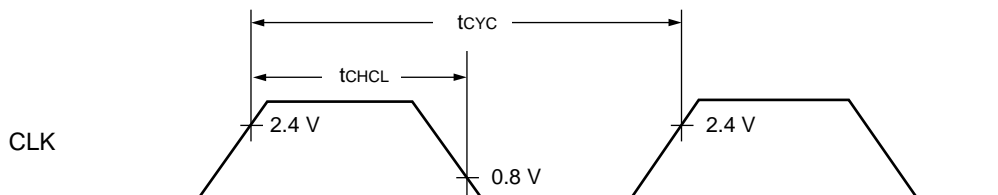
If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



## (4) Clock Output Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

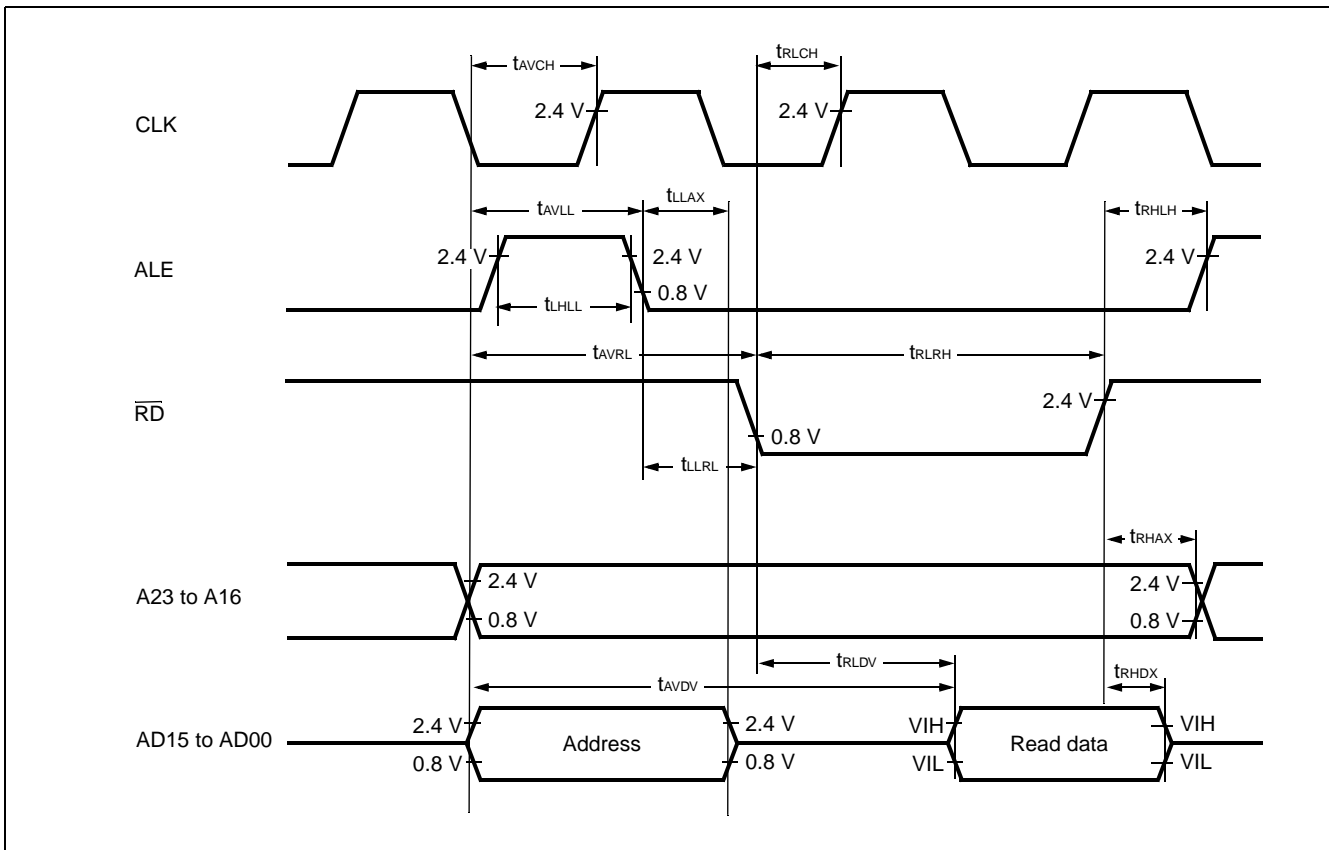
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	$t_{CYC}$	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.76	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK $\downarrow$	$t_{CHCL}$	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$



## (5) Bus Timing (Read)

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ALE pulse width	$t_{LHLL}$	ALE	—	$t_{CP}/2 - 10$	—	ns	
Valid address $\Rightarrow$ ALE $\downarrow$ time	$t_{AVLL}$	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE $\downarrow \Rightarrow$ Address valid time	$t_{LLAX}$	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address $\Rightarrow \overline{RD} \downarrow$ time	$t_{AVRL}$	A23 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address $\Rightarrow$ Valid data input	$t_{AVDV}$	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	$t_{RLRH}$	$\overline{RD}$		$3 t_{CP}/2 - 20$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ Valid data input	$t_{RLDV}$	$\overline{RD}$ , AD15 to AD00		—	$3 t_{CP}/2 - 50$	ns	
$\overline{RD} \uparrow \Rightarrow$ Data hold time	$t_{RHDX}$	$\overline{RD}$ , AD15 to AD00		0	—	ns	
$\overline{RD} \downarrow \Rightarrow$ ALE $\uparrow$ time	$t_{RHLH}$	$\overline{RD}$ , ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD} \uparrow \Rightarrow$ Address valid time	$t_{RHAX}$	$\overline{RD}$ , A23 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address $\Rightarrow$ CLK $\uparrow$ time	$t_{AVCH}$	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ CLK $\uparrow$ time	$t_{RLCH}$	$\overline{RD}$ , CLK		$t_{CP}/2 - 15$	—	ns	
ALE $\downarrow \Rightarrow \overline{RD} \downarrow$ time	$t_{LLRL}$	ALE, $\overline{RD}$	$t_{CP}/2 - 15$	—	ns		

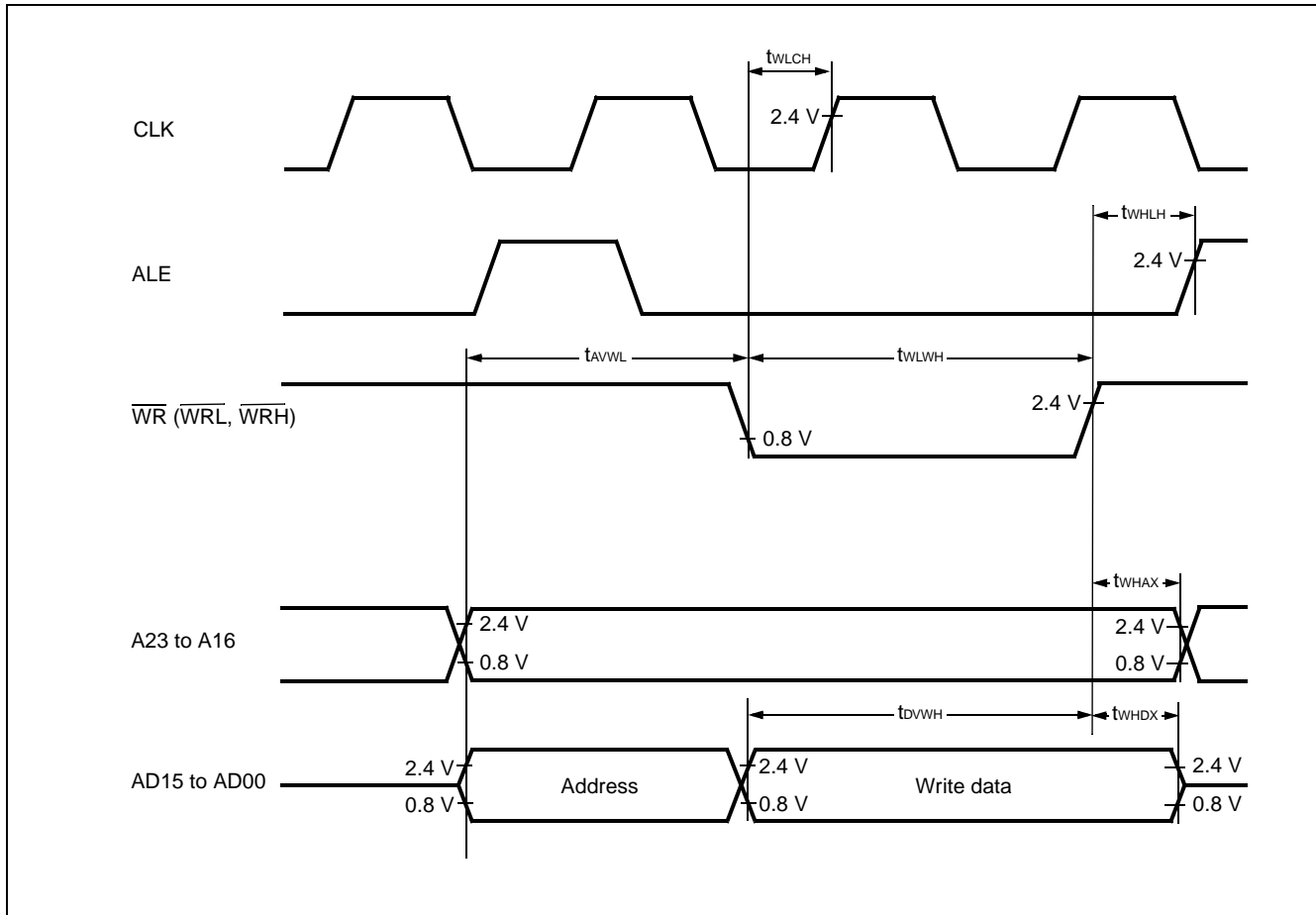


# MB90340 Series

## (6) Bus Timing (Write)

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow \overline{WR} \downarrow$ time	$t_{AVWL}$	A23 to A16, AD15 to AD00, $\overline{WR}$	—	$t_{CP} - 15$	—	ns	
$\overline{WR}$ pulse width	$t_{WLWH}$	$\overline{WR}$		$3 t_{CP} / 2 - 20$	—	ns	
Valid data output $\Rightarrow \overline{WR} \uparrow$ time	$t_{DVWH}$	AD15 to AD00, $\overline{WR}$		$3 t_{CP} / 2 - 20$	—	ns	
$\overline{WR} \uparrow \Rightarrow$ Data hold time	$t_{WHDX}$	AD15 to AD00, $\overline{WR}$		15	—	ns	
$\overline{WR} \uparrow \Rightarrow$ Address valid time	$t_{WHAX}$	A23 to A16, $\overline{WR}$		$t_{CP} / 2 - 10$	—	ns	
$\overline{WR} \uparrow \Rightarrow$ ALE $\uparrow$ time	$t_{WHLH}$	$\overline{WR}$ , ALE		$t_{CP} / 2 - 15$	—	ns	
$\overline{WR} \downarrow \Rightarrow$ CLK $\uparrow$ time	$t_{WLCH}$	$\overline{WR}$ , CLK		$t_{CP} / 2 - 15$	—	ns	

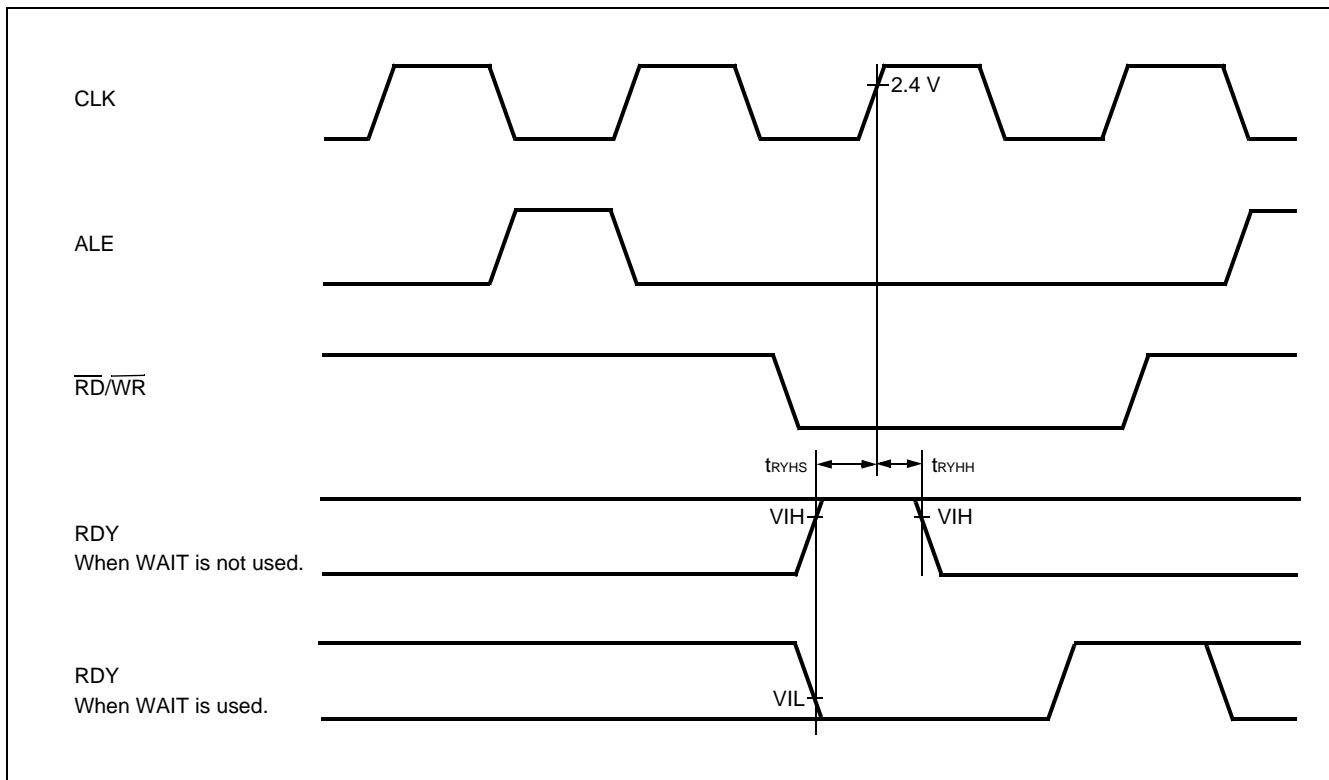


## (7) Ready Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	$t_{RYHS}$	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	$t_{RYHH}$	RDY	—	0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



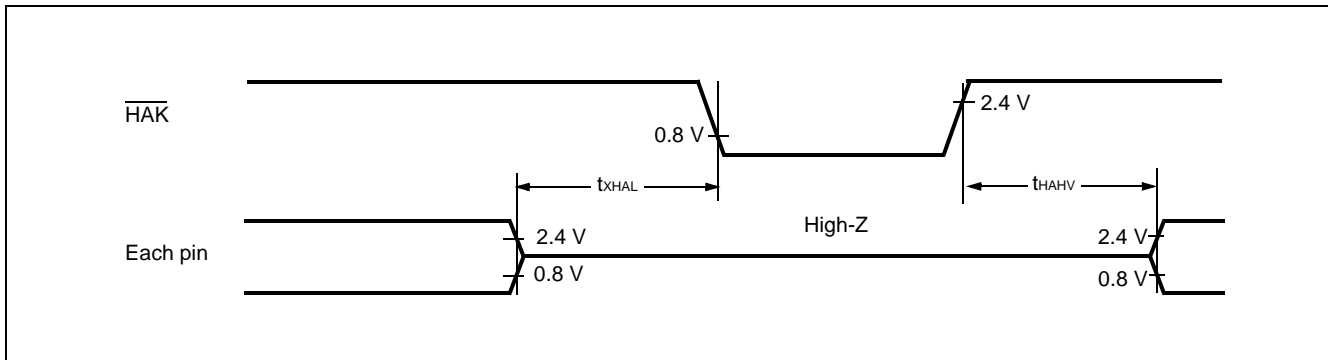
# MB90340 Series

## (8) Hold Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow \overline{\text{HAK}} \downarrow$ time	$t_{XHAL}$	$\overline{\text{HAK}}$	—	30	$t_{CP}$	ns	
$\overline{\text{HAK}} \uparrow$ time $\Rightarrow$ Pin valid time	$t_{HAHV}$	$\overline{\text{HAK}}$		$t_{CP}$	$2 t_{CP}$	ns	

Note : There is more than 1 cycle from when HRQ reads in until the  $\overline{\text{HAK}}$  is changed.

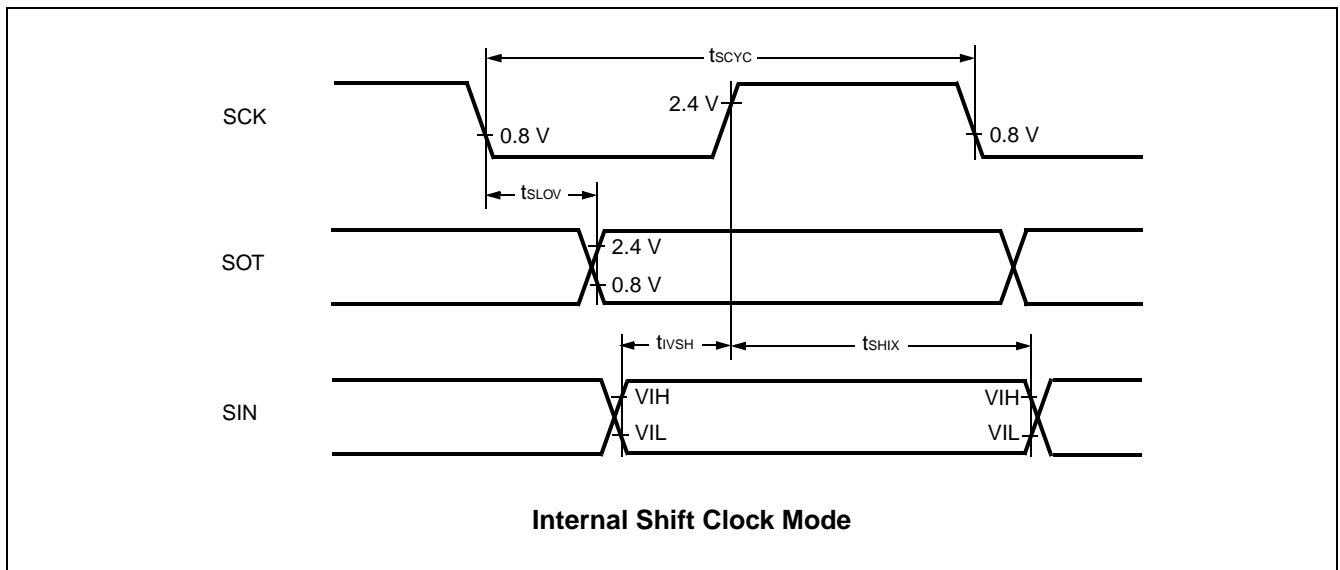


## (9) UART0/1/2/3/4

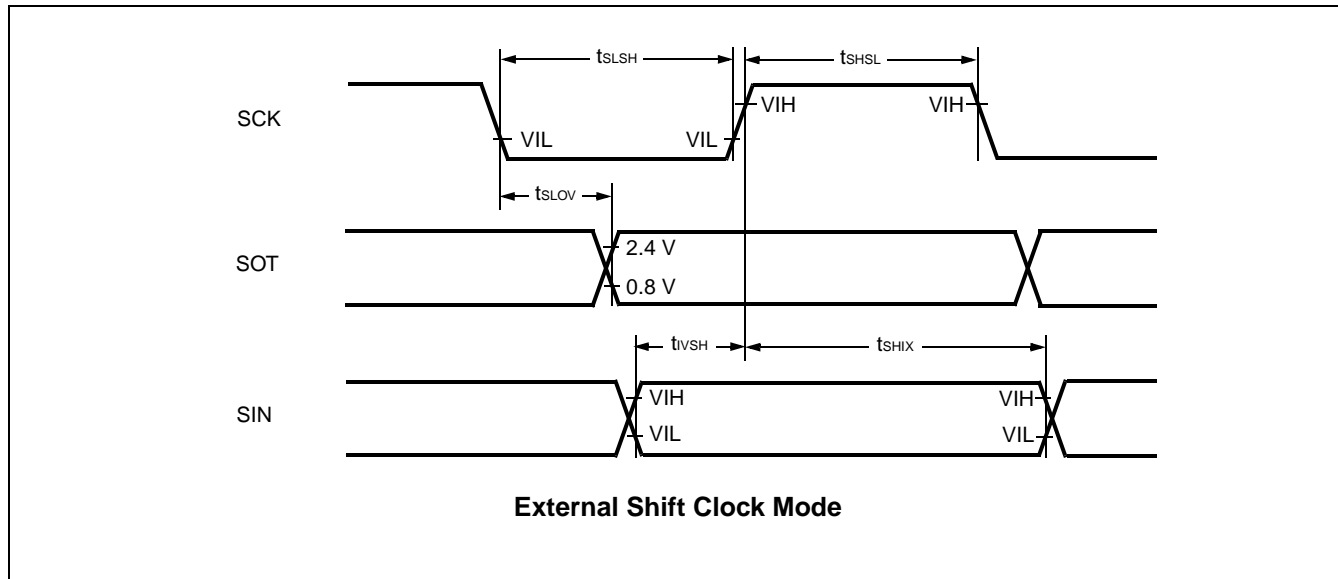
( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK4	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$8 t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0 to SCK4, SOT0 to SOT4		-80	+80	ns	
Valid SIN → SCK ↑	$t_{IVSH}$	SCK0 to SCK4, SIN0 to SIN4		100	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIX}$	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK0 to SCK4	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	SCK0 to SCK4		$4 t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0 to SCK4, SOT0 to SOT4		—	150	ns	
Valid SIN → SCK ↑	$t_{IVSH}$	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIX}$	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	

- Notes :
- AC characteristic in CLK synchronized mode.
  - $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is the machine cycle (Unit : ns)



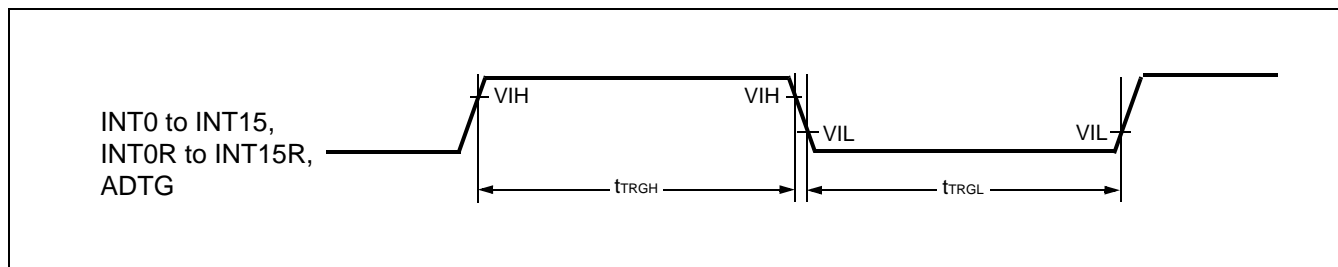
# MB90340 Series



## (10) Trigger Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ $t_{TRGL}$	INT0 to INT15, INT0R to INT15R, ADTG	—	5 $t_{CP}$	—	ns	

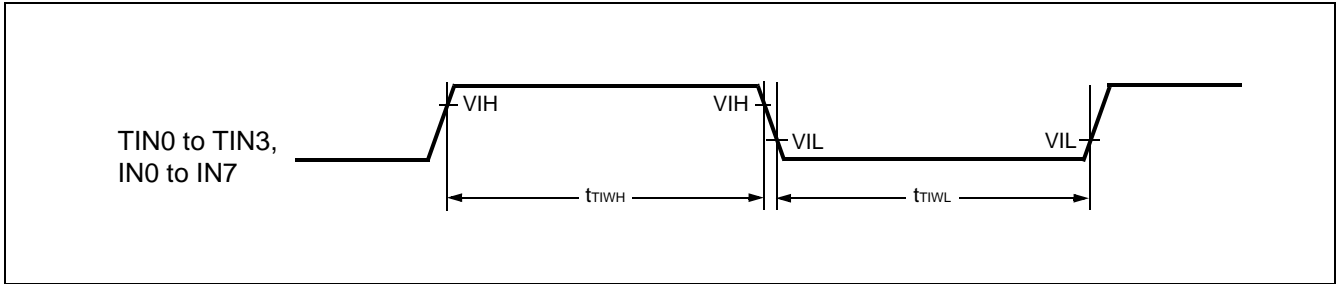




## (11) Timer Related Resource Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

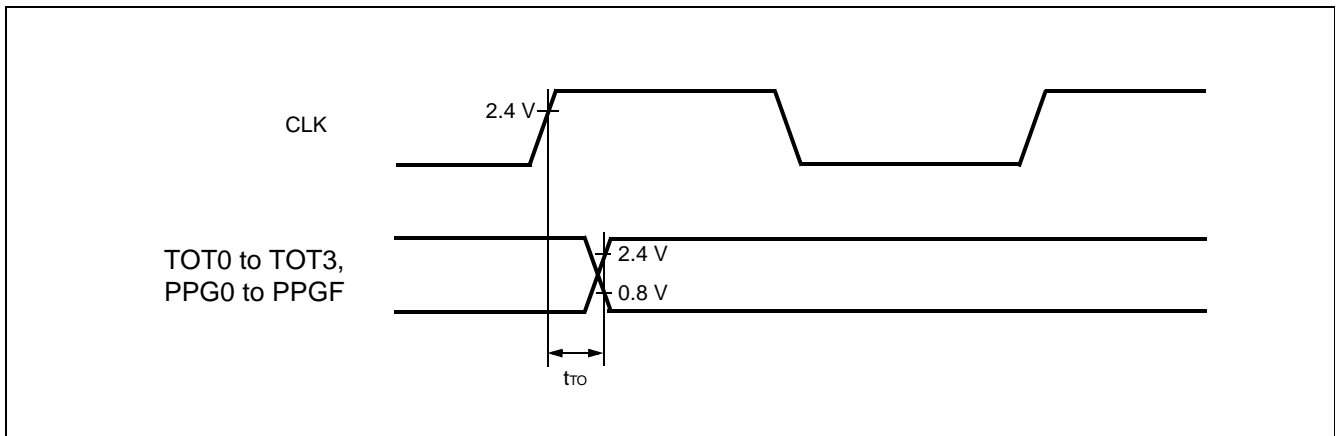
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$	TIN0 to TIN3, IN0 to IN7	—	4 $t_{CP}$	—	ns	
	$t_{TIWL}$						



## (12) Timer Related Resource Output Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
CLK $\uparrow$ $\Rightarrow$ $T_{OUT}$ change time	$t_{ro}$	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns	



# MB90340 Series

## (13) I<sup>2</sup>C Timing

(T<sub>A</sub> = -40°C to +105°C, V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V)

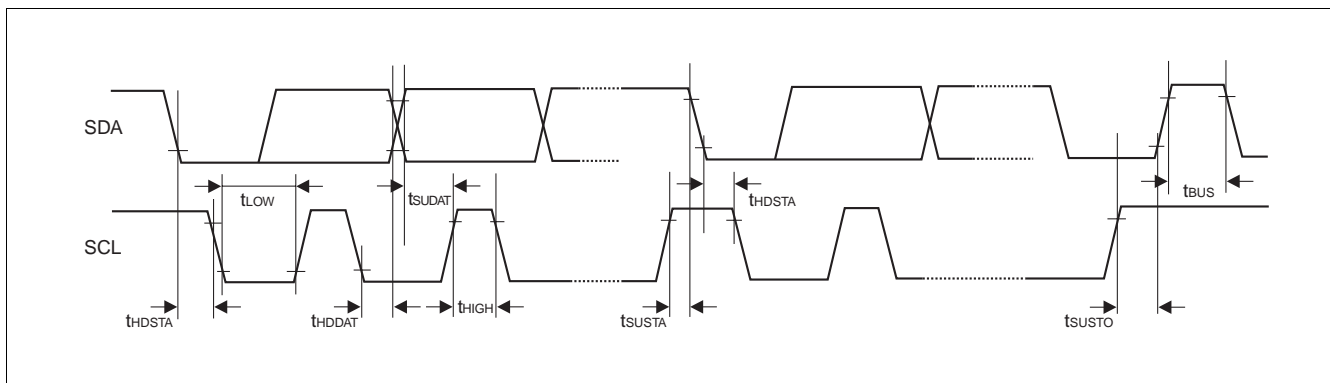
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t <sub>HDSTA</sub>		4.0	—	0.6	—	μs
"L" width of the SCL clock	t <sub>LOW</sub>		4.7	—	1.3	—	μs
"H" width of the SCL clock	t <sub>HIGH</sub>		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL↑→SDA↓	t <sub>SUSTA</sub>		4.7	—	0.6	—	μs
Data hold time SCL↓→SDA↓↑	t <sub>HDDAT</sub>		0	3.45*2	0	0.9*3	μs
Data set-up time SDA↓↑→SCL↑	t <sub>SUDAT</sub>		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t <sub>SUSTO</sub>		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t <sub>BUS</sub>	4.7	—	1.3	—	μs	

\*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : The maximum t<sub>HDDAT</sub> have only to be met if the device does not stretch the "L" width (t<sub>LOW</sub>) of the SCL signal.

\*3 : A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SUDAT</sub> ≥ 250 ns must then be met.

\*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



## 5. A/D Converter

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $3.0\text{ V} \leq AVRH - AVRL$ ,  $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	$\pm 3.0$	LSB	
Nonlinearity error	—	—	—	—	$\pm 2.5$	LSB	
Differential nonlinearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero reading voltage	$V_{OT}$	AN0 to AN23	$AVRL - 1.5$	$AVRL + 0.5$	$AVRL + 2.5$	LSB	
Full scale reading voltage	$V_{FST}$	AN0 to AN23	$AVRH - 3.5$	$AVRH - 1.5$	$AVRH + 0.5$	LSB	
Compare time	—	—	1.0	—	16,500	$\mu\text{s}$	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	$\infty$	$\mu\text{s}$	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Analog port input current	$I_{AIN}$	AN0 to AN23	-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage range	$V_{AIN}$	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$AVRL + 2.7$	—	$AV_{CC}$	V	
	—	AVRL	0	—	$AVRH - 2.7$	V	
Power supply current	$I_A$	$AV_{CC}$	—	3.5	7.5	mA	
	$I_{AH}$	$AV_{CC}$	—	—	5	$\mu\text{A}$	*
Reference voltage current	$I_R$	AVRH	—	600	900	$\mu\text{A}$	
	$I_{RH}$	AVRH	—	—	5	$\mu\text{A}$	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

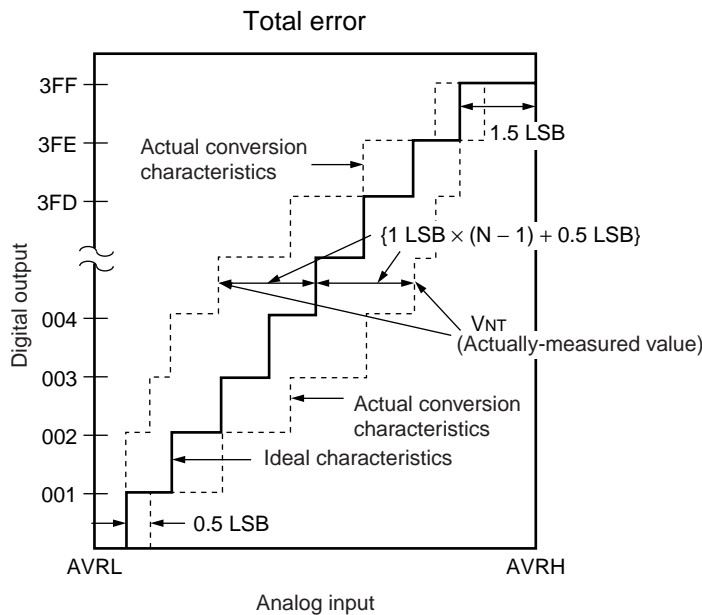
\* : IF A/D convertor is not operating, a current when CPU is stopped is applicable ( $V_{CC} = AV_{CC} = AVRH = 5.0\text{ V}$ ) .

Note : The accuracy gets worse as  $AVRH - AVRL$  becomes smaller.

# MB90340 Series

## 6. Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Non linearity error : Deviation between a line across zero-transition line ( “00 0000 0000” ← → “00 0000 0001” ) and full-scale transition line ( “11 1111 1110” ← → “11 1111 1111” ) and actual conversion characteristics.
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.
- Zero reading voltage : Input voltage which results in the minimum conversion value.
- Full scale reading voltage : Input voltage which results in the maximum conversion value.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

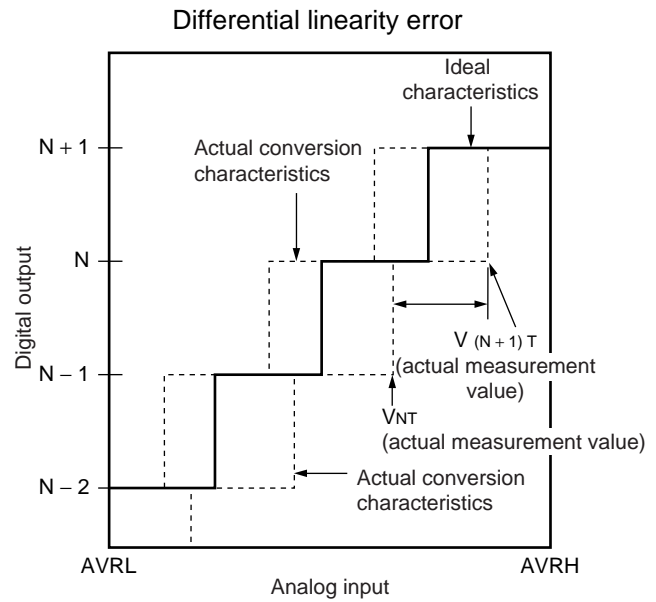
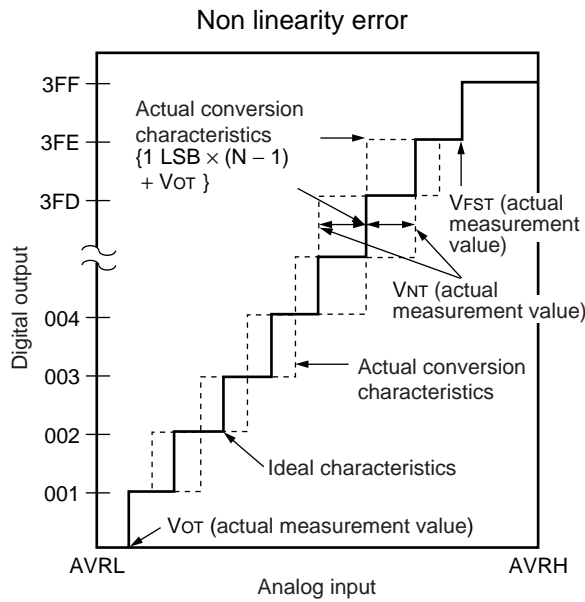
$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB [V]}$$

$V_{NT}$  : A voltage at which digital output transitions from (N - 1) to N.

(Continued)

(Continued)



$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

$V_{OT}$  : Voltage at which digital output transits from "000<sub>H</sub>" to "001<sub>H</sub>."

$V_{FST}$  : Voltage at which digital output transits from "3FE<sub>H</sub>" to "3FF<sub>H</sub>."

# MB90340 Series

## 7. Notes on A/D Converter Section

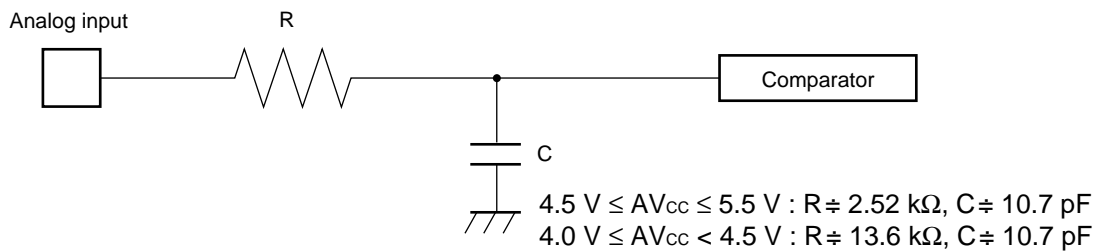
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower ( $4.0\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$ , sampling period  $\leq 0.5\text{ }\mu\text{s}$ )

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



Note : Use the values in the figure only as a guideline.

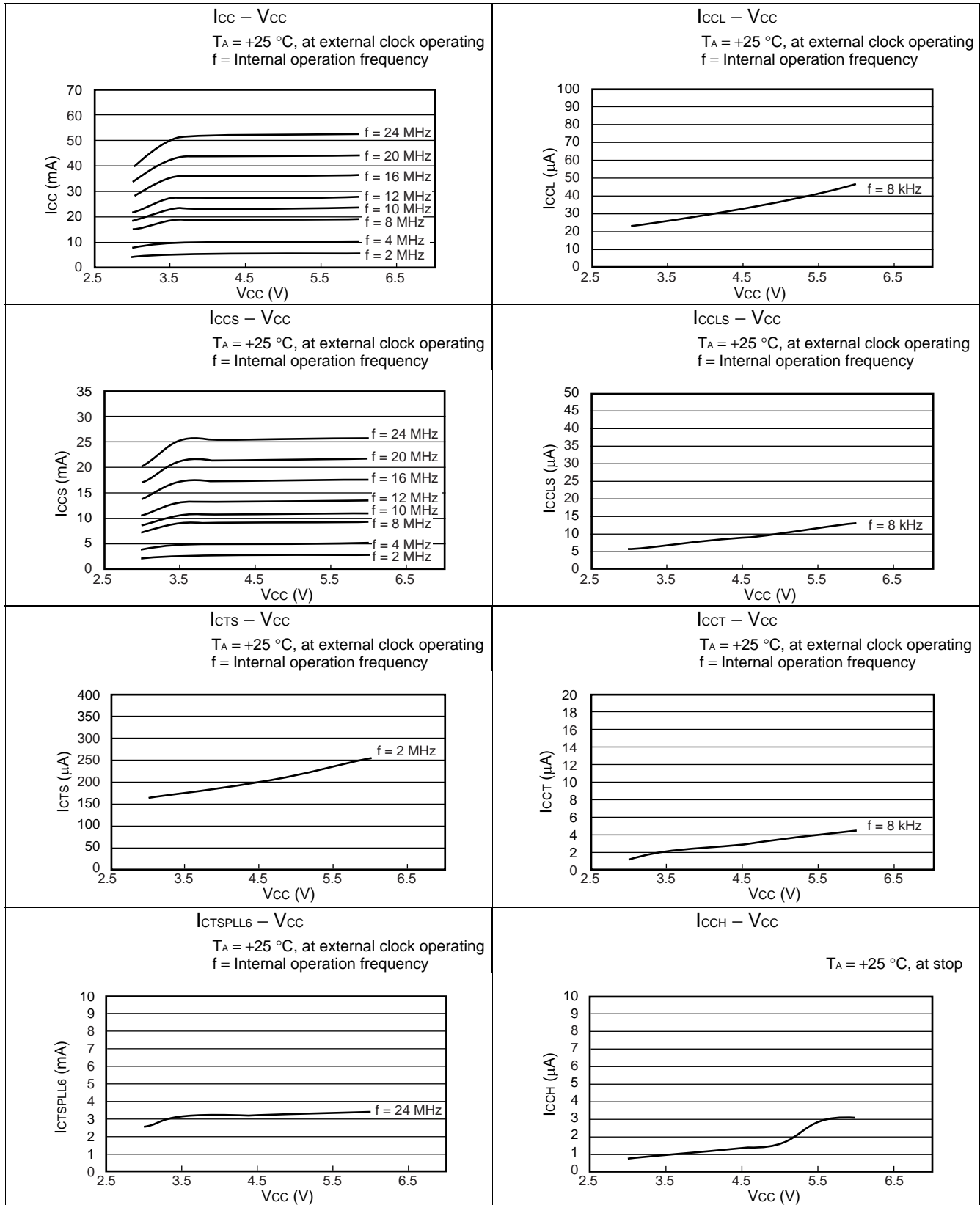
## 8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16 bit width) programming time		—	—	16	3,600	$\mu\text{s}$
Programs/Erase cycle	—	10,000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85\text{ }^\circ\text{C}$	20	—	—	Year	*

\* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at  $+85\text{ }^\circ\text{C}$ ) .

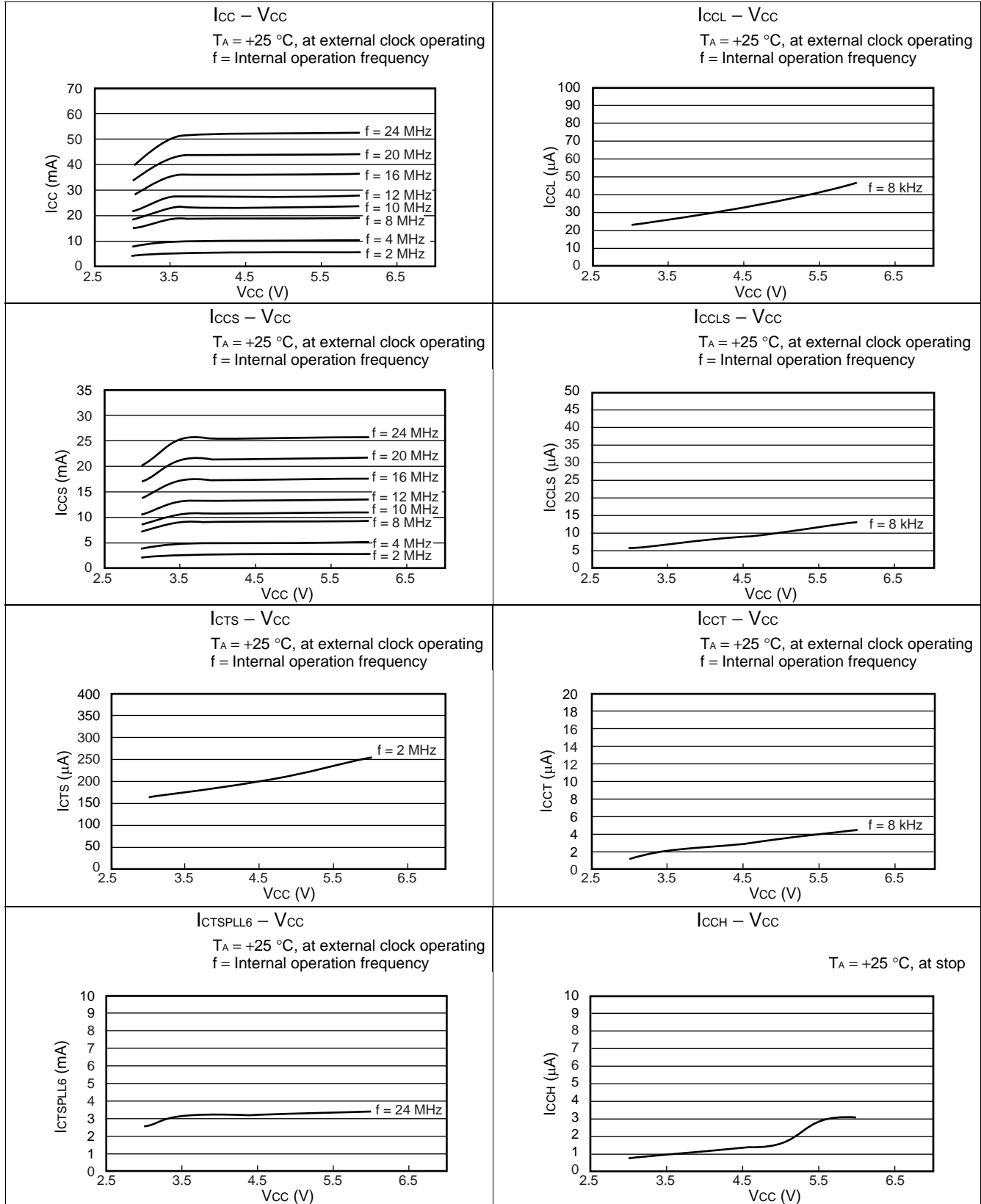
## EXAMPLE CHARACTERISTICS

- MB90F346A, MB90F346AS, MB90F346CA, MB90F346CAS



# MB90340 Series

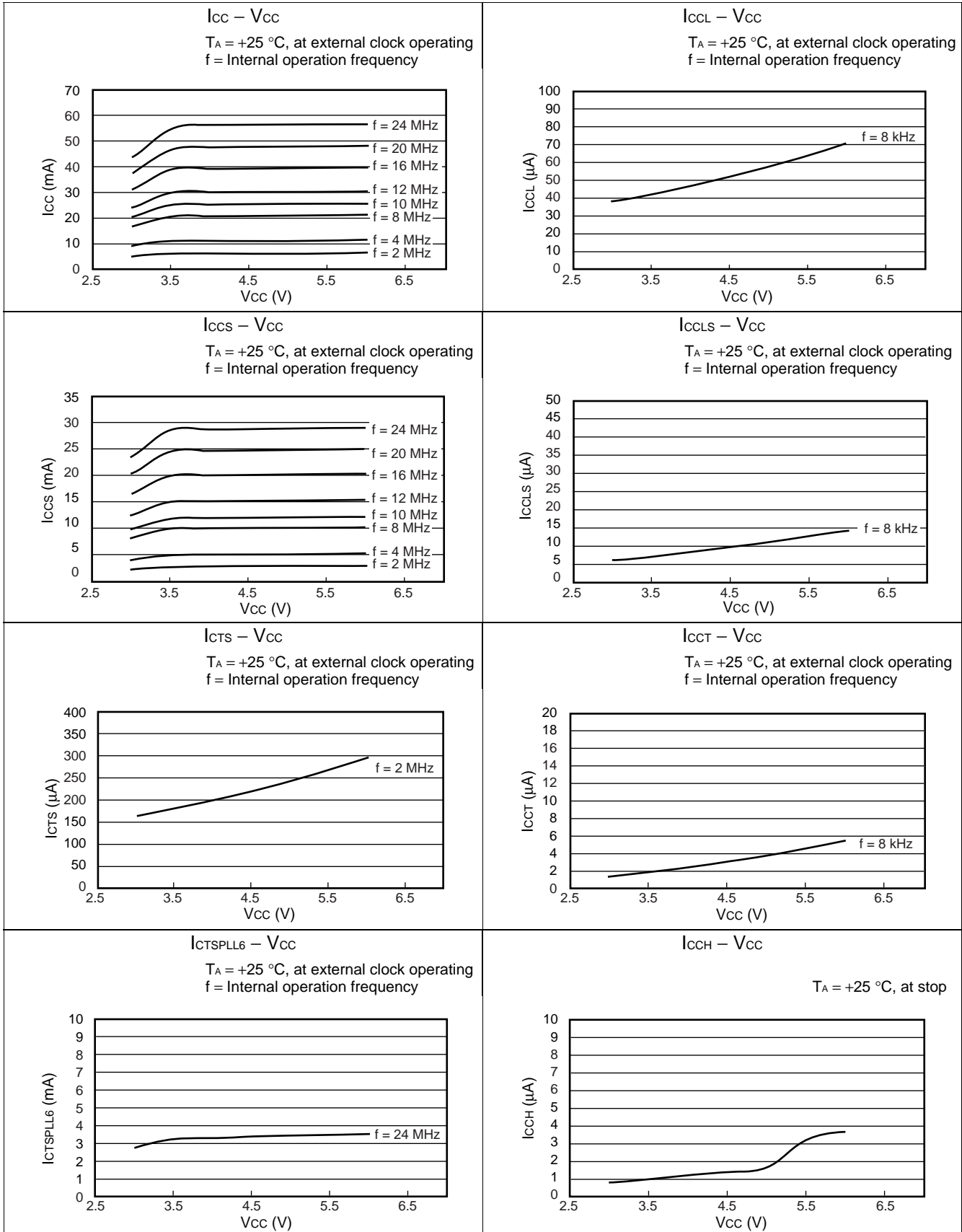
- MB90F347A, MB90F347AS, MB90F347CA, MB90F347CAS





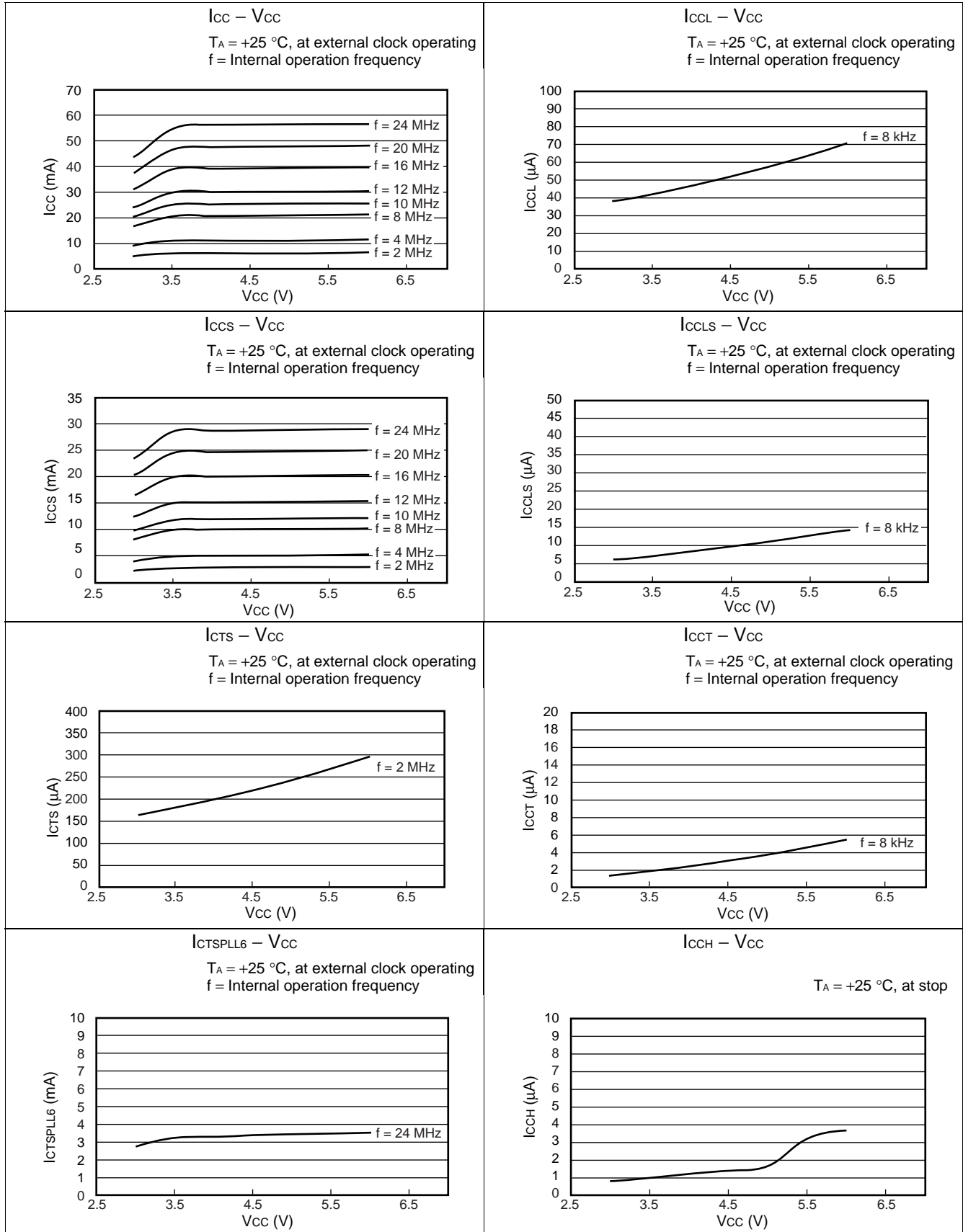
# MB90340 Series

- MB90F349A, MB90F349AS, MB90F349CA, MB90F349CAS



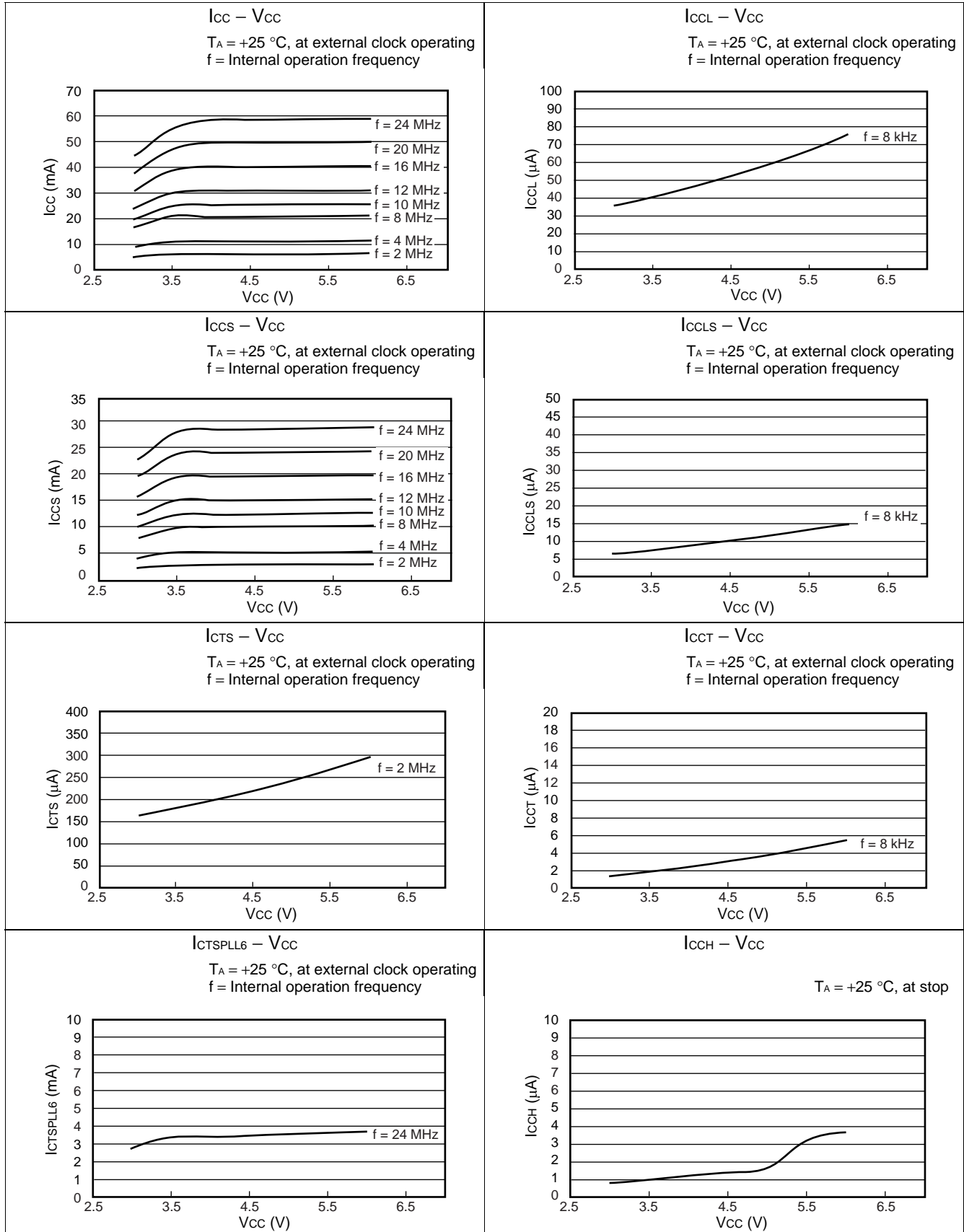
# MB90340 Series

- MB90F342A, MB90F342AS, MB90F342CA, MB90F342CAS



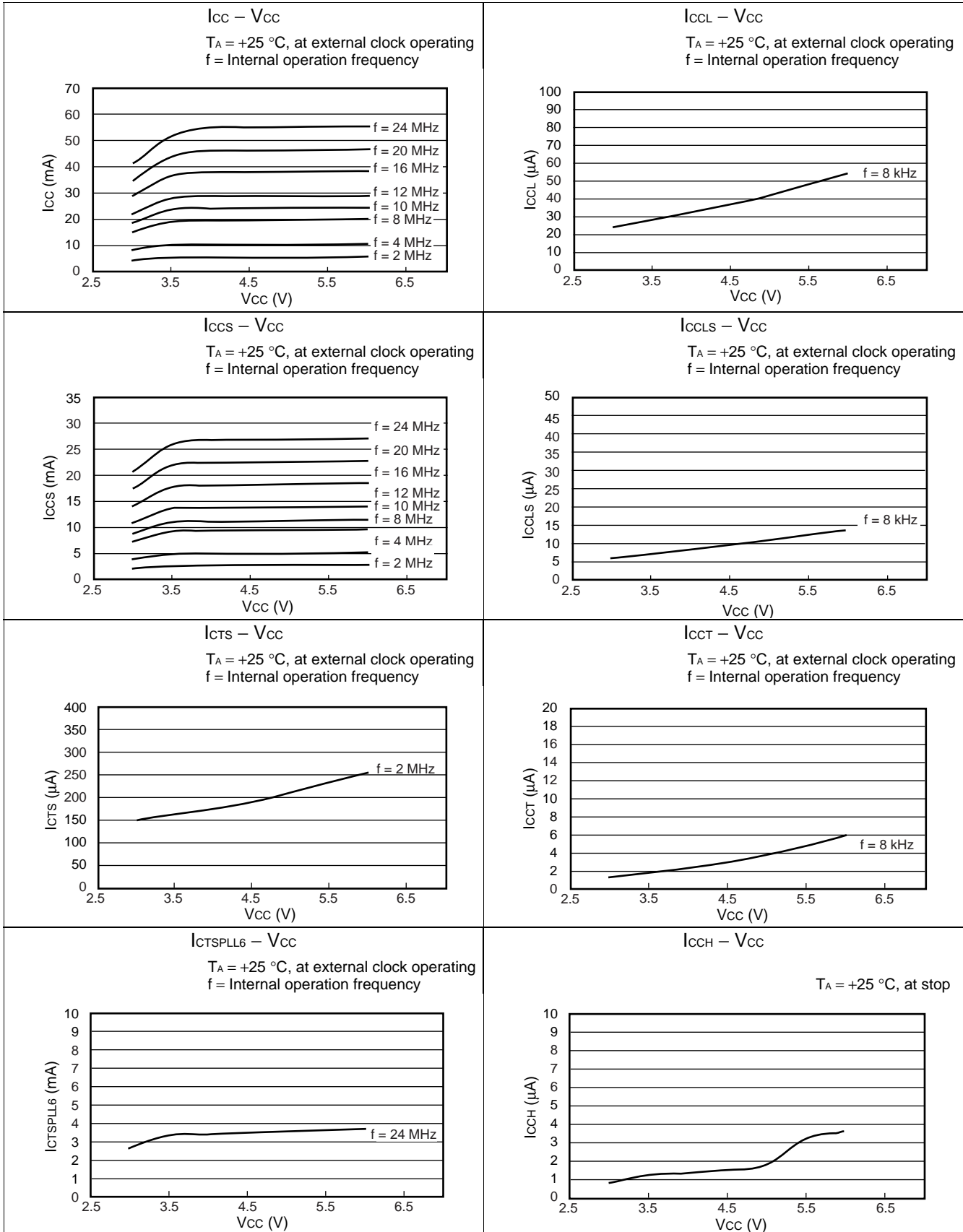
# MB90340 Series

- MB90F345A, MB90F345AS, MB90F345CA, MB90F345CAS



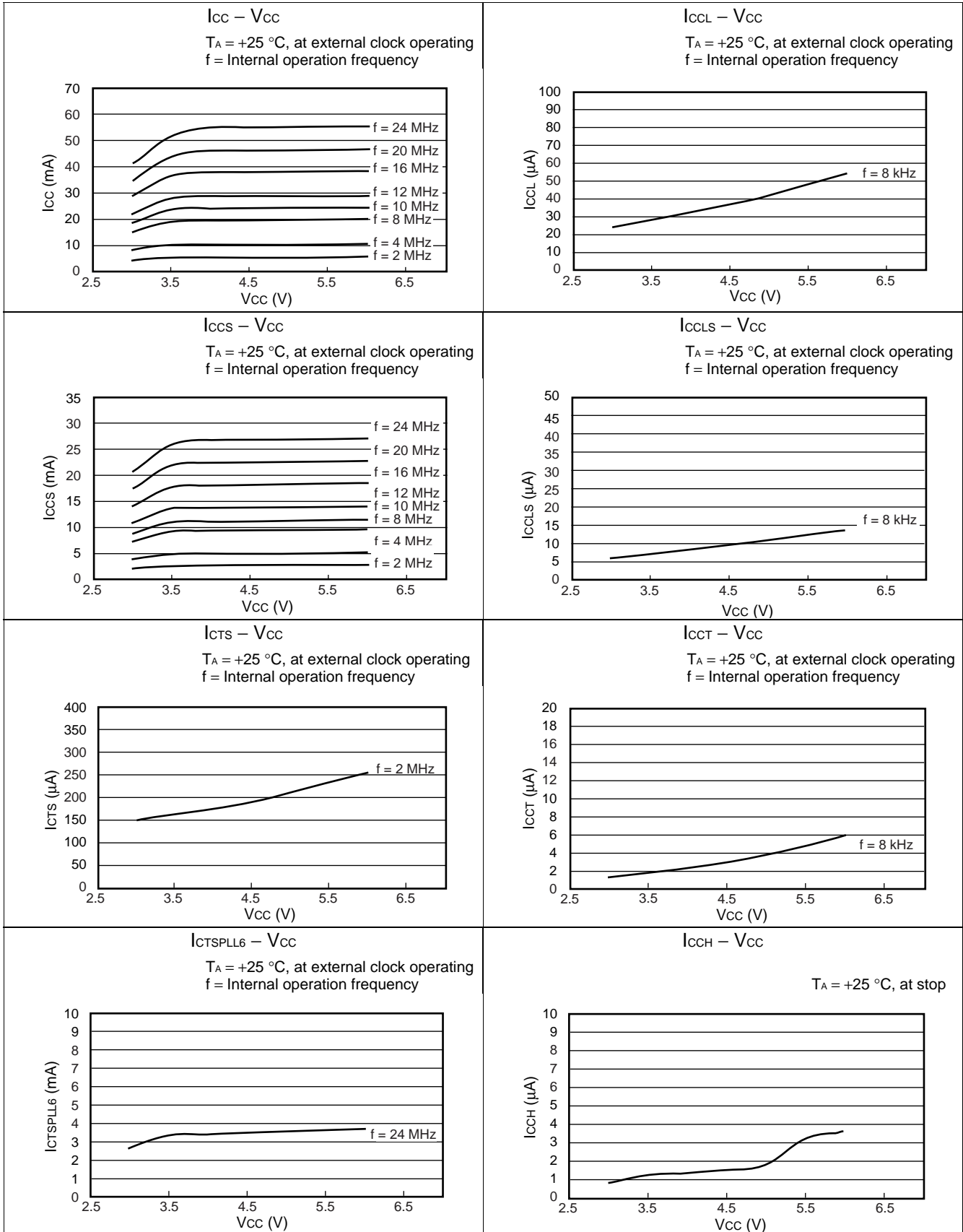
# MB90340 Series

- MB90346A, MB90346AS, MB90346CA, MB90346CAS



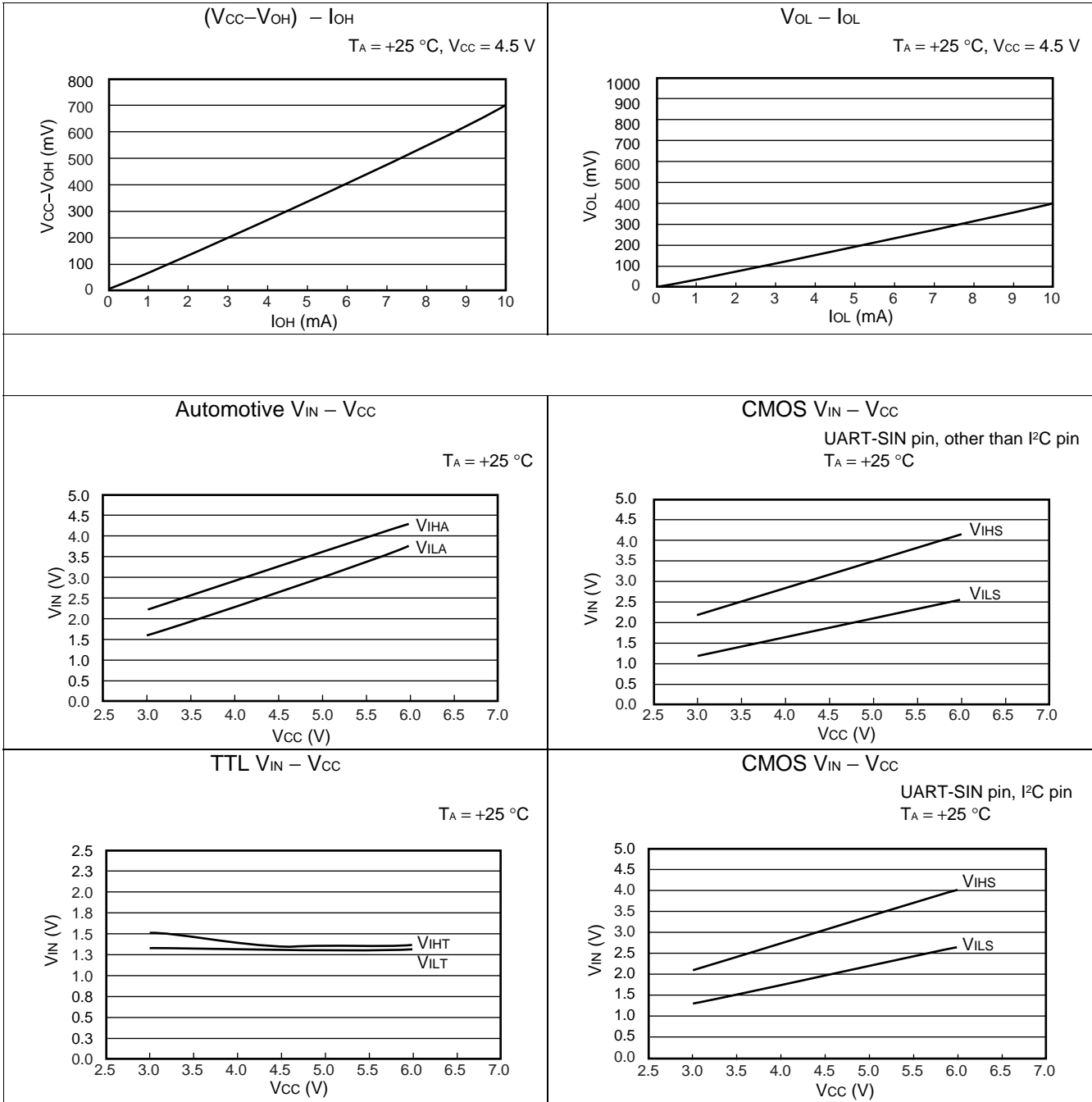
# MB90340 Series

- MB90347A, MB90347AS, MB90347CA, MB90347CAS



# MB90340 Series

• I/O characteristics



# MB90340 Series

## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F342APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F342ASPF		
MB90F342CAPF		
MB90F342CASPF		
MB90F342APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F342ASPFV		
MB90F342CAPFV		
MB90F342CASPFV		
MB90F343APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F343ASPF		
MB90F343CAPF		
MB90F343CASPF		
MB90F343APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F343ASPFV		
MB90F343CAPFV		
MB90F343CASPFV		
MB90F345APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F345ASPF		
MB90F345CAPF		
MB90F345CASPF		
MB90F345APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F345ASPFV		
MB90F345CAPFV		
MB90F345CASPFV		
MB90F346APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F346ASPF		
MB90F346CAPF		
MB90F346CASPF		
MB90F346APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F346ASPFV		
MB90F346CAPFV		
MB90F346CASPFV		

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# MB90340 Series

Part number	Package	Remarks
MB90F347APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F347ASPF		
MB90F347CAPF		
MB90F347CASPF		
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MB90F347ASPFV		
MB90F347CAPFV		
MB90F347CASPFV		
MB90F349APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F349ASPF		
MB90F349CAPF		
MB90F349CASPF		
MB90F349APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F349ASPFV		
MB90F349CAPFV		
MB90F349CASPFV		
MB90341APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90341ASPF		
MB90341CAPF		
MB90341CASPF		
MB90341APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90341ASPFV		
MB90341CAPFV		
MB90341CASPFV		
MB90342APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90342ASPF		
MB90342CAPF		
MB90342CASPF		
MB90342APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90342ASPFV		
MB90342CAPFV		
MB90342CASPFV		

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# MB90340 Series

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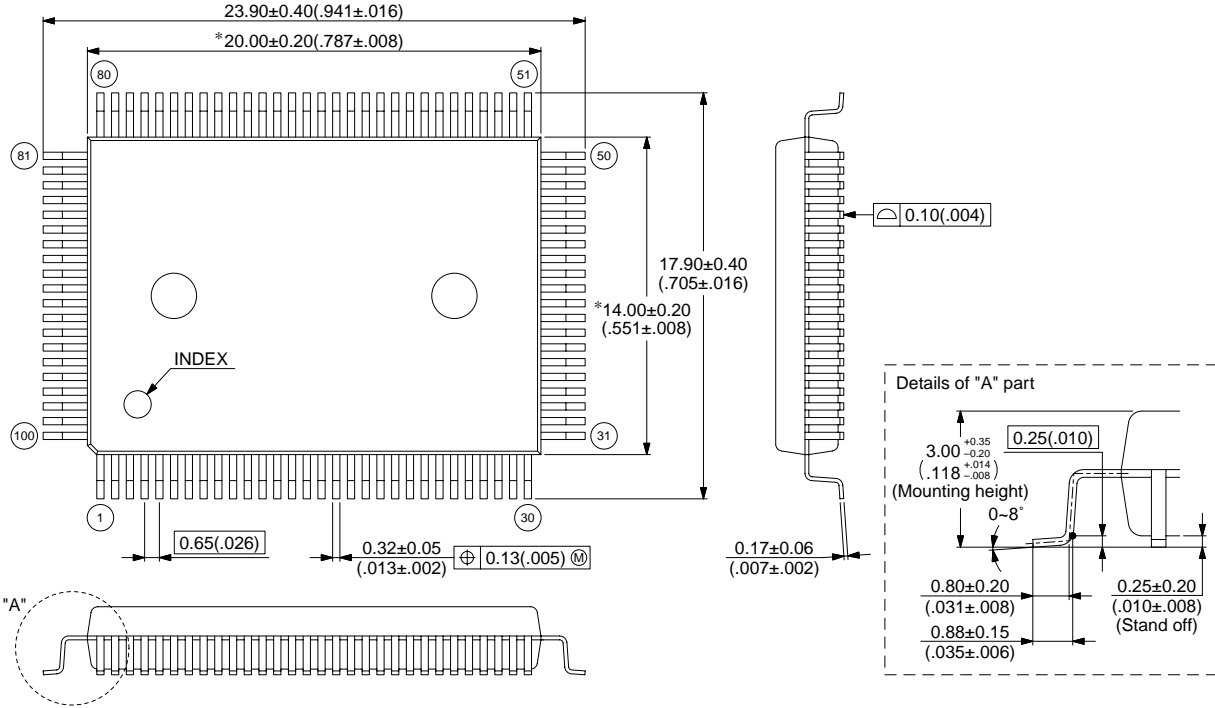
Part number	Package	Remarks
MB90346APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90346ASPF		
MB90346CAPF		
MB90346CASPF		
MB90346APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90346ASPFV		
MB90346CAPFV		
MB90346CASPFV		
MB90347APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90347ASPF		
MB90347CAPF		
MB90347CASPF		
MB90347APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90347ASPFV		
MB90347CAPFV		
MB90347CASPFV		
MB90348APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90348ASPF		
MB90348CAPF		
MB90348CASPF		
MB90348APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90348ASPFV		
MB90348CAPFV		
MB90348CASPFV		
MB90349APF	100-pin Plastic QFP (FPT-100P-M06)	
MB90349ASPF		
MB90349CAPF		
MB90349CASPF		
MB90349APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90349ASPFV		
MB90349CAPFV		
MB90349CASPFV		
MB90V340A-101	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340A-102		

# MB90340 Series

## ■ PACKAGE DIMENSIONS

100-pin Plastic QFP  
(FPT-100P-M06)

Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness including plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

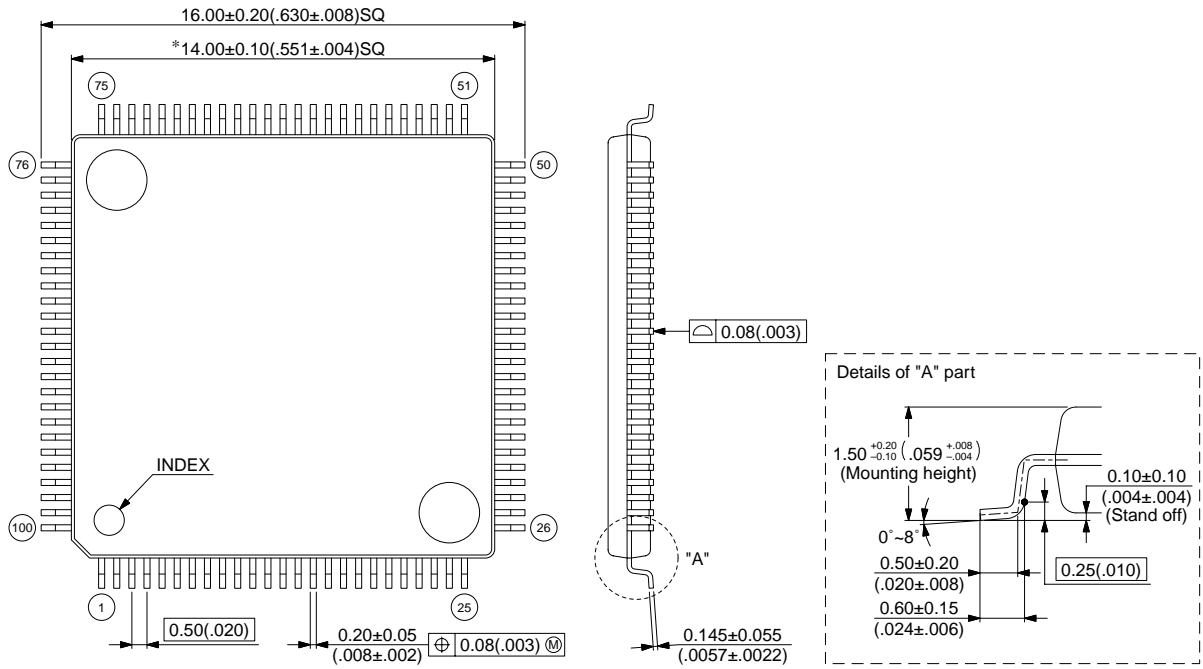
(Continued)

# MB90340 Series

(Continued)

100-pin Plastic LQFP  
(FPT-100P-M05)

Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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