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F²MC-16LX MB90595G Series CMOS 16-bit Proprietary Microcontroller

The MB90595G series with FULL-CAN interface and FLASH ROM is especially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The instruction set of F²MC-16LX CPU core inherits an AT architecture of the F²MC* family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90595G series has peripheral resources of 8/10-bit A/D converters, UART (SCI), extended I/O serial interface, 8/16-bit PPG timer, I/O timer (input capture (ICU), output compare (OCU)) and stepping motor controller.

Features

- Clock
 - Embedded PLL clock multiplication circuit
 - Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).
 - Minimum instruction execution time: 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V_{CC} of 5.0 V)
- Instruction set to optimize controller applications
 - Rich data types (bit, byte, word, long word)
 - Rich addressing mode (23 types)
 - Enhanced signed multiplication/division instruction and RETI instruction functions
 - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
 - Adoption of system stack pointer
 - Enhanced pointer indirect instructions
 - Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4-byte instruction queue
- Enhanced interrupt function: 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
 - Extended intelligent I/O service function (EI²OS): Up to 10 channels
- Embedded ROM size and types
 - Mask ROM: 128 Kbytes
 - Flash ROM: 128 Kbytes
 - Embedded RAM size: 4 Kbytes (MB90595G: 6 Kbytes)
- Flash ROM
 - Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands
 - A flag indicating completion of the algorithm
 - Hard-wired reset vector available in order to point to a fixed boot sector
 - Erase can be performed on each block
 - Block protection with external programming voltage
- Low-power consumption (stand-by) mode
 - Sleep mode (mode in which CPU operating clock is stopped)
 - Stop mode (mode in which oscillation is stopped)
- CPU intermittent operation mode
- Hardware stand-by mode
- Process: 0.5 μm CMOS technology
- I/O port
 - General-purpose I/O ports: 78 ports
 - Push-pull output and Schmitt trigger input.
 - Programmable on each bit as I/O or signal for peripherals.
- Timer
 - Watchdog timer: 1 channel
 - 8/16-bit PPG timer: 8/16-bit × 6 channels
 - 16-bit re-load timer: 2 channels
- 16-bit I/O timer
 - 16-bit Free-run timer: 1 channel
 - Input capture: 4 channels
 - Output compare: 4 channels
- Extended I/O serial interface: 1 channel
- UART0
 - With full-duplex double buffer (8-bit length)
 - Clock asynchronous or clock synchronized (with start/stop bit) transmission can be selectively used.
- UART1 (SCI)
 - With full-duplex double buffer (8-bit length)
 - Clock asynchronous or clock synchronized serial transmission (I/O extended transmission) can be selectively used.
- Stepping motor controller (4 channels)
- External interrupt circuit (8 channels)
 - A module for starting an extended intelligent I/O service (EI²OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module: Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
 - 8/10-bit resolution can be selectively used.
 - Starting by an external trigger input.
- FULL-CAN interface: 1 channel
 - Conforming to Version 2.0 Part A and Part B
 - Flexible message buffering (mailbox and FIFO buffering can be mixed)
- 18-bit Time-base counter
- External bus interface: Maximum address space 16 Mbytes

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1. Product Lineup

Features		MB90598G	MB90F598G	MB90V595G
Classification		Mask ROM product	Flash ROM product	Evaluation product
ROM size		128 Kbytes	128 Kbytes Boot block Hard-wired reset vector	None
RAM size		4 Kbytes	4 Kbytes	6 Kbytes
Emulator-specific power supply *1		—		None
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 μ s (at machine clock frequency of 16 MHz, minimum value)		
UART0		Clock synchronized transmission (500 K/1 M/2 Mbps) Clock asynchronous transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
UART1(SCI)		Clock synchronized transmission (62.5 K/125 K/250 K/500 K/1 Mbps) Clock asynchronous transmission (1202/2404/4808/9615/31250 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers (6 channels)		Number of channels: 6 (8/16-bit \times 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ (f_{sys} = system clock frequency) 128 μ s (f_{osc} = 4MHz: oscillation clock frequency)		
16-bit Reload timer		Number of channels: 2 Operation clock frequency: $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)		

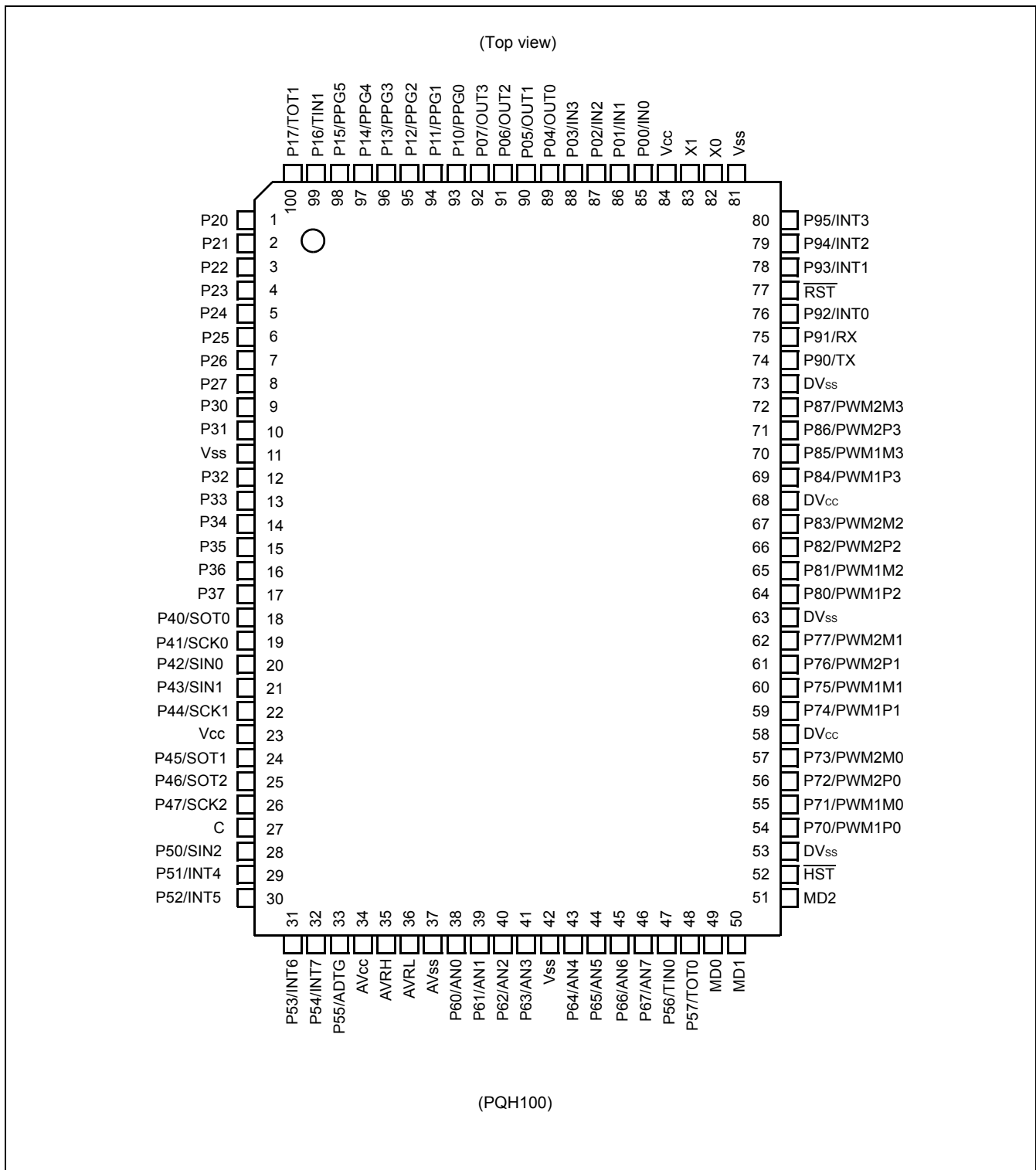
Features	MB90598G	MB90F598G	MB90V595G
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90598G/F598G:TSEG2 ≥ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics, Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*2	+5 V±10 %		
Package	QFP-100		PGA-256

*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.

Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2: Varies with conditions such as the operating frequency. (See "Electrical Characteristics.")

2. Pin Assignment



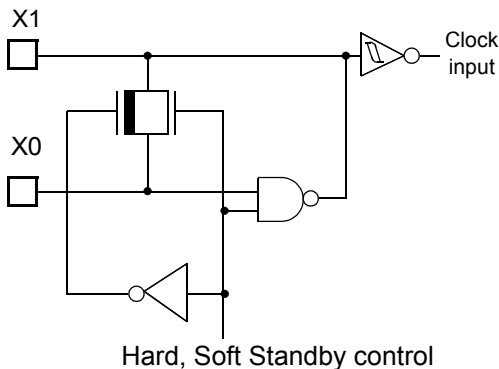
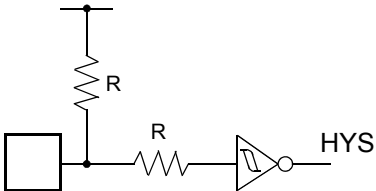
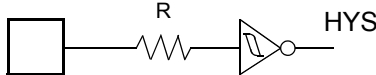
3. Pin Description

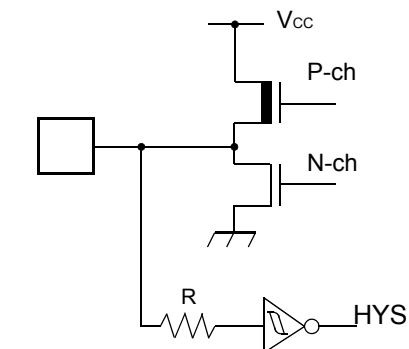
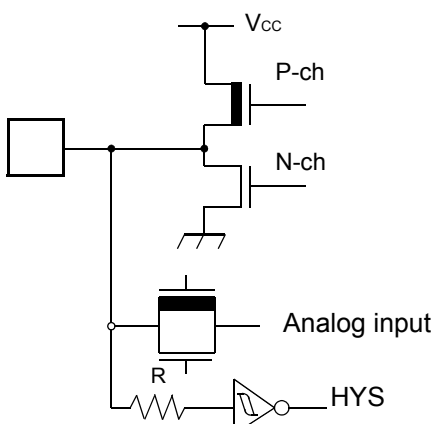
Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{\text{RST}}$	B	Reset input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

Pin no.	Pin name	Circuit type	Function
28	P50	D	General purpose IO
	SIN2		SIN Input for the Serial IO
29 to 32	P51 to P54	D	General purpose IO
	INT4 to INT7		External interrupt input for INT4 to INT7
33	P55	D	General purpose IO
	ADTG		Input for the external trigger of the A/D Converter
38 to 41	P60 to P63	E	General purpose IO
	AN0 to AN3		Inputs for the A/D Converter
43 to 46	P64 to P67	E	General purpose IO
	AN4 to AN7		Inputs for the A/D Converter
47	P56	D	General purpose IO
	TIN0		TIN input for the 16-bit Reload Timer 0
48	P57	D	General purpose IO
	TOT0		TOT output for the 16-bit Reload Timer 0
54 to 57	P70 to P73	F	General purpose IO
	PWM1P0 PWM1M0 PWM2P0 PWM2M0		Output for Stepper Motor Controller channel 0
59 to 62	P74 to P77	F	General purpose IO
	PWM1P1 PWM1M1 PWM2P1 PWM2M1		Output for Stepper Motor Controller channel 1
64 to 67	P80 to P83	F	General purpose IO
	PWM1P2 PWM1M2 PWM2P2 PWM2M2		Output for Stepper Motor Controller channel 2
69 to 72	P84 to P87	F	General purpose IO
	PWM1P3 PWM1M3 PWM2P3 PWM2M3		Output for Stepper Motor Controller channel 3
74	P90	D	General purpose IO
	TX		TX output for CAN Interface
75	P91	D	General purpose IO
	RX		RX input for CAN Interface

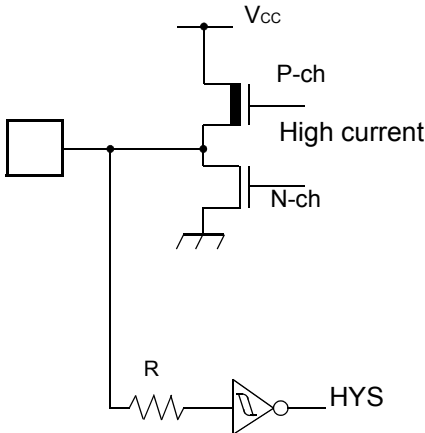
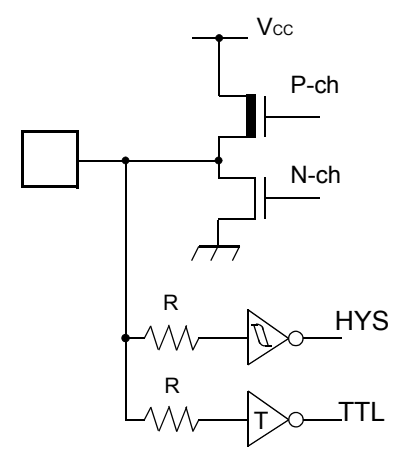
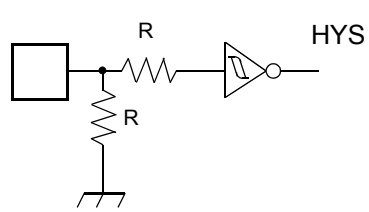
Pin no.	Pin name	Circuit type	Function
76	P92	D	General purpose IO
	INT0		External interrupt input for INT0
78 to 80	P93 to P95	D	General purpose IO
	INT1 to INT3		External interrupt input for INT1 to INT3
58, 68	DV _{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV _{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV _{CC}	Power supply	Dedicated power supply pin for the A/D Converter
37	AV _{SS}	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter
49, 50	MD0 MD1	C	Operating mode selection input pins. These pins should be connected to V _{CC} or V _{SS} .
51	MD2	H	Operating mode selection input pin. This pin should be connected to V _{CC} or V _{SS} .
27	C	—	External capacitor pin. A capacitor of 0.1μF should be connected to this pin and V _{SS} .
23, 84	V _{CC}	Power supply	Power supply pins (5.0 V).
11, 42, 81	V _{SS}	Power supply	Ground pins (0.0 V).

4. I/O Circuit Type

Circuit Type	Circuit	Remarks
A	 <p>Hard, Soft Standby control</p>	<ul style="list-style-type: none"> ■ Oscillation feedback resistor: 1 MΩ approx.
B		<ul style="list-style-type: none"> ■ Hysteresis input with pull-up Resistor: 50 kΩ approx.
C		<ul style="list-style-type: none"> ■ Hysteresis input

Circuit Type	Circuit	Remarks
D		<ul style="list-style-type: none"> ■ CMOS output ■ CMOS Hysteresis input
E		<ul style="list-style-type: none"> ■ CMOS output ■ CMOS Hysteresis input ■ Analog input

(Continued)

Circuit Type	Circuit	Remarks
F		<ul style="list-style-type: none"> ■ CMOS high current output ■ CMOS Hysteresis input
G		<ul style="list-style-type: none"> ■ CMOS output ■ CMOS Hysteresis input ■ TTL input (MB90F598G, only in Flash mode)
H		<ul style="list-style-type: none"> ■ Hysteresis input Pull-down Resistor: 50 kΩ approx. (except MB90F598G)

5. Handling Devices

(1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when a voltage exceeding V_{CC} or a voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS} .

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC} , $AVRH$, DV_{CC}) and analog input voltages not exceed the digital voltage (V_{CC}).

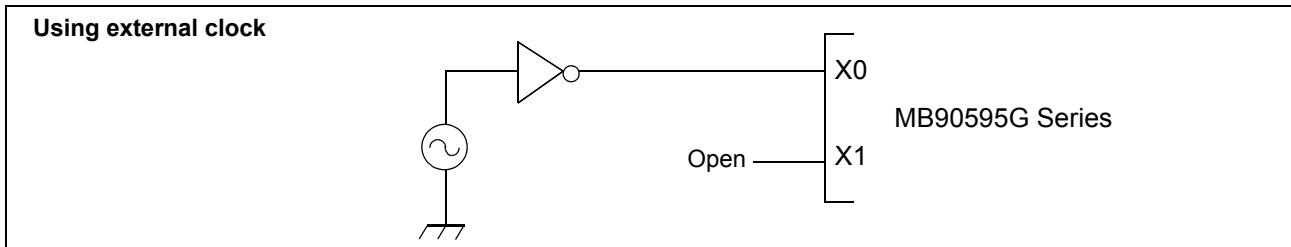
(2) Treatment of Unused Pins

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 k Ω resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

(3) Using external clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

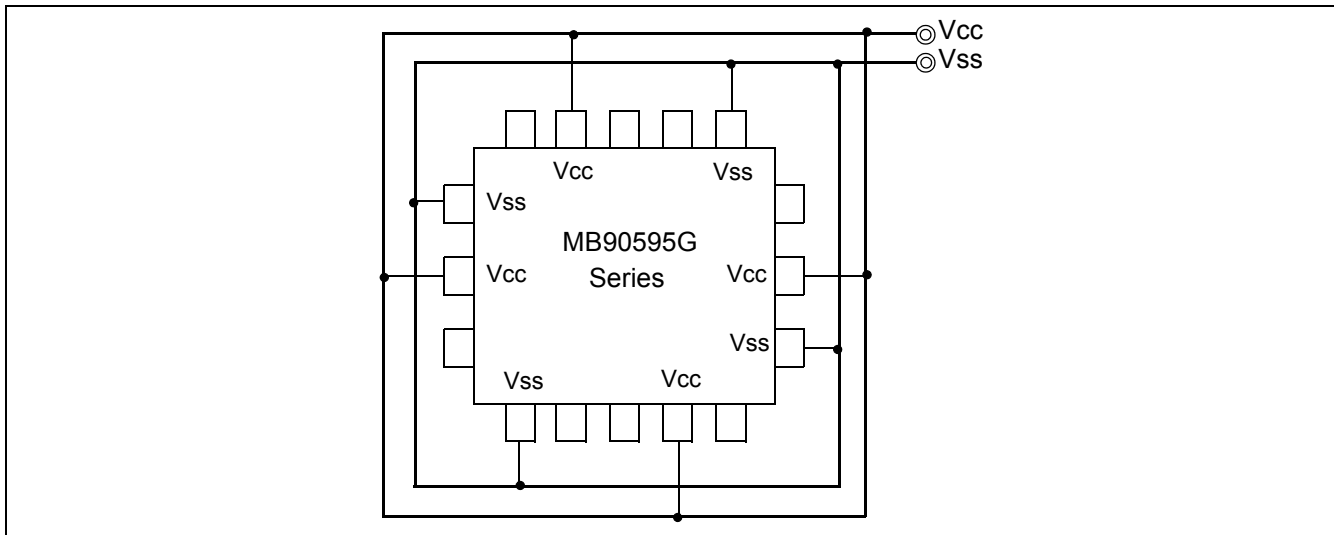


(4) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pins near the device.



(5) Pull-up/down resistors

The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVR_H, AVR_L) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVR_H or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to AV_{CC} = V_{CC}, AV_{SS} = AVR_H = DV_{CC} = V_{SS}.

(9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

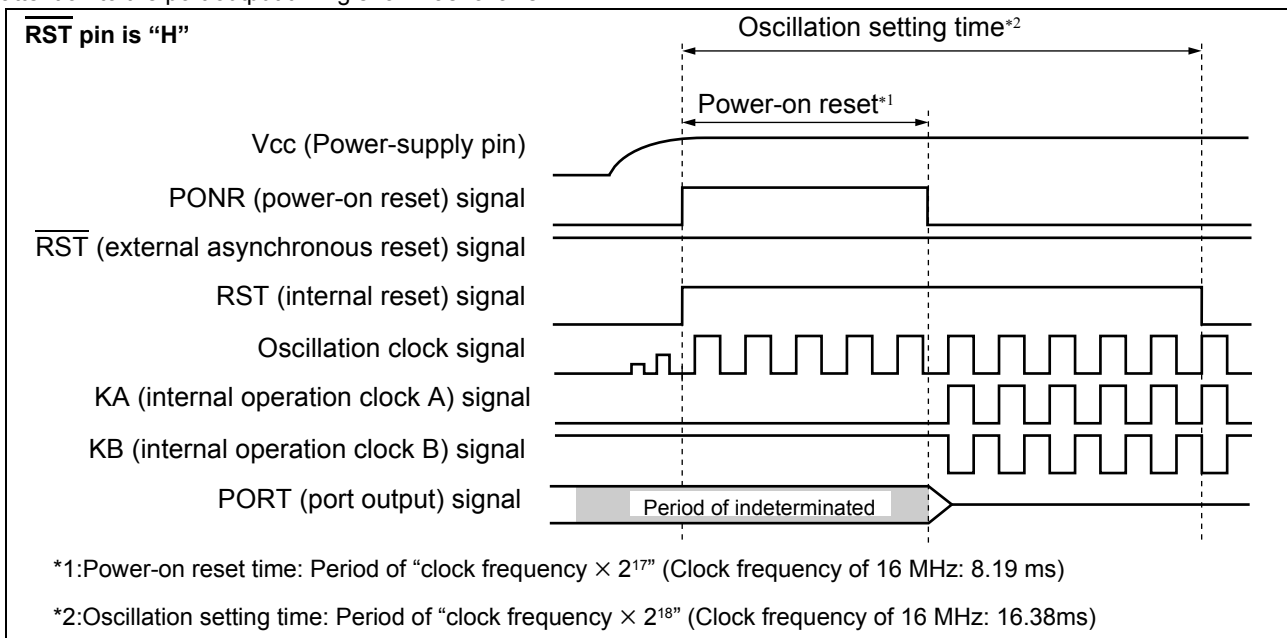
(10) Notes on Energization

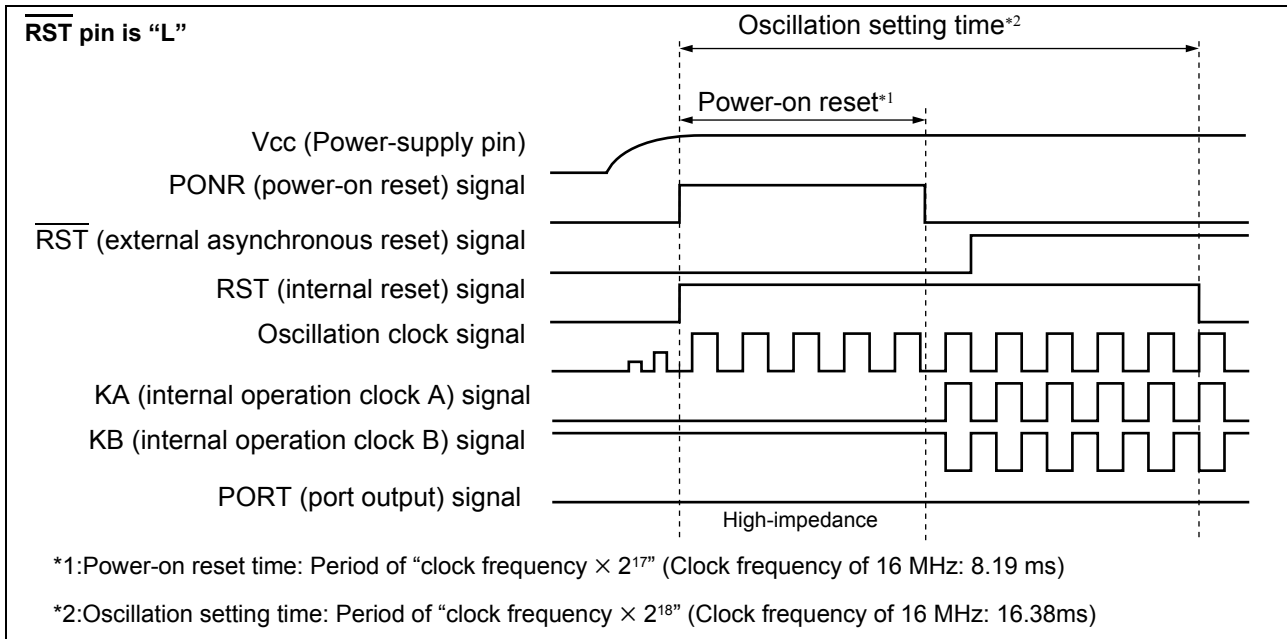
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{\text{RST}}$ pin is "H", the outputs become indeterminate.
 - If $\overline{\text{RST}}$ pin is "L", the outputs become high-impedance.
- Pay attention to the port output timing shown as follows.





(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

If the values of the corresponding bank register (DTB, ADB, USB, SSB) are set to other than "00H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

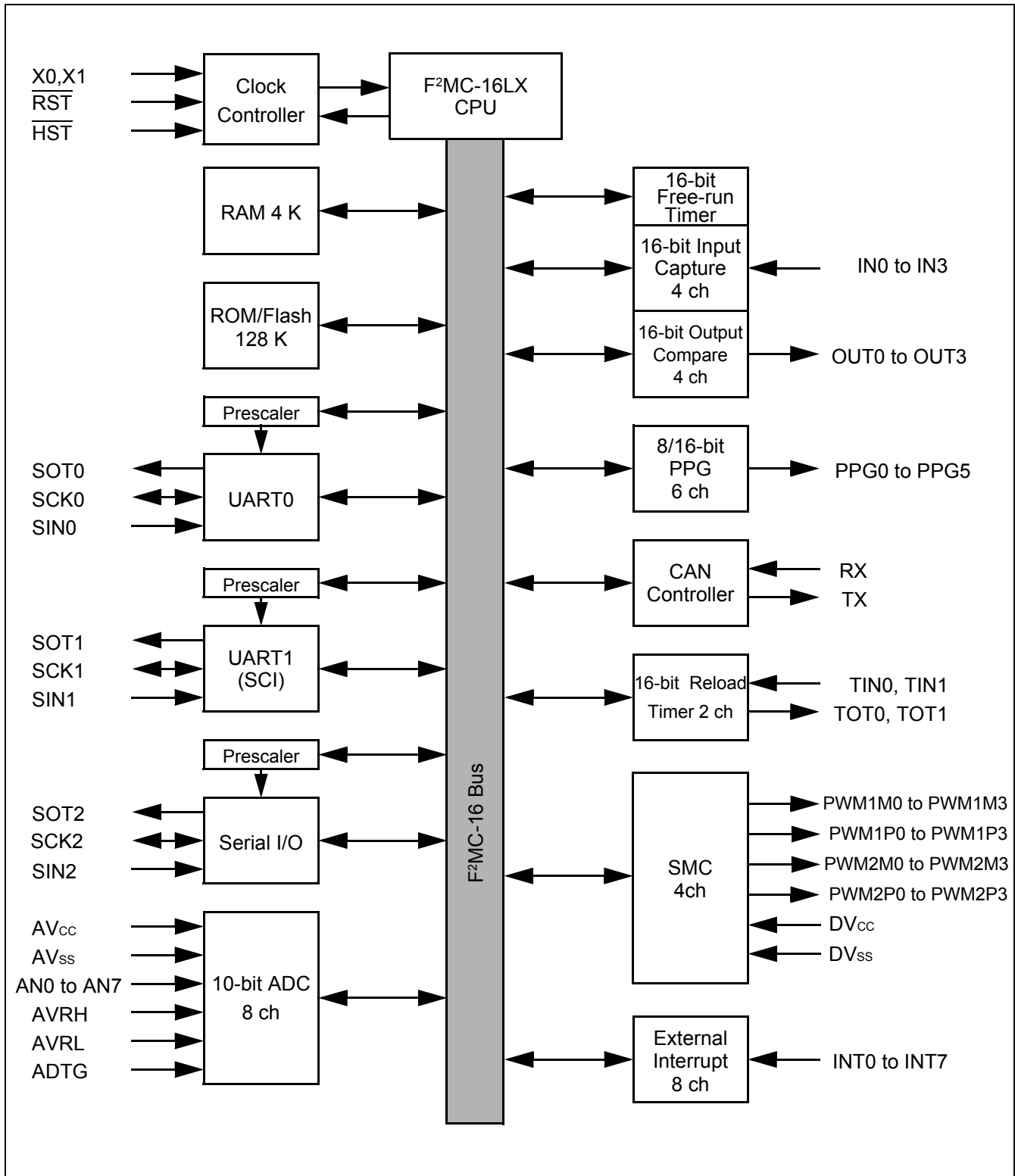
(14) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

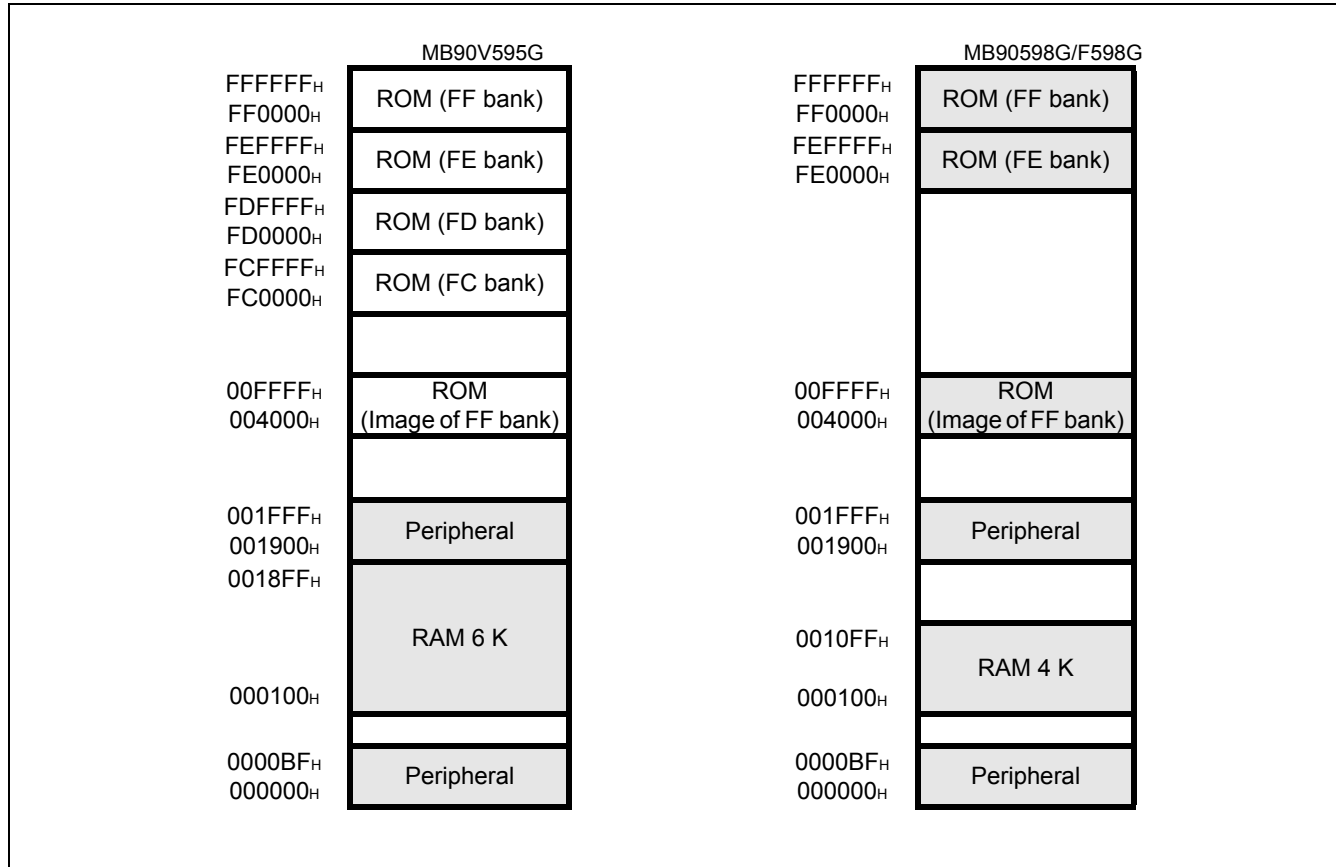
6. Block Diagram



7. Memory Space

The memory space of the MB90595G Series is shown below

Figure 1. Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating "far".
 For example, if an attempt has been made to access 00C000_H, the contents of the ROM at FFC000_H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000_H to FFFFFFF_H looks, therefore, as if it were the image for 004000_H to 00FFFF_H. Thus, it is recommended that the ROM data table be stored in the area of FF4000_H to FFFFFFF_H.

8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00 _H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
01 _H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
02 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
03 _H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
04 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
05 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
06 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
07 _H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
08 _H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
09 _H	Port 9 Data Register	PDR9	R/W	Port 9	__XXXXX _B
0A _H to 0F _H	Reserved				
10 _H	Port 0 Direction Register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
11 _H	Port 1 Direction Register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
12 _H	Port 2 Direction Register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
13 _H	Port 3 Direction Register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
14 _H	Port 4 Direction Register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0 _B
15 _H	Port 5 Direction Register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0 _B
16 _H	Port 6 Direction Register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0 _B
17 _H	Port 7 Direction Register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0 _B
18 _H	Port 8 Direction Register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0 _B
19 _H	Port 9 Direction Register	DDR9	R/W	Port 9	__0 0 0 0 0 0 _B
1A _H	Reserved				
1B _H	Analog Input Enable Register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1 _B
1C _H to 1F _H	Reserved				
20 _H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 1 0 0 _B
21 _H	Serial status Register 0	USR0	R/W		0 0 0 1 0 0 0 0 _B
22 _H	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W		XXXXXXXX _B
23 _H	Rate and Data Register 0	URD0	R/W		0 0 0 0 0 0 X _B
24 _H	Serial Mode Register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial Control Register 1	SCR1	R/W		0 0 0 0 1 0 0 0 _B
26 _H	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W		XXXXXXXX _B
27 _H	Serial Status Register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 _B
28 _H	UART1 Prescaler Control Register	U1CDCR	R/W		0 _ _ _ 1 1 1 1 _B

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
29 _H to 2A _H	Reserved				
2B _H	Serial IO Prescaler	SCDCR	R/W	Serial IO	0 ___ 1 1 1 1 _B
2C _H	Serial Mode Control Register (low-order)	SMCS	R/W		___ 0 0 0 0 _B
2D _H	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 1 0 _B
2E _H	Serial Data Register	SDR	R/W		XXXXXXXX _B
2F _H	Edge Selector	SES	R/W		___ 0 _B
30 _H	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 _B
31 _H	External Interrupt Request Register	EIRR	R/W		XXXXXXXX _B
32 _H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 _B
33 _H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 _B
34 _H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 _B
35 _H	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 _B
36 _H	A/D Data Register 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38 _H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1 _B
39 _H	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1 _B
3A _H	PPG0, 1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 _ _ _B
3B _H	Reserved				
3C _H	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1 _B
3D _H	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1 _B
3E _H	PPG2, 3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 _ _ _B
3F _H	Reserved				
40 _H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1 _B
41 _H	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1 _B
42 _H	PPG4, 5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 _ _ _B
43 _H	Reserved				
44 _H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1 _B
45 _H	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1 _B
46 _H	PPG6, 7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 _ _ _B
47 _H	Reserved				
48 _H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1 _B
49 _H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1 _B
4A _H	PPG8, 9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 _ _ _B
4B _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
4C _H	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0_000__1 _B
4D _H	PPGB Operation Mode Control Register	PPGCB	R/W		0_000001 _B
4E _H	PPGA, B Output Pin Control Register	PPGAB	R/W		000000__ _B
4F _H	Reserved				
50 _H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 _B
51 _H	Timer Control Status Register 0	TMCSR0	R/W		____0000 _B
52 _H	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
53 _H	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
54 _H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 _B
55 _H	Timer Control Status Register 1	TMCSR1	R/W		____0000 _B
56 _H	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
57 _H	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
58 _H	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0000__00 _B
59 _H	Output Compare Control Status Register 1	OCS1	R/W		__000000 _B
5A _H	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0000__00 _B
5B _H	Output Compare Control Status Register 3	OCS3	R/W		__000000 _B
5C _H	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
5D _H	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
5E _H	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	00000__0 _B
5F _H	Reserved				
60 _H	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	00000__0 _B
61 _H	Reserved				
62 _H	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	00000__0 _B
63 _H	Reserved				
64 _H	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	00000__0 _B
65 _H	Reserved				
66 _H	Timer Data Register (low-order)	TCDT	R/W	16-bit Free-run Timer	00000000 _B
67 _H	Timer Data Register (high-order)	TCDT	R/W		00000000 _B
68 _H	Timer Control Status Register	TCCS	R/W		00000000 _B
69 _H to 6E _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
6F _H	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	_____1 _B
70 _H	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX _B
71 _H	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX _B
72 _H	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0 _B
73 _H	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 _B
74 _H	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX _B
75 _H	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX _B
76 _H	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0 _B
77 _H	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 _B
78 _H	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX _B
79 _H	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX _B
7A _H	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0 _B
7B _H	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 _B
7C _H	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX _B
7D _H	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX _B
7E _H	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0 _B
7F _H	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 _B
80 _H to 8F _H	CAN Controller. Refer to section about CAN Controller				
90 _H to 9D _H	Reserved				
9E _H	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 _B
9F _H	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	_____0 _B
A0 _H	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0 _B
A1 _H	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0 _B
A2 _H to A7 _H	Reserved				
A8 _H	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
A9 _H	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 _ _ 0 0 1 0 0 _B
AA _H to AD _H	Reserved				
AE _H	Flash Memory Control Status Register (MB90F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0 _B
AF _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
B0 _H	Interrupt Control Register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B1 _H	Interrupt Control Register 01	ICR01	R/W		0 0 0 0 0 1 1 1 _B
B2 _H	Interrupt Control Register 02	ICR02	R/W		0 0 0 0 0 1 1 1 _B
B3 _H	Interrupt Control Register 03	ICR03	R/W		0 0 0 0 0 1 1 1 _B
B4 _H	Interrupt Control Register 04	ICR04	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B5 _H	Interrupt Control Register 05	ICR05	R/W		0 0 0 0 0 1 1 1 _B
B6 _H	Interrupt Control Register 06	ICR06	R/W		0 0 0 0 0 1 1 1 _B
B7 _H	Interrupt Control Register 07	ICR07	R/W		0 0 0 0 0 1 1 1 _B
B8 _H	Interrupt Control Register 08	ICR08	R/W		0 0 0 0 0 1 1 1 _B
B9 _H	Interrupt Control Register 09	ICR09	R/W		0 0 0 0 0 1 1 1 _B
BA _H	Interrupt Control Register 10	ICR10	R/W		0 0 0 0 0 1 1 1 _B
BB _H	Interrupt Control Register 11	ICR11	R/W		0 0 0 0 0 1 1 1 _B
BC _H	Interrupt Control Register 12	ICR12	R/W		0 0 0 0 0 1 1 1 _B
BD _H	Interrupt Control Register 13	ICR13	R/W		0 0 0 0 0 1 1 1 _B
BE _H	Interrupt Control Register 14	ICR14	R/W		0 0 0 0 0 1 1 1 _B
BF _H	Interrupt Control Register 15	ICR15	R/W		0 0 0 0 0 1 1 1 _B
C0 _H to FF _H	Reserved				
1900 _H	Reload Register L	PRL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
1901 _H	Reload Register H	PRLH0	R/W		XXXXXXXX _B
1902 _H	Reload Register L	PRL1	R/W		XXXXXXXX _B
1903 _H	Reload Register H	PRLH1	R/W		XXXXXXXX _B
1904 _H	Reload Register L	PRL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
1905 _H	Reload Register H	PRLH2	R/W		XXXXXXXX _B
1906 _H	Reload Register L	PRL3	R/W		XXXXXXXX _B
1907 _H	Reload Register H	PRLH3	R/W		XXXXXXXX _B
1908 _H	Reload Register L	PRL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
1909 _H	Reload Register H	PRLH4	R/W		XXXXXXXX _B
190A _H	Reload Register L	PRL5	R/W		XXXXXXXX _B
190B _H	Reload Register H	PRLH5	R/W		XXXXXXXX _B
190C _H	Reload Register L	PRL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
190D _H	Reload Register H	PRLH6	R/W		XXXXXXXX _B
190E _H	Reload Register L	PRL7	R/W		XXXXXXXX _B
190F _H	Reload Register H	PRLH7	R/W		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910 _H	Reload Register L	PRL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX _B
1911 _H	Reload Register H	PRLH8	R/W		XXXXXXXX _B
1912 _H	Reload Register L	PRL9	R/W		XXXXXXXX _B
1913 _H	Reload Register H	PRLH9	R/W		XXXXXXXX _B
1914 _H	Reload Register L	PRLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX _B
1915 _H	Reload Register H	PRLHA	R/W		XXXXXXXX _B
1916 _H	Reload Register L	PRLB	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX _B
1917 _H	Reload Register H	PRLHB	R/W		XXXXXXXX _B
1918 _H to 191F _H	Reserved				
1920 _H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
1921 _H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXX _B
1922 _H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXX _B
1923 _H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXX _B
1924 _H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
1925 _H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXX _B
1926 _H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXX _B
1927 _H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXX _B
1928 _H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
1929 _H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXX _B
192A _H	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXX _B
192B _H	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXX _B

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Address	Register	Abbreviation	Access	Peripheral	Initial value
192C _H	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
192D _H	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX _B
192E _H	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX _B
192F _H	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX _B
1930 _H to 19FF _H	Reserved				
1A00 _H to 1AFF _H	CAN Controller. Refer to section about CAN Controller				
1B00 _H to 1BFF _H	CAN Controller. Refer to section about CAN Controller				
1C00 _H to 1EFF _H	Reserved				
1FF0 _H	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX _B
1FF1 _H	Program Address Detection Register 0 (middle-order)				XXXXXXXX _B
1FF2 _H	Program Address Detection Register 0 (high-order)				XXXXXXXX _B
1FF3 _H	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX _B
1FF4 _H	Program Address Detection Register 1 (middle-order)				XXXXXXXX _B
1FF5 _H	Program Address Detection Register 1 (high-order)				XXXXXXXX _B
1FF6 _H to 1FFF _H	Reserved				

■ Description for Read/Write

R/W : Readable/writable

R : Read only

W : Write only

■ Description of initial value

0 : the initial value of this bit is "0".

1 : the initial value of this bit is "1".

X : the initial value of this bit is undefined.

_ : this bit is unused. the initial value is undefined.

Note : Addresses in the range of 0000_H to 00FF_H, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading "X", and any write access should not be performed.

9. Can Controller

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
 - - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame format
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

9.1 List of Control Registers

Address	Register	Abbreviation	Access	Initial Value
000080 _H	Message buffer valid register	BVALR	R/W	00000000 00000000 _B
000081 _H				
000082 _H	Transmit request register	TREQR	R/W	00000000 00000000 _B
000083 _H				
000084 _H	Transmit cancel register	TCANR	W	00000000 00000000 _B
000085 _H				
000086 _H	Transmit complete register	TCR	R/W	00000000 00000000 _B
000087 _H				
000088 _H	Receive complete register	RCR	R/W	00000000 00000000 _B
000089 _H				
00008A _H	Remote request receiving register	RRTRR	R/W	00000000 00000000 _B
00008B _H				
00008C _H	Receive overrun register	ROVRR	R/W	00000000 00000000 _B
00008D _H				
00008E _H	Receive interrupt enable register	RIER	R/W	00000000 00000000 _B
00008F _H				
001B00 _H	Control status register	CSR	R/W, R	00---000 0----0-1 _B
001B01 _H				
001B02 _H	Last event indicator register	LEIR	R/W	----- 000-0000 _B
001B03 _H				
001B04 _H	Receive/transmit error counter	RTEC	R	00000000 00000000 _B
001B05 _H				
001B06 _H	Bit timing register	BTR	R/W	-1111111 11111111 _B
001B07 _H				

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Address	Register	Abbreviation	Access	Initial Value
001B08 _H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX _B
001B09 _H				
001B0A _H	Transmit RTR register	TRTRR	R/W	00000000 00000000 _B
001B0B _H				
001B0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX _B
001B0D _H				
001B0E _H	Transmit interrupt enable register	TIER	R/W	00000000 00000000 _B
001B0F _H				
001B10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX _B
001B11 _H				XXXXXXXX XXXXXXXX _B
001B12 _H				XXXXXXXX XXXXXXXX _B
001B13 _H				XXXXXXXX XXXXXXXX _B
001B14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX _B
001B15 _H				XXXXX--- XXXXXXXX _B
001B16 _H				XXXXX--- XXXXXXXX _B
001B17 _H				XXXXX--- XXXXXXXX _B
001B18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX _B
001B19 _H				XXXXX--- XXXXXXXX _B
001B1A _H				XXXXX--- XXXXXXXX _B
001B1B _H				XXXXX--- XXXXXXXX _B

9.2 List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
001A00 _H to 001A1F _H	General-purpose RAM	--	R/W	XXXXXXXX _B to XXXXXXXX _B
001A20 _H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX _B
001A21 _H				XXXXX--- XXXXXXXX _B
001A22 _H				XXXXX--- XXXXXXXX _B
001A23 _H				XXXXX--- XXXXXXXX _B
001A24 _H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX _B
001A25 _H				XXXXX--- XXXXXXXX _B
001A26 _H				XXXXX--- XXXXXXXX _B
001A27 _H				XXXXX--- XXXXXXXX _B
001A28 _H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX _B
001A29 _H				XXXXX--- XXXXXXXX _B
001A2A _H				XXXXX--- XXXXXXXX _B
001A2B _H				XXXXX--- XXXXXXXX _B

Address	Register	Abbreviation	Access	Initial Value
001A2C _H	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX _B
001A2D _H				XXXXXXXX-- XXXXXXXX _B
001A2E _H				
001A2F _H				
001A30 _H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX _B
001A31 _H				XXXXXXXX-- XXXXXXXX _B
001A32 _H				
001A33 _H				
001A34 _H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX _B
001A35 _H				XXXXXXXX-- XXXXXXXX _B
001A36 _H				
001A37 _H				
001A38 _H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX _B
001A39 _H				XXXXXXXX-- XXXXXXXX _B
001A3A _H				
001A3B _H				
001A3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
001A3D _H				XXXXXXXX-- XXXXXXXX _B
001A3E _H				
001A3F _H				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
001A40 _H	ID register 8	IDR8	R/W	XXXXXXXXXXXXXXXX _B
001A41 _H				
001A42 _H				
001A43 _H				XXXXX---XXXXXXXX _B
001A44 _H	ID register 9	IDR9	R/W	XXXXXXXXXXXXXXXX _B
001A45 _H				
001A46 _H				
001A47 _H				XXXXX---XXXXXXXX _B
001A48 _H	ID register 10	IDR10	R/W	XXXXXXXXXXXXXXXX _B
001A49 _H				
001A4A _H				
001A4B _H				XXXXX---XXXXXXXX _B
001A4C _H	ID register 11	IDR11	R/W	XXXXXXXXXXXXXXXX _B
001A4D _H				
001A4E _H				
001A4F _H				XXXXX---XXXXXXXX _B
001A50 _H	ID register 12	IDR12	R/W	XXXXXXXXXXXXXXXX _B
001A51 _H				
001A52 _H				
001A53 _H				XXXXX---XXXXXXXX _B
001A54 _H	ID register 13	IDR13	R/W	XXXXXXXXXXXXXXXX _B
001A55 _H				
001A56 _H				
001A57 _H				XXXXX---XXXXXXXX _B
001A58 _H	ID register 14	IDR14	R/W	XXXXXXXXXXXXXXXX _B
001A59 _H				
001A5A _H				
001A5B _H				XXXXX---XXXXXXXX _B
001A5C _H	ID register 15	IDR15	R/W	XXXXXXXXXXXXXXXX _B
001A5D _H				
001A5E _H				
001A5F _H				XXXXX---XXXXXXXX _B

9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60 _H	DLC register 0	DLCR0	R/W	---XXXX _B
001A61 _H				
001A62 _H	DLC register 1	DLCR1	R/W	---XXXX _B
001A63 _H				
001A64 _H	DLC register 2	DLCR2	R/W	---XXXX _B
001A65 _H				
001A66 _H	DLC register 3	DLCR3	R/W	---XXXX _B
001A67 _H				
001A68 _H	DLC register 4	DLCR4	R/W	---XXXX _B
001A69 _H				
001A6A _H	DLC register 5	DLCR5	R/W	---XXXX _B
001A6B _H				
001A6C _H	DLC register 6	DLCR6	R/W	---XXXX _B
001A6D _H				
001A6E _H	DLC register 7	DLCR7	R/W	---XXXX _B
001A6F _H				
001A70 _H	DLC register 8	DLCR8	R/W	---XXXX
001A71 _H				
001A72 _H	DLC register 9	DLCR9	R/W	---XXXX _B
001A73 _H				
001A74 _H	DLC register 10	DLCR10	R/W	---XXXX _B
001A75 _H				
001A76 _H	DLC register 11	DLCR11	R/W	---XXXX _B
001A77 _H				
001A78 _H	DLC register 12	DLCR12	R/W	---XXXX _B
001A79 _H				
001A7A _H	DLC register 13	DLCR13	R/W	---XXXX _B
001A7B _H				
001A7C _H	DLC register 14	DLCR14	R/W	---XXXX _B
001A7D _H				
001A7E _H	DLC register 15	DLCR15	R/W	---XXXX _B
001A7F _H				
001A80 _H to 001A87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B

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Address	Register	Abbreviation	Access	Initial Value
001A88 _H to 001A8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
001A90 _H to 001A97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
001A98 _H to 001A9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
001AA0 _H to 001AA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
001AA8 _H to 001AAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
001AB0 _H to 001AB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
001AB8 _H to 001ABF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
001AC0 _H to 001AC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
001AC8 _H to 001ACF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
001AD0 _H to 001AD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
001AD8 _H to 001ADF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
001AE0 _H to 001AE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
001AE8 _H to 001AEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
001AF0 _H to 001AF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
001AF8 _H to 001AFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

Interrupt source	EI ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	# 08	FFFFDC _H	—	—
INT9 instruction	N/A	# 09	FFFFD8 _H	—	—
Exception	N/A	# 10	FFFFD4 _H	—	—
CAN RX	N/A	# 11	FFFFD0 _H	ICR00	0000B0 _H
CAN TX/NS	N/A	# 12	FFFFCC _H		
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8 _H	ICR01	0000B1 _H
Time Base Timer	N/A	# 14	FFFFC4 _H		
16-bit Reload Timer 0	*1	# 15	FFFFC0 _H	ICR02	0000B2 _H
8/10-bit A/D Converter	*1	# 16	FFFFBC _H		
16-bit Free-run Timer	N/A	# 17	FFFFB8 _H	ICR03	0000B3 _H
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4 _H		
Serial I/O	*1	# 19	FFFFB0 _H	ICR04	0000B4 _H
External Interrupt (INT4/INT5)	*1	# 20	FFFFAC _H		
Input Capture 0	*1	# 21	FFFFA8 _H	ICR05	0000B5 _H
8/16-bit PPG 0/1	N/A	# 22	FFFFA4 _H		
Output Compare 0	*1	# 23	FFFFA0 _H	ICR06	0000B6 _H
8/16-bit PPG 2/3	N/A	# 24	FFFF9C _H		
External Interrupt (INT6/INT7)	*1	# 25	FFFF98 _H	ICR07	0000B7 _H
Input Capture 1	*1	# 26	FFFF94 _H		
8/16-bit PPG 4/5	N/A	# 27	FFFF90 _H	ICR08	0000B8 _H
Output Compare 1	*1	# 28	FFFF8C _H		
8/16-bit PPG 6/7	N/A	# 29	FFFF88 _H	ICR09	0000B9 _H
Input Capture 2	*1	# 30	FFFF84 _H		
8/16-bit PPG 8/9	N/A	# 31	FFFF80 _H	ICR10	0000BA _H
Output Compare 2	*1	# 32	FFFF7C _H		
Input Capture 3	*1	# 33	FFFF78 _H	ICR11	0000BB _H
8/16-bit PPG A/B	N/A	# 34	FFFF74 _H		
Output Compare 3	*1	# 35	FFFF70 _H	ICR12	0000BC _H
16-bit Reload Timer 1	*1	# 36	FFFF6C _H		
UART 0 RX	*2	# 37	FFFF68 _H	ICR13	0000BD _H
UART 0 TX	*1	# 38	FFFF64 _H		
UART 1 RX	*2	# 39	FFFF60 _H	ICR14	0000BE _H
UART 1 TX	*1	# 40	FFFF5C _H		
Flash Memory	N/A	# 41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N/A	# 42	FFFF54 _H		

*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A: The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Notes:

- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	AV_{RH} , AV_{RL}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AV_{RH}/L$, $AV_{RH} \geq AV_{RL}$ *1
	DV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} \geq DV_{CC}$
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum Clamp Current	I_{CLAMP}	-2.0	2.0	mA	*6
Maximum Total Clamp Current	$\sum I_{CLAMP} $	—	20	mA	*6
"L" level Max. output current	I_{OL1}	—	15	mA	Normal output *3
"L" level Avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
"L" level Max. output current	I_{OL2}	—	40	mA	High current output *3
"L" level Avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
"L" level Max. overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
"L" level Max. overall output current	$\sum I_{OL2}$	—	330	mA	Total high current output
"L" level Avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
"L" level Avg. overall output current	$\sum I_{OLAV2}$	—	250	mA	Total high current output, average value *5
"H" level Max. output current	I_{OH1}	—	-15	mA	Normal output *3
"H" level Avg. output current	I_{OHAV1}	—	-4	mA	Normal output, average value *4
"H" level Max. output current	I_{OH2}	—	-40	mA	High current output *3
"H" level Avg. output current	I_{OHAV2}	—	-30	mA	High current output, average value *4
"H" level Max. overall output current	$\sum I_{OH1}$	—	-100	mA	Total normal output
"H" level Max. overall output current	$\sum I_{OH2}$	—	-330	mA	Total high current output
"H" level Avg. overall output current	$\sum I_{OHAV1}$	—	-50	mA	Total normal output, average value *5
"H" level Avg. overall output current	$\sum I_{OHAV2}$	—	-250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F598G
		—	400	mW	MB90598G
Operating temperature	T_A	-40	+85	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1: AV_{CC} , AV_{RH} , AV_{RL} and DV_{CC} shall not exceed V_{CC} . AV_{RH} and AV_{RL} shall not exceed AV_{CC} . Also, AV_{RL} shall never exceed AV_{RH} .

*2: V_I and V_O should not exceed $V_{CC} + 0.3\text{V}$. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

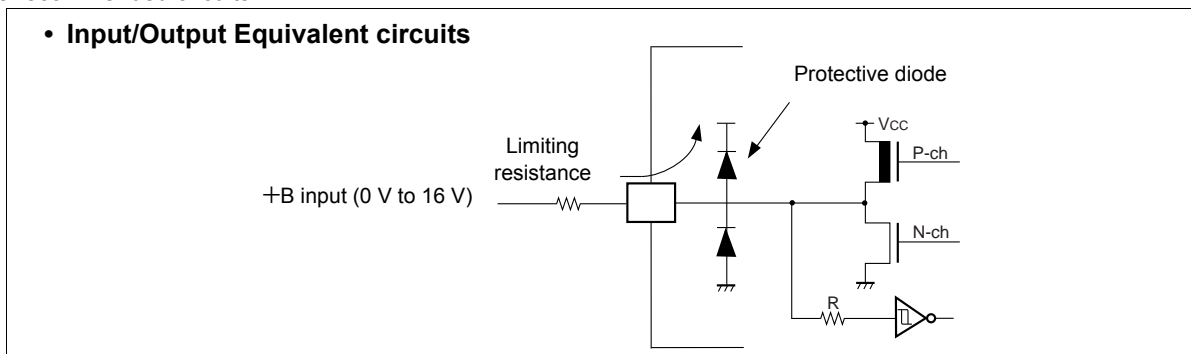
*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6:

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :



Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

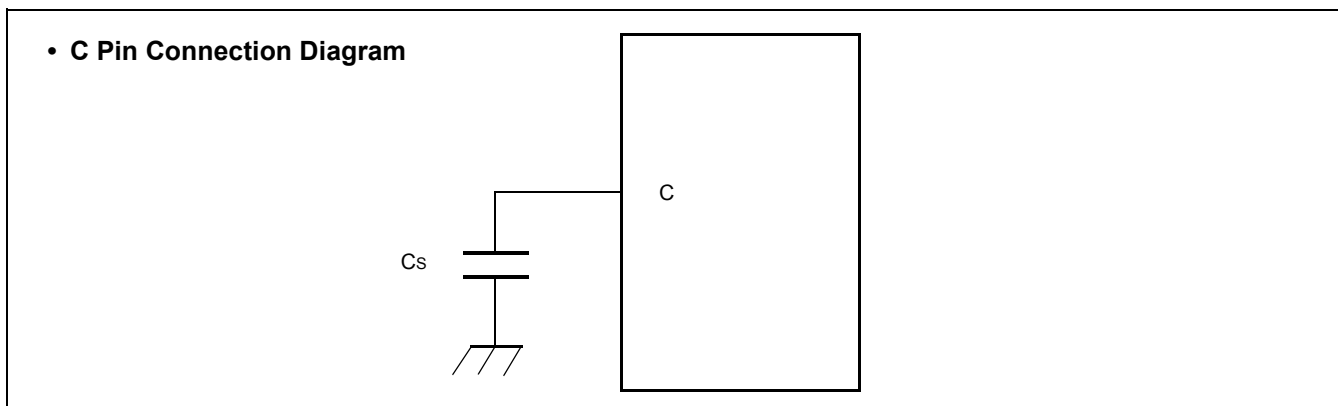
11.2 Recommended Conditions
 $(V_{SS} = AV_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	Under normal operation
	AV_{CC}	3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	μF	*
Operating temperature	T_A	-40	—	+85	$^{\circ}\text{C}$	

*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S .

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.


11.3 DC Characteristics
 $(V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C})$

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHM}	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{ILM}	MD input pin	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH1}	Output pins except P70 to P87	$V_{CC} = 4.5 \text{ V}, I_{OH1} = -4.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	V_{OH2}	P70 to P87	$V_{CC} = 4.5 \text{ V}, I_{OH2} = -30.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL1}	Output pins except P70 to P87	$V_{CC} = 4.5 \text{ V}, I_{OL1} = 4.0 \text{ mA}$	—	—	0.4	V	
	V_{OL2}	P70 to P87	$V_{CC} = 4.5 \text{ V}, I_{OL2} = 30.0 \text{ mA}$	—	—	0.5	V	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}		$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-5	—	5	μA	
Power supply current *	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V} \pm 10\%$, Internal frequency: 16 MHz, At normal operating	—	35	60	mA	MB90598G
				—	40	60	mA	MB90F598G
	I_{CCS}		$V_{CC} = 5.0\text{ V} \pm 10\%$, Internal frequency: 16 MHz, At sleep	—	11	18	mA	
	I_{CTS}		$V_{CC} = 5.0\text{ V} \pm 1\%$, Internal frequency: 2 MHz, At timer mode	—	0.3	0.6	mA	
	I_{CCH}		$V_{CC} = 5.0\text{ V} \pm 10\%$, At stop, $T_A = 25^\circ\text{C}$	—	—	20	μA	
	I_{CCH2}		$V_{CC} = 5.0\text{ V} \pm 10\%$, At Hardware stand- by mode, $T_A = 25^\circ\text{C}$	—	—	20	μA	MB90598G
				—	50	100	μA	MB90F598G

(Continued)

(Continued)

 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV _{CC} , AV _{SS} , AVRH, AVRL, V _{CC} , V _{SS} , DV _{CC} , DV _{SS} , P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	\overline{RST}	—	25	50	100	k Ω	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	k Ω	

* : The power supply current testing conditions are when using the external clock.

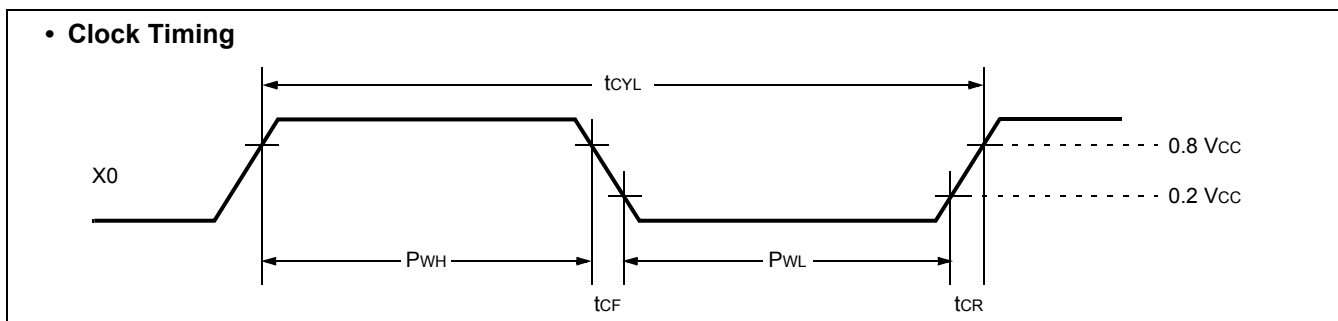
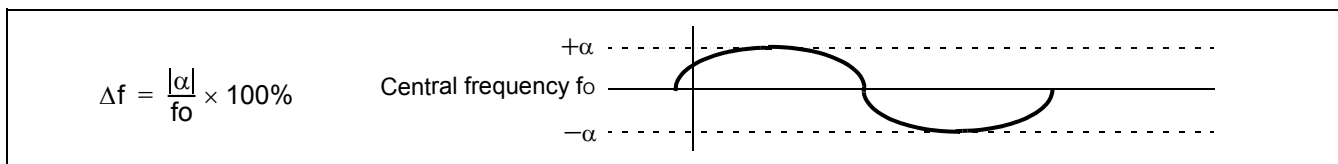
11.4 AC Characteristics

11.4.1 Clock Timing

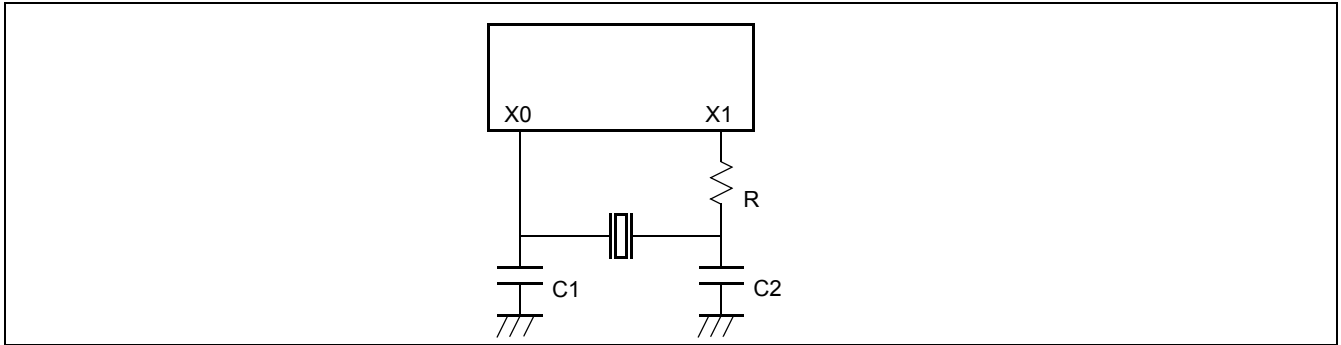
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$

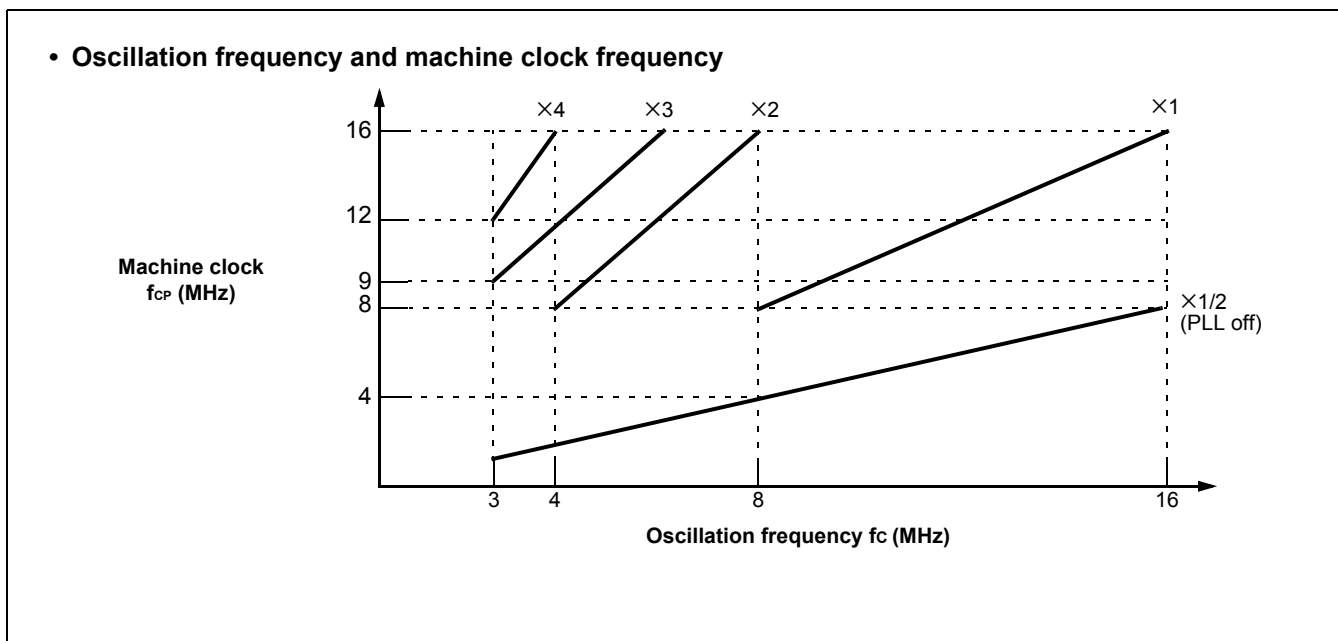
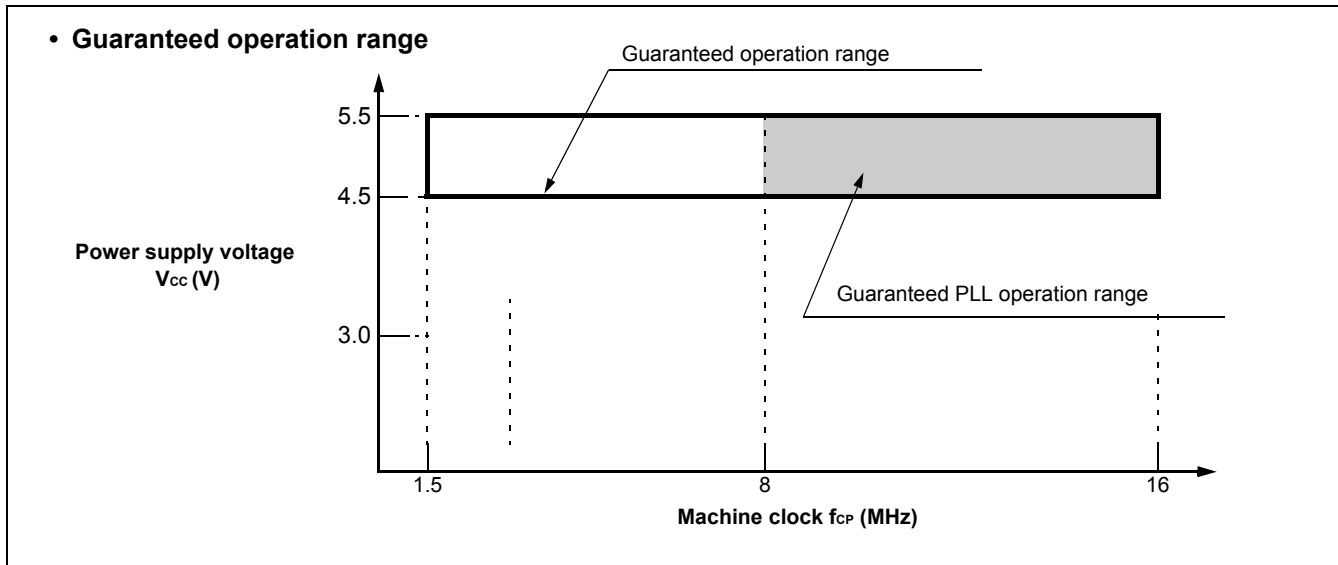
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	5	MHz	When using oscillation circuit
Oscillation cycle time	t_{CYL}	X0, X1	200	—	333	ns	When using oscillation circuit
External clock frequency	f_C	X0, X1	3	—	16	MHz	When using external clock
External clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using external clock
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash Read cycle time	t_{CYL}	—	—	$2 \cdot t_{CP}$	—	ns	When Flash is accessed via CPU

*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

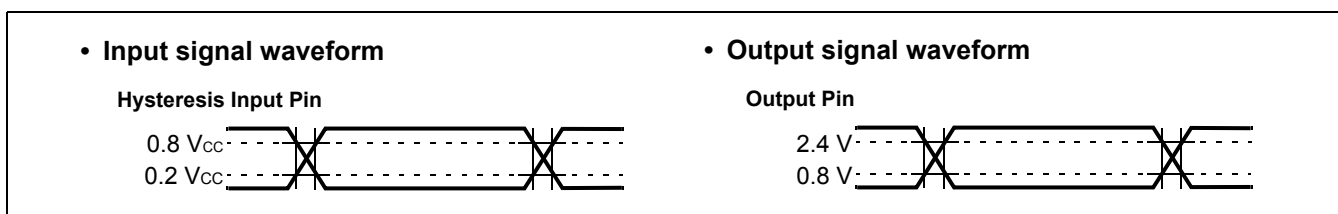


■ Example of Oscillation circuit





AC characteristics are set to the measured reference voltage values below.



11.4.2 Reset and Hardware Standby Input
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C})$

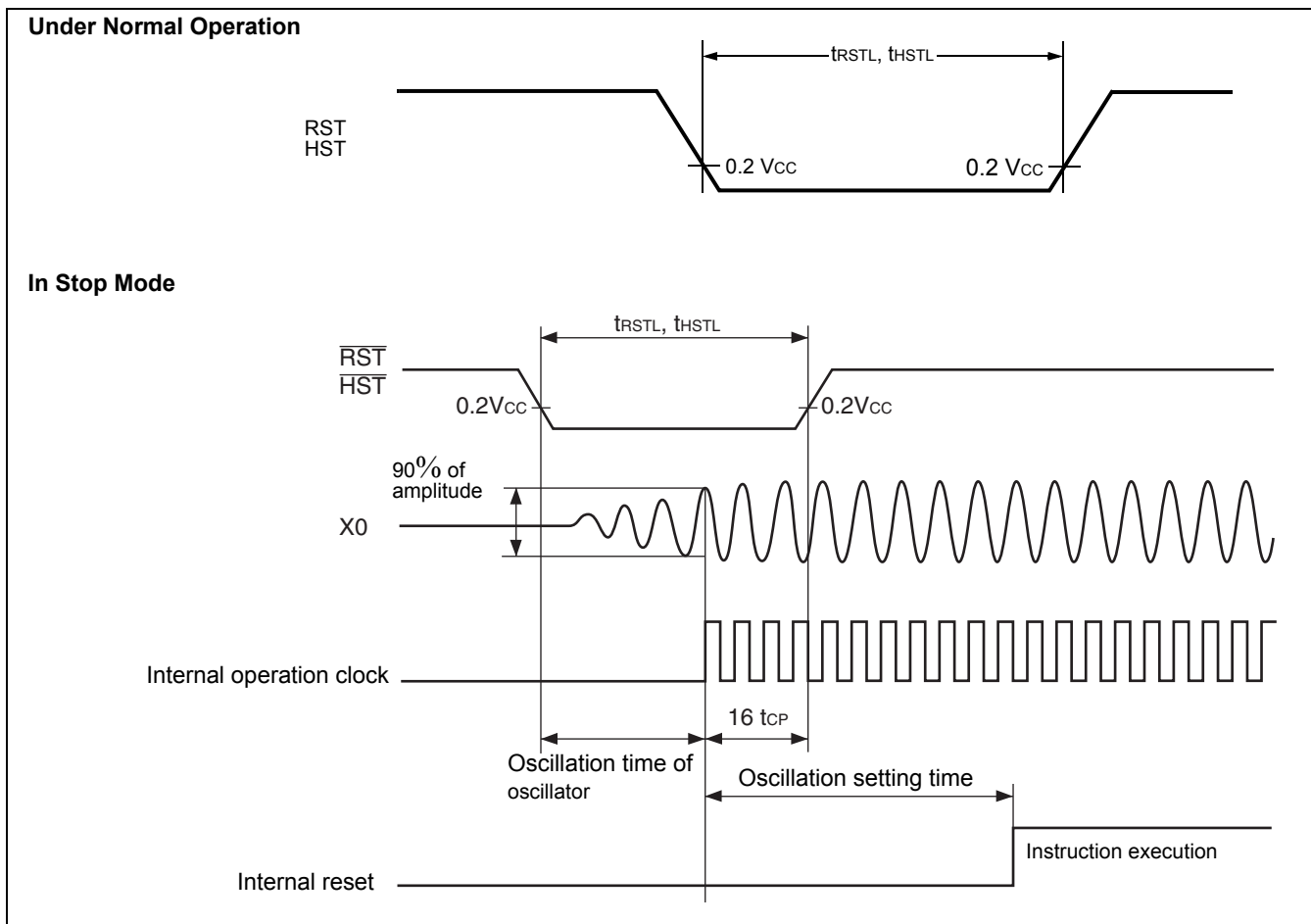
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	\overline{RST}	$16 t_{CP}^{*1}$	—	ns	Under normal operation
			Oscillation time of oscillator ^{*2} + $16 t_{CP}^{*1}$	—	ms	In stop mode
Hardware standby input time	t_{HSTL}	\overline{HST}	$16 t_{CP}^{*1}$	—	ns	Under normal operation
			Oscillation time of oscillator ^{*2} + $16 t_{CP}^{*1}$	—	ms	In stop mode

*1: “ t_{CP} ” represents one cycle time of the machine clock.

No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.

In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.



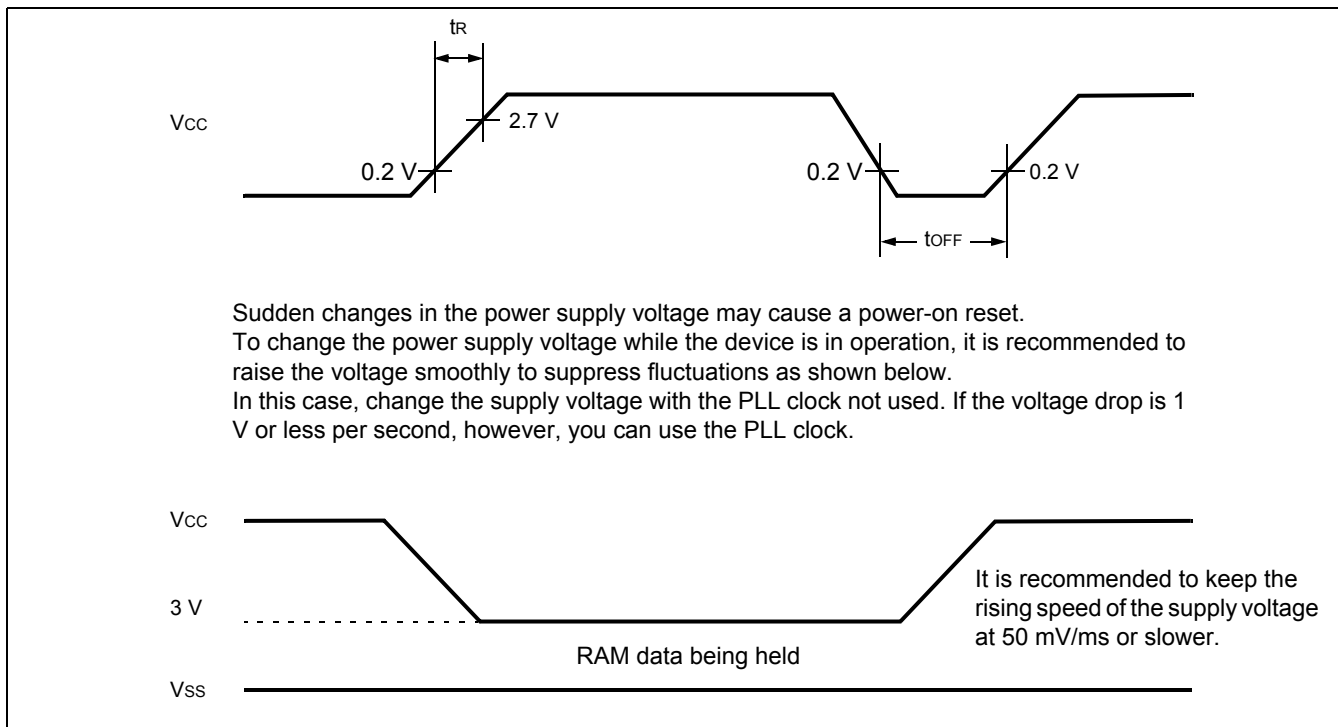
11.4.3 Power On Reset
 $(V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0\text{ V}, T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

*: V_{CC} must be kept lower than 0.2 V before power-on.

Notes:

- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn on the power supply using the above values.


11.4.4 UART0/1, Serial I/O Timing
 $(V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0\text{ V}, T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$

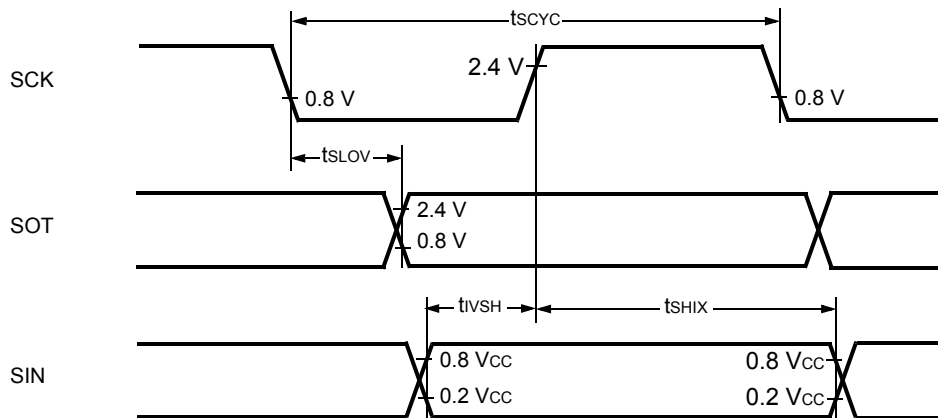
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	8 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		-80	80	ns	
Valid SIN ⇒ SCK ↑	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

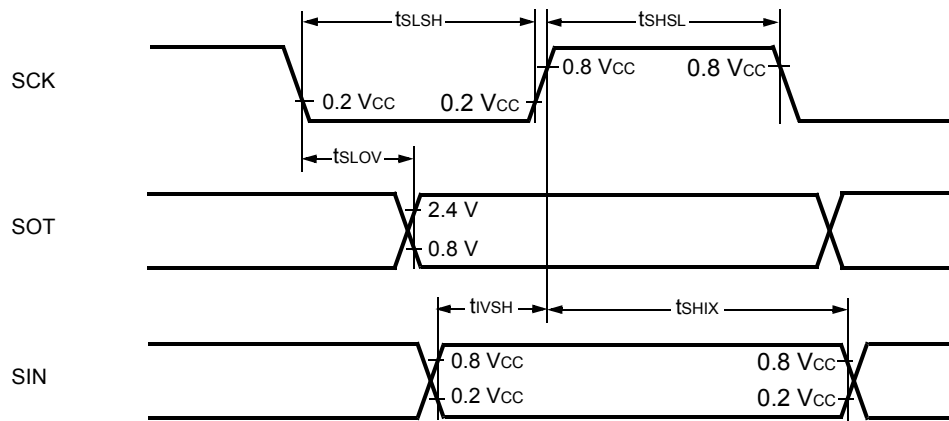
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are $C_L = 80$ pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK $\downarrow \Rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN \Rightarrow SCK \uparrow	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK $\uparrow \Rightarrow$ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes:

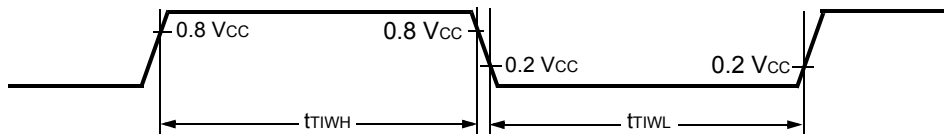
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} (external operation clock cycle time) : see Clock timing.

• Internal Shift Clock Mode

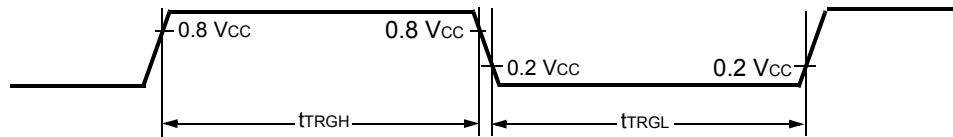


External Shift Clock Mode

(5) Timer Input Timing
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4 t_{CP}$	—	ns	
	t_{TIWL}	IN0 to IN3					

Timer Input Timing

11.4.5 Trigger Input Timing
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	INT0 to INT7, ADTG	—	$5 t_{CP}$	—	ns	Under normal operation
	t_{TRGL}			1	—		μs

• Trigger Input Timing

11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	150	ns	

• Slew Rate Output Timing


$$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$$

$$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$$

11.5 A/D Converter
 $(V_{CC} = AV_{CC} = 5.0 V \pm 10\%, V_{SS} = AV_{SS} = 0.0 V, 3.0 V \leq AV_{RH} - AV_{RL}, T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$

Parameter	Sym- bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	± 5.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential linearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{RL} - 3.5 \text{ LSB}$	$AV_{RL} + 0.5 \text{ LSB}$	$AV_{RL} + 4.5 \text{ LSB}$	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	$AV_{RH} - 6.5 \text{ LSB}$	$AV_{RH} - 1.5 \text{ LSB}$	$AV_{RH} + 1.5 \text{ LSB}$	V	
Conversion time	—	—	—	$352t_{CP}$	—	ns	
Sampling time	—	—	—	$64t_{CP}$	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	-10	—	10	μA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AV_{RL}	—	AV_{RH}	V	

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	—	AVRH	AVRL + 3.0	—	AVCC	V	
	—	AVRL	0	—	AVRH – 3.0	V	
Power supply current	I _A	AVCC	—	5	—	mA	
	I _{AH}	AVCC	—	—	5	μA	*
Reference voltage current	I _R	AVRH	—	400	600	μA	MB90V595G, MB90F598G
			—	140	600	μA	MB90598G
	I _{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current ($V_{CC} = AV_{CC} = AVRH = 5.0$ V) when the CPU is stopped.

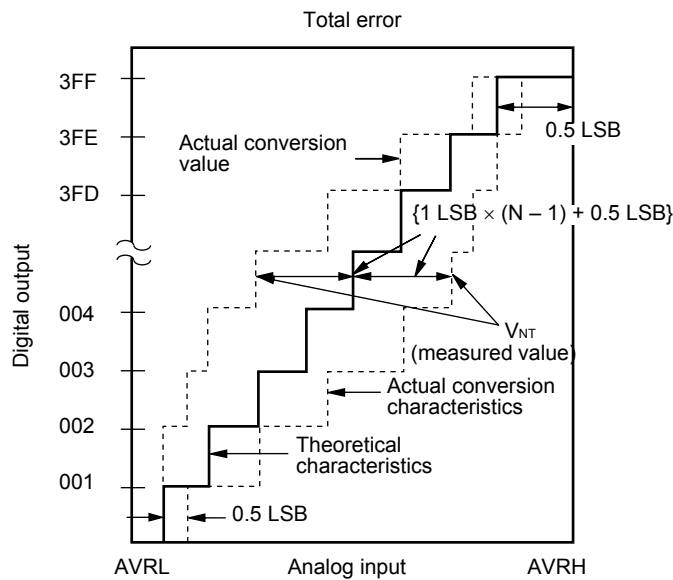
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

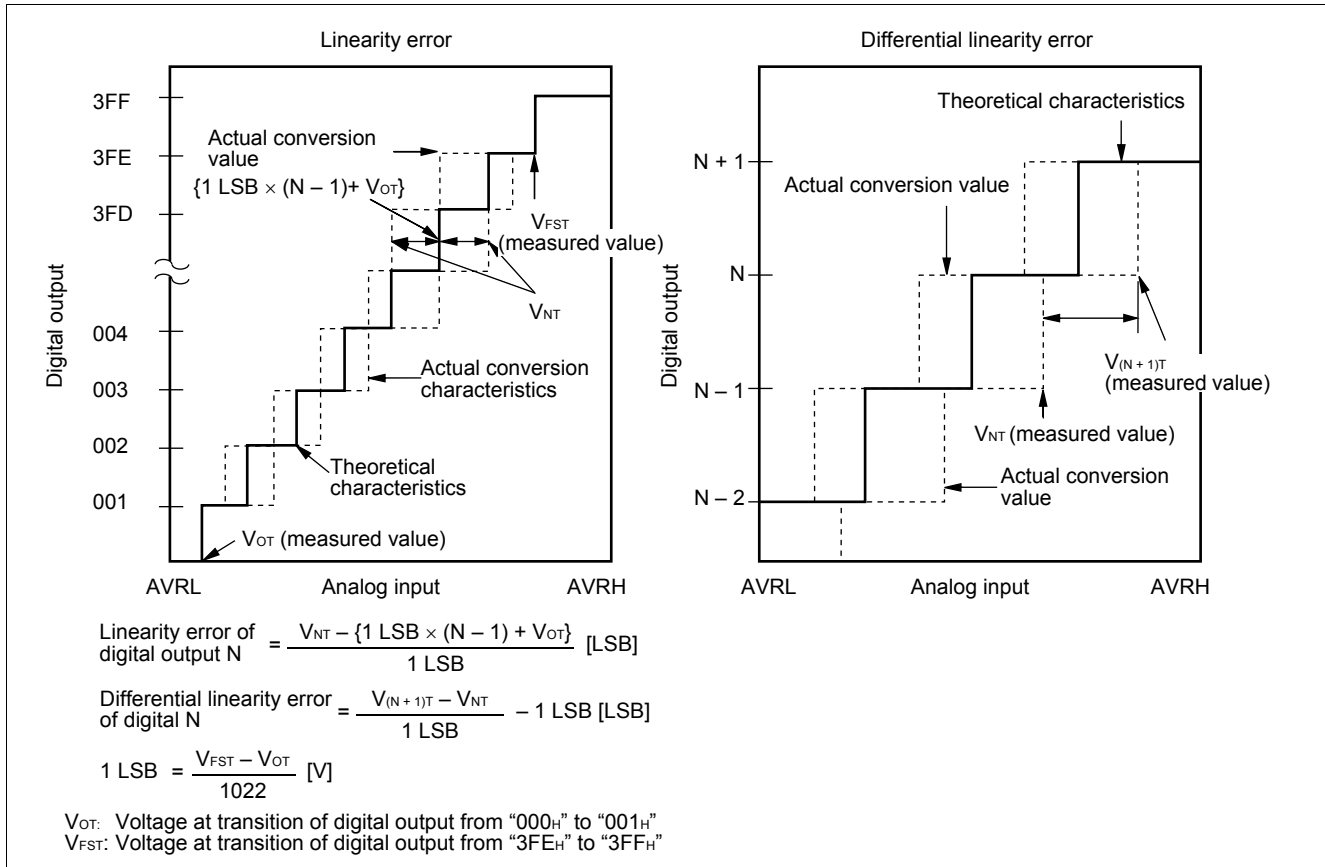
$$V_{OT} \text{ (Theoretical value)} = \text{AVRL} + 0.5 \text{ LSB [V]}$$

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

$$V_{FST} \text{ (Theoretical value)} = \text{AVRH} - 1.5 \text{ LSB [V]}$$

(Continued)

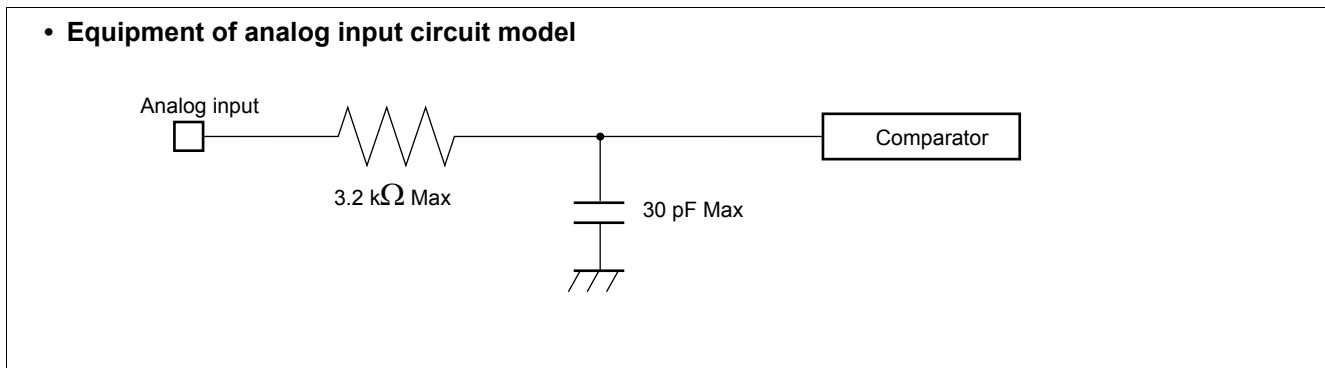
(Continued)



11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions.:

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
 - When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.
- When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).



■ Error

The smaller the | AVRH – AVRL |, the greater the error would become relatively.

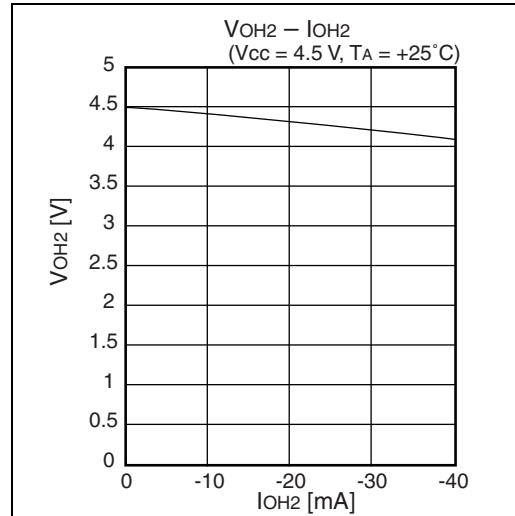
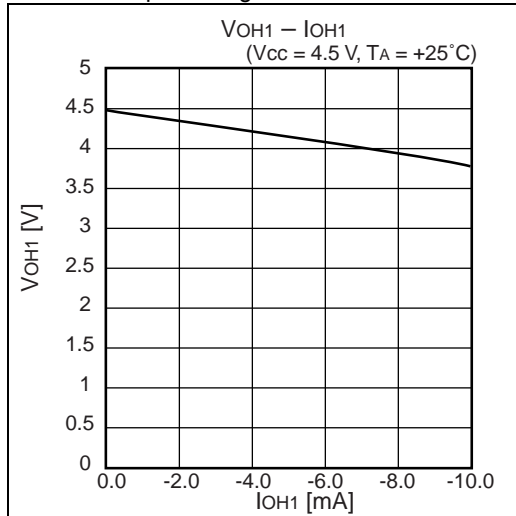
11.8 Flash memory

■ Erase and programming performance

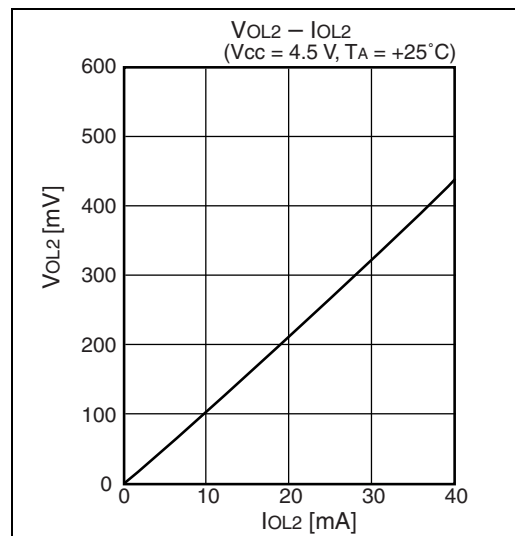
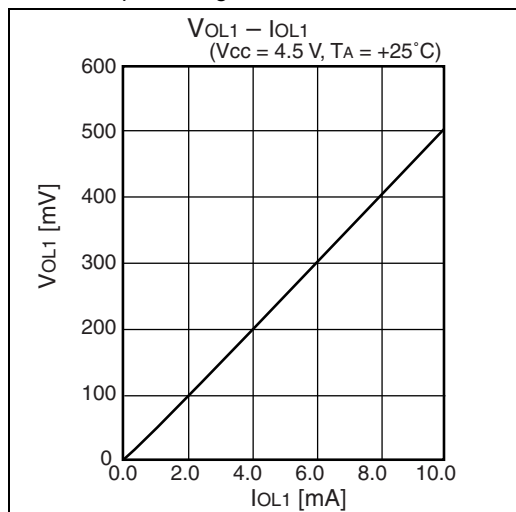
Parameter	Condition	Value			Unit	Remarks	
		Min	Typ	Max			
Sector erase time	$T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$	—	1	15	s	MB90F598G	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	MB90F598G	Excludes 00H programming prior
Word (16-bit) programming time		—	16	3600	μs	MB90F598G	Excludes system-level overhead
Erase/Program cycle	—	10000	—	—	cycle		

12. Example Characteristics

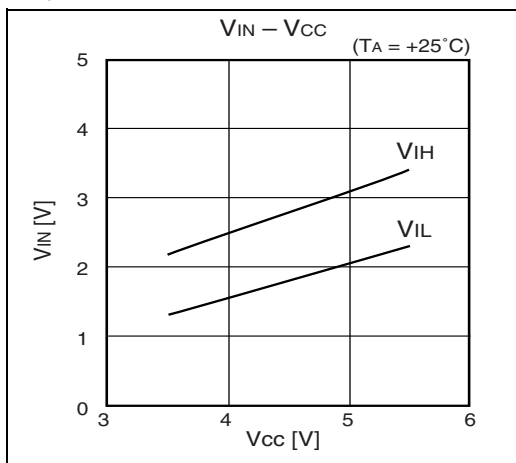
■ H⁺ Level Output Voltage



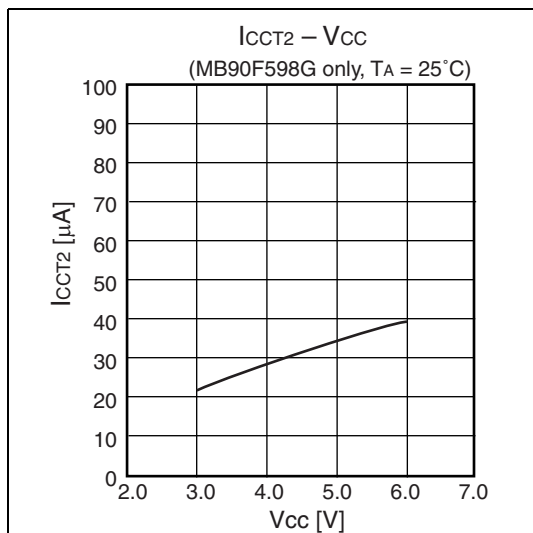
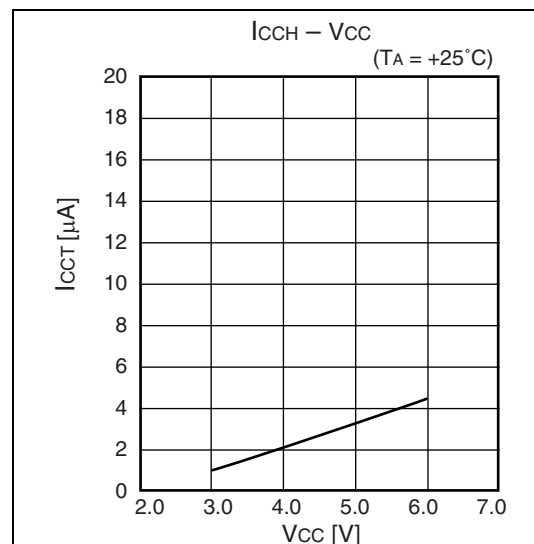
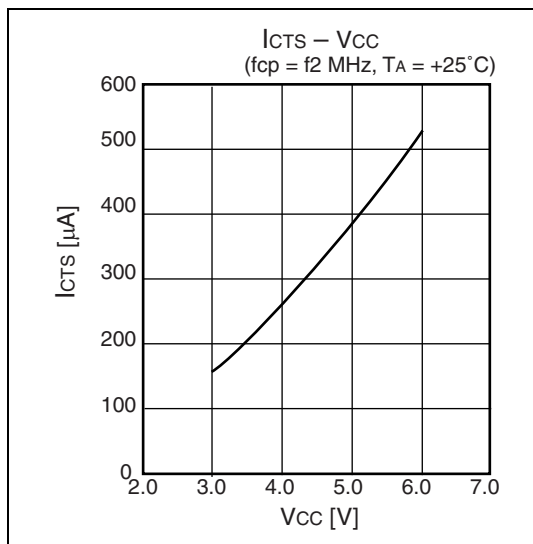
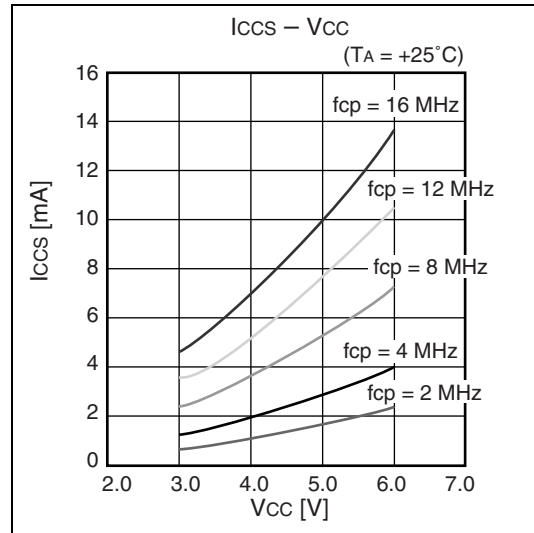
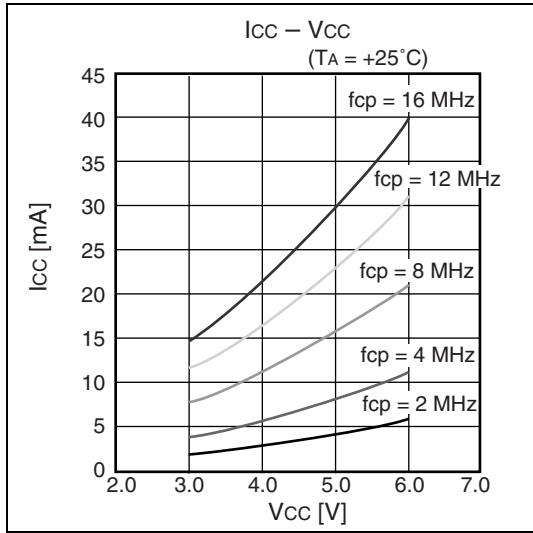
■ L⁻ Level Input Voltage



■ H⁺ Level Input Voltage/L⁻ Level Input Voltage (Hysteresis Input)



Supply Current

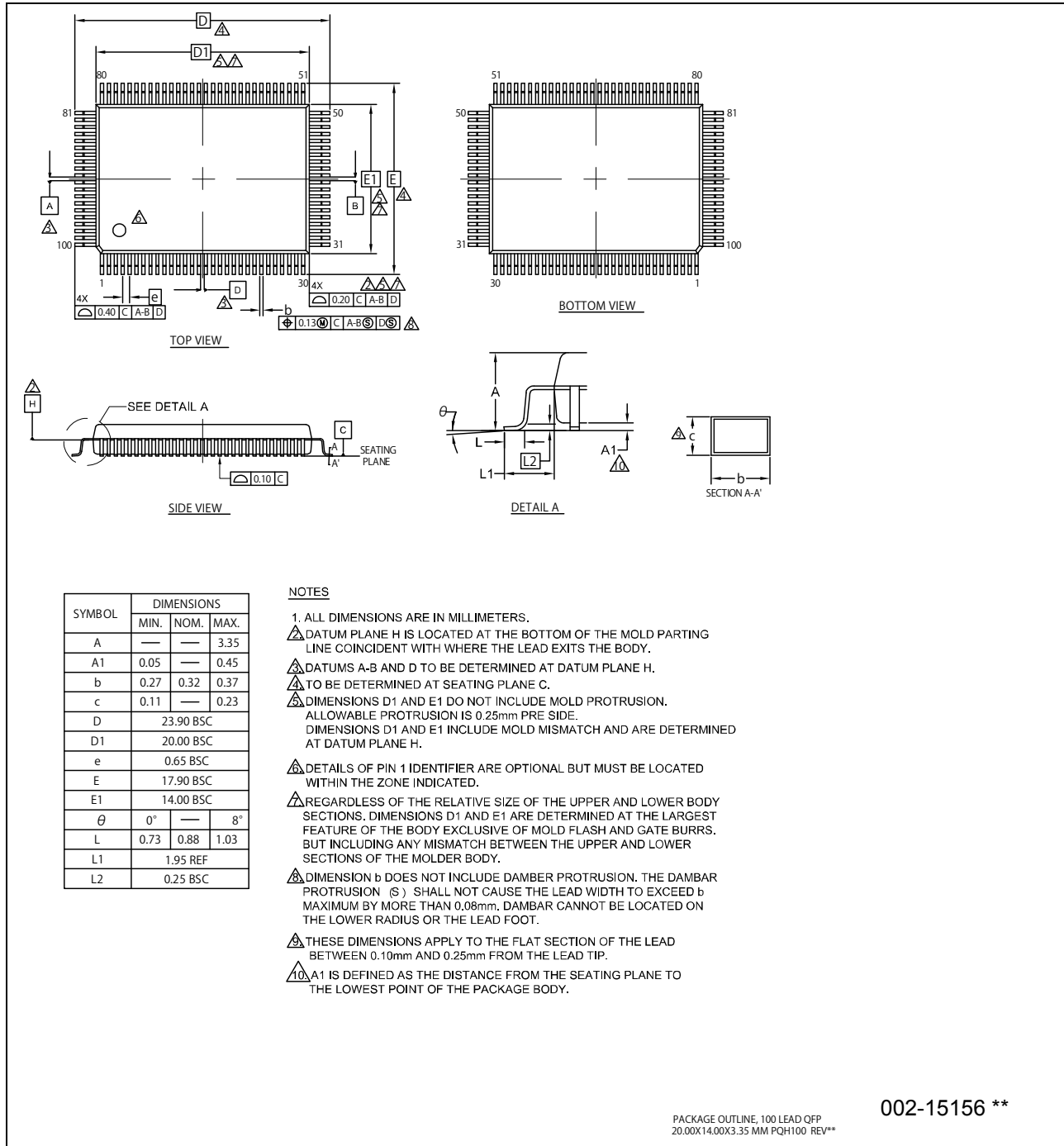


13. Ordering Information

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (PQH100)	
MB90V595GCR	256-pin Ceramic PGA	For evaluation

14. Package Dimensions

Package Type	Package Code
QFP 100	PQH100



15. Major Changes

Spancion Publication Number: DS07-13705-7E

Section	Change Results
—	Deleted the old products, MB90598, MB90F598, and MB90V595.
—	Changed the series name: MB90595/595G series ? MB90595G series
—	Changed the following erroneous name. I/O timer → 16-bit Free-run Timer
PRODUCT LINEUP	One of Standby mode name is changed. Clock mode → Watch mode
I/O CIRCUIT TYPE	Changed Pull-down resistor value of circuit type H.
ELECTRICAL CHARACTERISTICS AC Characteristics	Add the “External clock input” and “Flash Read cycle time” in (1) Clock Timing Figure in (2) Reset and Hardware Standby Input RST/HST input level of “In Stop Mode” is changed. 0.6 V _{CC} 0.2 V _{CC}
ELECTRICAL CHARACTERISTICS 5. A/D Converter	Changed the items of “Zero transition voltage” and “Full scale transition voltage”.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90598G/F598G/V595G F ² MC-16LX MB90595G Series CMOS 16-bit Proprietary Microcontroller Document Number: 002-07700				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	09/26/2008	Migrated to Cypress and assigned document number 002-07700. No change to document contents or format.
*A	5537128	AKIH	11/30/2016	Updated to Cypress template
*B	6059031	TORS	02/06/2018	Adapted new Cypress logo Updated following package code FPT-100P-M06 → PQH100

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