# SM560

# Spread Spectrum Clock Generator

## Features

- 25- to 108-MHz operating frequency range
- Wide (9) range of spread selections
- Accepts clock and crystal inputs
- Low power dissipation
- 3.3V = 85 mw (50 MHz)
- Frequency Spread disable function
- Center Spread modulation
- Low cycle-to cycle jitter
- Eight-pin SOIC package

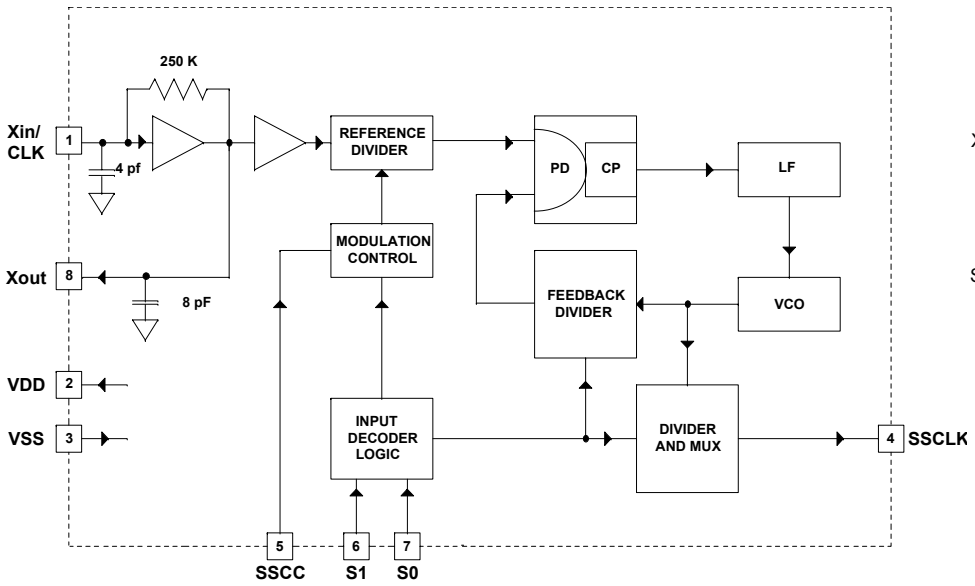
## Applications

- VGA controllers
- LCD panels and monitors
- Printers and multi-function devices (MFP)

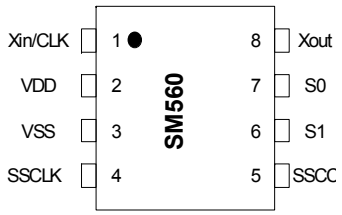
## Benefits

- Peak electromagnetic interference (EMI) reduction by 8 to 16 dB
- Fast time to market
- Cost reduction

## Block Diagram




## Pin Configuration



## Pin Definitions

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | Xin/CLK | I | **Clock or Crystal connection input**. Refer to *Table 1* for input frequency range selection. |
| 2 | VDD | P | **Positive power supply**. |
| 3 | GND | P | **Power supply ground**. |
| 4 | SSCLK | O | **Modulated clock output**. |
| 5 | SSCC | I | **Spread Spectrum Clock Control (Enable/Disable) function**. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally. |
| 6 | S1 | I | **Tri-level Logic input control pin used to select frequency and bandwidth**. Frequency/bandwidth selection and Tri-level Logic programming. See *Figure 1*. |
| 7 | S0 | I | **Tri-level Logic input control pin used to select frequency and bandwidth**. Frequency/bandwidth selection and Tri-level Logic programming. See *Figure 1*. |
| 8 | Xout | O | **Oscillator output pin connected to crystal**. Leave this pin unconnected If an external clock drives Xin/CLK. |

## Functional Description

The Cypress SM560 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital electronic systems.

The SM560 uses a Cypress-proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies of Clock (SSCLK1) is greatly reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading the system performance.

The SM560 is a very simple and versatile device to use. The frequency and spread% range is selected by programming S0 and S1digital inputs. These inputs use three (3) logic states including High (H), Low (L) and Middle (M) logic levels to select one of the nine available Frequency Modulation and Spread% ranges. Refer to *Table 1* for programming details.

The SM560 is optimized for SVGA (40 MHz) and XVGA (65 MHz) Controller clocks and also suitable for the applications with the frequency range of 25 to 108 MHz.

A wide range of digitally selectable spread percentages is made possible by using three-level (High, Low and Middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

Spread Spectrum Clock Control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

The SM560 is available in an eight-pin SOIC package with a 0 to 70°C operating temperature range.

**Table 1. Frequency and Spread% Selection (Center Spread)**

**25 – 54 MHz (Low Range)**

| Input Frequency (MHz) | S1=M S0=M (%) | S1=M S0=0 (%) | S1=1 S0=0 (%) | S1=0 S0=0 (%) | S1=0 S0=M (%) |
|---|---|---|---|---|---|
| 25 – 35 | 3.8 | 3.2 | 2.8 | 2.3 | 1.9 |
| 35 – 40 | 3.5 | 3.0 | 2.5 | 2.1 | 1.7 |
| 40 – 45 | 3.2 | 2.8 | 2.4 | 1.9 | 1.6 |
| 45 – 50 | 3.0 | 2.6 | 2.2 | 1.8 | 1.5 |
| 50 – 54 | 2.8 | 2.4 | 2.0 | 1.7 | 1.4 |

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

**50 – 108 MHz (High Range)**

| Input Frequency (MHz) | S1=1 S0=M (%) | S1=0 S0=1 (%) | S1=1 S0=1 (%) | S1=M S0=1 (%) |
|---|---|---|---|---|
| 50 – 60 | 2.5 | 1.9 | 1.2 | 1.0 |
| 60 – 70 | 2.4 | 1.8 | 1.1 | 0.9 |
| 70 – 80 | 2.3 | 1.6 | 1.1 | 0.9 |
| 80 – 100 | 2.0 | 1.4 | 1.0 | 0.8 |
| 100 – 108 | 1.8 | 1.3 | 0.8 | 0.6 |

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

## Tri-level Logic

With binary logic, four states can be programmed with two control lines, whereas Tri-level Logic can program nine logic states using two control lines. Tri-level Logic in the SM560 is implemented by defining a third logic state in addition to the standard logic “1” and “0.” Pins 6 and 7 of the SM560 recognize a logic state by the voltage applied to the respective pin. These states are defined as “0” (Low), “M” (Middle), and “1” (One). Each of these states has a defined voltage range that is interpreted by the SM560 as a “0,” “M,” or “1” logic state. Refer to *Table 2* for voltage ranges for each logic state. By using two equal value resistors (typically 20K) the “M” state can be easily programmed. Pins 6 or 7 can be tied directly to ground or VDD for Logic “0” or “1” respectively.

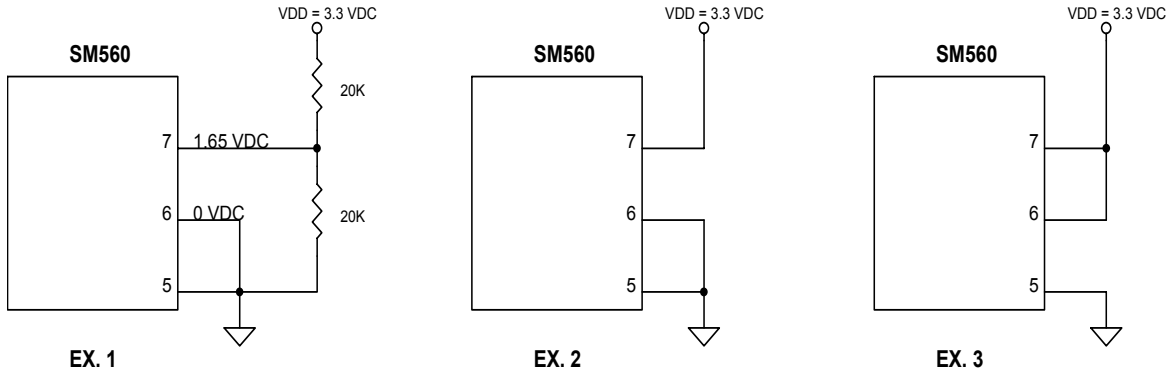



**Figure 1.**

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{DD}$): ..... –0.5V to +6.0V
DC Input Voltage: .....–0.5V to VDD + 0.5V
Junction Temperature .....–40°C to +140°C
Operating Temperature:..... 0°C to 70°C
Storage Temperature ..... –65°C to +150°C
Static Discharge Voltage (ESD)..... 2,000V-Min.

**Table 2. DC Electrical Characteristics:** $V_{DD}$ = 3.3V, Temp. = 25°C and $C_L$ (Pin 4) = 15 pF, unless otherwise noted

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Range | ±10% | 2.97 | 3.3 | 3.63 | V |
| $V_{INH}$ | Input High Voltage | S0 and S1 only | $0.85V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V |
| $V_{INM}$ | Input Middle Voltage | S0 and S1 only | $0.40V_{DD}$ | $0.50V_{DD}$ | $0.60V_{DD}$ | V |
| $V_{INL}$ | Input Low Voltage | S0 and S1 only | 0.0 | 0.0 | $0.15V_{DD}$ | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = 6 mA | 2.4 | | | V |
| $V_{OH2}$ | Output High Voltage | $I_{OH}$ = 20 mA | 2.0 | | | V |
| $V_{OL1}$ | Output Low Voltage | $I_{OH}$ = 6 mA | | | 0.4 | V |
| $V_{OL2}$ | Output Low Voltage | $I_{OH}$ = 20 mA | | | 1.2 | V |
| Cin1 | Input Capacitance | Xin/CLK (Pin 1) | 3 | 4 | 5 | pF |
| Cin2 | Input Capacitance | Xout (Pin 8) | 6 | 8 | 10 | pF |
| Cin2 | Input Capacitance | S0, S1, SSCC (Pins 7,6,5) | 3 | 4 | 5 | pF |
| $I_{DD1}$ | Power Supply Current | $F_{IN}$ = 40 MHz | | 30 | 40 | mA |
| $I_{DD2}$ | Power Supply Current | $F_{IN}$ = 65 MHz | | 35 | 45 | mA |

**Table 3. Electrical Timing Characteristics:** $V_{DD}$ = 3.3V, T = 25°C and $C_L$ = 15 pF, unless otherwise noted

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ICLKFR | Input Clock Frequency Range | $V_{DD}$ = 3.30V | 25 | | 108 | MHz |
| Trise | Clock Rise Time (Pin 4) | SSCLK1 @ 0.4 – 2.4V | 1.2 | 1.4 | 1.6 | ns |
| Tfall | Clock Fall Time (Pin 4) | SSCLK1 @ 0.4 – 2.4V | 1.2 | 1.4 | 1.6 | ns |
| DTYin | Input Clock Duty Cycle | XIN/CLK (Pin 1) | 20 | 50 | 80 | % |
| DTYout | Output Clock Duty Cycle | SSCLK1 (Pin 4) | 45 | 50 | 55 | % |
| JCC | Cycle-to-Cycle Jitter | Fin = 25 – 108 MHz | - | 125 | 175 | ps |

## SSCG Theory of Operation

The SM560 is a PLL-type clock generator using a proprietary Cypress design. By precisely controlling the bandwidth of the output clock, the SM560 becomes a Low EMI clock generator. The theory and detailed operation of the SM560 will be discussed in the following sections.

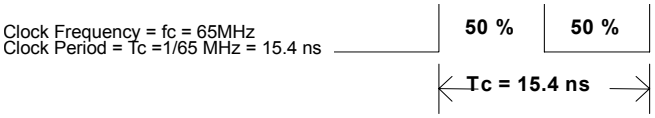
## EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of this 50/50-duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; third, fifth, seventh, etc. It is possible to reduce the amount of energy contained in the fundamental and odd harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for EMI. Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCBs, etc. The SM560 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

## SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The SM560 takes a narrow band digital reference clock in the range of 25–108 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 65-MHz clock with a 50% duty cycle. From a 65-MHz clock we know the following:

**Note:**
1. **Single Power Supply:** The Voltage on any input or I/O pin cannot exceed the power pin during power up.




If this clock is applied to the Xin/CLK pin of the SM560, the output clock at pin 4 (SSCLK) will be sweeping back and forth between two frequencies. These two frequencies, F1 and F2, are used to calculate to total amount of spread or bandwidth applied to the reference clock at pin 1. As the clock is making the transition from f1 to f2, the amount of time and sweep waveform play a very important role in the amount of EMI reduction realized from an SSCG clock.

The modulation domain analyzer is used to visualize the sweep waveform and sweep period. The left side of *Figure 2* shows the modulation profile of a 65-MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. The right side of *Figure 2* is a scan of the same SSCG clock using a spectrum analyzer. In this scan you can see a 6.48-dB reduction in the peak RF energy when using the SSCG clock.

## Modulation Rate

Spectrum Spread Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the Modulation Rate, Tmr. Modulation Rates of SSCG clocks are generally referred to in terms of frequency or Fmod = 1/Tmod.

The input clock frequency, Fin, and the internal divider count, Cdiv, determine the Modulation Rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the part. The SM560 and SM561 have a fixed divider count, as listed below.

| Device | Cdiv | |
|---|---|---|
| SM560 | 1166 | (All Ranges) |
| SM561 | 2332 | (All Ranges) |

Example:

Device = SM560
Fin = 65 MHz
Range = S1 = 1, S0 = M

Then;
Modulation Rate = Fmod = 65 MHz/1166 = 55.8 kHz.

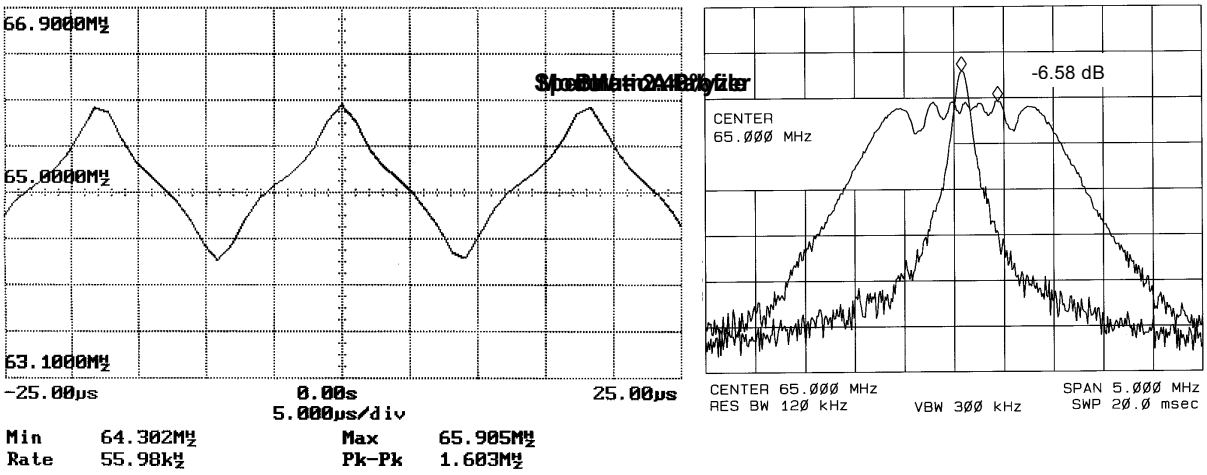



**Figure 2. SSCG Clock, SM560, Fin = 65 MHz**

## SM560 Application Schematic

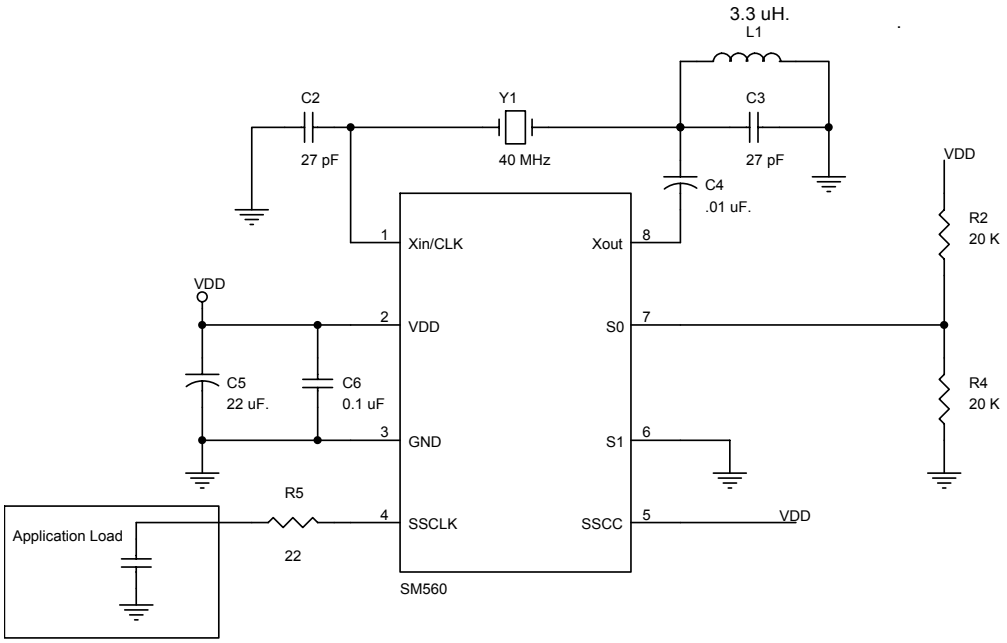



**Figure 3. Application Schematic**[2]

The schematic in *Figure 3* above demonstrates how the SM560 is configured in a typical application. This application is using a 40-MHz reference derived from a third overtone crystal connected to pins 1 and 8. Since Y1 is a third overtone crystal a notch filter is created with L1 and C3 to dampen the gain of the oscillator at the fundamental frequency of this crystal which is 13.33 MHz.

*Figure 3* also demonstrates how to properly use the tri-level logic employed in the SM560. Notice that resistors R2 and R4 create a voltage divider that places $V_{DD}/2$ on pin 7 to satisfy the voltage requirement for an “M” state.

With this configuration, the SM560 will produce an SSCG clock that is at a center frequency of 40 MHz. Referring to *Table 2*, range “0, M” at 40 MHz will generate a modulation profile that has a 1.7% peak to peak spread.

## Ordering Information[3]

| Part Number | Package Type | Product Flow |
|---|---|---|
| IMISM560BZ | 8-pin SOIC | Commercial, 0° to 70°C |
| IMISM560BZT | 8-pin SOIC–Tape and Reel | Commercial, 0° to 70°C |
| **Lead Free Devices** | | |
| CYISM560BSXC | 8-pin SOIC | Commercial, 0° to 70°C |
| CYISM560BSXCT | 8-pin SOIC–Tape and Reel | Commercial, 0° to 70°C |

Marking: Example: IMI
SM560BS
Date Code, Lot#

**SM560 B S**

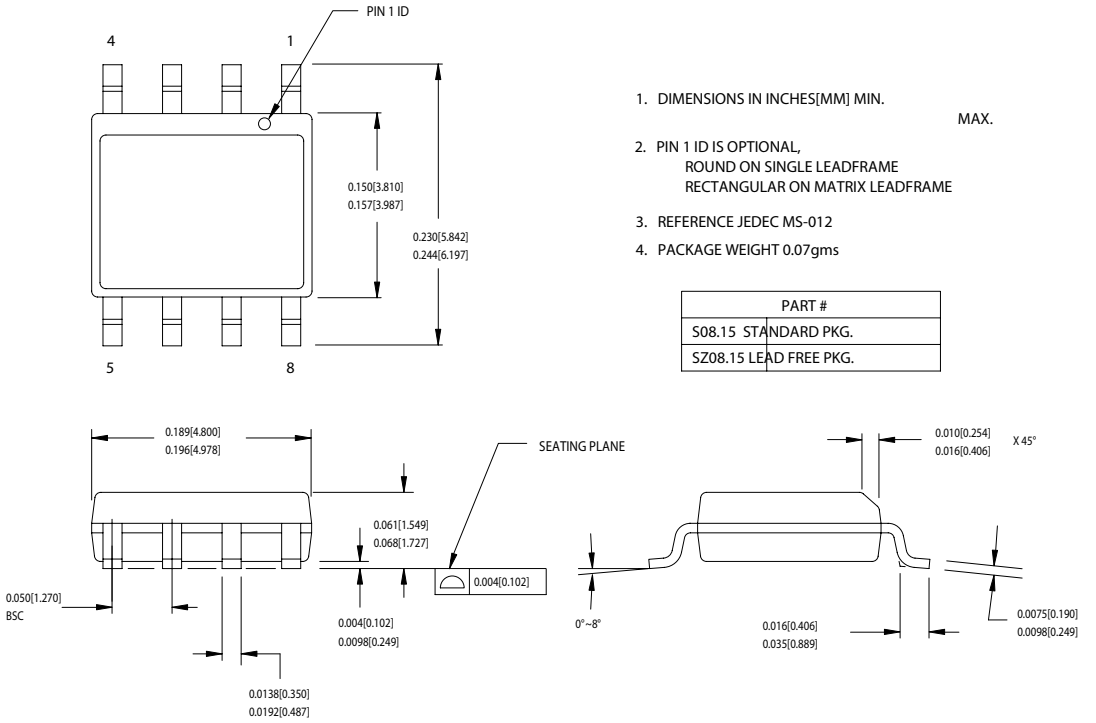
- Package S = SOIC
- Revision
- IMI Device Number

**Note:**

2. The value of L1 is calculated such that L1 and C3 are tuned to a frequency that is 130% higher than the fundamental frequency of the crystal.
   ZC1 = 1/2πfC
   ZC1 = 1/6.28 (17.33 MHz) (27 pF)
   ZC1 = 340Ω
   ZL1 = 2πFL
   L = ZL1/2πf
   L = 340/6.28(17.33 MHz)
   L = 3.12 μH
3. The ordering part number differs from the marking on the actual device.

## Package Drawing and Dimensions

### 8-lead (150-Mil) SOIC S8




1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

| PART # |
|---|
| S08.15 STANDARD PKG. |
| SZ08.15 LEAD FREE PKG. |

51-85066-*C

## Document History Page

| Document Title: SM560 Spread Spectrum Clock Generator<br>Document Number: 38-07020 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 106948 | 06/07/01 | IKA | Convert from IMI to Cypress |
| *A | 113520 | 04/10/02 | DMG | Package suffix changed (per Cypress standard) |
| *B | 119445 | 10/16/02 | RGL | Corrected the values in the Absolute Maximum Ratings to match the device. |
| *C | 122675 | 12/14/02 | RBI | Added power up requirements to operating conditions information. |
| *D | 231055 | See ECN | RGL | Added Lead Free Devices |
| *E | 237630 | See ECN | RGL | Minor Change: Added letter C in the ordering for Lead Free |

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