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EZ-PD CCG4

USB Type-C Port Controller

General Description

EZ-PD™ CCG4 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG4 provides a complete dual USB Type-C and USB-Power Delivery port control solution for notebooks, power adapters and docking stations. It can also be used in dual role and downstream facing port applications. EZ-PD CCG4 uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz Arm® Cortex®-M0 processor with 128 KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors R_P and R_D.

Applications

- Notebooks
- Power adapters
- Docking stations

Features

32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0 CPU
- 128-KB Flash
- 8-KB SRAM

Integrated Digital Blocks

- Up to four integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time serial communication blocks (SCBs) with re-configurable I^2C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Type-C and USB-PD Support

- Integrated USB Power Delivery 3.0 support (only PD 2.0 support for 33-ball CSP part)
- Two integrated USB-PD BMC transceivers
- Integrated UFP[1] (R_D) and current sources for DFP[2] (R_P) on both Type-C ports
- Integrated dead battery termination for DRP (Power Source/Sink) applications
- Supports two USB Type-C ports
- Integrated VCONN FETs to power EMCA cables
- Integrated fast role swap and extended data messaging (not supported for 33-ball CSP part)

Low-Power Operation

- 2.7-V to 5.5-V operation
- Independent supply voltage pin for GPIO that allows 1.71-V to 5.5-V signaling on the I/Os
- Reset: 1.0 µA, Deep Sleep: 2.5 µA, Sleep: 2.5 mA

System-Level ESD on CC Pins

- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C (on 40-pin QFN and 33-ball CSP only)

Hot Swappable I/Os

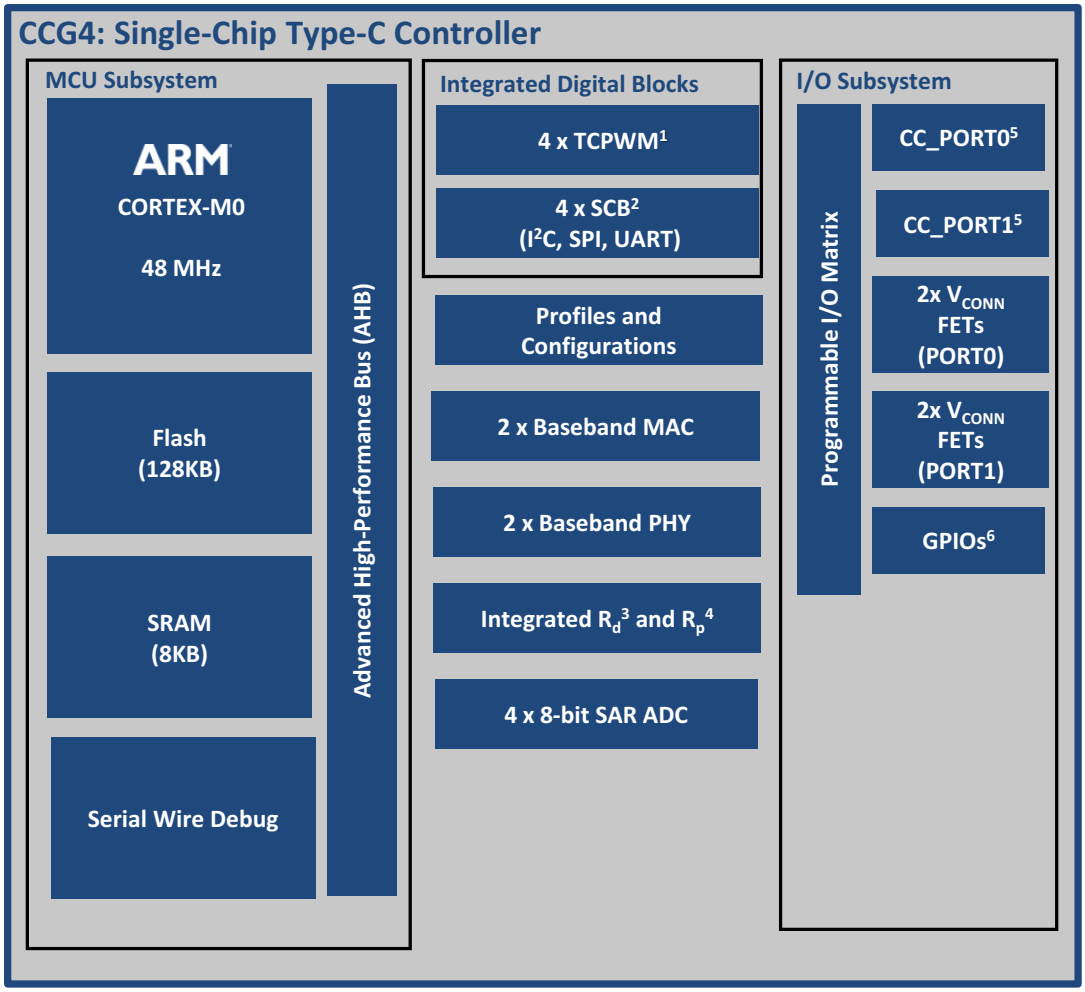
- Port 0 I^2C pins and CC1, CC2 pins are hot-swappable

Packages

- 4.0 mm × 4.0 mm, 0.5 mm, 24-pin QFN
- 6.0 mm × 6.0 mm, 0.6 mm, 40-pin QFN
- 2.4 mm x 2.5 mm, 0.5 mm, 33-ball CSP
- Supports extended industrial temperature range (–40 °C to +105 °C)

Notes
1. UFP refers to Power Sink.
2. DFP refers to Power Source.

Logic Block Diagram



1. Timer, counter, pulse width modulation block
2. Serial communication block configurable as UART, SPI, or I²C
3. Termination resistor denoting a UFP
4. Current sources to indicate a DFP
5. Configuration channel
6. General purpose input/output

Contents

Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

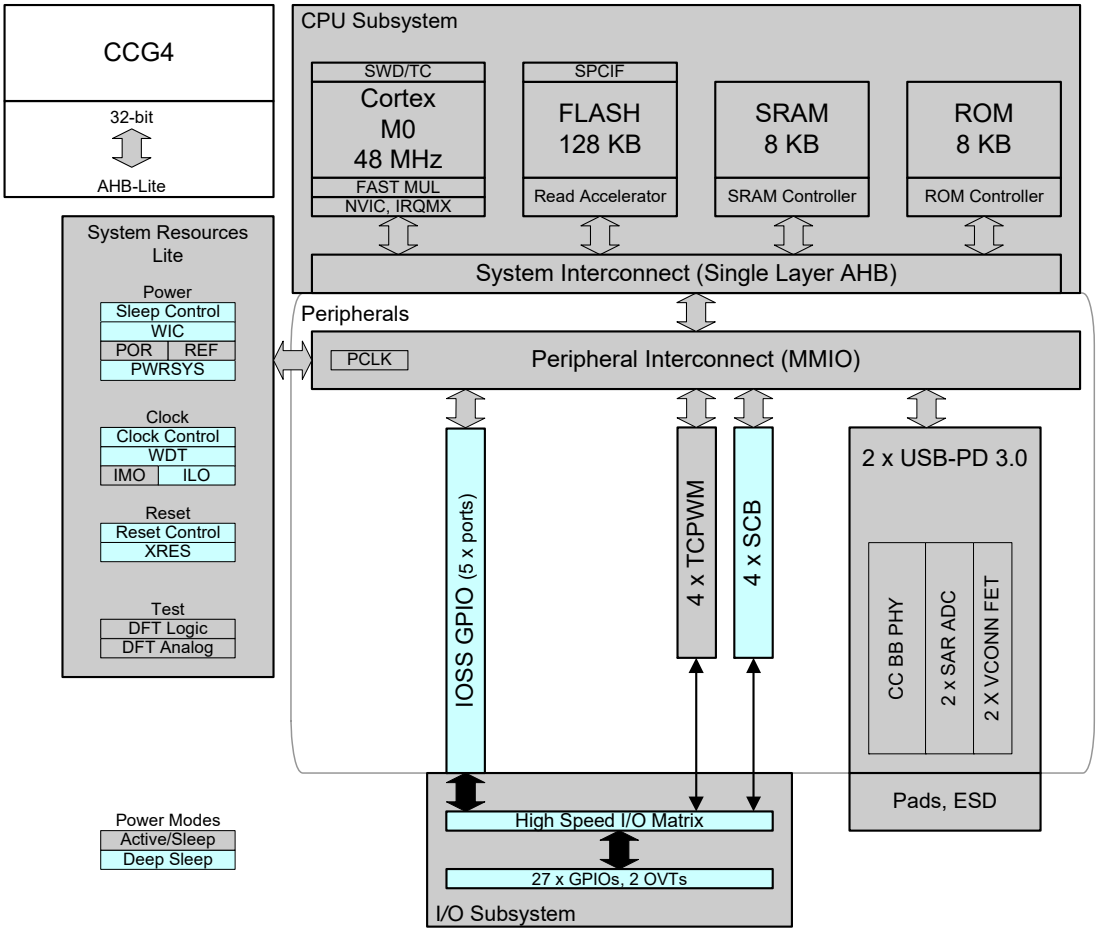
The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility

EZ-PD CCG4 Block Diagram

Figure 1. EZ-PD CCG4 Block Diagram



Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG4 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a nonmaskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG4 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG4 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait-states (WS) access time at 48 MHz and with 0-WS access time at 16 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

EZ-PD CCG4 has two USB-PD subsystems consisting of USB Type-C baseband transceivers and physical-layer logic. These transceivers perform the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V analog front end. This subsystem integrates the required termination resistors to identify the role of the EZ-PD CCG4 solution. R_D is used to identify EZ-PD CCG4 as a UFP in a DRP application. When configured as a DFP, integrated current sources perform the role of R_P or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the USB Type-C spec. EZ-PD CCG4 responds to all USB-PD communication.

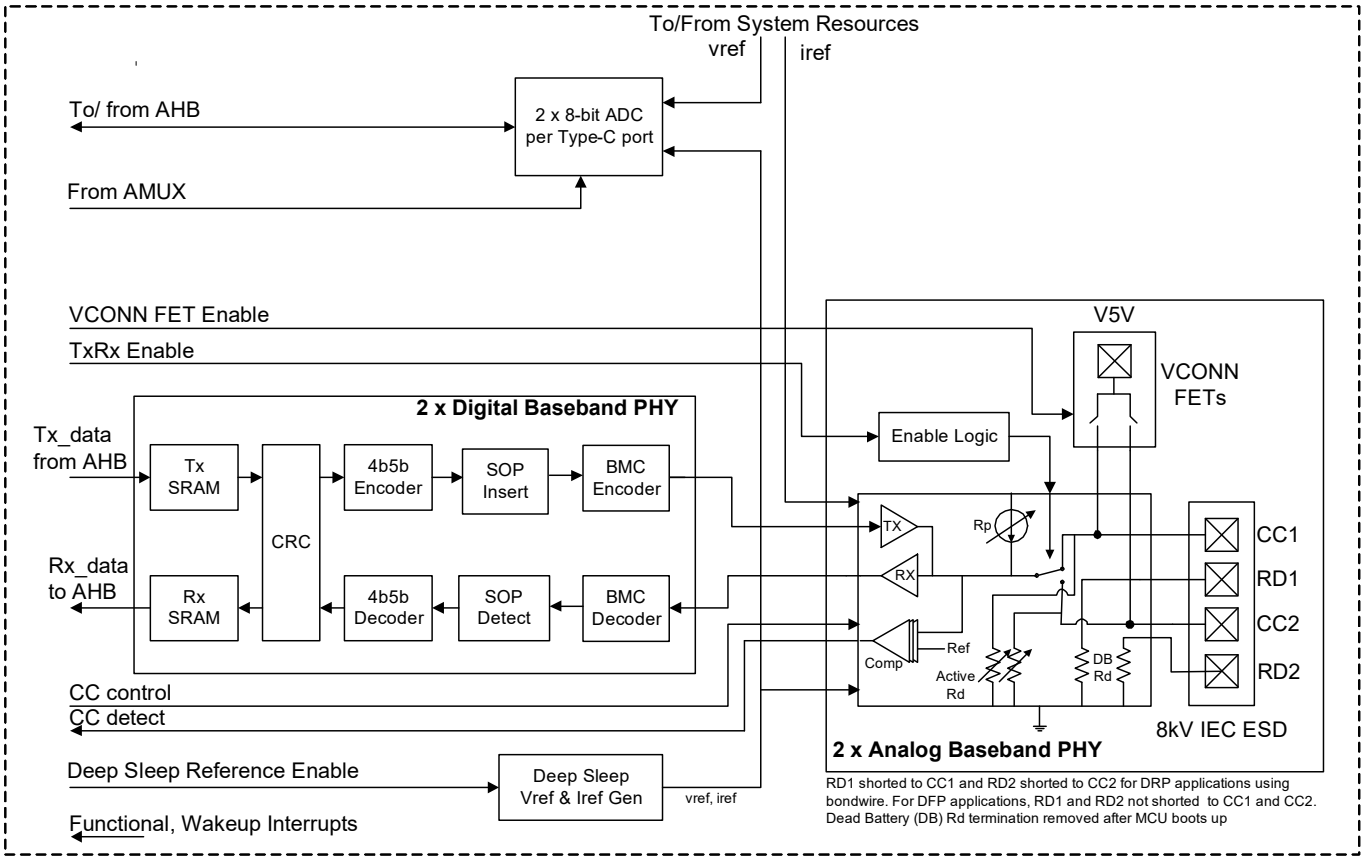
The USB-PD sub-system contains two 8-bit SAR (successive approximation register) ADCs for analog to digital conversions. The ADCs include an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global analog multiplex busses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use. The CC1 and CC2 pins of both Type-C ports are not available to connect to the mux busses.

To support the latest USB-PD 3.0 specification, CCG4 has implemented the fast role swap feature. Fast Role Swap enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. For more details, refer to Section 6.3.17 (FR_Swap Message) in the USB-PD 3.0 specification.

CCG4 is designed to be fully interoperable with revision 3.0 of the USB Power Delivery specification as well as revision 2.0 of the USB Power Delivery specification.

CCG4 supports Extended Messages containing data of up to 260 bytes. The Extended Messages will be larger than expected by the USB-PD 2.0 hardware. To accommodate Revision 2.0 based systems, a Chunking mechanism is implemented such that Messages are limited to Revision 2.0 sizes unless it is discovered that both systems support the longer Message lengths.

Figure 2. USB-PD Subsystem



System Resources

Power System

The power system is described in detail in the section Power on page 18. It provides the assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). EZ-PD CCG4 can operate from three different power sources over the range of 2.7 to 5.5 V and has three different power modes, transitions between which are managed by the power system. EZ-PD CCG4 provides Sleep and Deep Sleep low-power modes.

Clock System

The clock system for EZ-PD CCG4 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO).

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG4 has four SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as a master or a slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG4 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1, SCB 2 and SCB 3 blocks of EZ-PD CCG4 are not completely compliant with the I^2C spec in the following:

- The GPIO cells for SCB 1 to SCB 3 I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG4 has up to four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG4 has 30 GPIOs that includes the I^2C and SWD pins, which can also be used as GPIOs. The I^2C pins from only SCB 0 are overvoltage-tolerant. The number of available GPIOs vary with the part numbers. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

Table 1. Pinout for CYPD4225-40LQXIT, CYPD4226-40LQXIT, and CYPD4236-40LQXIT

Group	Pin Name	Pin Number	ESD Protection	Description
USB Type-C Port 0	CC1_P0	9	HBM, IEC	USB PD connector detect/Configuration Channel 1
	CC2_P0	7	HBM, IEC	USB PD connector detect/Configuration Channel 2
USB Type-C Port 1	CC1_P1	22	HBM, IEC	USB PD connector detect/Configuration Channel 1
	CC2_P1	24	HBM, IEC	USB PD connector detect/Configuration Channel 2
VBUS Control	VBUS_P_CTRL_P0/P1.6	11	HBM	Full rail control I/O for enabling/disabling Provider load FET of USB Type-C port 0
	VBUS_C_CTRL_P0/P1.7	12	HBM	Full rail control I/O for enabling/disabling Consumer load FET of USB Type-C port 0/SCB0 (see Table 3 on page 14 through Table 6 on page 14)
	VBUS_P_CTRL_P1/P4.2	39	HBM	Full rail control I/O for enabling/disabling Provider load FET of USB Type-C port 1
	VBUS_C_CTRL_P1/P4.1	38	HBM	Full rail control I/O for enabling/disabling Consumer load FET of USB Type-C port 1
	VBUS_DISCHARGE_P0/ P2.5	20	HBM	I/O used for discharging VBUS line during voltage change
	VBUS_DISCHARGE_P1/ P4.3	40	HBM	I/O used for discharging VBUS line during voltage change
VCONN Control	VCONN_MON_P0/P2.4	19	HBM	VCONN_MON_P0 (Monitor VCONN for UVP condition on port 0)/GPIO
	SCL_2/VCONN_MON_P1/ P2.7	25	HBM	SCB2 (see Table 3 on page 14 through Table 6 on page 14) or VCONN_MON_P1(Monitor VCONN for UVP condition on port 1)
Over-voltage Protection (OVP)	OVP_TRIP_P0/P2.1	14	HBM	VBUS overvoltage output indicator for port 0 (active LOW)
	OVP_TRIP_P1/P3.0	21	HBM	VBUS overvoltage output indicator for port 1 (active LOW)
GPIOs and Serial Interfaces	VBUS_MON_P0/P2.0	13	HBM	VBUS_MON_P0 (VBUS overvoltage protection monitoring signal)/GPIO
	HPD_P0/P2.3	18	HBM	HPD_P0 (Hot Plug Detect I/O for port 0)/GPIO
	HPD_P1/P3.4	30	HBM	HPD_P1 (Hot Plug Detect I/O for port 1)/GPIO
	MUX_CTRL_3_P1/ OCP_DET_P1/P3.5	34	HBM	MUX_CTRL_3_P1 (Mux control for port 1) or VBUS Overcurrent Protection Input for port 1 (active LOW)
	MUX_CTRL_2_P1/P3.6	35	HBM	MUX_CTRL_2_P1 (Mux control for port 1)/SCB3 (see Table 3 on page 14 through Table 6 on page 14)
	MUX_CTRL_1_P1/P3.7	36	HBM	MUX_CTRL_1_P1 (Mux control for port 2)/SCB3 (see Table 3 on page 14 through Table 6 on page 14)
	VBUS_MON_P1/P4.0	37	HBM	VBUS_MON_P1(VBUS overvoltage protection monitoring signal)
	VSEL_2_P1/P3.1	27	HBM	VSEL_2_P1(Voltage selection control for VBUS on port 1)/GPIO
	I2C_SCL_SCB0_EC/P0.1	17	HBM	SCB0/SCB3 (see Table 3 on page 14 through Table 6 on page 14)
	I2C_SDA_SCB0_EC/P0.0	16	HBM	SCB0/SCB2 (see Table 3 on page 14 through Table 6 on page 14)
	I2C_INT_EC/P2.2	15	HBM	I2C Interrupt line
	I2C_SCL_SCB1_AR/ VSEL_1_P1/P1.0	4	HBM	SCB1 (see Table 3 on page 14 through Table 6 on page 14) or VSEL_1_P1 (Voltage selection control for VBUS on port 1)

Table 1. Pinout for CYPD4225-40LQXIT, CYPD4226-40LQXIT, and CYPD4236-40LQXIT *(continued)*

Group	Pin Name	Pin Number	ESD Protection	Description
GPIOs and Serial Interfaces	I2C_SDA_SCB1_AR/ VSEL_1_P0/P1.3	3	HBM	SCB0/SCB1 (see Table 3 on page 14 through Table 6 on page 14) or VSEL_1_P0 (Voltage selection control for VBUS on port 0)
	I2C_INT_AR_P0/ OCP_DET_P0/P1.4	5	HBM	I2C interrupt line or VBUS Overcurrent Protection Input for port 0 (active LOW)
	I2C_INT_AR_P1/P1.5	6	HBM	I2C interrupt line/SCB0/SCB1 (see Table 3 on page 14 through Table 6 on page 14)
	SDA_2/MUX_C-TRL_3_P0/VSEL_2_P0/P2.6	26	HBM	SCB2 (see Table 3 on page 14 through Table 6 on page 14) or MUX_CTRL_3_P1 (Mux control for port 0) or VSEL_2_P0 (Voltage selection control for VBUS on port 0)
	SCL_3/MUX_C-TRL_1_P0/P3.3	29	HBM	SCB3 (see Table 3 on page 14 through Table 6 on page 14) /MUX_CTRL_1_P0 (Mux control for port 0)
	SDA_3/MUX_C-TRL_2_P0/P3.2	28	HBM	SCB3 (see Table 3 on page 14 through Table 6 on page 14) /MUX_CTRL_2_P0 (Mux control for port 0)
	SWD_IO/AR_RST#/P1.1	1	HBM	SWD_IO (serial wire debug I/O)/SCB0. See Table 3 on page 14 through Table 6 on page 14.
	SWD_CLK/I2C_CFG_EC/ P1.2	2	HBM	SWD Clock/I2C_CFG_EC
Reset	XRES[3]	10	HBM	Reset input (active LOW)
Power	V5V_P0	8	HBM	2.7-V to 5.5-V supply for VCONN FET of Type-C port 0
	V5V_P1	23	HBM	2.7-V to 5.5-V supply for VCONN FET of Type-C port 1
	VDDIO	32	HBM	1.71-V to 5.5-V supply for I/Os
	VCCD	33	HBM	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDD	31	HBM	VDDD supply input/output (2.7 V to 5.5 V)
	VSS	EPAD	HBM	Ground supply

Note
3. This is firmware configurable GPIO. By default, this pin is floating. Firmware can add pull-up/pull-down and enable/disable I/O buffers.

Figure 3. 40-pin QFN Pin Map (Top View) for CYPD4225-40LQXIT, CYPD4226-40LQXIT, and CYPD4236-40LQXIT

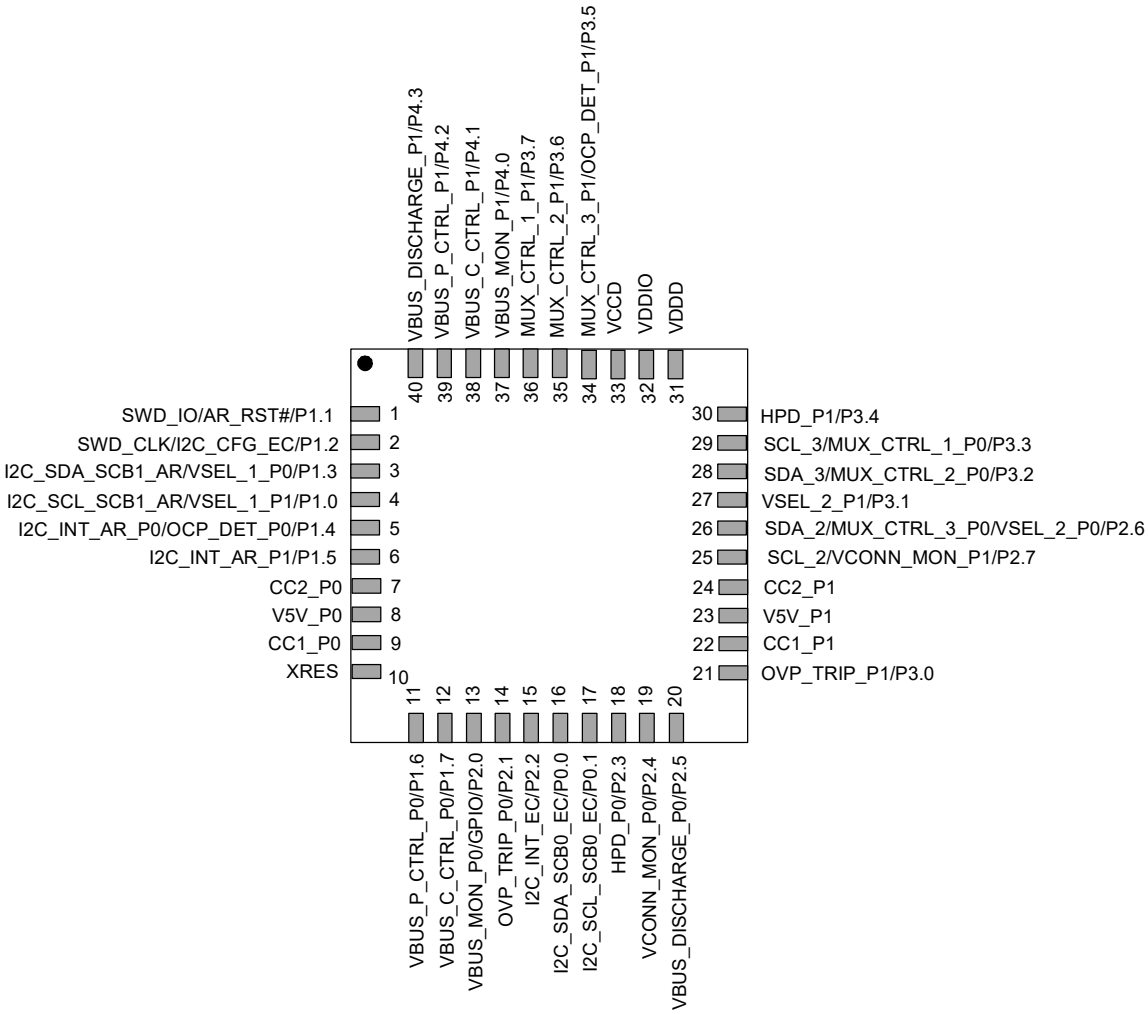


Table 2. Pinout for CYPD4125-40LQXIT and CYPD4126-40LQXIT

Group	Pin Name	Pin Number	ESD Protection	Description
USB Type-C Port 0	CC1_P0	9	HBM, IEC	USB PD connector detect/Configuration Channel 1
	CC2_P0	7	HBM, IEC	USB PD connector detect/Configuration Channel 2
VBUS Control	VBUS_P_CTRL_P0/P1.6	11	HBM	Full rail control I/O for enabling/disabling. Provider load FET of USB Type-C port 0.
	VBUS_C_CTRL_P0/P1.7	12	HBM	Full rail control I/O for enabling/disabling. Consumer load FET of USB Type-C port 0/SCB0 (see Table 3 on page 14 through Table 6 on page 14).
	VBUS_DIS-CHARGE_P0/P2.5	20	HBM	I/O used for discharging VBUS line during voltage change
VCONN Control	VCONN_MON_P0/P2.4	19	HBM	VCONN_MON_P0 (Monitor VCONN for OVP condition on port 0)/GPIO
Over-voltage Protection (OVP)	OVP_TRIP_P0/P2.1	14	HBM	VBUS overvoltage output indicator for port 0 (active LOW)
GPIOs and Serial Interfaces	P3.1	27	HBM	SCB2 (see Table 3 on page 14 through Table 6 on page 14)/GPIO
	VBUS_MON_P0/P2.0	13	HBM	VBUS_MON_P0 (VBUS overvoltage protection monitoring signal)/GPIO
	HPD_P0/P2.3	18	HBM	HPD_P0 (Hot Plug Detect I/O for port 0)/GPIO
	P3.0	21	HBM	GPIO
	P3.4	30	HBM	
	P3.5	34	HBM	
	P3.6	35	HBM	GPIO/SCB3 (see Table 3 on page 14 through Table 6 on page 14)
	P3.7	36	HBM	
	P4.0	37	HBM	GPIO
	P4.1	38	HBM	
	P4.2	39	HBM	
	P4.3	40	HBM	
	I2C_SCL_SCB0_EC/P0.1	17	HBM	SCB0/SCB3 (see Table 3 on page 14 through Table 6 on page 14)
	I2C_SDA_SCB0_EC/ P0.0	16	HBM	SCB0/SCB2 (see Table 3 on page 14 through Table 6 on page 14)
	I2C_INT_EC/P2.2	15	HBM	I2C interrupt line
	I2C_SCL_SCB1_AR/P1.0	4	HBM	SCB1 (see Table 3 on page 14 through Table 6 on page 14)
	I2C_SDA_SCB1_AR/ VSEL_1_P0/P1.3	3	HBM	SCB0 or SCB1 (see Table 3 on page 14 through Table 6 on page 14) or voltage selection control for VBUS on port 0
	I2C_INT_AR_P0/ OCP_DET_P0/P1.4	5	HBM	I2C interrupt line or VBUS Overcurrent Protection Input for port 0 (Active LOW)
	P1.5	6	HBM	GPIO/SCB0/SCB1 (see Table 3 on page 14 through Table 6 on page 14)
	SCL_2/P2.7	25	HBM	GPIO/SCB2 (see Table 3 through Table 6)
	SDA_2/ MUX_CTRL_3_P0/ VSEL_2_P0/P2.6	26	HBM	SCB2 (see Table 3 on page 14 through Table 6 on page 14) or MUX_CTRL_3_P0 (Mux control for port 0), or Voltage selection control for VBUS on port 0

Table 2. Pinout for CYPD4125-40LQXIT and CYPD4126-40LQXIT *(continued)*

Group	Pin Name	Pin Number	ESD Protection	Description
GPIOs and Serial Interfaces	SCL_3/ MUX_CTRL_1_P0/P3.3	29	HBM	SCB3 (see Table 3 on page 14 through Table 6 on page 14) or MUX_CTRL_1_P0 (Mux control for port 0)
	SDA_3/ MUX_CTRL_2_P0/P3.2	28	HBM	SCB3 (see Table 3 on page 14 through Table 6 on page 14) or MUX_CTRL_2_P0 (Mux control for port 0)
	SWD_IO/AR_RST#/P1.1	1	HBM	Serial wire debug I/O (SWD IO)/SCB0. See Table 3 on page 14 through Table 6 on page 14 or Alpine Ridge Reset.
	SWD_CLK/I2C_CFG_EC/ P1.2	2	HBM	SWD Clock/I2C_CFG_EC
Reset	XRES[4]	10	HBM	Reset input (active LOW)
Power	V5V_P0	8	HBM	2.7-V to 5.5-V supply for VCONN FET of Type-C port 0
	VDDIO	32	HBM	1.71-V to 5.5-V supply for I/Os
	VCCD	33	HBM	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDD	31	HBM	VDDD supply I/O (2.7 V to 5.5 V)
	VSS	EPAD	HBM	Ground supply
No Connect	NC	22	-	These pins are not bonded
	NC	23	-	
	NC	24	-	

Note
4. This is firmware configurable GPIO. By default, this pin is floating. Firmware can add pull-up/pull-down and enable/disable IO buffers.

Figure 4. 40-pin QFN Pin Map (Top View) for CYPD4125-40LQXIT and CYPD4126-40LQXIT

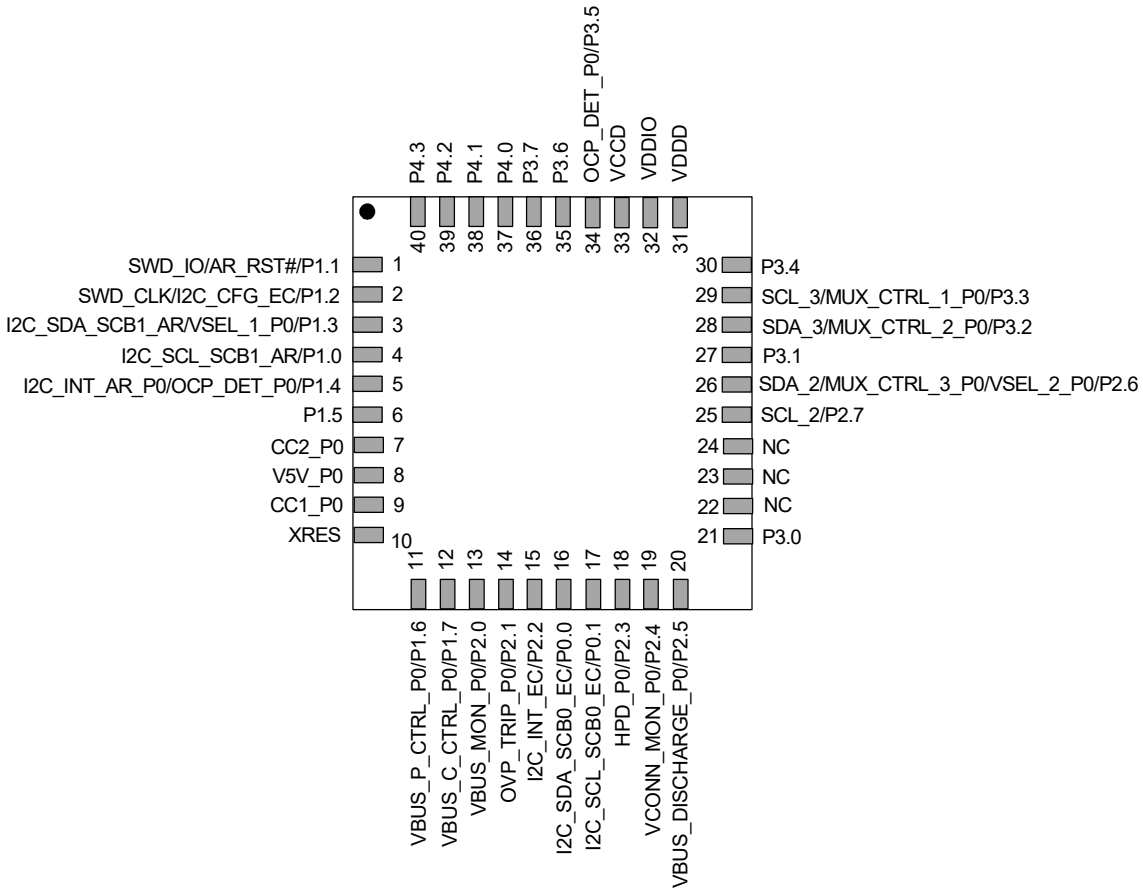


Table 3. Serial Communication Block (SCB0) Configuration

GPIO	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
P1.7	UART_TX_SCB0	SPI_MOSI_SCB0	SPI_MOSI_SCB0	VBUS_C_CTRL_P0	VBUS_C_CTRL_P0
P2.1	UART_RX_SCB0	SPI_CLK_SCB0	SPI_CLK_SCB0	VSEL_2_P0/ VCONN_MON_P0	VSEL_2_P0/ VCONN_MON_P0
P0.1	UART_RTS_SCB0	SPI_MISO_SCB0	SPI_MISO_SCB0	I2C_SDA_SCB0	I2C_SDA_SCB0
P0.0	UART_CTS_SCB0	SPI_SEL_SCB0	SPI_SEL_SCB0	I2C_SCL_SCB0	I2C_SCL_SCB0

Table 4. Serial Communication Block (SCB1) Configuration

GPIO	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
P1.0	UART_TX_SCB1	SPI_CLK_SCB1	SPI_CLK_SCB1	I2C_SCL_SCB1	I2C_SCL_SCB1
P1.3	UART_RX_SCB1	SPI_MISO_SCB1	SPI_MISO_SCB1	I2C_SDA_SCB1	I2C_SDA_SCB1
P1.5	UART_RTS_SCB1	SPI_SEL_SCB1	SPI_SEL_SCB1	GPIO	GPIO
P1.1	UART_CTS_SCB1	SPI_MOSI_SCB1	SPI_MOSI_SCB1	SWD_IO	SWD_IO

Table 5. Serial Communication Block (SCB2) Configuration

GPIO	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
P2.6	UART_TX_SCB2	SPI_MISO_SCB2	SPI_MISO_SCB1	I2C_SDA_SCB2	I2C_SDA_SCB2
P2.7	UART_RX_SCB2	SPI_MOSI_SCB2	SPI_MOSI_SCB2	I2C_SCL_SCB2	I2C_SCL_SCB2
P0.0	UART_RTS_SCB2	SPI_SEL_SCB2	SPI_SEL_SCB2	I2C_SCL_SCB0	I2C_SCL_SCB0
P3.0	UART_CTS_SCB2	SPI_CLK_SCB2	SPI_CLK_SCB2	AR_RST#	AR_RST#

Table 6. Serial Communication Block (SCB3) Configuration

GPIO	UART	SPI Master	SPI Slave	I2C Master	I2C Slave
P3.2	UART_TX_SCB3	SPI_MOSI_SCB3	SPI_MOSI_SCB3	I2C_SDA_SCB3	I2C_SDA_SCB3
P3.3	UART_RX_SCB3	SPI_MISO_SCB3	SPI_MISO_SCB3	I2C_SCL_SCB3	I2C_SCL_SCB3
P3.7	UART_RTS_SCB3	SPI_SEL_SCB3	SPI_SEL_SCB3	GPIO	GPIO
P3.6	UART_CTS_SCB3	SPI_CLK_SCB3	SPI_CLK_SCB3	GPIO	GPIO

Table 7. Pin List for CYPD4126-24LQXIT and CYPD4136-24LQXIT

Pin Name	Pin Number	ESD Protection	Description
P1.2	1	HBM	GPIO/SWD_CLK
P1.3	2	HBM	GPIO
P1.5	3	HBM	GPIO
CC2	4	HBM	Configuration Channel 2
V5V	5	HBM	2.7-V to 5.5-V supply for VCONN FET of Type-C
CC1	6	HBM	Configuration Channel 1
XRES	7	HBM	Reset input (active LOW)
P1.7	8	HBM	GPIO
P0.0	9	HBM	SCB0_I2C_SDA
P0.1	10	HBM	SCB0_I2C_SCL
P2.3	11	HBM	HotPlug_Detect
P2.5	12	HBM	GPIO/VBUS_DISCHARGE
P3.0	13	HBM	GPIO
P2.6	14	HBM	GPIO
P3.1	15	HBM	GPIO
P3.2	16	HBM	SCB3_I2C_SDA
P3.3	17	HBM	SCB3_I2C_SCL
P3.4	18	HBM	GPIO
GND	19	HBM	Ground supply
VDDD	20	HBM	VDDD supply input/output (2.7 V to 5.5 V)
VDDIO	21	HBM	1.71-V to 5.5-V supply for I/Os
VCCD	22	HBM	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
P3.6	23	HBM	GPIO
P1.1	24	HBM	GPIO/SWD_DATA
VSS	25/EPAD	HBM	Ground supply

Figure 5. 24-pin QFN Pin Map for CYPD4126-24LQXIT and CYPD4136-24LQXIT

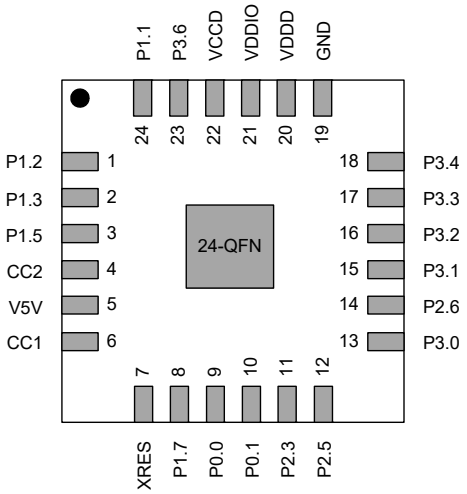
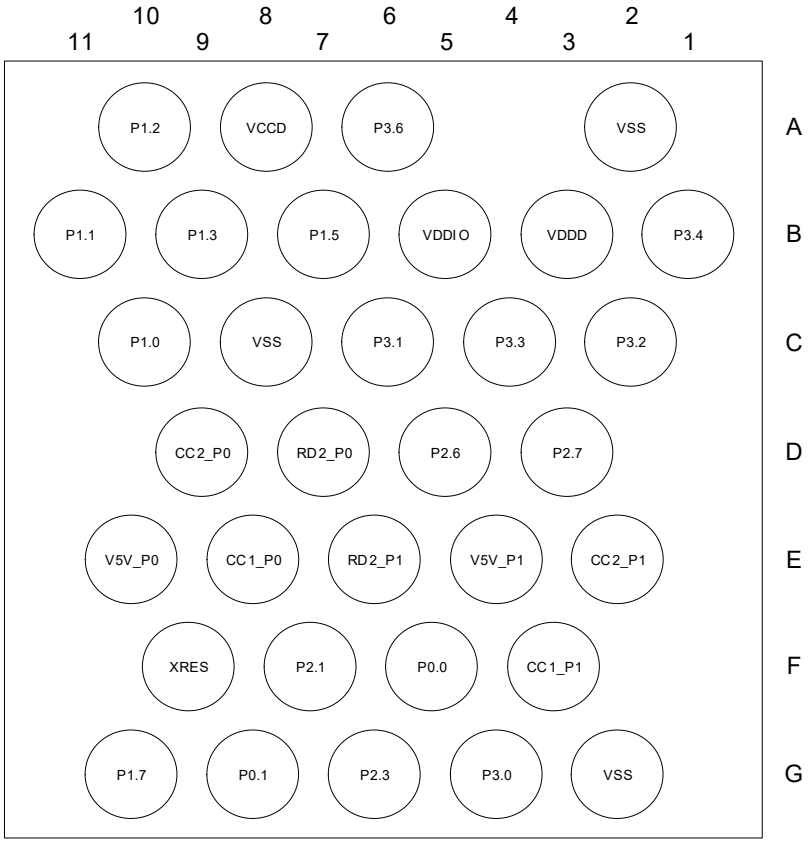


Table 8. Pin List for CYPD4225A0-33FNXIT

Pin Name	CCG4 Ball #	ESD Protection	Description
P3.1	C6	HBM	GPIO
P3.6	A6	HBM	GPIO
P0.0	F5	HBM	GPIO/optional SWD_DATA
P0.1	G8	HBM	GPIO/optional SWD_CLK
P1.0	C10	HBM	GPIO
P1.1	B11	HBM	GPIO/SWD_DATA
P1.2	A10	HBM	GPIO/SWD_CLK
P1.3	B9	HBM	GPIO
P1.5	B7	HBM	GPIO
P1.7	G10	HBM	GPIO
P2.1	F7	HBM	GPIO
P2.3	G6	HBM	GPIO
P2.6	D5	HBM	GPIO
P2.7	D3	HBM	GPIO
P3.0	G4	HBM	GPIO
P3.2	C2	HBM	GPIO
P3.3	C4	HBM	GPIO
P3.4	B1	HBM	GPIO
CC2_P0	D9	HBM, IEC	USB PD connector detect/ Configuration Channel 2 - Port 0. This pin can be hot swappable.
V5V_P0	E10	HBM	5V supply for VCONN FETs - Port 0.
CC1_P0	E8	HBM, IEC	USB PD connector detect/ Configuration Channel 1 - Port 0. This pin can be hot swappable. RD1_P0 is shorted to CC1_P0.
XRES	F9	HBM	Reset input.
CC1_P1	F3	HBM, IEC	USB PD connector detect/ Configuration Channel 1 - Port 1. This pin can be hot swappable. RD1_P1 is shorted to CC1_P1.
V5V_P1	E4	HBM	5V supply for VCONN FETs - Port 1.
CC2_P1	E2	HBM, IEC	USB PD connector detect/ Configuration Channel 2- Port 1. This pin can be hot swappable.
VDDD	B3	HBM	VDDD supply input/output (2.7 V to 5.5 V)
VDDIO	B5	HBM	1.71-V to 5.5-V supply for I/Os
VCCD	A8	HBM	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
VSS	A2, C8, G2	HBM	Ground supply
RD2_P0	D7	HBM	Rd for Port 0.
RD2_P1	E6	HBM	Rd for Port 1.

Figure 6. 33-CSP Ball Map for CYPD4225A0-FNXIT (Bottom View)



Power

The following power system diagram shows the set of power supply pins as implemented in EZ-PD CCG4.

CCG4 will be able to operate from three possible external supply sources: V5V_P0 for first Type-C port, V5V_P1 for second Type-C port and VDDD.

CCG4 has the power supply input V5V_P0 and V5V_P1 pins for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG4 per Type-C port to power either CC1 or CC2 pin. These FETs are capable of providing a minimum of 1W on the CC1 and CC2 pins for the EMCA cables. In USB-PD applications, the valid levels on V5V_P0 and V5V_P1 supplies can range from 4.85 V to 5.5 V.

The device's internal operating power supply is derived from VDDD. In UFP mode, CCG4 operates in 2.7 V– 5.5V. In DFP and DRP modes, it operates in the 3.0 V–5.5 V range.

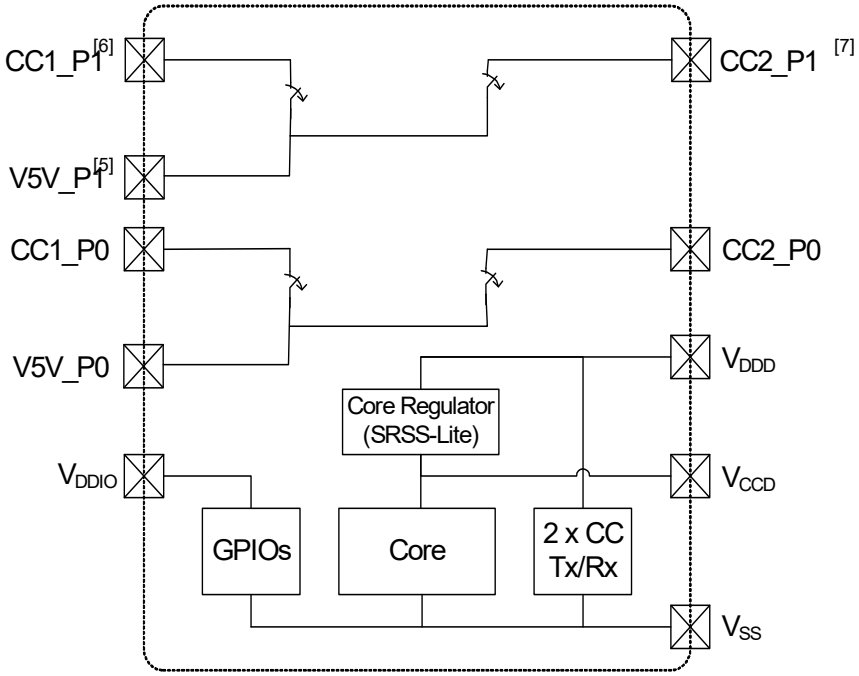
A separate I/O supply pin, VDDIO, allows the GPIOs to operate at levels from 1.71 V to 5.5 V. The VDDIO pin can be equal to or less than the voltages connected to the V5V_P0 or V5V_P1 and VDDD pins. The VDDIO supply should be less than or equal to VDDD supply.

The VCCD output of EZ-PD CCG4 must be bypassed to ground via an external capacitor (in the range of 80 to 120 nF; X5R ceramic or better).

Bypass capacitors must be used from VDDD and V5V_P0 or V5V_P1 pins to ground; typical practice for systems in this frequency range is to use a 0.1-µF capacitor on VDDD, V5V_P0 and V5V_P1. Note that these are simply rules of thumb; for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 7 shows an example of the power supply bypass capacitors.

Figure 7. EZ-PD CCG4 Power and Bypass Scheme Example



Notes
5. V5V_P0 denoted power supply input for Type-C port 0
   V5V_P1 denoted power supply input for Type-C port 1
6. CC1_P0:USB PD connector detect/Configuration Channel 1 for Type-C port 0
   CC1_P1:USB PD connector detect/Configuration Channel 1 for Type-C port 1
7. CC2_P0:USB PD connector detect/Configuration Channel 2 for Type-C port 0
   CC2_P1:USB PD connector detect/Configuration Channel 2 for Type-C port 1

Application Diagrams

Figure 8 and Figure 9 on page 20 show a dual Type-C port and a single Type-C port Notebook DRP application diagram using a CCG4 device. The Type-C port can be used as a power provider or a power consumer.

In each of these applications, CCG4 communicates with the Embedded Controller (EC), which manages the Battery Charger Controller (BCC) to control the charging and discharging of internal battery. It also controls the Data Mux to route the HighSpeed signals either to the USB chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode).The SBU, SuperSpeed, and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

For the dual Type-C notebook application, these Type-C ports can be power providers or power consumers simultaneously. In addition, the CCG4 device controls the transfer of DisplayPort signals over the Type-C interface using the display mux controllers.

Optional FETs are provided for applications that need to provide power for accessories and cables using VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. A VBUS_DISCHARGE FET controlled by CCG4 device is used to quickly discharge VBUS after the Type-C connection is detached.

Figure 8. CCG4 in a Dual Port Notebook Application using CYPD4225-40LQXIT

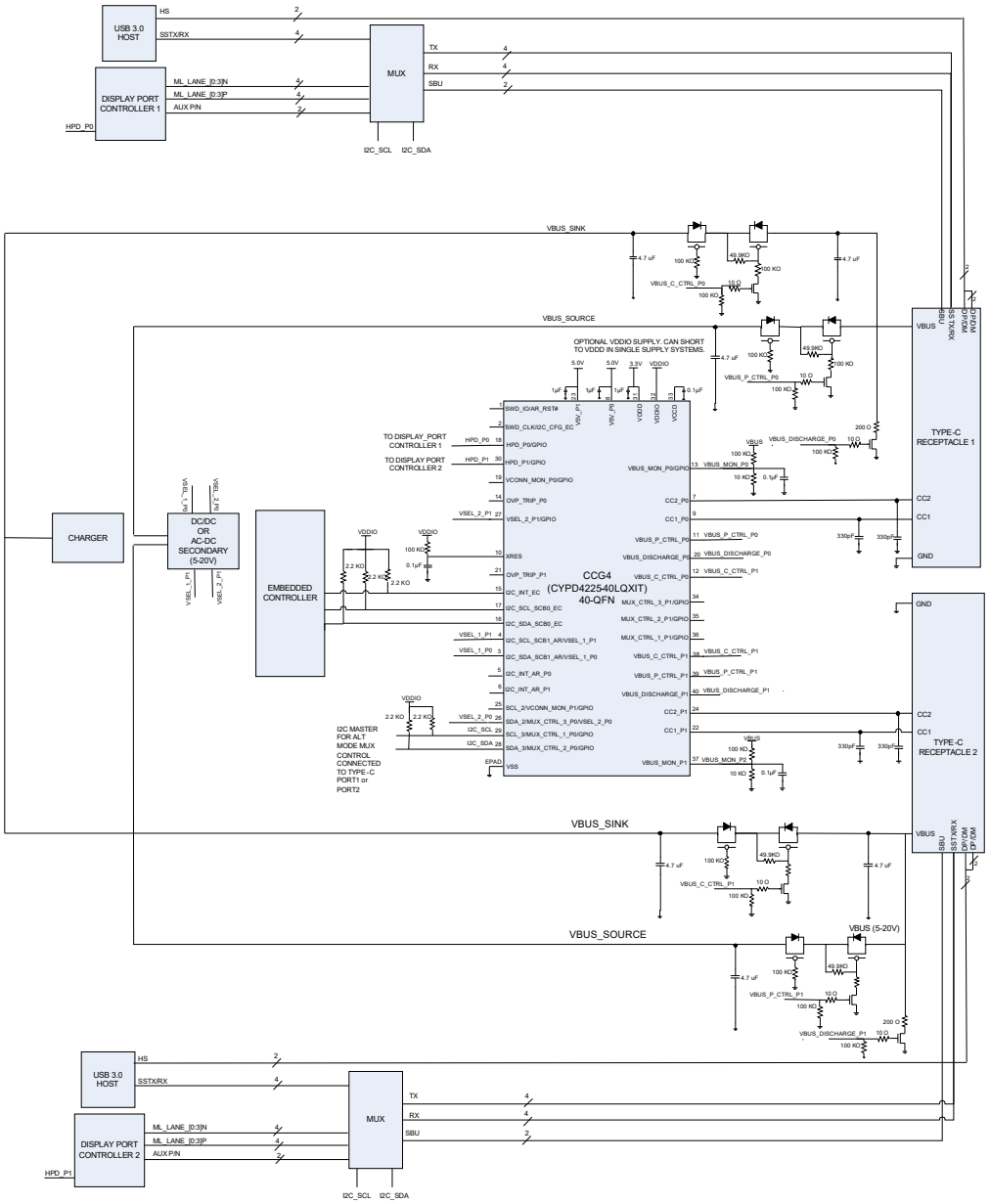
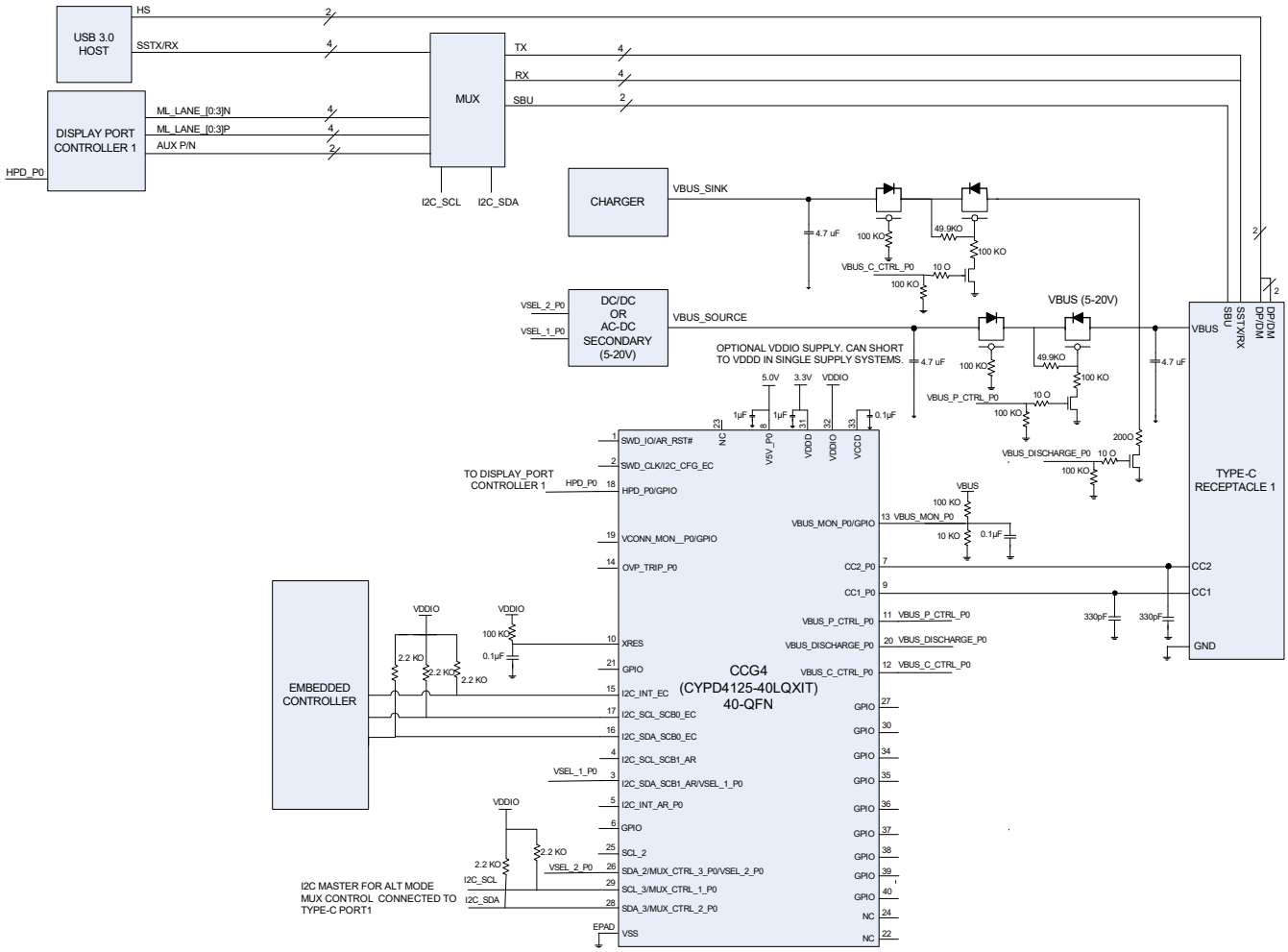


Figure 9. CCG4 in a Single Port Notebook Application using CYPD4125-40LQXIT



Electrical Specifications

Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings[8]

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V5V_P0	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V5V_P1	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	Absolute max
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1 and CC2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for pins CC1 and CC2

Note

8. Usage above the absolute maximum conditions listed in Table 9 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V, except where noted.

Table 10. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	UFP applications
SID.PWR#1_A	V_{DDD}	Power supply input voltage	3.15	–	5.5	V	DFP/DRP applications
SID.PWR#26	V5V_P0, V5V_P1	Power supply input voltage	4.85	–	5.5	V	–
PWR#13	V_{DDIO}	GPIO power supply	1.71	–	5.5	V	–
SID.PWR#24	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID.PWR#15	C_{EFC}	External regulator voltage bypass on V_{CCD}	80	100	120	nF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor on V_{DDD}	0.8	1	–	µF	X5R ceramic or better
SID.PWR#27	C_{EXV}	Power supply decoupling capacitor on V5V_P0 and V5V_P1	–	0.1	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 2.7 to 5.5 V. Typical values measured at V_{DD} = 3.3 V.							
SID.PWR#4	I_{DD12}	Supply current	–	10	–	mA	V5V_P0 and V5V_P1 = 5 V, T_A = 25 °C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, two PD ports active
Sleep Mode, V_{DDD} = 2.7 to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup WDT ON IMO at 48 MHz	–	2.5	4.0	mA	V_{DDD} = 3.3 V, T_A = 25 °C, all blocks except CPU are ON, CC I/O ON, no I/O sourcing current
Deep Sleep Mode, V_{DDD} = 2.7 to 3.6 V (Regulator on)							
SID34	I_{DD29}	V_{DDD} = 2.7 to 3.6 V I^2C wakeup and WDT ON	–	80	–	µA	V_{DDD} = 3.3 V, T_A = 25 °C
SID_DS	I_{DD_DS}	V_{DDD} = 2.7 to 3.6 V CC wakeup ON	–	2.5	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P disabled
SID_DS1	I_{DD_DS1}	V_{DDD} = 2.7 to 3.6 V CC wakeup ON	–	100	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P and R_D connected at 70 ms intervals by CPU. R_P, R_D connection should be enabled for both PD ports.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	1	10	µA	–

Table 11. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#4	F_{CPU}	CPU frequency	DC	–	48	MHz	3.0 V ≤ V_{DDD} ≤ 5.5 V
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	24-MHz IMO. Guaranteed by characterization.
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	Guaranteed by characterization
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C / CC command”	–	5	25	ms	Guaranteed by characterization

I/O

Table 12. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#37	V_{IH}[9]	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	V_{IH}[9]	LVTTL input, V_{DDIO} < 2.7 V	0.7× V_{DDIO}	–	–	V	–
SID.GIO#40	V_{IL}	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	V_{IH}[9]	LVTTL input, V_{DDIO} ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V_{IL}	LVTTL input, V_{DDIO} ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 4 mA at 1.8 V V_{DDIO}
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDIO}
SID.GIO#5	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#6	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDIO} = 3.0 V
SID.GIO#17	C_{IN}	Input capacitance	–	–	7	pF	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DDIO} ≥ 2.7 V. Guaranteed by characterization.
SID.GPIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDIO}	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DDIO}/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	Guaranteed by characterization

Note
9. V_{IH} must not exceed V_{DDIO} + 0.2 V.

Table 13. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID70	T_{RISEF}	Rise time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF
SID71	T_{FALLF}	Fall time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF

XRES

Table 14. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	–	0.05 × V_{DDIO}	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 15. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	Fc	–	MHz	Fc max = CLK_SYS. Maximum = 48 MHz
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	–	2/Fc	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	–	2/Fc	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	–	1/Fc	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	–	1/Fc	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	–	1/Fc	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 16. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

UART

Table 17. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

SPI

Table 18. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 19. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 20. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	48 + (3 × T_{SCB})	ns	$T_{SCB} = T_{CPU}$ = 1/24 MHz
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	–

Memory

Table 21. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.MEM#4	$T_{ROWWRITE}$[10]	Row (block) write time (erase and program)	–	–	20	ms	–
SID.MEM#3	$T_{ROWERASE}$[10]	Row erase time	–	–	13	ms	–
SID.MEM#8	$T_{ROWPROGRAM}$[10]	Row program time after erase	–	–	7	ms	–
SID178	$T_{BULKERASE}$[10]	Bulk erase time (128 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$[10]	Total device program time	–	–	25	seconds	Guaranteed by characterization
SID.MEM#6	F_{END}	Flash endurance	100K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET1}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization

Note
10. It can take as much as 20 milliseconds to write to flash. During this time the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Power-on-Reset (POR) with Brown Out

Table 22. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization

Table 23. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in deep sleep	1.1	–	1.5	V	Guaranteed by characterization

SWD Interface

Table 24. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ V_{DDIO} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 25. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID229	$T_{JITRMSIMO}$	RMS jitter at 48 MHz	–	145	–	ps	–
F_{IMO}	–	IMO frequency	24	–	48	MHz	–

Internal Low-Speed Oscillator

Table 26. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID234	$T_{STARTILO}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	ILO frequency	20	40	80	kHz	–

Power Down

Table 27. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP Dead Battery CC termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0 V and 1.0 V applied at CC1 or CC2. Applicable for DRP applications only.
SID.PD.15	Vdrop_V5V_CC1	Voltage drop from V5V_P0 and V5V_P1 pins to CC1 pin while sourcing 215 mA. CC1 and CC2 pins of Port0 and Port1 are not short circuit protected. Max sourcing current allowed is 500 mA.	–	–	100	mV	–
SID.PD.16	Vdrop_V5V_CC2	Voltage drop from V5V_P0 and V5V_P1 pins to CC2 pin while sourcing 215 mA. CC1 and CC2 pins of Port0 and Port1 are not short circuit protected. Max allowed sourcing current is 500 mA.	–	–	100	mV	–

Analog to Digital Converter

Table 28. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	bits	–
SID.ADC.2	INL	Integral nonlinearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential nonlinearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.0	–	1.0	LSB	–

Table 29. ADC AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

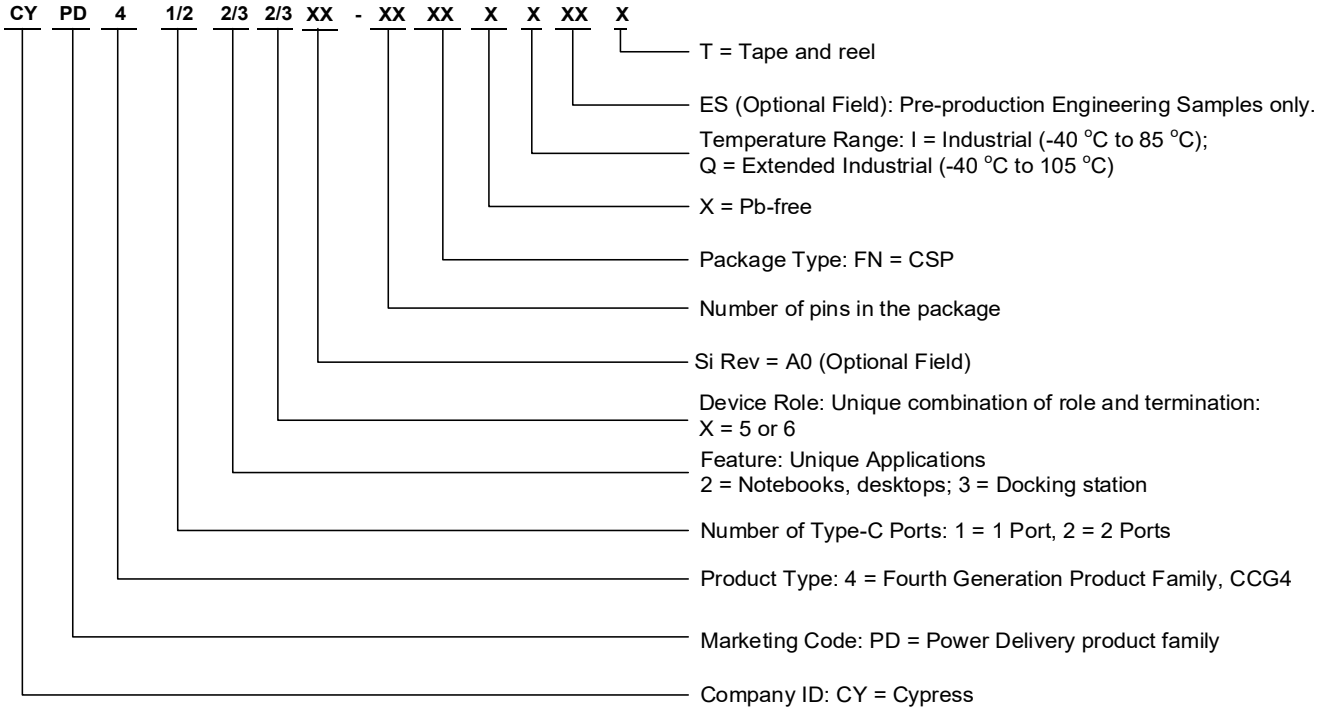
Ordering Information

The EZ-PD CCG4 part numbers and features are listed in Table 30.

Table 30. EZ-PD CCG4 Ordering Information

Part Number	Application	Type-C Ports	TCPWM	PD Spec#	Dead Battery Termination	Termination Resistor	Role	Package
CYPD4125-40LQXIT	Notebooks, desktops	1	4	PD2.0	Yes	R_P[11], R_D[12], R_{D-DB}[12]	DRP	40-pin QFN
CYPD4225-40LQXIT	Notebooks, desktops	2	4	PD2.0	Yes	R_P[11], R_D[12], R_{D-DB}[12]	DRP	40-pin QFN
CYPD4126-40LQXIT	Notebooks, desktops	1	2	PD3.0	Yes	R_P[11], R_D[12], R_{D-DB}[12]	DRP	40-pin QFN
CYPD4226-40LQXIT	Notebooks, desktops	2	2	PD3.0	Yes	R_P[11], R_D[12], R_{D-DB}[12]	DRP	40-pin QFN
CYPD4236-40LQXIT	Docking station	2	2	PD3.0	No	R_P[11], R_D[12]	DRP	40-pin QFN
CYPD4236-40LQXQT	Dual Port Power Adapter	2	2	PD3.0	No	R_P[11], R_D[12]	DFP	40-pin QFN
CYPD4126-24LQXIT	Notebooks, desktops	1	2	PD3.0	Yes	R_P[11], R_D[12], R_{D-DB}[12]	DRP	24-pin QFN
CYPD4136-24LQXIT	Docking station	1	2	PD3.0	No	R_P[11], R_D[12]	DRP	24-pin QFN
CYPD4225A0-33FNXIT	Notebooks, desktops	2	4	PD2.0	Yes	R_P[11], R_D[12], R_{D-DB}[12]	DRP	33-ball CSP

Ordering Code Definitions



Notes
11. Termination resistor denoting a downstream facing port.
12. Termination resistor denoting an accessory or upstream facing port.

Packaging

Table 31. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	31	–	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	29	–	°C/W
T_{JA}	Package θ_{JA} (24-pin QFN)	–	–	22	–	°C/W
T_{JC}	Package θ_{JC} (24-pin QFN)	–	–	29	–	°C/W
T_{JA}	Package θ_{JA} (33-ball CSP)	–	–	24	–	°C/W
T_{JC}	Package θ_{JC} (33-ball CSP)	–	–	1	–	°C/W

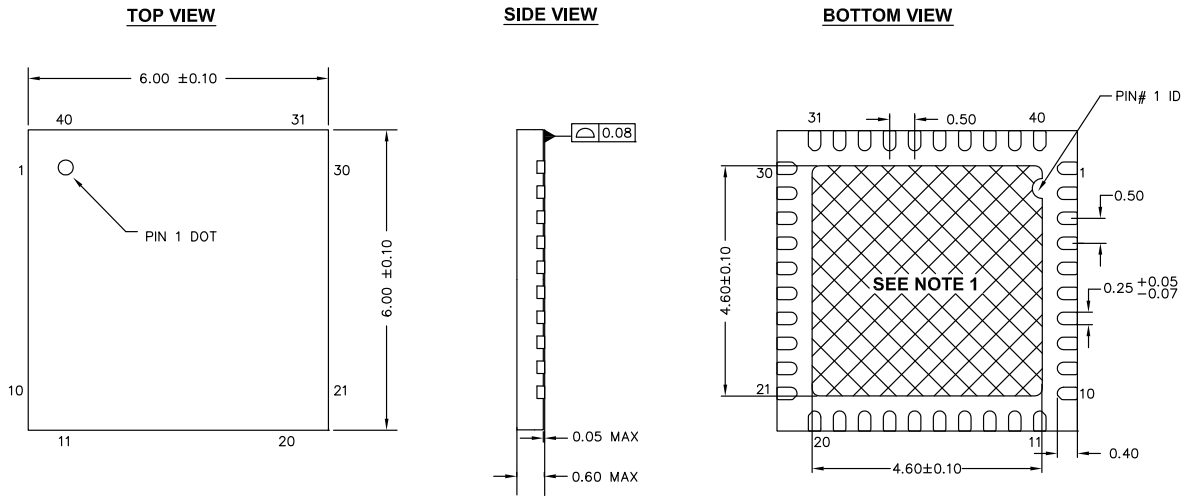
Table 32. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
24-pin QFN	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds
33-ball CSP	260 °C	30 seconds

Table 33. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL 3
40-pin QFN	MSL 3
33-ball CSP	MSL 1

Figure 10. 40-Pin QFN (6 × 6 × 0.6 mm), LR40A/LQ40A 4.6 × 4.6 E-PAD (Sawn) Package Outline, 001-80659

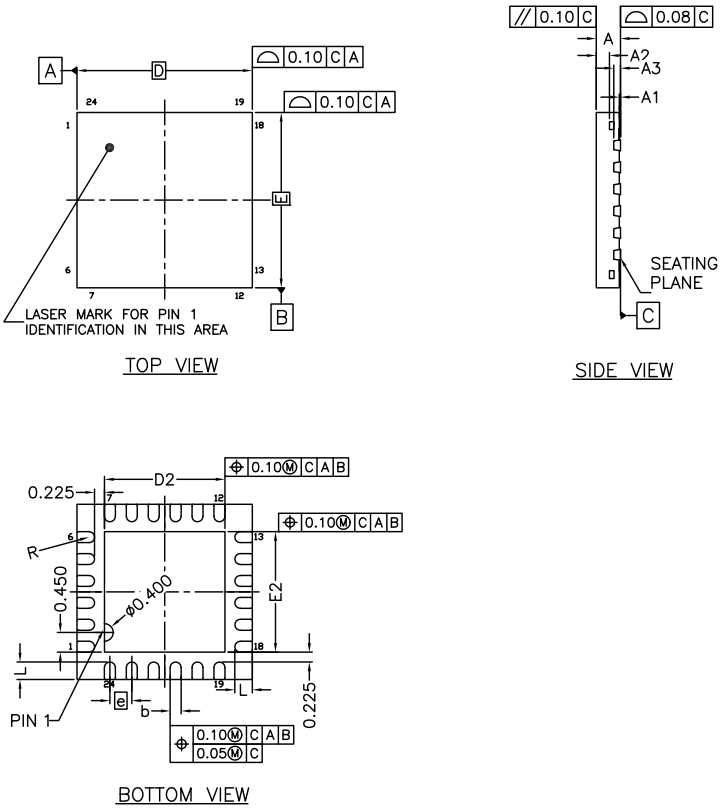


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 11. 24-pin QFN Package Outline



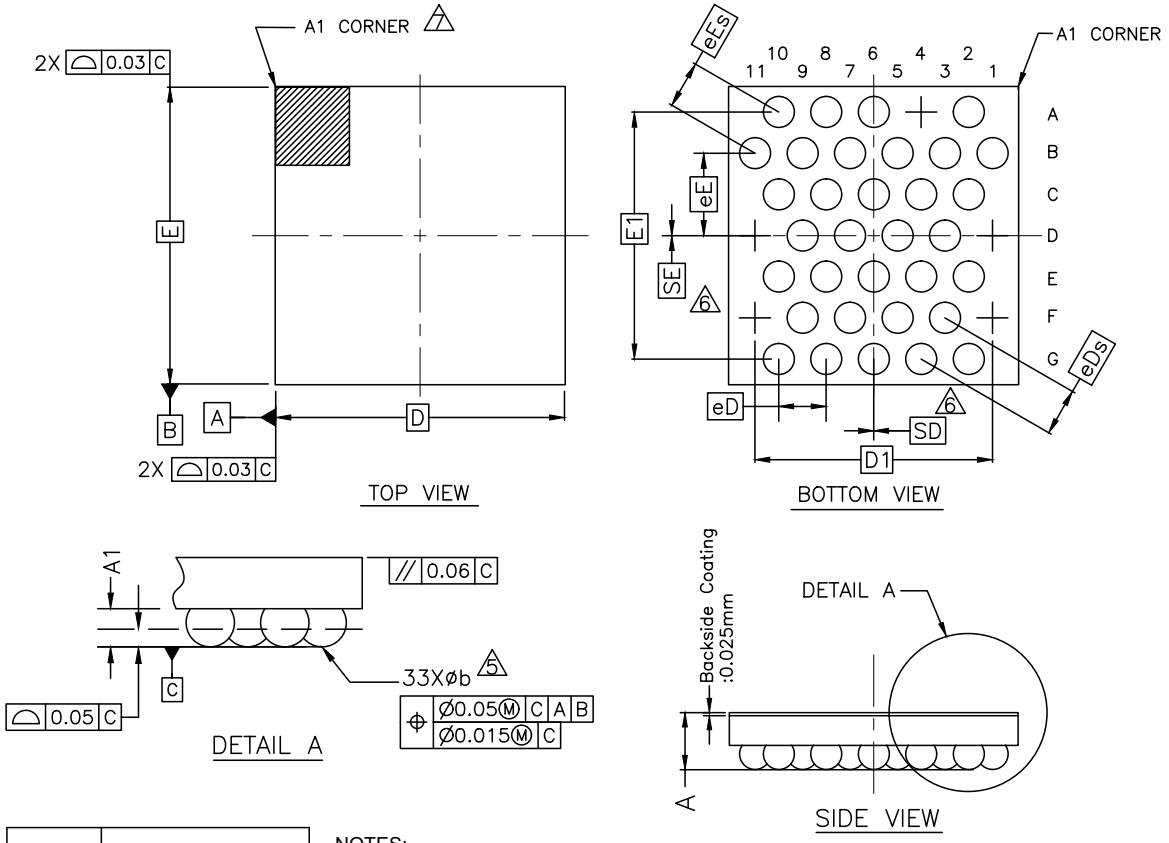
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A_1	0.00	—	0.05
A_2	—	0.40	0.425
A_3	0.152 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D_2	2.65	2.75	2.85
E	4.00 BSC		
E_2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.

002-16934 *C

Figure 12. 33-ball CSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.514
A1	0.169	-	-
D	2.443 BSC		
E	2.510 BSC		
D1	2.000 BSC		
E1	2.078 BSC		
MD	11		
ME	7		
N	33		
• ••••	0.235	0.265	0.295
eD	0.40 BSC		
eE	0.693 BSC		
eDs / eEs	0.40 BSC		
SD / SE	0.00 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-28711 **

Acronyms

Table 34. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 34. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG4 pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 35. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond

Table 35. Units of Measure *(continued)*

Symbol	Unit of Measure
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

References and Links to Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG3: USB Type-C Controller Datasheet

Document History Page

Document Title: EZ-PD CCG4, USB Type-C Port Controller Document Number: 001-98440			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	4921014	09/24/2015	New data sheet.
*A	4999504	11/03/2015	Updated Pinouts: Updated Table 1. Updated Table 2. Updated Figure 3. Updated Figure 4. Updated Application Diagrams: Updated Figure 8. Updated Figure 9. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 9. Updated Device-Level Specifications: Updated Table 10. Updated Digital Peripherals: Updated SPI: Updated Table 20. Updated System Resources: Updated Internal Main Oscillator: Updated Table 25.
*B	5049109	12/14/2015	Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 10. Updated System Resources: Updated Analog to Digital Converter: Updated Table 28.
*C	5141544	03/02/2016	Updated Features: Updated Low-Power Operation: Replaced “Sleep: 2 mA” with “Sleep: 2.5 mA”. Updated Pinouts: Updated Table 1: Updated details in “Description” column corresponding to pins 34, 5, and 10. Updated Table 2: Updated details in “Description” column corresponding to pins 5, and 10. Updated Application Diagrams: Updated Figure 8. Updated Figure 9. Updated Electrical Specifications: Updated Digital Peripherals: Updated I^2C: Removed table “Fixed I2C DC Specifications”. Updated UART: Removed table “Fixed UART DC Specifications”. Updated SPI: Removed table “Fixed SPI DC Specifications”. Updated System Resources: Updated Internal Main Oscillator: Removed table “IMO DC Specifications”. Updated Internal Low-Speed Oscillator: Removed table “ILO DC Specifications”. Updated copyright information.
*D	5290129	05/31/2016	Updated EZ-PD CCG4 Block Diagram: Updated Figure 1. Updated Functional Overview: Updated USB-PD Subsystem (SS): Updated description (Updated to include support for PD 3.0 features). Updated Table 33.
*E	5307418	06/14/2016	Added Available Firmware and Software Tools. Updated Application Diagrams: Added description (Added descriptive notes). Added References and Links to Applications Collaterals. Updated Cypress logo and copyright information.

Document History Page *(continued)*

Document Title: EZ-PD CCG4, USB Type-C Port Controller Document Number: 001-98440			
Revision	**ECN**	**Submission Date**	**Description of Change**
*F	5669709	03/30/2017	Changed status from Preliminary to Final. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 10: Changed typical value of I_{DD29} parameter from 60 µA to 80 µA corresponding to Condition "V_{DDD} = 3.3 V, T_A = 25 °C". Updated Ordering Information: Updated Table 30: Updated part numbers. Updated to new template.
*G	5830717	07/24/2017	Updated Pinouts: Added Table 7. Added Figure 5. Updated Ordering Information: Updated Table 30: Updated part numbers. Updated Packaging: Added spec 002-16934 *A. Completing Sunset Review.
*H	5899958	09/29/2017	Updated Pinouts: Updated Table (Updated caption only). Updated Table 2 (Updated caption only). Updated Figure 3 (Updated caption only). Updated Figure 4 (Updated caption only). Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 10: Changed minimum value of V_{DDD} parameter from 3 V to 3.15 V corresponding to Test Condition "DFP/DRP applications".
*I	5963293	11/10/2017	Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions: Updated details under "Device Role".
*J	6045099	01/25/2018	Updated Electrical Specifications: Updated Device-Level Specifications: Updated I/O: Updated Table 12: Changed maximum value of V_{OL} parameter from 0.6 V to 0.4 V corresponding to Test Condition "I_{OL} = 4 mA at 1.8 V V_{DDIO}". Updated to new template.
*K	6217334	06/26/2018	Updated Ordering Code Definitions.
*L	6730730	11/15/2019	Changed document status from Final to Preliminary. Updated Features. Updated Table 1 through Table 7 and Table 31 through Table 33. Updated Figure 3 and Figure 4. Added CY MPN "CYPD4225A0-33FNXIT" to Table 30. Added Table 8 for 33-ball CSP part. Added Figure 6 for 33-ball CSP part. Added Figure 12 for 33-ball CSP part. Updated Ordering Code Definitions. Updated spec 002-16934 *B in Packaging. Updated SCB nomenclatures from SCB1 thru SCB4 to SCB0 thru SCB3 across the entire document. Updated Port 1 and Port 2 nomenclatures to Port 0 and Port 1 across the entire document.
*M	7037701	12/08/2020	Removed Preliminary status. Updated Features. Added CY MPN "CYPD4236-40LQXQT" to Table 30. Updated Table 31. Updated Ordering Code Definitions. Updated Figure 11 in Packaging (spec 002-16934 *B to *C). Updated Sales, Solutions, and Legal Information.

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