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General Description

EZ-PD™ CCG6DF and EZ-PD CCG6SF are dual-port and single-port USB Type-C controllers that comply with the latest USB Type-C and PD specifications. These devices provide a complete USB Type-C and USB-Power Delivery port control solution for PCs and notebooks. Both of these devices include a VBUS provider path load switch. These devices also contain a True Random Number Generator for authentication, a 32-bit, 48-MHz Arm® Cortex®-M0 processor with 64-KB flash and 96-KB ROM, integrating a complete Type-C Transceiver including the Type-C termination resistors Rp, Rd, and dead battery Rd termination. CCG6DF is available in a 96-ball BGA package, whereas CCG6SF is available in 48-pin QFN package.

Applications

- Notebooks and desktops
- Thunderbolt hosts, non-Thunderbolt hosts

Features

USB-PD

- Supports latest USB PD 3.0 specification
- Fast Role Swap (FRS)
- Extended Data Messaging

Type-C

- Integrated current sources for DFP^[1] role (Rp)
 - Default current at 900 mA
 - 1.5 A
 - 3 A
- Integrated Rd resistor for UFP^[2] role
- Integrated VCONN FETs to power EMCA cables
- Integrated dead battery termination
- Integrated high-voltage protection on CC and SBU pins to protect against accidental shorts to the VBUS pin on the Type-C connector
- Integrated pass through SBU Switch for 20-V protection

Mux

- Integrated USB 2.0 Analog Mux for USB 2.0 HS and UART data

Integrated Provider VBUS Load Switch

- VBUS Provider Switch (5 V/3A)
- Slew rate controlled turn-on on the VBUS provider path, tolerant to 24 V
- Configurable hardware-controlled VBUS overvoltage, under-voltage, overcurrent, short circuit, reverse current protection, and thermal shutdown
- VBUS high-side current sense amplifier capable of measuring current across 5-mΩ series resistance on the provider path

- In response to Fast Role Swap request, turns OFF external consumer N-channel Field Effect Transistor (NFET) and turns ON internal provider load switch

LDO

- Integrated high-voltage LDO operational up to 21.5 V for dead battery mode operation

32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0 CPU
- 64-KB Flash
- 96-KB ROM
- 16-KB SRAM

Integrated Digital Blocks

- Two integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time serial communication blocks (SCBs) with reconfigurable I²C, SPI, or UART functionality

Authentication

- True Random Number Generator

Clocks and Oscillators

- Integrated oscillator eliminating the need for an external clock

Operating Range

- VSYS (2.75 V–5.5 V)
- VBUS (4 V–21.5 V)

Hot-Swappable I/Os

- I²C pins from SCB0 are hot-swappable

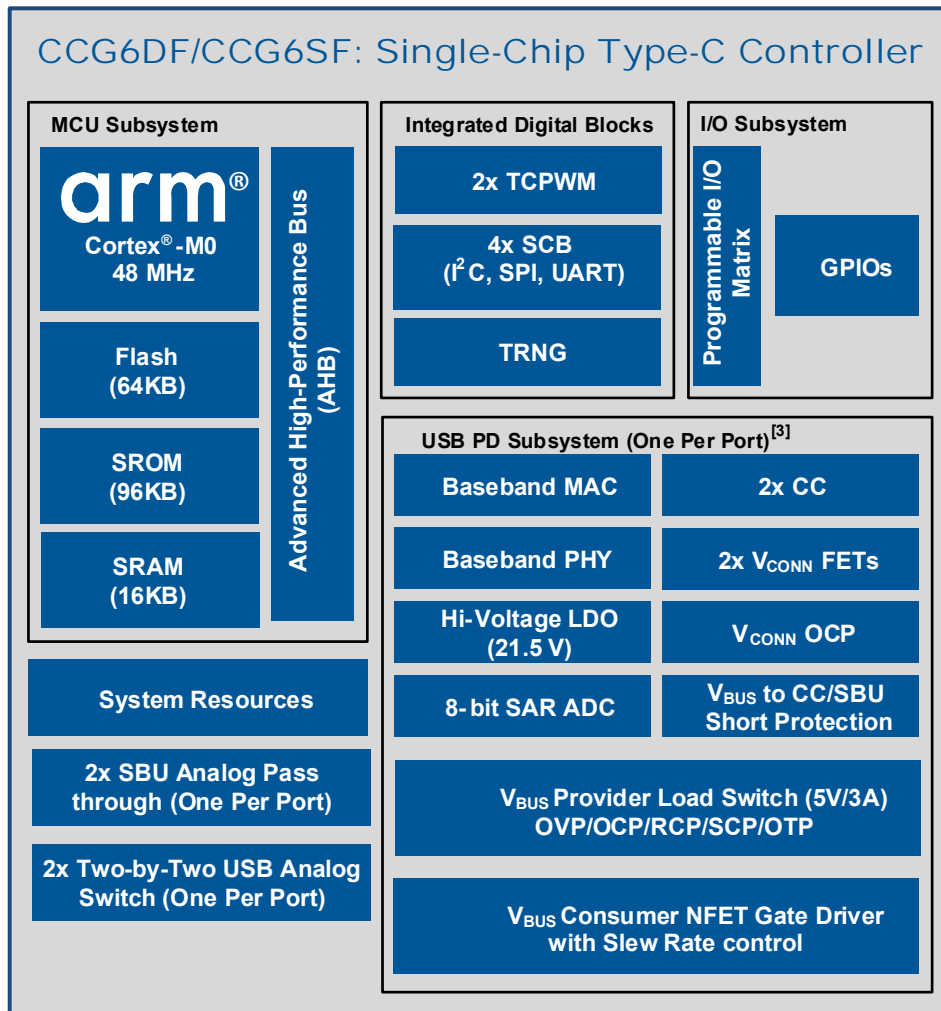
Packages

- CCG6DF: 6.0 mm × 6.0 mm × 1.0 mm, 96-ball BGA with 0.5-mm pitch
- CCG6SF: 6.0 mm × 6.0 mm × 0.6 mm, 48-pin QFN with 0.4-mm pitch

Notes

1. DFP refers to power source.
2. UFP refers to power sink.

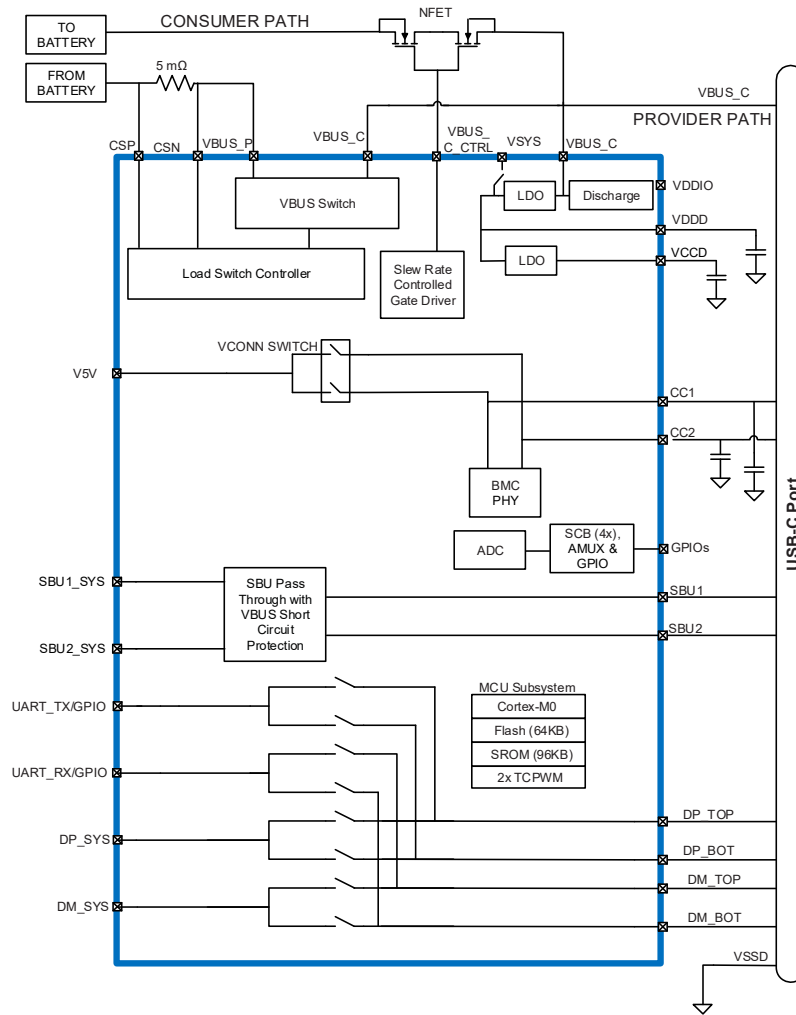
Logic Block Diagram



Note

3. Only one USB-PD subsystem exists for CCG6SF devices since it has only one Type-C port available.

CCG6DF/CCG6SF Functional Diagram



Note
To simplify, the functional block diagram is shown only for one port.

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Functional Overview

MCU Subsystem

CPU

The Cortex M0 in CCG6DF and CCG6SF devices is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set, which enables fully compatible binary upward migration of code to higher performance processors such as Cortex M3 and M4. Also included is a hardware multiplier, which provides a 32-bit result in one cycle. It includes an Interrupt Controller (the NVIC block) with 32 Interrupt inputs and a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode.

Flash, SRAM, and RAM

The 64-KB Flash and 96-KB ROM store the firmware implementing PD functionality.

The 16-KB RAM is used under software control to store temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

This subsystem provides the interface to the Type-C USB port. This subsystem comprises of:

- USB-PD Physical Layer
- VCONN FETs
- ADC
- SBU pass-through switch and USB HS mux
- Undervoltage, overvoltage and Reverse-Current Protection on VBUS
- High-side current sense amplifier for VBUS
- VBUS Discharge
- VBUS Regulator
- Consumer Gate Driver for VBUS NFET
- Integrated VBUS Provider path load switch with FRS
- VBUS tolerant SBU and CC pins

USB-PD Physical Layer

The USB-PD subsystem contains the USB-PD physical layer block and supporting circuits. The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC encoded data over the CC channel per the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

In addition, the USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB Type-C spec. R_P and R_D resistors are required to implement connection detection, plug orientation detection and for establishment of the USB source/sink roles. The R_P resistor is implemented as a current source.

The R_D resistors on CC pins are required even when the part is not powered on. This is required for dead battery termination detection and charging.

To support the latest USB-PD 3.0 specification, CCG6DF and CCG6SF devices implement the FRS feature. Fast Role Swap enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. This feature is supported for provider N-FET Gate Driver Output (NGDO). SCP and RCP fault detection are not enabled during the FRS sequence and it is assumed that provider side supply is present and higher than 4.85 V.

CCG6DF and CCG6SF devices are designed to be fully interoperable with revision 3.0 of the USB Power Delivery specification as well as revision 2.0 of the USB Power Delivery specification.

VCONN FET

CCG6DF and CCG6SF devices have power supply input V5V pin for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs per port in CCG6DF and CCG6SF devices to power either CC1 or CC2 pins. These FETs source a minimum of 1.5-W power per port over the valid VCONN range of 4.85 V to 5.5 V on the CC1/2 pins when providing power to EMCA cables. At any given time, only one of the VCONN FETs is in ON state to provide VCONN on either CC1 or CC2 lines depending on the cable orientation. The floating V5V pin does not cause CCG6DF to malfunction and draw more current.

ADC

CCG6DF and CCG6SF devices have a low power 8-bit SAR ADC that has access to the chip-wide analog mux. All GPIOs on these devices have access to the ADCs through the chip-wide analog mux.

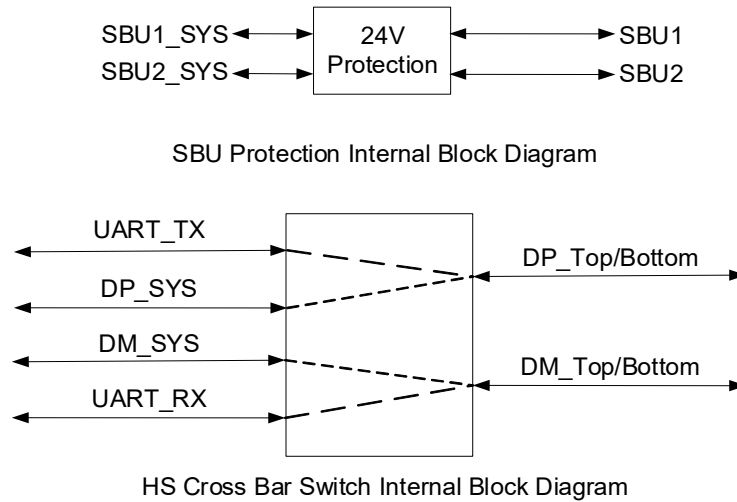
SBU Pass-Through Switch and USB HS Mux

CCG6DF has integrated 2x SBU pass-through switches and 2x high-speed (480 Mbps) switches as shown in [Figure 1](#).

The SBU switch is a simple pass-through switch. The Type-C facing SBU pins are protected from accidental short to VBUS.

The HS mux contains a 2×2 cross bar switch to route the system DP/DM lines to the Type-C top or bottom lines as per the CC (Type-C plug) orientation and connect the Debug pins to unused DP or DM top or bottom pins.

Figure 1. SBU Protection and High-Speed Crossbar Switch Block Diagram



Provider Load Switch

CCG6DF and CCG6SF devices have an integrated provider load switch with the following functions.

Undervoltage and Overvoltage Protection on VBUS

CCG6DF and CCG6SF devices implement an under-voltage/overvoltage (UVOV) detection circuit for the VBUS supply. The thresholds for both OCP and UVOV are programmable.

High-side Current Sense Amplifier for VBUS

CCG6DF and CCG6SF devices support the programmable threshold VBUS current sensing through VBUS provider path. External resistor (5 mΩ) placed in VBUS provider path connecting to the chip, the drop across this resistor is monitored to sense the magnitude of current.

VBUS Reverse Current Protection

CCG6DF and CCG6SF devices restrict reverse current to zero on the VBUS provider path when the Type-C VBUS is greater than VIN (provider voltage before the VBUS NFET).

VBUS Short Circuit Protection

CCG6DF and CCG6SF devices have a VBUS short circuit protection function of which the SCP threshold is programmable. Whenever current through the VBUS Provider Load Switch exceeds the programmed threshold, the SCP gets triggered instantly and turns off the VBUS provider path within a short duration.

VBUS Discharge

CCG6DF and CCG6SF devices support high-voltage (21.5 V) VBUS discharge circuitry inside. After cable removal detection, the chips discharge the residual charge and bring the floating VBUS to less than 0.8 V.

VBUS Regulator

CCG6DF and CCG6SF devices can either be powered by VSYS or VBUS power supplies. There is one VBUS per port. Hence the CCG6DF device can be powered by either VBUS (Port0 or Port1) or VSYS. A regulator operating on these power supplies derives the chip operating supply. When both power supplies are present, VSYS always takes priority over VBUS supplies. In absence of VSYS, the regulator powers the chip from VBUS.

Gate Driver for VBUS NFET

CCG6DF and CCG6SF devices have integrated gate drivers to drive external NFETs on the VBUS consumer path. The provider NFETs are integrated. The consumer side supports only the external NFET driver and these NFETs must be capable of supporting ±VBUS_MAX VGS. CCG6DF and CCG6SF must be in active mode to enable the consumer-side NGDO.

VBUS Tolerant SBU and CC Lines

CCG6DF and CCG6SF devices support VBUS tolerant SBU and CC lines. In case of SBU/CC short to VBUS through connectors, these lines are protected internally. Accidental shorts may occur because the SBU/CC pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of such accidental shorts. When overvoltage is detected on the SBU/CC lines, the internal protection circuit will turn off the connection between the Type-C connector and the rest of the device.

Serial Communication Block (SCB)

CCG6DF and CCG6SF devices have four SCB blocks that can be configured for I²C, SPI, or UART. These blocks implement full multi-master and slave I²C interfaces capable of multi-master arbitration. I²C is compatible with the standard Philips I²C Specification V3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU.

The SCB blocks support 8-byte deep FIFOs for Receive and Transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

Timer, Counter, Pulse-Width Modulator (TCPWM)

The TCPWM block of CCG6DF and CCG6SF supports up to two timers or counters or pulse-width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

True Random Number Generator (TRNG)

In notebook designs, CCG6DF's and CCG6SF's TRNG block is used in authenticating connected devices such as power adapters or docks that include support for USB Type-C Authentication Specification (USBTCAS). CCG6DF and CCG6SF devices, within notebook applications, are implemented as an initiate role as defined in USBTCAS, while the connected device would implement the responder-role. USBTCAS provides a means for authenticating Type-C devices with regards to identification and configuration.

GPIO Interface

The CCG6DF device has 23 GPIOs and the CCG6SF device has 19 GPIOs including the I²C and SWD pins, which can also be used as GPIOs.

The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled.
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output disables.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control.

During power-on and reset, the blocks are forced to the Disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may

connect to an I/O pin. Pin locations for fixed-function peripherals, such as USB Type-C ports, are also fixed to reduce internal multiplexing complexity. Data Output Registers and Pin State Register store, respectively, the values to be driven on the pins and the states of the pins themselves. The configuration of the pins can be done by programming of registers through software for each digital I/O Port.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an IRQ and ISR vector associated with it.

The I/O ports retain their state during Deep Sleep mode or remain ON. If operation is restored using reset, then the pins shall go the High-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The I/Os (on data bus) do not draw current on power down.

All GPIOs reside in a separate I/O power domain – VDDIO to provide flexible system-level interfacing.

System Resources

Watchdog Timer (WDT)

A watchdog timer is implemented in the Clock block running from the internal low-speed oscillator (ILO) for CCG6DF and CCG6SF devices. This allows watchdog operation during Deep Sleep and generates a Watchdog Reset if not serviced before the timeout occurs.

In addition to the chip-level watchdog timer, each USB-PD block implements a counter based on ILO (Low frequency) clock which can be used to wake/trigger the part periodically. This counter can be used to drive any periodic tasks to be performed by the device.

Clock System

CCG6DF and CCG6SF have a fully integrated clock with no external crystal required. CCG6DF/CCG6SF clock system is responsible for providing clocks to all subsystems that require clocks (SCB and USB-PD) and for switching between different clock sources, without glitches. The clock system for these devices consists of the internal main oscillator (IMO) and the ILO.

IMO Clock Source

The IMO is the primary source of internal clocking in CCG6DF and CCG6SF devices with an accuracy of $\pm 2\%$. The default IMO frequency for CCG6DF and CCG6SF devices is 48 MHz $\pm 2\%$.

ILO Clock Source

The ILO is a very low power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB Suspend (Deep Sleep) mode. The typical frequency of the ILO is 32-kHz.

Power

CCG6DF can operate either from VBUS_C (from Port 0 and/or 1) or V_{SYS} supply inputs. In addition, there is V5V supply pin, which sources the V_{CONN} supply to the Type-C connector, the valid levels on V5V supply can range from 4.85 – 5.5 V. V5V does not power the chip. The chip's internal operating power supply is derived from V_{SYS} (2.75 V to 5.5 V) or VBUS (4 V- 21.5 V). In dead battery mode, the chip can be supplied power from Type-C VBUS (from port 0 and/or 1). In UFP, DFP, and DRP modes (when the system battery is charged), the chip is powered via V_{SYS}. CCG6DF and CCG6SF devices support power modes to minimize energy consumption when not actively involved in data communication over the Type-C port.

Figure 2 and Figure 3 show an overview of the power system requirement for CCG6DF and CCG6SF devices. CCG6DF and CCG6SF devices have two different power modes: Active and Deep Sleep, transitions between which are managed by the Power System. A separate power domain, V_{DDIO}, is provided for the GPIOs and V_{DDD} which generates 3.3 V from internal regulator. V_{DDD} can be shorted to V_{DDIO}. V_{DDD} and V_{CCD} are not recommended to be used as power supplies for other circuits on the system. Also, V_{DDD} and V_{CCD} pins cannot be treated as power sources for the chip. The V_{CCD} pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1-μF capacitor for the regulator stability only.

Figure 2. CCG6DF Power Supply Requirement Block Diagram

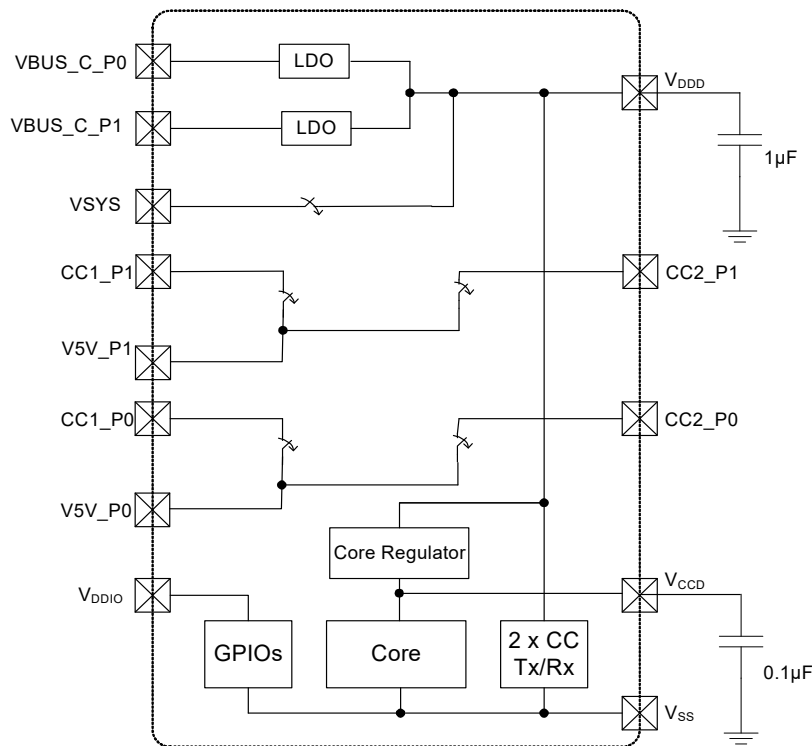


Figure 3. CCG6SF Power Supply Requirement Block Diagram

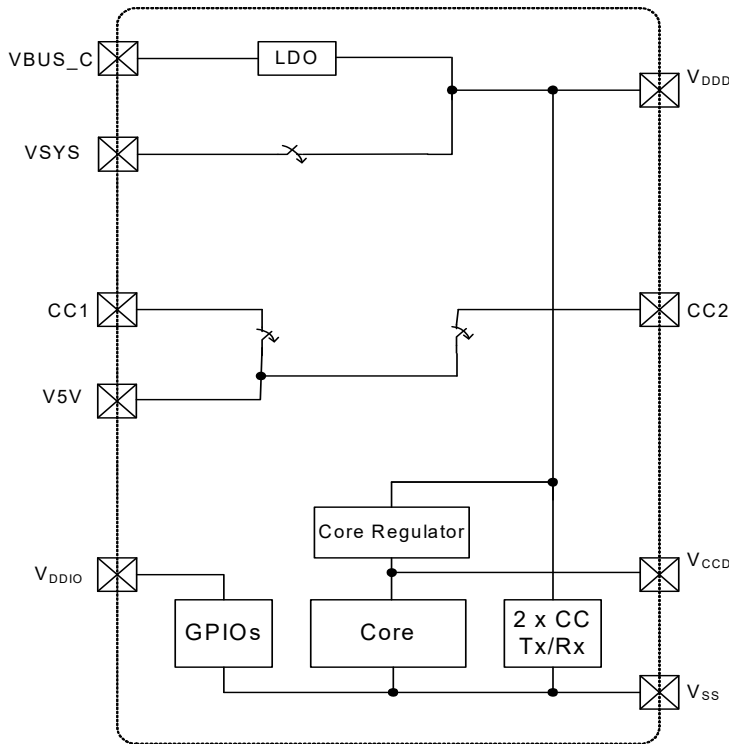


Table 1. CCG6DF/CCG6SF Power Modes

| Mode | Description |
|------------|--|
| Reset | Power is Valid and XRES is not asserted. An internal reset source is asserted or Sleep Controller is sequencing the system out of reset. |
| ACTIVE | Power is Valid and CPU is executing instructions. This mode includes the critical Type-C power spec requirement. |
| DEEP SLEEP | Main regulator and most hard-IP are shut off. DeepSleep regulator powers logic, but only low-frequency clock is available. |

Pinouts

Table 2. Pinout for CYPD6227-96BZXI

| Group Name | Pin Name | Port | Pin | Description |
|----------------|-----------------|--------|-----|--|
| USB Type-C | CC1_P0 | Analog | B3 | USB PD Port-0 connector detect/Configuration Channel 1 |
| | CC2_P0 | Analog | B5 | USB PD Port-0 connector detect/Configuration Channel 2 |
| | CC1_P1 | Analog | K5 | USB PD Port-1 connector detect/Configuration Channel 1 |
| | CC2_P1 | Analog | K3 | USB PD Port-1 connector detect/Configuration Channel 2 |
| Muxes/Switches | DP_SYS_P0 | Analog | K11 | USB 2.0 DP from the Host System: Port-0 |
| | DM_SYS_P0 | Analog | J11 | USB 2.0 DM from the Host System: Port-0 |
| | UART_TX_P0/P1.4 | GPIO | H10 | UART Tx from Host System: Port-0/GPIO |
| | UART_RX_P0/P1.3 | GPIO | G10 | UART Rx from Host System: Port-0/GPIO |
| | DP_BOT_P0 | Analog | K10 | USB 2.0 DP from Bottom of Type-C Connector: Port-0 |
| | DM_BOT_P0 | Analog | J10 | USB 2.0 DM from Bottom of Type-C Connector: Port-0 |
| | DM_TOP_P0 | Analog | H11 | USB 2.0 DM from Top of Type-C Connector: Port-0 |
| | DP_TOP_P0 | Analog | G11 | USB 2.0 DP from Top of Type-C Connector: Port-0 |
| | SBU2_P0 | Analog | A4 | Type-C Sideband Use signal – Connector side: Port-0 |
| | SBU1_P0 | Analog | A5 | Type-C Sideband Use signal – Connector side: Port-0 |
| | SBU1_SYS_P0 | Analog | B6 | Type-C Sideband Use signal – System side: Port-0 |
| | SBU2_SYS_P0 | Analog | A6 | Type-C Sideband Use signal – System side: Port-0 |
| | DP_SYS_P1 | Analog | L6 | USB 2.0 DP from the Host System: Port-1 |
| | DM_SYS_P1 | Analog | L5 | USB 2.0 DM from the Host System: Port-1 |
| | UART_TX_P1/P0.0 | GPIO | L4 | UART Tx from Host System: Port-1/GPIO |
| | UART_RX_P1/P0.1 | GPIO | K6 | UART Rx from Host System: Port-1/GPIO |
| | DP_BOT_P1 | Analog | K8 | USB 2.0 DP from Bottom of Type-C Connector: Port-1 |
| | DM_BOT_P1 | Analog | K7 | USB 2.0 DM from Bottom of Type-C Connector Port-1 |
| | DM_TOP_P1 | Analog | L7 | USB 2.0 DM from Top of Type-C Connector: Port-1 |
| | DP_TOP_P1 | Analog | L8 | USB 2.0 DP from Top of Type-C Connector: Port-1 |
| | SBU2_P1 | Analog | A9 | Type-C Sideband Use signal – Connector side: Port-1 |
| | SBU1_P1 | Analog | A8 | Type-C Sideband Use signal – Connector side Port-1 |
| | SBU1_SYS_P1 | Analog | B7 | Type-C Sideband Use signal – System side: Port-1 |
| | SBU2_SYS_P1 | Analog | A7 | Type-C Sideband Use signal – System side: Port-1 |
| VBUS Control | VBUS_C_CTRL_P0 | Analog | A3 | Full rail control I/O for enabling/disabling Consumer load NFET of USB Type-C Port-0 |
| | VBUS_C_CTRL_P1 | Analog | L3 | Full rail control I/O for enabling/disabling Consumer load NFET of USB Type-C Port-1 |
| VBUS OCP | CSP_P0 | Analog | A11 | Current Sense Positive Input for VBUS side external Rsense: Port-0 |
| | CSN_P0 | Analog | A10 | Current Sense Negative input for other side of external Rsense: Port-0 |
| | CSP_P1 | Analog | L11 | Current Sense Positive Input for VBUS side external Rsense: Port-1 |
| | CSN_P1 | Analog | L10 | Current Sense Negative input for other side of external Rsense: Port-1 |

Table 2. Pinout for CYPD6227-96BZXI (continued)

| Group Name | Pin Name | Port | Pin | Description |
|-----------------------------|---------------------|--------|--|--|
| GPIOs and Serial Interfaces | I2C_SDA_SCB1/P0.2 | GPIO | K9 | SCB1 data for communicating with SoC or TBT controller/ GPIO |
| | I2C_SCL_SCB1/P0.3 | GPIO | H7 | SCB1 clock for communicating with SoC or TBT controller / GPIO |
| | I2C_INT_EC/P1.2 | GPIO | F11 | Embedded Controller interrupt / GPIO |
| | P2.4 | GPIO | D10 | GPIO |
| | I2C_INT_TBT_P0/P0.4 | GPIO | L9 | ThunderBolt interrupt for Port-0 / GPIO |
| | SWD_IO/P1.1 | GPIO | G8 | Serial Wire Debug I/O / GPIO |
| | SWD_CLK/P1.0 | GPIO | F10 | Serial Wire Debug Clock / GPIO |
| | HPD_P0/P2.0 | GPIO | F8 | Hot Plug Detect I/O for Port-0 / GPIO |
| | I2C_SDA_SCB2/P2.1 | GPIO | E11 | SCB2 data for configuring Re-timer or DP/USB Multi-Function MUX/ GPIO |
| | I2C_SCL_SCB2/P2.2 | GPIO | E10 | SCB2 clock for configuring Re-timer or DP/USB Multi-Function MUX/ GPIO |
| | P2.3 | GPIO | E8 | GPIO |
| | I2C_INT_TBT_P1/P0.5 | GPIO | H8 | ThunderBolt interrupt for Port-1 / GPIO |
| | P2.5 | GPIO | D8 | GPIO |
| | I2C_SCL_SCB0/P4.0 | GPIO | D11 | SCB0 clock for communicating with Embedded controller / GPIO |
| | I2C_SDA_SCB0/P4.1 | GPIO | C11 | SCB0 data for communicating with Embedded controller / GPIO |
| | P3.0 | GPIO | B10 | GPIO |
| | I2C_SDA_SCB3/P3.1 | GPIO | B11 | SCB3 data / GPIO |
| I2C_SCL_SCB3/P3.2 | GPIO | B9 | SCB3 clock / GPIO | |
| HPD_P1/P3.3 | GPIO | B8 | Hot Plug Detect I/O for Port-1 / GPIO | |
| Reset | XRES | Analog | C10 | Reset input |
| Power | VBUS_C_P0 | Power | A1,A2,B1,B2,C1 | Type-C VBUS Connector Input for Port-0 (4-V to 21.5-V) |
| | VBUS_C_P1 | Power | J1,K1,K2,L1,L2 | Type-C VBUS Connector Input for Port-1 (4-V to 21.5-V) |
| | VBUS_P_P0 | Power | C2,D1,D2,E1,E2 | VBUS Provider Input for Port-0 (4-V to 5.5-V) |
| | VBUS_P_P1 | Power | G1,G2,H1,H2,J2 | VBUS Provider Input for Port-1 (4-V to 5.5-V) |
| | VSYS | Power | F4 | 2.75-V to 5.5-V supply for the system |
| | VDDD | Power | G7 | VDDD supply output 1. VSYS powered - (Min: VSYS-50 mV) 2.7 to 5.5 2. VBUS powered - 3.0 V to 3.6 V |
| | VDDIO | Power | F7 | At system-level short the VDDD to VDDIO |
| | VCCD | Power | E7 | 1.8-V regulator output for filter capacitor. This pin cannot drive external load. |
| | V5V_P0 | Power | B4 | 4.85-V to 5.5-V supply for VCONN FET of Type-C: Port-0 |
| | V5V_P1 | Power | K4 | 4.85-V to 5.5-V supply for VCONN FET of Type-C: Port-1 |
| Ground | VSSD | Ground | D7, E5, E6, F1, F2, F5, F6, G4, G5, G6 | Ground |

Figure 4. 96-Ball BGA Pin Map (Top View) for CYPD6227-96BZXI

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|-----------|-----------|----------------|-----------------|-----------|-----------------|-------------------|---------------------|---------------------|-------------------|-------------------|
| A | VBUS_C_P0 | VBUS_C_P0 | VBUS_C_CTRL_P0 | SBU2_P0 | SBU1_P0 | SBU2_SYS_P0 | SBU2_SYS_P1 | SBU1_P1 | SBU2_P1 | CSN_P0 | CSP_P0 |
| B | VBUS_C_P0 | VBUS_C_P0 | CC1_P0 | V5V_P0 | CC2_P0 | SBU1_SYS_P0 | SBU1_SYS_P1 | HPD_P1/P3.3 | I2C_SCL_SCB3/P3.2 | P3.0 | I2C_SDA_SCB3/P3.1 |
| C | VBUS_C_P0 | VBUS_P_P0 | | | | | | | | XRES | I2C_SDA_SCB0/P4.1 |
| D | VBUS_P_P0 | VBUS_P_P0 | | | DNU | DNU | VSSD | P2.5 | | P2.4 | I2C_SCL_SCB0/P4.0 |
| E | VBUS_P_P0 | VBUS_P_P0 | | DNU | VSSD | VSSD | VCCD | P2.3 | | I2C_SCL_SCB2/P2.2 | I2C_SDA_SCB2/P2.1 |
| F | VSSD | VSSD | | VSYS | VSSD | VSSD | VDDIO | HPD_P0/P2.0 | | SWD_CLK/P1.0 | I2C_INT_EC/P1.2 |
| G | VBUS_P_P1 | VBUS_P_P1 | | VSSD | VSSD | VSSD | VDDD | SWD_IO/P1.1 | | UART_RX_P0/P1.3 | DP_TOP_P0 |
| H | VBUS_P_P1 | VBUS_P_P1 | | DNU | DNU | DNU | I2C_SCL_SCB1/P0.3 | I2C_INT_TBT_P1/P0.5 | | UART_TX_P0/P1.4 | DM_TOP_P0 |
| J | VBUS_C_P1 | VBUS_P_P1 | | | | | | | | DM_BOT_P0 | DM_SYS_P0 |
| K | VBUS_C_P1 | VBUS_C_P1 | CC2_P1 | V5V_P1 | CC1_P1 | UART_RX_P1/P0.1 | DM_BOT_P1 | DP_BOT_P1 | I2C_SDA_SCB1/P0.2 | DP_BOT_P0 | DP_SYS_P0 |
| L | VBUS_C_P1 | VBUS_C_P1 | VBUS_C_CTRL_P1 | UART_TX_P1/P0.0 | DM_SYS_P1 | DP_SYS_P1 | DM_TOP_P1 | DP_TOP_P1 | I2C_INT_TBT_P0/P0.4 | CSN_P1 | CSP_P1 |

| |
|---------------|
| Type-C Port 1 |
| Type-C Port 2 |
| Power Pins |
| GND |
| GPIOs |

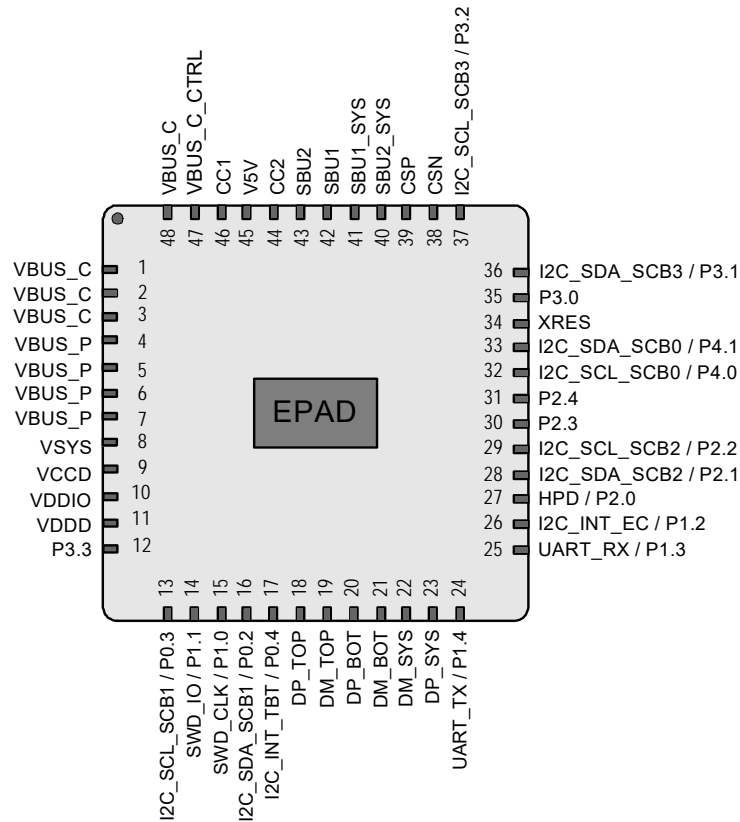
Table 3. Pinout for CYPD6127-48LQXI

| Group Name | Pin Name | Port | Pin | Description |
|-----------------------------|-------------------|--------|-----|---|
| USB Type-C | CC1 | Analog | 46 | USB PD connector detect/Configuration Channel 1 |
| | CC2 | Analog | 44 | USB PD connector detect/Configuration Channel 2 |
| Mux | DP_SYS | Analog | 23 | USB 2.0 DP from the Host System |
| | DM_SYS | Analog | 22 | USB 2.0 DM from the Host System |
| | UART_TX/P1.4 | GPIO | 24 | UART Tx from Host System/GPIO |
| | UART_RX/P1.3 | GPIO | 25 | UART Rx from Host System/GPIO |
| | DP_BOT | Analog | 20 | USB 2.0 DP from Bottom of Type-C Connector |
| | DM_BOT | Analog | 21 | USB 2.0 DM from Bottom of Type-C Connector |
| | DM_TOP | Analog | 19 | USB 2.0 DM from Top of Type-C Connector |
| | DP_TOP | Analog | 18 | USB 2.0 DP from Top of Type-C Connector |
| | SBU2 | Analog | 43 | Type-C Sideband Use signal – Connector side |
| | SBU1 | Analog | 42 | Type-C Sideband Use signal – Connector side |
| | SBU1_SYS | Analog | 41 | Type-C Sideband Use signal – System side |
| | SBU2_SYS | Analog | 40 | Type-C Sideband Use signal – System side |
| VBUS Control | VBUS_C_CTRL | Analog | 47 | Full rail control I/O for enabling/disabling Consumer load NFET of USB Type-C |
| VBUS OCP | CSP | Analog | 39 | Current Sense Positive Input for VBUS side external Rsense |
| | CSN | Analog | 38 | Current Sense Negative input for other side of external Rsense |
| GPIOs and Serial Interfaces | I2C_SDA_SCB1/P0.2 | GPIO | 16 | SCB1 data / GPIO |
| | I2C_SCL_SCB1/P0.3 | GPIO | 13 | SCB1 clock / GPIO |
| | I2C_INT_TBT/P0.4 | GPIO | 17 | ThunderBolt interrupt / GPIO |
| | I2C_INT_EC/P1.2 | GPIO | 26 | Embedded Controller interrupt / GPIO |
| | SWD_IO/P1.1 | GPIO | 14 | Serial Wire Debug I/O / GPIO |
| | SWD_CLK/P1.0 | GPIO | 15 | Serial Wire Debug Clock / GPIO |
| | HPD/P2.0 | GPIO | 27 | Hot Plug Detect I/O / GPIO |
| | I2C_SDA_SCB2/P2.1 | GPIO | 28 | SCB2 data / GPIO |
| | I2C_SCL_SCB2/P2.2 | GPIO | 29 | SCB2 clock / GPIO |
| | P2.3 | GPIO | 30 | GPIO |
| | P2.4 | GPIO | 31 | GPIO |
| | I2C_SCL_SCB0/P4.0 | GPIO | 32 | SCB0 clock / GPIO |
| | I2C_SDA_SCB0/P4.1 | GPIO | 33 | SCB0 data / GPIO |
| | P3.0 | GPIO | 35 | GPIO |
| | I2C_SDA_SCB3/P3.1 | GPIO | 36 | GPIO |
| | I2C_SCL_SCB3/P3.2 | GPIO | 37 | GPIO |
| | P3.3 | GPIO | 12 | GPIO |
| Reset | XRES | Analog | 34 | Reset input |

Table 3. Pinout for CYPD6127-48LQXI (continued)

| Group Name | Pin Name | Port | Pin | Description |
|------------|----------|--------|----------|--|
| Power | VBUS_C | Power | 1,2,3,48 | Type-C VBUS Connector Input (4-V to 21.5-V) |
| | VBUS_P | Power | 4,5,6,7 | VBUS Provider Input (4-V to 5.5-V) |
| | VSYS | Power | 8 | 2.75-V to 5.5-V Supply for the System |
| | VDDD | Power | 11 | VDDD supply output 1. VSYS powered - (Min: VSYS-50 mV) 2.7 to 5.5 2. VBUS powered - 3.0 V to 3.6 V |
| | VDDIO | Power | 10 | At system-level short the VDDD to VDDIO |
| | VCCD | Power | 9 | 1.8-V regulator output for filter capacitor. This pin cannot drive external load. |
| | V5V | Power | 45 | 4.85-V to 5.5-V supply for VCONN FET of Type-C |
| Ground | - | Ground | EPAD | Ground |

Figure 5. 48-pin QFN Pin Map for CYPD6127-48LQXI



Application Diagrams

The CCG6DF device communicates with the embedded controller (EC), which manages the Battery Charger Controller (BCC) to control the charging and discharging of the internal battery. It also updates the Thunderbolt Controller via I²C to route the HighSpeed signals coming from the Type-C port to the USB host (during normal mode) or the Graphics processor unit (during Display port Alternate mode) or the Thunderbolt Host (during Thunderbolt Alternate mode) based on the alternate mode negotiation.

The CCG6DF device controls the transfer of USB 2.0 DP and DM lines from the top and bottom of the Type-C receptacle to the DP and DM lines of the USB Host controller. CCG6DF offers VBUS Short protection on SBU and CC lines.

The CCG6DF device has integrated VCONN FETs for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. The 5-mΩ resistor between the 5-V supply and the integrated provider FETs is used for overcurrent detection on the VBUS.

Figure 6 illustrates a Dual Port Thunderbolt Notebook DRP application diagram using CYPD6227-96BZXI.

Figure 6. CCG6DF Dual Port Thunderbolt Notebook Application Diagram

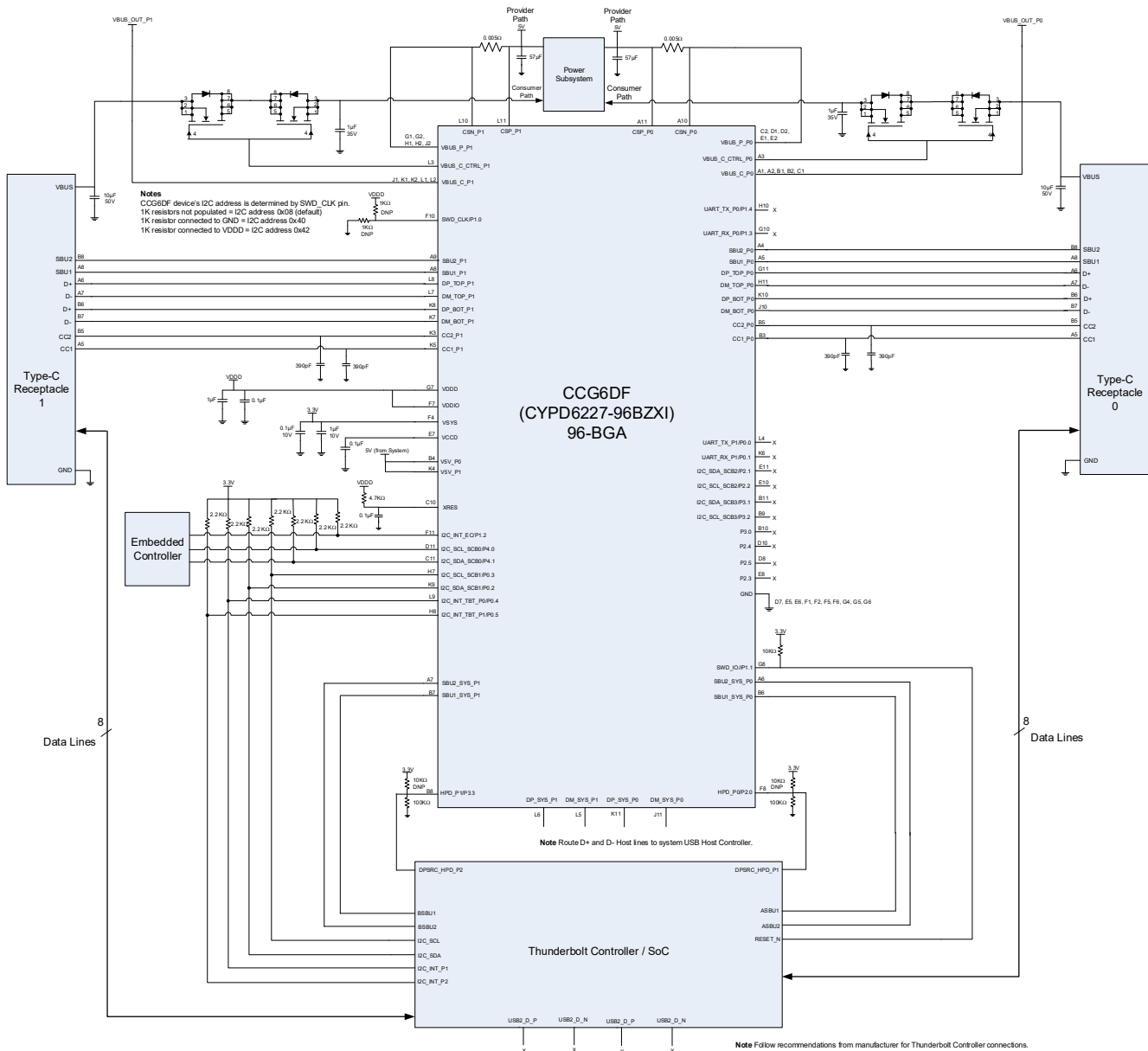
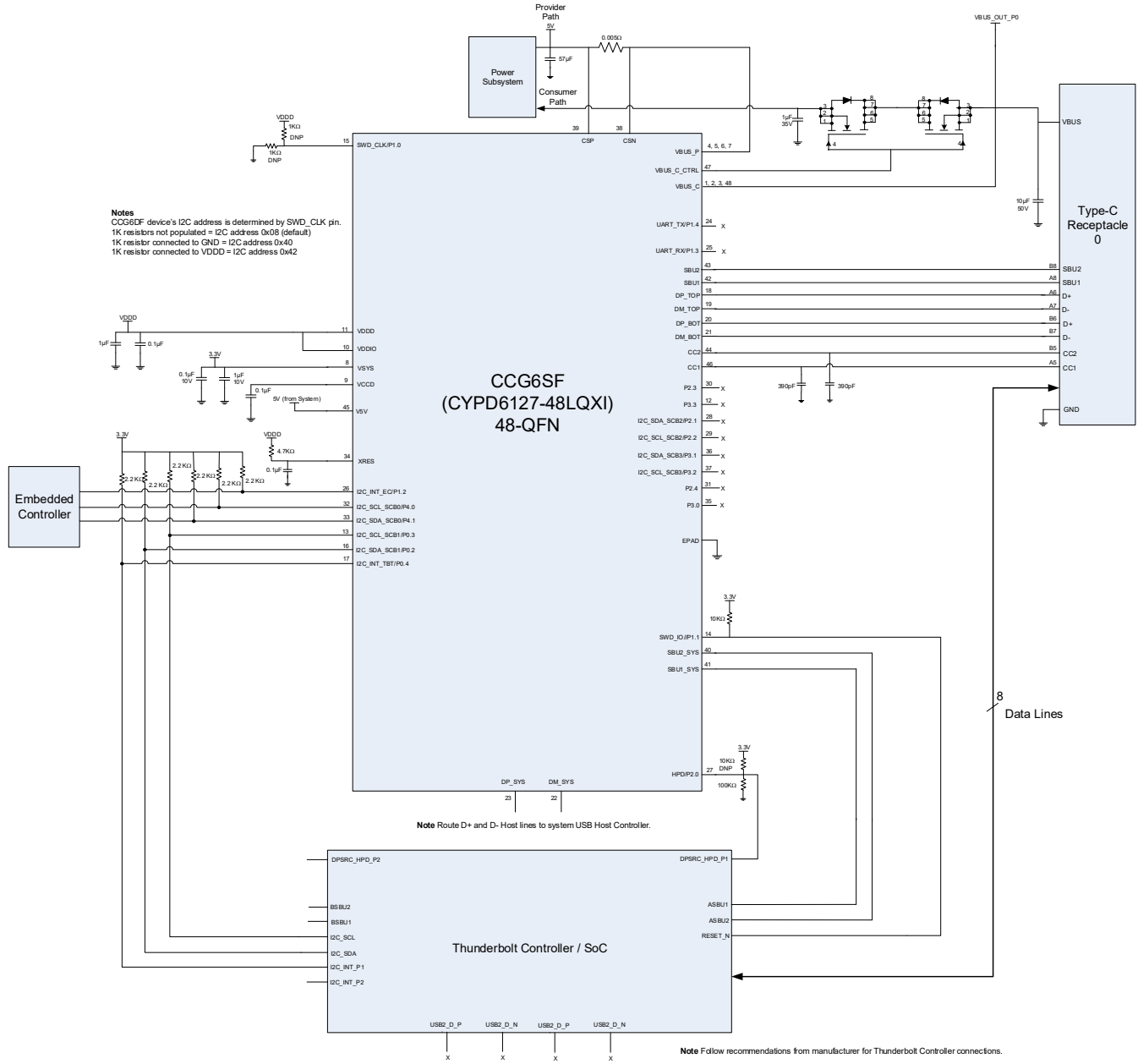


Figure 7 illustrates a Single-Port Thunderbolt Notebook DRP application diagram using CYPD6127-48LQXI.

Figure 7. CCG6SF 48-pin QFN Single Port Thunderbolt Notebook Application Diagram

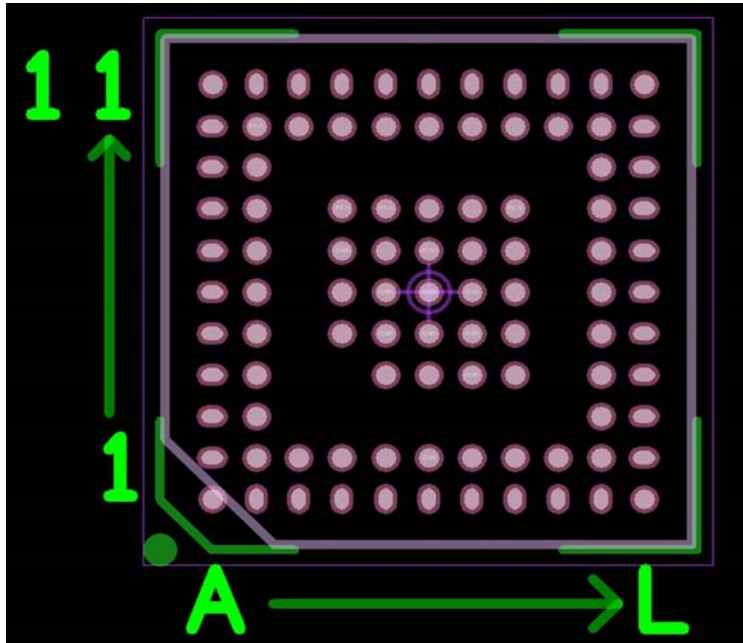


CCG6DF Layout Design Guidelines for BGA Package

Proper routing and placement help to maintain signal integrity for high-speed signals, improve thermal dissipation and reduce power consumption for CCG6DF/SF. The combination of power and high-speed data signals can be better routed if these design guidelines are followed. It is highly recommended to consult with a PCB manufacturer to verify the manufacturing capabilities to propose the right design guidelines. This section provides layout recommendations which are applicable to both CCG6DF and CCG6SF devices.

Figure 8 shows the CCG6DF 96-BGA device footprint that is recommended. The footprint has oval-shaped pads in specific locations. It is recommended to use oval pads in order to reduce the manufacturing cost by eliminating a High Density Interconnector (HDI) board processing. This method allows the PCB designer to route the inner perimeter balls through the top layer. The balls around the perimeter have their pads in an oval shape with the exception of the corner balls. This footprint is recommended for MDI (Medium Density) PCB designs that are generally less expensive to build.

Figure 8. Top View Standard Footprint (Recommended) for CCG6DF, CCG6SF 96-BGA

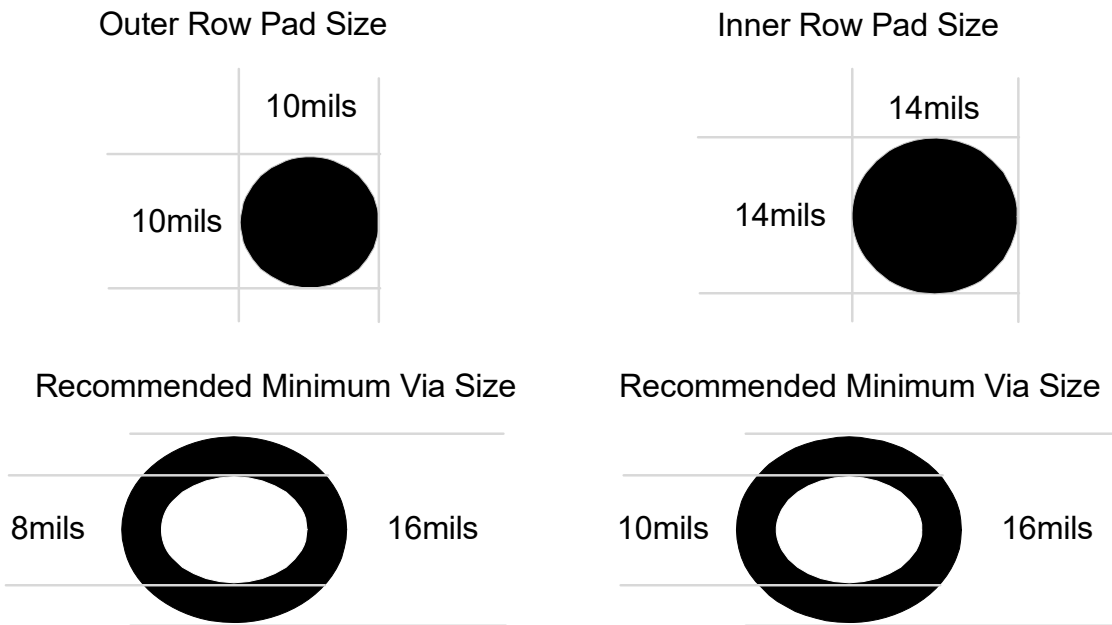


Usage of Via Size of 8-mil drill/16-mil Diameter and 10-mil drill/16-mil Diameter

In order to use larger via size of 8/16 (8-mil drill and 16-mil diameter) or 10/16 (10-mil drill and 16-mil diameter), one GPIO (BGA pad D8) is unusable and should be left unconnected. This would free up space underneath the package. This is a critical factor that helps to decide the minimum drill size for the vias. Two different pad sizes for the BGA balls are recommended for better yield in terms of assembly. Note that if GPIO pad D8 cannot be freed up, 6 mil hole / 12 mil diameter via sizes can be used to do PCB trace routing.

Via size of greater than 10-mil drill and 16-mil diameter is not feasible for inner BGA pads. Drill hole size of greater than 10-mils overlaps with the BGA pads and may result in "cold solder" during SMT reflow. Figure 9 shows the recommended 8/16 and 10/16 minimum via sizes (8-mil drill and 16-mil diameter).

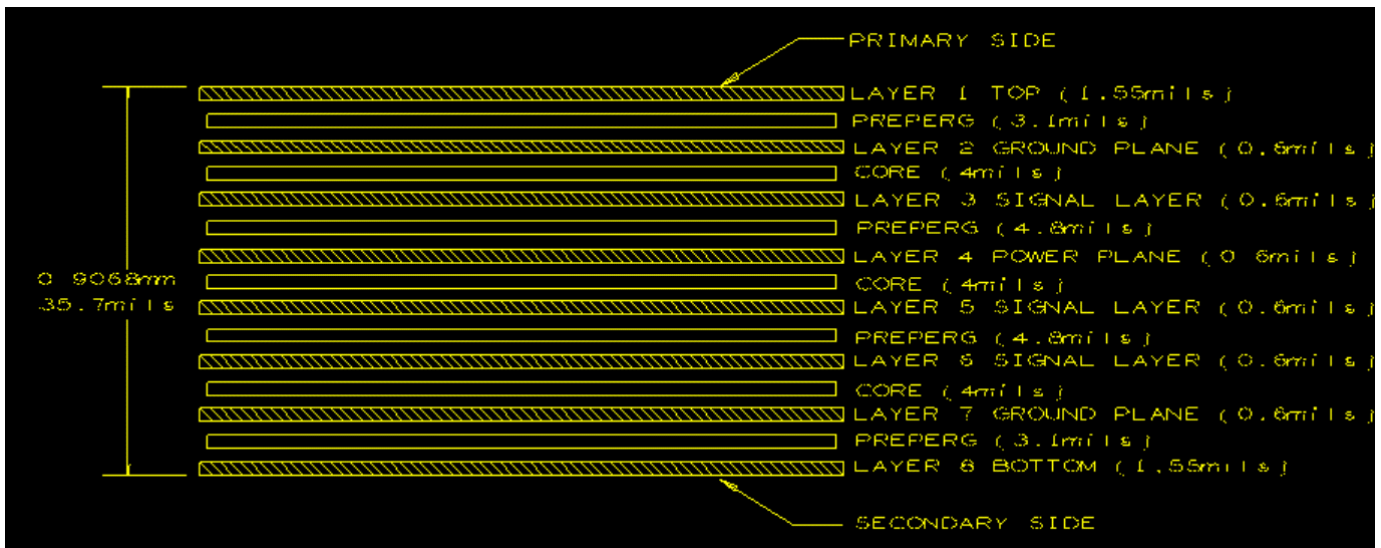
Figure 9. Recommended Pad Size and Via Size (8/16 and 10/16)



Layer Stack-up

A typical 8-layer stack up with 1 oz of copper is shown in Figure 10.

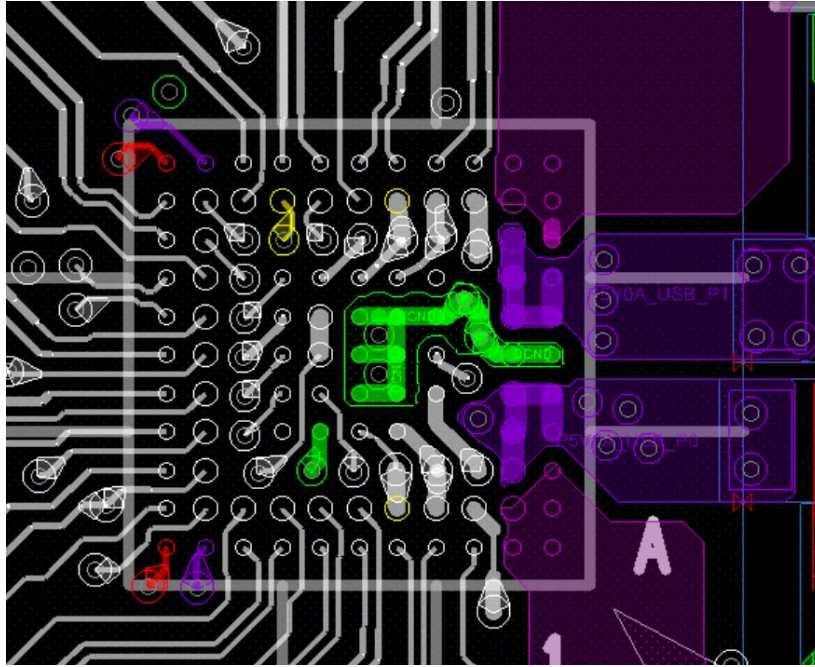
Figure 10. Eight Layer Stack-Up



Top Layer Fanout

Figure 11 shows a method of routing inner BGA balls and fan-out method for the routing for 8/16 or 10/16 via sizes.

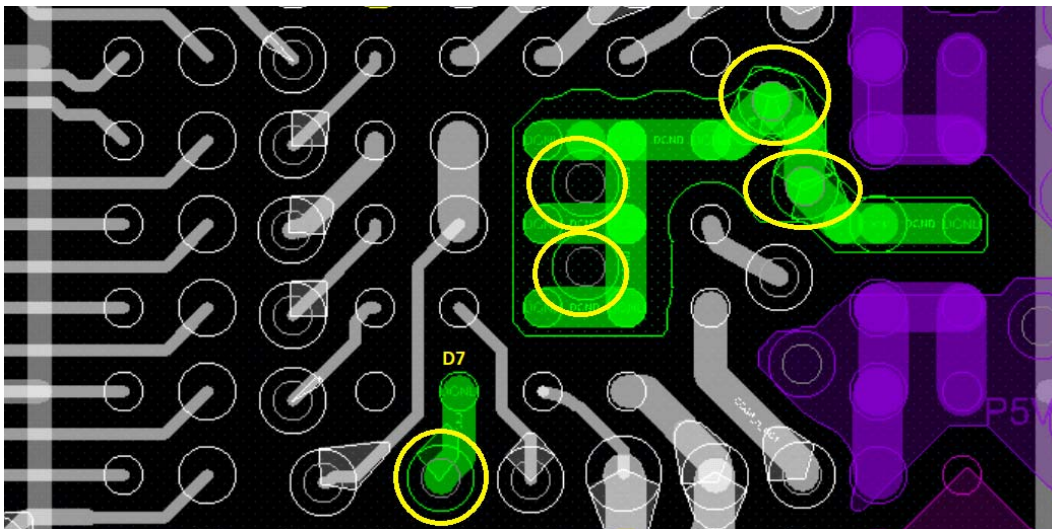
Figure 11. Top Layer Fanout (8/16 or 10/16 via sizes)



Via Count for GND Pads

Each via has a thermal resistance of 219 °C/W. Adding three such vias will help reducing thermal resistance to 73 °C/W and would help to distribute the heat better. As shown in Figure 12, it is recommended to short the 6 GND pads with a small split plane on the top layer and have a minimum of two vias to meet the thermal performance. Elevated temperature of more than 100 °C on BGA top may be observed if the via count is lesser than recommended. It is also recommended to have one via on GND pad (D7) with a trace width of 7 mils.

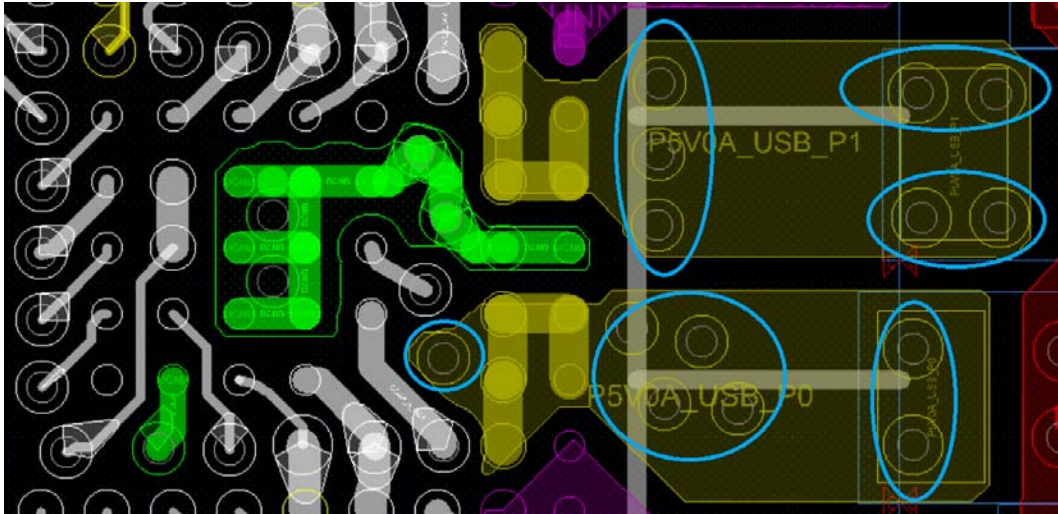
Figure 12. Via Count for GND Pads (8/16 or 10/16 via sizes)



Via Count for Provider Pads

As shown in [Figure 13](#), it is recommended to create a copper pour around the 5 provider pads on the top and bottom layers with minimum of 7 vias. It is also recommended to split the power plane on other layer to meet the thermal performance. These vias play a crucial role in dissipating the heat better.

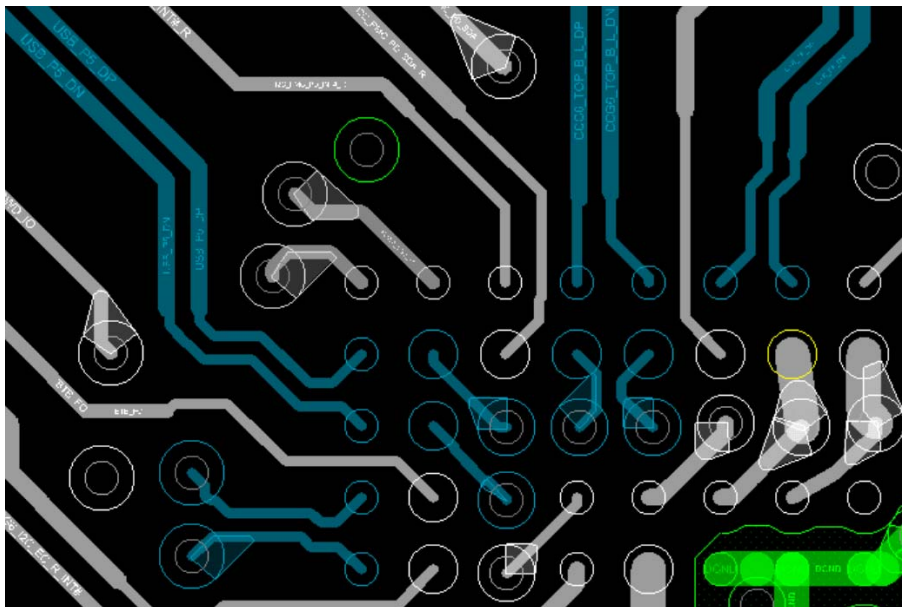
Figure 13. Via Count for Provider Pads (8/16 or 10/16 via sizes)



High-Speed (DP_SYS, DM_SYS) USB Connections

The traces of DP and DM lines with via size of 8-mil drill, 16-mil diameter and 10-mil drill, 16-mil diameter are shown in [Figure 14](#).

Figure 14. DP/DM Traces (8/16 or 10/16 via sizes)



Rsense and Capacitor Connections for Provider VBUS

It is always advisable to keep the sense resistor (Rsense) close to CCG6DF/CCG6SF as it has internal VBUS provider switch. Connection from the regulator to Rsense should be done using big copper shape (pour) for carrying high currents.

The longer the trace length between components, the higher the voltage drop between components. The additional resistance reduces efficiency of the system. The resistance of trace can be calculated from below equation.

$$R_{trace} = \rho \times \frac{Tracelength}{Tracewidth \times Tracethickness}$$

Where the bulk resistance ρ , of copper is $0.67 \mu\Omega/in$ or $1.7 \mu\Omega/cm$ at $25^\circ C$.

The differential signal from Rsense should be length matched. The capacitor for Provider VBUS should be as close as possible to the Rsense and connected using copper shape. Figure 15 and Figure 16 show routing for Rsense.

Figure 15. Rsense Resistor Placement (Top Layer)

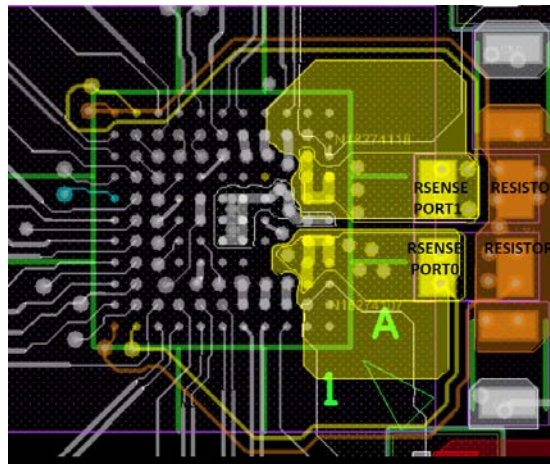
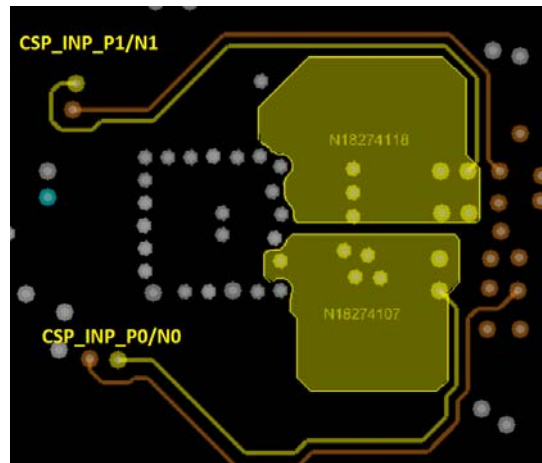


Figure 16. Rsense Resistor Trace Routing with Kelvin Connection (Inner Layer)



Trace Width Details for Critical Signals

Table 4 provides information on routing trace width for this layout example.

Table 4. Route Trace Width

| Route | Route Width (mils) (1-oz Copper Thickness) | Remarks / Key Feature / Constraints |
|-------------------|---|-------------------------------------|
| CC1, CC2 | 8 | Current rating = 500 mA |
| GPIOs | 5 | - |
| DP/DM/Dsys | 6 mils width/ 8mils spacing | 90-Ω impedance signals |
| V _{DDIO} | 10 | Current rating = 15 mA |
| V _{DDD} | | Current rating = 20 mA |
| V _{CCD} | | |
| V _{SYS} | | |
| V5V | | |

V_{DDIO}, V_{CCD}, V_{SYS}, and V_{DDD} Connections

Figure 17 and Figure 18 show how the V_{DDIO}, V_{DDD}, V_{SYS}, and V_{CCD} signals get routed amongst the top and bottom layers.

Figure 17. Top Layer Connection for V_{DDIO}, V_{DDD}, V_{SYS} and V_{CCD}

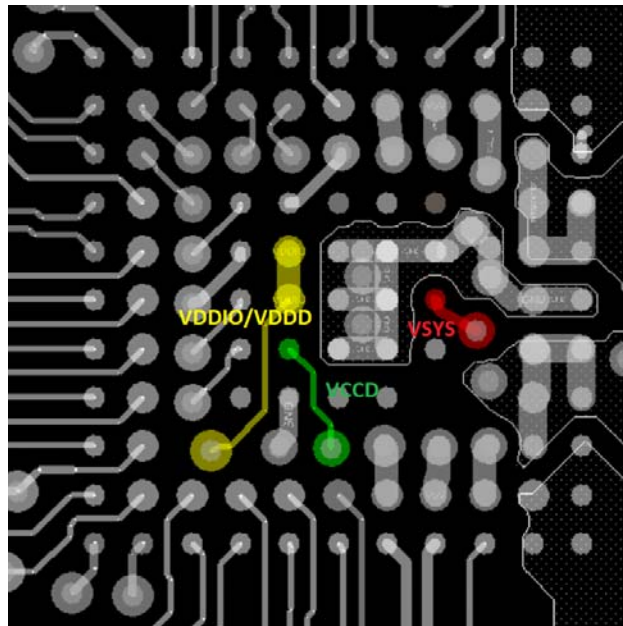
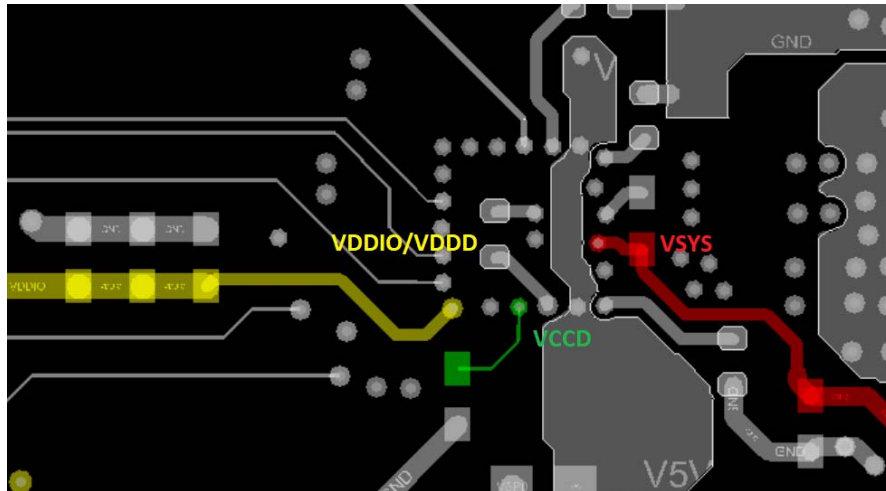


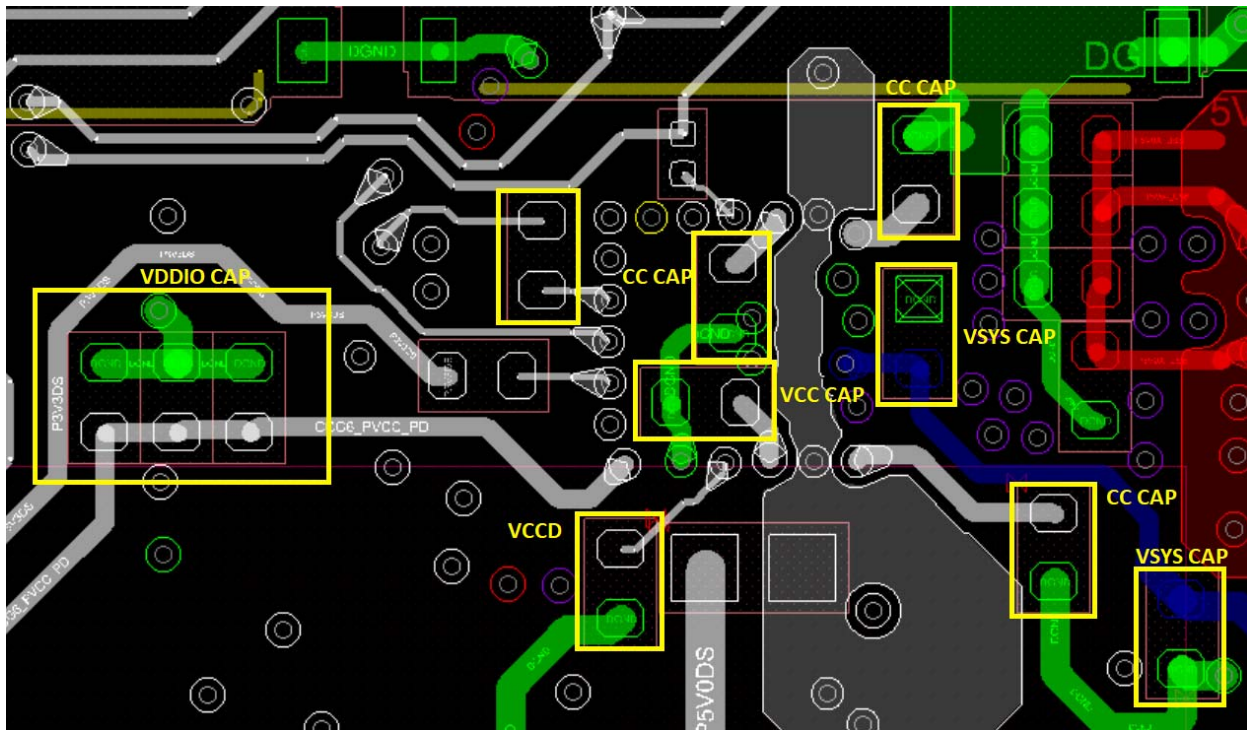
Figure 18. Bottom Layer Connection for V_{DDIO} , V_{DDD} , V_{SYS} and V_{CCD}



Capacitor Connections for CC Lines and Bypass Capacitors for V_{DDIO} , V_{DDD} , V_{CCD} , and V_{SYS} Pins

Figure 19 shows how the relevant capacitors can be placed for via sizes of 8-mil drill, 16-mil diameter or 10-mil drill, 16-mil diameter.

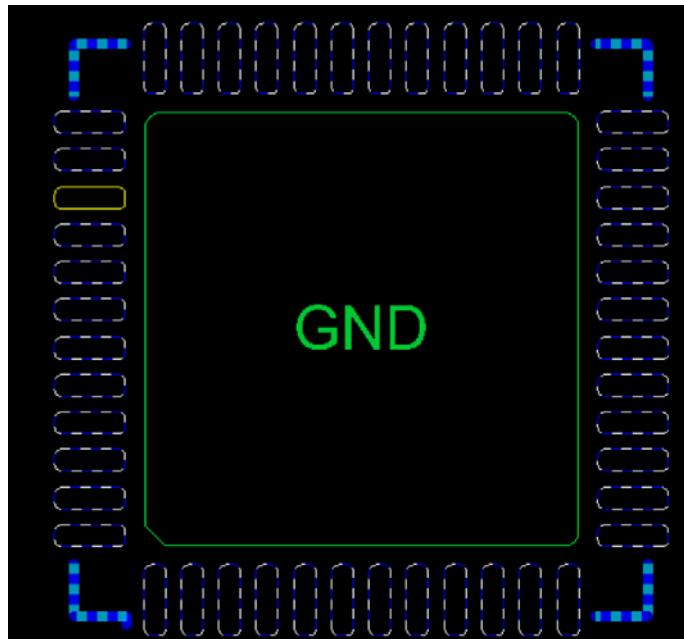
Figure 19. Capacitor Connections (Top and Bottom Layer Placements for 8/16 or 10/16 via size)



CCG6SF Layout Design Guidelines for 48-QFN Package

Figure 20 shows the CCG6SF 48-QFN device footprint that is recommended. The footprint has rectangular shaped pads in all pins of this package. It is recommended to use rectangular pads to reduce the manufacturing cost by eliminating a HDI board processing.

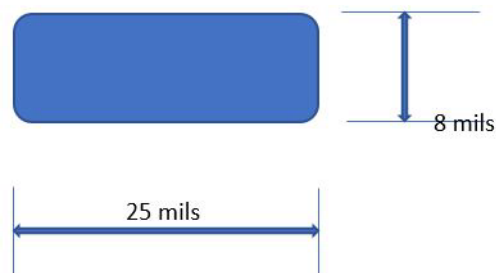
Figure 20. Top View Standard Footprint (Recommended) for CCG6SF 48-QFN



Recommended Pad Size

Figure 21 is the recommended pad size for the QFN package.

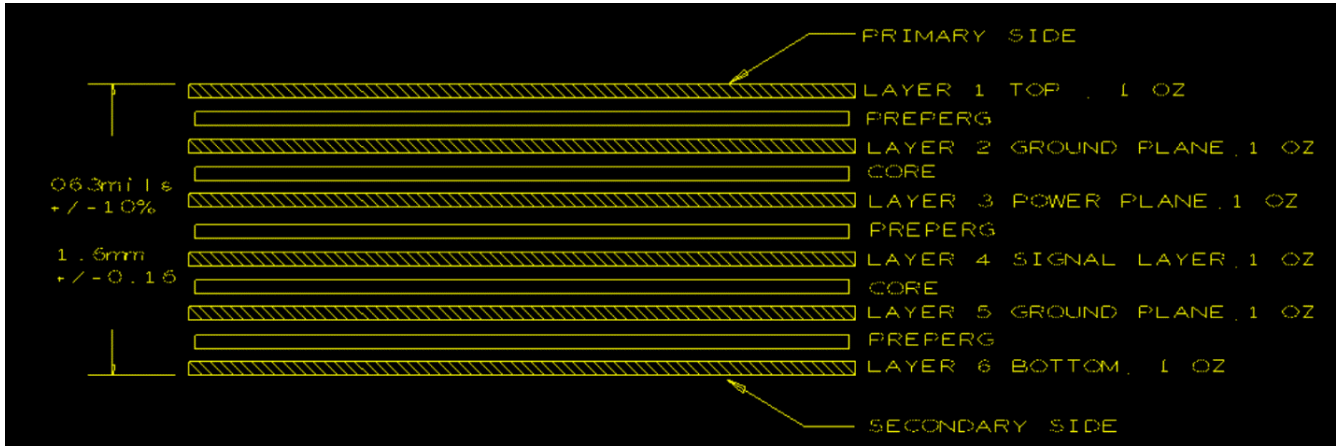
Figure 21. QFN Pad Size



Stackup

Figure 22 shows a typical 6-layer stack up with 1 oz of copper.

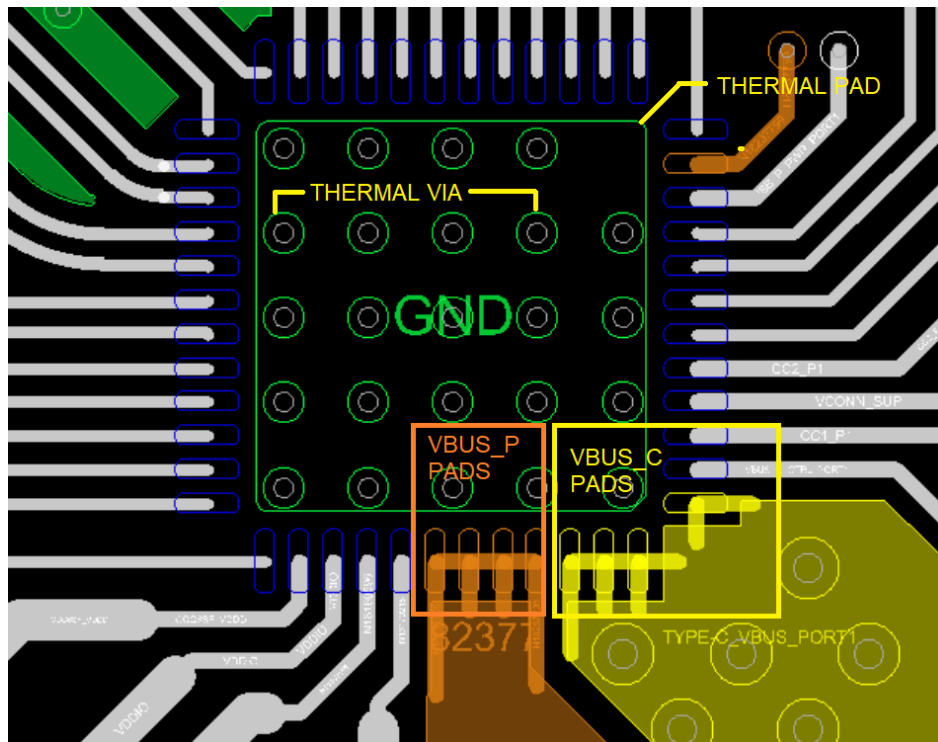
Figure 22. Six Layer Stack-up



48-QFN Fanout

CCG6SF 48-QFN device uses 5 mil trace width for all the QFN pads and complies to MDI standards. It is better to use 5 mil trace on each of VBUS provider input (VBUS_P) pads and Type-C VBUS connector input (VBUS_C) pads and then connect with corresponding power shape. Otherwise, wider trace width would have Non-solder mask between the pads and results in alignment issue during assembly.

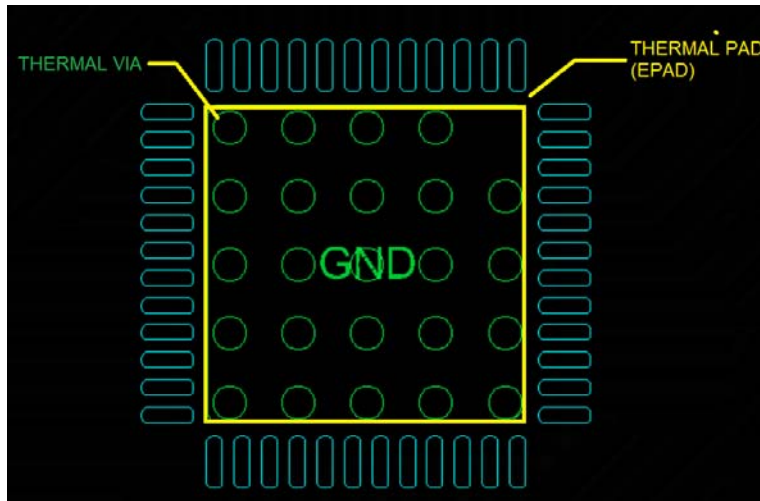
Figure 23. QFN Fanout with Thermal vias



Via Count on Thermal Pads

As shown in Figure 24, CCG6SF 48-QFN device has 5 × 5 via array (25 vias) on the thermal pads. It is recommended to have minimum of 4 × 4 via array (16 vias) on the thermal pads to meet the thermal performance. Via array means number of vias present on row and column of the EPAD. Each Via size should be minimum of 10mil drill and 20mil diameter. Each via has a thermal resistance of 179 °C/W. Adding 4 × 4 vias will help reducing thermal resistance to (179/16 vias) 11 °C/W and would help to distribute the heat better. Lesser the thermal resistance better the thermal performance. Power plane is required on this path to able to carry ~6A of current.

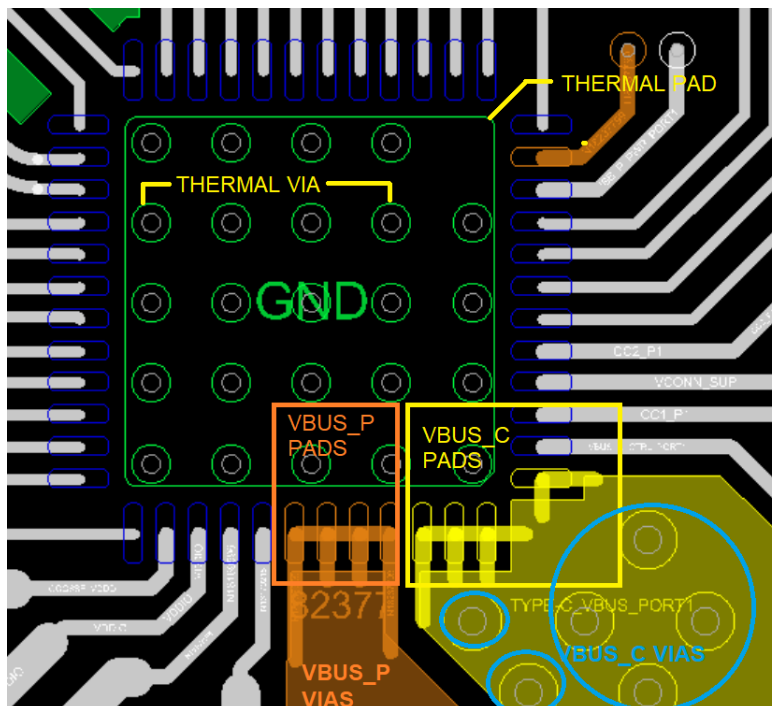
Figure 24. Thermal Pad (EPAD) and Thermal Via



Via Count for VBUS_P and VBUS_C Pads

As shown in Figure 25, it is recommended to create a copper pour around the VBUS_P and VBUS_C pads on the top and bottom layers with minimum of 6 vias. It is also recommended to split the power plane on other layer to meet the thermal performance. These vias play a crucial role in dissipating the heat better.

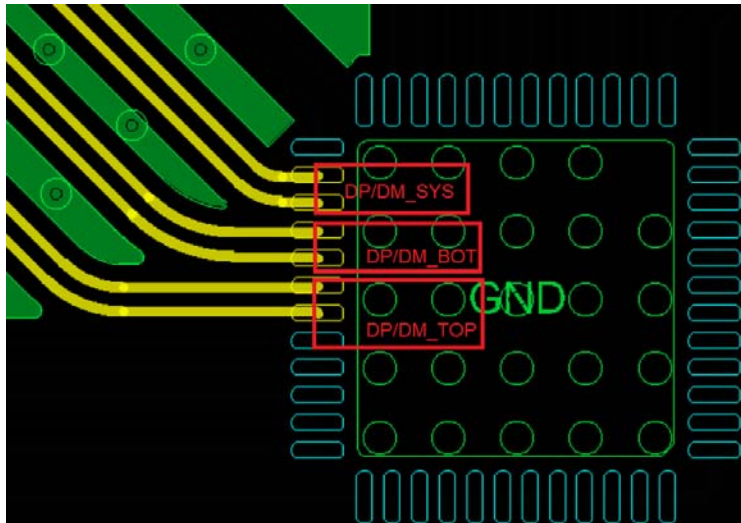
Figure 25. Via Count for VBUS_P and VBUS_C (8/16 or 10/16 via sizes)



High-Speed (DP/DM_SYS, DP/DM_BOT, DP/DM_TOP) USB Connections Fanout

Figure 26 shows differential fanout. The DP/DM lines from CCG6SF to connector should be differentially routed and length match $\pm 10\%$ tolerance. It should maintain 90- Ω impedance.

Figure 26. Differential Fanout



CC Connections

CC lines for CCG6DF/CCG6SF devices carry ~500-mA current. It is recommended to have 0.15 mm trace width for CC1, CC2 and V5V pads. The capacitors are placed on bottom layer and are routed to the Type-C Connector. The CC1 and CC2 fanout is shown in Figure 27 and Figure 28.

Figure 27. CC1 and CC2 Fanout

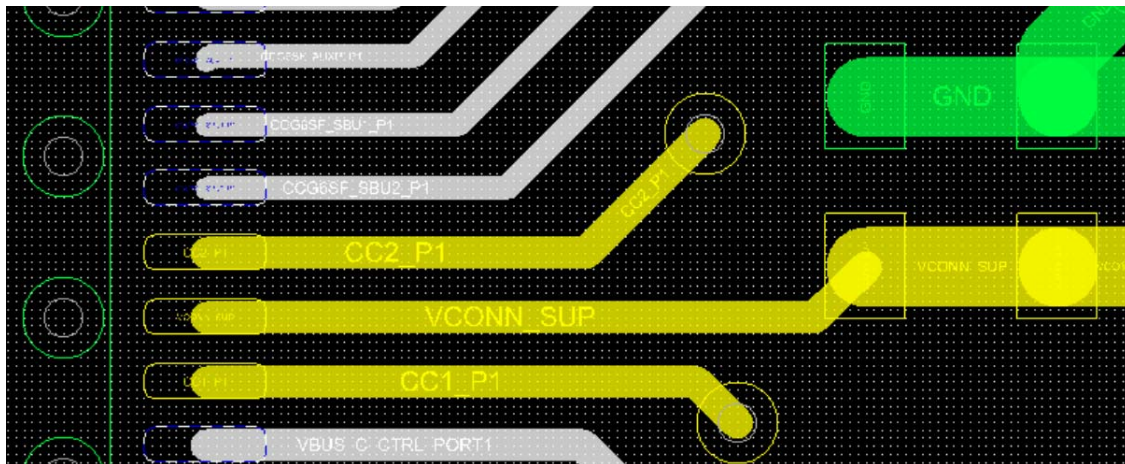
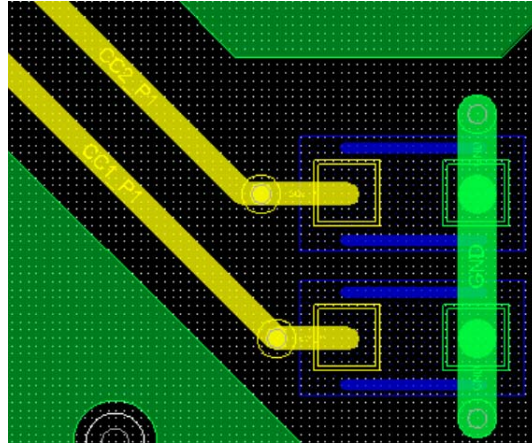


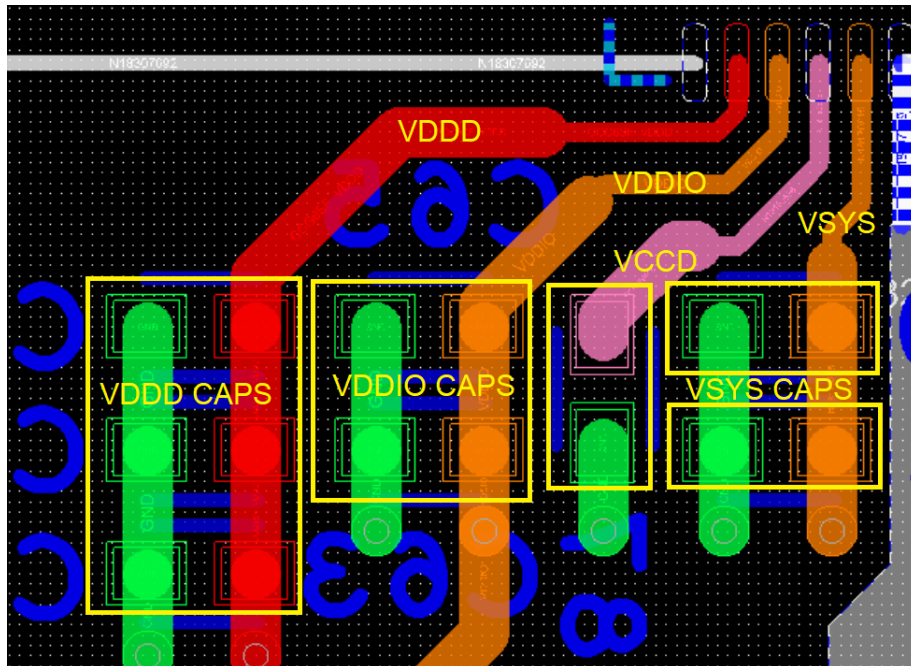
Figure 28. CC1 and CC2 Caps



V_{DDIO}, V_{CCD}, V_{SYS}, and V_{DDD} Connections

Figure 29 shows how the V_{DDIO}, V_{DDD}, V_{SYS}, and V_{CCD} signals get routed amongst the top and bottom layers.

Figure 29. V_{DDIO}, V_{CCD}, V_{SYS}, and V_{DDD} Connections



Electrical Specifications

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings^[4]

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions | |
|-----------------------------|---|---------------------|-----|-------------------------|------|--|---|
| V _{SYS_MAX} | Supply relative to V _{SS} | – | – | 6 | V | – | |
| V _{5V_MAX} | Max supply voltage relative to V _{SS} | – | – | 6 | | | |
| V _{BUS_C} | V _{BUS} voltage relative to V _{SS} | -0.3 ^[5] | – | 24 | | | |
| V _{DDIO_MAX} | Max supply voltage relative to V _{SS} | – | – | V _{DDIO} | | | |
| V _{GPIO_ABS} | Inputs to GPIO, DP/DM mux (UART, SYS, DP/DM_top/bot pins), SBU mux (SBU1/2 pins) | -0.5 | – | V _{DDIO} + 0.5 | | | |
| I _{GPIO_ABS} | Maximum current per GPIO | -25 | – | 25 | mA | – | |
| I _{GPIO_INJECTION} | GPIO injection current, Max for V _{IH} > V _{DDIO} , and Min for V _{IL} < V _{SS} | -0.5 | – | 0.5 | | Absolute max, current injected per pin | |
| ESD_HBM | Electrostatic discharge human body model | 2200 | – | – | V | Applicable for all pins except SBU1_P0/1, SBU2_P0/1, CC1_0/1, CC2_0/1, VBUS_P_P0/1 & VBUS_C_P0/1 pins. | |
| ESD_HBM_SBU | Electrostatic discharge human body model for SBU1, SBU2 pins | 1100 | – | – | | Only applicable to SBU1_P0/1, SBU2_P0/1 pins | |
| ESD_HBM_CC | Electrostatic discharge human body model for CC1 and CC2 pins for both ports | 1100 | – | – | | Only applicable to CC1_P0/1, CC2_P0/1 pins | |
| ESD_CDM | Electrostatic discharge charged device model | 500 | – | – | | Charged Device Model ESD | |
| ESD_HBM_VBUS | Electrostatic discharge human body model for VBUS_P_P0/1 & VBUS_C_P0/1 pins | 500 | – | – | V | Only applicable to VBUS_P_P0/1 and VBUS_C_P0/1 pins | |
| LU | Pin current for latch-up | -100 | – | 100 | mA | – | |
| VCC_PIN_ABS | Max voltage on CC1 and CC2 pins | – | – | 24 | | V | – |
| VSBU_PIN_ABS | Max voltage on SBU1 and SBU2 pins | – | – | 24 | | | – |
| VGPIO_OVT_ABS | OVT pins (16, 17) voltage | -0.5 | – | 6 | – | | |
| T _A | Internal system ambient temperature | -40 | – | 55 | °C | Ambient temp inside system enclosure | |
| T _J | Junction temperature | -40 | – | 125 | | – | |

Notes

- Usage above the absolute maximum conditions listed in Table 5 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
- In a system, if the negative spike exceeds the minimum voltage specified here, it is recommended to add Schottky diode to clamp the negative spike.

Device-Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 55\text{ }^{\circ}\text{C}$ and $T_J \leq 125\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

DC Specifications
Table 6. DC Specifications (Operating Conditions)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--|----------------------------|---|-------------------------|-----|------------------|---------------|--|
| SID.PWR#23 | $V_{\text{SYS_UFP}}$ | VSYS valid range | 2.75 | – | 5.5 | V | UFP applications |
| SID.PWR#23_A | $V_{\text{SYS_UFP_DRP}}$ | – | 3 | – | 5.5 | | DFP/DRP applications |
| SID.PWR#22 | $V_{\text{BUS_C}}$ | $V_{\text{BUS_C}}$ Port 0/1 valid range | 4 | – | 21.5 | | – |
| SID.PWR#22A | $V_{\text{BUS_MAX}}$ | Max $V_{\text{BUS_C_P0/1}}$ voltage relative to V_{SS} | – | – | 24 | | –40 °C to +55 °C T_A , Absolute Maximum A far-end short through cable resulting in a maximum of 30V allowed with the following conditions: a. Max pulse-width of 2 at 27V b. No more than 1000 times during the entire life-cycle |
| SID.PWR#24 | $V_{\text{BUS_P}}$ | $V_{\text{BUS_P}}$ Port 0/1 valid range | 4.9 | – | 5.5 | | This is not a power pin. |
| SID.PWR#1 | V_{DDD} | Regulated output voltage when V_{SYS} powered | $V_{\text{SYS}} - 0.05$ | – | V_{SYS} | | –40 °C $\leq T_A \leq$ +55 °C |
| SID.PWR#1_A | V_{DDD} | Regulated output voltage when V_{BUS} powered | 3 | – | 3.65 | | –40 °C $\leq T_A \leq$ +55 °C |
| SID.PWR#26 | V_{5V} | – | 4.85 | – | 5.5 | | – |
| SID.PWR#13 | V_{DDIO} | Supply voltage for I/O | V_{DDD} | – | V_{DDD} | | –40 °C $\leq T_A \leq$ +55 °C, All V_{DDD} |
| SID.PWR#24 | V_{CCD} | Regulated output voltage (for Core Logic) | – | 1.8 | – | | – |
| SID.PWR#15 | C_{EFC} | Regulator bypass capacitor for V_{CCD} | – | 100 | – | nF | X5R ceramic |
| SID.PWR#16 | C_{EXC} | Power Supply decoupling capacitor for V_{DDD} | – | 1 | – | μF | |
| Active Mode, $V_{\text{SYS}} = 2.75\text{ V to }5.5\text{ V}$. Typical values measured at $V_{\text{SYS}} = 3.3\text{ V}$ | | | | | | | |
| SID.PWR#4 | I_{DD12} | Supply current | – | 10 | – | mA | $T_A = 25\text{ }^{\circ}\text{C}$, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, PD port active |
| Deep Sleep Mode, $V_{\text{SYS}} = 2.75\text{ V to }3.6\text{ V}$ | | | | | | | |
| SID34 | I_{DD29} | $V_{\text{SYS}} = 2.75\text{ to }3.6\text{ V}$, I ² C, wakeup and WDT on. | – | 150 | – | μA | $V_{\text{SYS}} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$ |
| SID_DS1 | $I_{\text{DD_DS1}}$ | $V_{\text{SYS}} = 3.3\text{ V}$, CC wakeup on, Type-C not connected. | – | 200 | – | μA | Power source = V_{SYS} , Type-C not attached, CC enabled for wakeup, R_P and R_D connected at 70-ms intervals by CPU. R_D connection should be enabled by both PD ports. |
| SID_DS3 | $I_{\text{DD_DS2}}$ | $V_{\text{SYS}} = 3.3\text{ V}$, CC wakeup on, DP/DM, SBU ON with NGDO/CSA/UVOV On | – | 500 | – | | One Port attached, Chip in Deep-sleep |
| XRES Current | | | | | | | |
| SID307 | $I_{\text{DD_XR}}$ | Supply current while XRES asserted | – | 130 | – | μA | Power Source = $V_{\text{SYS}} = 3.3\text{ V}$, Type-C Not Attached, $T_A = 25\text{ }^{\circ}\text{C}$ |

CPU
Table 7. CPU Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|------------------------|---|-----|-----|-----|------|--|
| SID.CLK#4 | F _{CPU} | CPU input frequency | – | – | 48 | MHz | –40 °C ≤ T _A ≤ +55 °C, All V _{DDD} |
| SID.PWR#21 | T _{DEEPSLEEP} | Wakeup from Deep Sleep mode | – | 35 | – | μs | Guaranteed by characterization |
| SYS.XRES#5 | T _{XRES} | External reset pulse width | 5 | – | – | | |
| SYS.FES#1 | T _{PWR_RDY} | Power-up to “Ready to accept I ² C/CC command” | – | 5 | 25 | ms | |

GPIO
Table 8. GPIO DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-------------|---------------------------|--|--------------------------|-----|-------------------------|------|---|
| SID.GIO#37 | V _{IH_CMOS} | Input voltage HIGH threshold | 0.7 × V _{DDIO} | – | – | V | CMOS input |
| SID.GIO#38 | V _{IL_CMOS} | Input voltage LOW threshold | – | – | 0.3 × V _{DDIO} | | |
| SID.GIO#39 | V _{IH_VDDIO2.7-} | LVTTL input, V _{DDIO} < 2.7 V | 0.7 × V _{DDIO} | – | – | | – |
| SID.GIO#40 | V _{IL_VDDIO2.7-} | LVTTL input, V _{DDIO} < 2.7 V | – | – | 0.3 × V _{DDIO} | | – |
| SID.GIO#41 | V _{IH_VDDIO2.7+} | LVTTL input, V _{DDIO} ≥ 2.7 V | 2.0 | – | – | | – |
| SID.GIO#42 | V _{IL_VDDIO2.7+} | LVTTL input, V _{DDIO} ≥ 2.7 V | – | – | 0.8 | | – |
| SID.GIO#33 | V _{OH_3V} | Output voltage HIGH level | V _{DDIO} – 0.6 | – | – | V | I _{OH} = –4 mA at 3-V V _{DDIO} |
| SID.GIO#35C | V _{OL1_20mA} | Output low voltage | – | – | 0.4 | | I _{OL} = 20 mA, V _{DDIO} > 3.0 V, Applicable for overvoltage-tolerant pins only |
| SID.GIO#36 | V _{OL_3V} | Output voltage LOW level | – | – | 0.6 | V | I _{OL} = 10 mA at 3-V V _{DDIO} |
| SID.GIO#5 | R _{pu} | Pull-up resistor when enabled | 3.5 | 5.6 | 8.5 | kΩ | +25 °C T _A , All V _{DDIO} |
| SID.GIO#6 | R _{pd} | Pull-down resistor when enabled | 3.5 | 5.6 | 8.5 | | |
| SID.GIO#16 | I _{IL} | Input leakage current (absolute value) | – | – | 2 | nA | +25 °C T _A , 3-V V _{DDIO} |
| SID.GIO#17 | C _{PIN} | Max pin capacitance | – | 3 | 7 | pF | –40 °C ≤ T _A ≤ +55 °C, ALL V _{DDD} , ALL I/Os |
| SID.GIO#43 | V _{HYSTTL} | Input hysteresis, LVTTL, V _{DDIO} > 2.7 V | 15 | 40 | – | mV | V _{DDIO} > 2.7 V. Guaranteed by characterization. |
| SID.GIO#44 | V _{HYSCMOS} | Input hysteresis CMOS | 0.05 × V _{DDIO} | – | – | | V _{DDIO} < 4.5 V |
| SID.GIO#44A | V _{HYSCMOS55} | Input hysteresis CMOS | 200 | – | – | | V _{DDIO} > 4.5 V |
| SID.GIO#41A | V _{IH_VCCHIB} | V _{IH} , 1.8 V input mode | 1.26 | – | – | V | – |
| SID.GIO#42A | V _{IL_VCCHIB} | V _{IL} , 1.8 V input mode | – | – | 0.54 | | – |
| SID.GIO#43A | V _{HYS_VCCHIB} | Input hysteresis, 1.8 V input mode | 90 | – | – | mV | – |

Table 9. GPIO AC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|------------------------|--|-----|-----|-----|------|---|
| SID70 | T _{RISEF} | Rise time in Fast Strong mode | 2 | – | 12 | ns | 3.3-V V _{DDIO} , C _{load} = 25 pF |
| SID71 | T _{FALLF} | Fall time in Fast Strong mode | 2 | – | 12 | | |
| SID.GIO#46 | T _{RISES} | Rise time in Slow Strong mode | 10 | – | 60 | | |
| SID.GIO#47 | T _{FALLS} | Fall time in Slow Strong mode | 10 | – | 60 | | |
| SID.GIO#48 | F _{GPIO_OUT1} | GPIO F _{OUT} ; 3.3 V ≤ V _{DDIO} ≤ 5.5 V. Fast Strong mode. | – | – | 16 | MHz | 90/10%, 25-pF load |
| SID.GIO#49 | F _{GPIO_OUT2} | GPIO F _{OUT} ; 1.7 V ≤ V _{DDIO} ≤ 3.3 V. Fast Strong mode. | – | – | 16 | MHz | 90/10%, 25-pF load |
| SID.GIO#50 | F _{GPIO_OUT3} | GPIO F _{OUT} ; 3.3 V ≤ V _{DDIO} ≤ 5.5 V. Slow Strong mode. | – | – | 7 | | |
| SID.GIO#51 | F _{GPIO_OUT4} | GPIO F _{OUT} ; 1.7 V ≤ V _{DDIO} ≤ 3.3 V. Slow Strong mode. | – | – | 3.5 | | |
| SID.GIO#52 | F _{GPIO_IN} | GPIO input operating frequency; 1.7 V ≤ V _{DDIO} ≤ 5.5 V. | – | – | 16 | | 90/10% V _{IO} |

XRES
Table 10. XRES DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|----------------------|--|-------------------------|--------------------------|-------------------------|------|--------------------------------|
| SID.XRES#1 | V _{IH_XRES} | Input voltage HIGH threshold on XRES pin | 0.7 × V _{DDIO} | – | – | V | CMOS input |
| SID.XRES#2 | V _{IL_XRES} | Input voltage LOW threshold on XRES pin | – | – | 0.3 × V _{DDIO} | | |
| SID.XRES#3 | C _{IN_XRES} | Input capacitance on XRES pin | – | – | 7 | pF | – |
| SID.XRES#4 | V _{HYSXRES} | Input voltage hysteresis | – | 0.05 × V _{DDIO} | – | mV | Guaranteed by characterization |

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins
Table 11. PWM AC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------|-----------------------|------------------------------|------------------|-----|----------------|------|--|
| SID.TCPWM.3 | TCPWM _{FREQ} | Operating frequency | – | – | F _c | MHz | F _c max = 48 MHz |
| SID.TCPWM.4 | T _{PWMENEXT} | Input trigger pulse width | 2/F _c | – | – | ns | For all trigger events |
| SID.TCPWM.5 | T _{PWMEXT} | Output trigger pulse width | 2/F _c | – | – | | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | T _{CRES} | Resolution of counter | 1/F _c | – | – | | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM resolution | 1/F _c | – | – | | Minimum pulse width of PWM output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | 1/F _c | – | – | | Minimum pulse width between quadrature-phase inputs |

I²C
Table 12. Fixed I²C AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Mbps | – |

UART
Table 13. Fixed UART AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|------|--------------------|
| SID162 | F _{UART} | Bit rate | – | – | 1 | Mbps | – |

SPI
Table 14. Fixed SPI AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|------------------|---|-----|-----|-----|------|--------------------|
| SID166 | F _{SPI} | SPI operating frequency (Master; 6X oversampling) | – | – | 8 | MHz | – |

Table 15. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|------------------|---------------------------------------|-----|-----|-----|------|----------------------------------|
| SID167 | T _{DMO} | MOSI valid after SClk driving edge | – | – | 15 | ns | – |
| SID168 | T _{DSI} | MISO valid before SClk capturing edge | 20 | – | – | | Full clock, late MISO sampling |
| SID169 | T _{HMO} | Previous MOSI data hold time | 0 | – | – | | Referred to slave capturing edge |

Table 16. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|---------------------------------|---|-----|-----|------------------------------|------|---------------------------------------|
| SID170 | T _{DMI} | MOSI valid before Sclck capturing edge | 40 | – | – | ns | – |
| SID171 | T _{D_{SO}} | MISO valid after Sclck driving edge | – | – | 48 + (3 × T _{CPU}) | | T _{CPU} = 1/F _{CPU} |
| SID171A | T _{D_{SO}_EXT} | MISO valid after Sclck driving edge in Ext Clk mode | – | – | 48 | | – |
| SID172 | T _{H_{SO}} | Previous MISO data hold time | 0 | – | – | | – |
| SID172A | T _{SSEL_{SCK}} | SSEL valid to first SCK Valid edge | 100 | – | – | | – |

Memory
Table 17. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|-------------------------|--|------|-----|-----|--------|---|
| SID.MEM#4 | T _{ROW_WRITE} | Row (Block) write time (erase and program) | – | – | 20 | ms | –40 °C ≤ T _A ≤ +55 °C, All V _{DD} |
| SID.MEM#3 | T _{ROW_ERASE} | Row erase time | – | – | 13 | | |
| SID.MEM#8 | T _{ROWPROGRAM} | Row program time after erase | – | – | 7 | | 25 °C to 55 °C, All V _{DD} |
| SID178 | T _{BULKERASE} | Bulk erase time (64 KB) | – | – | 35 | | Guaranteed by design |
| SID180 | T _{DEVPROG} | Total device program time | – | – | 25 | s | |
| SID.MEM#6 | FLASH_ENPB | Flash write endurance | 100k | – | – | cycles | – |
| SID182 | F _{RET1} | Flash retention, T _A ≤ 55 °C, 100K P/E cycles | 20 | – | – | years | – |
| SID182A | F _{RET2} | Flash retention, T _A ≤ 85 °C, 10K P/E cycles | 10 | – | – | | – |

System Resources
Power-on-Reset (POR) with Brown Out
Table 18. Imprecise Power-on Reset (IPOR)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|-----------------------|--|------|-----|------|------|--------------------|
| SID185 | V _{RISEIPOR} | Power-on reset (POR) rising trip voltage | 0.80 | – | 1.50 | V | – |
| SID186 | V _{FALLIPOR} | POR falling trip voltage | 0.70 | – | 1.4 | | |

Table 19. Precise POR

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|------------------------|---|------|-----|------|------|--------------------|
| SID190 | V _{FALLPPOR} | Brown-out Detect (BOD) trip voltage in active/sleep modes | 1.48 | – | 1.62 | V | – |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep mode | 1.1 | – | 1.5 | | |

SWD Interface
Table 20. SWD Interface Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|--------------|-----------------------------------|----------|-----|----------|------|----------------------------------|
| SID.SWD#1 | F_SWDCLK1 | 3.3 V ≤ V _{DDIO} ≤ 5.5 V | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID.SWD#2 | F_SWDCLK2 | 1.8 V ≤ V _{DDIO} ≤ 3.3 V | – | – | 7 | | |
| SID.SWD#3 | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25 × T | – | – | ns | – |
| SID.SWD#4 | T_SWDI_HOLD | T = 1/f SWDCLK | 0.25 × T | – | – | | |
| SID.SWD#5 | T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.50 × T | | |
| SID.SWD#6 | T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | | |

Internal Main Oscillator
Table 21. IMO AC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|-----------------------|---|-----|-----|-----|------|---|
| SID.CLK#13 | F _{IMOTOL} | Frequency variation at 48 MHz (trimmed) | – | – | ±2 | % | 2.7 V ≤ V _{DDD} < 5.5 V, –25 °C ≤ T _A ≤ 55 °C |
| SID226 | T _{STARTIMO} | IMO start-up time | – | – | 7 | µs | – |
| SID.CLK#1 | F _{IMO} | IMO frequency | – | 48 | – | MHz | –40 °C ≤ T _A ≤ +55 °C, All V _{DDD} |

Internal Low-speed Oscillator
Table 22. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|------------------------|-------------------------------|-----|-----|-----|------|--------------------------------|
| SID234 | T _{STARTILO1} | I _{LO} start-up time | – | – | 2 | ms | Guaranteed by characterization |
| SID238 | T _{ILODUTY} | I _{LO} duty cycle | 40 | 50 | 60 | % | |
| SID.CLK#5 | F _{ILO} | I _{LO} frequency | 20 | 40 | 80 | kHz | – |

Table 23. Consumer NGDO Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|----------|------------------|---|------|-----|-----------|------|---|
| SID.GD.1 | GD_VGS | Gate to Source overdrive during ON condition | 4.5 | – | 10 | V | NFET Driver is ON. |
| SID.GD.2 | GD_RPD | Resistance when pull-down enabled | – | – | 2 | KΩ | Applicable on VBUS_C_C-TRL_P0/1 to turn OFF external NFET. |
| SID.GD.3 | GD_VGS_OFF | Gate to Source overdrive during OFF condition | – | – | -VBUS_MAX | V | External NFET must be able to tolerate “VGS < -VBUS_MAX” in OFF state as V _{gate} = 0 V. |
| SID.GD.4 | IOUT_VBUS_C_CTRL | Output current from VBUS_C_CTRL pin when consumer NGDO is enabled | 3.44 | 4.3 | 5.16 | µA | Consumer NGDO is enabled and voltage on VBUS_C_CTRL pin at 1.4 V-5.5 V (decimal setting of slew-ctrl register = 27) |

PD
Table 24. PD DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------------|------------|---|-------|-----|-------|------|----------------------|
| SID.DC.cc_shvt.1 | vSwing | Transmitter Output High Voltage | 1.05 | – | 1.2 | V | – |
| SID.DC.cc_shvt.2 | vSwing_low | Transmitter Output Low Voltage | – | – | 0.075 | | – |
| SID.DC.cc_shvt.3 | zDriver | Transmitter output impedance | 33 | – | 75 | Ω | – |
| SID.DC.cc_shvt.4 | zBmcRx | Receiver Input Impedance | 10 | – | – | MΩ | Guaranteed by design |
| SID.DC.cc_shvt.5 | Idac_std | Source current for USB standard advertisement | 64 | – | 96 | µA | – |
| SID.DC.cc_shvt.6 | Idac_1p5a | Source current for 1.5A at 5 V advertisement | 165.6 | – | 194.4 | | – |
| SID.DC.cc_shvt.7 | Idac_3a | Source current for 3A at 5 V advertisement | 303.6 | – | 356.4 | | – |

Table 24. PD DC Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-------------------|------------------|--|------|-----|------|------|--------------------|
| SID.DC.cc_shvt.8 | Rd | Pull down termination resistance when acting as UFP (upstream facing port) | 4.59 | – | 5.61 | kΩ | – |
| SID.DC.cc_shvt.9 | Rd_db | Pull down termination resistance when acting as UFP, with dead battery | 4.08 | – | 6.12 | | – |
| SID.DC.cc_shvt.10 | zOPEN | CC impedance to ground when disabled | 108 | – | | | – |
| SID.DC.cc_shvt.11 | DFP_default_0p2 | CC voltages on DFP side-Standard USB | 0.15 | – | 0.25 | V | – |
| SID.DC.cc_shvt.12 | DFP_1.5A_0p4 | CC voltages on DFP side-1.5A | 0.35 | – | 0.45 | | – |
| SID.DC.cc_shvt.13 | DFP_3A_0p8 | CC voltages on DFP side-3A | 0.75 | – | 0.85 | | – |
| SID.DC.cc_shvt.14 | DFP_3A_2p6 | CC voltages on DFP side-3A | 2.45 | – | 2.75 | | – |
| SID.DC.cc_shvt.15 | UFP_default_0p66 | CC voltages on UFP side-Standard USB | 0.61 | – | 0.7 | | – |
| SID.DC.cc_shvt.16 | UFP_1.5A_1p23 | CC voltages on UFP side-1.5A | 1.16 | – | 1.31 | | – |
| SID.DC.cc_shvt.17 | Vattach_ds | Deep sleep attach threshold | 0.3 | – | 0.6 | % | – |
| SID.DC.cc_shvt.18 | Rattach_ds | Deep sleep pull-up resistor | 10 | – | 50 | kΩ | – |
| SID.DC.cc_shvt.19 | VTX_step | TX Drive voltage step size | 80 | – | 120 | mV | – |
| SID.DC.cc_shvt.30 | FS_0p53 | Voltage threshold for Fast Swap Detect | 0.49 | – | 0.58 | V | – |

Analog-to-Digital Converter
Table 25. ADC DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|------------|----------------------------|--------------------|-----|--------------------|------|---|
| SID.ADC.1 | Resolution | ADC resolution | – | 8 | – | Bits | – |
| SID.ADC.2 | INL | Integral non-linearity | –1.5 | – | 1.5 | LSB | – |
| SID.ADC.3 | DNL | Differential non-linearity | –2.5 | – | 2.5 | | – |
| SID.ADC.4 | Gain Error | Gain error | –1.5 | – | 1.5 | | – |
| SID.ADC.5 | VREF_ADC1 | Reference voltage of ADC | V _{DDmin} | – | V _{DDmax} | V | Reference voltage generated from V _{DD} |
| SID.ADC.6 | VREF_ADC2 | Reference voltage of ADC | 1.96 | 2.0 | 2.04 | | Reference voltage generated from deep sleep reference |

V_{SYS} Switch
Table 26. V_{SYS} Switch Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------|-----------|---|-----|-----|-----|------|--|
| SID.DC.VDDDSW.1 | Res_sw | Resistance from supply input to output supply V _{DD} | – | – | 1.5 | Ω | Measured with a load current of 5 mA to 10 mA on V _{DD} . |

CSA

Table 27. CSA DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------------|----------------------|---|------|-------------|------|------|--|
| DC.csa_scp.42 | SCP_6A | Short circuit current detect @ 6A | – | ±10 | – | % | – |
| DC.csa_scp.43 | SCP_10A | Short circuit current detect @10A | – | ±10 | – | | – |
| OP.csa_scp.11 | Rsense | External sense register | 4.95 | 5 | 5.05 | mΩ | |
| DC.csa_scp.44 | locp_1A | OCP Trip threshold for 1A | – | 130 ±20% | – | % | 1A PD contracts OCP set at 130% of contract value or user programmable |
| DC.csa_scp.45 | locp_5A | OCP Trip threshold for 2A, 3A, 4A and 5A contracts | – | 130 ±10% | – | | 2A, 3A, 4A, and 5A PD contracts OCP set at 130% of contract value OR user programmable |
| DC.rcp_scp.7a | I_csainn_lk | CSP pin input leakage when RCP and CSA blocks are OFF | – | – | 10 | μA | For provider V _{BUS_P_P0/1} = 5 V. |
| DC.rcp_scp.6a | I_csainp_lk | CSN pin input leakage when RCP and CSA blocks are OFF | – | – | 80 | | |
| DC.sys.1 | I_CSP_RCP_ON_CSA_OFF | CSP pin current when RCP block is ON and SCP is OFF | – | – | 20 | | |
| DC.sys.2 | I_CSN_RCP_ON_CSA_OFF | CSN pin current when RCP block is ON and SCP is OFF | – | – | 100 | | |
| DC.sys.3 | I_CSP_CSA_ON | CSP pin current when RCP block is OFF and SCP is ON | – | – | 30 | | |
| DC.sys.4 | I_CSN_CSA_ON | CSN pin current when RCP block is OFF and SCP is ON | – | – | 100 | | |
| DC.sys.5 | I_CSP_RCP_ON_CSA_ON | CSP pin current when RCP block is ON and SCP is ON | – | – | 50 | μA | For provider V _{BUS} = 5 V. Guaranteed by design. |
| DC.sys.6 | I_CSP_RCP_ON_CAS_ON | CSN pin current when RCP block is ON and SCP is ON | – | – | 120 | | |

 V_{BUS} UV/OV

Table 28. V_{BUS} UV/OV Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------|----------------------|--|-----|-----|-----|------|--------------------|
| SID.UVOV.1 | V _{THUVOV1} | Voltage threshold accuracy in active mode using bandgap reference | – | ±3 | – | % | – |
| SID.UVOV.2 | V _{THUVOV2} | Voltage threshold accuracy in deep sleep mode using deep sleep reference | – | ±5 | – | | – |
| SID.COMP_ACC | COMP_ACC | Comparator input offset at 4sigma | -15 | – | 15 | mV | – |

Provider Side RCP
Table 29. Provider Side RCP DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|--------------|---|-----|-------|-----|------|--------------------|
| DC.RCP.44 | Vcsa_rcp | Voltage across external R _{sense} between CSP/CSN for which RCP condition detected (CSN higher than CSP by Vcsa_rcp) | – | 2 | 6 | mV | – |
| DC.RCP.45 | Vcomp_rcp | Voltage across V _{BUS} and CSN pins for which RCP condition is detected | 20 | – | 130 | | – |
| DC.RCP.46 | Vbus_max_det | Voltage on CSN pad during provider FET ON (source) for which RCP condition is triggered (this threshold is user programmable) | – | 5.375 | – | V | – |

Table 30. Provider Side RCP, SCP AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------|-----------|--|-----|-----|-----|------|--|
| AC.RCP_SYS.1 | Toff_rcp | Provider NFET switching off after reverse current detect through provider FET (for 20-V hot plug-in) | – | 1 | – | μs | VBUS = 5 V/3A, Provider path ON, 47-μF ceramic cap on VBUS_P pin |
| AC.RCP_SYS.2 | Ton | Time taken to detect RCP out-of-fault | – | 55 | 80 | μs | VBUS falls below CSN and start NGDO enable |

Table 31. V_{BUS} Provider Switch Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------------|-------------------|--|-----|-----|-----|------|--|
| DC.ngdo_fet_sys.1 | RDS _{ON} | FET RDS _{ON} (96-BGA) | – | 40 | 55 | mΩ | 3A Load current, Short-duration pulse, –40 °C to 55 °C TA |
| DC.ngdo_fet_sys.1a | RDS _{ON} | FET RDS _{ON} (48-QFN) | – | 45 | 55 | | |
| DC.NGDO_FET_SYS.2 | Isw | Continuous current | – | – | 3.0 | A | If one port is sourcing 3A, the other port can source only up to 1.5A. Measurement done in pulse mode. |
| AC.NGDO_FET_SYS.1 | Ton | V _{BUS} Low to High (10% to 90%) | – | 5 | – | ms | 0.8 to 4.5-V transition, system-level (with 10Ω load on VBUS_C) |
| AC.NGDO_FET_SYS.2 | Toff_fault | VBUS High to Low (90% to 10%) - Under fault condition of SCP/RCP | – | 1 | – | μs | |
| AC.NGDO_FET_SYS.3 | Toff | VBUS High to Low (90% to 10%) - Under normal condition | – | 7 | – | μs | |
| AC.NGDO_FET_SYS.4 | OTsth_OFF | Overtemperature shutdown threshold OFF, Junction temperature | – | 125 | – | °C | – |
| AC.NGDO_FET_SYS.5 | OTsth_OFF | Overtemperature shutdown threshold ON, Junction temperature | – | 90 | – | °C | |

SBU Switch
Table 32. SBU Switch DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------------|-----------------|--|------|-----|------|------|--------------------|
| DC.ccg6df.20sbu.1 | Ron1 | On resistance of AUXP/N to SBU1/2 switch @3.3-V input | - | 4 | 7 | Ω | - |
| DC.ccg6df.20sbu.2 | Ron2 | On resistance of AUXP/N to SBU1/2 switch @1-V input | - | 3 | 5 | | - |
| DC.ccg6df.20sbu.4 | Ileak1 | Pin leakage current for SBU1, SBU2 | -4.5 | - | 4.5 | μA | - |
| DC.ccg6df.20sbu.5 | Ileak2 | Pin leakage current for SBU1_SYS, SBU2_SYS | -1 | - | 1 | μA | - |
| DC.ccg6df.20sbu.16 | OVP_threshold | Overvoltage protection detection threshold above V _{DDIO} | 200 | - | 1200 | mV | - |
| DC.ccg6df.20sbu.19 | aux_ron_flat_fs | Switch On flat resistance of SBU1/2_SYS to SBU1/2 switch (from 0 to 3.3 V) | - | - | 2.5 | Ω | - |
| DC.ccg6df.20sbu.20 | aux_ron_flat_hs | Switch On flat resistance of SBU1/2_SYSto SBU1/2 switch (from 0 to 1 V) | - | - | 0.5 | | - |

Table 33. SBU Switch AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------------|----------------------------|---|-----|-----|-----|------|----------------------|
| AC.ccg6df.20sbu.1 | Con | Switch On capacitance | - | - | 120 | pF | - |
| AC.ccg6df.20sbu.2 | Coff | Switch Off capacitance-Connector side | - | - | 80 | | Guaranteed by design |
| AC.ccg6df.20sbu.3 | Off_isolation | Switch isolation at F = 1 MHz | -50 | - | - | dB | |
| AC.ccg6df.20sbu.4 | TON | SBU switch turn-on time | - | - | 200 | μs | - |
| AC.ccg6df.20sbu.5 | TOFF | SBU switch turn-off time | - | - | 400 | | - |
| AC.ccg6df.20sbu.3_aux | Off_isolation_AC_aux | Switch isolation at F = 1 MHz, from SBU_5V to SBU pins | -50 | - | - | dB | Guaranteed by design |
| AC.ccg6df.20sbu.6_aux | Off_isolation_tran_d-B_aux | Coupling on sbu1, 2 terminated to 50 Ω, switch-OFF, 1-MHz rail-to-rail toggling on SBU1_5V, SBU2_5V | -30 | - | - | | |
| AC.ccg6df.20sbu.7_aux | X_talk_AC_aux | Cross talk of Switch at F = 1 MHz SBU1/2 to SBU2/1 when is data transferred from SBU1/2_5V | -50 | - | - | | Guaranteed by design |
| AC.ccg6df.20sbu.8_aux | X_talk_tran_d-B_aux | Coupling on SBU2 (1) When Data is transferred from SBU1(2)_5V to SBU1 (2). Rail-to-rail data on SBU1(2), static signal on SBU2(1) | -30 | - | - | | |

DP/DM Switch
Table 34. DP/DM Switch DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ Conditions |
|-------------------|---------------|---|-----|-----|-----|------|------------------------|
| DC.ccg6df.dpdm.1 | RON_HS | DP/DM On resistance (0 to 0.5 V) - HS mode | - | - | 8 | Ω | - |
| DC.ccg6df.dpdm.2 | RON_FS | DP/DM On resistance (0 to 3.3 V) - FS mode | - | - | 12 | | - |
| DC.ccg6df.dpdm.5 | Con_FS | Switch On capacitance at 6 MHz - FS mode | - | - | 50 | pF | Guaranteed by design |
| DC.ccg6df.dpdm.6 | Con_HS | Switch on capacitance at 240 MHz - HS mode | - | - | 10 | | |
| DC.ccg6df.dpdm.9 | ileak_pin | pin leakage at DP/DM connector side and host side | - | - | 1 | μA | - |
| DC.ccg6df.dpdm.10 | RON_UART | DP/DM On resistance for UART lines (0 to 3.3 V) | - | - | 17 | Ω | - |
| DC.ccg6df.dpdm.11 | RON_FLAT_HS | DP/DM On Flat resistance in HS mode (0 to 0.4 V) | - | - | 0.5 | | - |
| DC.ccg6df.dpdm.12 | RON_FLAT_FS | DP/DM On flat resistance in FS mode (0 to 3.3 V) | - | - | 4 | | - |
| DC.ccg6df.dpdm.13 | RON_FLAT_UART | DP/DM UART On flat resistance (0 to 3.3 V) | - | - | 4 | | - |

Table 35. DP/DM Switch AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ Conditions |
|-------------------|-----------------------|--|-----|-----|-----|------|------------------------|
| AC.ccg6df.dpdm.1 | BW_3dB_HS | 3-db bandwidth | 700 | - | - | MHz | - |
| AC.ccg6df.dpdm.2 | BW_3dB_FS | 3-db bandwidth | 100 | - | - | | - |
| AC.ccg6df.dpdm.5 | T _{ON} | DP/DM Switch turn-on time | - | - | 200 | μs | - |
| AC.ccg6df.dpdm.6 | T _{OFF} | DP/DM Switch turn-off time | - | - | 0.4 | | - |
| AC.ccg6df.dpdm.7 | T _{ON_VPUMP} | DP/DM charge pump startup time | - | - | 200 | | - |
| AC.ccg6df.dpdm.8 | Off_isolation_HS | Switch-off isolation for HS | -20 | - | - | dB | Guaranteed by design |
| AC.ccg6df.dpdm.9 | Off_isolation_FS | Switch-off isolation for FS | -50 | - | - | | |
| AC.ccg6df.dpdm.10 | X_talk | Cross talk of Switch From FS to HS at F = 12 MHz | -50 | - | - | | |
| AC.ccg6df.dpdm.11 | uart_coupling | Peak-to-peak coupling of UART signal to DP lines. (UART signal 0 to 3.3 V) | - | - | 20 | mV | - |

VCONN Switch
Table 36. VCONN Switch DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|----------------------|------------------|---|-----|-----|------|------|----------------------|
| DC.ccg6df.20VCONN.1 | R _{on} | Switch ON resistance at V5V = 5 V with 215-mA load current | – | 0.7 | 1.3 | Ω | – |
| DC.ccg6df.20VCONN.9 | I _{ocp} | Overcurrent detection range for CC1/CC2 | 550 | – | – | mA | – |
| DC.ccg6df.20VCONN.10 | OVP_threshold | CC1, CC2 overvoltage protection detection threshold above V _{DD} or V5V, whichever is higher | 200 | – | 1200 | mV | – |
| DC.ccg6df.20VCONN.11 | OVP_hysteresis | Overvoltage detection hysteresis | 50 | – | 300 | | Guaranteed by design |
| DC.ccg6df.20VCONN.12 | OCP_hysteresis | Overcurrent detection hysteresis | 20 | – | 80 | | mA |
| DC.ccg6.20VCONN.14 | OVP_threshold_on | Overvoltage detection threshold above V5V of CC1/2, with CC1 or CC2 switch enabled. Same threshold triggers reverse current protection circuit. | 200 | – | 700 | mV | – |

Table 37. VCONN Switch AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------------------|------------------|----------------------------|-----|-----|-----|------|----------------------|
| AC.ccg6df.20VCONN.1 | T _{ON} | VCONN switch turn-on time | – | – | 200 | μs | – |
| AC.ccg6df.20VCONN.2 | T _{OFF} | VCONN switch turn-off time | – | – | 3 | | Guaranteed by design |

V_{BUS}
Table 38. V_{BUS} Discharge Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------|------------------|---|------|-----|------|------|--------------------|
| SID.VBUS.DISC.1 | R _{on1} | 20-V NMOS ON resistance (with dischg_ds<0> = 1; dischg_ds<4:1> = 0) | 1500 | – | 3000 | Ω | – |
| SID.VBUS.DISC.2 | R _{on2} | 20-V NMOS ON resistance (with dischg_ds<1:0> = 1; dischg_ds<4:2> = 0) | 750 | – | 1500 | | – |
| SID.VBUS.DISC.3 | R _{on3} | 20-V NMOS ON resistance (with dischg_ds<2:0> = 1; dischg_ds<4:3> = 0) | 500 | – | 1000 | | – |
| SID.VBUS.DISC.4 | R _{on4} | 20-V NMOS ON resistance (with dischg_ds<3:0> = 1; dischg_ds<4> = 0) | 375 | – | 750 | | – |
| SID.VBUS.DISC.5 | R _{on5} | 20-V NMOS ON resistance (with dischg_ds<4:0> = 1) | 300 | – | 600 | | – |

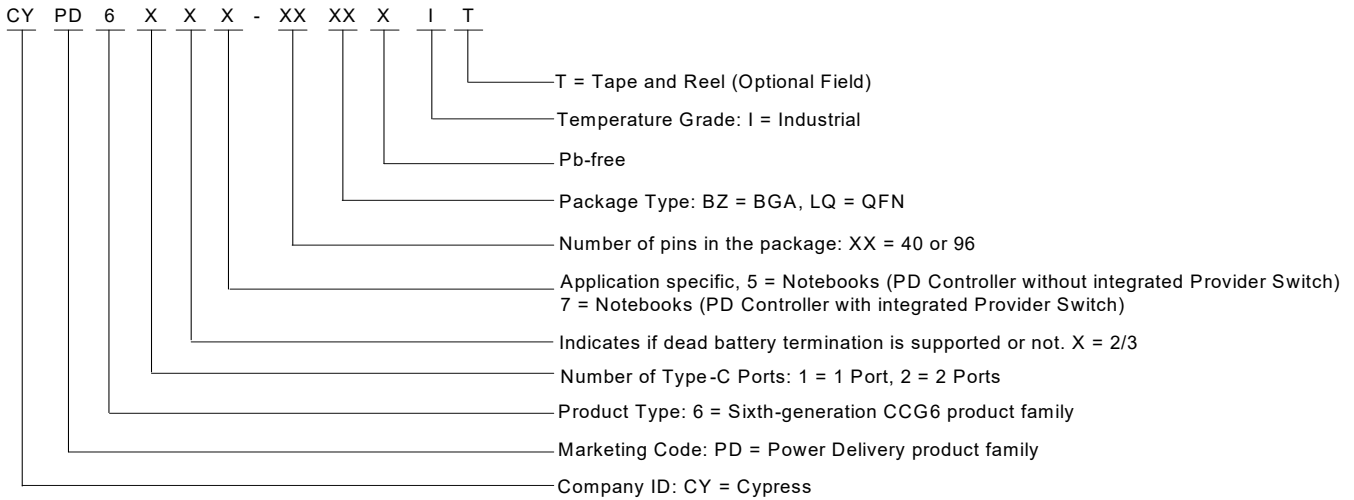
Ordering Information

Table 39 lists the EZ-PD CCG6DF, EZ-PD CCG6SF part numbers and features.

Table 39. EZ-PD CCG6DF Ordering Information

| Product | Part Number | Application | Integrated VBUS Switch | Type-C Ports | Dead Battery Termination | Termination Resistor | Role | Package |
|---------|-----------------|-------------|------------------------|--------------|--------------------------|---------------------------------------|------|-------------|
| CCG6SF | CYPD6127-48LQXI | Notebooks | Yes | 1 | Yes | Rp ^[6] , Rd ^[7] | DRP | 48-pin QFN |
| CCG6DF | CYPD6227-96BZXI | | | 2 | | | | 96-ball BGA |

Ordering Code Definitions



Notes

- Termination resistor denoting a Source.
- Termination resistor denoting an accessory or Sink.

Packaging

Table 40. Package Characteristics

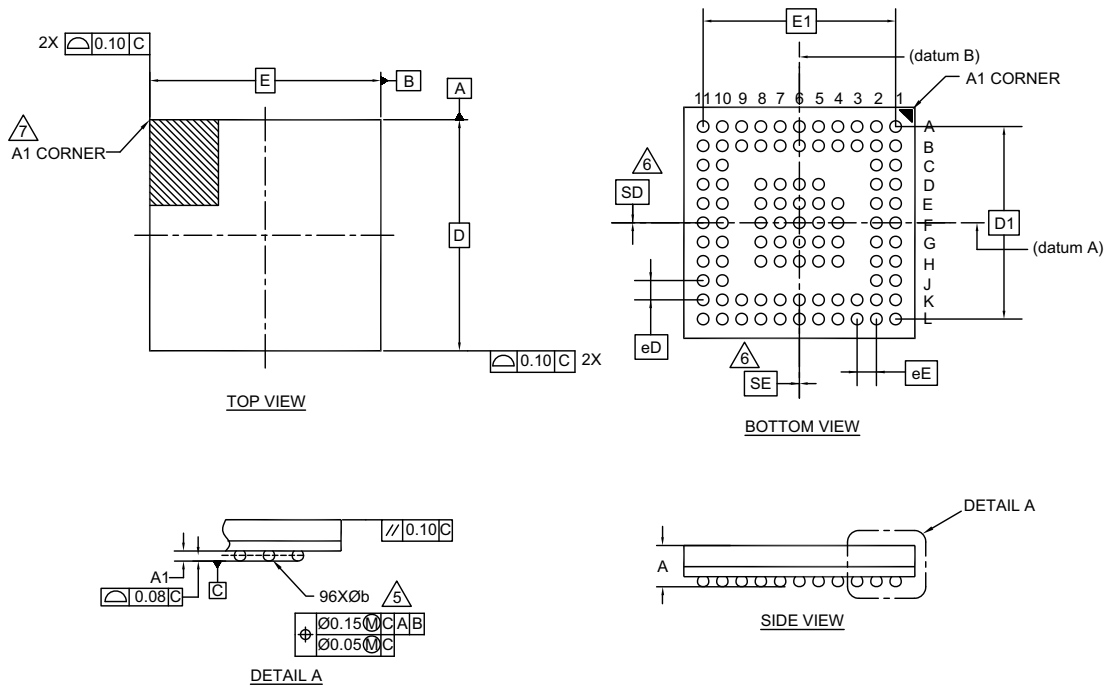
| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|------------|-----|-----|------|------|
| T _A | Operating ambient temperature | Industrial | -40 | 25 | 55 | °C |
| T _J | Operating junction temperature | | | | 125 | |
| T _{JA} | Package θ_{JA} (96-ball BGA) | - | - | - | 56.9 | °C/W |
| T _{JC} | Package θ_{JC} (96-ball BGA) | | | | 36.9 | |
| T _{JA} | Package θ_{JA} (48-pin QFN) | - | - | - | 40.2 | |
| T _{JC} | Package θ_{JC} (48-pin QFN) | | | | 40.1 | |

Table 41. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time within 5 °C of Peak Temperature |
|-------------|--------------------------|--|
| 96-ball BGA | 260 °C | 30 seconds |
| 48-pin QFN | | |

Table 42. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|-------------|-------|
| 96-ball BGA | MSL 3 |
| 48-pin QFN | |

Figure 30. 96-ball BGA (6 × 6 × 0.5 mm), 6.0 × 6.0 x 1.0 mm Package Outline


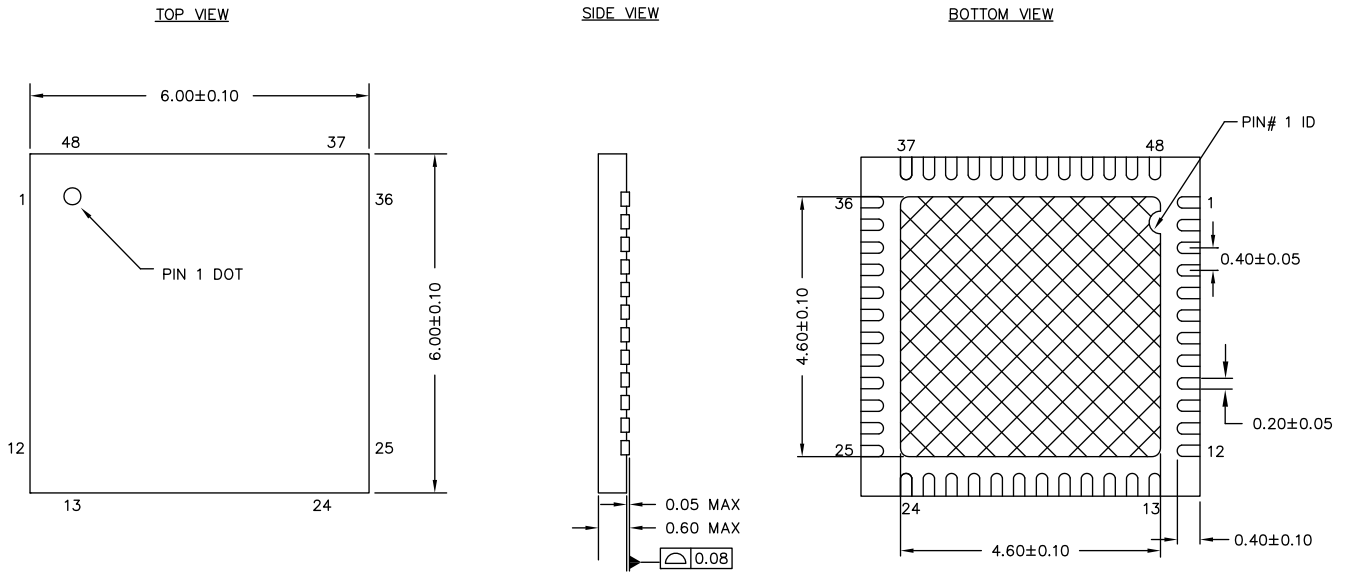
| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | - | - |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| D1 | 5.00 BSC | | |
| E1 | 5.00 BSC | | |
| MD | 11 | | |
| ME | 11 | | |
| N | 96 | | |
| Ø b | 0.25 | 0.30 | 0.35 |
| eD | 0.50 BSC | | |
| eE | 0.50 BSC | | |
| SD | 0.00 | | |
| SE | 0.00 | | |

NOTES:


- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : MO-225.

002-10631 *B

Figure 31. 48L-QFN 6 mm x 6 mm x 0.6 mm Package Outline



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Acronyms

Table 43. Acronyms Used in this Document

| Acronym | Description |
|--------------------------|---|
| ADC | analog-to-digital converter |
| API | application programming interface |
| Arm® | advanced RISC machine, a CPU architecture |
| CC | configuration channel |
| CSN | current sense negative |
| BCC | battery charger controller |
| BOD | Brown out Detect |
| CC | configuration channel |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| CS | current sense |
| CSA | current sense amplifier |
| CSN | current sense negative |
| CSP | current sense positive |
| DFP | downstream facing port |
| DM | data minus |
| DP | data plus signal |
| DP | DisplayPort, digital display interface developed by Video Electronics Standards Association |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DRP | dual role power |
| EC | embedded controller |
| EEPROM | electrically erasable programmable read-only memory |
| EMCA | a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FPB | flash patch and breakpoint |
| FRS | fast role swap |
| FS | full-speed |
| GPIO | general-purpose input/output |
| HDI | high density interconnect |
| HSCSA | high-side current sense amplifier |
| IC | integrated circuit |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |

Table 43. Acronyms Used in this Document (continued)

| Acronym | Description |
|---------|--|
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| I/O | input/output, see also GPIO |
| IPOR | imprecise POR |
| IRQ | interrupt request |
| ISR | interrupt service request |
| LVD | low-voltage detect |
| LVTTL | low-voltage transistor-transistor logic |
| MCU | microcontroller unit |
| MDI | medium density |
| NC | no connect |
| NGDO | N-FET gate driver output |
| NMI | nonmaskable interrupt |
| NVIC | nested vectored interrupt controller |
| opamp | operational amplifier |
| OCP | overcurrent protection |
| OVP | overvoltage protection |
| PCB | printed circuit board |
| PD | power delivery |
| PGA | programmable gain amplifier |
| PHY | physical layer |
| POR | power-on reset |
| PRES | precise power-on reset |
| PSoC® | Programmable System-on-Chip™ |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RCP | reverse current protection |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RX | receive |
| SAR | successive approximation register |
| SCB | serial communication block |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SMT | surface-mount technology |
| SPI | Serial Peripheral Interface, a communications protocol |
| SRAM | static random access memory |

Table 43. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|---------|--|
| SWD | serial wire debug, a test protocol |
| TBT | Thunderbolt, hardware interface standard for peripherals developed by Intel |
| TCPWM | timer/counter pulse-width modulation |
| TRNG | true random number generator |
| TX | transmit |
| Type-C | a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UFP | upstream facing port |
| USB | Universal Serial Bus |
| USBIO | USB input/output, CCG6D/CCG6DF pins used to connect to a USB port |
| USBTCAS | USB Type-C Authentication Specification |
| UVOV | under-voltage/over-voltage |
| WDT | watchdog timer |
| XRES | external reset I/O pin |

Document Conventions

Units of Measure

Table 44. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| Hz | hertz |
| KB | 1024 bytes |
| kHz | kilohertz |
| kΩ | kilo ohm |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| mΩ | milliohm |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| V | volt |

References and Links to Applications Collateral

Knowledge Base Articles

- [Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG5 - KBA210740](#)
- [Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG5 Using PSoC® Programmer and MiniProg3 - KBA96477](#)
- [CCGX Frequently Asked Questions \(FAQs\) - KBA97244](#)
- [Cypress EZ-PD™ CCGx Hardware - KBA204102](#)
- [Difference between USB Type-C and USB-PD - KBA204033](#)
- [CCGX Programming Methods - KBA97271](#)
- [Getting started with Cypress USB Type-C Products - KBA04071](#)
- [Type-C to DisplayPort Cable Electrical Requirements](#)
- [Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273](#)
- [Termination Resistors Required for the USB Type-C Connector – KBA97180](#)
- [VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270](#)
- [Need for Regulator and Auxiliary Switch in Type-C to DisplayPort \(DP\) Cable Solution - KBA97274](#)
- [Need for a USB Billboard Device in Type-C Solutions – KBA97146](#)
- [Cypress USB Type-C Controller Supported Solutions – KBA97179](#)
- [Termination Resistors for Type-C to Legacy Ports – KBA97272](#)
- [Handling Instructions for CY4502 CCG2 Development Kit – KBA97916](#)
- [Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976](#)
- [Power Adapter Application Using CCG3 Devices - KBA210975](#)
- [Methods to Upgrade Firmware on CCG3 Devices - KBA210974](#)
- [Device Flash Memory Size and Advantages - KBA210973](#)
- [Applications of EZ-PD™ CCG5 - KBA210739](#)

Application Notes

- [AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2](#)
- [AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2](#)
- [AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers](#)
- [AN210771 - Getting Started with EZ-PD™ CCG4](#)

Reference Designs

- [EZ-PD™ CCG2 Electronically Marked Cable Assembly \(EMCA\) Paddle Card Reference Design](#)
- [EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution](#)
- [EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution](#)
- [EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle](#)
- [EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution](#)
- [CCG2 20W Power Adapter Reference Design](#)
- [CCG2 18W Power Adapter Reference Design](#)
- [EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit](#)

Kits

- [CY4502 EZ-PD™ CCG2 Development Kit](#)
- [CY4531 EZ-PD CCG3 Evaluation Kit](#)
- [CY4541 EZ-PD™ CCG4 Evaluation Kit](#)

Datasheets

- [CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C](#)
- [CCG2: USB Type-C Port Controller Datasheet](#)
- [CCG3: USB Type-C Controller Datasheet](#)
- [CCG5C: USB Type-C Controller Datasheet](#)

Document History Page

| Document Title: EZ-PD CCG6DF, CCG6SF, USB Type-C Port Controller | | | |
|--|---------|-----------------|---|
| Document Number: 002-27161 | | | |
| Revision | ECN | Submission Date | Description of Change |
| ** | 6580063 | 05/27/2019 | Initial release |
| *A | 6649813 | 08/09/2019 | Modified Document Title for EZ-PD CCG6DF, CCG6SF, USB Type-C Controller. Updated EZ-PD CCG6DF, CCG6SF, USB Type-C Port Controller, Features, Logic Block Diagram, CCG6DF/CCG6SF Functional Diagram and Application Diagrams sections. Updated Table 2 , Table 39 , Table 40 , Table 41 , Table 42 . Added Table 3 . Updated Figure 4 , added Figure 4 , removed Figure 2 and Figure 3 from previous version. |
| *B | 6673392 | 09/13/2019 | Changed status from "Advance" to "Preliminary". Updated Logic Block Diagram, Features, CCG6DF/CCG6SF Functional Diagram , and References and Links to Applications Collateral . Added Functional Overview, Power, Application Diagrams , and CCG6SF 48-pin QFN Single Port Thunderbolt Notebook Application Diagram . Updated Table 2 , Table 3 , Table 39 , and Table 42 . Updated Figure 4 and Figure 4 . Added Electrical Specifications in Table 5 through Table 38 . |
| *C | 6682221 | 09/26/2019 | Updated Pinouts (added Figure 5 and Table 3). Updated Ordering Information , and Packaging (added Figure 31). Updated Table 31 : Updated typical and max values for DC.ngdo.fet_sys.1 spec. Added new spec DC.ngdo.fet_sys.1a for QFN package. |
| *D | 6732422 | 11/18/2019 | Updated General Description and Features . Updated Figure 5 , Figure 6 , and Figure 8 . Updated Table 3 , Table 40 , Table 41 , and Table 42 . Added Figure 3 and Figure 7 . Updated Figure 30 . |
| *E | 6769410 | 01/14/2020 | Updated Logic Block Diagram . Updated Figure 1 , Figure 4 , Figure 4 , Figure 6 , and Figure 8 . Updated Table 2 , Table 3 , Table 6 (SID.PWR#1_A and SID_DS3 parameters), Table 29 (added DC.RCP.46 parameter) and Table 31 (RDS _{ON} parameter for 96-BGA). Removed Usage of Via Size of 6-mil drill and 12-mil diameter section. Added Usage of Via Size of 8-mil drill/16-mil Diameter and 10-mil drill/16-mil Diameter section. Updated Copyright information. |
| *F | 6797977 | 03/13/2020 | Updated General Description and Features . Updated Watchdog Timer (WDT) section. Removed Pinout for CYPD6127-96BZXI table. Removed 96-Ball BGA Pin Map (Top View) for CYPD6127-96BZXI and CCG6SF 96-ball BGA Single Port Thunderbolt Notebook Application Diagram figures. Updated Table 40 . Updated Acronyms . |
| *G | 6864182 | 05/28/2020 | Removed PRELIMINARY document status. Added CCG6SF Layout Design Guidelines for 48-QFN Package . Deleted CC Connections subsection in CCG6DF Layout Design Guidelines for BGA Package . Added Table 23 . Updated Table 5 , Table 36 , and Table 39 . |
| *H | 6897712 | 07/23/2020 | Updated Table 6 , Table 8 , and Table 23 . |

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