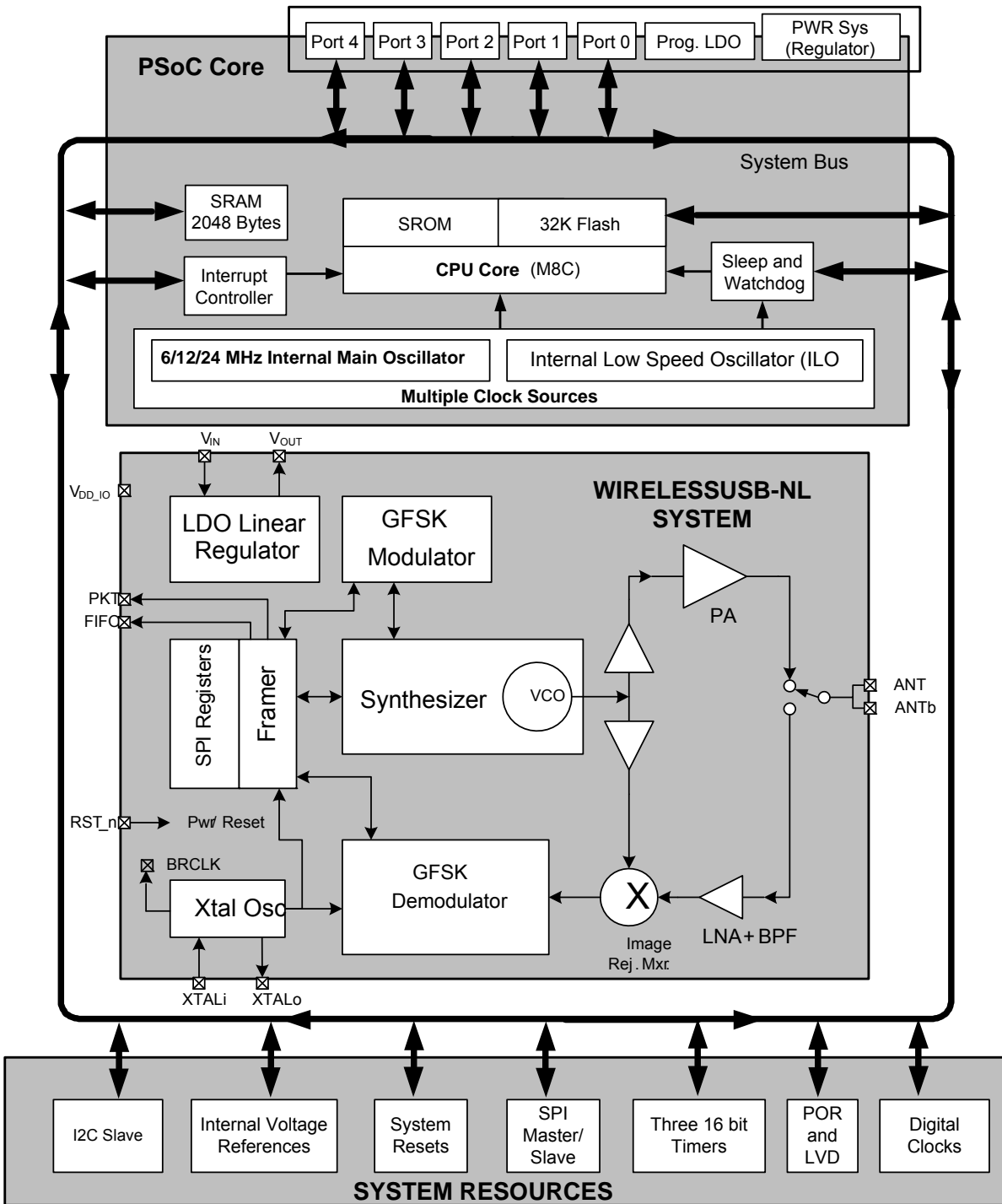


## PRoC™ – Embedded Features

- Single Device, two functions
  - 8-bit flash based MCU function and 2.4-GHz WirelessUSB™ NL radio transceiver function in a single device
- RF Attributes
  - Wide operating range: 1.9 V to 3.6 V
  - 2.4-GHz WirelessUSB NL Transceiver function
  - Operates in the 2.4-GHz ISM Band (2.402 GHz–2.479 GHz)
  - 1-Mbps over-the-air data rate
  - Receive sensitivity typical: –87 dBm
  - 1  $\mu$ A typical current consumption in sleep state
  - Closed-loop frequency synthesis
  - Supports frequency-hopping spread spectrum
  - On-chip packet framer with 64-byte first in first out (FIFO) data buffer
  - Built-in auto-retry-acknowledge protocol simplifies usage
  - Built-in cyclic redundancy check (CRC), forward error correction (FEC), data whitening
  - Additional outputs for interrupt request (IRQ) generation
  - Digital readout of received signal strength indication (RSSI)
- MCU Attributes
  - Powerful Harvard-architecture processor
  - M8C CPU – Up to 4 MIPS with 24 MHz Internal clock, external crystal resonator or clock signal
  - Low power at high speed
- Temperature range: 0 °C to +70 °C
- Flexible on-chip memory
  - 32 KB Flash/2 KB SRAM
  - 50,000 flash erase/write cycles
  - Partial flash updates
  - Flexible protection modes
  - In-system serial programming (ISSP)
- Precision, programmable clocking
  - Internal main oscillator (IMO): 6/12/24 MHz  $\pm$  5%
  - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
  - Precision 32 kHz oscillator for optional external crystal
- Programmable pin configurations
  - Up to 35 general-purpose I/Os (GPIOs)
  - Dual mode GPIO: All GPIOs support digital I/O and analog inputs
  - 25-mA sink current on each GPIO
    - 120 mA total sink current on all GPIOs
  - Pull-up, high Z, open-drain modes on all GPIOs
  - CMOS drive mode –5 mA source current on ports 0 and 1 and 1 mA on port 2
  - 20 mA total source current on port 1.
  - Configurable input threshold for Port 1.
- Versatile analog system
  - Low-dropout voltage regulator for all analog resources
  - High power supply rejection ratio (PSRR) comparator
  - 8 to 10-bit incremental analog-to-digital converter (ADC)
- Additional system resources
  - I<sup>2</sup>C slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
  - SPI master and slave: Configurable 46.9 kHz to 12 MHz
  - Three 16-bit timers
  - Watchdog and sleep timers
  - Integrated supervisory circuit
  - Emulated E2PROM using flash memory
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Package option
  - 68-pin 8mm  $\times$  8mm  $\times$  1.0 mm QFN

Logical Block Diagram



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## PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the [Logical Block Diagram on page 2](#), consists of three main areas:

- The Core
- WirelessUSB NL System
- System Resources.

A common, versatile bus allows connection between I/O and the analog system.

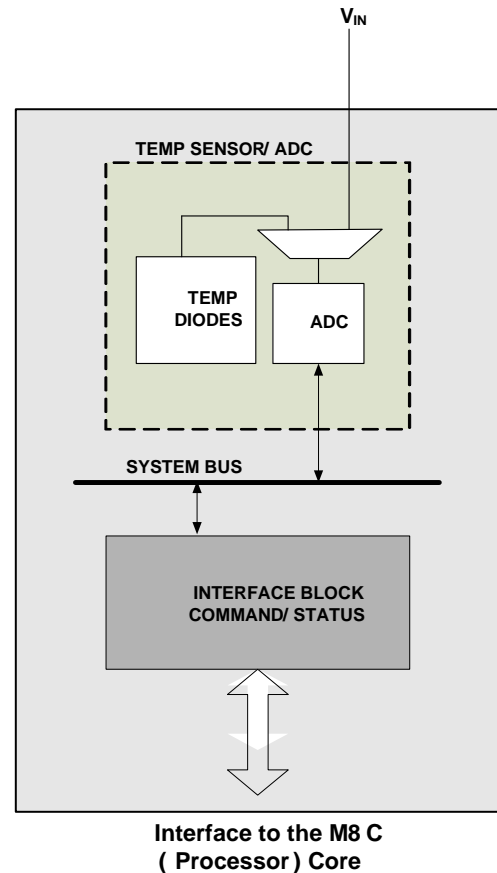
### PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as a configurable I<sup>2</sup>C slave and SPI master-slave communication interface and various system resets supported by the M8C.

### 10 bit ADC

The ADC on PProC-EMB is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog Mux Bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.



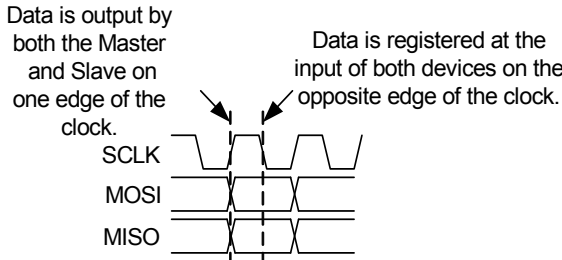
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the Analog Global Input Mux or the temperature sensor with an input voltage range of 0 V to 1.3 V, where 1.3 V is 72% of full scale.

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**SPI**

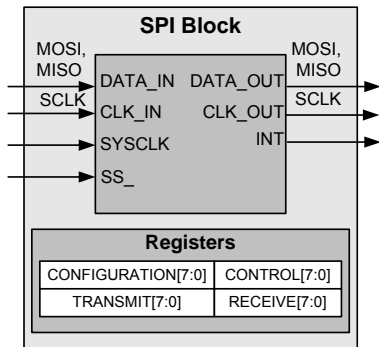
The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

**Figure 1. Basic SPI Configuration**



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

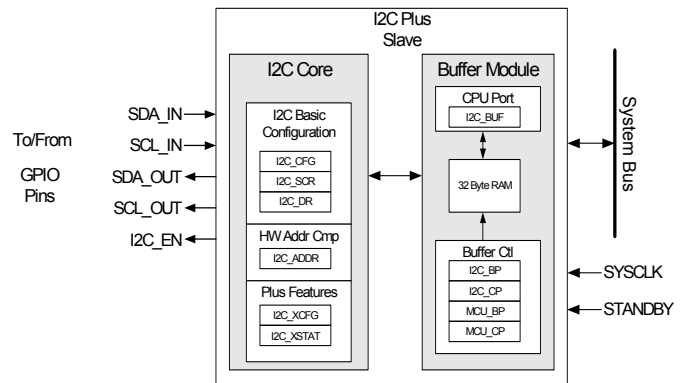
A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.



**I<sup>2</sup>C Slave**

The I<sup>2</sup>C slave enhanced communications block is a serial-to-parallel processor, designed to interface the P<sup>RO</sup>C-EMB device to a two-wire I<sup>2</sup>C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I<sup>2</sup>C-specific support for status detection and generation of framing bits. By default, the I<sup>2</sup>C Slave Enhanced module is firmware compatible with the previous generation of I<sup>2</sup>C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing.

**Figure 2. I<sup>2</sup>C Block Diagram**



The basic I<sup>2</sup>C features include

- Slave, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for clock rates of up to 400 kHz
- 7- or 10-bit addressing (through firmware support)
- SMBus operation (through firmware support)
- Enhanced features of the I<sup>2</sup>C Slave Enhanced Module include:
  - Support for 7-bit hardware address compare
  - Flexible data buffering schemes
  - A ‘no bus stalling’ operating mode

A low power bus monitoring modeThe I<sup>2</sup>C block controls the data (SDA) and the clock (SCL) to the external I<sup>2</sup>C interface through direct connections to two dedicated GPIO pins. When I<sup>2</sup>C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V LV CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

**WirelessUSB NL System**

WirelessUSB NL, optimized to operate in the 2.4-GHz ISM band, is Cypress's third generation of 2.4-GHz low-power RF technology. WirelessUSB NL implements a Gaussian frequency-shift keying (GFSK) radio using a differentiated single-mixer, closed-loop modulation design that optimizes power efficiency and interference immunity. Closed-loop modulation effectively eliminates the problem of frequency drift, enabling WirelessUSB NL to transmit up to 255-byte payloads without repeatedly having to pay power penalties for re-locking the phase-locked loop (PLL) as in open-loop designs

Among the advantages of WirelessUSB NL are its fast lock times and channel switching, along with the ability to transmit larger payloads. Use of longer payload packets, compared to multiple short payload packets, can reduce overhead, improve overall power efficiency, and help alleviate spectrum crowding.

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Combined with Cypress’s controller, WirelessUSB NL also provides the lowest bill of materials (BOM) cost solution for sophisticated PC peripheral applications such as wireless keyboards and mice, as well as best-in-class wireless performance in other demanding applications. such as toys, remote controls, fitness, automation, presenter tools, and gaming.

With PSoC-EMB 68-pin QFN, the WirelessUSB NL transceiver can add wireless capability to a wide variety of applications.

The WirelessUSB NL is a fully-integrated CMOS RF transceiver, GFSK data modem, and packet framer, optimized for use in the 2.4-GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver uses extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

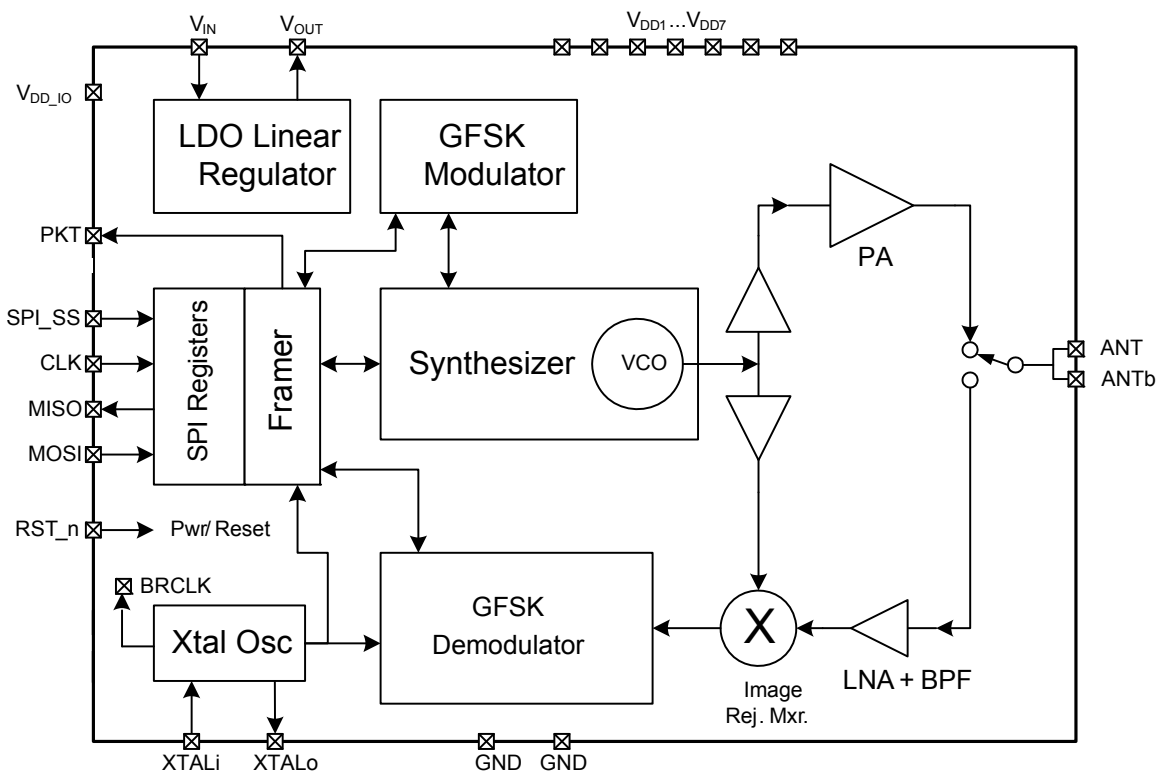
The product transmits GFSK data at approximately 0-dBm output power. Sigma-Delta PLL delivers high-quality DC-coupled transmit data path.

The low-IF receiver architecture produces good selectivity and image rejection, with typical sensitivity of -87 dBm or better on most channels. Sensitivity on channels that are integer multiples of the crystal reference oscillator frequency (12 MHz) may show approximately 5 dB degradation. Digital RSSI values are available to monitor channel quality.

On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-air data rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

For more details on the radio’s implementation details and timing requirements, please go through the WirelessUSB NL datasheet in [www.cypress.com](http://www.cypress.com).

Figure 3. WirelessUSB NL logic Block Diagram



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## Transmit Power Control

The following table lists recommended settings for register 9 for short-range applications, where reduced transmit RF power is a desirable trade off for lower current.

**Table 1. Transmit Power Control**

Power Setting Description	Typical Transmit Power (dBm)	Register 9
PA0 - Highest power	+1	0x1820
PA2 - High power	0	0x1920
PA4 - High power	-3	0x1A20
PA8 - Low power	-7.5	0x1C20
PA12 - Lower power	-11.2	0x1E20

## Power-on and Register Initialization Sequence

For proper initialization at power up,  $V_{IN}$  must ramp up at the minimum overall ramp rate no slower than shown by  $T_{VIN}$  specification in the following figure. During this time, the RST\_n line must track the  $V_{IN}$  voltage ramp-up profile to within approximately 0.2 V. Since most MCU GPIO pins automatically default to a high-Z condition at power up, it only requires a pull-up resistor. When power is stable and the MCU POR releases, and MCU begins to execute instructions, RST\_n must then be pulsed low as shown in [Figure 13](#), followed by writing Reg[27 = 0x4200. During or after this SPI transaction, the State Machine status can be read to confirm FRAMER\_ST = 1, indicating a proper initialization.

## Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource:

- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- The 3.6 V maximum input, 1.8, 2.5, or 3 V selectable output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

- A register-controlled bypass mode allows the user to disable the LDO regulator.

## Getting Started

The quickest way to understand the PSoC-EMB silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the enCoRe-V LV.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at [www.cypress.com/psoc](http://www.cypress.com/psoc).

## Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com), covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

## Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

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## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C slaves and masters
  - SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

## PSoC Designer Software Subsystems

### *Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

### *Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

### *Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

### *In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.



## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the

internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

### Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

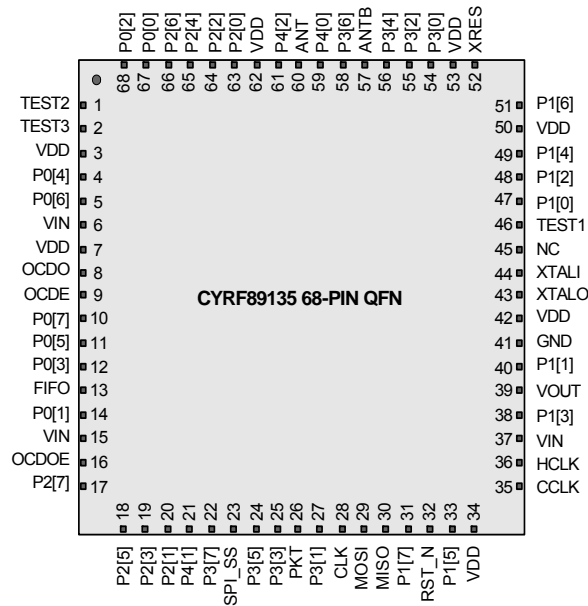
A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. The interface lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

## Pinouts

The CYRF89135-68LTXC P<sub>RoC</sub>-EMB device is available in a 68-pin QFN package, which is illustrated in the following table. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V<sub>DD</sub>, and XRES are not capable of Digital I/O.

Figure 4. 68-pin QFN pinout



## Pin Definitions

This table gives the pin definitions. [1, 2]

Pin No.	Pin Name	Description
1	TEST2	Reserved for factory test. Do not connect.
2	TEST3	Reserved for factory test. Do not connect.
3	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin
4	P0[4]	Analog I/O, Digital I/O, VREF
5	P0[6]	Analog I/O, Digital I/O
6	VIN	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator.
7	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
8	OCDO	OCD odd data IO, NC
9	OCDE	OCD even data output, NC
10	P0[7]	Analog I/O, Digital I/O, SPI CLK
11	P0[5]	Analog I/O, Digital I/O

### Notes

1. Connect all VDD pin to VOUT pin.
2. Each of the ANT and ANTB pins must be DC grounded, 20 kΩ or less.

**Pin Definitions** *(continued)*

This table gives the pin definitions. [1, 2]

Pin No.	Pin Name	Description
12	P0[3]	Analog I/O, Digital I/O, Integrating input
13	FIFO	FIFO status indicator bit
14	P0[1]	Analog I/O, Digital I/O, Integrating input
15	VIN	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator.
16	OCDOE	OCD mode direction pin, NC
17	P2[7]	Analog I/O, Digital I/O
18	P2[5]	Analog I/O, Digital I/O, XTAL Out
19	P2[3]	Analog I/O, Digital I/O, XTAL In
20	P2[1]	Analog I/O, Digital I/O
21	P4[1]	Analog I/O, Digital I/O
22	P3[7]	Analog I/O, Digital I/O
23	SPI_SS	Enable input for SPI, active low. Also used to bring device out of sleep state.
24	P3[5]	Analog I/O, Digital I/O
25	P3[3]	Analog I/O, Digital I/O
26	PKT	Transmit/receive packet status indicator bit
27	P3[1]	Analog I/O, Digital I/O
28	CLK	Clock input for SPI interface
29	MOSI	Data input for the SPI bus
30	MISO	Data output (tristate when not active)
31	P1[7]	Digital I/O, Analog I/O, I2C SCL, SPI SS
32	RST_N	RST_N Low: Chip shutdown to conserve power. Register values lost RST_N High: Turn on chip, registers restored to default value
33	P1[5]	Digital I/O, Analog I/O, I2C SDA, SPI MISO
34	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
35	CCLK	OCD CPU CLK OUTPUT, NC
36	HCLK	OCD HIGH SPEED CLK, NC
37	VIN	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator
38	P1[3]	Digital I/O, Analog I/O, SPI CLK
39	VOUT	1.8 V output from on-chip LDO. Connect to all Vdd pins, do not connect to external loads.
40	P1[1]	Digital I/O, Analog I/O, TC CLK, I2C SCL, SPI MOSI
41	GND	Ground Pin
42	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
43	XTALO	Output of the crystal oscillator gain block
44	XTALI	Input to the crystal oscillator gain block
45	NC	No Connect
46	TEST1	Reserved for factory test. Do not connect.
47	P1[0]	Analog I/O, Digital I/O, TC DATA, I2C SDA
48	P1[2]	Analog I/O, Digital I/O
49	P1[4]	Analog I/O, Digital I/O, EXT CLK
50	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.

Not recommended for new designs

**Pin Definitions** *(continued)*

This table gives the pin definitions. [1, 2]

Pin No.	Pin Name	Description
51	P1[6]	Analog I/O, Digital I/O
52	XRES	Active high external reset with internal pull down
53	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
54	P3[0]	Analog I/O, Digital I/O
55	P3[2]	Analog I/O, Digital I/O
56	P3[4]	Analog I/O, Digital I/O.
57	ANTb	Differential RF input/output.
58	P3[6]	Analog I/O, Digital I/O.
59	P4[0]	Analog I/O, Digital I/O.
60	ANT	Differential RF input/output.
61	P4[2]	Analog I/O, Digital I/O.
62	VDD	Core power supply voltage. Connect all VDD pins to VOUT pin.
63	P2[0]	Analog I/O, Digital I/O
64	P2[2]	Analog I/O, Digital I/O
65	P2[4]	Analog I/O, Digital I/O
66	P2[6]	Analog I/O, Digital I/O
67	P0[0]	Analog I/O, Digital I/O
68	P0[2]	Analog I/O, Digital I/O

Not recommended for new designs

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 2. Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>STG</sub>	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	25	125	°C
V <sub>IN</sub>		-	1.9	-	3.63	V
V <sub>DD</sub>	Supply voltage	-	-0.5	-	1.98	V
V <sub>IO</sub>	DC input voltage	-	-0.5	-	VDD + 0.5	V
V <sub>IOZ</sub> <sup>[3]</sup>	DC voltage applied to tristate	-	-0.5	-	VDD + 0.5	V
I <sub>MIO</sub>	Maximum current into any port pin	-	-25	-	50	mA
ESD	Electrostatic discharge voltage	Human body model ESD i) RF pins (ANT, ANTb) ii) Analog pins (XTALi, XTALo) iii) Remaining pins	500 500 2000	-	-	V
LU	Latch-up current	In accordance with JESD78 standard	-	-	140	mA

## Operating Temperature

**Table 3. Operating Temperature**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Ambient temperature	-	0	-	70	°C

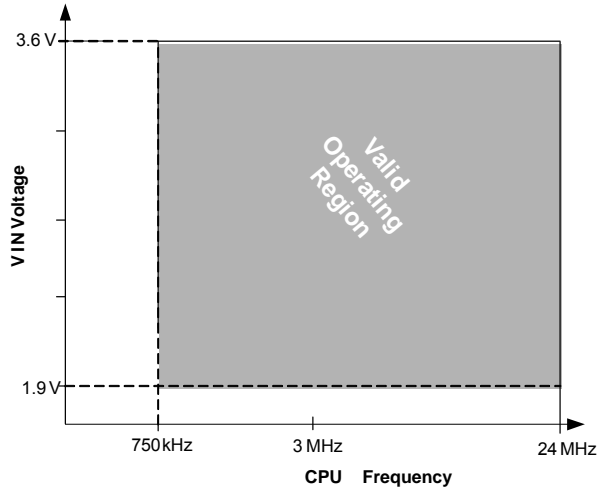
**Note**

3. Port1 pins are hot-swap capable with I/O configured in High-Z mode, and pin input voltage above V<sub>IN</sub>.

### Electrical Specifications – PSoC Core

This section presents the DC and AC electrical specifications of the CYRF89435-68LTXC PSoC device. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 5. Voltage versus CPU Frequency



Not recommended for new designs

**DC Chip-Level Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 4. DC Chip Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>DD</sub> [4, 5]	Supply voltage	See table titled <a href="#">DC POR and LVD Specifications on page 20</a> .	1.71	–	3.6	V
I <sub>DD24</sub>	Supply current, IMO = 24 MHz	Conditions are V <sub>DD</sub> ≤ 3.0 V, T <sub>A</sub> = 25 °C, CPU = 24 MHz No I2C/SPI	–	2.9	4.0	mA
I <sub>DD12</sub>	Supply current, IMO = 12 MHz	Conditions are V <sub>DD</sub> ≤ 3.0 V, T <sub>A</sub> = 25 °C, CPU = 12 MHz No I2C/SPI	–	1.7	2.6	mA
I <sub>DD6</sub>	Supply current, IMO = 6 MHz	Conditions are V <sub>DD</sub> ≤ 3.0 V, T <sub>A</sub> = 25 °C, CPU = 6 MHz No I2C/SPI	–	1.2	1.8	mA
I <sub>SB1</sub>	Standby current with POR, LVD, and Sleep timer	V <sub>DD</sub> ≤ 3.0V, T <sub>A</sub> = 25 °C, I/O regulator turned off	–	1.1	1.5	μA
I <sub>SB0</sub>	Deep sleep current	V <sub>DD</sub> ≤ 3.0 V, T <sub>A</sub> = 25 °C, I/O regulator turned off	–	0.1	–	μA

Not recommended for new designs

**Notes**

4. If powering down in standby sleep mode, to properly detect and recover from a V<sub>IN</sub> brown out condition any of the following actions must be taken:  
 Bring the device out of sleep before powering down.  
 Assure that V<sub>IN</sub> falls below 100 mV before powering back up.  
 Set the No Buzz bit in the OSC\_CR0 register to keep the voltage monitoring circuit powered during sleep.  
 Increase the buzz rate to assure that the falling edge of V<sub>IN</sub> is captured. The rate is configured through the PSSDC bits in the SLP\_CFG register.  
 For the referenced registers, refer to the *CY8C20X36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V<sub>IN</sub> brown out conditions to be detected for edge rates slower than 1V/ms.
5. Always greater than 50 mV above V<sub>PPOR1</sub> voltage for falling supply.
6. Always greater than 50 mV above V<sub>PPOR2</sub> voltage for falling supply.
7. Always greater than 50 mV above V<sub>PPOR3</sub> voltage for falling supply.

**DC GPIO Specifications**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and  $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ , or 1.9 V to 2.4 V and  $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

**Table 5. 2.4 V to 3.0 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> = 0.2 mA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.40	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.50	–	–	V
V <sub>OH5A</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> < 10 μA, V <sub>IN</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V <sub>OH6A</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> = 1 mA, V <sub>IN</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V <sub>IL</sub>	Input low voltage	–	–	–	0.72	V
V <sub>IH</sub>	Input high voltage	–	1.40	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (absolute value)	–	–	1	1000	nA
C <sub>PIN</sub>	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
V <sub>ILLVT2.5</sub>	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	–	–	V
V <sub>IHLVT2.5</sub>	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2	–	–	V

Not recommended for new designs



**Table 6. 1.9 V to 2.4 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> = 10 μA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> = 0.5 mA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.50	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I <sub>OH</sub> = 100 μA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>IN</sub> – 0.50	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V <sub>IL</sub>	Input low voltage	–	–	–	0.30 × V <sub>IN</sub>	V
V <sub>IH</sub>	Input high voltage	–	0.65 × V <sub>IN</sub>	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (absolute value)	–	–	1	1000	nA
C <sub>PIN</sub>	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Not recommended for new designs

### Analog DC Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 7. DC Analog Mux Bus Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>SW</sub>	Switch resistance to common analog bus	–	–	–	800	Ω
R <sub>GND</sub>	Resistance of initialization switch to GND	–	–	–	800	Ω

The maximum pin voltage for measuring R<sub>SW</sub> and R<sub>GND</sub> is 1.8 V.

### DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 8. DC Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>LPC</sub>	Low power comparator (LPC) common mode	Maximum voltage limited to V <sub>IN</sub>	0.0	–	1.8	V
I <sub>LPC</sub>	LPC supply current	–	–	10	40	μA
V <sub>OSLPC</sub>	LPC voltage offset	–	–	3	30	mV

### Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: 0 °C ≤ T<sub>A</sub> ≤ 70 °C, 1.9 V ≤ V<sub>IN</sub> ≤ 3.6 V.

**Table 9. Comparator User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
t <sub>COMP</sub>	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to (V <sub>IN</sub> – 0.2 V)	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	μA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0	–	1.5	V

Not recommended for new designs

**ADC Electrical Specifications**
**Table 10. ADC User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>Input</b>						
V <sub>IN</sub>	Input voltage range	–	0	–	V <sub>REFADC</sub>	V
C <sub>IIN</sub>	Input capacitance	–	–	–	5	pF
R <sub>IN</sub>	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
<b>Reference</b>						
V <sub>REFADC</sub>	ADC reference voltage	–	1.14	–	1.26	V
<b>Conversion Rate</b>						
F <sub>CLK</sub>	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2 <sup>Resolution</sup> /Data Clock)	–	23.43	–	kSPS
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2 <sup>resolution</sup> /data clock)	–	5.85	–	kSPS
<b>DC Accuracy</b>						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E <sub>OFFSET</sub>	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E <sub>GAIN</sub>	Gain error	For any resolution	–5	–	+5	%FSR
<b>Power</b>						
I <sub>ADC</sub>	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V <sub>IN</sub> > 3.0 V)	–	24	–	dB
		PSRR (V <sub>IN</sub> < 3.0 V)	–	30	–	dB

Not recommended for new designs

**DC POR and LVD Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 11. DC POR and LVD Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>POR1</sub>	2.36 V selected in PSoC Designer PORLEV[1:0] = 00b, HPOR = 1	V <sub>IN</sub> must be greater than or equal to 1.9 V during startup, reset from the XRES pin, or reset from watchdog.	–	2.36	2.41	V
V <sub>POR2</sub>	2.60 V selected in PSoC Designer PORLEV[1:0] = 01b, HPOR = 1		–	2.60	2.66	
V <sub>POR3</sub>	2.82 V selected in PSoC Designer PORLEV[1:0] = 10b, HPOR = 1		–	2.82	2.95	
V <sub>LVD0</sub>	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V <sub>LVD1</sub>	2.71 V selected in PSoC Designer		2.64 <sup>[8]</sup>	2.71	2.78	
V <sub>LVD2</sub>	2.92 V selected in PSoC Designer		2.85 <sup>[9]</sup>	2.92	2.99	
V <sub>LVD3</sub>	3.02 V selected in PSoC Designer		2.95 <sup>[10]</sup>	3.02	3.09	
V <sub>LVD4</sub>	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V <sub>LVD5</sub>	1.90 V selected in PSoC Designer		1.84	1.90	2.32	

Not recommended for new designs

**Notes**

- 8. Always greater than 50 mV above V<sub>PPOR1</sub> voltage for falling supply.
- 9. Always greater than 50 mV above V<sub>PPOR2</sub> voltage for falling supply.
- 10. Always greater than 50 mV above V<sub>PPOR3</sub> voltage for falling supply.

**DC Programming Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 12. DC Programming Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>IN</sub>	Supply voltage for flash write operations	–	1.91	–	3.6	V
I <sub>DDP</sub>	Supply current during programming or verify	–	–	5	25	mA
V <sub>ILP</sub>	Input low voltage during programming or verify	See the appropriate <a href="#">DC GPIO Specifications on page 16</a>	–	–	V <sub>IL</sub>	V
V <sub>IHP</sub>	Input high voltage during programming or verify	See the appropriate <a href="#">DC GPIO Specifications on page 16</a>	V <sub>IH</sub>	–	–	V
I <sub>ILP</sub>	Input current when Applying V <sub>ILP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I <sub>IHP</sub>	Input current when applying V <sub>IHP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V <sub>OLP</sub>	Output low voltage during programming or verify		–	–	+ 0.75	V
V <sub>OHP</sub>	Output high voltage during programming or verify	See appropriate <a href="#">DC GPIO Specifications on page 16</a> . For V <sub>IN</sub> > 3 V use V <sub>OH4</sub> in <a href="#">Table 3 on page 13</a> .	V <sub>OH</sub>	–	V <sub>IN</sub>	V
Flash <sub>ENPB</sub>	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash <sub>DR</sub>	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Not recommended for new designs

**DC I<sup>2</sup>C Specifications**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3, 2.4 V to 3.0 V and 0 °C ≤ T<sub>A</sub> ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T<sub>A</sub> ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

**Table 13. DC I<sup>2</sup>C Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>IL</sub> I <sup>2</sup> C	Input low level	3.1 V ≤ V <sub>IN</sub> ≤ 3.6 V	–	–	0.25 × V <sub>IN</sub>	V
		2.5 V ≤ V <sub>IN</sub> ≤ 3.0 V	–	–	0.3 × V <sub>IN</sub>	V
		1.9 V ≤ V <sub>IN</sub> ≤ 2.4 V	–	–	0.3 × V <sub>IN</sub>	V
V <sub>IH</sub> I <sup>2</sup> C	Input high level	1.9 V ≤ V <sub>IN</sub> ≤ 3.6 V	0.65 × V <sub>IN</sub>	–	–	V

**DC Reference Buffer Specifications**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and 0 °C ≤ T<sub>A</sub> ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T<sub>A</sub> ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

**Table 14. DC Reference Buffer Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>Ref</sub>	Reference buffer output	1.9 V to 3.6 V	1	–	1.05	V
V <sub>RefHi</sub>	Reference buffer output	1.9 V to 3.6 V	1.2	–	1.25	V

Not recommended for new designs

**AC Chip-Level Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 15. AC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>IMO24</sub>	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F <sub>IMO12</sub>	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F <sub>IMO6</sub>	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F <sub>CPU</sub>	CPU frequency	–	0.75	–	25.20	MHz
F <sub>32K1</sub>	ILO frequency	–	19	32	50	kHz
F <sub>32K_U</sub>	ILO untrimmed frequency	–	13	32	82	kHz
DC <sub>IMO</sub>	Duty cycle of IMO	–	40	50	60	%
DC <sub>ILO</sub>	ILO duty cycle	–	40	50	60	%
SR <sub>POWER_UP</sub>	Power supply slew rate	VIN slew rate during power-up	–	–	250	V/ms
t <sub>XRST</sub>	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t <sub>XRST2</sub>	External reset pulse width after power-up	Applies after part has booted	10	–	–	μs
t <sub>OS</sub>	Startup time of ECO	–	–	1	–	s
t <sub>JIT_IMO</sub>	N = 32	6 MHz IMO cycle-to-cycle jitter (RMS)	–	0.7	6.7	ns
		6 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	4.3	29.3	ns
		6 MHz IMO period jitter (RMS)	–	0.7	3.3	ns
		12 MHz IMO cycle-to-cycle jitter (RMS)	–	0.5	5.2	ns
		12 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	2.3	5.6	ns
		12 MHz IMO period jitter (RMS)	–	0.4	2.6	ns
		24 MHz IMO cycle-to-cycle jitter (RMS)	–	1.0	8.7	ns
		24 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	1.4	6.0	ns
		24 MHz IMO period jitter (RMS)	–	0.6	4.0	ns

Not recommended for new designs

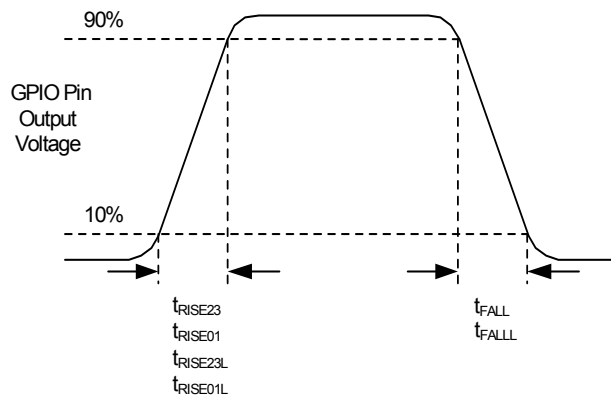
**AC GPIO Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 16. AC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>GPIO</sub>	GPIO operating frequency	Normal strong mode Port 0, 1	0	–	6 MHz for 1.9 V < VIN < 2.40 V	MHz
			0	–	12 MHz for 2.40 V < VIN < 3.6 V	MHz
t <sub>RISE23</sub>	Rise time, strong mode, Clload = 50 pF Port 2 or 3 or 4 pins	VIN = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
t <sub>RISE23L</sub>	Rise time, strong mode low supply, Clload = 50 pF, Port 2 or 3 or 4 pins	VIN = 1.9 to 3.0 V, 10% to 90%	15	–	80	ns
t <sub>RISE01</sub>	Rise time, strong mode, Clload = 50 pF, Ports 0 or 1	VIN = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
t <sub>RISE01L</sub>	Rise time, strong mode low supply, Clload = 50 pF, Ports 0 or 1	VIN = 1.9 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
t <sub>FALL</sub>	Fall time, strong mode, Clload = 50 pF, all ports	VIN = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
t <sub>FALLL</sub>	Fall time, strong mode low supply, Clload = 50 pF, all ports	VIN = 1.9 to 3.0 V, 10% to 90%	10	–	70	ns

**Figure 6. GPIO Timing Diagram**



Not recommended for new designs



**AC Comparator Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 17. AC Low Power Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$t_{LPC}$	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

**AC External Clock Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

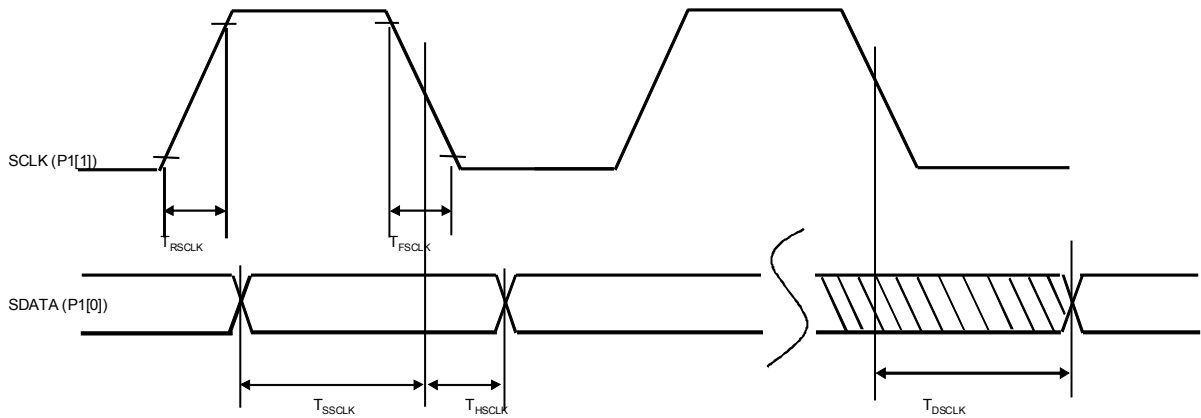
**Table 18. AC External Clock Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{OSCEXT}$	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	$\mu$ s

Not recommended for new designs

AC Programming Specifications

Figure 7. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t <sub>RSCLK</sub>	Rise time of SCLK	–	1	–	20	ns
t <sub>FSCLK</sub>	Fall time of SCLK	–	1	–	20	ns
t <sub>SSCLK</sub>	Data setup time to falling edge of SCLK	–	40	–	–	ns
t <sub>HSCLK</sub>	Data hold time from falling edge of SCLK	–	40	–	–	ns
F <sub>SCLK</sub>	Frequency of SCLK	–	0	–	8	MHz
t <sub>ERASEB</sub>	Flash erase time (block)	–	–	–	18	ms
t <sub>WRITE</sub>	Flash block write time	–	–	–	25	ms
t <sub>DSCLK3</sub>	Data out delay from falling edge of SCLK	3.0 ≤ V <sub>IN</sub> ≤ 3.6	–	–	85	ns
t <sub>DSCLK2</sub>	Data out delay from falling edge of SCLK	1.9 ≤ V <sub>IN</sub> ≤ 3.0	–	–	130	ns
t <sub>XRST3</sub>	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	μs
t <sub>XRES</sub>	XRES pulse length	–	300	–	–	μs
t <sub>VDDWAIT</sub>	V <sub>DD</sub> stable to wait-and-poll hold off	–	0.1	–	1	ms
t <sub>VDDXRES</sub>	V <sub>DD</sub> stable to XRES assertion delay	–	14.27	–	–	ms
t <sub>POLL</sub>	SDATA high pulse time	–	0.01	–	200	ms
t <sub>ACQ</sub>	“Key window” time after a V <sub>DD</sub> ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
t <sub>XRESINI</sub>	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	μs

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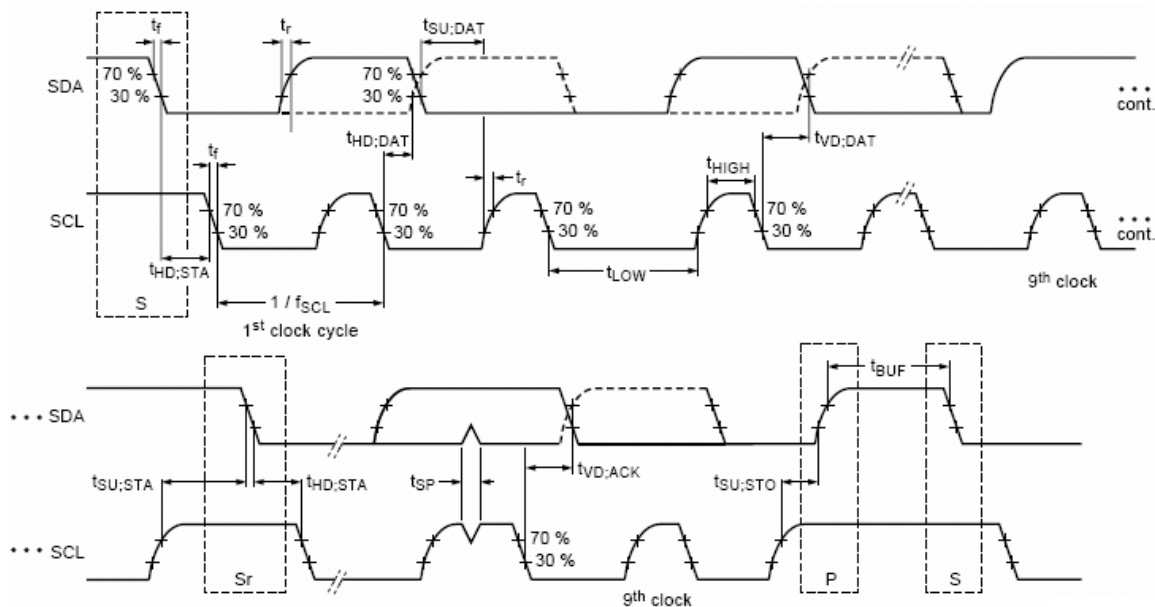
**AC I<sup>2</sup>C Specifications**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 20. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>HD;STA</sub>	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7	–	1.3	–	µs
t <sub>HIGH</sub>	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
t <sub>SU;STA</sub>	Setup time for a repeated START condition	4.7	–	0.6	–	µs
t <sub>HD;DAT</sub>	Data hold time	0	3.45	0	0.90	µs
t <sub>SU;DAT</sub>	Data setup time	250	–	100 <sup>[11]</sup>	–	ns
t <sub>SU;STO</sub>	Setup time for STOP condition	4.0	–	0.6	–	µs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t <sub>SP</sub>	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

**Figure 8. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**



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**Note**

11. A Fast-Mode I<sup>2</sup>C-bus device can be used in a standard mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT} \geq 250$  ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

Table 21. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	$V_{IN} \geq 2.4\text{ V}$ $V_{IN} < 2.4\text{ V}$	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
$t_{SETUP}$	MISO to SCLK setup time	$V_{IN} \geq 2.4\text{ V}$ $V_{IN} < 2.4\text{ V}$	60 100	– –	– –	ns ns
$t_{HOLD}$	SCLK to MISO hold time	–	40	–	–	ns
$t_{OUT\_VAL}$	SCLK to MOSI valid time	–	–	–	40	ns
$t_{OUT\_HIGH}$	MOSI high time	–	40	–	–	ns

Figure 9. SPI Master Mode 0 and 2

**SPI Master, modes 0 and 2**

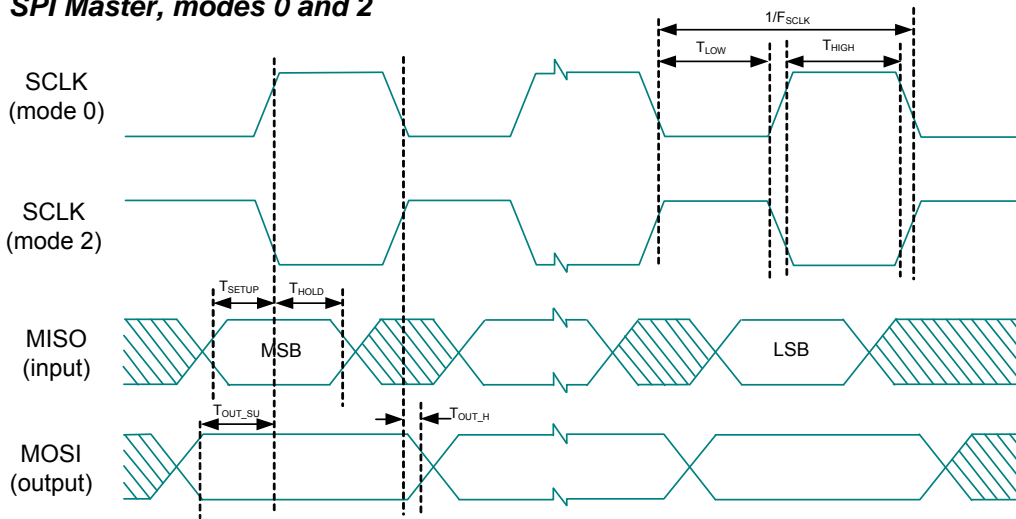
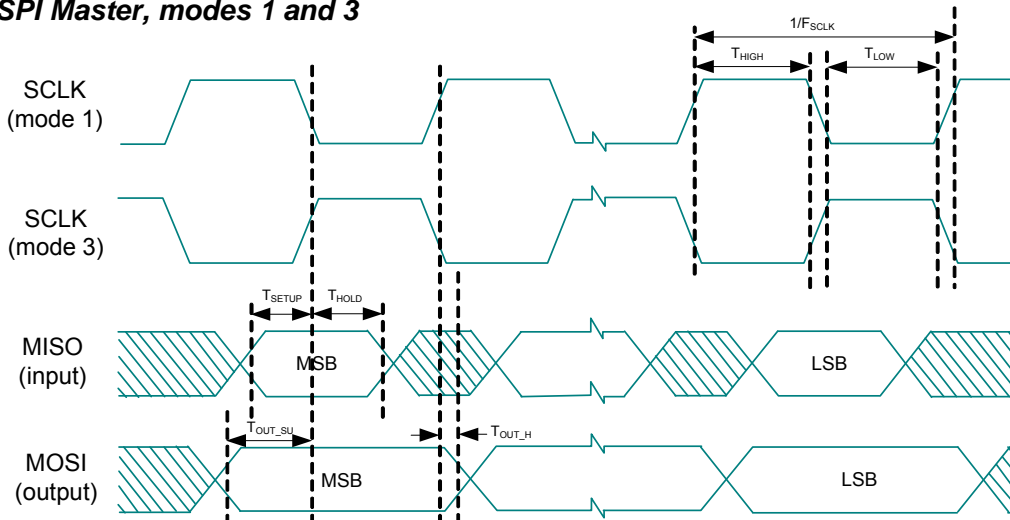


Figure 10. SPI Master Mode 1 and 3

**SPI Master, modes 1 and 3**



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Table 22. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>SCLK</sub>	SCLK clock frequency	–	–	–	4	MHz
t <sub>LOW</sub>	SCLK low time	–	42	–	–	ns
t <sub>HIGH</sub>	SCLK high time	–	42	–	–	ns
t <sub>SETUP</sub>	MOSI to SCLK setup time	–	30	–	–	ns
t <sub>HOLD</sub>	SCLK to MOSI hold time	–	50	–	–	ns
t <sub>SS_MISO</sub>	SS high to MISO valid	–	–	–	153	ns
t <sub>SCLK_MISO</sub>	SCLK to MISO valid	–	–	–	125	ns
t <sub>SS_HIGH</sub>	SS high time	–	50	–	–	ns
t <sub>SS_CLK</sub>	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
t <sub>CLK_SS</sub>	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 11. SPI Slave Mode 0 and 2

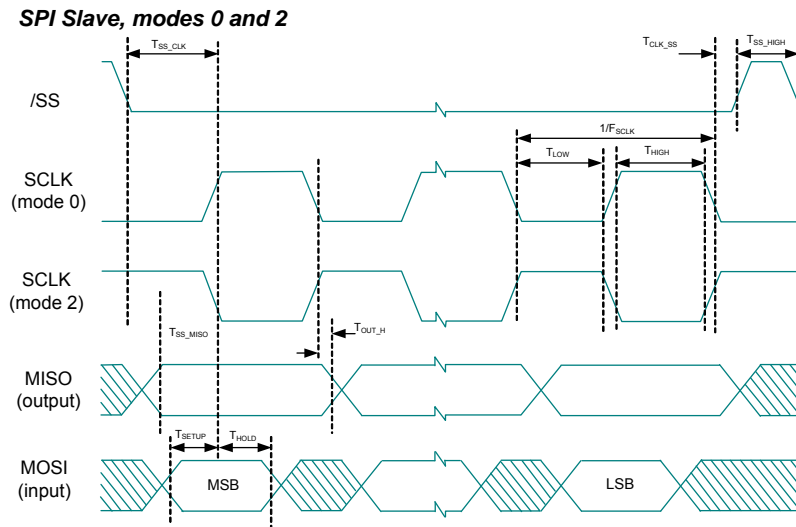
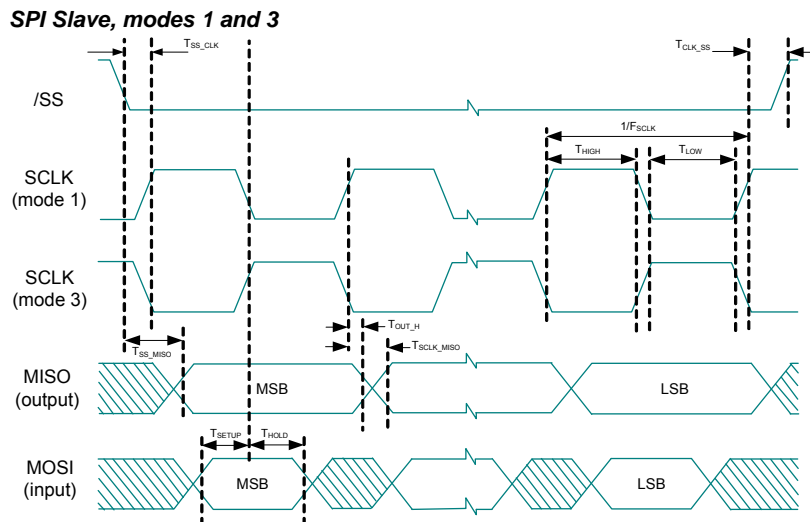


Figure 12. SPI Slave Mode 1 and 3



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**Electrical Specifications – RF Section**

Symbol	Description	Min	Typ	Max	Units	Test Condition and Notes
	Supply voltage					
V <sub>IN</sub>	DC power supply voltage range	1.9	–	3.6	VDC	Input to V <sub>IN</sub> pins
	Current consumption					
I <sub>DD_TX2</sub>	Current consumption – Tx	–	18.5	–	mA	Transmit power PA2.
I <sub>DD_TX12</sub>		–	13.7	–	mA	Transmit power PA12.
I <sub>DD_RX</sub>	Current consumption – Rx	–	18	–	mA	
I <sub>DD_IDLE1</sub>	Current consumption – idle	–	1.1	–	mA	
I <sub>DD_SLPx</sub>	Current consumption – sleep	–	1	–	μA	Temperature = +25 °C. Using firmware sleep patch. Register 27 = 0x1200, for V <sub>IN</sub> ≥ 3.00 VDC only
I <sub>DD_SLP<sub>r</sub></sub>		–	8	–	μA	Temperature = +25 °C; using firmware sleep patch Register 27 = 0x4200.
I <sub>DD_SLP<sub>h</sub></sub>		–	38	–	μA	Temperature = +70 °C 'C' grade part; using firmware sleep patch Register 27 = 0x4200
V <sub>IH</sub>	Logic input high	0.8 V <sub>IN</sub>	–	1.2 V <sub>IN</sub>	V	
V <sub>IL</sub>	Logic input low	0	–	0.8	V	
I <sub>LEAK_IN</sub>	Input leakage current	–	–	10	μA	
V <sub>OH</sub>	Logic output high	0.8 V <sub>IN</sub>	–	–	V	I <sub>OH</sub> = 100 μA source
V <sub>OL</sub>	Logic output low	–	–	0.4	V	I <sub>OL</sub> = 100 μA sink
I <sub>LEAK_OUT</sub>	Output leakage current	–	–	10	μA	MISO in tristate
T <sub>RISE_OUT</sub>	Rise/fall time (SPI MISO)	–	8	25	ns	7 pF cap. load
T <sub>RISE_IN</sub>	Rise/fall time (SPI MOSI)	–	–	25	ns	
T <sub>r_spi</sub>	CLK rise, fall time (SPI)	–	–	25	ns	Requirement for error-free register reading, writing.
F <sub>OP</sub>	Operating frequency range	2400	–	2482	MHz	Usage on-the-air is subject to local regulatory agency restrictions regarding operating frequency.
V <sub>SWR_I</sub>	Antenna port mismatch (Z <sub>0</sub> = 50 Ω)	–	<2:1	–	VSWR	Receive mode. Measured using LC matching circuit
V <sub>SWR_O</sub>		–	<2:1	–	VSWR	Transmit mode. Measured using LC matching circuit
Receive section						Measured using LC matching circuit for BER ≤ 0.1%
RxS <sub>base</sub>	Receiver sensitivity (FEC off)	–	–87	–	dBm	Room temperature only 0-ppm crystal frequency error.
RxS <sub>temp</sub>		–	–84	–	dBm	Over temperature; 0-ppm crystal frequency error.

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**Electrical Specifications – RF Section** *(continued)*

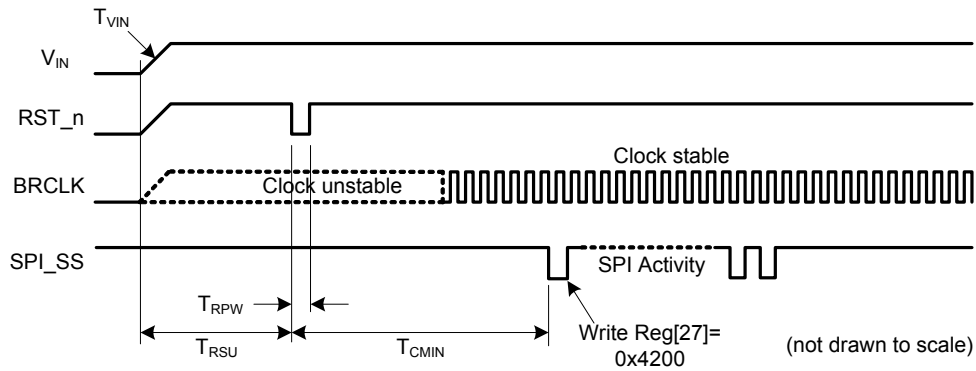
Symbol	Description	Min	Typ	Max	Units	Test Condition and Notes
RxS <sub>ppm</sub>		–	–84	–	dBm	Room temperature only 80-ppm total frequency error (± 40-ppm crystal frequency error, each end of RF link)
RxS <sub>temp+ppm</sub>		–	–80	–	dBm	Over temperature; 80-ppm total frequency error (± 40-ppm crystal frequency error, each end of RF link)
R <sub>xmax-sig</sub>	Maximum usable signal	–20	0	–	dBm	Room temperature only
T <sub>s</sub>	Data (Symbol) rate	–	1	–	µs	
Minimum Carrier/Interference ratio						For BER ≤ 0.1%. Room temperature only.
Cl <sub>_cochannel</sub>	Co-channel interference	–	+9	–	dB	–60-dBm desired signal
Cl <sub>_1</sub>	Adjacent channel interference, 1-MHz offset	–	+6	–	dB	–60-dBm desired signal
Cl <sub>_2</sub>	Adjacent channel interference, 2-MHz offset	–	–12	–	dB	–60-dBm desired signal
Cl <sub>_3</sub>	Adjacent channel interference, 3-MHz offset	–	–24	–	dB	–67-dBm desired signal
OBB	Out-of-band blocking	–	≥ –27	–	dBm	30 MHz to 12.75 GHz Measured with ACX BF2520 ceramic filter on ant. pin. –67-dBm desired signal, BER ≤ 0.1%. Room temperature only.
Transmit section						Measured using a LC matching circuit
P <sub>AVH</sub>	RF output power	–	+1	–	dBm	PA0 (PA_GN = 0, Reg9 = 0x1820). Room temperature only
P <sub>AVL</sub>		–	–11.2	–	dBm	PA12 (PA_GN = 12, Reg9 = 0x1E20). Room temperature only.
TxP <sub>fx2</sub>	Second harmonic	–	–45	–	dBm	Measured using a LC matching circuit. Room temperature only.
TxP <sub>fx3</sub>	Third and higher harmonics	–	≤ –45	–	dBm	Measured using a LC matching circuit. Room temperature only.
Modulation characteristics						
Df <sub>1avg</sub>		–	263	–	kHz	Modulation pattern: 11110000...
Df <sub>2avg</sub>		–	255	–	kHz	Modulation pattern: 10101010...
In-band spurious emission						
IBS <sub>_2</sub>	2-MHz offset	–	–	–20	dBm	
IBS <sub>_3</sub>	3-MHz offset	–	–	–30	dBm	
IBS <sub>_4</sub>	≥ 4-MHz offset	–	≤ –30	–	dBm	
RF VCO and PLL section						
F <sub>step</sub>	Channel (Step) size	–	1	–	MHz	

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**Electrical Specifications – RF Section** *(continued)*

Symbol	Description	Min	Typ	Max	Units	Test Condition and Notes
L <sub>100k</sub>	SSB phase noise		-75	-	dBc/Hz	100-kHz offset
L <sub>1M</sub>			-105	-	dBc/Hz	1-MHz offset
dF <sub>X0</sub>	Crystal oscillator frequency error	-40	-	+40	ppm	Relative to 12-MHz crystal reference frequency
T <sub>HOP</sub>	RF PLL settling time	-	100	150	μs	Settle to within 30 kHz of final value. AutoCAL off.
T <sub>HOP_AC</sub>		-	250	350	μs	Settle to within 30 kHz of final value. AutoCAL on.
LDO voltage regulator section						
V <sub>DO</sub>	Dropout voltage	-	0.17	0.3	V	Measured during receive state

**Figure 13. Power-on and Register Programming Sequence**



**Table 23. Initialization Timing Requirements**

Timing Parameter	Min	Max	Unit	Notes
T <sub>RSU</sub>	-	30 / 150	ms	30 ms Reset setup time necessary to ensure complete Reset for VIN=6.5mV/s, 150 ms Reset setup time necessary to ensure complete Reset for VIN=2mV/s
T <sub>RPW</sub>	1	10	μs	Reset pulse width necessary to ensure complete reset
T <sub>CMIN</sub>	3	-	ms	Minimum recommended crystal oscillator and APLL settling time
T <sub>VIN</sub>	-	6.5 / 2	mV/s	Maximum ramp time for V <sub>IN</sub> , measured from 0 to 100% of final voltage. For example, if V <sub>IN</sub> = 3.3 V, the max ramp time is 6.5 × 3.3 = 21.45 ms. If V <sub>IN</sub> = 1.9 V, the max ramp time = 6.5 × 1.9 = 12.35 ms. Reset setup time necessary to ensure complete Reset for VIN=6.5mV/s Reset setup time necessary to ensure complete Reset for VIN=6.5mV/s Reset setup time necessary to ensure complete Reset for VIN=6.5mV/s

■ After register initialization, CYRF89435 68-pin QFN is ready to transmit or receive.

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Figure 14. Initialization Flowchart

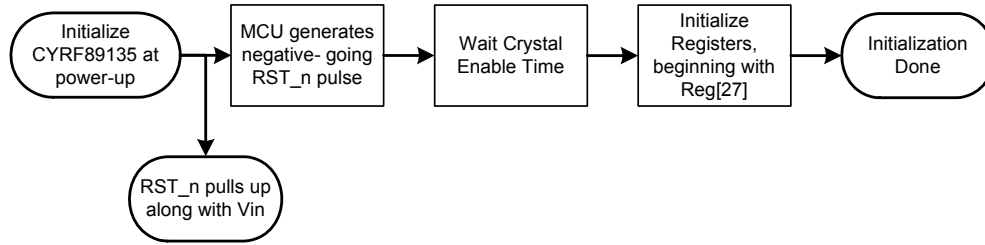


Table 24. SPI Timing Requirements

Timing Parameter	Min	Max	Unit	Notes
T <sub>SS</sub>	20	–	ns	Setup time from assertion of SPI_SS to CLK edge
T <sub>SSH</sub>	200	–	ns	Hold time required deassertion of SPI_SS
T <sub>SCKH</sub>	20	–	ns	CLK minimum high time
T <sub>SCKL</sub>	20	–	ns	CLK minimum low time
T <sub>SCK</sub>	83	–	ns	Maximum CLK clock is 12 MHz
T <sub>SSU</sub>	10	–	ns	MOSI setup time
T <sub>SHD</sub>	10	–	ns	MOSI hold time
T <sub>SS_SU</sub>	10	–	ns	Before SPI_SS enable, CLK hold low time requirement
T <sub>SS_HD</sub>	200	–	ns	Minimum SPI inactive time
T <sub>SDO</sub>	–	35	ns	MISO setup time, ready to read
T <sub>SDO1</sub>	–	5	ns	If MISO is configured as tristate, MISO assertion time
T <sub>SDO2</sub>	–	250	ns	If MISO is configured as tristate, MISO deassertion time
T1 Min_R50	350	–	ns	When reading register 50 (FIFO)
T1 Min	83	–	ns	When writing Register 50 (FIFO), or reading/writing any registers other than register 50.

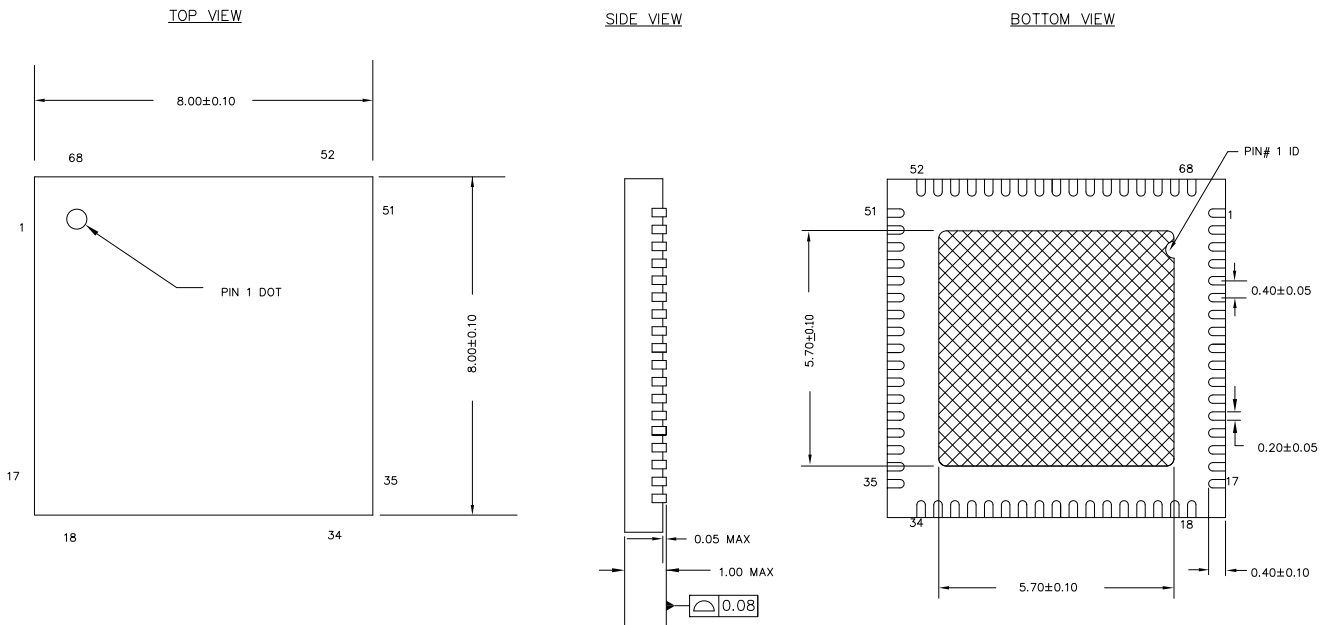
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## Packaging Information


This section illustrates the packaging specifications for the CYRF89135-68LTXC PSoC device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

**Figure 15. 68-pin QFN (8 × 8 × 1.0 mm) LT68 5.7 × 5.7 E-Pad (Sawn Type) Package Outline, 001-09618**



**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 \*E

### Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at [http://www.amkor.com/products/notes\\_papers/MLFAppNote.pdf](http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).
- Pinned vias for thermal conduction are not required for the low power PSoC device.

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**Thermal Impedances**

**Table 25. Thermal Impedances per Package**

Package	Typical $\theta_{JA}$ <sup>[12]</sup>	Typical $\theta_{JC}$
68-pin QFN <sup>[13]</sup>	29 °C/W	23 °C/W

**Capacitance on Crystal Pins**

**Table 26. Typical Package Capacitance on Crystal Pins**

Package	Package Capacitance
68-pin QFN	3.3 pF

**Solder Reflow Specifications**

Table 27 shows the solder reflow temperature limits that must not be exceeded.

**Table 27. Solder Reflow Specifications**

Package	Maximum Peak Temperature ( $T_C$ )	Maximum Time above $T_C - 5$ °C
68-pin QFN	240 °C	260 °C

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**Notes**

12.  $T_J = T_A + \text{Power} \times \theta_{JA}$ .

13. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

## Development Tool Selection

### Software

#### *PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at <http://www.cypress.com>.

#### *PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at <http://www.cypress.com>.

### Development Kits

All development kits are sold at the Cypress Online Store.

#### *CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29X66A Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- 2 CY8C29466A-24PXI 28-PDIP Chip Samples

### Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

#### *CY8CKIT-002 - MiniProg 3*

The *CY8CKIT-002 - MiniProg 3* kit enables the user to program PSoC devices via the MiniProg3 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- USB 2.0 cable to connect it to PC

#### *CY8CKIT-006 PSoC® 3 LCD Segment Drive Evaluation Kit*

Cypress's PSoC programmable system-on-chip architecture gives you the freedom to not only imagine revolutionary new products, but the capability to also get those products to market faster than anyone else. The ability to drive a 5V display on 0.5V of input and the ability to drive multiple displays on one PSoC device can translate to the ultimate in design freedom, lower BOM costs and new product differentiators with this easy to use evaluation kit. The kit contains:

- PSoC 3 LCD Segment Drive Evaluation Board
- 9V Battery
- 12V Wall Power Supply
- MiniProg3 Programmer / Debugger
- USB Cable (to connect MiniProg3 to the PC)
- Kit Stand
- Quick Start Guide
- Kit CD, which includes: PSoC Creator, PSoC Programmer, Projects and Documentation

### Device Programmers

Firmware needs to be downloaded to PSoC-EMB device only at 3.3 V using MiniProg3 Programmer. This Programmer kit can be purchased from Cypress Store using part# 'CY8CKIT-002-MiniProg3'. It is small, compact programmer which connects PC via a USB 2.0 cable (Provided along with CY8CKIT-002)

**NOTE:** MiniProg1 Programmer should not be used as it does not support programming at 3.3 V.



## Acronyms

**Table 29. Acronyms Used in this Document**

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
EOP	end of packet
FSR	full scale range
GPIO	general purpose input/output
GUI	graphical user interface
I <sup>2</sup> C	inter-integrated circuit
ICE	in-circuit emulator
IDAC	digital analog converter current
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	mega instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debugger
POR	power on reset
PPOR	precision power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC <sup>®</sup>	Programmable System-on-Chip
SLIMO	slow internal main oscillator
SRAM	static random access memory
SNR	signal to noise ratio
QFN	quad flat no-lead
SCL	serial I2C clock
SDA	serial I2C data
SDATA	serial ISSP data
SPI	serial peripheral interface
SS	slave select
SSOP	shrink small outline package
TC	test controller
USB	universal serial bus
WLCSP	wafer level chip scale package
XTAL	crystal

## Reference Documents

- *In-system Serial Programming (ISSP) protocol for 20xx6 (AN2026C)*
- *Host Sourced Serial Programming for 20xx6 devices (AN59389)*

## Document Conventions

### Units of Measure

**Table 30. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femtofarad
g	gram
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
nF	nanofarad
ns	nanosecond
nV	nanovolt
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volt
W	watt

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## Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

## Glossary

Crosspoint connection	Connection between any GPIO combination via analog multiplexer bus.
Differential non-linearity	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
Hold time	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
I <sup>2</sup> C	It is a serial multi-master bus used to connect low speed peripherals to MCU.
Integral nonlinearity	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
Latch-up current	Current at which the latch-up test is conducted according to JESD78 standard (at 125 degree Celsius)
Power supply rejection ratio (PSRR)	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
Scan	The conversion of all sensor capacitances to digital values.
Setup time	Period required to prepare a device, machine, process, or system for it to be ready to function.
Signal-to-noise ratio	The ratio between a capacitive finger signal and system noise.
SPI	Serial peripheral interface is a synchronous serial data link standard.

**Document History Page**

Document Title: CYRF89135, PRoC™ - Embedded Document Number: 001-86331				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3924802	AKHL	04/03/2013	New silicon document.
*A	5742799	SGUP	05/19/2017	Added watermark "Not recommended for new designs" across the document. Updated to new template.

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