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Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CYUSB4347
CYUSB4357

HX3PD USB 3.1 Gen 2 Type-C Hub with PD

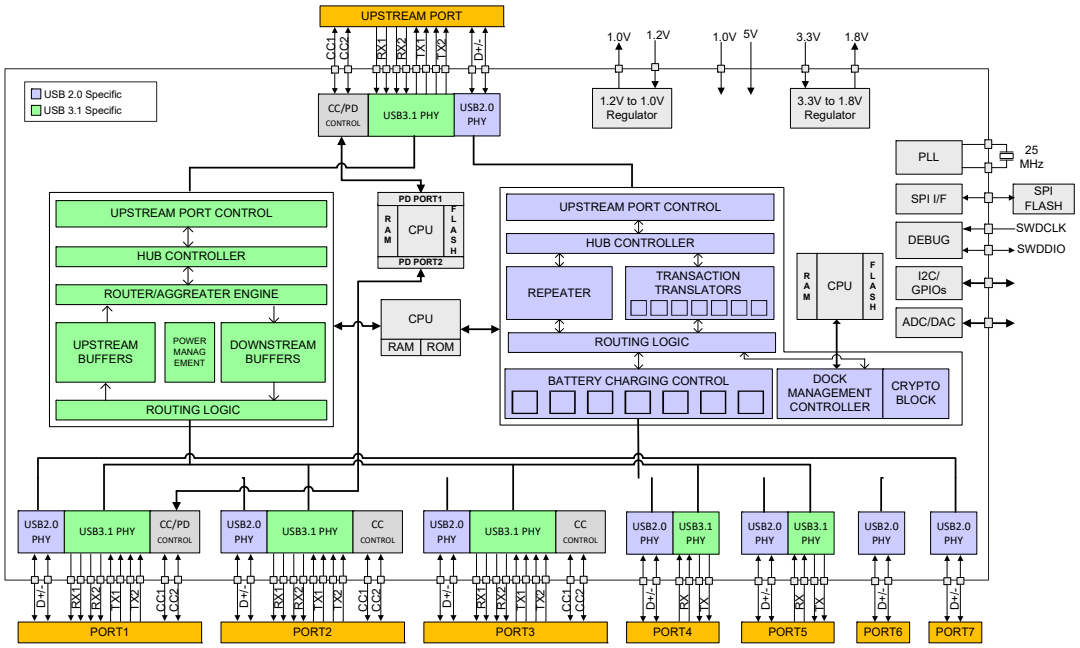
Functional Description

HX3PD is a family of USB 3.1 Gen 2 Type-C hub with USB Power Delivery (PD) that complies with the USB 3.1 Gen 2 (10 Gbps) specification, and the latest Type-C and PD standards. HX3PD supports SuperSpeed USB (10 Gbps), SuperSpeed (5 Gbps), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS) on selective ports. HX3PD provides a complete Type-C and USB PD port controller solution in Upstream (US) and one Downstream (DS) port.

Features

- USB-IF Certified USB 3.1 Gen 2 Hub Silicon, TID# 5030000008
- USB 3.1 Gen 2-compliant Hub Controller with 7 downstream ports
  - Five downstream ports support SS (10 Gbps), SS (5 Gbps), and are backward-compatible with HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps)
  - Two downstream ports support HS, and are backward-compatible with FS, and LS
  - SS (10 Gbps), SS (5 Gbps) and USB 2.0 Link Power Management (LPM)
  - Dedicated Hi-Speed Transaction Translators (Multi-TT)
- Integrated Type-C transceivers, supporting Type-C plug orientation
  - Type-C supported in four ports (1 US port and 3 DS ports)
  - Integrated transceiver (baseband PHY)
  - Integrated UFP (R_D), and current sources for DFP (R_P)
- Integrated PD controllers, supporting PD 3.0 specification in US port and 1 DS port
- Upstream: Configurable as either Type-C or Type-B port
- Downstream: Configurable as either three Type-C and four Type-A ports, or seven Type-A ports
- Compound USB PD hub with integrated USB device controller support:
  - USB Billboard
  - In-system firmware upgrade
  - Vendor specific messaging
- Integrated Dock Management Controller support
  - Signed and unsigned firmware updates
  - Firmware upgrade over USB
  - Dynamic configurations of port enable and disable from Embedded Controllers over I2C
- Charging Standard support:
  - USB PD 3.0, Battery Charging v1.2 and Apple Charging Standards
- PD policy engine configures power profiles dynamically
- Ghost Charge™: Charging DS port without US connection
- 192-ball BGA (12 mm × 12 mm, 0.8-mm ball-pitch)

Block Diagram



Contents

Architecture Overview

The Block Diagram on page 1 shows the HX3PD architecture. HX3PD consists of two independent hub controllers (SS (10 Gbps) and USB 2.0), the Arm® Cortex®-M0 CPU subsystem, 2-port USB-PD controllers, Dock Management Controller (DMC), SPI interface, Serial communication block, and GPIOs.

SS (10 Gbps) Hub Controller

This block supports the SS (10 Gbps) hub functionality based on the USB 3.1 Gen 2 (10 Gbps) specification. The SS (10 Gbps) hub controller supports the following:

- USB precision time management (PTM)
- Link power management (U0, U1, U2, U3 states)
- Store and forward packet architecture
- Full-duplex data transmission

USB 2.0 Hub Controller

This block supports the LS, FS, and HS hub functionalities. It includes the repeater, frame timer, and seven transaction translators. The USB 2.0 hub controller block supports the following:

- USB 2.0 link power management (L0, L1, L2, L3 states)
- Suspend, resume, and remote wake-up signaling
- Multi-TT (one TT for each DS port)

The hub is also integrated with USB device, which can function as a DMC and USB Billboard.

USB-PD Controller

HX3PD supports two USB PD ports, consisting of USB Type-C baseband transceivers and physical-layer logic. The USB-PD PHY consists of a transmitter and receiver that communicate Biphase Mark Coding (BMC) and 4b/5b encoded data over the CC channel based on the PD 3.0 standard. In addition, the USB-PD block includes all termination resistors (R_P and R_D) as required by the USB Type-C spec. R_P and R_D resistors are required to implement connection detection, plug orientation detection, and for establishing the USB source/sink roles.

The integrated R_P resistor enables the PD port to be configured as a DFP. The R_P resistor is implemented as a current source and can be programmed to support the complete range of current capacity on the VBUS defined in the USB Type-C Spec.

The R_D resistor is used to identify the HX3PD port as a UFP in a DRP application. The R_D resistor on the CC pins is required even when the part is not powered for dead battery termination detection and charging. HX3PD's PD ports respond to all USB-PD communication.

HX3PD is designed to be fully interoperable with revision 3.0 as well as revision 2.0 of the USB PD specification. HX3PD supports Extended Messages containing data up to 260 bytes. The Extended Messages will be larger than expected by the USB-PD 2.0 hardware. To accommodate Revision 2.0 based systems, a Chunking mechanism is implemented such that Messages are limited to Revision 2.0 sizes unless it is discovered that both systems support the longer Message lengths.

The CPU in HX3PD's USB-PD controller is a Cortex-M0 32-bit MCU controller, which is optimized for low-power operation with extensive clock gating. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user. The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG.

SPI, I²C, and GPIO Interfaces

HX3PD has dedicated SPI flash interfaces, used for downloading configuration/firmware of the hub during boot-up.

HX3PD has dedicated I^2C interfaces for Hub, DMC, and PD controllers. These I^2C interfaces shall be used for configurations of individual blocks, communication between individual blocks, and/or interface with external controllers.

HX3PD contains many GPIOs which can be configured as input, output to support custom features, these I/Os can be used for serial communication with external master/slave devices. The serial communication protocols supported are I2C, SPI, and UART.

Dock Management Controller

Dock Management Controller (DMC) integrates a Full-Speed USB controller that is designed for managing the USB dock system. DMC supports USB Billboard as well as firmware download over USB to externally interfaced peripherals (over I2C/SPI).

Firmware Update Support

DMC has the capability to do firmware update to Hub controller, PD controller, DMC, and other dock components. It implements the firmware update functionality and status reporting on a vendor interface using a full-speed USB 2.0 device controller.

Unsigned Firmware Update

The firmware update procedure expects the host to send the metadata of the programmable component's FW information.

This metadata includes SHA-256 of the individual firmware image. DMC notifies the host to send the individual component's firmware image one by one and update to the dock components. DMC verifies the firmware validity by comparing the received SHA-256 with the calculated SHA-256 of the firmware received.

Signed Firmware Update

The signed firmware update follows the same procedure as the unsigned firmware update but is uses RSA-2018/SHA-256 for signing.

Contact Cypress customer support for more information on the signed firmware update.

Crypto Block

HX3PD integrates a Crypto block for hardware assisted authentication of firmware images. It supports field upgradeability of firmware in a trusted ecosystem. The Crypto block provides cryptography functionality. It includes hardware acceleration blocks for Advanced Encryption Standard (AES) block cipher, Secure Hash Algorithm (SHA), Cyclic Redundancy Check (CRC), and pseudo random number generation.

Application Diagrams

Docking Stations

Figure 1 and Figure 2 show USB-C Dock design application diagrams using HX3PD.

HX3PD integrates five chips (two 4-port USB Hubs, two USB-PD controllers, and Dock Management controller) in typical dock designs to a single chip; significantly reducing BOM and design complexity. HX3PD Dock solution provides seven downstream ports (five USB 3.1 Gen 2, and two USB 2.0) and supports PD 3.0, BC 1.2, and Apple charging standards. It also supports signed firmware upgrades via DMC, thereby enable to keep pace with future specification changes.

Figure 1. USB-C Dock for Notebook PCs

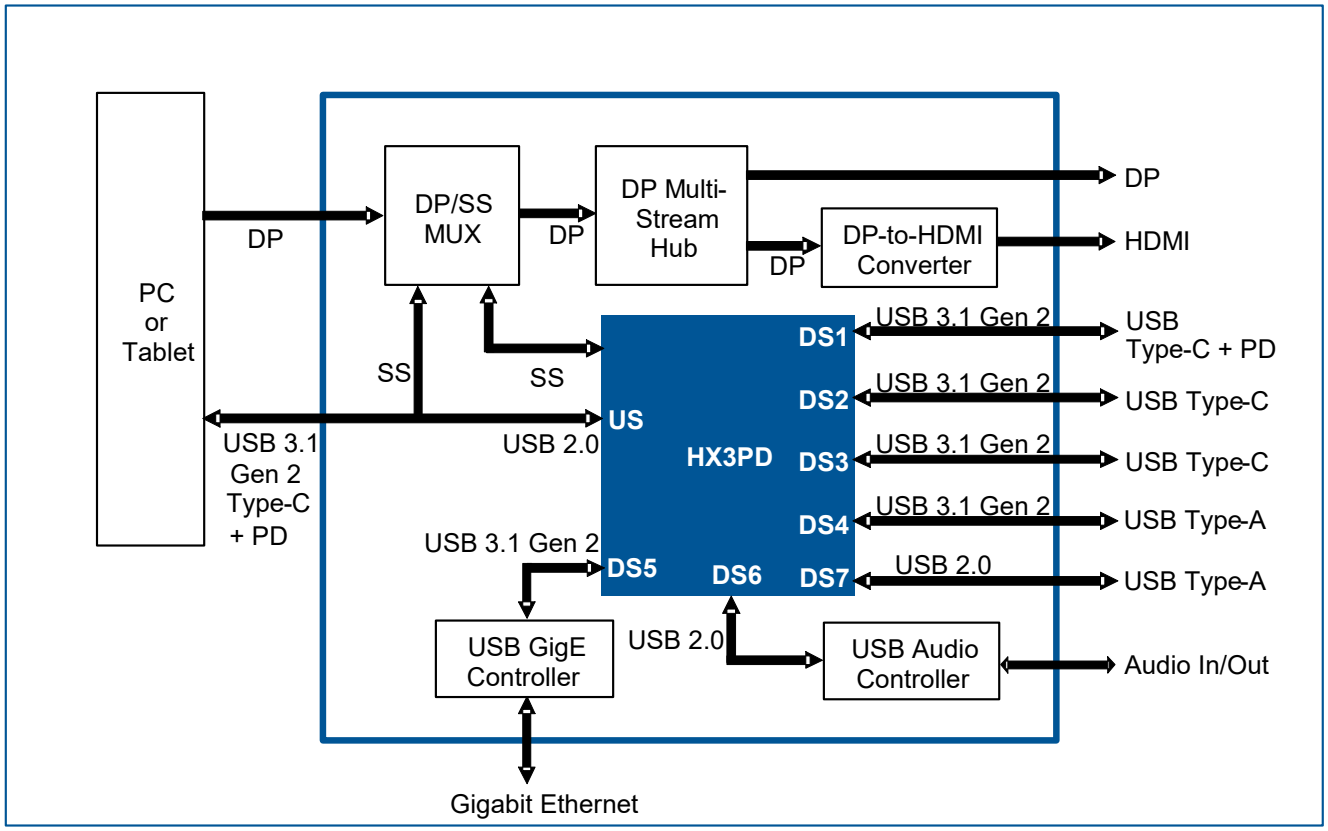
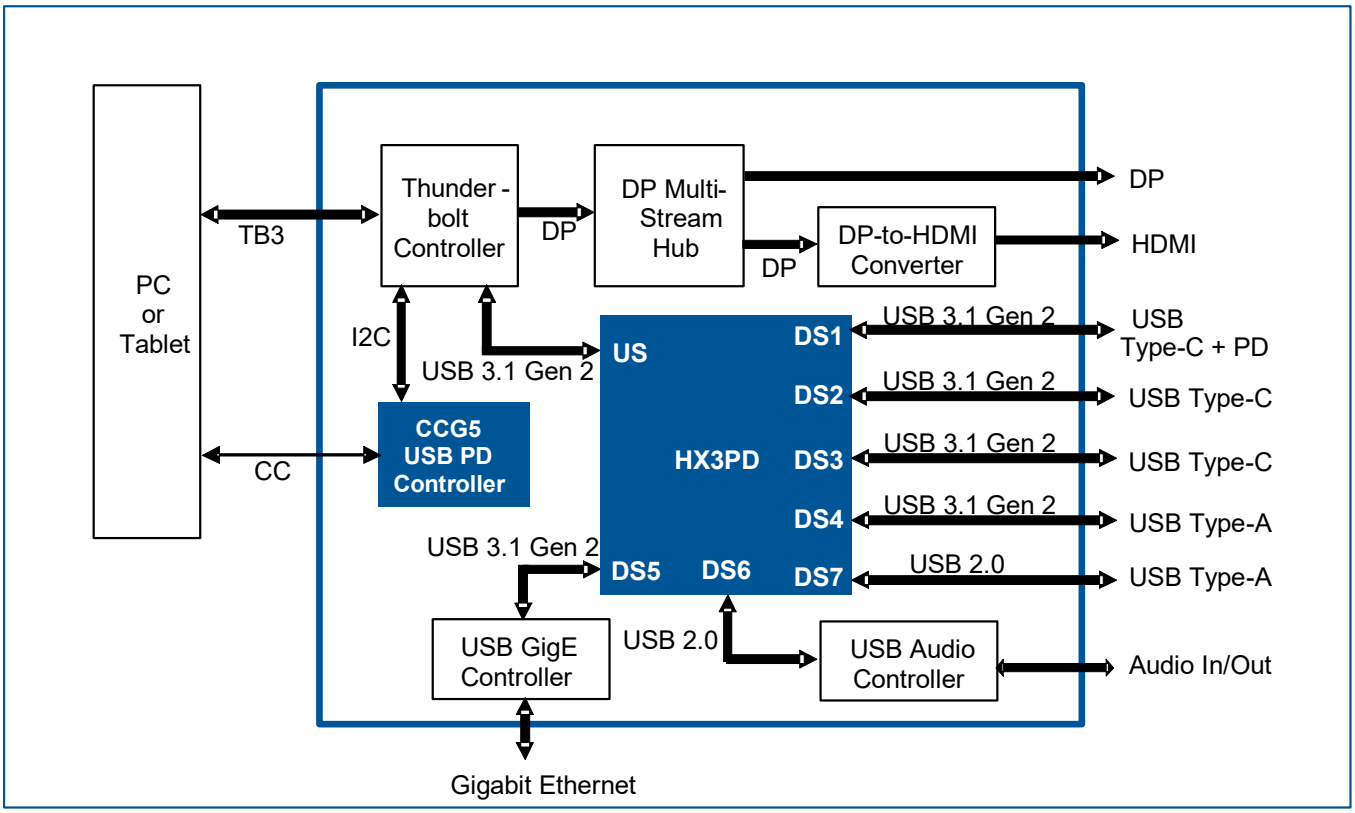


Figure 2. Thunderbolt Dock for Notebook PCs



HX3PD Product Options

Table 1. HX3PD Product Options

Marketing Part Number	Application	No of DS Ports	US PD Port	DS PD Port	Legacy Charging on DS	USB Billboard	Signed FW Download	Package
CYUSB4347	Docking Station, Monitor	7	DRP	DFP	Yes	Yes	No	192-Ball BGA
CYUSB4357	Docking Station, Monitor	7	DRP	DFP	Yes	Yes	Yes	192-Ball BGA

Pinouts

Figure 3. 192-Ball BGA Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	–	DM_P7	DP_P7	VBUS_DISCHARGE_P1	VDDD_PD	XIN	XOUT	HPD_P1	I2C_SCL2	SPI_MISO_DMC	DMC_P24	DM_P6	DP_P6	–
B	DM_P1	DP_P1	CC2_P0	SWDCLK_PD	VBUS_MON_P1	VCCD_PD	VSEL_GPIO3	VSEL_GPIO4	I2C_SDA2	SPI_SS_DMC	DMC_P25	DMC_P26	DM_P2	DP_P2
C	TXP1_P1	TXN1_P1	VDDIO	V5P0_P0	VBUS_CTRL_P1	OCP_DET_P1	CC2_P1	VCONN_MON_P1/PD_P27	VDDD_DMC	SWDIO_DMC	XRES_DMC	VDDIO	TXP2_P2	TXN2_P2
D	RXP1_P1	RXN1_P1	CC1_P0	VBUS_MON_P0	VSEL_GPIO1	VBUS_P_CTRL_P1	V5P0_P1	CC1_P1	VCCD_DMC	SWDCLK_DMC	I2C_SDA1	SPI_CLK_DMC	RXP2_P2	RXN2_P2
E	RXN2_P1	RXP2_P1	PD_P15	VBUS_P_CTRL_P0	HPD_P0	VBUS_DISCHARGE_P0	V5P0	AVDD33	PWREN_P2	PGANG	I2C_SCL1	DMC_P32	RXN1_P2	RXP1_P2
F	TXN2_P1	TXP2_P1	SWDIO_PD	DVDD10	VSEL_GPIO2	GND	GND	GND	GND	OVCUR_P2	DVDD10	SPI_MOSI_DMC	TXN1_P2	TXP1_P2
G	TXP_P5	TXN_P5	V3P3	V1P0_P7	OCP_DET_P0	GND	GND	GND	GND	I2C_SDA_HUB	V1P0_P6	V3P3	RXN_P4	RXP_P4
H	RXP_P5	RXN_P5	V1P0_P1	VBUS_CTRL_P0	SPI_MOSI_HUB	GND	GND	GND	GND	OVCUR_P6	V1P0_P2	V1P0_P2	TXN_P4	TXP_P4
J	DP_P5	DM_P5	V1P0_P1	DVDD10	SPI_MISO_HUB	PWREN_P1	GND	GND	GND	PWREN_P6	DVDD10	VDDIO	DM_P4	DP_P4
K	DM_P0	DP_P0	V1P0_P5	XRES_PD	VCONN_MON_P0/PD_P24	OVCUR_P1	SPI_CLK_HUB	AVDD10	CC1_P2	CC2_P2	PSELF	V1P0_P4	DM_P3	DP_P3
L	TXP1_P0	TXN1_P0	V3P3	V1P0_P0	OVCUR_P5	PWREN_P5	OVCUR_P4	CC1_P3	CC2_P3	VDDIO	V1P0_P3	V3P3	TXP2_P3	TXN2_P3
M	RXP1_P0	RXN1_P0	V3P3	V1P0_P0	I2C_SCL_HUB	SPI_SS_HUB	VBUS	RESET_HUB	CHIPEN	RTERM	OVCUR_P7	V1P0_P3	RXP2_P3	RXN2_P3
N	RXN2_P0	RXP2_P0	PWREN_P4	V1P0_MEM_B	V1P0_MEM_A	V1P2	GPIO4_HUB	V1P0_PHY	V1P0_PHY	FB	PWREN_P3	OVCUR_P3	RXP1_P3	RXN1_P3
P	–	TXN2_P0	TXP2_P0	V1P2	V1P2	V1P2	GPIO3_HUB	V1P0_PHY	V1P0_PHY	V3P3_REG	PWREN_P7	TXP1_P3	TXN1_P3	–

Refer to the Application Note “AN222944 - HX3PD Hardware Design Guidelines and Checklist” for recommendation on individual pin schematics.

Pin Description

No.	Pin Name	Type	Pin Number	Description
Upstream Port USB Signals				
1	DP_P0	I/O	K2	Upstream port USB 2.0 data plus
2	DM_P0	I/O	K1	Upstream port USB 2.0 data minus
3	TXP1_P0	O	L1	Upstream port, SuperSpeed transmit plus lane 1
4	TXN1_P0	O	L2	Upstream port, SuperSpeed transmit minus lane 1
5	RXP1_P0	I	M1	Upstream port, SuperSpeed receive plus lane 1
6	RXN1_P0	I	M2	Upstream port, SuperSpeed receive minus lane 1
7	TXP2_P0	O	P3	Upstream port, SuperSpeed transmit plus lane 2
8	TXN2_P0	O	P2	Upstream port, SuperSpeed transmit minus lane 2
9	RXP2_P0	I	N2	Upstream port, SuperSpeed receive plus lane 2
10	RXN2_P0	I	N1	Upstream port, SuperSpeed receive minus lane 2
Downstream Port1 USB Signals				
11	DP_P1	I/O	B2	Downstream port1, USB 2.0 data plus
12	DM_P1	I/O	B1	Downstream port1, USB 2.0 data minus
13	TXP1_P1	O	C1	Downstream port1, SuperSpeed transmit plus lane 1
14	TXN1_P1	O	C2	Downstream port1, SuperSpeed transmit minus lane 1
15	RXP1_P1	I	D1	Downstream port1, SuperSpeed receive plus lane 1
16	RXN1_P1	I	D2	Downstream port1, SuperSpeed receive minus lane 1
17	TXP2_P1	O	F2	Downstream port1, SuperSpeed transmit plus lane 2
18	TXN2_P1	O	F1	Downstream port1, SuperSpeed transmit minus lane 2
19	RXP2_P1	I	E2	Downstream port1, SuperSpeed receive plus lane 2
20	RXN2_P1	I	E1	Downstream port1, SuperSpeed receive minus lane 2
Downstream Port2 USB Signals				
21	DP_P2	I/O	B14	Downstream port2, USB 2.0 data plus
22	DM_P2	I/O	B13	Downstream port2, USB 2.0 data minus
23	TXP1_P2	O	F14	Downstream port2, SuperSpeed transmit plus lane 1
24	TXN1_P2	O	F13	Downstream port2, SuperSpeed transmit minus lane 1
25	RXP1_P2	I	E14	Downstream port2, SuperSpeed receive plus lane 1
26	RXN1_P2	I	E13	Downstream port2, SuperSpeed receive minus lane 1
27	TXP2_P2	O	C13	Downstream port2, SuperSpeed transmit plus lane 2
28	TXN2_P2	O	C14	Downstream port2, SuperSpeed transmit minus lane 2
29	RXP2_P2	I	D13	Downstream port2, SuperSpeed receive plus lane 2
30	RXN2_P2	I	D14	Downstream port2, SuperSpeed receive minus lane 2
Downstream Port3 USB Signals				
31	DP_P3	I/O	K14	Downstream port3, USB 2.0 data plus
32	DM_P3	I/O	K13	Downstream port3, USB 2.0 data minus
33	TXP1_P3	O	P12	Downstream port3, SuperSpeed transmit plus lane 1

Pin Description *(continued)*

No.	Pin Name	Type	Pin Number	Description
34	TXN1_P3	O	P13	Downstream port3, SuperSpeed transmit minus lane 1
35	RXP1_P3	I	N13	Downstream port3, SuperSpeed receive plus lane 1
36	RXN1_P3	I	N14	Downstream port3, SuperSpeed receive minus lane 1
37	TXP2_P3	O	L13	Downstream port3, SuperSpeed transmit plus lane 2
38	TXN2_P3	O	L14	Downstream port3, SuperSpeed transmit minus lane 2
39	RXP2_P3	I	M13	Downstream port3, SuperSpeed receive plus lane 2
40	RXN2_P3	I	M14	Downstream port3, SuperSpeed receive minus lane 2
Downstream Port4 USB Signals				
41	DP_P4	I/O	J14	Downstream port4, USB 2.0 data plus
42	DM_P4	I/O	J13	Downstream port4, USB 2.0 data minus
43	TXP_P4	O	H14	Downstream port4, SuperSpeed transmit plus
44	TXN_P4	O	H13	Downstream port4, SuperSpeed transmit minus
45	RXP_P4	I	G14	Downstream port4, SuperSpeed receive plus
46	RXN_P4	I	G13	Downstream port4, SuperSpeed receive minus
Downstream Port5 USB Signals				
47	DP_P5	I/O	J1	Downstream port5, USB 2.0 data plus
48	DM_P5	I/O	J2	Downstream port5, USB 2.0 data minus
49	TXP_P5	O	G1	Downstream port5, SuperSpeed transmit plus
50	TXN_P5	O	G2	Downstream port5, SuperSpeed transmit minus
51	RXP_P5	I	H1	Downstream port5, SuperSpeed receive plus
52	RXN_P5	I	H2	Downstream port5, SuperSpeed receive minus
Downstream Port6 USB Signals				
53	DP_P6	I/O	A13	Downstream port6, USB 2.0 data plus
54	DM_P6	I/O	A12	Downstream port6, USB 2.0 data minus
Downstream Port7 USB Signals				
55	DP_P7	I/O	A3	Downstream port7, USB 2.0 data plus
56	DM_P7	I/O	A2	Downstream port7, USB 2.0 data minus
USB Port Control Signals				
57	OVCUR_P1	I	K6	Downstream port1, Active low Over current detect
58	OVCUR_P2	I	F10	Downstream port2, Active low Over current detect
59	OVCUR_P3	I	N12	Downstream port3, Active low Over current detect
60	OVCUR_P4	I	L7	Downstream port4, Active low Over current detect
61	OVCUR_P5	I	L5	Downstream port5, Active low Over current detect
62	OVCUR_P6	I	H10	Downstream port6, Active low Over current detect
63	OVCUR_P7	I	M11	Downstream port7, Active low Over current detect
64	PWREN_P1	O	J6	Downstream port1, Active low Power enable
65	PWREN_P2	O	E9	Downstream port2, Active low Power enable
66	PWREN_P3	O	N11	Downstream port3, Active low Power enable
67	PWREN_P4	O	N3	Downstream port4, Active low Power enable
68	PWREN_P5	O	L6	Downstream port5, Active low Power enable

Pin Description *(continued)*

No.	Pin Name	Type	Pin Number	Description
69	PWREN_P6	O	J10	Downstream port6, Active low Power enable
70	PWREN_P7	O	P11	Downstream port7, Active low Power enable
71	VBUS	I	M7	Upstream VBUS input
Upstream PD Control				
72	VBUS_MON_P0	A	D4	GPIO used as VBUS monitor for Upstream PD port
73	VBUS_P_CTRL_P0	I/O	E4	GPIO used for controlling provider power switch of Upstream PD port
74	VBUS_C_CTRL_P0	I/O	H4	GPIO used for controlling consumer power switch of Upstream PD port
75	VBUS_DISCHARGE_P0	I/O	E6	GPIO for controlling VBUS discharge switch of Upstream PD port
Downstream PD Control				
76	VBUS_MON_P1	A	B5	GPIO used as VBUS monitor for Downstream PD port
77	VBUS_P_CTRL_P1	I/O	D6	GPIO used for controlling provider power switch of Downstream PD port
78	VBUS_C_CTRL_P1	I/O	C5	GPIO used for controlling consumer power switch of Downstream PD port
79	VBUS_DISCHARGE_P1	I/O	A4	GPIO for controlling VBUS discharge switch of Downstream PD port
Type-C PD Control Signals				
80	CC1_P0	A	D3	Upstream port connect detect/Configuration Channel 1
81	CC1_P1	A	D8	Downstream port1 connect detect/Configuration Channel 1
82	CC1_P2	A	K9	Downstream port2 connect detect/Configuration Channel 1
83	CC1_P3	A	L8	Downstream port3 connect detect/Configuration Channel 1
84	CC2_P0	A	B3	Upstream port connect detect/Configuration Channel 2
85	CC2_P1	A	C7	Downstream port1 connect detect/Configuration Channel 2
86	CC2_P2	A	K10	Downstream port2 connect detect/Configuration Channel 2
87	CC2_P3	A	L9	Downstream port3 connect detect/Configuration Channel 2
88	OCP_DET_P0	I	G5	Over current detection input for upstream Type-C port
89	OCP_DET_P1	I	C6	Over current detection input for downstream Type-C port 1
90	VSEL_GPIO1	I/O	D5	GPIO for selecting VBUS voltage level of PD ports; When used for I2C interface, this pin must be used as I2C_MASTER_SDA.
91	VSEL_GPIO2	I/O	F5	GPIO for selecting VBUS voltage level of PD ports; When used for I2C interface, this pin must be used as I2C_MASTER_SCL.
92	VSEL_GPIO3	I/O	B7	GPIO
93	VSEL_GPIO4	I/O	B8	GPIO

Pin Description *(continued)*

No.	Pin Name	Type	Pin Number	Description
SPI, I2C, and GPIOs				
94	SPI_CLK_HUB	O	K7	SPI clock. Connect to SPI EEPROM
95	SPI_SS_HUB	O	M6	SPI select. Connect to SPI EEPROM
96	SPI_MISO_HUB	I	J5	SPI data in. Connect to SPI EEPROM
97	SPI_MOSI_HUB	O	H5	SPI data out. Connect to SPI EEPROM
98	SPI_MISO_DMC	I/O	A10	SPI data in. This SPI interface from DMC block
99	SPI_SS_DMC	I/O	B10	SPI slave select. This SPI interface from DMC block
100	SPI_MOSI_DMC	I/O	F12	SPI data out. This SPI interface from DMC block
101	SPI_CLK_DMC	I/O	D12	SPI clock. This SPI interface from DMC block
102	I2C_SCL1	I/O	E11	I2C clock - 1; Connected to DMC (I2C master)
103	I2C_SDA1	I/O	D11	I2C data - 1; Connected to DMC (I2C master)
104	I2C_SCL2	I/O	A9	I2C clock - 2; Connected to DMC (I2C slave)
105	I2C_SDA2	I/O	B9	I2C data - 2; Connected to DMC (I2C slave)
106	I2C_SCL_HUB	I/O	M5	I2C clock, Connected to Hub controller (I2C slave) block
107	I2C_SDA_HUB	I/O	G10	I2C data, Connected to Hub controller (I2C slave) block
108	GPIO3_HUB	I/O	P7	GPIO from Hub
109	GPIO4_HUB	I/O	N7	GPIO from Hub
110	DMC_P24	I/O	A11	GPIO
111	DMC_P25	I/O	B11	GPIO
112	DMC_P26	I/O	B12	GPIO
113	DMC_P32	I/O	E12	GPIO
114	HPD_P0	I/O	E5	GPIO used as Hot plug detect input from DisplayPort (DP) of Upstream PD port
115	HPD_P1	I/O	A8	GPIO used as Hot plug detect output to DP of Downstream PD port
116	PD_P15	I/O	E3	GPIO
117	VCONN_MON_P0/PD_P24	I/O	K5	GPIO
118	VCONN_MON_P1/PD_P27	I/O	C8	GPIO
Clock, Reset, Debug, and Mode Select				
119	XIN	A	A6	Crystal In
120	XOUT	A	A7	Crystal Out
121	CHIPEN	I	M9	Chip enable, Recommend to connect it HIGH. Chip has a weak internal pull-up.
122	RESET_HUB	I	M8	Active Low reset input of hub controller
123	XRES_DMC	I	C11	Active Low reset input of DMC
124	XRES_PD	I	K4	Active Low reset input of PD controller
125	SWDCLK_DMC	I/O	D10	SWD clock input for DMC
126	SWDIO_DMC	I/O	C10	SWD data I/O for DMC
127	SWDCLK_PD	I/O	B4	SWD clock input for PD controller

Pin Description *(continued)*

No.	Pin Name	Type	Pin Number	Description
128	SWDIO_PD	I/O	F3	SWD data I/O for PD controller
129	PSELF	I	K11	Self/Bus power mode: This pin must be pulled HIGH for SELF power mode and pulled LOW for BUS power mode.
130	PGANG	I	E10	Gang/Individual mode: This pin must be pulled HIGH for GANG mode and pulled LOW for INDIVIDUAL mode.
131	RTERM	A	M10	Connect this pin to a precision resistor (20 kΩ ±1%)
Ground, Power, and NC				
132	AVDD10	PWR	K8	1.0-V Input (1.0-V power for Analog)
133	AVDD33	PWR	E8	3.3-V Input (3.3-V power for Analog)
134–137	DVDD10	PWR	F4, F11, J4, J11	1.0-V Input (1.0-V power for Digital)
138	FB	PWR	N10	Reserved. Connect this pin to Ground.
139	VCCD_DMC	PWR	D9	Regulator output of DMC
140	VCCD_PD	PWR	B6	Regulator output of PD controller
141–144	VDDIO	PWR	C3, C12, L10, J12	3.3-V I/O supply
145	VDDD_DMC	PWR	C9	3.3-V supply for DMC
146	VDDD_PD	PWR	A5	3.3-V supply for PD controller
147	V1P0_MEM_A	PWR	N5	1.0-V supply for internal memory
148	V1P0_MEM_B	PWR	N4	1.0-V supply for internal memory
149–150	V1P0_P0	PWR	L4, M4	1.0-V supply for US port
151–152	V1P0_P1	PWR	J3, H3	1.0-V supply for port 1
153–154	V1P0_P2	PWR	H12, H11	1.0-V supply for port 2
155–156	V1P0_P3	PWR	M12, L11	1.0-V supply for port 3
157	V1P0_P4	PWR	K12	1.0-V supply for port 4
158	V1P0_P5	PWR	K3	1.0-V supply for port 5
159	V1P0_P6	PWR	G11	1.0-V supply for port 6
160	V1P0_P7	PWR	G4	1.0-V supply for port 7
161–164	V1P0_PHY	PWR	P8, N8, P9, N9	1.0-V supply for PHY
165–168	V1P2	PWR	P4, P5, P6, N6	1.2-V input for internal LDO
169	V3P3_REG	PWR	P10	3.3-V input for internal LDO. Connect to VDDIO
170–174	V3P3	PWR	L3, G3, G12, L12, M3	3.3-V supply for USB 2.0
175	V5P0_P0	PWR	C4	5-V VCONN input to Upstream PD port
176	V5P0_P1	PWR	D7	5-V VCONN input to Downstream PD port
177	V5P0	PWR	E7	5-V input supply to hub controller
178–192	GND	GND	F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J7, J8, J9	Ground

System Interfaces

Upstream Port (US)

The HX3PD USB port can function in Type-C or Legacy Type-B modes; it operates in the USB 3.1 Gen 2 (10 Gbps) specification. This port includes an integrated 1.5-kΩ pull-up resistor and termination resistors. The HX3PD US port has an integrated PD controller, which supports the PD 3.0 specification and can charge up to 5A at 20 V.

Downstream Ports (DS1, 2, 3, 4, 5, 6, 7)

The following table summarizes the operations of HX3PD DS ports.

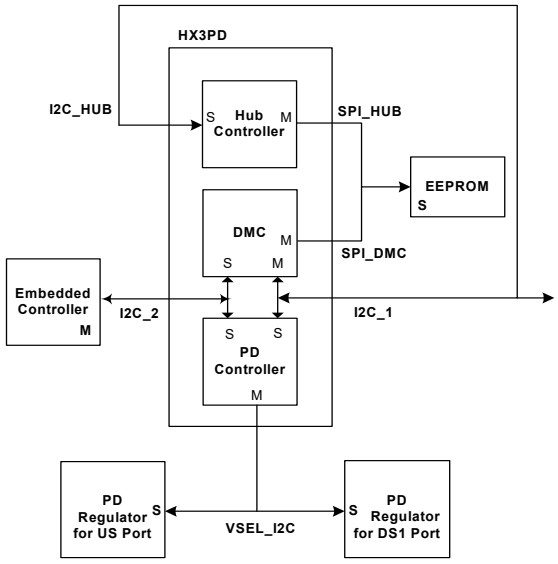
Table 2. Operations of HX3PD DS Ports

DS Port	Connector	USB Speed	Charging Mode	Max Charging Current
DS1	Type-C	USB 3.1 Gen 2	PD 3.0	5A at 20 V
DS2	Type-C	USB 3.1 Gen 2	BC 1.2, Apple	3A at 5 V
DS3	Type-C	USB 3.1 Gen 2	BC 1.2, Apple	3A at 5 V
DS4	Type-A	USB 3.1 Gen 2	BC 1.2, Apple	2.4A at 5 V
DS5	Type-A	USB 3.1 Gen 2	BC 1.2, Apple	2.4A at 5 V
DS6	Type-A	USB 2.0	BC 1.2, Apple	2.4A at 5 V
DS7	Type-A	USB 2.0	BC 1.2, Apple	2.4A at 5 V

Three HX3PD DS ports (DS1, DS2, and DS3) work in the Type-C mode. The other ports work in the Type-A mode. USB 3.1 Gen 2 (10 Gbps) is supported in ports DS1 to DS5 and USB 2.0 (480 Mbps) is supported in ports DS6 and DS7. All DS ports support, by default, the Battery Charging Specification 1.2. DS1 has an integrated PD controller which supports the PD 3.0 specification. Port enable/disable and charging modes shall be configured using configuration options.

Communication Interfaces

Figure 4. Communication Interfaces



Note
M = Master; S = Slave

HX3PD supports SPI and I²C interfaces for communications between individual blocks and with the Embedded Controller (EC).

HX3PD has two SPI and four I²C interfaces.

SPI_HUB

This interface is connected to an SPI EEPROM. Hub controller uses this interface to read firmware and configurations from EEPROM.

SPI_DMC

DMC also shall access SPI EEPROM using the SPI_DMC interface.

I2C_1

The I²C interface I2C-1 is connected to the DMC and PD controllers. DMC acts as an I²C master and PD controller acts as the I²C slave for this interface.

I2C_2

The I²C interface I2C-2 is connected to the DMC and PD controllers – DMC I²C is a slave; and PD I²C is unused with default firmware. An external I²C master, such as Embedded Controller (EC), shall use this interface to communicate to the DMC and PD controllers.

I2C_HUB

The I²C interface I2C_HUB is connected to the Hub controller – Hub controller acting as I²C slave. DMC shall access I2C_HUB by connecting externally using I2C_1 to read hub status and write hub configurations.

VSEL_I2C

VSEL_GPIO1 and VSEL_GPIO2 shall be used for selecting the VBUS voltage level of PD ports. VSEL_GPIO1 acts as I2C_MASTER_SDA and VSEL_GPIO2 acts as I2C_MASTER_SCL. These pins must be connected to the external Power Regulator's I^2C interface to configure voltage levels for PD ports.

Reset

There are three reset pins for the HX3PD device. These pins control reset operations for the Hub controller (RESET_HUB), reset to DMC (XRES_DMC), and reset to PD controller (XRES_PD). Additionally, the HX3PD reset shall be controlled by DMC using a Software reset mechanism during configuration and initialization.

Clock

HX3PD requires an external crystal connected to XIN/XOUT with 25 MHz (±150 ppm), parallel resonant, fundamental mode, and be capable of low drive level (<200 µW) with a peak-to-peak jitter less than 50 ps.

Configuration Options

EZ-USB HX3PD Configuration Utility can be used to update firmware and configurations of Hub controller, PD controller, and DMC. Firmware and configuration image for the hub controller is stored in an external SPI EEPROM. PD controller and DMC images will be stored in device flash.

Following configuration options are available in EZ-USB HX3PD Configuration tool.

Table 3. EZ-USB HX3PD Configuration Options

No	Settings	Description
Hub Controller Configurations		
1	VID	Custom Vendor ID
2	USB 2.0 PID	Custom Product ID for USB 2.0 Hub
3	USB 3.1 PID	Custom Product ID for USB 3.1 Hub
4	Power good time	Time for Power-On sequence start in a port to Power is good to that port
5	PolyFuse	Set the hub for polyfuse mode operation. Power good time is set to '0' for polyfused mode
6	String descriptor: Vendor	String descriptor for Vendor name
7	String descriptor: USB 2.0 Product	String descriptor for USB 2.0 Hub Product Name
8	String descriptor: USB 3.1 Product	String descriptor for USB 3.1 Hub Product Name
9	Serial	Product Serial Number
10	Number of USB 2.0 ports	Number of active USB 2.0 ports
11	Number of USB 3.1 ports	Number of active USB 3.1 ports. **Note** "Number of USB 3.1 ports" should be equal or lower than "Number of USB 2.0 ports".
12	Charging port	Enable or disable of BC 1.2 or Apple charging for DS ports
13	Compound hub	Removable or non-removable settings for DS ports. **Note** DMC port is always set as "Non-removable".
14	DFP fast charging	Enable or disable of CDP, Pure DCP, and Auto DCP modes in downstream ports. **Note** Pure DCP used for compliance tests. Auto DCP allows fast charging for Apple 2.1A/2.4A supported device or Samsung Galaxy devices.
15	USB type-C current	Maximum Type-C current for DS2 and DS3, 1.5A or 3.0 A
16	High active power switch	Enable Active-High power switch
PD Controller Configurations		
1	VID	PD controller Vendor ID
2	PID	PD controller Product ID
3	PD version	PD version supported by device. PD controller support PD 2.0 and PD 3.0 versions supported.
4	Port power role	Selection of Sink, Source, or Dual Role modes
5	Rp supported	Rp values supported by the PD ports. Both PD ports support Default, 1.5A and 3A current levels

Table 3. EZ-USB HX3PD Configuration Options *(continued)*

No	Settings	Description
Hub Controller Configurations		
6	Power data objects (PDOs)	Power source and sink capabilities of the PD ports. Default PD firmware support 5V, 9V, 15V and 20V PDOs.
7	Overvoltage protection	Enable, threshold, and debounce of Over voltage protection
8	Overcurrent protection	Enable, threshold, and debounce of Over current protection
9	VCONN OCP	Enable, threshold, and debounce of VCONN over current protection
DMC Configurations		
1	VID	DMC Vendor ID
2	PID	DMC Product ID
3	Billboard enable	Billboard enable selection

You can download the EZ-USB HX3PD Configuration tool and its associated documentation at the following link:
www.cypress.com/products/ez-usb-hx3pd-usb-31-gen-2-hub-power-delivery

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Operating temperature ..... 0 °C to +70 °C

Electrostatic discharge voltage ..... 2200 V

Oscillator or crystal frequency ..... 25 MHz ±150 ppm

I/O voltage supply (3.3 V) ..... 3 V to 3.6 V

I/O voltage supply (1.2 V) .....1.14 V to 1.26 V

Maximum input sink current per I/O ..... 4 mA

Electrical Specifications

HX3PD meets all USB-IF Electrical Compliance specifications.

DC Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
V1P2	1.2-V voltage supply	1.14	1.2	1.26	V
V_{DDIO}	3.3-V I/O voltage supply	3.0	3.3	3.6	V
V3P3	3.3-V voltage supply	3	3.3	3.6	V
V_{DD10}	1.0-V core supply voltage	0.95	1.0	1.05	V
V3P3_U2	3.3-V supply for the USB 2.0 PHY	3	3.3	3.6	V
$V_{DDD\ (PD)}$	3.3-V supply input to PD controller	3	3.3	5.5	V
V_{CCD_PD}	Regulator output for PD controller	–	1.8	–	V
$V_{DDD\ (DMC)}$	3.3-V supply input to DMC	2.7	3.3	5.5	V
V_{CCD_DMC}	Regulator output for DMC	–	1.8	–	V
V_{BUS}	VBUS for upstream port	0	5	5.25	V
V5P0_P0	VCONN input to Upstream PD port	2.7	–	5.5	V
V5P0_P1	VCONN input to Downstream PD port	2.7	–	5.5	V
VRAMP	Voltage ramp rate on core and I/O supplies	0.05	–	5	V/s
ESD_HBM	Electrostatic discharge human body model	–	–	2200	V
ESD_CDM	Electrostatic discharge charged device model	–	–	500	V
LU	Pin current for latch-up	–100	–	100	mA
Power Supply Specifications					
I_{CC12}	1.2 V supplies operating current	–	–	750	mA
I_{CC33}	3.3 V supplies operating current	–	–	70	mA
I_{SB12}	1.2 V supplies combined suspend current	–	23	–	mA
I_{SB33}	3.3 V supplies combined suspend current	–	3	–	mA
I/O Specifications - Except USB Signals					
V_{IH}	Input voltage HIGH threshold	2	–	5.5	V
V_{IL}	Input voltage LOW threshold	–	–	0.8	V
V_{OH}	Output voltage HIGH level (when I_{OH} = 4 mA)	2.4	–	–	V
V_{OL}	Output voltage LOW level (when I_{OL} = 8 mA)	–	–	0.4	V
I_{IL}	Input leakage current	–1	–	1	µA

Power Consumption

Table 4 provides the power consumption estimates for HX3PD under different conditions.

Table 4. Power Consumption

Hub Operating Condition		Measured Current (mA)	
		VP12	VP33
Upstream Not Connected to Host		52.0	36.0
Hub in Suspend Mode		25.0	12.8
Connected to Host and Hub in Idle Mode		63.0	48.5
Hub in Reset Mode		14.5	2.5
Write	1 USB 3.1 device connected	298.0	50.0
	2 USB 3.1 devices connected	376.0	49.3
	3 USB 3.1 devices connected	442.0	49.3
	4 USB 3.1 devices connected	485.0	49.3
	5 USB 3.1 devices connected	520.0	49.3
	5 USB 3.1 and 1 USB 2.0 devices connected	535.0	49.3
	5 USB 3.1 and 2 USB 2.0 devices connected	548.0	49.3
Read	1 USB 3.1 device connected	295.0	49.3
	2 USB 3.1 devices connected	375.0	49.3
	3 USB 3.1 devices connected	442.0	49.3
	4 USB 3.1 devices connected	482.0	49.3
	5 USB 3.1 devices connected	519.0	49.3
	5 USB 3.1 and 1 USB 2.0 devices connected	535.0	49.3
	5 USB 3.1 and 2 USB 2.0 devices connected	548.0	49.3

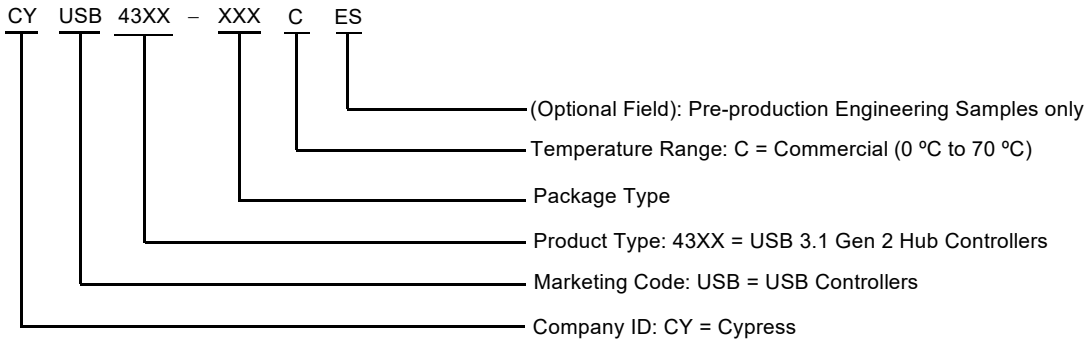
Ordering Information

The following table lists HX3PD's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers with customized configurations can be made available on request. For more information, visit the Cypress website or contact the local sales representative.

Table 5. Ordering Information

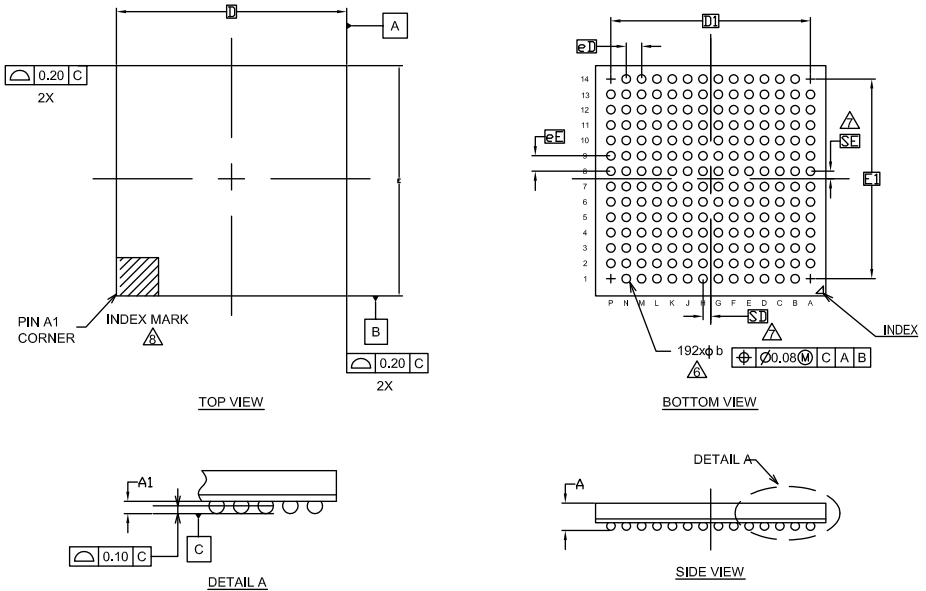
Ordering Part Number	No of Ports	US PD Port	DS PD Port	Signed FW Download
CYUSB4347-BZXC	7	DRP	DFP	No
CYUSB4357-BZXC	7	DRP	DFP	Yes

Ordering Code Definitions



Package Diagram

Figure 5. 192-Ball FBGA Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.45
A1	0.25	0.35	0.45
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E1	10.40 BSC		
MD	14		
ME	14		
n	192		
Φb	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD / SE	0.40 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-13493 *A

Silicon Revision History

This datasheet is applicable for USB-IF certified (TID# 5030000008) HX3PD Rev B and Rev A silicon.

Rev B: This silicon improves the yield of HX3PD, and fixed the Errata #2 ("Hub LVS Test "TD 10.102" Failure in DS1 to DS5 ports [1]") applicable to the Rev A silicon. There is no need to change the board design or layout to use the HX3PD Rev B Silicon. Products are completely compatible with the HX3 Rev A Silicon.

However Rev B silicon requires a different firmware compared to Rev A silicon. Refer to EZ-USB HX3PD Firmware webpage for more details

Method of Identification

Markings on row 3 of the HX3PD package differentiate Rev. B Silicon from Rev. A Silicon as indicated in the example below. Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Figure 6. HX3PD REV A Silicon

Figure 7. HX3PD REV B Silicon

Acronyms

Table 6. Acronyms Used in this Document

Acronym	Description
AES	Advanced Encryption Standard
BC	Battery Charging
CC	Configuration Channel
CDP	Charging Downstream Port
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check, an Error-Checking Protocol
DS	DownStream
DCP	Dedicated Charging Port
DFP	Downstream Facing Port
DMC	Dock Management Controller
DNU	Do Not Use
DP	DisplayPort
DRP	Dual-Role Power Port
DWG	Device Working Group
EC	Embedded Controller
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	Full-Speed
FW	FirmWare
GND	GrouND
GPIO	General-Purpose Input/Output
HS	Hi-Speed
I2C	Inter Integrated Circuit, a communications protocol
ISP	In-System Programming
I/O	Input/Output
LS	Low-Speed
MCU	Microcontroller Unit
NC	No Connect
OTG	On-The-Go
PD	Power Delivery
PID	Product ID
POR	Power-On Reset
ROM	Read-Only Memory
SCL	Serial CLock
SDA	Serial DAta
SHA	Secure Hash Algorithm
SPI	Serial Peripheral Interface, a communications protocol

Table 6. Acronyms Used in this Document

Acronym	Description
SS	SuperSpeed
TT	Transaction Translator
UFP	Upstream Facing Port
US	UpStream
USB	Universal Serial Bus
VID	Vendor ID

Reference Documents

USB 2.0 Specification
USB 3.1 Specification
Battery Charging Specifications
USB Type-C Specification
USB Power Delivery Specification

Document Conventions

Units of Measure

Table 7. Units of Measure

Symbol	Unit of Measure
°C	degree celsius
Ω	ohm
Gbps	gigabit per second
KB	kilobyte
kHz	kilohertz
kΩ	kilo-ohm
Mbps	megabit per second
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
ppm	parts per million
V	volt

Errata

No.	Errata	Applicability
1	Type-C Compliance Test “TD 4.1.2” Failure in DS2 and DS3 ports	HX3PD Rev A and Rev B silicon
2	Hub LVS Test “TD 10.102” Failure in DS1 to DS5 ports	HX3PD Rev A silicon only

1. Type-C Compliance Test “TD 4.1.2” Failure in DS2 and DS3 ports

- **Problem Definition:** DS2 and DS3 ports present Rd when HX3PD is in Power-off state that leads to this compliance failure.
- **Parameters Affected:** N/A
- **Trigger Condition(s):** Type-C compliance test “TD 4.1.2 Unpowered CC Voltage Test” shows this failure condition. This is because test expects no power to be present when HX3PD is in Power-off state.
- **Scope of Impact:** There is no functional impact to the end user. This Errata is applicable only when DS2 and DS3 ports are used as Type-C ports and there will be no impact when DS2 and DS3 are used as Legacy Type-A ports. Also, Type-C compliance test “TD 4.1.2 Unpowered CC Voltage Test” failure is applicable only when DS2 and DS3 ports are expected to connect to a VBUS Source (such as power adapter) which is not a real use case.
- **Workaround:** No workaround available. This issue will not cause any functional issues or damage to silicon. Need waiver for compliance tests.
- **Fix Status:** No fix planned.

2. Hub LVS Test “TD 10.102” Failure in DS1 to DS5 ports [1]

- **Problem Definition:** HX3PD’s Hub port shows wrong value for PORT_LINK_STATE parameter during link loopback mode.
- **Parameters Affected:** N/A
- **Trigger Condition(s):** Hub LVS test “TD 10.102” shows this failure condition. This failure will never happen in functional modes.
- **Scope of Impact:** Hub LVS test “TD 10.102 Power Off Upstream Port Test” failure is applicable only in test mode; in a normal functional mode, HX3PD will never be in test mode and hence no impact.
- **Workaround:** No workaround available for Rev A silicon. Issue fixed in Rev B silicon.
- **Fix Status:** Errata seen only in Rev A silicon. It is fixed in Rev B silicon.

Note
1. Applicable only for Rev A silicon.

Document History Page

Document Title: CYUSB4347/CYUSB4357, HX3PD USB 3.1 Gen 2 Type-C Hub with PD Document Number: 002-16615			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	5894940	10/03/2017	New data sheet.
*A	6000726	12/21/2017	Updated Document Title to read as “CYUSB4347/CYUSB4357, HX3PD USB 3.1 Gen 2 Type-C Hub with PD”. Updated Features: Updated description. Updated Block Diagram. Updated Architecture Overview: Updated USB-PD Controller: Updated description. Removed “SPI Interfaces”. Removed “Serial Communication/GPIO Block”. Removed “Dock Management Controller”. Added SPI, I2C, and GPIO Interfaces. Added Dock Management Controller. Updated HX3PD Product Options: Updated Table 1: Updated entire table. Updated Pinouts: Updated Figure 5. Updated Pin Description: Updated entire table. Added System Interfaces. Added Absolute Maximum Ratings. Added Electrical Specifications. Added Ordering Information. Added Errata. Updated to new template.
*B	6111605	03/27/2018	Updated Pinouts: Updated Figure 5 (Updated details in C4 and D7). Updated Pin Description: Updated details in all columns corresponding to pin numbers C4, D7, E7. Updated Electrical Specifications: Updated Power Consumption: Updated Table 4 (Updated entire table). Removed Errata.
*C	6288356	09/27/2018	Updated Features: Updated description. Updated Block Diagram. Updated Architecture Overview: Added Crypto Block. Updated HX3PD Product Options: Updated Table 1. Updated System Interfaces: Updated Downstream Ports (DS1, 2, 3, 4, 5, 6, 7): Updated Table 2. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated details in “Min” and “Max” columns corresponding to ESD_HBM parameter. Updated Power Consumption: Updated Table 4.

Document History Page *(continued)*

Document Title: CYUSB4347/CYUSB4357, HX3PD USB 3.1 Gen 2 Type-C Hub with PD Document Number: 002-16615			
Revision	**ECN**	**Submission Date**	**Description of Change**
*C (cont.)	6288356	09/27/2018	Updated Reference Documents: Updated links. Added “Silicon Revision History”. Completing Sunset Review.
*D	6352040	10/31/2018	Updated Architecture Overview: Updated USB-PD Controller: Updated description. Updated Pinouts: Updated Figure 5 (Updated details in A5 and C9). Updated Pin Description: Updated details in “Description” column corresponding to pin numbers B11 and B12. Updated details in “Pin Name” and “Description” columns corresponding to pin numbers C9 and A5. Updated System Interfaces: Updated Communication Interfaces: Updated I2C_2: Updated description. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated details in “Min” and “Max” columns corresponding to ESD_CDM parameter. Added LU parameter and its corresponding details. Updated Power Consumption: Updated Table 4.
*E	6439058	04/24/2019	Updated Functional Description: Updated description. Updated Features: Updated description. Updated Block Diagram. Updated Architecture Overview: Updated description. Updated Dock Management Controller: Added Firmware Update Support. Added Application Diagrams. Updated Pinouts: Updated Figure 3. Updated Pin Description: Updated almost entire table. Updated System Interfaces: Updated Downstream Ports (DS1, 2, 3, 4, 5, 6, 7): Updated Table 2. Updated Communication Interfaces: Updated Figure 4. Updated SPI_HUB: Updated description. Updated I2C_1: Updated description. Updated I2C_2: Updated description. Updated I2C_HUB: Updated description. Added Configuration Options.

Document History Page *(continued)*

Document Title: CYUSB4347/CYUSB4357, HX3PD USB 3.1 Gen 2 Type-C Hub with PD Document Number: 002-16615			
Revision	**ECN**	**Submission Date**	**Description of Change**
*E (cont.)	6439058	04/24/2019	Updated Electrical Specifications: Updated DC Electrical Characteristics: Added V5P0_P0, V5P0_P1, VRAMP parameters and their corresponding details. Added Power Supply Specifications, I/O Specifications - Except USB Signals sub sections and added corresponding details. Updated Power Consumption: Updated Table 4. Updated to new template.
*F	6534152	06/14/2019	Updated Ordering Information: Updated part numbers. Removed “Silicon Revision History”.
*G	6904997	06/25/2020	Changed status from Preliminary to Final. Updated Block Diagram. Updated Architecture Overview: Updated Dock Management Controller: Updated Firmware Update Support: Updated description. Updated Signed Firmware Update: Added hyperlinks in required places. Updated Application Diagrams: Updated Docking Stations: Updated description. Updated Pinouts: Updated Figure 3. Updated Pin Description: Updated details in all columns corresponding to pin numbers K5 and C8. Updated details in “Pin Name” column corresponding to pin numbers C9 and A5. Updated System Interfaces: Updated Communication Interfaces: Updated Figure 4. Updated VSEL_I2C: Updated description. Updated Configuration Options: Updated description. Updated Table 3 (Updated details in Description column corresponding to “USB type-C current” setting, replaced “DMC Controller Configurations” with “DMC Configurations”). Updated Electrical Specifications: Updated Power Consumption: Updated Table 4 (Updated entire table). Added Errata. Updated to new template.
*H	6993324	10/13/2020	Updated part numbers in Ordering Information.
*I	7105316	03/19/2021	Added Silicon Revision History section. Updated “Hub LVS Test” section in Errata and added a note “Applicable only for Rev A silicon”. Updated Power Consumption and Ordering Code Definitions.

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