

Power-Voltage Monitoring IC with Watchdog Timer Datasheet

Description

The MB3793 is an integrated circuit to monitor power voltage; it incorporates a watchdog timer. A reset signal is output when the power is cut or falls abruptly. When the power recovers normally after resetting, a power-on reset signal is output to microprocessor units (MPUs). An internal watchdog timer with two inputs for system operation diagnosis can provide a fail-safe function for various application systems.

| Model No. | Marking Code | Detection Voltage |
|-----------|--------------|-------------------|
| MB3793-45 | 3793-7 | 4.5 V |

Features

- Precise detection of power voltage fall: ±2.5%
- · Detection voltage with hysteresis
- Low power dispersion: I_{CC} = 31 μ A (reference)
- · Internal dual-input watchdog timer
- · Watchdog timer halt function (by inhibition pin)
- · Independently-set watchdog and reset times

Application

· Arcade Amusement etc.



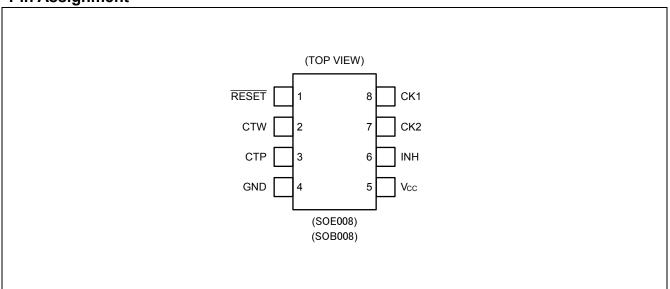
Contents

| De | escription | . 1 |
|----|---|-----|
| Fe | eatures | . 1 |
| Αŗ | oplication | . 1 |
| 1. | Pin Assignment | . 3 |
| 2. | Pin Description | . 3 |
| 3. | Block Diagram | . 4 |
| 4. | Block Functions | . 5 |
| 5. | Absolute Maximum Ratings | . 6 |
| 6. | Recommended Operating Conditions | . 6 |
| 7. | Electrical Characteristics | . 7 |
| | 7.1 DC Characteristics | |
| | 7.2 AC Characteristics | |
| 8. | Timing Diagram | . 8 |
| | 8.1 Basic Operation (Positive Clock Pulse) | |
| | 8.2 Basic Operation (Negative Clock Pulse) | |
| | 8.3 Single-Clock Input Monitoring (Positive Clock | |
| | Pulse) | 10 |
| | 8.4 Inhibition Operation (Positive Clock Pulse) | 11 |

| | 8.5 Clock Pulse Input Supplementation (Positive | |
|------|---|----|
| | Clock Pulse) | 12 |
| 9. (| Operation Sequence | 13 |
| 10. | Typical Characteristics | 15 |
| 11. | Application Example | 18 |
| | 11.1 Supply Voltage Monitor and Watchdog Timer | |
| | 11.2 Supply Voltage Monitor and Watchdog Timer | |
| | Stop | 19 |
| | 11.3 Setting of Compulsory Reset | 19 |
| 12. | Usage Precaution | 20 |
| 13. | Ordering Information | 20 |
| 14. | RoHS Compliance Information | 20 |
| 15. | Package Dimensions | 21 |
| 16. | Major Changes | 23 |
| | es, Solutions, and Legal Information | |
| | | |



1. Pin Assignment

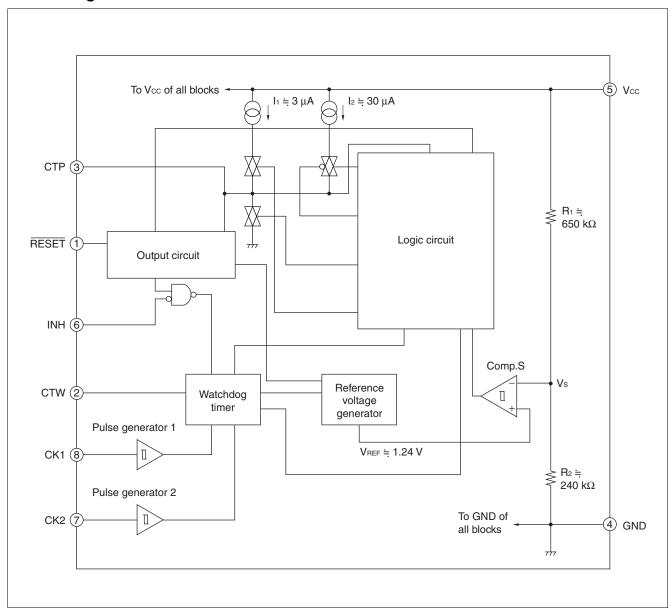


2. Pin Description

| Pin No. | Symbol | Description |
|---------|--------|----------------------------------|
| 1 | RESET | Outputs reset |
| 2 | CTW | Sets monitoring time |
| 3 | СТР | Sets power-on reset hold time |
| 4 | GND | Ground |
| 5 | Vcc | Power supply |
| 6 | INH | Inhibits watchdog timer function |
| 7 | CK2 | Inputs clock 2 |
| 8 | CK1 | Inputs clock 1 |



3. Block Diagram





4. Block Functions

1. Comp. S

Comp. S is a comparator with hysteresis to compare the reference voltage with a voltage (Vs) that is the result of dividing the power voltage (Vcc) by resistors R_1 and R_2 . When Vs falls below 1.24 V, a reset signal is output. This function enables the MB3793 to detect an abnormality within 1 μ s when the power is cut or falls abruptly.

2. Output Circuit

The output circuit has a comparator to control the reset signal (RESET) output. When the voltage at the CTP pin for setting the power-on reset hold time exceeds the threshold voltage, resetting is canceled.

Since the reset (RESET) output buffer has the CMOS organization, no pull-up resistor is needed.

3. Pulse Generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 input clock pins changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

4. Watchdog Timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock pins to monitor a single clock pulse.

5. Inhibition Pin

The inhibition (INH) pin forces the watchdog timer on/off. When this pin is High level, the watchdog timer is stopped.

6. Logic Circuit

Logic circuit controls charging and discharging of the power-on reset hold time setting capacity (C_{TP}) on a signal of Comp.S and Watchdog timer.



5. Absolute Maximum Ratings

| Parameter | | Symbol Conditions | | Ratir | Unit | |
|-----------------------|-----------|------------------------------------|-------------------------|------------|--------------------------------|-------|
| Farameter | Farameter | | Symbol Conditions — | | Max | Oiiit |
| Power supply voltage* | | V _{CC} | _ | -0.3 | +7 | V |
| Input voltage* | CK1 | V _{CK1} | _ | -0.3 | V _{CC} + 0.3 (≤+7) | V |
| | CK2 | V _{CK2} | _ | | (≤+/) | |
| | INH | I _{INH} | _ | | | |
| Reset output voltage* | RESET | V _{OL} V _{OH} | _ | -0.3 | V _{CC} + 0.3 (≤+7) | V |
| Reset output current | | I _{OL} I _{OH} | _ | -10 | +10 | mA |
| Power dissipation | • | P_{D} | Ta ≤ +85 ⁰ C | _ | 200 | mW |
| Storage temperature | | Tstg | _ | -55 | +125 | 0C |

^{*:} The voltage is based on the ground voltage (0 V).

WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

6. Recommended Operating Conditions

| Parameter | Symbol | Symbol Conditions | | Unit | | |
|--|-----------------|-------------------|------------|------|-----|------|
| Farameter | Syllibol | | Min | Тур | Max | Onit |
| Power supply voltage | V _{CC} | _ | 1.2 | 5.0 | 6.0 | V |
| Reset (RESET) output current | I _{OL} | _ | 0 | _ | +5 | mA |
| | I _{OH} | _ | - 5 | _ | 0 | |
| Power-on reset hold time setting capacity | C _{TP} | _ | 0.001 | 0.1 | 10 | μF |
| Watchdog-timer monitoring time setting capacity* | C _{TW} | _ | 0.001 | 0.01 | 1 | μF |
| Operating ambient temperature | Та | _ | -40 | +25 | +85 | 0C |

^{*:} The watchdog timer monitor time range depends on the rating of the setting capacitor.

WARNING:

Document Number: 002-08552 Rev. *C Page 6 of 24

^{1.} The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

^{2.} Any use of semiconductor devices will be under their recommended operating condition.

^{3.} Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

^{4.}No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.



7. Electrical Characteristics

7.1 DC Characteristics

 $(V_{CC} = +5 \text{ V}, \text{Ta} = +25^{\circ}\text{C})$

| _ , | | | | | Value | | |
|---|--------|------------------------|--|-------|-------|-----------------|------|
| Parameter | Symbol | Conditions | | Min | Тур | Max | Unit |
| Power current | ICC1 | After exit from | m reset | _ | 31 | 45 | μΑ |
| Detection voltage | VsL | Vcc falling Ta = +25°C | | 4.40 | 4.50 | 4.60 | V |
| | | | Ta = $-40 \text{ to } +85^{\circ}\text{C}$ | 4.35* | 4.50 | 4.65* | |
| | VsH | Vcc rising | Ta = +25°C | 4.50 | 4.60 | 4.70 | V |
| | | | Ta = $-40 \text{ to } +85^{\circ}\text{C}$ | 4.45* | 4.60 | 4.75* | |
| Detection voltage hysteresis difference | Vshys | Vsh - Vsl | Vsh - VsL | | 100 | 150 | mV |
| CK input threshold voltage | VCIH | _ | | 1.4* | 1.9 | 2.5 | V |
| | VCIL | _ | | 0.8 | 1.3 | 1.8* | V |
| CK input hysteresis | Vchys | _ | | 0.4* | 0.6 | 0.8* | V |
| INH input voltage | VIIH | | _ | 3.5 | _ | V _{CC} | V |
| | VIIL | _ | | 0 | _ | 0.8 | V |
| Input current | Іін | Vck = Vcc | | _ | 0 | 1.0 | μΑ |
| (CK1,CK2,INH) | lıL | Vck = 0 V | VCK = 0 V | | 0 | _ | μΑ |
| Reset output voltage | Voн | IRESET = -5 mA | | 4.5 | 4.75 | _ | V |
| | VoL | IRESET = +5 mA | | _ | 0.12 | 0.4 | V |
| Reset-output minimum power voltage | VCCL | IRESET = +50 μA | | _ | 0.8 | 1.2 | V |

^{*:} This parameter is guaranteed by design, which is not supported by a final test.

7.2 AC Characteristics

 $(Vcc = +5 V, Ta = +25^{\circ}C)$

| Parameter | | Symbol | Conditions | Value | | | Unit |
|--------------------------------------|---------|--------|-------------------------------|-------|-----|------|------|
| | | Symbol | Conditions | Min | Тур | Max | Onit |
| Power-on reset hold time | | tpr | CTP = 0.1 μF | 80 | 130 | 180 | ms |
| Watchdog timer monitoring time | | two | CTW = 0.01 μF CTP = 0.1 μF | 7.5 | 15 | 22.5 | ms |
| Watchdog timer reset time | | twr | CTP = 0.1 μF | 5 | 10 | 15 | ms |
| CK input pulse duration | | tckw | _ | 500 | _ | _ | ns |
| CK input pulse cycle | | tckt | _ | 20 | _ | _ | μs |
| Reset (RESET) output transition time | Rising | tr* | CL = 50 pF | _ | _ | 500 | ns |
| | Falling | tf* | CL = 50 pF | _ | _ | 500 | ns |

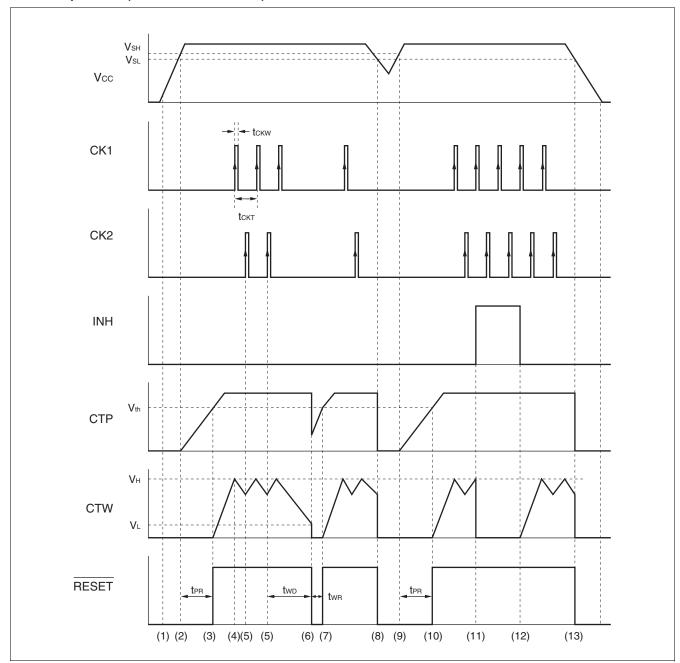
 $[\]ensuremath{^{\star}}\xspace$ The voltage range is 10% to 90% at testing the reset output transition time.

Document Number: 002-08552 Rev. *C



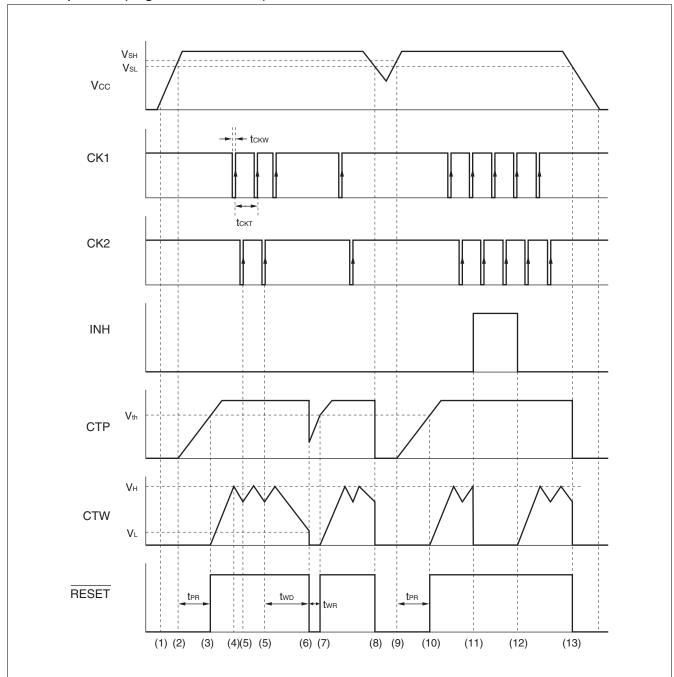
8. Timing Diagram

8.1 Basic Operation (Positive Clock Pulse)



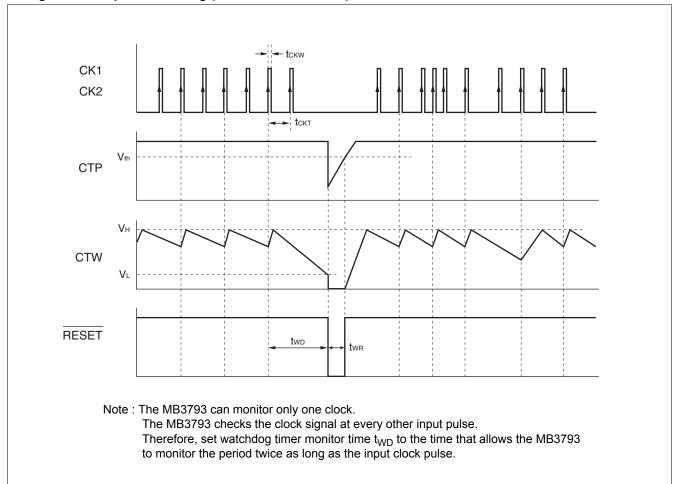


8.2 Basic Operation (Negative Clock Pulse)



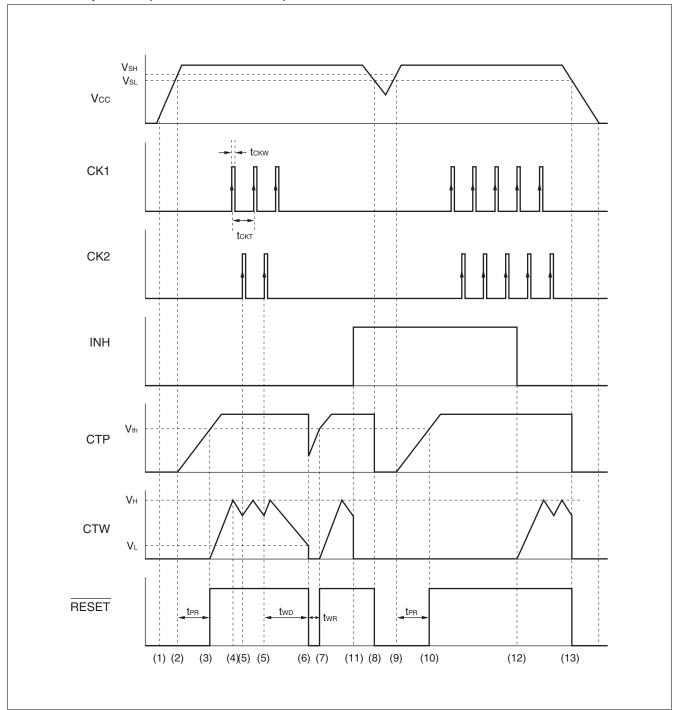


8.3 Single-Clock Input Monitoring (Positive Clock Pulse)



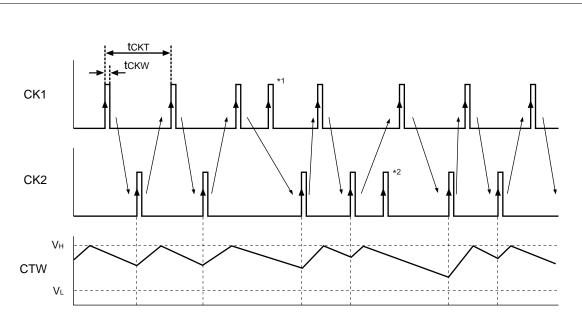


8.4 Inhibition Operation (Positive Clock Pulse)





8.5 Clock Pulse Input Supplementation (Positive Clock Pulse)



Note: The MB3793 watchdog timer monitors Clock1 (CK1) and Clock2 (CK2) pulses alternately. When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (C_{TW}) switches to charging from discharging.

When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored.

In the above figure, pulse *1 and *2 are ignored.



9. Operation Sequence

1. Positive Clock Pulse Input

Refer to "8.1 Basic Operation (Positive Clock Pulse)" under "8. Timing Diagram"

2. Negative Clock Pulse Input

Refer to "8.2 Basic Operation (Negative Clock Pulse)" under "8. Timing Diagram"

The MB3793 operates in the same way whether it inputs positive or negative pulses.

3. Clock Monitoring

To use the MB3793 while monitoring only one clock, connect clock pins CK1 and CK2.

Although the MB3793 operates basically in the same way as when monitoring two clocks, it monitors the clock signal at every other input pulse.

Refer to "8.3 Single-Clock Input Monitoring (Positive Clock Pulse)" under "8. Timing Diagram"

4. Description of Operations

The numbers given to the following items correspond to numbers (1) to (13) used in "8. Timing Diagram"

- (1) The MB3793 outputs a reset signal when the supply voltage (V_{CC}) reaches about 0.8 V (V_{CCL})
- (2) If V_{CC} reaches or exceeds the rise-time detected voltage V_{SH}, the MB3793 starts charging the power-on reset hold time setting capacitor C_{TP}. At this time, the output remains in a reset state. The V_{SH} value is 4.60 V (Typ) .
- (3) When C_{TP} has been charged for a certain period of time T_{PR} (until the CTP pin voltage exceeds the threshold voltage (V_{th}) after the start of charging), the MB3793 cancels the reset (setting the RESET pin to "H" level from "L" level). The V_{th} value is about 3.6 V with V_{CC} = 5.0 V

The power-on reset hold time t_{PR} is set with the following equation:

 t_{PR} (ms) $\approx A \times C_{TP}$ (μF)

The value of A is about 1300 with V_{CC} = 5.0 V. The MB3793 also starts charging the watchdog timer monitor time setting capacitor (C_{TW}).

- (4) When the voltage at the watchdog timer monitor time setting pin C_{TW} reaches the "H" level threshold voltage V_H, the CTW switches from the charge state to the discharge state.
 - The value of V_H is always about 1.24 V regardless of the detected voltage.
- (5) If the CK2 pin inputs a clock pulse (positive edge trigger) when the C_{TW} is being discharged in the CK1-CK2 order or simultaneously, the C_{TW} switches from the discharge state to the charge state.
 - The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses with the system logic circuit operating normally.
- (6) If no clock pulse is fed to the CK1 or CK2 pin within the watchdog timer monitor time t_{WD} due to some problem with the system <u>logic cir</u>cuit, the CTW pin is set to the "L" level threshold voltage V_L or less and the MB3793 outputs a reset signal (setting the RESET pin to "L" level from "H" level).

The value of V_L is always about 0.24 V regardless of the detected voltage.

The watchdog \bar{t} imer monitor time t_{WD} is set with the following equation:

 t_{WD} (ms) $\approx B \times C_{TW}$ (μF) + $C \times C_{TP}$ (μF)

The value of B is hardly affected by the power supply voltage; it is about 1500 with V_{CC} = 5.0 V.

The value in C is about 3 which is tremendously smaller than the value in B. For this reason, it is possible to simplify the formula as below when $C_{TP}/C_{TW} \approx 10$ or less. t_{WD} (ms) $\approx B \times C_{TW}$ (μ F)

(7) When a certain period of time t_{WR} has passed (until the CTP pin voltage reaches or exceeds Vth again after recharging the C_{TP}), the MB3793 cancels the reset signal and starts operating the watchdog timer.

The watchdog timer monitor reset time t_{WR} is set with the following equation:

 t_{WR} (ms) \approx D x C_{TP} (μ F) The value of D is 100

with $V_{CC} = 5.0 \text{ V}$.

The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses. If no clock pulse is input, the MB3793 repeats operations (6) and (7).

- (8) If V_{CC} is lowered to the fall-time detected voltage (V_{SL}) or less, the CTP pin voltage decreases and the MB3793 outputs a reset signal (setting the RESET pin to "L" level from "H" level). The value of V_{SL} is 4.50 V (Typ).
- (9) When V_{CC} reaches or exceeds V_{SH} again, the MB3793 starts charging the C_{TP} .
- (10) When the CTP pin voltage reaches or exceeds V_{th} , the MB3793 cancels the reset and restarts operating the watchdog timer. It repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses.

Document Number: 002-08552 Rev. *C



(11) Making the inhibit pin active (setting the INH pin to "H" from "L") forces the watchdog timer to stop operation.

This stops only the watchdog timer, leaving the MB3793 monitoring V_{CC} (operations (8) to (10)).

The watchdog timer remains inactive unless the inhibit input is canceled.

The inhibition (INH) pin must be connecting a voltage of more low impedance, to evade of the noise.

- (12) Canceling the inhibit input (setting the INH pin to "L" from "H") restarts the watchdog timer.
- (13) The reset signal is output when the power supply is turned off to set V_{CC} to V_{SL} or less.

1. Equation of Time-Setting Capacitances (C_{TP} and C_{TW}) and Set Time

$$t_{PR}$$
 [ms] $\approx A \times C_{TP}$ [μF]

$$t_{WD}$$
 [ms] \approx B \times C_{TW} [μ F] + C \times C_{TP} [μ F]

However, when $C_{TP}/C_{TW} \approx 10$ or less, t_{WD} [ms] $\approx B \times C_{TW}$ [μ F]

$$t_{WR}$$
 [ms] $\approx D \times C_{TP}$ [μ F]

Values of A, B, C, and D

| Α | В | С | D | Remark |
|------|------|---|-----|--------------------|
| 1300 | 1500 | 3 | 100 | V_{CC} = 5.0 V |

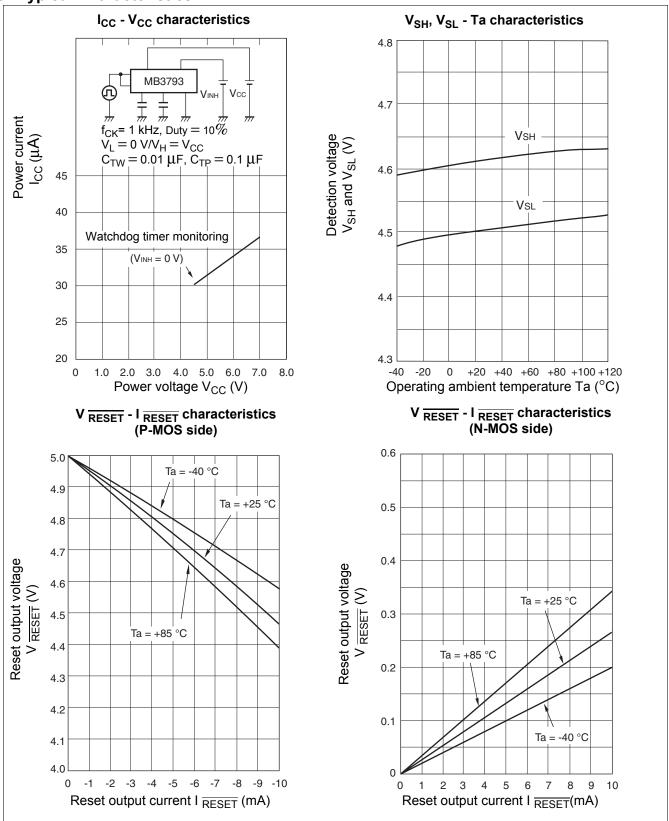
Note: The width of value of t_{PR} , t_{WD} and t_{WR} becomes the same ratio as width (Min, Max) of each specification value.

2. Example (when $C_{TP} = 0.1 \mu F$ and $C_{TW} = 0.01 \mu F$)

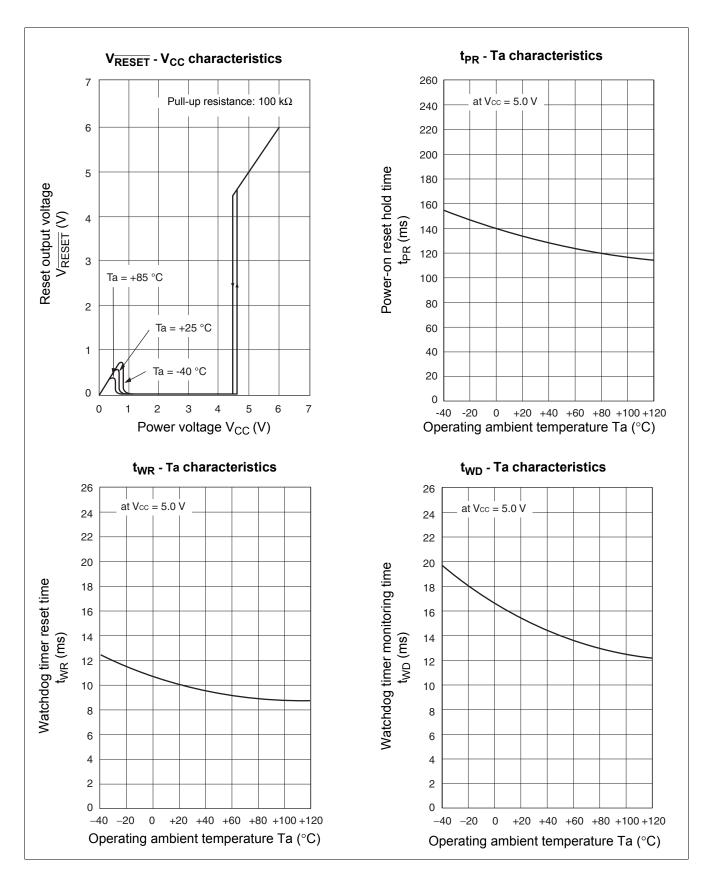
| | Symbol | V _{CC} = 5.0 V |
|------|-----------------|-------------------------|
| Time | t _{PR} | 130 |
| (ms) | t _{WD} | 15 |
| | t _{WR} | 10 |



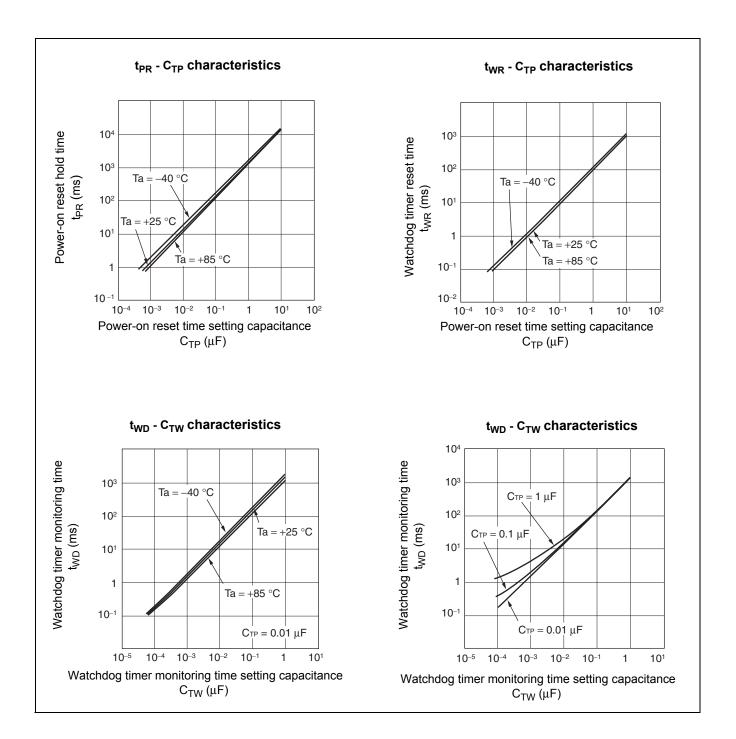
10. Typical Characteristics









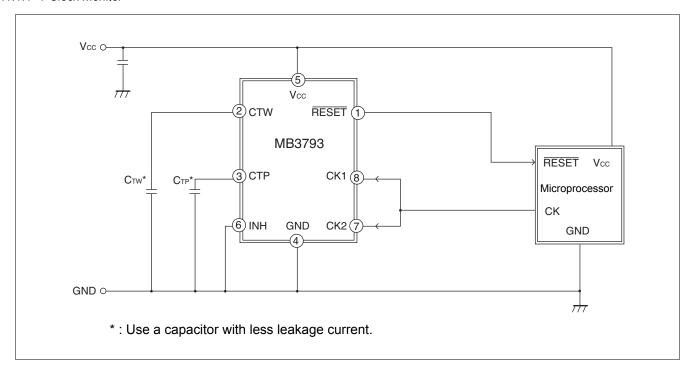




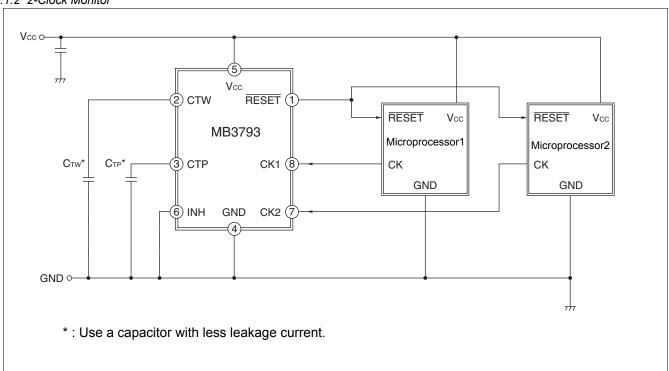
11. Application Example

11.1 Supply Voltage Monitor and Watchdog Timer

11.1.1 1-Clock Monitor

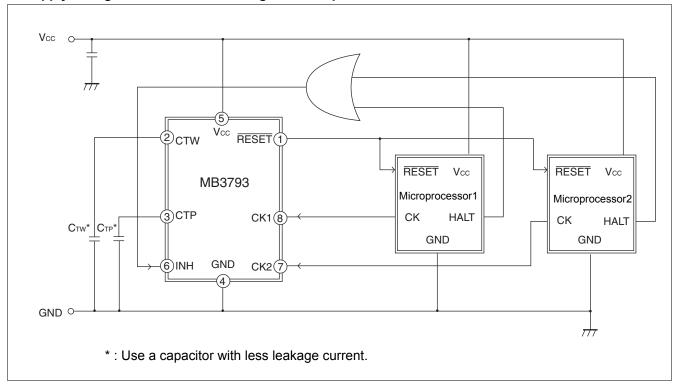


11.1.2 2-Clock Monitor

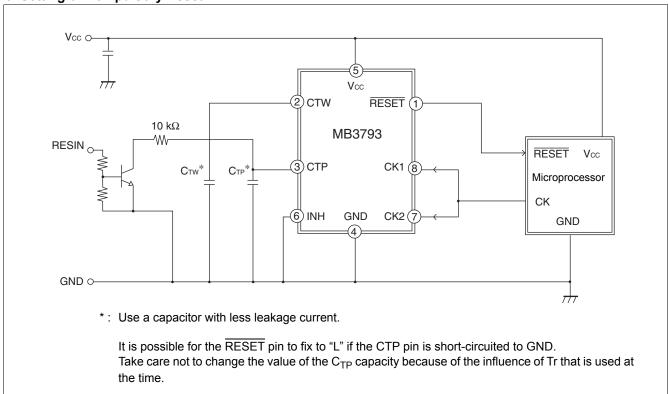




11.2 Supply Voltage Monitor and Watchdog Timer Stop



11.3 Setting of Compulsory Reset





12. Usage Precaution

1. Do Not Configure the IC over the Maximum Ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.

It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have a bad effect on the reliability of the LSI.

2. Use the Devices within Recommended Operating Conditions

The recommended operating conditions are under which the LSI is guaranteed to operate.

The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed Circuit Board Ground Lines should be Set Up with Consideration for Common Impedance

4. Take Appropriate Measures Against Static Electricity

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- · Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 k Ω to 1 M Ω between body and ground.

5. Do Not Apply Negative Voltages

The use of negative voltages below -0.3 V may create parasitic transistors on LSI lines, which can cause malfunctions.

13. Ordering Information

| Part Number | Package | Remarks |
|--------------|-------------------------------|---------|
| MB3793-45PF | 8-pin plastic SOP (SOE008) | - |
| MB3793-45PNF | 8-pin plastic SOP (SOB008) | - |

14. RoHS Compliance Information

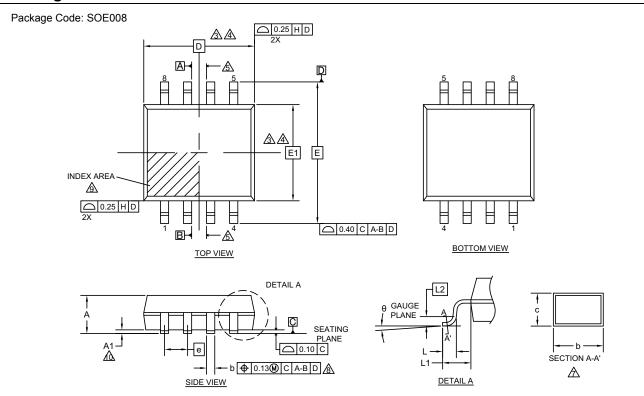
The LSI products of Spansion with "E1" are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

The product that conforms to this standard is added "E1" at the end of the part number.

Document Number: 002-08552 Rev. *C



15. Package Dimensions



| SYMBOL | DI | MENSIC | N | | |
|---------|----------------|----------|------|--|--|
| STWIBOL | MIN. | NOM. | MAX. | | |
| А | _ | _ | 2.25 | | |
| A1 | 0.05 | 1 | 0.20 | | |
| D | 6 | .35 BSC | | | |
| Е | 7 | 7.80 BSC | ; | | |
| E1 | 5.30 BSC | | | | |
| θ | 0° | | 8° | | |
| С | 0.13 | | 0.20 | | |
| b | 0.39 | 0.47 | 0.55 | | |
| L | 0.45 0.60 0.75 | | | | |
| L 1 | 1.25 REF | | | | |
| L 2 | 0.25 BSC | | | | |
| е | | 1.27 BS | С | | |

NOTES

- 1. ALL DIMENSIONS ARE IN MILLIMETER.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ⚠ DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

 DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST

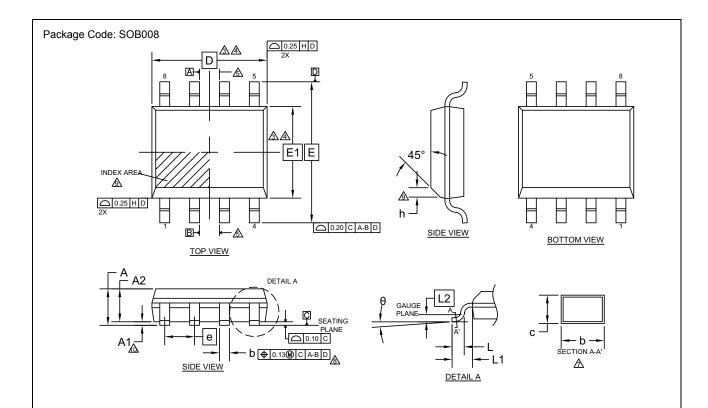
 EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH,

 THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING

 ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ⚠ DATUMS A & B TO BE DETERMINED AT DATUM H.
- 6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
- ⚠ DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- ⚠ THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
- 10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- 11. JEDEC SPECIFICATION NO. REF: N/A

002-15857 Rev. **





| SYMBOL | DIMENSIONS | | | |
|---------|------------|------|------|--|
| STWIBOL | MIN. | NOM. | MAX. | |
| А | _ | | 1.75 | |
| A1 | 0.05 | _ | 0.25 | |
| A2 | 1.30 | 1.40 | 1.50 | |
| D | 5.05 BSC. | | | |
| E | 6.00 BSC. | | | |
| E1 | 3.90 BSC | | | |
| θ | 0° | | 8° | |
| С | 0.15 | | 0.25 | |
| b | 0.36 | 0.44 | 0.52 | |
| L | 0.45 | 0.60 | 0.75 | |
| L 1 | 1.05 REF | | | |
| L 2 | 0.25 BSC | | | |
| е | 1.27 BSC. | | | |
| h | 0.40 BSC. | | | |

NOTES

- 1. ALL DIMENSIONS ARE IN MILLIMETER.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ⚠ DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

 DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST

 EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH,

 THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING

 ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ⚠ DATUMS A & B TO BE DETERMINED AT DATUM H.
- "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
- ⚠ DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- ATHIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
- 10 "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- 11. JEDEC SPECIFICATION NO. REF: N/A

002-15856 Rev. **



16. Major Changes

| Page | Section | Change Results | |
|--------------|-------------|--|--|
| Revision 3.0 |) | | |
| - | - | - Company name and layout design change | |
| 1 | DESCRIPTION | Deleted "There is also a mask option that can detect voltages of 4.9 V to 2.4 V in 0.1-V steps." | |

NOTE: Please see "Document History" about later revised information.

Document History

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|----------|---------|--------------------|--------------------|---|
| ** | - | TAOA | 01/06/2015 | Migrated to Cypress and assigned document number 002-08552. No change to document contents or format. |
| *A | 5151492 | TAOA | 03/01/2016 | Updated to Cypress template |
| *B | 5611415 | НІХТ | 01/31/2017 | Updated Pin Assignment: Change the package name from FPT-8P-M01 to SOE008 Change the package name from FPT-8P-M02 to SOB008 Updated Ordering Information: Change the package name from FPT-8P-M01 to SOE008 Change the package name from FPT-8P-M02 to SOB008 Updated Package Dimensions: Updated to Cypress format Deleted "Marking Format (Lead Free version)" Deleted "Labeling Sample (Lead free version)" Deleted "MB3793-45PF, MB3793-45PNF Recommended Conditions of Moisture Sensitivity Level" |
| *C | 5790329 | MASG | 06/29/2017 | Adapted Cypress new logo. |



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers cypress.com/arm Automotive cypress.com/automotive Clocks & Buffers cypress.com/clocks Interface cypress.com/interface Internet of Things cypress.com/iot Memory cypress.com/memory Microcontrollers cypress.com/mcu **PSoC** cypress.com/psoc Power Management ICs cypress.com/pmic Touch Sensing cypress.com/touch **USB Controllers** cypress.com/usb Wireless/RF cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2001-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Document Number: 002-08552 Rev. *C Revised June 29, 2017 Page 24 of 24

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Supervisory Circuits category:

Click to view products by Cypress manufacturer:

Other Similar products are found below:

NCP304LSQ38T1G NCP304LSQ40T1G NCP304LSQ42T1G NCP304LSQ43T1G NCP304LSQ46T1G NCP305LSQ11T1G NCP305LSQ16T1G NCP305LSQ17T1G NCP305LSQ18T1G NCP305LSQ24T1G NCP305LSQ25T1G NCP305LSQ29T1G NCP305LSQ31T1G NCP305LSQ32T1G NCP308MT250TBG NCP308SN300T1G NCP391FCALT2G NCV303LSN42T1G NCV308SN330T1G CAT1161LI-25-G CAT853STBI-T3 MAX1232CPA MAX705CPA CAT1026LI-30-G CAT1320LI-25-G CAT872-30ULGT3 LA-ispPAC-POWR1014-01TN48E NCP304HSQ18T1G NCP304HSQ29T1G NCP304LSQ27T1G NCP304LSQ29T1G NCP304LSQ45T1G NCP305LSQ35T1G NCP305LSQ35T1G NCP305LSQ35T1G NCP308MT300TBG NCV300LSN36T1G NCV302LSN30T1G NCV303LSN16T1G NCV303LSN22T1G NCV303LSN27T1G NCV30