MB39A130A 1ch DC/DC Buck Converter IC with Synchronous Rectification

Description

MB39A130A is a 1ch DC/DC Buck converter equipped with a bottom detection comparator and N-ch/N-ch synchronous rectification. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. MB39A130A realizes ultra-rapid response and high efficiency with built-in enhanced protection features.

Features

- Power conversion efficiency :96 % (Max.)
- Adjustable frequency setting by an external resistor :100 kHz to 600 kHz
- High accuracy reference voltage : ±1.0%
- Output voltage setting range :0.7 V to 5 V or fixed to 1.2 V/2.5 V
- Adjustable output voltages setting by the external control
- Input voltage range (V_{IN}) :4.5 V to 25 V
- Inductor saturation detection function which can be set optional
- Built-in over voltage protection function
- Built-in under voltage protection function
- Built-in over current protection function
- Built-in Power-Good detection function
- Built-in over temperature protection function
- Built-in soft-start circuit without load dependence
- Built-in discharge control circuit
- Built-in synchronous rectification type output driver for N-ch MOS FET
- Standby current : 0 [µA] (Typ.)
- Small package : TSSOP-24 (4.4 × 6.5 [mm])

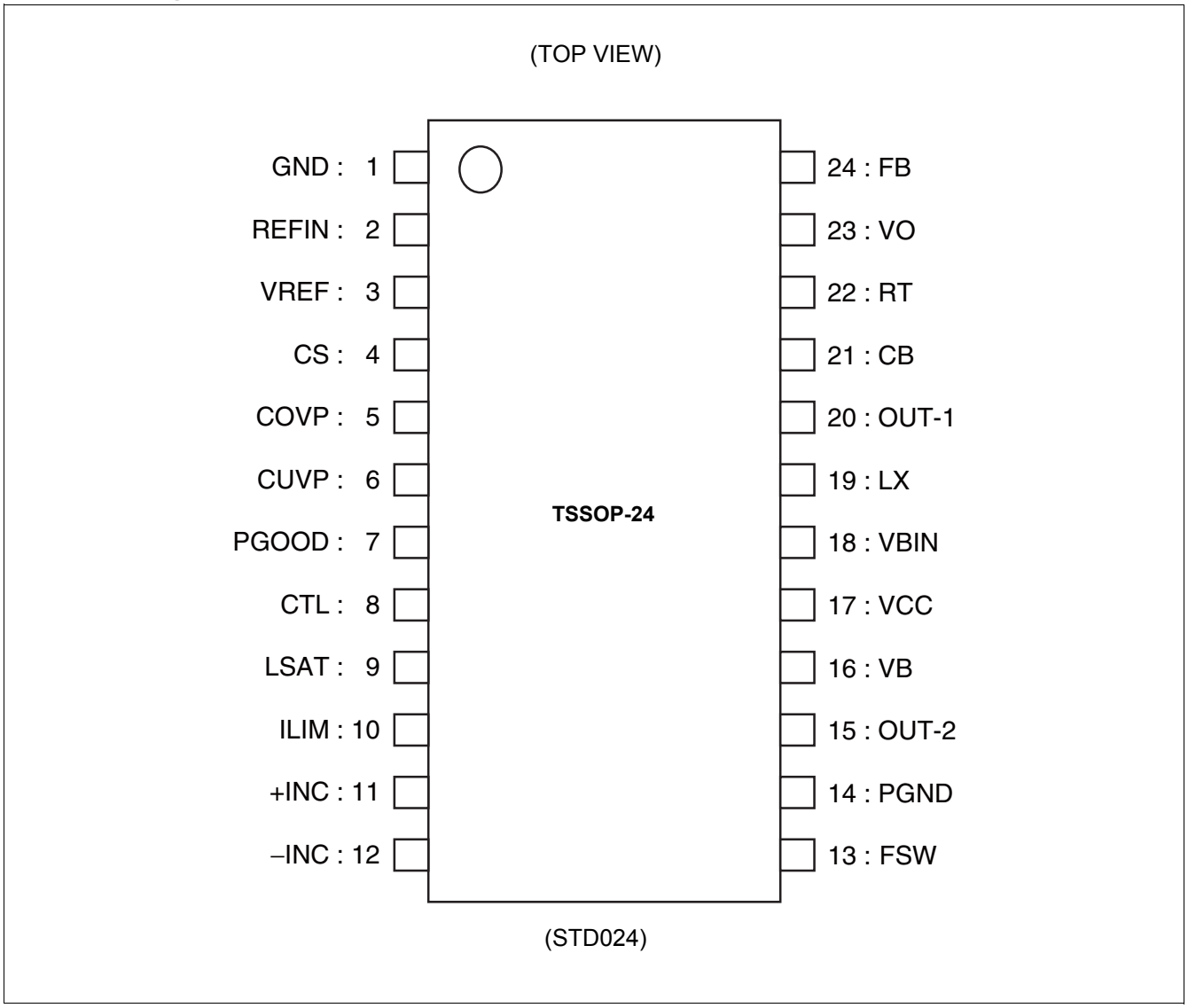
Applications

- Digital TV
- Photocopiers
- STB
- BD, DVD players/recorders
- Projectors

Various other advanced devices

Contents

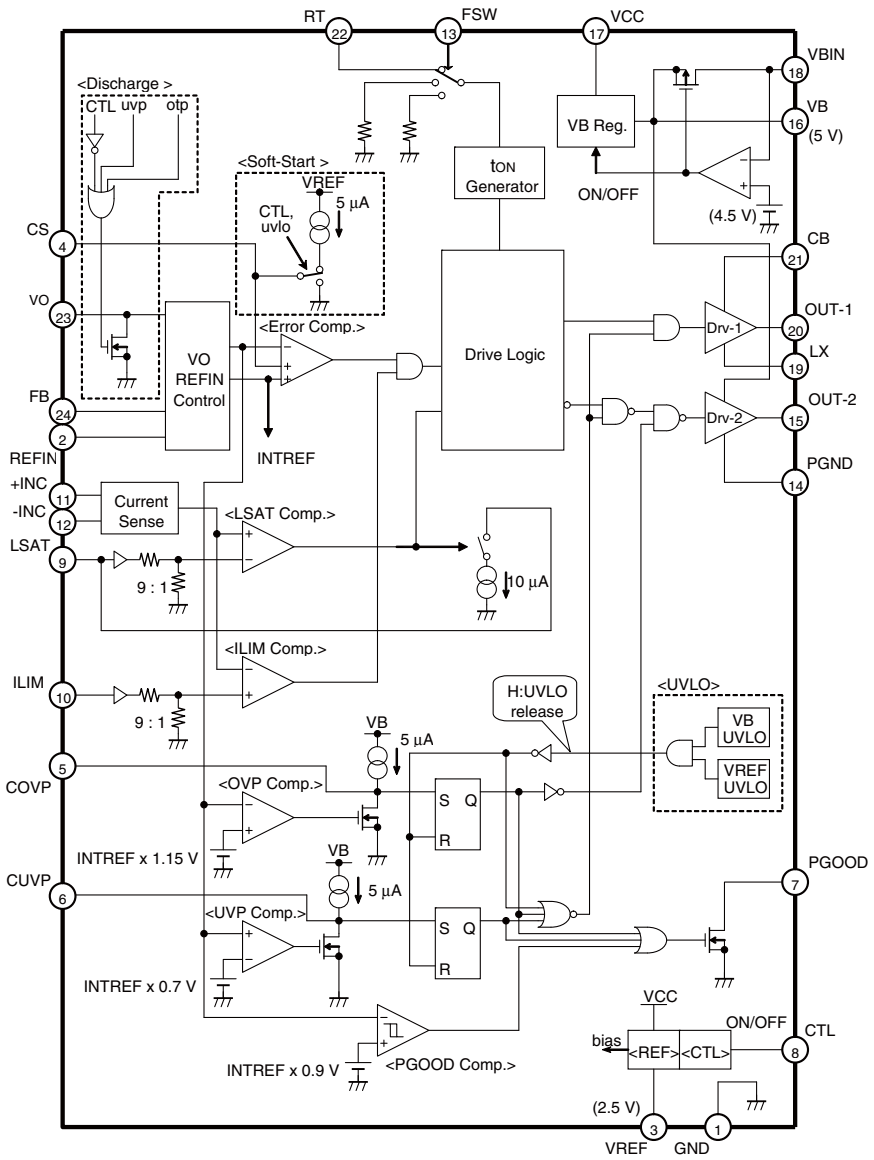
1. Pin Assignment



2. Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	GND	-	Ground pin.
2	REFIN	I	Reference voltage input pin for Error Comp.
3	VREF	O	Reference voltage output pin.
4	CS	I	Soft-start time setting capacitor connection pin.
5	COVP	-	Detection time setting capacitor connection pin for OVP function. The OVP function can be disabled by a short circuit with GND pin.
6	CUVP	-	Detection time setting capacitor connection pin for UVP function. The UVP function can be disabled by a short circuit with GND pin.
7	PGOOD	O	Power-Good detection circuit output pin. (Open-drain output)
8	CTL	I	Power supply control pin. IC changes to standby state when CTL is set to “L” level.
9	LSAT	I	Inductor oversaturation detection level setting voltage input pin.
10	ILIM	I	Over current detection level setting voltage input pin.
11	+INC	I	Current detection block (Current Sense) input pin.
12	-INC	I	Current detection block (Current Sense) input pin.
13	FSW	I	Preset value switching pin for operating frequency.
14	PGND	-	Ground pin for output circuit.
15	OUT-2	O	Output pin for external low-side FET gate drive.
16	VB	O	Bias output pin for output circuit.
17	VCC	-	Power supply pin.
18	VBIN	I	Bias voltage external input pin for output circuit and control circuit.
19	LX	-	Inductor and external high-side FET source and external low-side FET drain connection pin.
20	OUT-1	O	Output pin for external high-side FET gate drive.
21	CB	-	Connection pin for boot strap capacitor. It connects a capacitor between CB and LX pins.
22	RT	-	Connection pin for t_{ON} time setting resistor.
23	VO	I	Input pin for DC/DC output voltage.
24	FB	I	Feedback pin for DC/DC output voltage.

3. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	—	—	27	V
CB pin input voltage	V_{CB}	—	—	32	V
Voltage between CB and LX	V_{CBLX}	—	—	7	V
Bias external input voltage	V_{BIN}	—	—	7	V
Control input voltage	V_I	CTL pin	—	27	V
Input voltage	V_I	FB, VO, REFIN, FSW pins	—	VB + 0.3	V
	V_{+INC}	—	—	27	V
	V_{-INC}	—	—	27	V
	V_{ILIM}	—	—	VB + 0.3	V
	V_{LSAT}	—	—	VB + 0.3	V
PGOOD pin voltage	V_{PG}	—	—	7	V
Output current	I_{OUT}	DC	—	60	mA
Power dissipation	P_D	Ta ≤ + 25°C	—	1315	mW
Storage temperature	T_{STG}	—	-55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	—	4.5	—	25.0	V
CB pin input voltage	V_{CB}	—	—	—	30	V
Reference voltage output current	I_{REF}	—	-100	—	0	µA
Bias output current	I_{VB}	—	-1	—	—	mA
CTL pin input voltage	V_I	CTL pin	0	—	25	V
Input voltage	V_I	FB, VO, REFIN, FSW pins	0	—	VB	V
	V_{+INC}	—	-0.3	—	+ 2.9	V
	V_{-INC}	—	-0.3	—	+ 25	V
	V_{ILIM}	—	0	—	VB	V
	V_{LSAT}	—	0	—	VB	V
PGOOD pin output voltage	V_{PG}	—	0	—	5.5	V
PGOOD pin output current	I_{PG}	—	0	—	4	mA
Peak output current	I_{OUT}	Duty≤5% ($t = 1/f_{OSC} \times$ Duty)	-1200	—	+ 1200	mA
Operation frequency range	f_{OSC}	—	100	450	780	kHz
Timing resistor	R_T	—	—	43	—	kΩ
Current detection resistor	R_S	—	—	10	—	mΩ
Soft start capacitor	C_S	—	—	0.018	—	µF
CB pin capacitor	C_{CB}	—	—	0.1	—	µF
Reference voltage output capacitor	C_{REF}	—	—	0.01	1.0	µF
Bias voltage output capacitor	C_{VB}	—	—	2.2	10	µF
Operating ambient temperature	Ta	—	-30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

6. Electrical Characteristics

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [REF]	Output voltage	V_{REF}	3	—	2.463	2.500	2.537	V
	Load stability	Load	3	VREF pin = 0 µA to -100 µA	—	1	10	mV
	Short-circuit output current	I_{OS}	3	VREF pin = 0 V	-20	-10	-5	mA
Bias Voltage Block [VB Reg.]	Output voltage	V_B	16	—	4.9	5.0	5.1	V
	Inside/Outside switching threshold	V_{TLH}	18	VBIN pin ↑	4.3	4.5	4.7	V
		V_{THL}	18	VBIN pin ↓	4.1	4.3	4.5	V
	Switch (SW) resistor	R_{SW}	18	VBIN pin = 5 V	—	4*1	—	Ω
Under voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	16	VB pin	3.8	4.0	4.2	V
		V_{THL}	16	VB pin	3.1	3.3	3.5	V
	Hysteresis width	V_H	16	VB pin	—	0.7*1	—	V
	Threshold voltage	V_{TLH}	3	VREF pin	1.8	2.0	2.2	V
		V_{THL}	3	VREF pin	1.6	1.8	2.0	V
	Hysteresis width	V_H	3	VREF pin	—	0.2*1	—	V
Soft-Start/Discharge Block [Soft-Start/ Discharge]	Charge current	I_{CS}	4	CTL pin = 5 V, CS pin = 0 V	-6.3	-4.5	-3.1	µA
	Electrical discharge resistance	R_D	23	CTL pin = 0 V, VO pin ≥ 0.3 V	—	16*1	—	Ω
	Discharge end voltage	V_O	23	CTL pin = 0 V	—	0.3*1	—	V
ON/OFF Time Generator Block [t_{ON} Generator]	ON time	t_{ON}	20	RT pin = 43 kΩ, FSW pin = GND, VCC pin = 15 V, VO pin = 1.5 V	246	280	314	ns
	ON time (Preset value 1)	t_{ON_2}	20	RT pin = GND, FSW pin = VREF pin, VCC pin = 15 V, VO pin = 1.5 V	272	390	508	ns
	ON time (Preset value 2)	t_{ON_3}	20	RT pin = GND, FSW pin = VB pin, VCC pin = 15 V, VO pin = 1.5 V	142	220	298	ns
	Minimum OFF time	t_{OFF}	20	—	360	480	600	ns
	R_T external condition	V_{FSW1}	13	FSW pin	0	—	1.5	V
	Preset value 1 condition	V_{FSW2}	13	FSW pin	1.5	VREF	VB-1.5	V
	Preset value 2 condition	V_{FSW}	13	FSW pin	VB-1.5	—	VB	V
	Input current	I_{FSWL}	13	FSW pin = 0 V	-10	-5	—	µA
		I_{FSWM}	13	FSW pin = VREF pin	-1	0	+1	µA
		I_{FSWH}	13	FSW pin = VB pin	—	5	10	µA

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Voltage Setting Block [VO REFIN Control, Error Comp.]	Output bottom detection voltage	V_{O1}	23	REFIN pin = GND pin, FB pin = VB pin	1.172	1.190	1.208	V
		V_{O2}	23	REFIN pin = VB pin, FB pin = VB pin	2.453	2.490	2.527	V
	Feedback voltage	V_{FB1}	24	REFIN pin = GND pin	0.693	0.700	0.707	V
		V_{FB1T}	24	REFIN pin = GND pin*3, Ta = -20°C to +70°C	0.689*2	0.700	0.711*2	V
		V_{FB2}	24	REFIN pin = VB pin	1.442	1.457	1.472	V
		V_{FB2T}	24	REFIN pin = VB pin*3, Ta = -20°C to +70°C	1.435*2	1.457	1.479*2	V
	REFIN input current	I_{REFIN}	2	REFIN pin = 0.6 V	-0.5	0	+0.5	µA
	FB input current	I_{FB}	24	FB pin = 0.7 V	-0.5	0	+0.5	µA
	VO input current	I_{VO}	23	VO pin = 2 V	—	17.0	24.3	µA
	Threshold voltage	V_{TH1}	24,2	REFIN, FB pins : Hi-side	2.4	2.5	—	V
		V_{TH2}	2	REFIN pin : Lo-side	—	0.3	0.4	V
Current Detection Block [Current Sense]	Input current	I_{INC}	11,12	+INC, -INC pins = 0	-1.0	-0.3	—	µA
Over Current Detection Block [ILIM Comp.]	Current limit setting value	V_{TH}	11,12	(+INC pin) - (-INC pin) ILIM pin = 5 V Internally fixed value	40	50	60	mV
		V_{TH2}	11,12	(+INC pin) - (-INC pin) ILIM pin = 1.0 V Externally fixed value	90	100	110	mV
	Input current	I_{ILIM}	10	ILIM pin = 0 V	-1	0	+1	µA
	Threshold voltage	V_{TH3}	10	ILIM pin	3.5	3.7	—	V
Inductor Saturation Detection Block [LSAT Comp.]	Oversaturation detection setting value	V_{TH}	11,12	(+INC pin) - (-INC pin) LSAT pin = 2.0 V	180	200	220	mV
	Input current	I_{LSAT}	9	LSAT pin = 0 V	-1	0	+1	µA
	LSAT pin sink current at detection of oversaturation	I_{LSAT2}	9	LSAT pin = 1 V	7.7	10.0	14.3	µA

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Over-voltage Protection Circuit Block [OVP Comp.]	Over-voltage detecting voltage	V_{OVP}	24	Error Comp. input	INTREF ×1.12	INTREF ×1.15	INTREF ×1.18	V
	Charge current	I_{COVP}	5	—	-7.7	-5.5	-4.1	µA
	Threshold voltage	V_{TH}	5	COVP pin	—	VB×0.5	—	V
	COVP pin on-resistance	R_{COVP}	5	—	—	1.1*1	—	kΩ
Under-voltage Protection Circuit Block [UVP Comp.]	Under-voltage detecting voltage	V_{UVP}	24	Error Comp. input	INTREF ×0.65	INTREF ×0.70	INTREF ×0.75	V
	Charge current	I_{CUVP}	6	—	-7.7	-5.5	-4.1	µA
	Threshold voltage	V_{TH}	6	CUVP pin	—	VB×0.5	—	V
	CUVP pin on-resistance	R_{CUVP}	6	—	—	1.1*1	—	kΩ
Power-Good Detection Circuit Block [PGOOD Comp.]	Threshold voltage	V_{THL}	24	Error Comp. input	INTREF ×0.87	INTREF ×0.90	INTREF ×0.93	V
	Hysteresis width	VH	24	Error Comp. input	—	INTREF×0.02*1	—	V
	Output leak current	I_{LEAK}	7	PGOOD pin = 5 V	—	0	1	µA
	“L” level output voltage	V_{OL}	7	PGOOD pin = 1 mA	—	0.1	0.4	V
Over-temperature Protection Circuit Block [OTP]	Protection temperature	T_{OTPH}	—	—	—	+150*1	—	°C
		T_{OTPL}	—	—	—	+125*1	—	°C

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Block [Drv-1, Drv-2]	High-side output on-resistance	R_{OH}	20	OUT–1 pin = – 100 mA	—	4	7	Ω
		R_{OL}	20	OUT–1 pin = 100 mA	—	1.0	3.5	Ω
	Low-side output on-resistance	R_{OH}	15	OUT–2 pin = –100 mA	—	4	7	Ω
		R_{OL}	15	OUT–2 pin = 100 mA	—	1.0	3.5	Ω
	Output source current	I_{SOURCE}	15,20	LX pin = 0 V, CB pin = 5 V, OUT–1, OUT–2 pins = 2.5 V, Duty ≤ 5%	—	–0.5*1	—	A
	Output sink current	I_{SINK1}	20	LX pin = 0 V, CB pin = 5 V, OUT-1 pin = 2.5 V, Duty ≤ 5%	—	0.9*1	—	A
		I_{SINK2}	15	OUT-2 pin = 2.5 V, Duty ≤ 5%	—	1.8*1	—	A
	Dead time	T_D	15,20	LX pin = 0 V, CB pin = 5 V	—	50*1	—	ns
Control Block [CTL]	ON condition	V_{ON}	8	—	2	—	25	V
	OFF condition	V_{OFF}	8	—	0	—	0.8	V
	Input current	I_{CTLH}	8	CTL pin = 5 V	—	25	40	µA
		I_{CTLL}	8	CTL pin = 0 V	—	0	1	µA
General	Standby current	I_{CCS}	17	CTL pin = 0 V	—	0	10	µA
	Power-supply current	I_{CC1}	17	CTL pin = 5 V, REFIN pin = GND pin, LX pin = 0 V, FB pin = 1.0 V	—	1.3	2.2	mA
		I_{CC2}	17	CTL pin = 5 V, LX pin = 0 V, FB pin = 1.0 V, VBIN pin = 5 V	—	130	220	µA

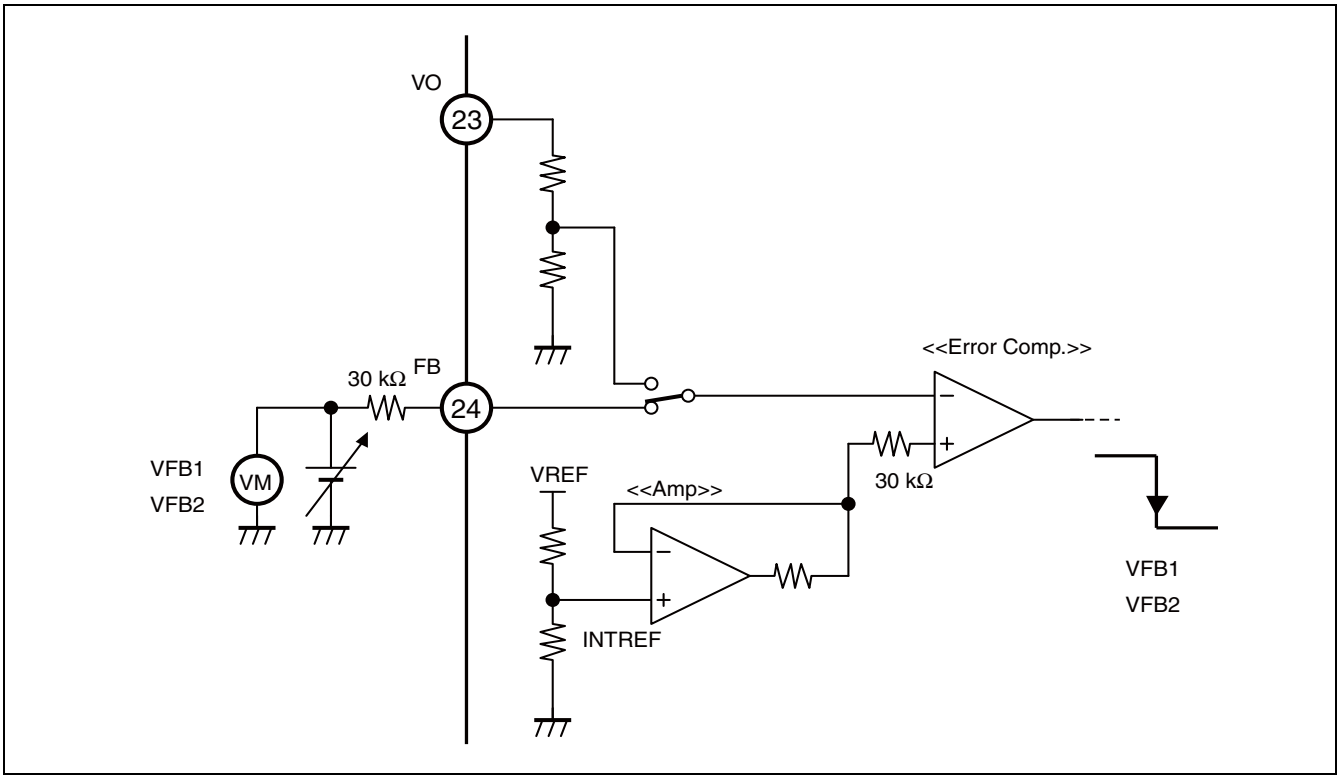
*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: This parameter is guaranteed by design, which is not supported by a final test.

*3: For the measurement circuit, see the “ Diagram of Feedback Voltage Measurement Circuit”.

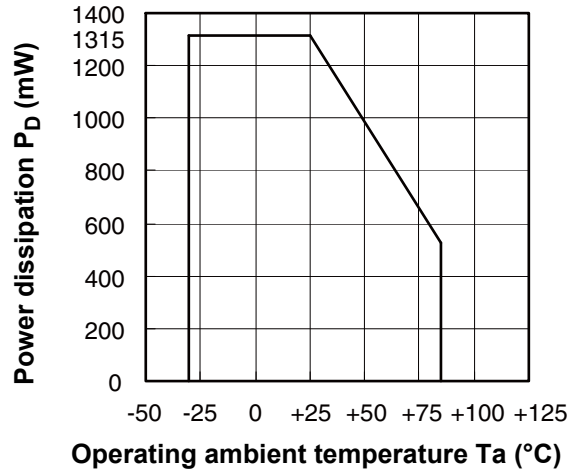
7. Diagram of Feedback Voltage Measurement Circuit

- VFB1,VFB2

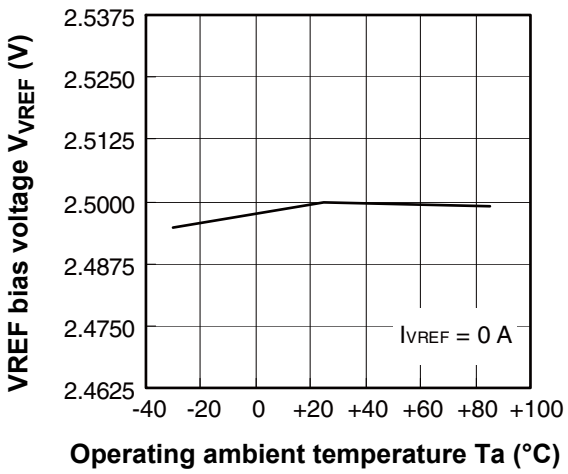


8. Typical Characteristics

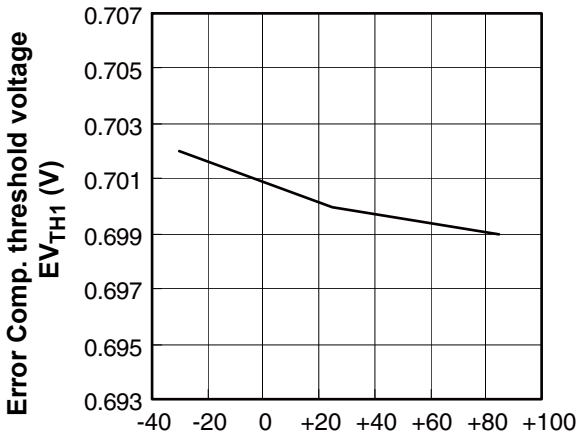
Power dissipation vs.
Operating ambient temperature



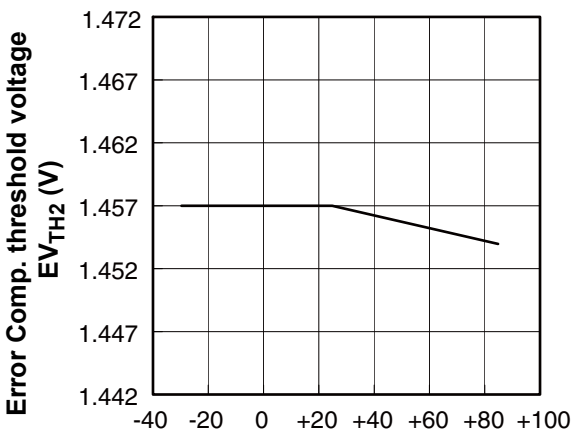
VREF bias voltage vs.
Operating ambient temperature



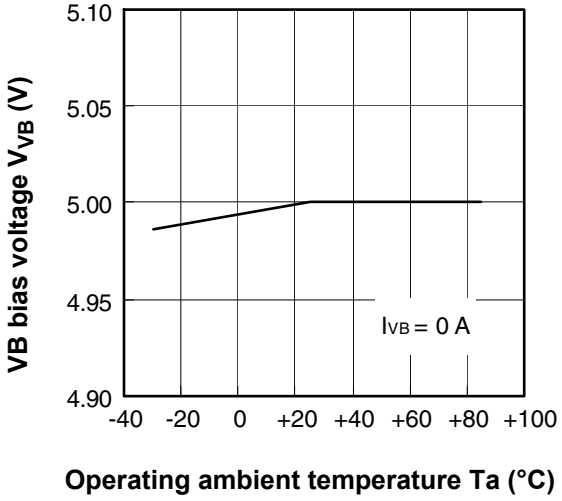
Error Comp. threshold voltage vs.
Operating ambient temperature



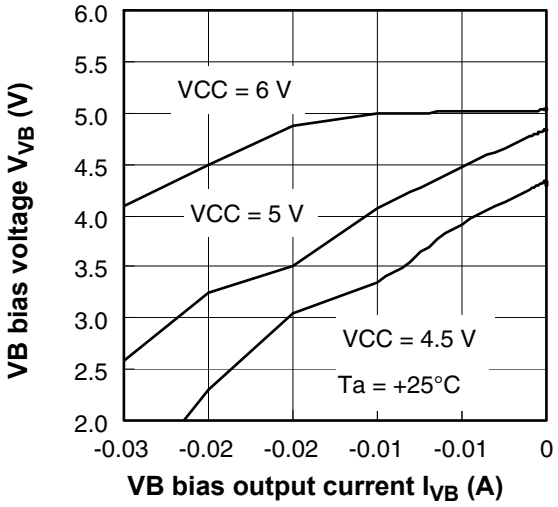
Error Comp. threshold voltage vs.
Operating ambient temperature



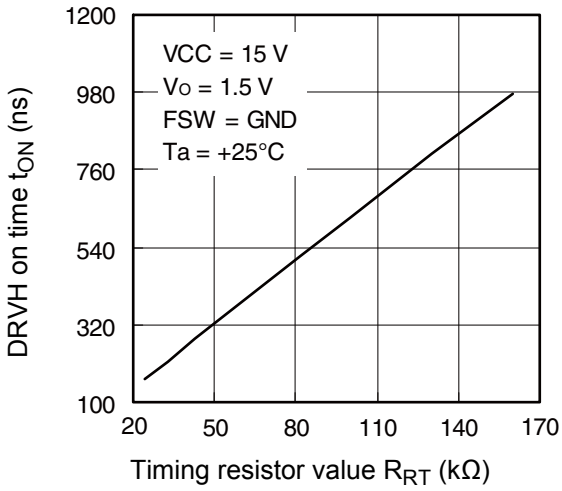
VB bias voltage vs.
Operating ambient temperature



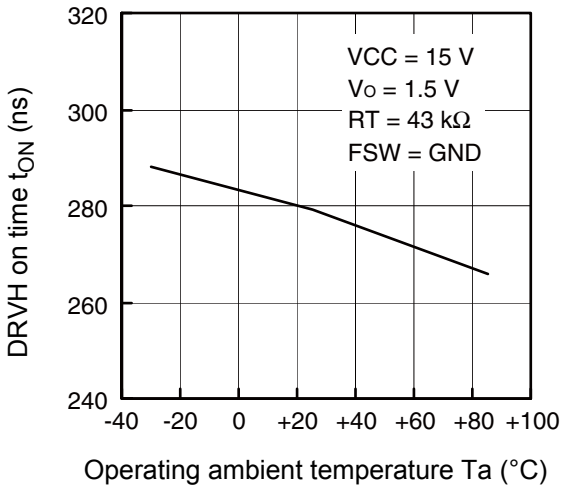
VB bias voltage vs.
VB bias output current



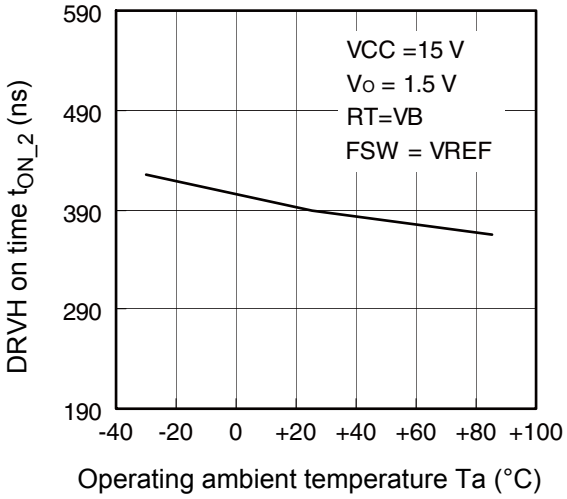
DRVH on time vs.
Timing resistor value



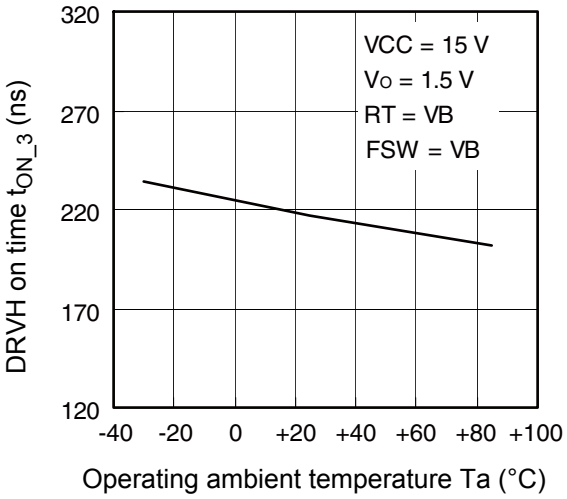
DRVH on time vs.
Operating ambient temperature



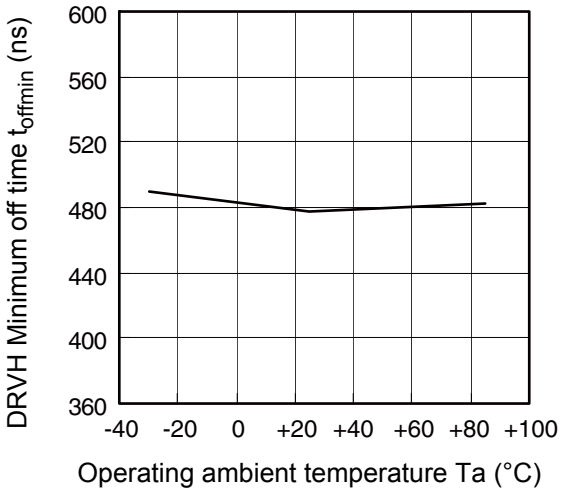
DRVH on time vs.
Operating ambient temperature



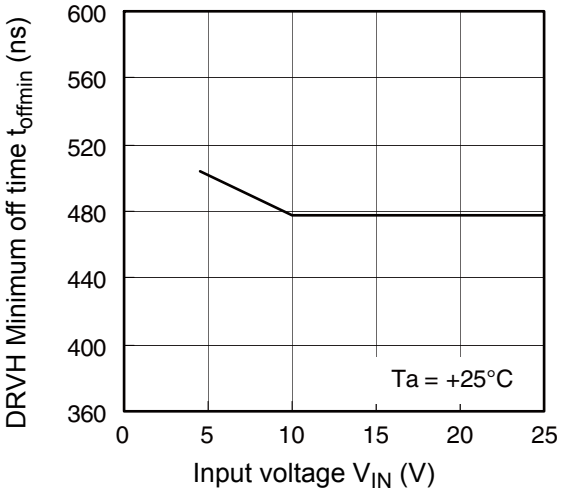
DRVH on time vs.
Operating ambient temperature

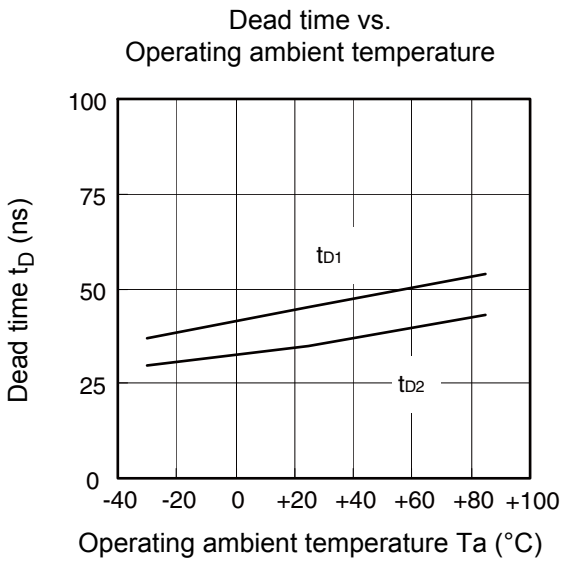


DRVH Minimum off time vs.
Operating ambient temperature



DRVH Minimum off time vs.
Input voltage




Dead time vs.
Operating ambient temperature
Dead time t_D (ns)
100
75
50
25
0
t_{D1}
t_{D2}
-40
-20
0
+20
+40
+60
+80
+100
Operating ambient temperature Ta (°C)

9. Function

Bottom detection comparator system

The bottom detection comparator system uses fixed ON time (t_{ON}) and the switching ripple voltage which superimposed the output voltage (V_O) , instead of a certain triangular waveform.

The t_{ON} time is uniquely defined by the power supply voltage (V_{IN}) and the output voltage (V_O) .

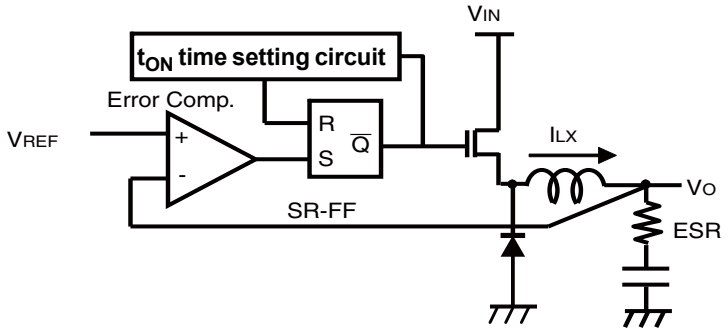
During the t_{ON} period, a current is supplied from the power supply voltage (V_{IN}) . This results in an increased inductor current (I_{LX}). And also an increased output voltage (V_O) due to the parasitic resistance (ESR) of the output capacitor.

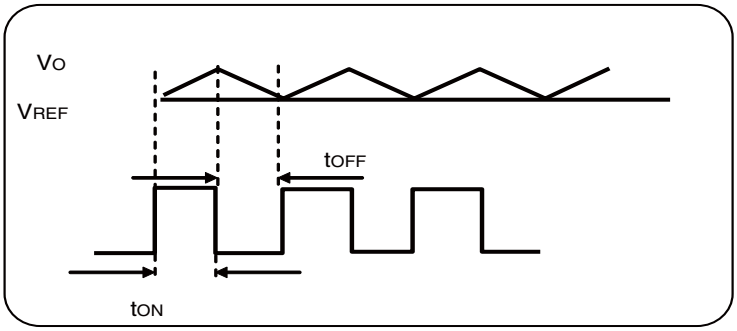
And when the t_{OFF} period arrives, the energy accumulated in the inductor is supplied to the load to decrease the inductor current (I_{LX}) gradually. Consequently, the output voltage (V_O) , which has been increasing due to the parasitic resistance (ESR) of the output capacitor, also decreases.

When the output voltage goes below a certain V_{REF} potential, SR-FF is set and the t_{ON} period comes back.

Switching is repeated as described above. Error Comp. is used to compare the reference voltage (VREF) with the output voltage (V_O) to control the off-duty condition in order to stabilize the output voltage.

Bottom Detection Comparator Model





9.1 Reference Voltage Block (REF)

The reference voltage block (REF) generates a temperature-compensated stable voltage (2.5 V Typ.) based on the voltage supplied from the VCC pin (Pin 17) . It is used as the reference power supply for the IC's internal circuit.

The reference voltage is output from the VREF pin (Pin 3), and up to 100 µA can be supplied to the outside as the maximum load current.

9.2 Under Voltage Lockout Protection Circuit Block (UVLO)

A bias voltage (V_B) , a transitional state at startup, or a sudden drop in an internal reference voltage (V_{REF}) leads to malfunction of the control IC, causing system destruction/deterioration. To prevent such malfunction, the under voltage lockout protection circuit detects a voltage drop at the VB pin (Pin 16) or the VREF pin (Pin 3) and fixes the OUT-1 pin (Pin 20) and the OUT-2 pin (Pin 15) to the "L" level. When voltages at the VB pin and the VREF pin exceed the threshold voltage of the under voltage lockout protection circuit, the system is restored.

Table of Protection Circuit (VB-UVLO, VREF-UVLO) Operation Functions

The logics of the following pins are fixed during UVLO operation (when VB and VREF voltages are below the UVLO threshold voltage) .

OUT-1	OUT-2	CS	OVP	UVP
L	L	L	Latch reset COVP = L	Latch reset CUVP = L

9.3 Soft-start Block (Soft-Start)

It prevents a rush current or an output voltage (V_O) overshooting at the output start.

It prevents a rush current at start-up by connecting a capacitor to the CS pin (Pin 4) .

When the CTL pin (Pin 8) is set to the "H" level, the capacitor connected to the CS pin starts charging and its lamp voltage is input to the error comparator (Error Comp.) . This allows for the setting of the soft-start time that does not depend on the output load of the DC/DC converter.

9.4 Discharge Block (Discharge)

It discharges electrical charges stored in a smoothing capacitor at output stop. When the CTL pin (Pin 8) is set to the "L" level, the OUT-1 pin (Pin 20) and the OUT-2 pin (Pin 15) are set to the "L" level and turn on the discharging FET (RON ≈ 16 Ω) which is connected between the VO pin (Pin 23) and GND. When the voltage at the VO pin falls below 0.3 V, the discharging FET is turned off and the IC changes to standby state. The discharge function also operates after the under-voltage protection circuit block (UVP Comp.) is latched or when the over-temperature protection circuit block is in operation.

9.5 ON/OFF Time Generator Block (t_{ON} Generator)

The ON time generator block (t_{ON} Generator, ON ONE-SHOT) has a built-in capacitor for timing setting. When the FSW pin (Pin 13) is connected to GND, ON time that is dependent on the input voltage is generated by connecting a timing setting resistor to the RT pin (Pin 22) .

$$t_{ON} = \frac{V_O}{V_{CC}} \times R_T \times 0.059 + 30$$

t_{ON} : ON time on high-side FET [ns]
R_T : Timing resistor value [Ω]
V_{CC} : Power supply voltage [V]
V_O : Output voltage [V]

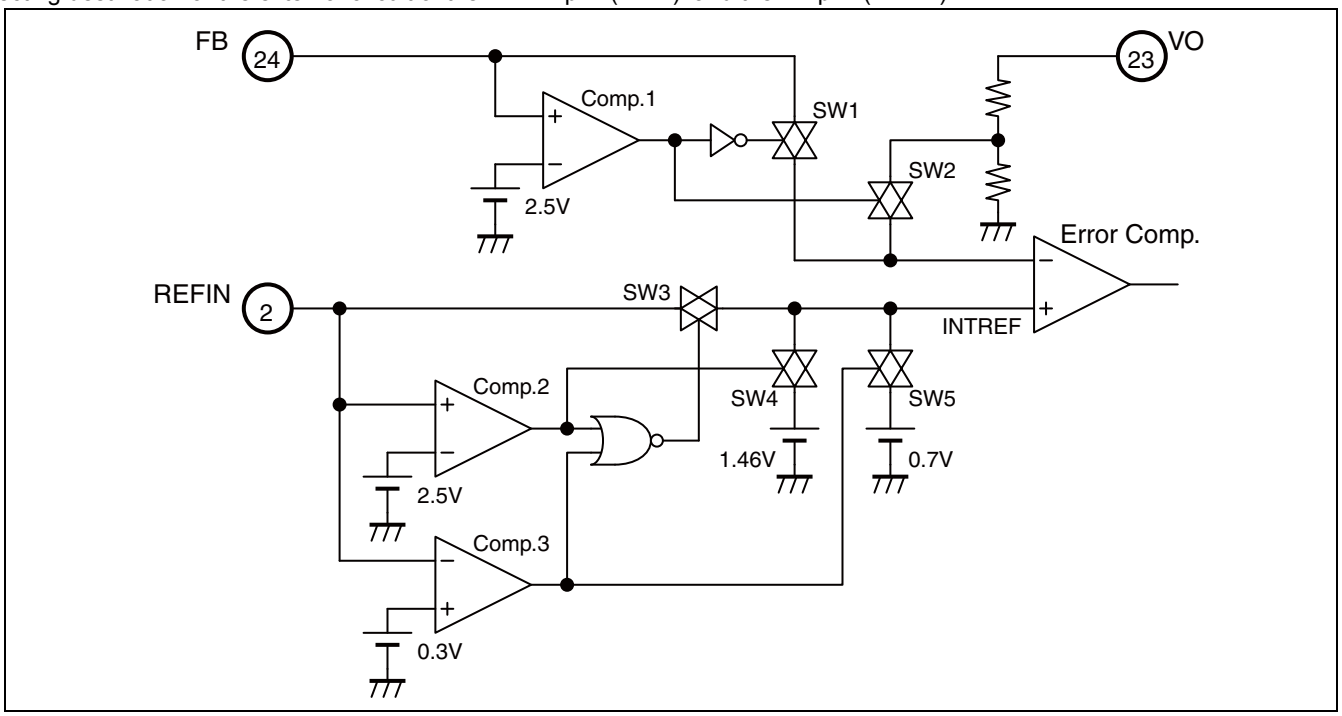
If the V_O1 and V_O2 voltages are 0.1 V or less at soft-start, it is fixed in a value at 0.1V in V_O1 and V_O2 in ON time.
In addition, the FSW pin can be used to switch the ON time setting between the setting by the resistor that is externally connected to the RT pin and the setting by the IC's internal resistor.
The OFF time generator block (OFF ONE-SHOT) generates 480[ns] (Typ.) as the minimum OFF time.

$$t_{OFF} = \left(\frac{V_{CC}}{V_O} - 1 \right) \times t_{ON}$$

t_{ON} : ON time on high-side FET [ns]
V_{CC} : Power supply voltage [V]
V_O : Output voltage [V]

9.6 Output Voltage Setting Block (VO REFIN Control, Error Comp.)

The output voltage setting block (VO REFIN Control, Error Comp.) supports the setting of various output voltages according to connecting destination or the external circuit of the REFIN pin (Pin 2) and the FB pin (Pin 24) .



Output Voltage Setting Table

REFIN	FB	SW state	INTREF (Internal Reference Voltage)	Remarks
GND	VB	SW2,5:ON, SW1,3,4:OFF	0.7 V (Typ.)	VO = 1.2 V set (internal setting)
VB	VB	SW2,4:ON, SW1,3,5:OFF	1.46 V (Typ.)	VO = 2.5 V set (internal setting)
GND	0.7 V	SW1,5:ON, SW2,3,4:OFF	0.7 V (Typ.)	Internal reference voltage fixed to 0.7 V, output voltage setting discretionary by external resistor value ratio between VO-FB and between FB-GND
VB	1.457 V	SW1,4:ON, SW2,3,5:OFF	1.457 V (Typ.)	Internal reference voltage fixed to 1.457 V, output voltage setting discretionary by external resistor value ratio between VO-FB and between FB-GND
0.5 V to 2.2 V	VB	SW2,3:ON, SW1,4,5:OFF	= REFIN pin voltage	The reference voltage can be discretionary set by the external resistor value ratio between VREF-REFIN and between REFIN-GND, and the built-in feedback resistor for the output setting is used.

Error Comp. detects the end timing of the OFF period by comparing the non-inverting input and inverting input. In other words, it detects that the output voltage has fallen below the output setting voltage, and puts the output in ON state. In this case, the delay time is 100 ns (Typ.) .

9.7 Current Detection Block (Current Sense)

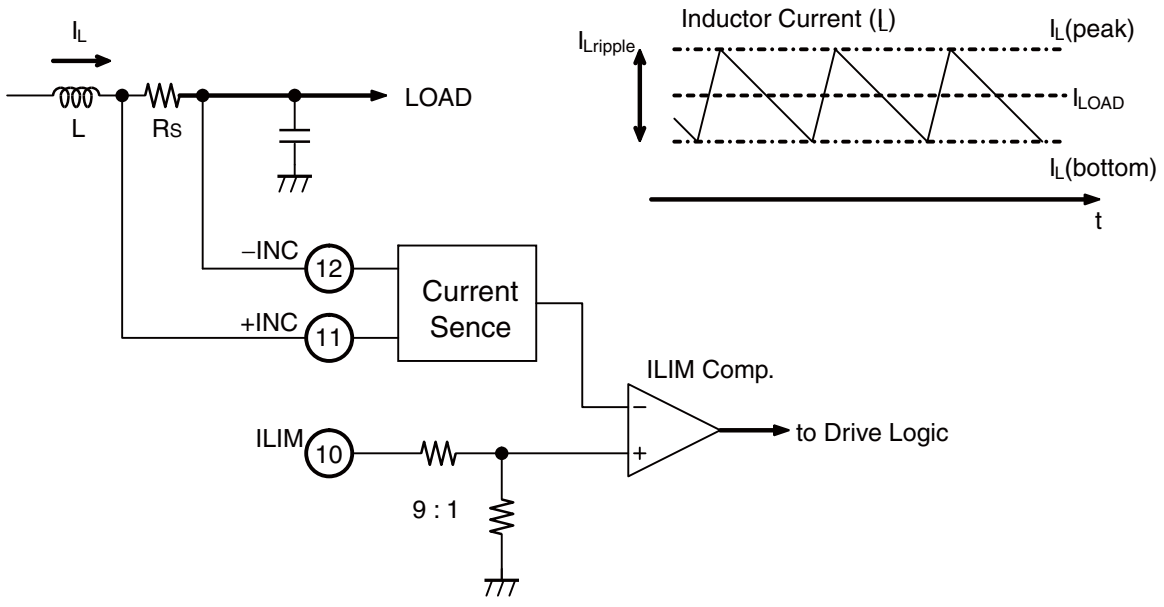
This circuit is used to detect a inductor current (I_L) . The current detection block (Current Sense) converts a voltage waveform between the +INC pin (Pin 11) and the -INC pin (Pin 12) into the GND-standard voltage waveform. Therefore, it can detect a ripple current of the inductor by the current sense resistor R_S connected between the +INC and -INC pins.

9.8 Over Current Detection Block (ILIM Comp.)

Comparing the current value of the current sense resistor and the setting value of over current detection starts the over current protection operation. The over current detection block (ILIM Comp.) compares the output voltage waveform in the current detection block and the over current detection level which is 1/10 of the voltage externally set to the ILIM pin (Pin 10). The over current detection block detects the bottom value of the ripple current which flows into the inductor. The OFF state has been kept until the output voltage waveform in the current detection block goes down below the over current detection level, and the ON state of the high-side FET is permitted when the waveform goes down below the level. This is the protection operation against the over current. The protection operation is the operation which drops the output voltage.

Moreover, the over current detection level can be set to a fixed value (50 mV Typ.) by applying 3.8 V (Typ.) or more voltage to the ILIM pin.

- Current detection block / Over current detection block



Rs : Current sense resistor

9.9 Inductor Saturation Detection Block (LSAT Comp.)

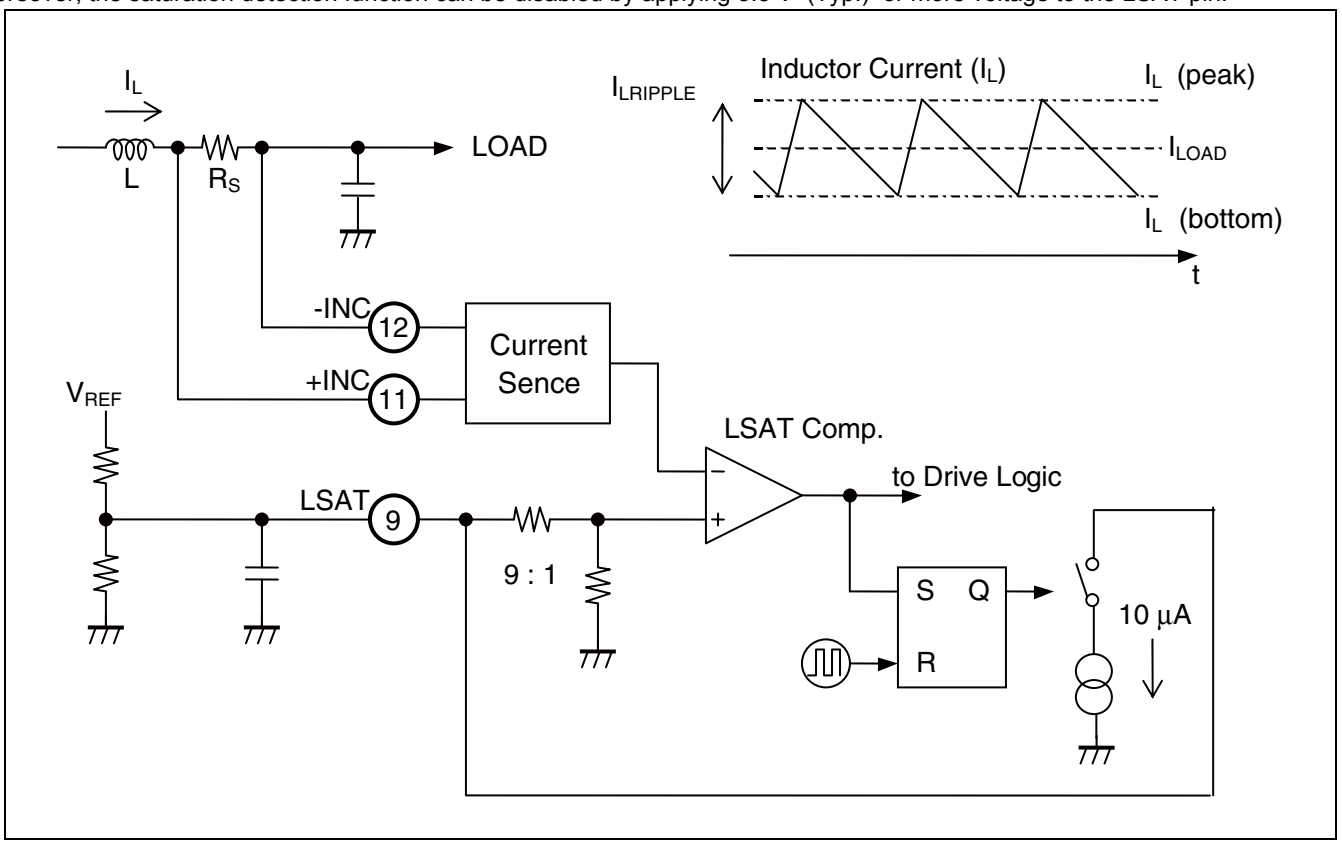
As an auxiliary function for over current protection, this circuit prevents the occurrence of excessive currents due to magnetic saturation of the inductor.

The inductor saturation detection block (LSAT Comp.) compares the output voltage waveform of the current detection block (Current Sense) with 1/10 of the saturation detection level of the voltage externally set to the LSAT pin (Pin 9) and detects the peak value of the ripple current that flows to the inductor.

During the ON period of high-side FET, the output voltage waveform of the current detection block exceeds the saturation detection level, immediately after it detected that it sets an OFF-state. Simultaneously, it also sets an SR latch in LSAT Comp. and sinks 10 µA (Typ.) of a constant current from the LSAT pin. This SR latch is reset in every cycle and the same operation is repeated. The saturation detection level goes down by sinking the electric charge of the capacitor connected to the LSAT pin in every cycle.

Depending on the external parts or use conditions, the ILIM and LSAT pins must be set to various voltages; therefore, the detection level can be set freely by the external resistor value ratio.

Moreover, the saturation detection function can be disabled by applying 3.8 V (Typ.) or more voltage to the LSAT pin.



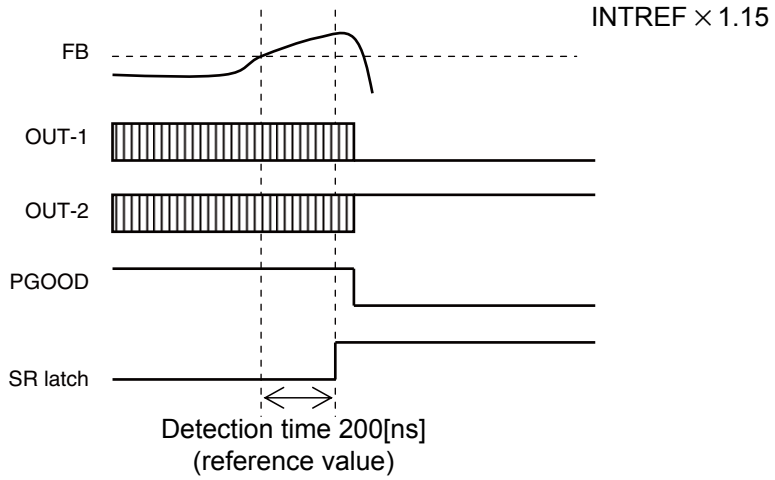
9.10 Over-voltage Protection Circuit Block (OVP Comp.)

The circuit protects an output connecting device when the output voltage (V_O) rises.
This function is that 1.15 times (Typ.) of the internal reference voltage (INTREF) that is set by the output voltage setting block (VO REFIN Control) is compared with the voltage that is inverting-input into Error Comp. If the thing that the inverting-input-voltage into Error Comp. has gone up is detected, an SR latch is set, each pin's logic is fixed as described in “Function table when the over-voltage protection circuit block is in operation”, and the voltage output is stopped.

- Function table when the over-voltage protection circuit block is in operation

OUT-1	OUT-2	CS	PGOOD
L (High-side FET : OFF)	H (Low-side FET : ON)	L	L

- Timing chart example for over-voltage protection operation (PGOOD pulled up to VB)



The over-voltage protection state can be cancelled by setting the IC to standby state first and then resetting the latch using the UVLO signal. Also, the over-voltage protection function can be disabled by causing a short between the COVP pin (Pin 5) and the GND pin (Pin 1).

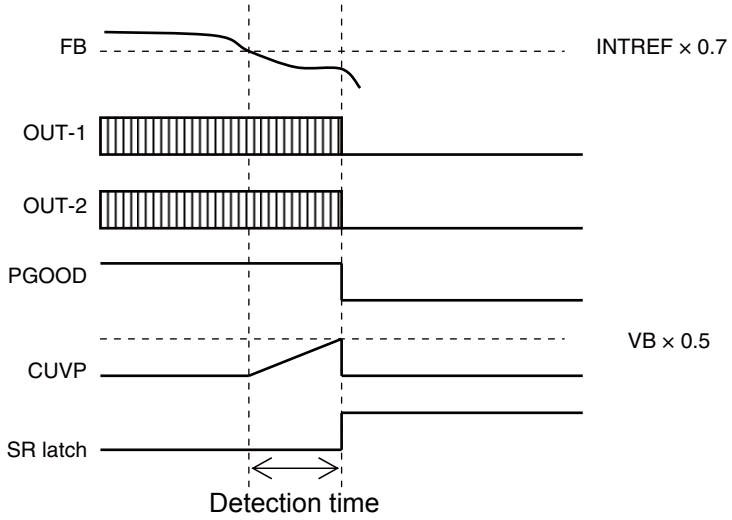
9.11 Under-voltage Protection Circuit Block (UVP Comp.)

It protects an output connecting device by stopping the output when the output voltage (V_O) drops.
This function is that 0.7 times (Typ.) of the internal reference voltage (INTREF) that is set by the output voltage setting block (VO REFIN Control) is compared with the voltage that is inverting-input into Error Comp. If the thing that the inverting input-voltage into Error Comp. has dropped is detected, the capacitor connected to the CUVP pin (Pin 6) starts charging.
When the voltage at the CUVP pin rises and an SR latch is set in UVP Comp., the PGOOD pin (Pin 7) is set to the "L" level and discharge operation is performed to stop the voltage output.

- Function table when the under-voltage protection circuit block is in operation

OUT-1	OUT-2	CS	PGOOD
L (High-side FET : OFF)	L (Low-side FET : OFF)	L	L

- Timing chart example for under-voltage protection operation (PGOOD pulled up to VB)

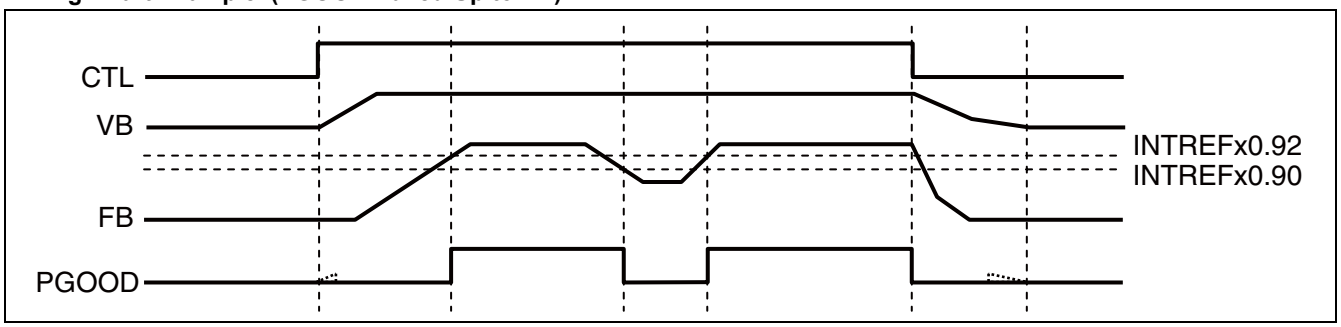


The under-voltage protection state can be cancelled by setting the IC to standby state first and then resetting the latch using the UVLO signal.
Also, the under-voltage protection function can be disabled by causing a short between the CUVP pin and the GND pin (Pin 1).

9.12 Power-Good Detection Circuit Block (PGOOD Comp.)

This function is that 0.9 times (Typ.) of the internal reference voltage (INTREF) that is set by the output voltage setting block (VO REFIN Control) is compared with the voltage that is inverting-input into Error Comp. If the thing that the inverting-input voltage into Error Comp. has raised is detected, it determines that the output voltage of the DC/DC converter has reached the setting voltage and turns off N-ch MOS which are built into the PGOOD pin (Pin 7) .

Timing Chart Example (PGOOD Pulled Up to VB)



9.13 Output Block (Drv-1, Drv-2)

This circuit drives the external N-ch MOS FET. The output circuit is configured in CMOS type for both the high-side and the low-side.

9.14 Control Block (CTL)

The block changes to standby state, when the CTL pin (Pin 8) is set to the “L” level.

(The maximum power-supply current at standby is 10 μA.)

Setting the CTL pin to the “H” level can send the DC/DC converter block into operating state.

Control Function Table

CTL	DC/DC converter
L	OFF
H	ON

9.15 Bias Voltage Block (VB Reg.)

It outputs 5 V as the power supply to the internal control circuit and for setting the bootstrap voltage.

Moreover, it can switch the 5 V power supply to external (VBIN) from internal (VB Reg.). By inputting the voltage of 4.5 V (Typ.) or more to the VBIN pin (Pin 18) from outside.

9.16 Over temperature Protection Circuit Block (OTP)

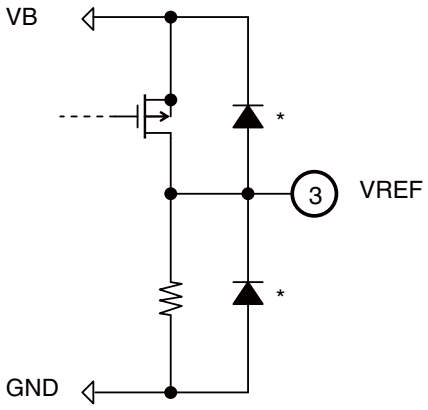
The circuit protects an IC from heat-destruction. If the junction temperature reaches + 150°C, the over temperature protection circuit sets the CS pin (Pin 4) to the “L” level, the OUT-1 pin (Pin 20) and the OUT-2 pin (Pin 15) to the “L” level, and turns on the discharge FET (RON ≈ 16 Ω) which is connected between the VO pin (Pin 23) and GND. In addition, if the junction temperature drops to + 125°C, the normal operation restarts. The condition for the over temperature protection function to operate is that the maximum rating of this IC is exceeded. Therefore, make sure to design the DC/DC power supply system so that the over temperature protection does not start frequently.

10. Protection Function Table

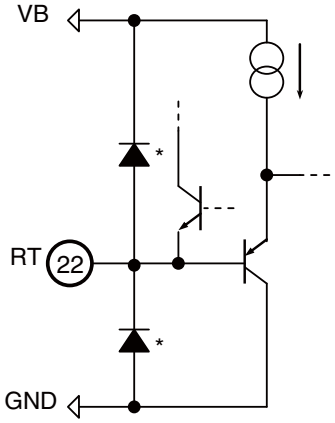
Control/ protection function	Detection condition	Output of each pin after detection				DC/DC output dropping operation, etc.
		VREF	VB	OUT-1	OUT-2	
Under Voltage Lock Out (UVLO)	VB < 3.3 V VREF < 1.8 V	< 1.8 V	< 3.3 V	L	L	Self-discharge by load
Under Voltage Protection (UVP)	FB < INTREF × 0.7 Equivalent to less than VO× 0.7	2.5 V	5 V	L	L	Discharge by IC discharge function Discharge stopped at VO ≤ 0.3 V
Over Voltage Protection (OVP)	FB > INTREF × 1.15 Equivalent to VO×1.15 or more	2.5 V	5 V	L	H	VO = 0 V clamping
Over Current Protection (ILIM)	+INC to −INC > ILIM Equivalent to over current detection value	2.5 V	5 V	switching	switching	Dropping by constant current (Output drops but does not stop)
Over Temperature Protection (OTP)	Tj > + 150°C	2.5 V	5 V	L	L	Discharge by IC discharge function Discharge stopped at VO ≤ 0.3 V
CONTROL (CTL)	CTL: H → L (VO > 0.3 V)	2.5 V	5 V	L	L	Discharge by IC discharge function VREF = 0 V, VB = 0 V, and discharge stopped at VO ≤ 0.3 V

11. I/O Pin Equivalent Circuit Diagram

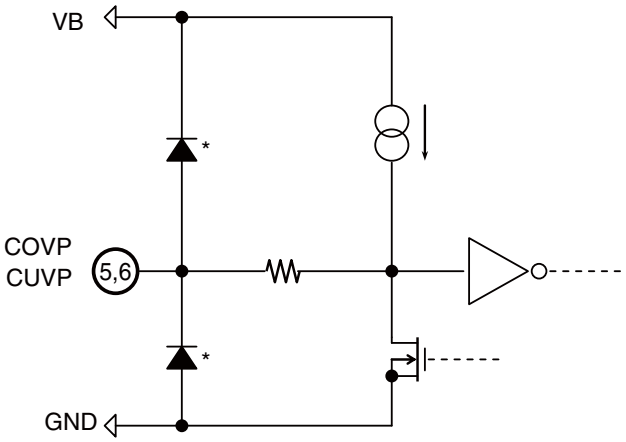
<<Reference voltage block>>



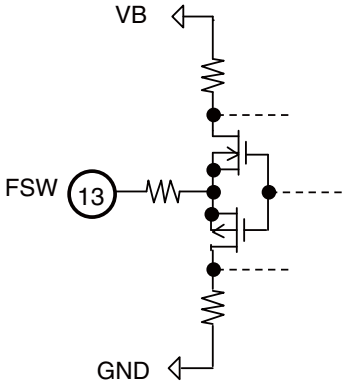
<<ON/OFF time generator block>>



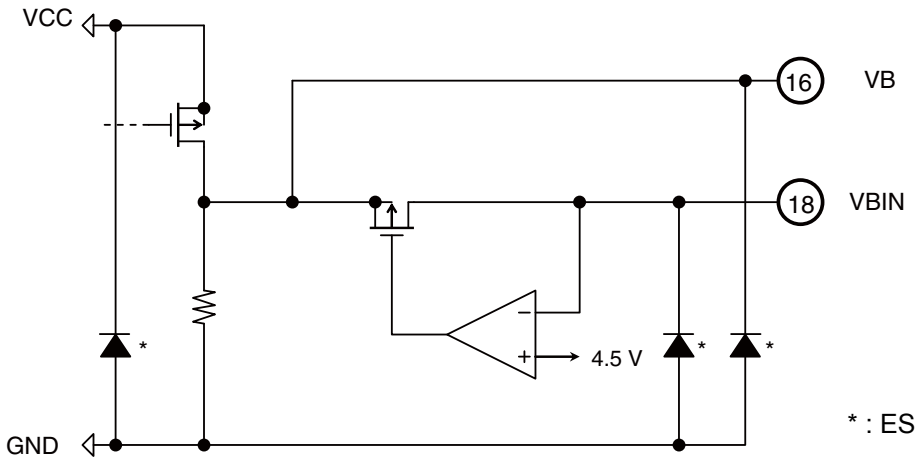
<<Over voltage protection block>>
<<Under voltage protection block>>



<<ON/OFF time generator block>>

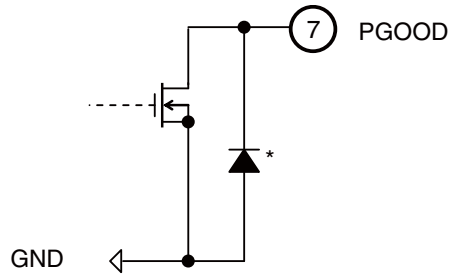


<<Bias voltage block>>

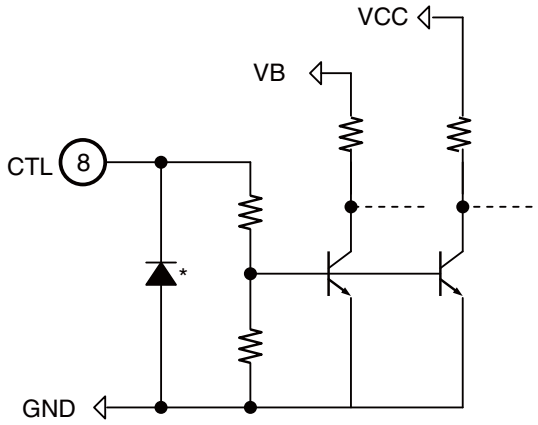


* : ESD protection element

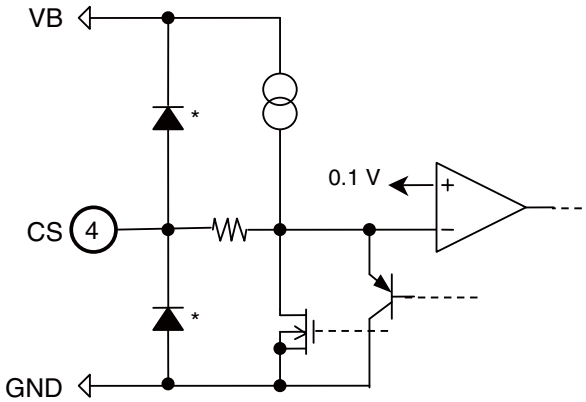
<<Power-Good detection block>>



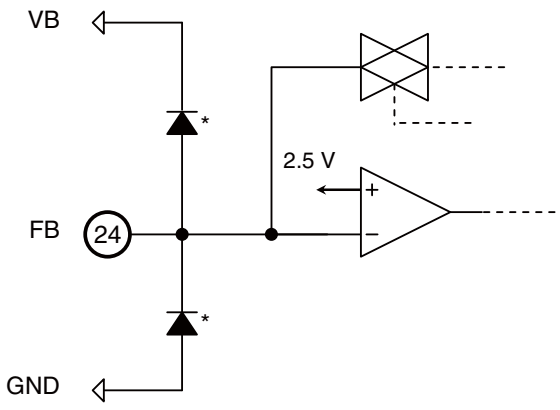
<<Control block>>



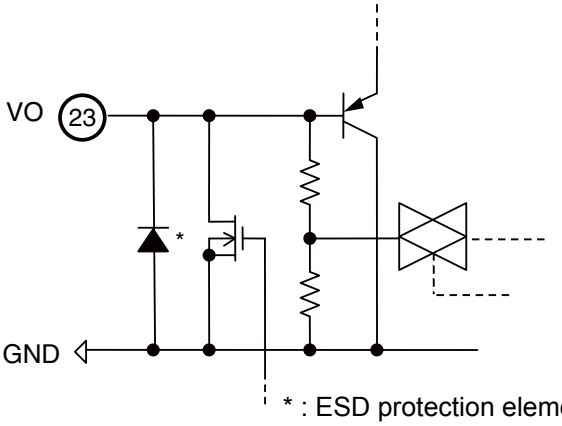
<<Soft-start block>>



<<Output voltage setting block (FB) >>

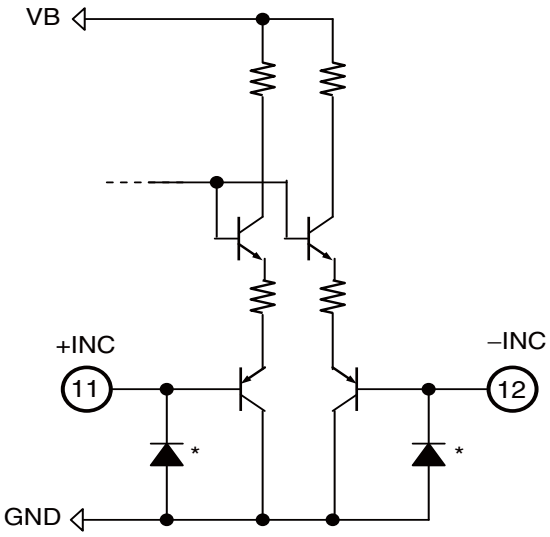


<<Output voltage setting block (VO) >>

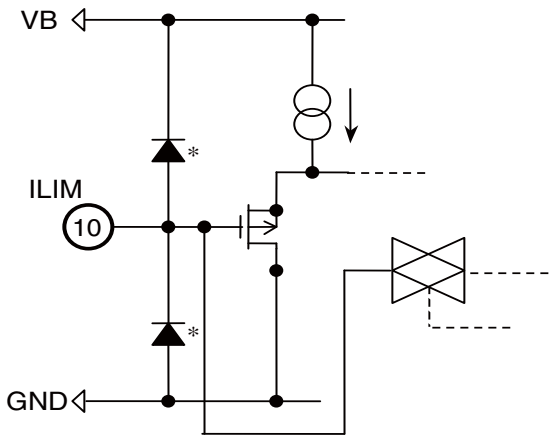


* : ESD protection element

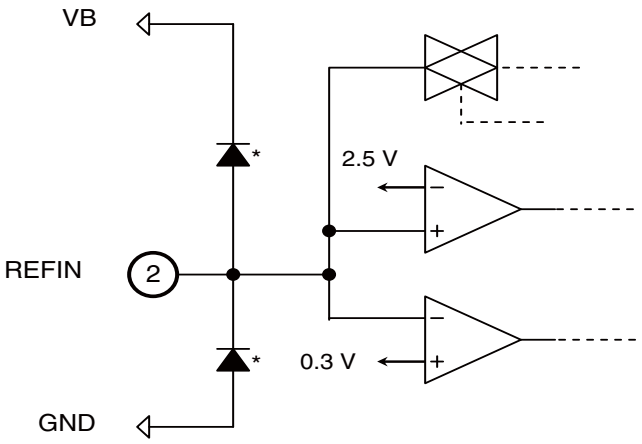
<Charge current setting block>



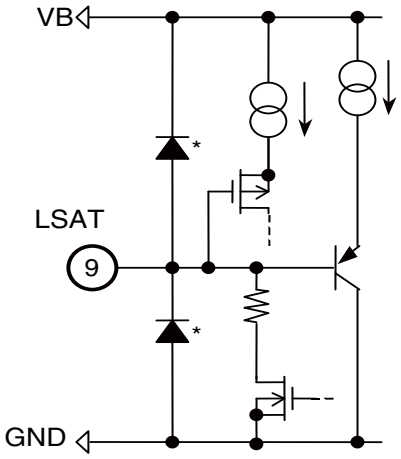
<Over current detection block>



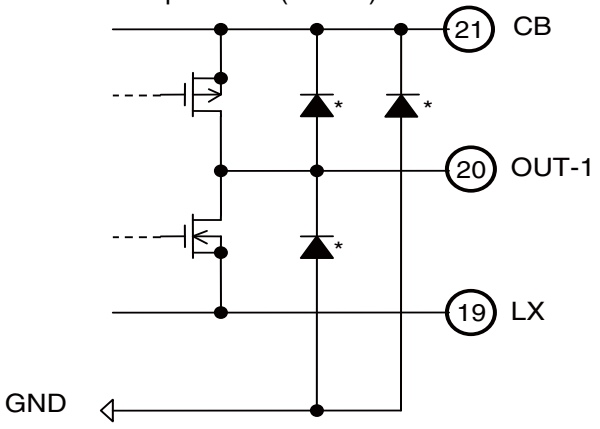
<<Output voltage setting block (REFIN)>>



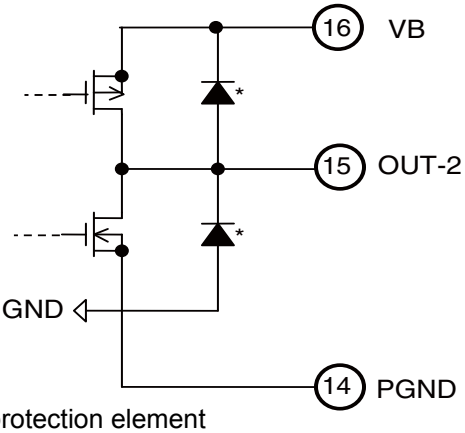
<<Oversaturation detection block>>



<<Output block (OUT-1)>>

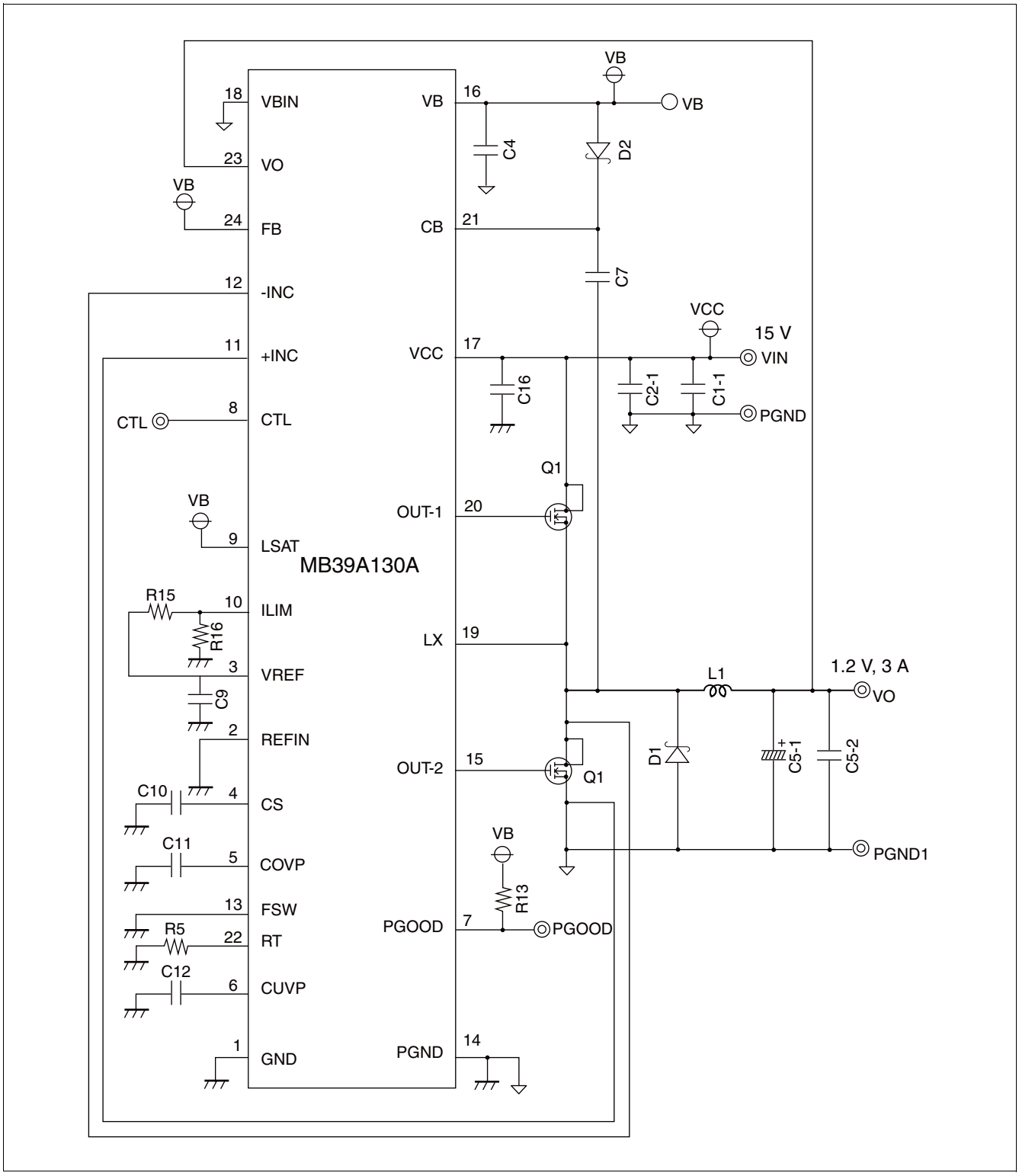


<<Output block (OUT-2)>>



*: ESD protection element

12. Example Application Circuit



13. Parts List

Component	Item	Specification	Vendor	Package	Part Number	Remarks
Q1	N-ch FET	VDS = 30 V, ID = 8 A, Ron = 21 mΩ	RENESAS	SO-8	μPA2755	Dual type (2 elements)
D1	Diode	Io = 1A, VRRM = 40 V, VF = 0.55 V at IF = 1A	ON semi	SOD-123FL	MBR140SFT1	
D2	Diode	VF = 0.4 V (Max) at IF = 0.2 A	ON semi	SOD-523	BAT54XV2T1G	
L1	Inductor	2.2 μH (10 mΩ, 6.1 A)	TDK	—	RLF7030T-2R2M5R4	
C1-1	Ceramic capacitor	22 μF (25 V)	TDK	3225	C3225JC1E226M	
C1-2	Ceramic capacitor	22 μF (25 V)	TDK	3225	C3225JC1E226M	
C4	Ceramic capacitor	4.7 μF (6.3 V)	TDK	1608	C1608JB0J475M	
C5-1	POSCAP	220 μF (4 V, 40 mΩ)	SANYO	D	4TPC220M	
C5-2	Ceramic capacitor	1000 pF (50 V)	TDK	1608	C1608CH1H102J	
C7	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C9	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C10	Ceramic capacitor	0.022 μF (25 V)	TDK	1608	C1608JB1H223K	
C11	Ceramic capacitor	470 pF (50 V)	TDK	1608	C1608CH1H471J	
C12	Ceramic capacitor	470 pF (50 V)	TDK	1608	C1608CH1H471J	
C13	Ceramic capacitor	470 pF (50 V)	TDK	1608	C1608CH1H471J	
C16	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
R5	Resistor	43 kΩ	SSM	1608	RR0816P433D	
R13	Resistor	100 kΩ	SSM	1608	RR0816P104D	
R14	Resistor	56 kΩ	SSM	1608	RR0816P563D	
R15	Resistor	43 kΩ	SSM	1608	RR0816P433D	
R16	Resistor	22 kΩ	SSM	1608	RR0816P223D	

RENESAS : Renesas Electronics Corporation
ON semi : ON Semiconductor
SANYO : SANYO Electric Co., Ltd.
TDK : TDK Corporation
SSM : SUSUMU Co.,Ltd.

14. Application Note

[1] Setting Operating Conditions

Setting output voltages

1. When the Output Setting Voltages (V_O) are 1.2 V and 2.5 V:

They can be set by the internal preset function. In this case, the smallest number of parts is required for the setting, as it is not necessary to apply a reference voltage externally or use a resistor to set the output voltage.

REFIN Pin	FB Pin	Output Voltage Setting Value (V_O)
GND	VB	V_O = 1.2 V
VB	VB	V_O = 2.5 V

VB: Power supply voltage of control system (VB voltage)

2. When the Output Setting Voltages (V_O) are Other than 1.2 V and 2.5 V:

They can be set by fixing the reference voltage of Error Comp. to 0.7 V and adjusting the output voltage setting resistor value ratio.

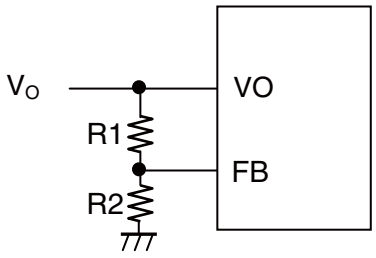
For setting $V_O \geq 1.5$ V, use it with REFIN = VB.

REFIN Pin	FB Pin	Output Voltage Setting Value (V_O)
GND	Output setting voltage setting resistor connected	$V_O = \frac{R1 + R2}{R2} \times 0.7 + \frac{\Delta V_O}{2}$
VB	Output setting voltage setting resistor connected	$V_O = \frac{R1 + R2}{R2} \times 1.457 + \frac{\Delta V_O}{2}$

The output ripple voltage value is calculated by the following formula.

$$\Delta V_O = ESR \times \frac{V_{IN} - V_O}{L} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

ΔV_O : Output ripple voltage [V]
L : Coil inductor value [H]
V_{IN} : Power supply voltage [V]
V_O : Output setting voltage [V]
f_{OSC} : Oscillation frequency [Hz]



3. When Setting/Changing the Output Setting Voltage Dynamically:

The output voltage can be set / changed dynamically by changing the REFIN voltage (V_{REFIN}) under the following condition.

The output voltage setting value can be set within the range from 0.855 V to 3.762 V.

VB: Power supply voltage of control system (VB voltage)

REFIN Pin	FB Pin	Output Voltage Setting Value (V_O)
Following voltage applied externally (0.5 to 2.2 V)	VB	$V_O = 1.71 \times V_{REFIN}$

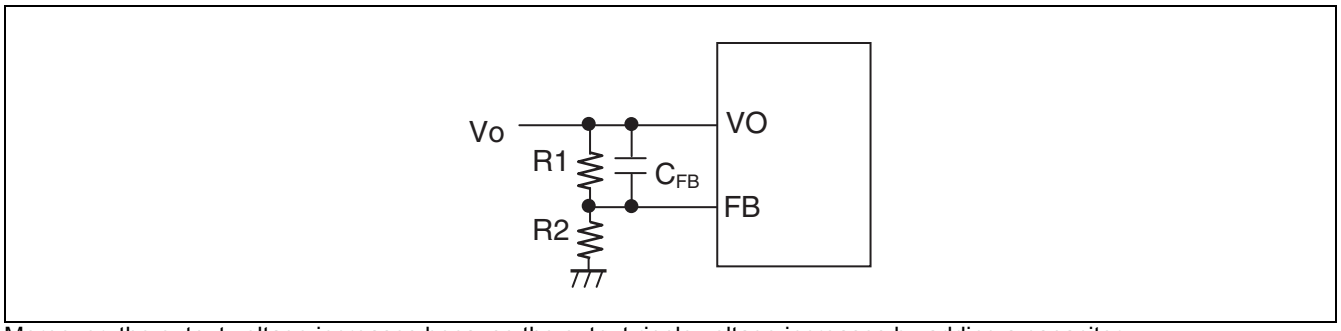
Note When the output voltage set as mentioned above the method 2 or 3, select a resistor value that achieves R1//R2 ≤ 50 [kΩ] as a target.

In output voltage setting method 2 or 3, the oscillation frequency may become unstable, if the output voltage setting resistor value ratio (R1/R2) is high. This occurs because the value of the ripple voltage applied to the FB pin is reduced by the R1/R2 ratio. In this case, a stable oscillation frequency can be achieved by increasing the output ripple voltage or adding a capacitor in parallel to R1.

Select an additional capacitor using the following formula as a guide.

$$C_{FB} \geq \frac{10 \times (R1 + R2)}{2\pi \times f_{OSC} \times R1 \times R2}$$

C_{FB} : Feedback capacitor [F]
R1,R2 : Output voltage setting resistor value [Ω]
f_{OSC} : Oscillation frequency [Hz]

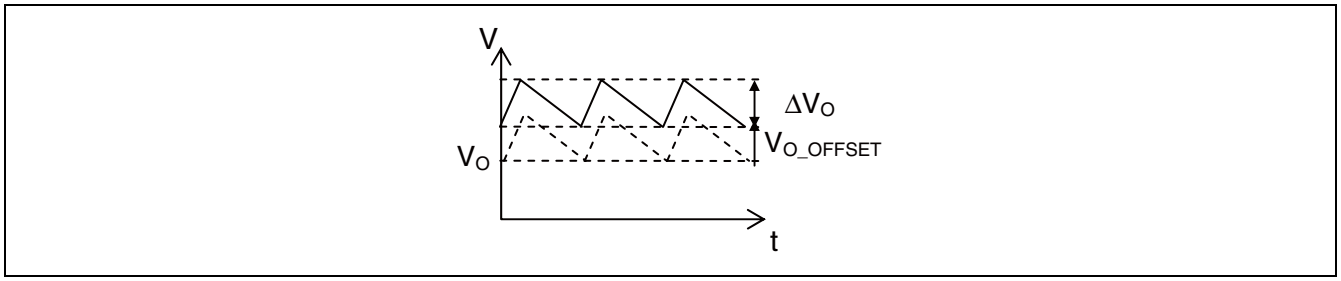


Moreover, the output voltage increases because the output ripple voltage increases by adding a capacitor.

The following formula is used to calculate the output voltage increase. If it is required to adjust the output voltage, change the output voltage setting resistor value.

$$V_{O\_OFFSET} = \frac{(V_O - INTREF) \times \Delta V_O}{2 \times INTREF}$$

V_{O_OFFSET} : Output setting voltage offset value [V]
V_O : Output setting voltage [V]
ΔV_O : Output ripple voltage [V]
INTREF : Error Comp. reference voltage [V]
(For details, see “ Output Voltage Setting Table” in “ Function”) .



Consideration of output ripple voltage

This device requires an output ripple voltage as an operating principle. It must secure about 20 mV at the FB pin voltage. Calculate the output ripple voltage required for the output of the DC/DC converter by the following formula.

$$\Delta V_O \geq K \times 20\ mV$$

ΔV_O : Output ripple voltage [V]

K : Coefficient: When CFB is used: K = 1; When C_{FB} is not used : K = $\frac{V_O}{INTREF}$

V_O : Output setting voltage [V]

INTREF : Error Comp. reference voltage [V]
(For details, see “ Output Voltage Setting Table” in “ Function”) .

A stable oscillation frequency can be achieved by increasing the output ripple voltage.

The output ripple voltage can be increased by selecting a larger output capacitor ESR or a smaller inductor value.

However, if the output ripple voltage is increased excessively, the slope of the output ripple voltage during the off-period becomes steeper, which affects the bottom detection voltage more. As a result, it affects the output voltage. This become prominent, if it increase on-duty or oscillation frequency. Ensure that the ripple voltage at the FB pin is not excessively large.

Setting oscillation frequency

The operating frequency can be set as shown in the following table, according to the state of the RT and FSW pins.

RT	FSW	Operating Frequency
Connect resistor (R_{RT}) between RT and GND	GND	Frequency set by the following R_{RT} formula*
GND	VREF	(≈ 300 kHz)
GND	VB	(≈ 550 kHz)

* :

$$R_{RT} = \frac{\left(\frac{10^9}{f_{OSC}} - \frac{V_{CC} \times 30}{V_O}\right)}{0.059} \qquad 20 \times 10^3 \leq R_{RT} \leq 160 \times 10^3$$

R_{RT} : Timing resistor value [Ω]
V_{CC} : Power supply voltage (V_{IN}) [V]
V_O : Output setting voltage [V]
f_{OSC} : Oscillation frequency [Hz]

Note: Set the oscillation frequency so that the on-time (t_{ON}) is more than 100 ns and the off-time (t_{OFF}) is more than the minimum off-time. (For how to calculate the on-time and the off-time, see " (9.5) ON/OFF Time Generator Block" in " Function". For the minimum off-time, see " ON/OFF Time Generator Block [t_{ON} Generator]" in " Electrical Characteristics".)

Setting over voltage protection function/under voltage protection function

For each function, the timer can be set for the time until it stops. Calculate each setting capacitor value by the following formula.

$$C_{OVP} = \frac{11 \times t_{OVP}}{VB}$$

C_{OVP} : OVP pin capacitor value [pF]
t_{OVP} : Over voltage detection time [µs]
VB : VB power supply voltage [V]

$$C_{UVP} = \frac{11 \times t_{UVP}}{VB}$$

C_{UVP} : UVP pin capacitor value [pF]
t_{UVP} : Under voltage detection time [µs]
VB : VB power supply voltage [V]

Connect the COVP pin to GND when not using the over-voltage protection function.
Connect the CUVP pin to GND when not using the under-voltage protection function.

Setting over current protection function / oversaturation protection function

Over current protection function	Used to limit load current. Output voltage drops to limit the over-current flowing. When the over-current status is finished, the output voltage gets back to the normal setting value. (If the latch function is required to stop the output, it is realized to be used together with the under voltage protection function.)
Oversaturation protection function	Use this function if there is a concern about saturation of the inductor (a decrease in inductance) due to inductor current that flows when the above over current is detected. This function is not required when a inductor with a sufficient amount of current is used. Output voltage drops to limit the over-current flowing. When the over-current status is finished, the output voltage gets back to the normal setting value. (If the latch function is required to stop the output, it is realized to be used together with the under voltage protection function.)

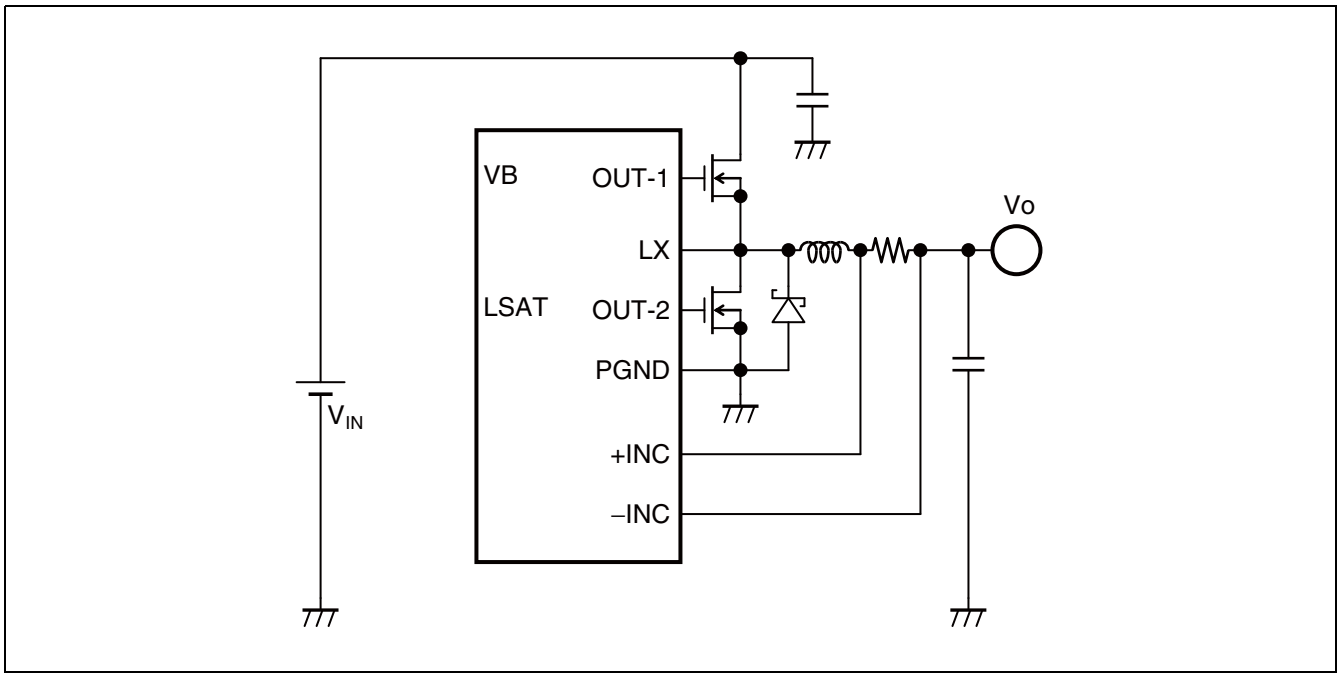
A current sense resistor is connected between the inductor and output, when using the over current protection/oversaturation protection function. Since the input limit of +INC is 2.9 V, the following conditions must be met.

$$2.9 \geq \left(I_{LIM} + \frac{\Delta IL}{2} \right) \times R_S + V_O$$

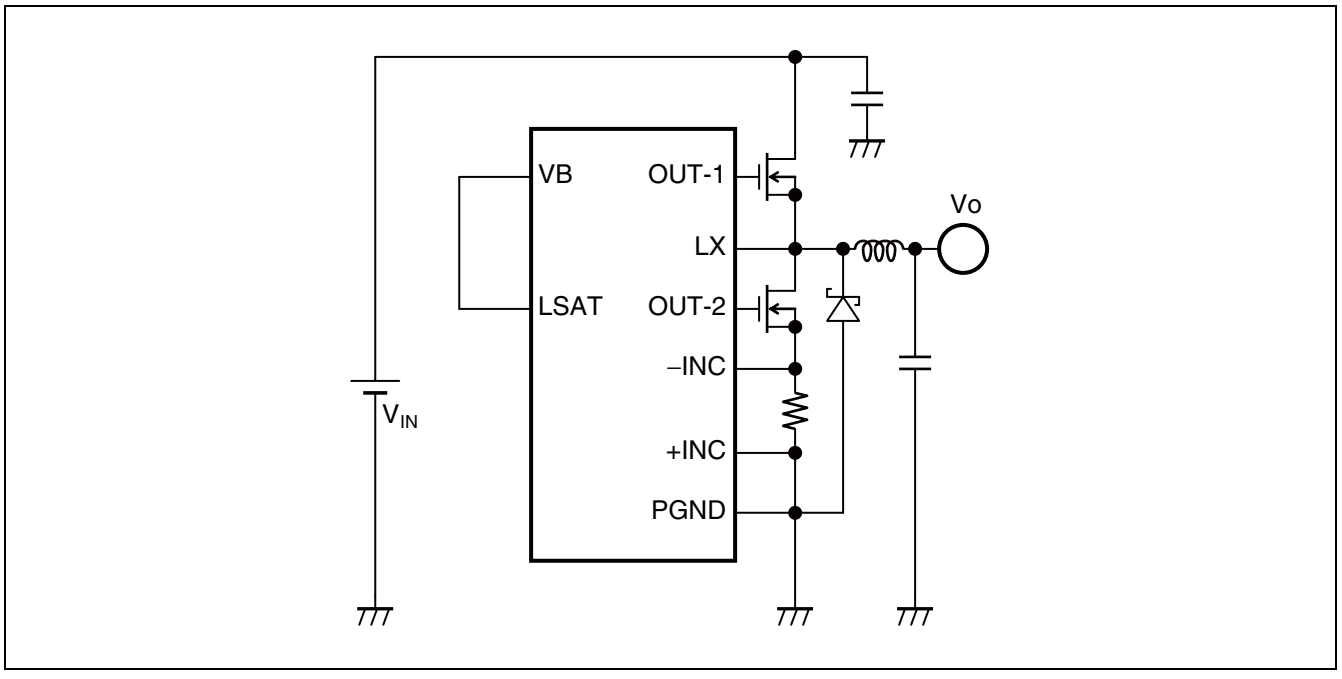
ΔIL : Ripple current peak-to-peak value of inductor [A]
V_O : Output setting voltage [V]
I_{LIM} : Over current detection value [A]
R_S : Current sense resistor value [Ω]

$$\Delta IL = \frac{V_{IN} - V_O}{L} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

L : Inductor value [H]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
f_{OSC} : Oscillation frequency [Hz]



If the voltage at the +INC pin exceeds 2.9 V due to the output voltage setting value, connect a current sense resistor between GND and the source of the low-side FET.



The oversaturation protection function cannot be used in this connecting arrangement. Connect the LSAT pin to the VB pin. Also, it is necessary to confirm that the voltage between LX and GND when the low-side FET is turned on is smaller than the forward voltage of the fly-back diode. Calculate the voltage between LX and GND by the following formula.

$$V_{LX} = \left(I_{LIM} + \frac{\Delta IL}{2} \right) \times \left(R_S + R_{ON} \right)$$

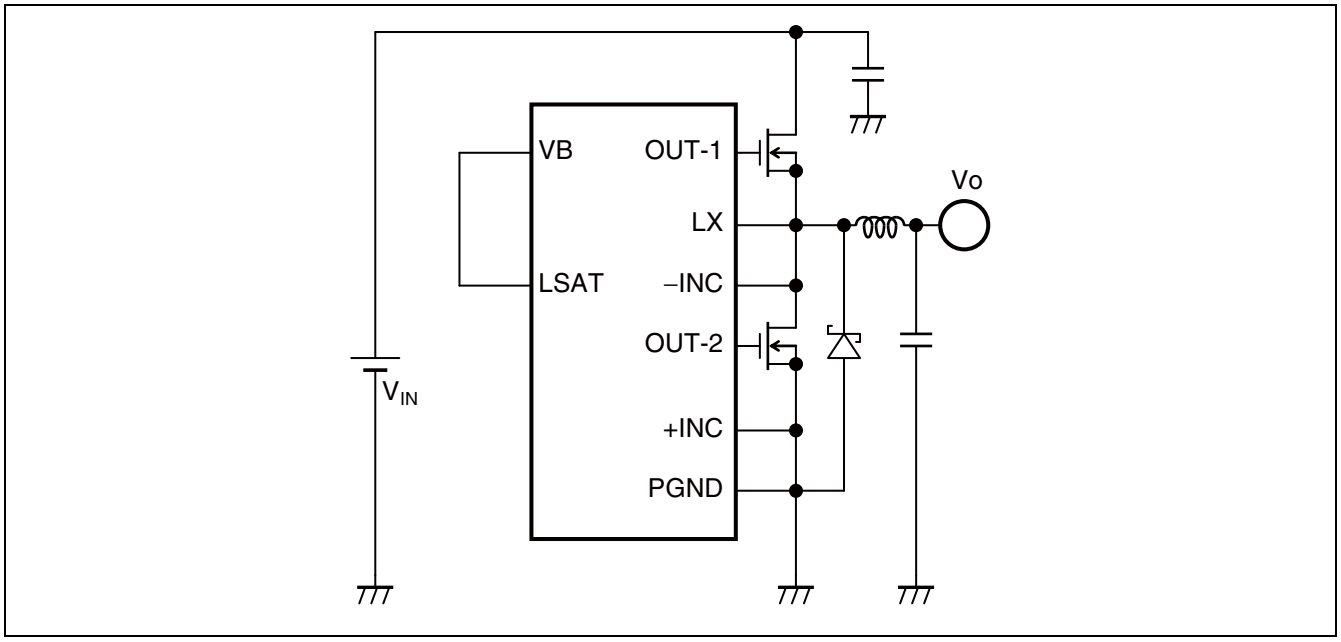
V_{LX} : Voltage between LX and GND
ΔIL : Ripple current peak-to-peak value of inductor [A]
I_{LIM} : Over current detection value [A]
R_S : Current sense resistor value [Ω]
R_{ON} : Low-side FET on-resistance [Ω]

It is also necessary to confirm that the minimum voltage at the -INC pin is -0.3[V] or more. Calculate the -INC pin voltage by the following formula.

$$V_{-INC\_MIN} = -\left(I_{LIM} + \frac{\Delta IL}{2} \right) \times R_S$$

V_{-INC_MIN} : –INC minimum voltage
ΔIL : Ripple current peak-to-peak value of inductor [A]
I_{LIM} : Over current detection value [A]
R_S : Current sense resistor value [Ω]

The on-resistance of the low-side FET can be used to detect over-current conditions by connecting the +INC pin and the –INC pin to the low-side FET drain and source.



Since this connection arrangement does not require a current sense resistor, it is cost-effective. It is also advantageous in conversion efficiency, as there is no loss related to a current sense resistor. However, as the over current detection value (I_{LIM}) is affected by fluctuation / variation in the on-resistance of the low-side FET, enough margin must be secured for the maximum load current (I_{OMAX}) . When calculating the over current detection value, replace the current sense resistor value (R_S) with the on-resistance of the low-side FET (R_{ON}) .
In addition, the oversaturation protection function cannot be used. Connect the LSAT pin to the VB pin.

(1) When using oversaturation protection function and over current protection function

Calculate each setting resistor value of the over-current detection value (I_{LIM}) and the oversaturation detection current value (I_{LSAT}) by the following formula.

$$K_{LIM} = 4 \times R_S \times \left(I_{LIM} - \frac{\Delta IL}{2} \right), \quad K_{LIM}' = 4 \times R_S \times \left(I_{LIM}' - \frac{\Delta IL}{2} \right), \quad K_{LSAT} = 4 \times R_S \times \left(I_{LSAT} - \frac{\Delta IL}{2} \right)$$

$$\frac{R3}{R1+R2+R3} = K_{LIM}, \quad \frac{R2+R3}{R1+R2+R3} = K_{LSAT}, \quad \frac{R1+R2+R3}{R3} + \frac{R1 \times 10^{-5} \times K_{LIM}'}{2.5} = K_{LIM}'$$

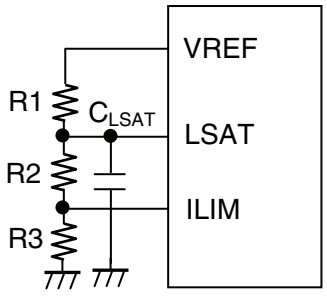
$$100 \times 10^3 \geq R1 + R2 + R3 \geq 30 \times 10^3$$

$$C_{LSAT} \approx \frac{5}{f_{OSC} \times R1 // (R2+R3)}$$

I_{LIM} : Over current detection value [A] ($2 \times I_{OMAX} \geq I_{LIM} \geq 1.5 \times I_{OMAX}$ as target)
I_{LIM}' : Current detection value after oversaturation detection [A]
($I_{LIM}' \approx 1.2 \times I_{OTYP}$ as target)
I_{LSAT} : Oversaturation detection current value [A]

$$\left(I_{LSAT} \geq 1.5 \times I_{LIM} - \frac{2.5 \times \Delta IL}{2} \text{ as target} \right)$$

ΔIL : Ripple current peak-to-peak value of inductor [A]
R_S : Current sense resistor value [Ω]
I_{OMAX} : Maximum load current [A]
C_{LSAT} : LSAT pin connection capacitor value [F]
fosc : Oscillation frequency [Hz]



(2) When only using over current protection function

Connect the LSAT pin to the VB pin to disable the oversaturation protection function.

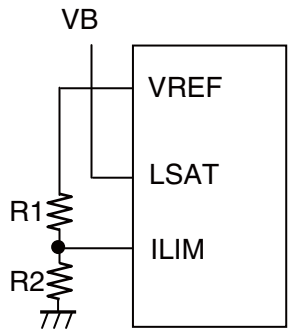
The over current detection value is set using the resistor value connected to the ILIM pin.

Calculate each resistor value by the following formula.

$$R1 = \left(\frac{1}{K_{LIM}} - 1\right) \geq R2,\ K_{LIM} = \frac{4 \geq R_S \geq \left(I_{LIM} - \frac{\Delta IL}{2}\right)}{}$$

$$100 \times 10^3 \geq R1 + R2 \geq 30 \times 10^3$$

I_{LIM} : Over current detection value [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]
R_S : Current sense resistor value [Ω]



When setting the over current detection value internally, connect the ILIM pin to the VB pin.

This setting does not require the resistor to set the over current detection value (I_{LIM}).

Calculate the internally set over current detection value (I_{LIM}) by the following formula.

$$I_{LIM} = \frac{0.05}{R_S} + \frac{\Delta IL}{2}$$

I_{LIM} : Over current detection value [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]
R_S : Current sense resistor value [Ω]

Power dissipation and the thermal design

As for this IC, considerations of the power dissipation and thermal design are not necessary in most cases because of its high efficiency. However, such considerations are necessary for the use at the conditions of a high power supply voltage, a high oscillation frequency, high load, and the high temperature.

Calculate IC internal loss (P_{IC}) by the following formula.

$$P_{IC} = V_{CC} \times (I_{CC} + Qg \times f_{OSC})$$

P_{IC}	: IC internal loss [W]
V_{CC}	: Power supply voltage [V] (V_{IN})
I_{CC}	: Power supply current [A] (2.2 mA Max)
Qg	: Total quantity of charge for all switching FET [C] (Total at Vgs = 5 V)
f_{OSC}	: Oscillation frequency [Hz]

Calculate junction temperature (Tj) by the following formula.

$$Tj = Ta + \theta ja \times P_{IC}$$

Tj	: Junction temperature [°C] (+ 125°C Max)
Ta	: Operation ambient temperature [°C]
θja	: TSSOP-24 Package thermal resistance (+ 76°C/ W)
P_{IC}	: IC internal loss [W]

VB Regulator

In the condition for which the potential difference between VCC and VB is insufficient, the decrease in the voltage of VB happens because of power output on-resistance and load current (mean current of all external FET gate driving current and load current of internal IC) of the VB regulator. Stop the switching operation when the voltage of VB decreases and it reaches threshold voltage (VTHL) of the under voltage lockout protection circuit.

Therefore, set oscillation frequency or external FET or I/O potential difference of the VB regulator using the following formula as a target when you use this IC. When using it in the condition for which the I/O potential difference is insufficient, check the operation on an actual device carefully during normal operation, startup and shutdown.

$$V_{IN} \geq VB\ (V_{THL}) + (Qg \times f_{OSC} + I_{CC}) \times R_{VB}$$

V_{IN}	: Power supply voltage [V]
VB (V_{THL})	: Threshold voltage of under-voltage lockout protection circuit = 3.5 [V] Max
Qg	: Total amount of gate charge of external FET [C]
f_{OSC}	: Oscillation frequency [Hz]
I_{CC}	: Power supply current = 3×10^{-3} [A] (≈ Load current of VB (LDO))
R_{VB}	: Output on-resistance = 100 [Ω] (The reference value at V_{IN} = 4.5 V)

[2] Selection of Parts

Selection of smoothing inductor

As an approximate guide, the inductor value to be selected should be a value which allows the ripple current peak-to-peak value of the inductor to be 50 [%] or less of the maximum load current.

Calculate the inductor value in this case by the following formula.

$$L \geq \frac{V_{IN} - V_O}{LOR \times I_{OMAX}} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

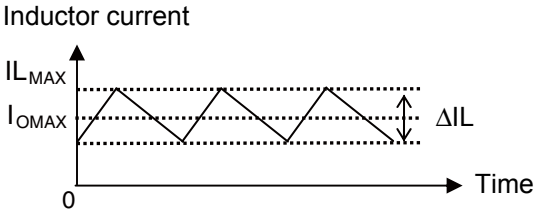
L	: inductor value [H]
I_{OMAX}	: Maximum load current [A]
LOR	: Ratio of inductor ripple current peak-to-peak value and Maximum load current (0.5)
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]

It is necessary to calculate the maximum current value that flows to the inductor to judge whether the electric current that flows to the inductor is a rated value or less. Calculate the maximum current value of the inductor by the following formula.

$$I_{LMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

$$\Delta IL = \frac{V_{IN} - V_O}{L} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

I_{LMAX}	: Maximum current value of inductor [A]
I_{OMAX}	: Maximum load current [A]
ΔIL	: Ripple current peak-to-peak value of inductor [A]
L	: Inductor value [H]
V_{IN}	: Power supply voltage of switching system [V]
Vo	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]



Selection of Switching FET

The maximum value of the current that flows to the switching FET must be calculated in order to determine whether the current flowing to the switching FET is within the rated value. Calculate the maximum value of the current that flows to the switching FET by the following formula.

$$I_D = Io_{MAX} + \frac{\Delta IL}{2}$$

I_D : Drain current [A]
I_{OMAX} : Maximum load current [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]

Moreover, it is necessary to calculate the loss of switching FET to judge whether a power dissipation of switching FET is a rated value or less.
Calculate the conduction loss on the switching FET by the following formula.

High-side FET conduction loss

$$P_{RON} = Io_{MAX}{}^2 \times R_{ON} \times \frac{V_O}{V_{IN}}$$

P_{RON} : High-side FET conduction loss [W]
I_{OMAX} : Maximum load current [A]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
R_{ON} : High-side FET ON resistance [Ω]

Low-side FET conduction loss

$$P_{RON} = Io_{MAX}{}^2 \times R_{ON} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

P_{RON} : Low-side FET conduction loss [W]
I_{OMAX} : Maximum load current [A]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
R_{ON} : Low-side FET on-resistance [Ω]

The gate drive power of switching FET is supplied by LDO in IC, therefore all of the allowable maximum total gate charge (QgTotalMax) of all switching FET is calculated by the following formula.

$$Qg_{TotalMax} \leq \frac{30000}{f_{OSC}}$$

$Qg_{TotalMax}$: Allowable maximum total gate charge of all switching FET [nC]
f_{OSC} : Oscillation frequency [kHz]

Selection of fly-back diode

Select schottky barrier diode (SBD) with the smallest possible forward voltage (Vf) .

In this DC/DC control IC, the period where electric current flows to fly-back diode is limited to synchronous rectification period (50ns×2) as the synchronous rectification method is used. For example, when the oscillation frequency is 600 kHz, the current flow time rate is 6%. Therefore, select a fly-back diode current that does not exceed the forward current surge peak ratings of fly-back diode (I_{FSM}) . Calculate the forward current surge peak ratings of fly-back diode by the following formula.

$$I_{FSM} \geq Io_{MAX} + \frac{\Delta IL}{2}$$

I_{FSM} : Forward current surge peak ratings of SBD [A]
I_{OMAX} : Maximum load current [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]

Note: When the forward voltage (Vf) of schottky barrier diode (SBD) is high and the load current of DC/DC output is large, the output may be stopped due to false detection by the protection function. This problem can be solved by changing to schottky barrier diode (SBD) of a smaller forward voltage.

Selection of output capacitor

A certain level of ESR is required for stable operation of this IC. Use a tantalum capacitor or polymer capacitor as the output capacitor. A ceramic capacitor with low ESR can also be used if a resistor is connected in series with it to increase ESR equivalently.

Calculate the necessary ESR value for the output capacitor by the following formula.

$$ESR \geq \frac{\Delta V_O}{\Delta IL}$$

ESR : Series resistance component of output capacitor [Ω]
ΔV_O : Output ripple voltage [V]
ΔIL : Ripple current peak-to-peak value of inductor [A]

Select the output capacitor value using the following condition as a guide.

$$C_O \geq \frac{1}{4 \times f_{OSC} \times ESR}$$

C_O : Output capacitor value [F]
f_{OSC} : Oscillation frequency [Hz]
ESR : Series resistance component of output capacitor [Ω]

Moreover, the output capacitor value needs to satisfy the following formula too, because of the amount of tolerance limit of output voltage overshoot/undershoot.
The following formula applies when the current through rate for a sudden load change is ∞, which is the worst condition.
For actual through rates are smaller than ∞, the output capacitor value to be used can be smaller than the value calculated by the following formula.

$$C_O \geq \frac{\Delta I_O^2 \times L}{2 \times V_O \times \Delta V_{O\_OVER}} \quad \bullet\bullet\bullet \text{ Overshoot condition}$$

$$C_O \geq \frac{\Delta I_O^2 \times L \times (V_O + V_{IN} \times f_{OSC} \times 480 \times 10^{-9})}{2 \times V_O \times \Delta V_{O\_UNDER} \times (V_{IN} - V_O - V_{IN} \times f_{OSC} \times 480 \times 10^{-9})} \quad \bullet\bullet\bullet \text{ Undershoot condition}$$

C_O : Output capacitor value [F]
ΔV_{O_OVER} : Allowable amount of output voltage overshoot [V]
ΔV_{O_UNDER} : Allowable amount of output voltage undershoot [V]
ΔI_O : Electric current difference in sudden load change [A]
L : Inductor value [H]
V_{IN} : Power supply voltage [V]
V_O : Output setting voltage [V]
f_{OSC} : Oscillation frequency [Hz]

Note: The capacitor has frequency, operating temperature, bias voltage and other characteristics. Therefore, it must be noted that its effective capacitance may be significantly smaller, depending on the use conditions.

Calculate the allowable ripple current of the output capacitor by the following formula.

$$Irms \geq \frac{\Delta IL}{2\sqrt{3}}$$

Irms : Allowable ripple current (effective value) [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]

Selection of input smoothing capacitor

Select the input capacitor with the smallest possible ESR. A ceramic capacitor will be ideal.

Use a polymer capacitor or tantalum capacitor with low ESR, if a ceramic capacitor is not enough and a mass capacitor is required.

Calculate the required capacitor value of the input capacitor using the following formula as a guide.

$$C_{IN} \geq \frac{V_O \times C_O}{V_{IN}}$$

C_{IN} : Input capacitor value [F]
C_O : Output capacitor value [F]
V_O : Output voltage [V]
V_{IN} : Power supply voltage of switching system [V]

A ripple voltage occurs due to the switching operation of DC/DC, if a inductor is connected as a noise filter between the power supply of the switching system and the input capacitor and the cut-off frequency for this inductor and input capacitor is set to a value lower than the oscillation frequency. In this case, consider the lower limit of the input capacitor also in relation to the allowable ripple voltage.

Calculate the ripple voltage of the power supply of the switching system by the following formula.

$$\Delta V_{IN} = \frac{I_{OMAX}}{C_{IN}} \times \frac{V_O}{V_{IN} \times f_{OSC}} + ESR \times \left(I_{OMAX} + \frac{\Delta IL}{2}\right)$$

ΔV_{IN} : Switching system power supply ripple voltage peak-to-peak value [V]
I_{OMAX} : Maximum load current value [A]
C_{IN} : Input capacitor value [F]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
f_{OSC} : Oscillation frequency [Hz]
ESR : Series resistance component of input capacitor [Ω]
ΔIL : Ripple current peak-to-peak value of inductor [A]

Note: The capacitor has frequency, temperature, bias voltage and other characteristics. Therefore, it must be noted that its effective value may be significantly smaller, depending on the use conditions.

The ripple current must be considered when using a capacitor that has a rated value for its allowable ripple current.
Calculate the ripple current by the following formula.

$$Irms \geq I_{OMAX} \times \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}}$$

Irms	: Allowable ripple current (effective value) [A]
I_{OMAX}	: Maximum load current value [A]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]

Current sense resistor
Select a ripple voltage (ΔV_{Rs}) of about 100 mV as a target for the inductor current and the current sense resistor. Calculate the resistor value by the following formula.

$$R_S \geq \frac{\Delta V_{Rs}}{I_{LIM} - \frac{\Delta IL}{2}}$$

Rs	: Current sense resistor value [Ω] (or low-side FET on-resistance (R_{ON}))
ΔV_{Rs}	: Ripple voltage of current sense resistor [V] (about 100 mV is recommended as a target)
I_{LIM}	: Current limit value [A]
ΔIL	: Ripple current peak-to-peak value of inductor [A]

Select the power dissipation of the current sense resistor so that it does not exceed the allowable dissipation amount.
Power dissipation of current sense resistor $= RS \times I_{OMAX}^2 \times (1 - V_O/V_{IN})$ [W]

R_S	: Current sense resistor value [Ω] (or low-side FET on-resistance (R_{ON}))
I_{OMAX}	: Maximum load current value [A]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]

Boot strap diode
Select Schottky barrier diode (SBD) with the smallest possible forward current.
The electric current that drives the gate of high-side FET flows to boot strap diode.
Calculate the mean current by the following formula. Select it so as not to exceed the electric current ratings.

$$I_D \geq Q_G \times f_{OSC}$$

I_D : Forward current [A]
Q_G : Total quantity of charge of gate on high-side FET [C]
f_{OSC} : Oscillation frequency [Hz]

Boot strap capacitor
To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. Therefore, a minimum value as a target is assumed the capacitor value which can store electric charge 10 times that of the Qg on high-side FET. And select the boot strap capacitor.

$$C_{BOOT} \geq 0.002 \times Qg$$

C_{BOOT} : Bootstrap capacitor value [µF]
Qg : Amount of gate charge on high-side FET [nC]

VB pin capacitor
2.2 µF is assumed to be a standard, and when Qg of Switching FET used is large, it is necessary to adjust it. To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. Therefore, a minimum value as a target is assumed the capacitance which can store electric charge 100 times that of the Qg on Switching FET. And select it.

Moreover, capacitor change may cause an overshoot when CTL was turned on.

Although the overshoot does not affect DC/DC operation, it must be made sure that the VB pin does not exceed its rating before its application.

$$C_{VB} \geq 0.02 \times Qg$$

C_{VB} : VB pin capacitor value [µF]
Qg : Total amount of gate charge on Switching FET [nC]

Setting method of soft-start time

To prevent a rush current to IC starting, soft-start time can be set by connecting a soft-start capacitor (C_S) to the CS pin.
When the IC starts with the CTL pin set to the "H" level, the bias voltage output capacitor (C_{VB}) which is externally connected to the VB pin starts charging. When the threshold voltage VB≥UVLO_VB is reached, the reference voltage output capacitor (C_{REF}) which is externally connected to the VREF pin starts charging. When the threshold voltage VREF≥UVLO_VREF is reached, the soft-start capacitor (C_S) which is externally connected to the CS pin starts charging at 5 µA.
The lower one of the electric potentials of the two non inverting input pins (INTREF, CS pin voltage) is compared with the voltage at the inverting input pin (INTFB) and Error Comp. output is decided. Consequently, the output of Error Comp. during the soft-start period (CS pin voltage <INTREF) is determined by comparing the INTFB voltage with the voltage at the CS pin, and the output voltage of the DC/DC converter increases in proportion to the voltage at the CS pin due to the charging to the soft-start capacitor that is externally connected to the CS pin. Calculate the soft-start time by the following formula.

$$ts \approx 0.22 \times INTREF \times C_S \times 10^6$$

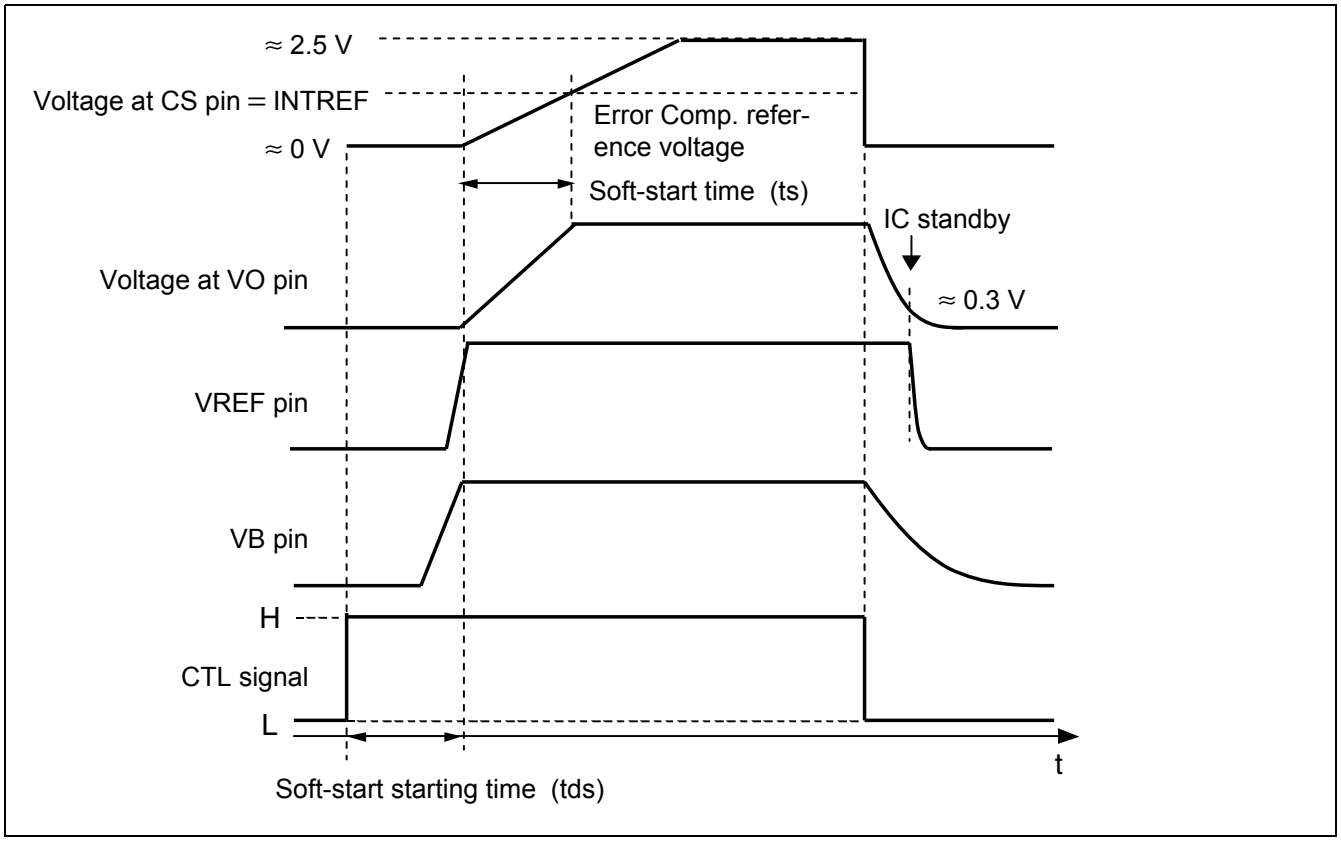
ts	: Soft-start time [S] (time until output reaches 100%)
INTREF	: Error Comp. reference voltage [V]
C_S	: CS pin capacitor value [F]

Note: If the CTL pin is changed from "H" to "L", IC's internal SW ($R_{ON} \approx 16\ \Omega$) which is connected to the VO pin is turned on to discharge output. When the output voltage falls below 0.3 V, the IC shuts down.

Calculate the soft-start starting time by the following formula.

$$tds \approx (80 + 4.50 \times 10^4 \times C_{VB}^{\frac{3}{5}}) \times (9.40 \times 10^{-5} \times V_{CC}^4 - 6.36 \times 10^{-3} \times V_{CC}^3 + 1.57 \times 10^{-1} \times V_{CC}^2 - 1.66 \times V_{CC} + 7.30) + 15.0$$

tds	: Soft-start starting time [ns] (time until soft-start operation starts)
V_{CC}	: Power supply voltage [V] (= V_{IN} [V])
C_{VB}	: VB pin capacitor value [F]


≈ 2.5 V
Voltage at CS pin = INTREF
≈ 0 V
Error Comp. reference voltage
Soft-start time (ts)
IC standby
Voltage at VO pin
≈ 0.3 V
VREF pin
VB pin
H
CTL signal
L
t
Soft-start starting time (tds)

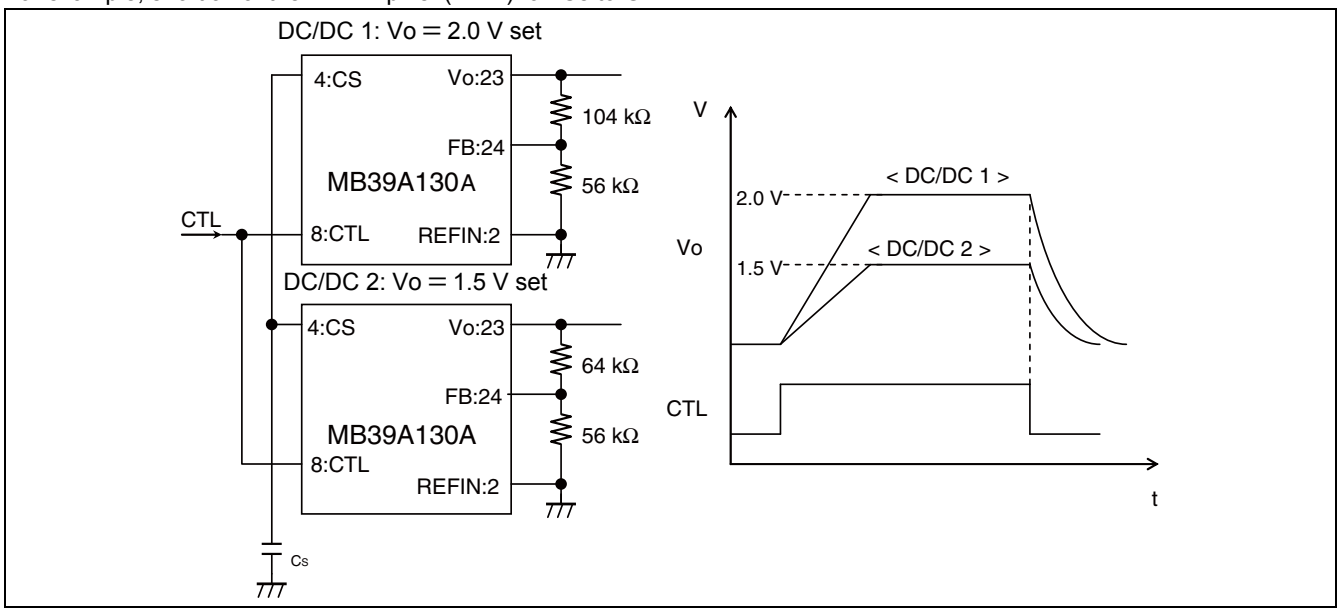
About the synchronization of multiple units of IC

The power ON/OFF sequence must be controlled, if multiple units of MB39A130A are used to supply various power supply voltages to the system. In this case, the connection shown in the following diagram may be adopted to allow simultaneous soft-start/discharge operation of multiple ICs using the same timing during power-up/power-down. It should be noted that as discharge operation is performed by NMOS SW, the decreasing rate of the output after CTL is disconnected varies depending on the setting of each output.

<Connection example 1> When aligning soft-start time

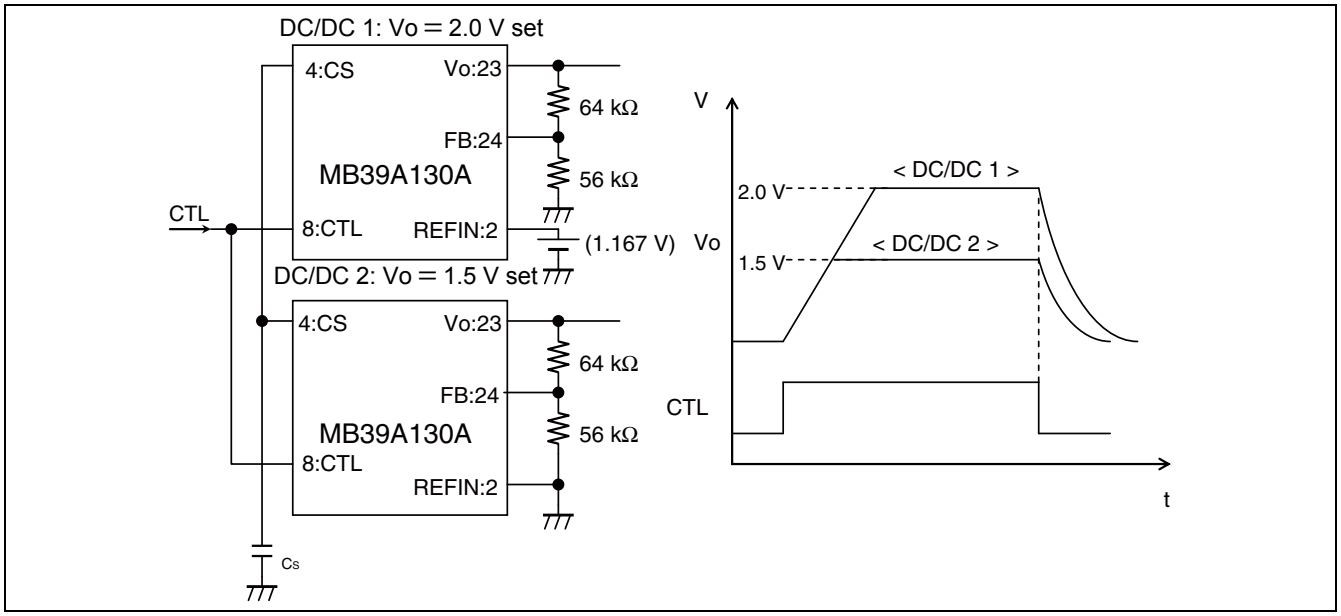
When aligning the soft-start time, set the reference voltage of Error Comp. of each IC to the same value.

For example, short all of the REFIN pins (Pin 2) of ICs to GND.



<Connection example 2> When aligning soft-start slope

When aligning the slope of the output voltage of each IC at soft-start, use the same output voltage setting resistor value ratio for all of the ICs and adjust the output voltages by adjusting the reference voltage of Error Comp.

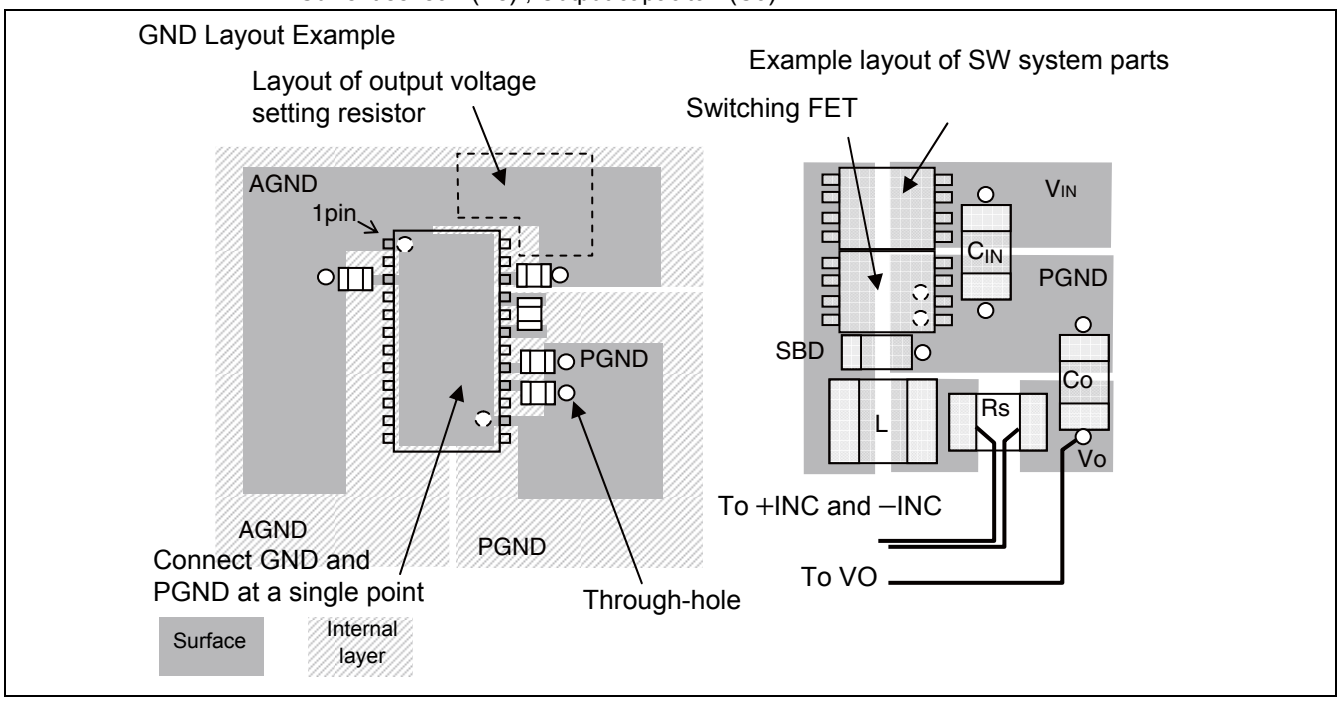


Layout

Consider the points listed below and do the layout design.

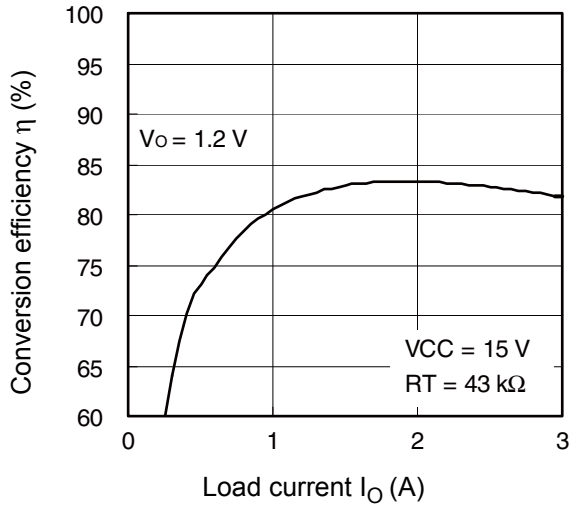
- Provide the ground plane as much as possible on the IC mounted face. Connect bypass capacitor connected with the VCC and VB pins and GND pin of the switching system parts as well as the PGND pin of the IC with switching system GND (PGND). Connect other GND connection pins with control system GND (AGND), and separate each GND, and try not to pass the heavy current path through the control system GND (AGND) as much as possible. In that case, connect control system GND (AGND) and switching system GND (PGND) at a single GND (PGND) point of the IC.
- Connect the switching system parts as much as possible on the surface. Avoid the connection through the through-hole as much as possible.
- As for GND pins of the switching system parts, provide the through hole at the proximal place, and connect it with GND of internal layer.
- Pay the most attention to the loop composed of input capacitor (C_{IN}), switching FET, and fly-back diode (SBD). Consider making the current loop as small as possible.
- Place the boot strap capacitor proximal to CB and LX pins of IC as much as possible.
- Large electric current flows momentary in the net of OUT-1 and OUT-2 pins connected with the gate of switching FET. Wire the linewidth of about 0.8 mm to be a standard, as short as possible.
- By-pass capacitor connected with VREF, VCC, and VB, and the resistor connected with the RT pin should be placed close to the pin as much as possible.
  Also connect the GND pin of the bypass capacitor with GND of internal layer in the proximal through-hole.
- +INC and −INC pins are very sensitive to noise. Therefore, pull them out individually near a pin of the element that plays the current sense role. Then, wire them close to each other through remote sensing (Kelvin connection).
  Also consider keeping them away from switching system parts as much as possible.
- Pull the feedback line to be connected to the VO pin of the IC separately from near the output capacitor pin, whenever possible, in order to feed back it to the IC more accurately. It is the ripple voltage which is generated from ESR of the output capacitor. Consider the net connected with VO and FB pins to keep away from a switching system parts as much as possible because it is sensitive to the noise. Moreover, place the output voltage setting resistor connected with this net close to the IC as much as possible, and try to make the net as short as possible. In addition, for the internal layer right under the mounting part of the output voltage setting resistor, provide the control system GND (AGND) of few ripple and few spike noises, or provide the ground plane of the power supply voltage as much as possible.

Switching system parts: Input capacitor (C_{IN}), Switching FET, Fly-back diode (SBD), Inductor (L), Current sensor (Rs), Output capacitor (Co)

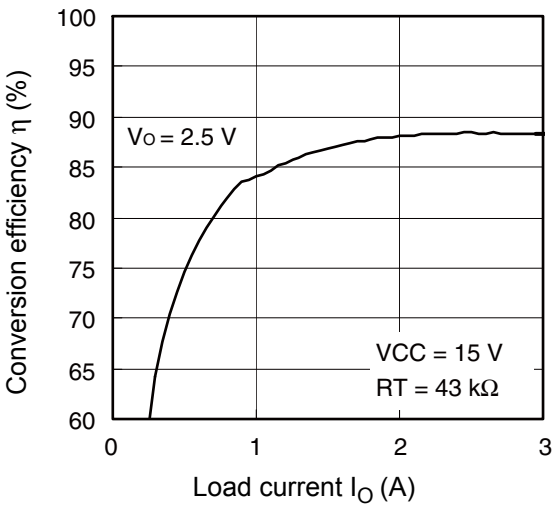


15. Reference Data

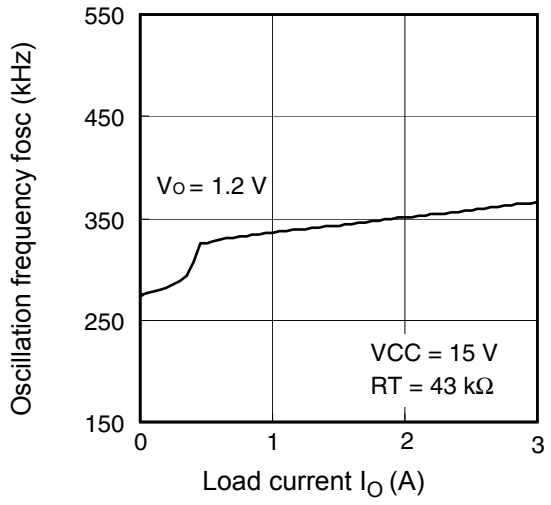
Conversion efficiency vs.Load current



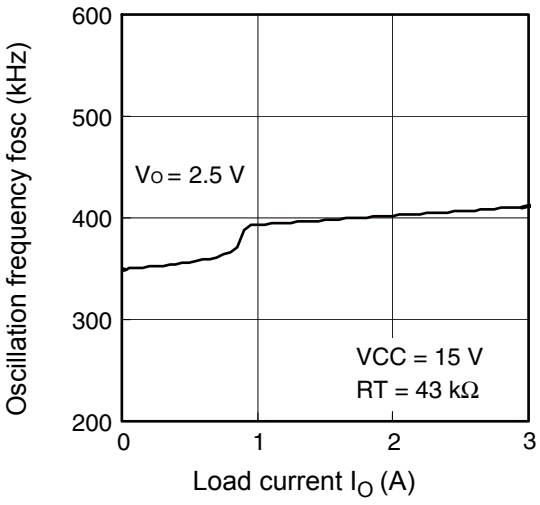
Conversion efficiency vs.Load current



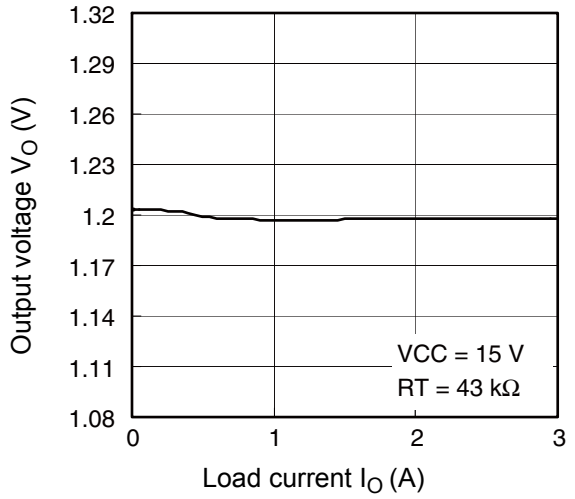
Oscillation frequency vs.Load current



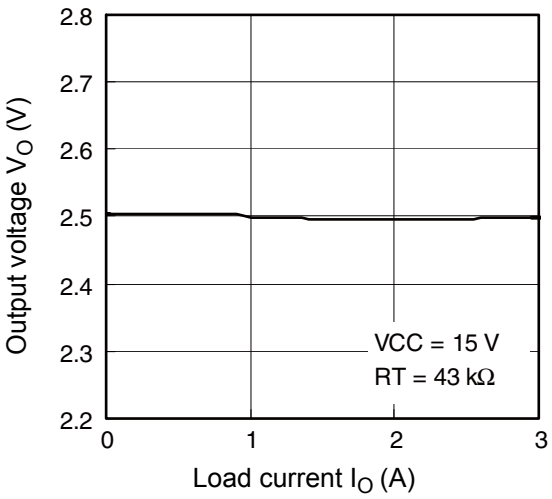
Oscillation frequency vs.Load current



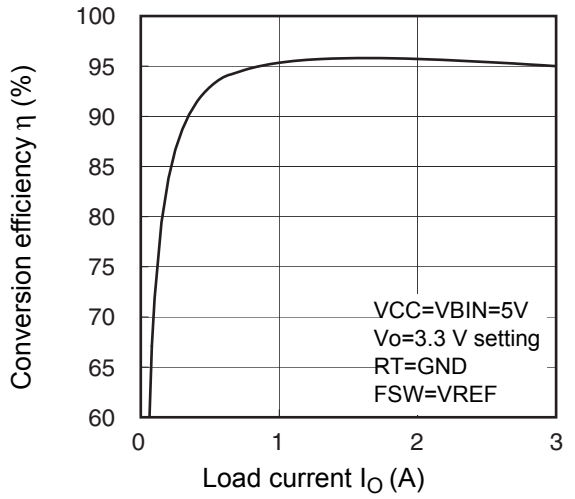
Output voltage vs.Load current



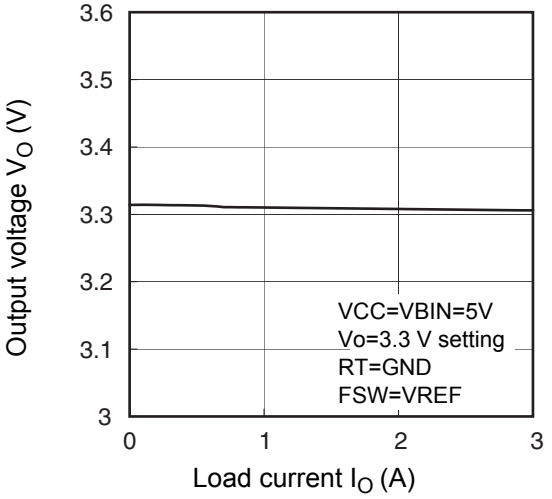
Output voltage vs.Load current



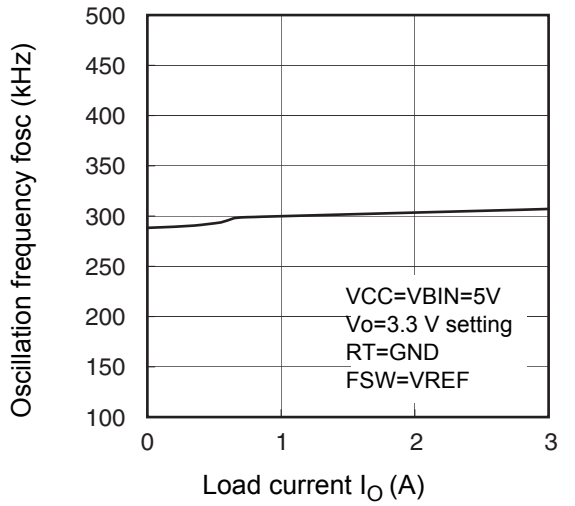
Conversion efficiency vs.Load current



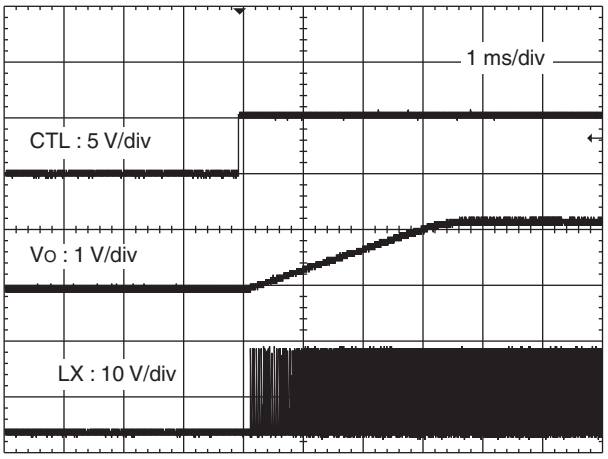
Output voltage vs.Load current



Oscillation frequency vs.Load current

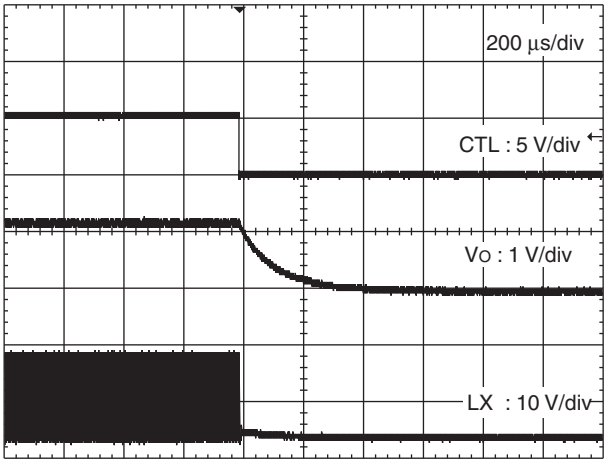


CTL Startup Waveform



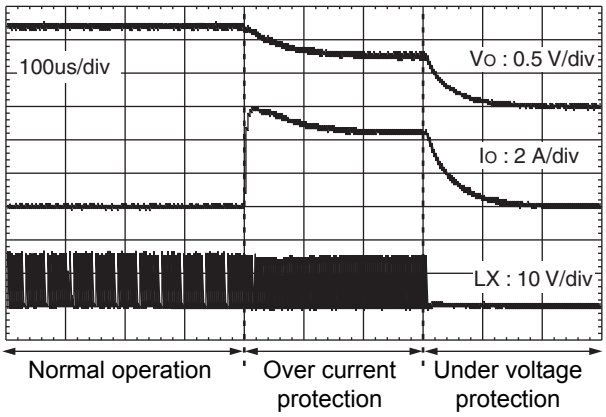
V_{IN} = 15 V, RT = 43 kΩ, Ta = +25 °C, V_O = 1.2 V
Soft-start setting time = 3.1 ms, I_O = 3 A (0.4 Ω)

CTL Shutdown Waveform



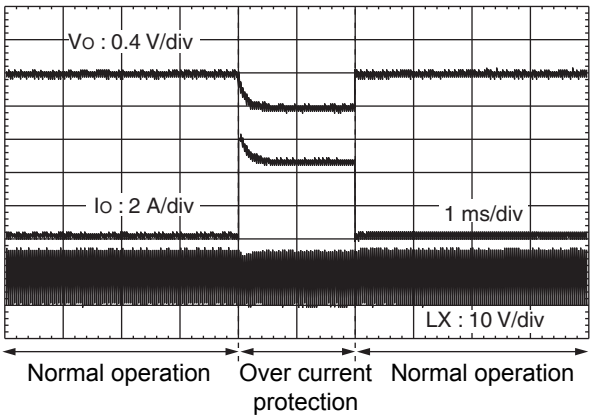
V_{IN} = 15 V, RT = 43 kΩ, Ta = +25 °C,
V_O = 1.2 V, I_O = 3 A (0.4 Ω)

Output Over Current Waveform(UVP Enabled)



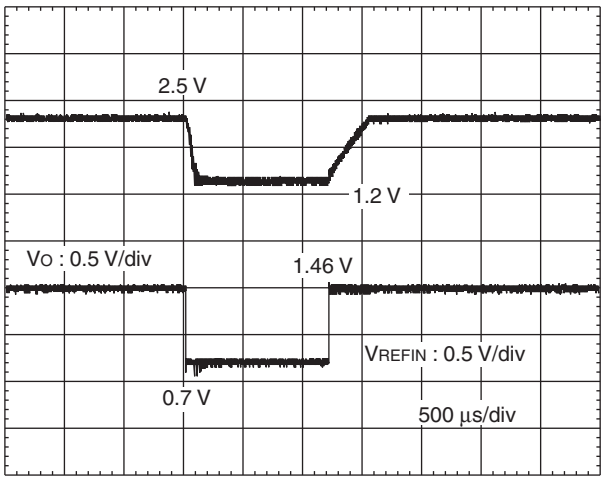
V_{IN} = 15 V ,V_O = 1.2 V, RT = 43 kΩ, Ta = +25 °C

Output Over Current Waveform (UVP Disabled)



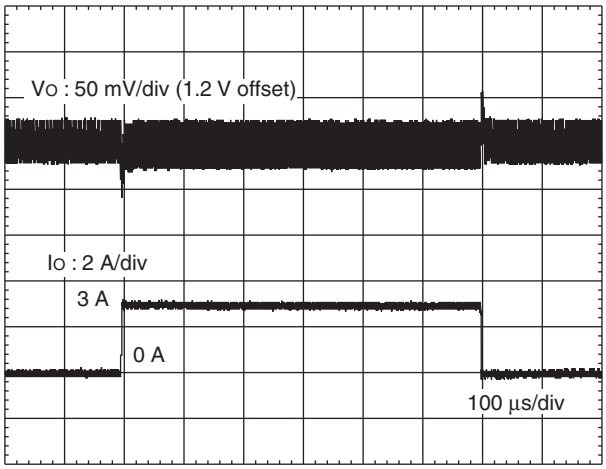
V_{IN} = 15 V, RT = 43 kΩ, V_O = 1.2 V, CUVP = GND,
Ta = +25 °C

Dynamic Output Voltage Transition



VIN = 15 V, IO = 0 A, RT = 43 kΩ, Ta = +25 °C

Load Sudden Change Waveform



VIN = 15 V, VO = 1.2 V
IO = 0 ⟷ 3 A, RT = 43 kΩ, Ta = +25 °C

16. Usage Precaution

1. Do not Configure the IC Over the Maximum Ratings.

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

2. Use the Device Within the Recommended Operating Conditions.

The recommended values guarantee the normal LSI operation under the recommended operating conditions.
The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed Circuit Board Ground Lines Should be Set up With Consideration for Common Impedance.

4. Take Appropriate Measures Against Static Electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

5. Do not Apply Negative Voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

17. Ordering Information

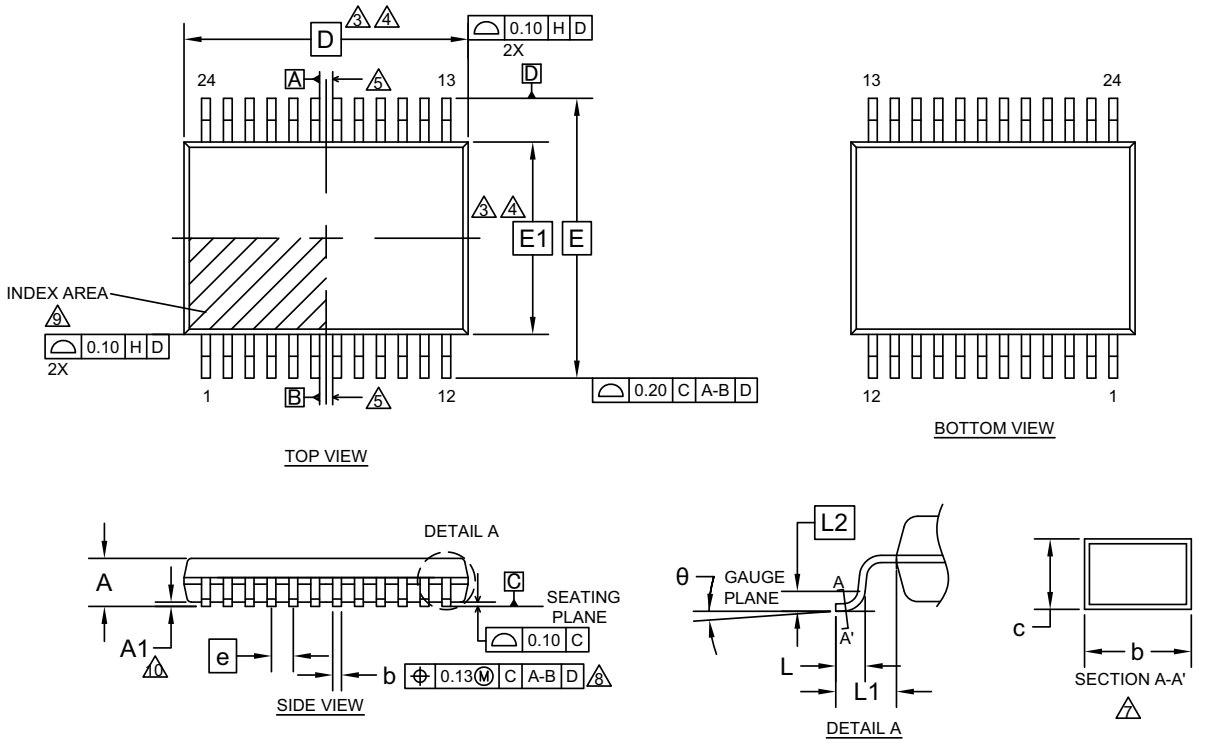
Part Number	Package	Remarks
MB39A130APFT	24-pin plastic TSSOP (STD024)	–

18. RoHS Compliance Information

The LSI products of Cypress with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) . A product whose part number has trailing characters “E1” is RoHS compliant.

19. Package Dimensions

Package Code: STD024



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	6.50 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.18	0.20	0.27
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.50 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15918 Rev. **

Document History

Document Title: MB39A130A 1ch DC/DC Buck Converter IC with Synchronous Rectification Document Number: 002-08423				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	TAOA	12/03/2010	Migrated to Cypress and assigned document number 002-08423. No change to document contents or format.
*A	5162205	TAOA	03/29/2016	Updated to Cypress template
*B	5641433	HIXT	02/24/2017	Updated Pin Assignment: Change the package name from FPT-24P-M09 to STD024 Updated Ordering Information: Change the package name from FPT-24P-M09 to STD024 Deleted “EV Board Ordering Information” Deleted “Marking Format (Lead Free Version)” Deleted “Labeling Sample (Lead Free Version)” Deleted “MB39A130APFT Recommended Conditions of Moisture Sensitivity Level” Updated Package Dimensions: Updated to Cypress format
*C	5772193	MASG	06/13/2017	Adapted Cypress new logo.

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