The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

MB91460M Series

FR60 32-bit Microcontroller

MB91460M series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.
This series contains the LIN-USART, CAN controllers, MediaLB(512Fs)*, and I^2S.

*: This product is licensed by SMSC Europe in conditions where it is used in the MediaLB system compliant with the MediaLB specification of the SMSC Europe.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal peripheral resources

- General-purpose ports : Maximum 175 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously. (External to external : 1 channel)
  - 3 transfer sources (external pin/internal peripheral/software)
  - Activation source can be selected using software.
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Fly-by transfer support (between external I/O and memory)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
  - 10-bit resolution: 12 channels
  - Conversion time: minimum 3 µs
- External interrupt inputs : 16 channels
  - 4 channels shared with CAN RX or I^2C pins
- Bit search module (for REALOS)
  - Function to search from the MSB (most significant bit) for the position of the first “0”, “1”, or changed bit in a word
- LIN-USART (full duplex double buffer): 9 channels
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
  - 4 channel is equipped with 16 stages of transmission and reception FIFO buffers.
- I^2C bus interface (supports 400 kbps): 8 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 2 channels
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- MediaLB
  - Supports 512Fs
  - 15 channels
  - Contains local channel buffers: 32 bit × 2 k.
  - Contains a 32 bit × 2 k FIFO buffer for between MediaLB and I^2S.
- I^2S : 10 channels
- 16-bit PPG timer : 8 channels
- 16-bit reload timer: 5 channels
- 16-bit free-run timer: 4 channels (1 channel each for ICU and OCU)
- Input capture: 4 channels (operates in conjunction with the free-run timer)
- Output compare: 4 channels (operates in conjunction with the free-run timer)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit
- Clock modulator
- Sub-clock calibration
  - Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator

- Main oscillator stabilization timer
  - Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  - Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

Package and technology

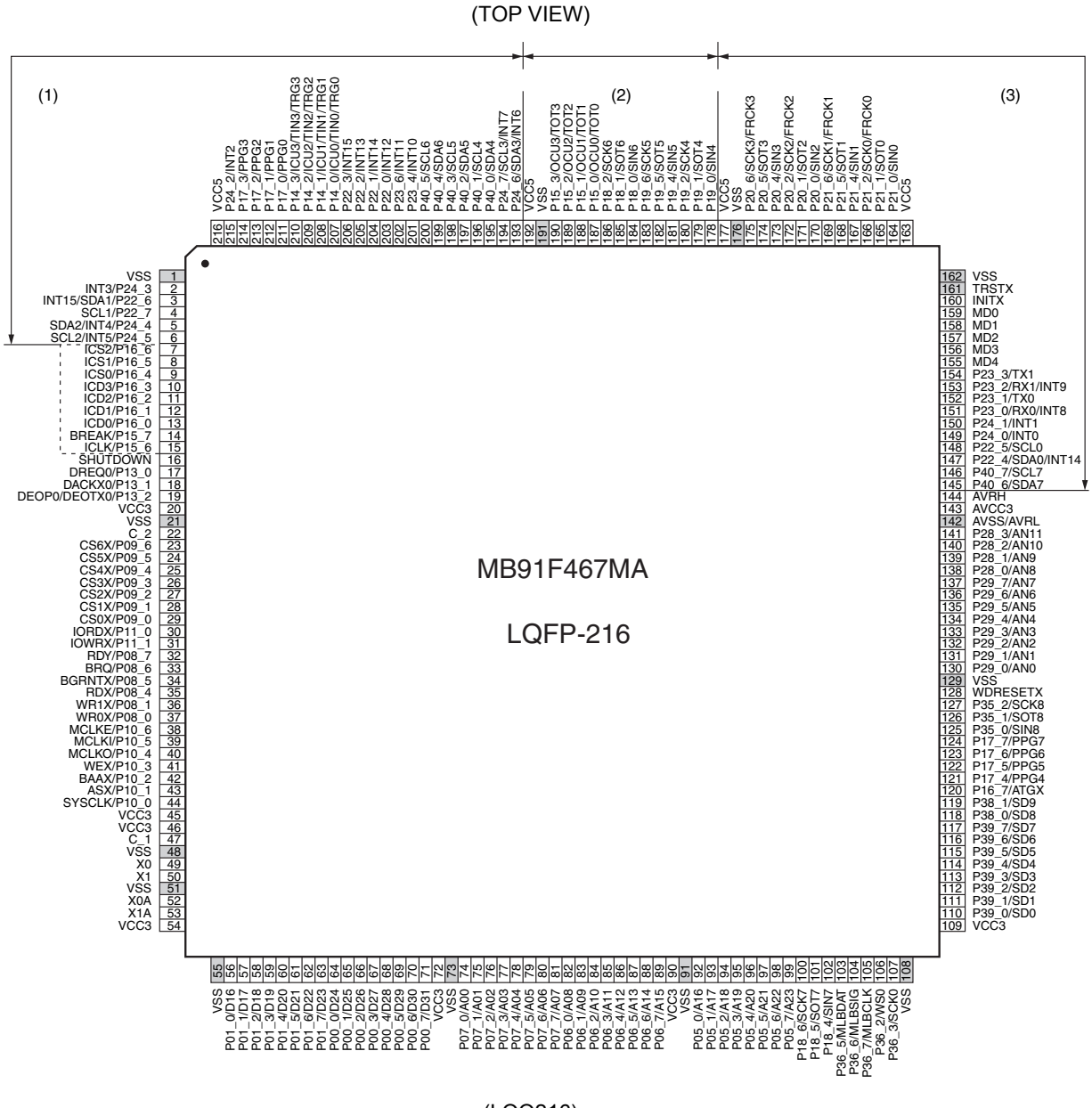
- Package : QFP-216
- CMOS 0.18 µm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 105°C

Contents

1. Product Lineup

Feature	MB91F467MA	MB91V460 (Reference)
Core frequency	80 MHz	80 MHz
Resource frequency	20 MHz	40 MHz
External bus frequency	40 MHz	40 MHz
Watchdog timer	Yes	Yes
Bit Search	Yes	Yes
Reset input pin	Yes	Yes
Low power consumption mode	Yes	Yes
DMA	5 channels	5 channels
Flash	1 Mbyte	SRAM
Flash security	Yes	No
D-RAM	48 Kbytes	64 Kbytes
I/D-RAM	16 Kbytes	64 Kbytes
Direct map cache	8 Kbytes	16 Kbytes
I-Cache	4 Kbytes	4 Kbytes
Boot-ROM	4 Kbytes	4 Kbytes
RTC	1 channel	1 channel
Free-run timer	4 channels	8 channels
ICU	4 channels	8 channels
OCU	4 channels	8 channels
Reload timer	5 channels	8 channels
PPG	8 channels	16 channels
C_CAN	2 channels (32 msg + 64 msg)	6 channels (128 msg)
LIN-USART	5 channels + 4 channels FIFO	4 channels + 4 channels FIFO + 8 channels
I^2C	8 channels	4 channels
MediaLB	512Fs	No
I^2S	10 channels	No
External bus	24 bit address / 16 bit data	32 bit address / 32 bit data
External Interrupts	16 channels	16 channels
A/D converter	12 channels	32 channels
DSU4	Yes	Yes
EDSU	Yes	Yes

2. Pin Assignment



The 5 V/3 V block is the area (1) to (3) in the figure.
This area is available for both 5 V and 3 V.However, when 5 V is used in at least one place, 5 V must be used for the area (3).

3. Pin Description

Pin no.	Pin name	I/O	I/O circuit type*	Function
2	P24_3	I/O	D	General-purpose input/output ports
	INT3			Request input pin of external interrupt ch.3.
3	P22_6	I/O	C	General-purpose input/output ports
	SDA1			Serial data input/output pin of I^2C 1.
	INT15			Request input pin of external interrupt ch.15. Exclusive from P22_3.
4	P22_7	I/O	C	General-purpose input/output ports
	SCL1			Serial clock input/output pin of I^2C 1.
5	P24_4	I/O	C	General-purpose input/output ports
	INT4			Request input pin of external interrupt ch.4.
	SDA2			Serial data input/output pin of I^2C 2.
6	P24_5	I/O	C	General-purpose input/output ports
	INT5			Request input pin of external interrupt ch.5.
	SCL2			Serial clock input/output pin of I^2C 2.
7	P16_6	I/O	H	General-purpose input/output ports. Enabled when MD4 = “0”.
	ICS2			Status output pin of DSU4. Enabled when MD4 = “1”.
8	P16_5	I/O	H	General-purpose input/output ports.Enabled when MD4 = “0”.
	ICS1			Status output pin of DSU4. Enabled when MD4 = “1”.
9	P16_4	I/O	H	General-purpose input/output ports. Enabled when MD4 = “0”.
	ICS0			Status output pin of DSU4. Enabled when MD4 = “1”.
10	P16_3	I/O	H	General-purpose input/output ports. Enabled when MD4 = “0”.
	ICD3			Data input/output pin of DSU4. Enabled when MD4 = “1”.
11	P16_2	I/O	H	General-purpose input/output ports. Enabled when MD4 = “0”.
	ICD2			Data input/output pin of DSU4. Enabled when MD4 = “1”.
12	P16_1	I/O	H	General-purpose input/output ports. Enabled when MD4 = “0”.
	ICD1			Data input/output pin of DSU4. Enabled when MD4 = “1”.
13	P16_0	I/O	H	General-purpose input/output ports. Enabled when MD4 = “0”.
	ICD0			Data input/output pin of DSU4. Enabled when MD4 = “1”.
14	P15_7	I/O	H	General-purpose input/output ports. Enabled when MD4 = “0”.
	BREAK			BREAK input pin of DSU4. Enabled when MD4 = “1”.
15	P15_6	I/O	I	General-purpose input/output ports. Enabled when MD4 = “0”.
	ICLK			Clock output pin of DSU4. Enabled when MD4 = “1”.
16	SHUTDOWN	O	J	Shutdown output, H active.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
17	P13_0	I/O	H	General-purpose input/output ports.
	DREQ0			Input pin for DMA transfer request.
18	P13_1	I/O	H	General-purpose input/output ports.
	DACKX0			Output pin for DMA transfer request acknowledge.
19	P13_2	I/O	H	General-purpose input/output ports.
	DEOTX0			Input pin for DMA transfer stop request.
	DEOP0			Output pin for DMA transfer end.
23	P09_6	I/O	H	General-purpose input/output ports.
	CS6X			Output pin of external bus chip select area 6.
24	P09_5	I/O	H	General-purpose input/output ports.
	CS5X			Output pin of external bus chip select area 5.
25	P09_4	I/O	H	General-purpose input/output ports.
	CS4X			Output pin of external bus chip select area 4.
26	P09_3	I/O	H	General-purpose input/output ports.
	CS3X			Output pin of external bus chip select area 3.
27	P09_2	I/O	H	General-purpose input/output ports.
	CS2X			Output pin of external bus chip select area 2.
28	P09_1	I/O	H	General-purpose input/output ports.
	CS1X			Output pin of external bus chip select area 1.
29	P09_0	I/O	H	General-purpose input/output ports.
	CS0X			Output pin of external bus chip select area 0.
30	P11_0	I/O	H	General-purpose input/output ports.
	IORDX			Output pin for DMA fly-by transfer from I/O to memory.
31	P11_1	I/O	H	General-purpose input/output ports.
	IOWRX			Output pin for DMA fly-by transfer from memory to I/O.
32	P08_7	I/O	H	General-purpose input/output ports.
	RDY			External bus ready input pin (when RDY is enabled to a corresponding CS area).

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
33	P08_6	I/O	H	General-purpose input/output ports.
	BRQ			External bus open request input pin (when sharing is enabled to a corresponding CS area) .
34	P08_5	I/O	H	General-purpose input/output ports.
	BGRNTX			External bus release acceptance output pin (when sharing is enabled to a corresponding CS area)
35	P08_4	I/O	H	General-purpose input/output ports.
	RDX			Output pin for external bus read strobe.
36	P08_1	I/O	H	General-purpose input/output ports.
	WR1X			Output pin for external bus write strobe.
37	P08_0	I/O	H	General-purpose input/output ports.
	WR0X			Output pin for external bus write strobe.
38	P10_6	I/O	H	General-purpose input/output ports.
	MCLKE			Output pin for external bus memory clock enabled.
39	P10_5	I/O	H	General-purpose input/output ports.
	MCLKI			Input pin for external bus memory clock.
40	P10_4	I/O	H	General-purpose input/output ports.
	MCLKO			Output pin for external bus memory clock.
41	P10_3	I/O	H	General-purpose input/output ports.
	WEX			Output pin for external bus write strobe.
42	P10_2	I/O	H	General-purpose input/output ports.
	BAAX			Output pin for external bus burst access.
43	P10_1	I/O	H	General-purpose input/output ports.
	ASX			Output pin for external bus address strobe.
44	P10_0	I/O	H	General-purpose input/output ports.
	SYSCLK			Output pin for external bus clock.
49	X0	—	G	Main oscillation pin
50	X1	—	G	Main oscillation pin
52	X0A	—	G	Sub oscillation pin
53	X1A	—	G	Sub oscillation pin
56	P01_0	I/O	H	General-purpose input/output ports.
	D16			I/O pin for 16-bit external data bus.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
57	P01_1	I/O	H	General-purpose input/output ports.
	D17			I/O pin for 17-bit external data bus.
58	P01_2	I/O	H	General-purpose input/output ports.
	D18			I/O pin for 18-bit external data bus.
59	P01_3	I/O	H	General-purpose input/output ports.
	D19			I/O pin for 19-bit external data bus.
60	P01_4	I/O	H	General-purpose input/output ports.
	D20			I/O pin for 20-bit external data bus.
61	P01_5	I/O	H	General-purpose input/output ports.
	D21			I/O pin for 21-bit external data bus.
62	P01_6	I/O	H	General-purpose input/output ports.
	D22			I/O pin for 22-bit external data bus.
63	P01_7	I/O	H	General-purpose input/output ports.
	D23			I/O pin for 23-bit external data bus.
64	P00_0	I/O	H	General-purpose input/output ports.
	D24			I/O pin for 24-bit external data bus.
65	P00_1	I/O	H	General-purpose input/output ports.
	D25			I/O pin for 25-bit external data bus.
66	P00_2	I/O	H	General-purpose input/output ports.
	D26			I/O pin for 26-bit external data bus.
67	P00_3	I/O	H	General-purpose input/output ports.
	D27			I/O pin for 27-bit external data bus.
68	P00_4	I/O	H	General-purpose input/output ports.
	D28			I/O pin for 28-bit external data bus.
69	P00_5	I/O	H	General-purpose input/output ports.
	D29			I/O pin for 29-bit external data bus.
70	P00_6	I/O	H	General-purpose input/output ports.
	D30			I/O pin for 30-bit external data bus.
71	P00_7	I/O	H	General-purpose input/output ports.
	D31			I/O pin for 31-bit external data bus.
74	P07_0	I/O	H	General-purpose input/output ports.
	A00			I/O pin for 0-bit external address bus.
75	P07_1	I/O	H	General-purpose input/output ports.
	A01			I/O pin for 1-bit external address bus.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
76	P07_2	I/O	H	General-purpose input/output ports.
	A02			I/O pin for 2-bit external address bus.
77	P07_3	I/O	H	General-purpose input/output ports.
	A03			I/O pin for 3-bit external address bus.
78	P07_4	I/O	H	General-purpose input/output ports.
	A04			I/O pin for 4-bit external address bus.
79	P07_5	I/O	H	General-purpose input/output ports.
	A05			I/O pin for 5-bit external address bus.
80	P07_6	I/O	H	General-purpose input/output ports.
	A06			I/O pin for 6-bit external address bus.
81	P07_7	I/O	H	General-purpose input/output ports.
	A07			I/O pin for 7-bit external address bus.
82	P06_0	I/O	H	General-purpose input/output ports.
	A08			I/O pin for 8-bit external address bus.
83	P06_1	I/O	H	General-purpose input/output ports.
	A09			I/O pin for 9-bit external address bus.
84	P06_2	I/O	H	General-purpose input/output ports.
	A10			I/O pin for 10-bit external address bus.
85	P06_3	I/O	H	General-purpose input/output ports.
	A11			I/O pin for 11-bit external address bus.
86	P06_4	I/O	H	General-purpose input/output ports.
	A12			I/O pin for 12-bit external address bus.
87	P06_5	I/O	H	General-purpose input/output ports.
	A13			I/O pin for 13-bit external address bus.
88	P06_6	I/O	H	General-purpose input/output ports.
	A14			I/O pin for 14-bit external address bus.
89	P06_7	I/O	H	General-purpose input/output ports.
	A15			I/O pin for 15-bit external address bus.
92	P05_0	I/O	H	General-purpose input/output ports.
	A16			I/O pin for 16-bit external address bus.
93	P05_1	I/O	H	General-purpose input/output ports.
	A17			I/O pin for 17-bit external address bus.
94	P05_2	I/O	H	General-purpose input/output ports.
	A18			I/O pin for 18-bit external address bus.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
95	P05_3	I/O	H	General-purpose input/output ports.
	A19			I/O pin for 19-bit external address bus.
96	P05_4	I/O	H	General-purpose input/output ports.
	A20			I/O pin for 20-bit external address bus.
97	P05_5	I/O	H	General-purpose input/output ports.
	A21			I/O pin for 21-bit external address bus.
98	P05_6	I/O	H	General-purpose input/output ports.
	A22			I/O pin for 22-bit external address bus.
99	P05_7	I/O	H	General-purpose input/output ports.
	A23			I/O pin for 23-bit external address bus.
100	P18_6	I/O	H	General-purpose input/output ports.
	SCK7			Clock input/output pin of LIN-USART 7.
101	P18_5	I/O	H	General-purpose input/output ports.
	SOT7			Serial data output pin of LIN-USART 7
102	P18_4	I/O	H	General-purpose input/output ports.
	SIN7			Serial data input pin of LIN-USART 7
103	P36_5	I/O	L	General-purpose input/output ports.
	MLBDAT			Data input/output pin for MediaLB.
104	P36_6	I/O	L	General-purpose input/output ports.
	MLBSIG			Data input/output pin for MediaLB.
105	P36_7	I/O	L	General-purpose input/output ports.
	MLBCLK			Clock input pin for MediaLB.
106	P36_2	I/O	H	General-purpose input/output ports.
	WS0			Input/output pin of L/R judgement signal for I^2S.
107	P36_3	I/O	H	General-purpose input/output ports.
	SCK0			Clock input/output pin for I^2S.
110	P39_0	I/O	H	General-purpose input/output ports.
	SD0			Sound data input/output pin for I^2S ch.0.
111	P39_1	I/O	H	General-purpose input/output ports.
	SD1			Sound data input/output pin for I^2S ch.1.
112	P39_2	I/O	H	General-purpose input/output ports.
	SD2			Sound data input/output pin for I^2S ch.2.
113	P39_3	I/O	H	General-purpose input/output ports.
	SD3			Sound data input/output pin for I^2S ch.3.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
114	P39_4	I/O	H	General-purpose input/output ports.
	SD4			Sound data input/output pin for I^2S ch.4.
115	P39_5	I/O	H	General-purpose input/output ports.
	SD5			Sound data input/output pin for I^2S ch.5.
116	P39_6	I/O	H	General-purpose input/output ports.
	SD6			Sound data input/output pin for I^2S ch.6.
117	P39_7	I/O	H	General-purpose input/output ports.
	SD7			Sound data input/output pin for I^2S ch.7.
118	P38_0	I/O	H	General-purpose input/output ports.
	SD8			Sound data input/output pin for I^2S ch.8.
119	P38_1	I/O	H	General-purpose input/output ports.
	SD9			Sound data input/output pin for I^2S ch.9.
120	P16_7	I/O	H	General-purpose input/output ports.
	ATGX			A/D converter external trigger input.
121	P17_4	I/O	H	General-purpose input/output ports.
	PPG4			Waveform output pin of programmable pulse generator PPG 4.
122	P17_5	I/O	H	General-purpose input/output ports.
	PPG5			Waveform output pin of programmable pulse generator PPG 5.
123	P17_6	I/O	H	General-purpose input/output ports.
	PPG6			Waveform output pin of programmable pulse generator PPG 6.
124	P17_7	I/O	H	General-purpose input/output ports.
	PPG7			Waveform output pin of programmable pulse generator PPG 7.
125	P35_0	I/O	H	General-purpose input/output ports.
	SIN8			Serial data input of LIN-USART 8.
126	P35_1	I/O	H	General-purpose input/output ports.
	SOT8			Serial data output of LIN-USART 8.
127	P35_2	I/O	H	General-purpose input/output ports.
	SCK8			Clock input/output of LIN-USART 8.
128	WDRESETX	O	J	Watchdog reset output, L Active.
130	P29_0	I/O	F	General-purpose input/output ports.
	AN0			Analog input ch.0 for A/D converter.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
131	P29_1	I/O	F	General-purpose input/output ports.
	AN1			Analog input ch.1 for A/D converter.
132	P29_2	I/O	F	General-purpose input/output ports.
	AN2			Analog input ch.2 for A/D converter.
133	P29_3	I/O	F	General-purpose input/output ports.
	AN3			Analog input ch.3 for A/D converter.
134	P29_4	I/O	F	General-purpose input/output ports.
	AN4			Analog input ch.4 for A/D converter.
135	P29_5	I/O	F	General-purpose input/output ports.
	AN5			Analog input ch.5 for A/D converter.
136	P29_6	I/O	F	General-purpose input/output ports.
	AN6			Analog input ch.6 for A/D converter.
137	P29_7	I/O	F	General-purpose input/output ports.
	AN7			Analog input ch.7 for A/D converter.
138	P28_0	I/O	F	General-purpose input/output ports.
	AN8			Analog input ch.8 for A/D converter.
139	P28_1	I/O	F	General-purpose input/output ports.
	AN9			Analog input ch.9 for A/D converter.
140	P28_2	I/O	F	General-purpose input/output ports.
	AN10			Analog input ch.10 for A/D converter.
141	P28_3	I/O	F	General-purpose input/output ports.
	AN11			Analog input ch.11 for A/D converter.
145	P40_6	I/O	C	General-purpose input/output ports.
	SDA7			Serial data input/output pin of I^2C 7.
146	P40_7	I/O	C	General-purpose input/output ports.
	SCL7			Serial clock input/output pin of I^2C 7.
147	P22_4	I/O	C	General-purpose input/output ports.
	SDA0			Serial data input/output pin of I^2C 0.
	INT14			Request input pin of external interrupt ch.14. Exclusive from P22_1.
148	P22_5	I/O	C	General-purpose input/output ports.
	SCL0			Serial clock input/output pin of I^2C 0.
149	P24_0	I/O	D	General-purpose input/output ports.
	INT0			Request input pin of external interrupt ch.0.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
150	P24_1	I/O	D	General-purpose input/output ports.
	INT1			Request input pin of external interrupt ch.1.
151	P23_0	I/O	D	General-purpose input/output ports.
	RX0			Reception input pin of CAN 0.
	INT8			Request input pin of external interrupt ch.8.
152	P23_1	I/O	D	General-purpose input/output ports.
	TX0			Transmission output pin of CAN 0.
153	P23_2	I/O	D	General-purpose input/output ports.
	RX1			Reception input pin of CAN 1.
	INT9			Request input pin of external interrupt ch.9.
154	P23_3	I/O	D	General-purpose input/output ports.
	TX1			Transmission output pin of CAN 1.
155	MD4	I	A	Mode pin 4
156	MD3	I	A	Mode pin 3
157	MD2	I	K	Mode pin 2
158	MD1	I	K	Mode pin 1
159	MD0	I	K	Mode pin 0
160	INITX	I	B	MCU reset input pin, L active doesn't change.
161	TRSTX	I	E	Tool reset input pin, L active doesn't change.
164	P21_0	I/O	D	General-purpose input/output ports.
	SIN0			Serial data input pin of LIN-USART 0.
165	P21_1	I/O	D	General-purpose input/output ports.
	SOT0			Serial data output pin of LIN-USART 0.
166	P21_2	I/O	D	General-purpose input/output ports.
	SCK0			Clock input/output pin of LIN-USART 0.
	FRCK0			Clock input pin of Free-run timer FRT0.
167	P21_4	I/O	D	General-purpose input/output ports.
	SIN1			Serial data input pin of LIN-USART 1 .
168	P21_5	I/O	D	General-purpose input/output ports.
	SOT1			Serial data output pin of LIN-USART 1.
169	P21_6	I/O	D	General-purpose input/output ports.
	SCK1			Clock input/output pin of LIN-USART 1.
	FRCK1			Clock input pin of Free-run timer FRT1.
170	P20_0	I/O	D	General-purpose input/output ports.
	SIN2			Serial data input pin of LIN-USART 2 .

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
171	P20_1	I/O	D	General-purpose input/output ports.
	SOT2			Serial data output pin of LIN-USART 2.
172	P20_2	I/O	D	General-purpose input/output ports.
	SCK2			Clock input/output pin of LIN-USART 2.
	FRCK2			Clock input pin of Free-run timer FRT2.
173	P20_4	I/O	D	General-purpose input/output ports.
	SIN3			Serial data input pin of LIN-USART 3 .
174	P20_5	I/O	D	General-purpose input/output ports.
	SOT3			Serial data output pin of LIN-USART 3.
175	P20_6	I/O	D	General-purpose input/output ports.
	SCK3			Clock input/output pin of LIN-USART 3.
	FRCK3			Clock input pin of Free-run timer FRT3.
178	P19_0	I/O	D	General-purpose input/output ports.
	SIN4			Serial data input pin of LIN-USART 4 .
179	P19_1	I/O	D	General-purpose input/output ports.
	SOT4			Serial data output pin of LIN-USART 4.
180	P19_2	I/O	D	General-purpose input/output ports.
	SCK4			Clock input/output pin of LIN-USART 4.
181	P19_4	I/O	D	General-purpose input/output ports.
	SIN5			Serial data input pin of LIN-USART 5 .
182	P19_5	I/O	D	General-purpose input/output ports.
	SOT5			Serial data output pin of LIN-USART 5.
183	P19_6	I/O	D	General-purpose input/output ports.
	SCK5			Clock input/output pin of LIN-USART 5.
184	P18_0	I/O	D	General-purpose input/output ports.
	SIN6			Serial data input pin of LIN-USART 6 .
185	P18_1	I/O	D	General-purpose input/output ports.
	SOT6			Serial data output pin of LIN-USART 6.
186	P18_2	I/O	D	General-purpose input/output ports.
	SCK6			Clock input/output pin of LIN-USART 6.
187	P15_0	I/O	D	General-purpose input/output ports.
	OCU0			Waveform output pin of output compare OCU 0.
	TOT0			Output pin of reload timer RLT 0.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
188	P15_1	I/O	D	General-purpose input/output ports.
	OCU1			Waveform output pin of output compare OCU 1.
	TOT1			Output pin of reload timer RLT 1.
189	P15_2	I/O	D	General-purpose input/output ports.
	OCU2			Waveform output pin of output compare OCU 2.
	TOT2			Output pin of reload timer RLT 2.
190	P15_3	I/O	D	General-purpose input/output ports.
	OCU3			Waveform output pin of output compare OCU 3.
	TOT3			Output pin of reload timer RLT 3.
193	P24_6	I/O	D	General-purpose input/output ports.
	INT6			Request input pin of external interrupt ch.6.
	SDA3			Serial data input/output pin of I^2C 3.
194	P24_7	I/O	D	General-purpose input/output ports.
	INT7			Request input pin of external interrupt ch.7.
	SCL3			Serial clock input/output pin of I^2C 3.
195	P40_0	I/O	C	General-purpose input/output ports.
	SDA4			Serial data input/output pin of I^2C 4.
196	P40_1	I/O	C	General-purpose input/output ports.
	SCL4			Serial clock input/output pin of I^2C 4.
197	P40_2	I/O	C	General-purpose input/output ports.
	SDA5			Serial data input/output pin of I^2C 5.
198	P40_3	I/O	C	General-purpose input/output ports.
	SCL5			Serial clock input/output pin of I^2C 5.
199	P40_4	I/O	C	General-purpose input/output ports.
	SDA6			Serial data input/output pin of I^2C 6.
200	P40_5	I/O	C	General-purpose input/output ports.
	SCL6			Serial clock input/output pin of I^2C 6.
201	P23_4	I/O	D	General-purpose input/output ports.
	INT10			Request input pin of external interrupt ch.10.
202	P23_6	I/O	D	General-purpose input/output ports.
	INT11			Request input pin of external interrupt ch.11.
203	P22_0	I/O	D	General-purpose input/output ports.
	INT12			Request input pin of external interrupt ch.12.
204	P22_1	I/O	D	General-purpose input/output ports.
	INT14			Request input pin of external interrupt ch.14. Exclusive from P22_4.

(Continued)

(Continued)

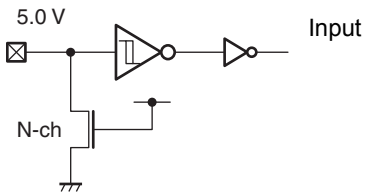
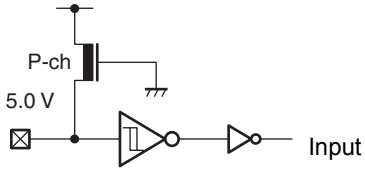
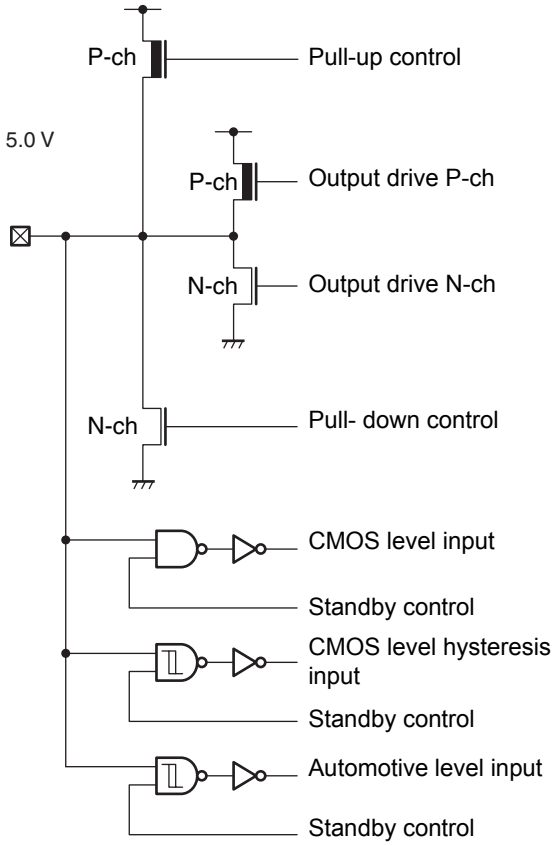
Pin no.	Pin name	I/O	I/O circuit type*	Function
205	P22_2	I/O	D	General-purpose input/output ports.
	INT13			Request input pin of external interrupt ch.13.
206	P22_3	I/O	D	General-purpose input/output ports.
	INT15			Request input pin of external interrupt ch.15. Exclusive from P22_6.
207	P14_0	I/O	D	General-purpose input/output ports.
	ICU0			Data sample input pin of Input capture ICU 0.
	TIN0			Event input pin of reload timer RLT 0.
	TRG0			Event input pin of programmable pulse generator PPG 0.
208	P14_1	I/O	D	General-purpose input/output ports.
	ICU1			Data sample input pin of Input capture ICU 1.
	TIN1			Event input pin of reload timer RLT 1.
	TRG1			Event input pin of programmable pulse generator PPG 1.
209	P14_2	I/O	D	General-purpose input/output ports.
	ICU2			Data sample input pin of input capture ICU 2.
	TIN2			Event input pin of reload timer RLT 2.
	TRG2			Event input pin of programmable pulse generator PPG 2.
210	P14_3	I/O	D	General-purpose input/output ports.
	ICU3			Data sample input pin of input capture ICU 3.
	TIN3			Event input pin of reload timer RLT 3.
	TRG3			Event input pin of programmable pulse generator PPG 3.
211	P17_0	I/O	D	General-purpose input/output ports.
	PPG0			Waveform output pin of programmable pulse generator PPG 0.
212	P17_1	I/O	D	General-purpose input/output ports.
	PPG1			Waveform output pin of programmable pulse generator PPG 1.
213	P17_2	I/O	D	General-purpose input/output ports.
	PPG2			Waveform output pin of programmable pulse generator PPG 2.
214	P17_3	I/O	D	General-purpose input/output ports.
	PPG3			Waveform output pin of programmable pulse generator PPG 3.
215	P24_2	I/O	D	General-purpose input/output ports.
	INT2			Request input pin of external interrupt ch.2.

* : For information about the I/O circuit type, refer to “4. I/O Circuit Types”.

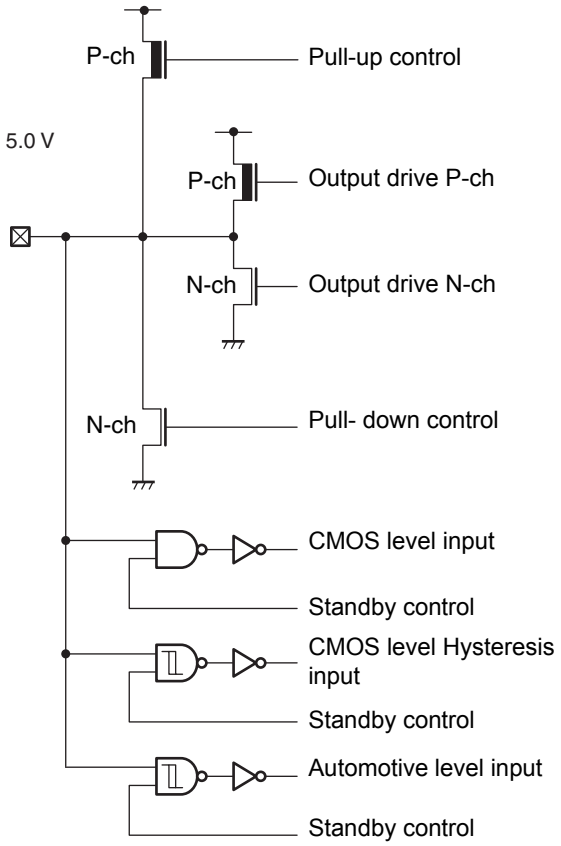
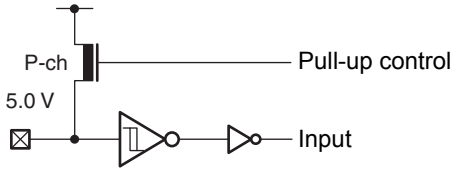
[Power supply/Ground pins]

Pin no.	Pin name	I/O	Function
1, 21, 48, 51, 55, 73, 91, 108, 129, 162, 176, 191	VSS	Supply	Ground pins
20, 45, 46, 54, 72, 90, 109	VCC3		Power supply pins for external data bus and internal regulator.
163, 177, 192, 216	VCC5		Power supply pins
143	AVCC3		Power supply pin for A/D converter
142	AVSS/AVRL		Analog ground pin, reference power supply pin for A/D converter.
144	AVRH		Reference power supply pin for A/D converter
47	C_1		Capacitor connection pin for internal regulator.
22	C_2		Capacitor connection pin for internal regulator.

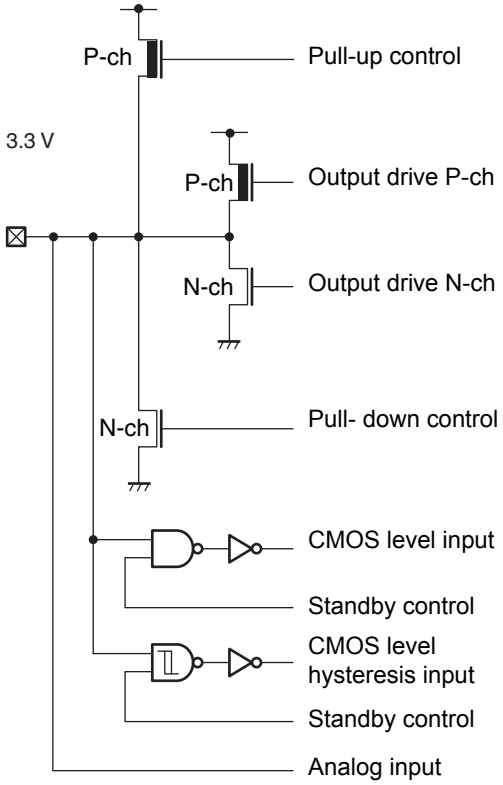
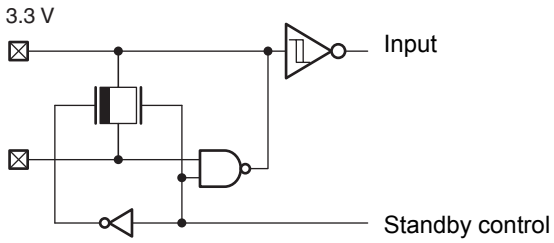
4. I/O Circuit Types

Type	Circuit	Remarks
A		• 5.0 V CMOS level hysteresis input • With Pull-down
B		• 5.0 V CMOS level hysteresis input • With Pull-up
C		• 5.0 V CMOS level output I_{OL} = 3 mA, I_{OH} = − 3 mA • 5.0 V CMOS level input • 5.0 V CMOS level hysteresis input • 5.0 V Automotive level input With standby control With Pull-up/down control • Pseudo open drain when using I^2C

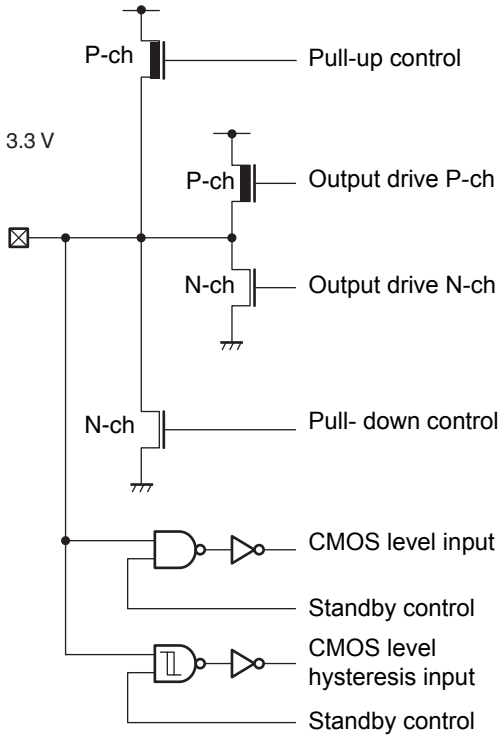
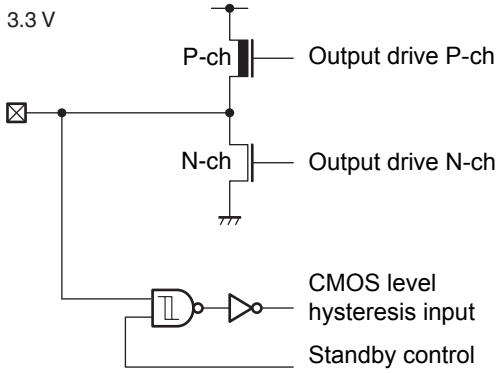
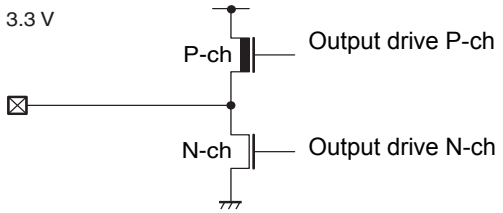
(Continued)

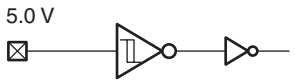
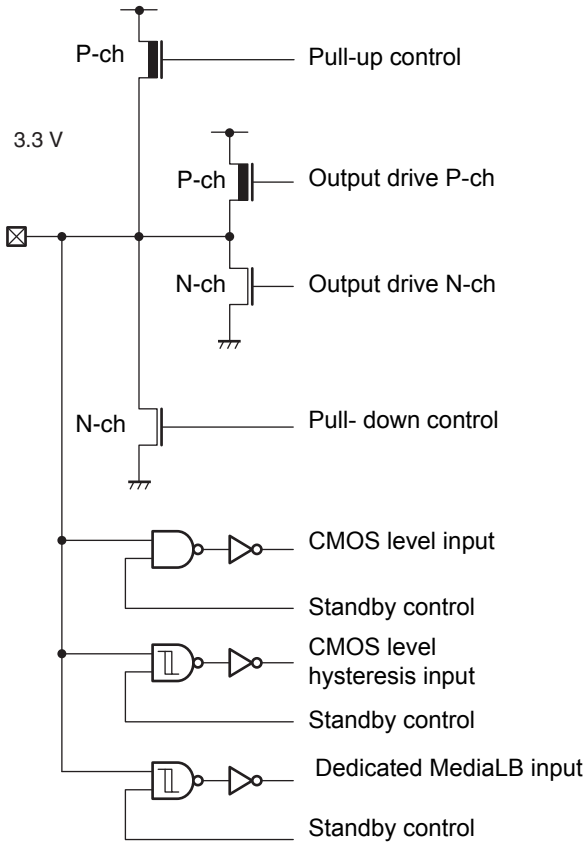
Type	Circuit	Remarks
D		• 5.0 V CMOS level output I_{OL} = 4 mA, I_{OH} = − 4 mA • 5.0 V CMOS level input • 5.0 V CMOS level hysteresis input • 5.0 V Automotive level input With standby control With Pull-up/down control
E		3.3 V CMOS level hysteresis input Withstand voltage 5 V 5.0 V pull-up function (When DSU4 is unused)

(Continued)

Type	Circuit	Remarks
F		• 3.3 V CMOS level output I_{OL} = 4 mA, I_{OH} = − 4 mA • 3.3 V CMOS level input • 3.3 V CMOS level hysteresis input With standby control • Analog input for A/D converter
G		3.3 V Oscillation cell Feedback resistor 1 MΩ With standby control

(Continued)

Type	Circuit	Remarks
H		• 3.3 V CMOS level output I_{OL} = 4 mA, I_{OH} = − 4 mA • 3.3 V CMOS level input • 3.3 V CMOS level hysteresis input With standby control With Pull-up/down control
I		• 3.3 V CMOS level output I_{OL} = 8 mA, I_{OH} = − 8 mA • 3.3 V CMOS level hysteresis input With standby control
J		3.3 V CMOS level output I_{OL} = 4 mA, I_{OH} = − 4 mA

Type	Circuit	Remarks
K		5.0 V CMOS level hysteresis input
L		• 3.3 V CMOS level output I_{OL} = 6 mA, I_{OH} = − 6 mA • 3.3 V CMOS level input • 3.3 V CMOS level hysteresis input • 3.3 V MediaLB level hysteresis input With standby control With Pull-up/down control

5. Handling Devices

Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than V_{CC} or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rating is applied between VCC and VSS pins.
If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2 KΩ or more) or enable internal pull up or pull down resistors before setting the global port enable bit.
Unused input and output pins need to leave open at the output state, or treat the same as for the input pin when they are at the input state.

Power supply pins

The MB91460M series has multiple of VCC and VSS pins.
The device is designed such that pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. However, all of these pins must be connected externally to the power supply or ground in order to minimize undesired electromagnetic radiation, prevent strobe signal malfunctions due to the rise in ground level, and conform to the total output current rating.
Moreover, connect the current supply source with the VCC and VSS pins of this device at the low impedance.
It is also recommended that a ceramic capacitor of around 0.1 µF be connected as a bypass capacitor between the VCC and VSS pins at a location close to the device.
This series has a built-in regulator. Connect a bypass capacitor of 4.7 µF to C_1 and C_2 pins for the regulator.

Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator (or ceramic oscillator), as well as bypass capacitors connected to ground, are placed as close together as possible. When the signal wires for transmitting from X0 and X1 pins are pulled along, use the circuit with them shielded on board. Be careful especially when a pin next to X0 pin is used.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation. Sub clock is also needed when dual clock product is used as single clock product.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

Treatment of NC and OPEN pins

Pins marked as NC and OPEN must be left open-circuit.

Mode pins (MD0 to MD4)

These pins should be connected directly to Vcc or Vss. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and Vcc or Vss on the printed circuit board as possible and connect them with low impedance.
Especially, MD3 must be directly connected to Vss with 0 Ω.

Operation at Start-up

Be sure to execute the setting initialized reset (INIT) with INITX pin immediately after start-up.
Hold the “L” level input to the INITX pin during the stabilization wait time immediately after the power on to ensure the stabilization wait time as required by the oscillator circuit (the stabilization wait time is initialized to the minimum value when INIT is asserted to reset using the INITX pin).

Note on oscillator input at power-on

At power-on, ensure that the clock is input until the oscillator stabilization wait time has elapsed.

Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

Notes on using external clock

When using an external clock, simultaneously supply the clock signal to the X1 (X1A) pin and a clock signal with the reverse phase to X0(X0A).
However, the external clock must not be used while the microcontroller is in stop mode (oscillator stop mode). The X1 pin outputs the H level and stops in STOP mode.

Setting external bus

This model guarantees the maximum frequency of 40 MHz for the external clock operation.
Setting the base clock frequency to the maximum operation frequency without changing the initial value of DIVR1 (external bus base clock division setting register) sets the external bus frequency that is not guaranteed.
Before changing the base clock frequency, set SYSCLK not to exceed the maximum guaranteed frequency.
The AC ratings cannot be guaranteed if a pull-up resistor is connected to the pin serving as an external bus pin.

Clock control

Input the “L” signal to INIT to assure the clock oscillation stabilization wait time.
Immediately after power-on or when returning from shutdown by INITX input, keep the "L" level input to the INITX pin for oscillation stabilization wait time (8ms) in order to secure stabilization wait for the built-in regulator or oscillation stabilization wait time for the oscillation circuit.

Switching multiplexed ports

Use PFR (port function register) to switch between the use as a PORT and the multiplexed port.

Low power consumption mode

■ For the standby mode, enable the synchronous standby mode (TBCR.SYNCS="1") to use and be sure to follow the sequence below.

```
LDI     #value_of_standby, R0       ;   value_of_standby is write data of STCR.
LDI     #_STCR, R12                 ;   _STCR is address (481H) of STCR.
STB     R0, @R12                    ;   Write to standby control register (STCR)
LDUB    @12, R0                     ;   Read STCR for synchronous standby
LDUB    @12, R0                     ;   Dummy re-read of STCR
NOP                                 ;   NOP x 5 for arrangement of timing
NOP
NOP
NOP
NOP
```

In addition, set I flag, ILM and ICR to diverge to the interruption handler which triggers the return after returning to the standby mode.

■ Do not do the following when the monitor debugger is used.

- Break point setting for the above instruction lines
- Step execution for above instruction lines

Power-on sequence for dual-power-supply model

Notes on the power-on and power-off sequences

Power-on sequence : (1) $V_{CC}5$ (2) $V_{CC}3$ (3) AVRH, AV_{CC}

Power-off sequence : (1) AVRH, AV_{CC} (2) $V_{CC}3$ (3) $V_{CC}5$

Follow the above sequence.
Turn on VCC3 before applying power supply to the analog power supply AVCC3 and AVRH, or the analog signal.
AVRH must not exceed voltage of AVCC3.

Multiplexed pin for analog input

Input voltage must not exceed $AV_{CC}3$ when the multiplexed pin serving for the analog input is used as a general-purpose port.

Recommended operating condition

$V_{CC}3$ = AVCC3 = AVRH : Recommended condition

Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling described below may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

■ The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

- a user interrupt is accepted;
- single-step execution is performed;
- or execution breaks due to a data event or from the emulator menu.

1. D0 and D1 flags are updated in advance.
2. An EIT handling routine (user interrupt or emulator) is executed.
3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).

■ The following behavior occurs when an ORCCR, STILM, MOV Ri or PS instruction is executed to enable a user interrupt while that interrupt is in the active state.

4. The PS register is updated in advance.
5. An EIT handling routine (user interrupt) is executed.
6. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 4.

Watchdog timer

The watchdog timer built in this model monitors a program and resets the CPU if the reset defer function is not executed within a certain period of time or the program runs out of control. Once the function of the watchdog timer is enabled, the watchdog timer keeps on operating program until it resets the CPU.
As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops executing the program. For those conditions to which this exception applies, see “Chapter 20 Watch dog timer in Hardware manual”.

Frequency fluctuation

This chip which contains PLL can switch divide-by-two external clock to PLL output fast clock. The clock gear function which is built in this model prevents consumption power from increasing rapidly at this time.

Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

Write to registers which include a status flag (1)

Be careful not to accidentally clear a status flag, when writing into registers which include a status flag (especially the interrupt request flag).
Take notice that a flag of a status bit is not cleared and the control bit is set to the expected value at writing.
When overwriting the control bit structured by multiple bits simultaneously, it is not possible to use the bit manipulation instruction. As a result, it is necessary to access data with usual byte/half word/word when writing to both a control bit and a status flag simultaneously. At this time, be careful not to accidentally clear other bits (bits in a status flag).

Almost all registers shown below include multiple control bits and status flags.

- TBCR
- OSCR
- TCCS0, TCCS1
- ICS01
- TMCSR0, TMCSR1, TMCSR2, TMCSR3
- PCN0, PCN1, PCN2, PCN3, PCN4, PCN5
- ADCSL0, ADCSL1

Note: It is not necessary to take special care when overwriting a single bit by the bit manipulation instruction.

Write to registers which include a status flag (2)

Take notice that actual access will be delayed when writing into registers which include a status flag (especially the interrupt request flag).
This is because data is written via multiple busses.
For example, when the program exits the interrupt routine after clearing the interrupt request flag, the interrupt flag may be cleared after accepting the RETI instructions. In this case, the interrupts may be accepted again because some of the interrupt requests are left at the time of returning from the interrupt routine.
To adjust any discord between this register address and instruction execution, read synchronous registers (RBSYNC, CBSYNC0/1, and MBSYNC) along with the area where written registers exist.
Adjustment at every writing makes a bus data band width narrow. Therefore, we recommend to adjust only if necessary. For example, when continuous writing is executed, adjustment at the last writing will be enough.

The table below shows the correspondence between a target area and a synchronous register.

Register name	Target area
RBSYNC	0x0000-0x01FF, 0x0280-0x037D, 0x0400-0x063F, 0x0C00-0x0FFF (Peripheral function on R-bus)
CBSYNC0/1	0xC000-0xFFFF (CAN on D-bus)
MBSYNC	0x6000-0x6FFF (MediaLB, I^2S and FIFO buffer on F-bus)

6. Notes On Debugger

Execution of the RETI Command

If an interrupt occurs frequently during step execution, the corresponding interrupt handling routine is executed repeatedly after step execution. As the result of that, the main routine and low-interrupt-level programs will not be executed.
Do not perform the step execution of RETI instruction to prevent this issue.
Disable the corresponding interrupt and execute debugger when the corresponding interrupt routine no longer needs debugging.

Operand break

Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

Flash security

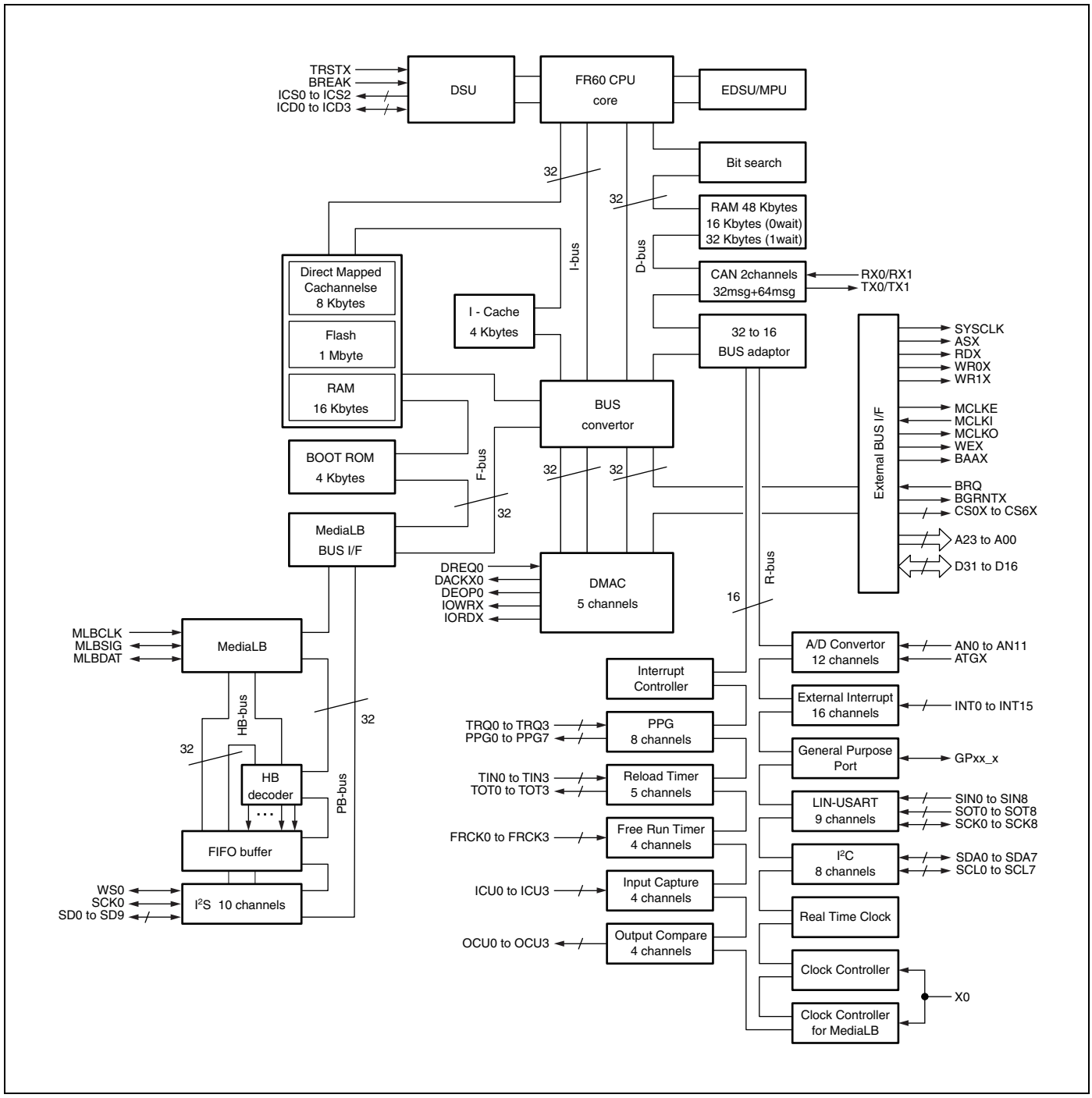
DSU4 will not be available due to security issues when Flash security is used.

Shutdown mode

It is impossible to execute debugger in the shutdown mode.

7. Block Diagram

MB91F467MA



■ CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

7.1 Features

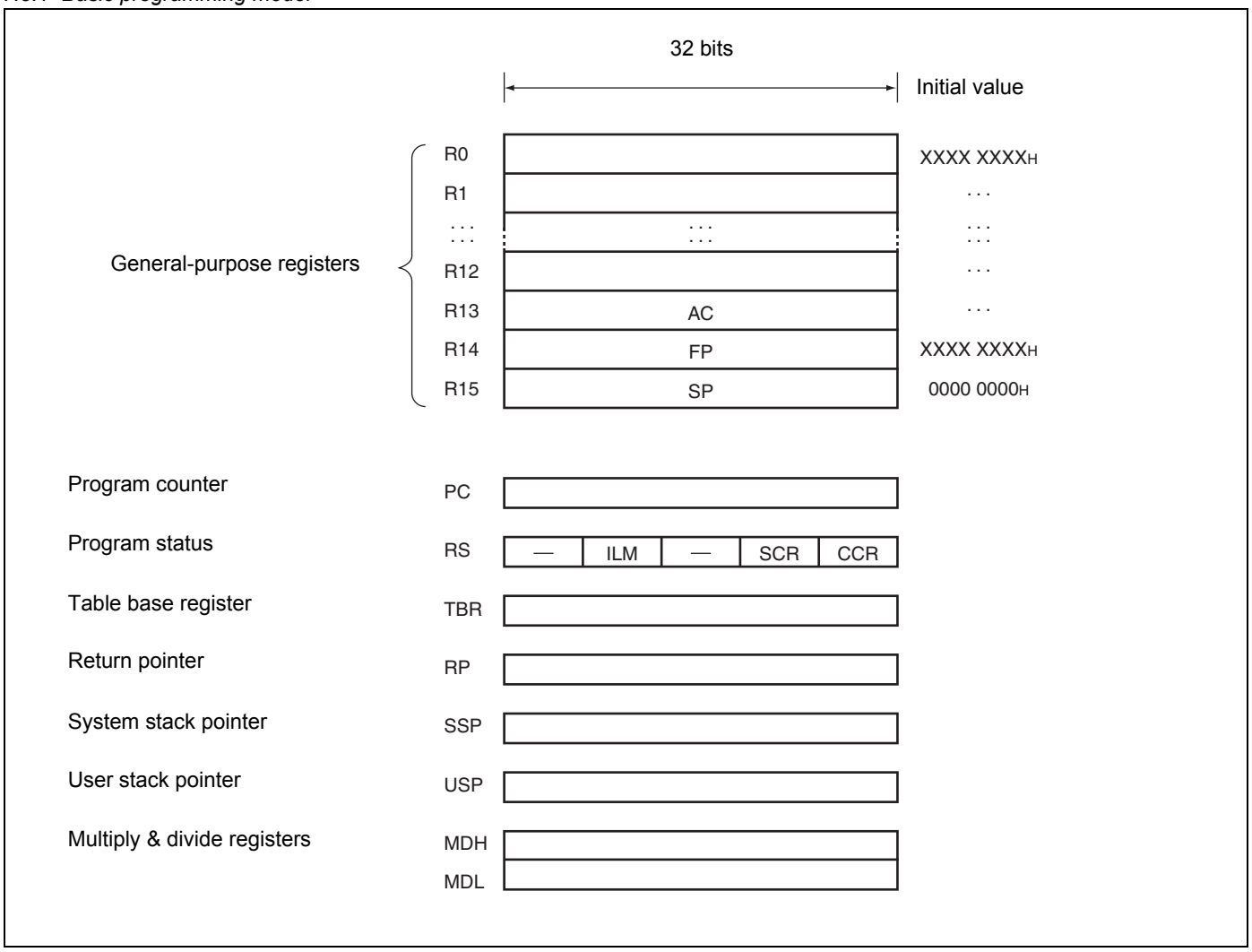
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

7.2 Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

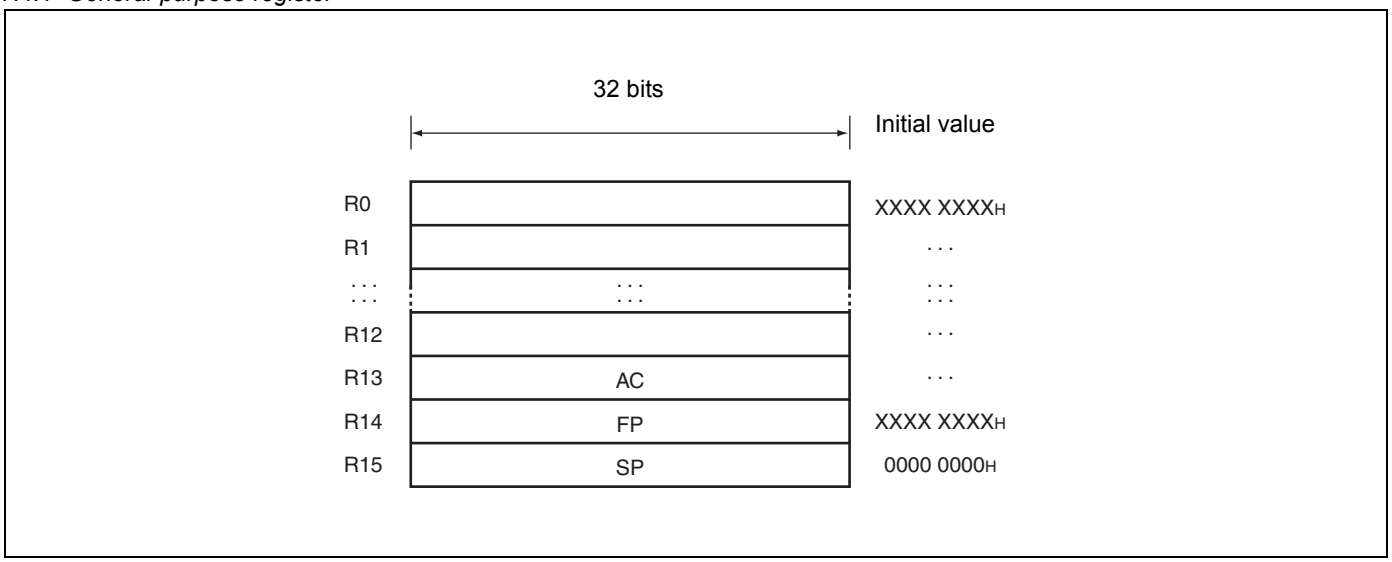
7.3 Programming model

7.3.1 Basic programming model



7.4 Registers

7.4.1 General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

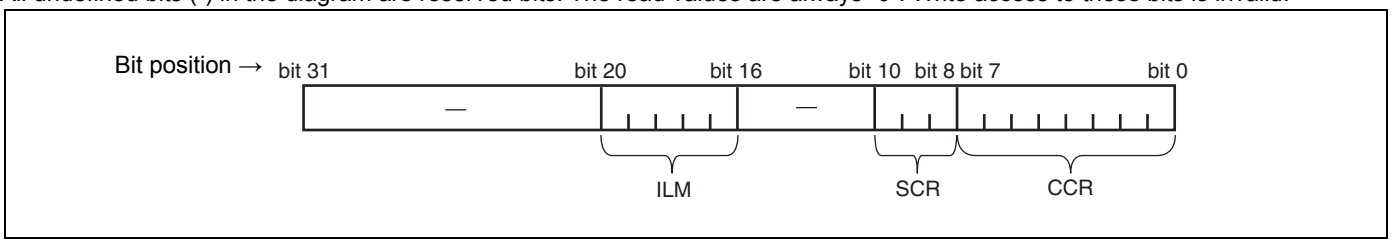
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

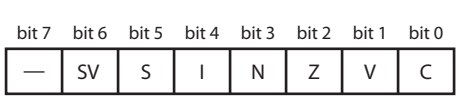
7.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



7.4.3 CCR (Condition Code Register)



Initial value

- 000XXXX$_B$

SV : Supervisor flag

S : Stack flag

I : Interrupt enable flag

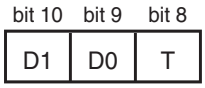
N : Negative enable flag

Z : Zero flag

V : Overflow flag

C : Carry flag

7.4.4 SCR (System Condition Register)



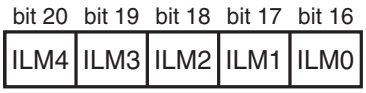
Initial value

XX0$_B$

Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

7.4.5 ILM (Interrupt Level Mask register)



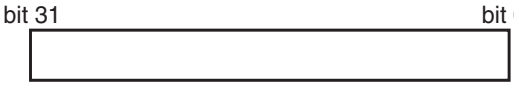
Initial value

01111$_B$

This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111_B” at reset.

7.4.6 PC (Program Counter)



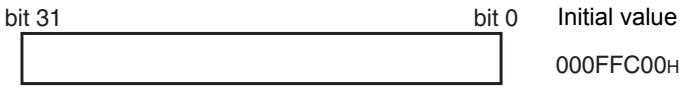
Initial value

XXXXXXXX$_H$

The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

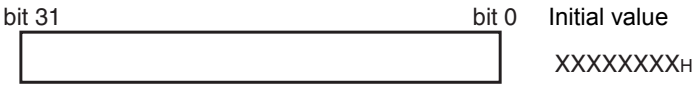
7.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

7.4.8 RP (Return Pointer)



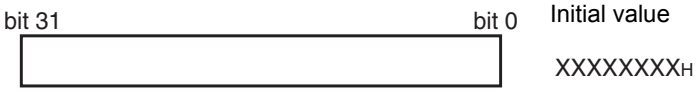
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

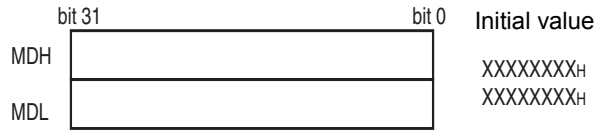
7.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

7.4.10 Multiply & divide registers



These registers are for multiplication and division, and are 32 bits each in length.

The initial value at reset is undefined.

8. Embedded Program/Data Memory (Flash)

8.1 Flash features

- MB91F467MA: 1088 Kbytes (16 × 64 Kbytes + 8 × 8 Kbytes = 8.7 Mbits)
- Programmable wait state for read/write access
- Flash and Boot security with security vector at $0014:8000_H$ to $0014:800F_H$
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

8.2 Operation modes

1. 64-bit CPU mode
   - CPU reads and executes programs in word (32-bit) length units.
   - Flash writing is not possible.
   - Actual Flash Memory access is performed in d-word (64-bit) length units.
2. 32-bit CPU mode :
   - Actual Flash Memory access is performed in word (32-bit) length units.
3. 16-bit CPU mode :
   - CPU reads and writes in half-word (16-bit) length units.
   - Program execution from the Flash is not possible.
   - Actual Flash Memory access is performed in half-word (16-bit) length units.

8.3 Flash access in CPU mode

8.3.1 Flash configuration

Flash memory map MB91F467MA

Address									
0014:FFFF$_H$ 0014:C000$_H$	SA6 (8kB)				SA7 (8kB)				ROMS7
0014:BFFF$_H$ 0014:8000$_H$	SA4 (8kB)				SA5 (8kB)				
0014:7FFF$_H$ 0014:4000$_H$	SA2 (8kB)				SA3 (8kB)				
0014:3FFF$_H$ 0014:0000$_H$	SA0 (8kB)				SA1 (8kB)				
0013:FFFF$_H$ 0012:0000$_H$	SA22 (64kB)				SA23 (64kB)				ROMS6
0011:FFFF$_H$ 0010:0000$_H$	SA20 (64kB)				SA21 (64kB)				
000F:FFFF$_H$ 000E:0000$_H$	SA18 (64kB)				SA19 (64kB)				ROMS5
000D:FFFF$_H$ 000C:0000$_H$	SA16 (64kB)				SA17 (64kB)				ROMS4
000B:FFFF$_H$ 000A:0000$_H$	SA14 (64kB)				SA15 (64kB)				ROMS3
0009:FFFF$_H$ 0008:0000$_H$	SA12 (64kB)				SA13 (64kB)				ROMS2
0007:FFFF$_H$ 0006:0000$_H$	SA10 (64kB)				SA11 (64kB)				ROMS1
0005:FFFF$_H$ 0004:0000$_H$	SA8 (64kB)				SA9 (64kB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

8.3.2 Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 80 MHz	1	1	3	-	4	

Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	-	-	0	4	
to 48 MHz	1	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 80 MHz	1	-	-	0	7	

8.3.3 Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

Notes: • Address mapping MB91F467MA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
$14:0000_H$ to $14:FFFF_H$	addr[2]=0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA = addr - addr%00:4000_H + (addr%00:4000_H)/2 - (addr/2)%4 + addr%4 - $05:0000_H$
$14:0000_H$ to $14:FFFF_H$	addr[2]=1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA = addr - addr%00:4000_H + (addr%00:4000_H)/2 - (addr/2)%4 + addr%4 - $05:0000_H$ + $00:2000_H$
$04:0000_H$ to $13:FFFF_H$	addr[2]=0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA = addr - addr%02:0000_H + (addr%02:0000_H)/2 - (addr/2)%4 + addr%4 + $0C:0000_H$
$04:0000_H$ to $13:FFFF_H$	addr[2]=1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA = addr - addr%02:0000_H + (addr%02:0000_H)/2 - (addr/2)%4 + addr%4 + $0C:0000_H$ + $01:0000_H$

Notes:
- FA result is without $20:0000_H$ offset for parallel Flash programming. Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.
- addr[2] is the value of the third lower bit when CPU address (addr) is described by binary numbers.
- FA[21] is the value of the twenty second lower bit when the flash address (FA) is described by binary numbers.
- “%” represents remainder. For example, “addr%00:4000_H” is the remainder after addr is divided by 4000_H.

8.4 Parallel Flash programming mode

8.4.1 Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F467MA

FA[21:0]	
003F:FFFFH 003F:0000H	SA23 (64kB)
003E:FFFFH 003E:0000H	SA22 (64kB)
003D:FFFFH 003D:0000H	SA21 (64kB)
003C:FFFFH 003C:0000H	SA20 (64kB)
003B:FFFFH 003B:0000H	SA19 (64kB)
003A:FFFFH 003A:0000H	SA18 (64kB)
0039:FFFFH 0039:0000H	SA17 (64kB)
0038:FFFFH 0038:0000H	SA16 (64kB)
0037:FFFFH 0037:0000H	SA15 (64kB)
0036:FFFFH 0036:0000H	SA14 (64kB)
0035:FFFFH 0035:0000H	SA13 (64kB)
0034:FFFFH 0034:0000H	SA12 (64kB)
0033:FFFFH 0033:0000H	SA11 (64kB)
0032:FFFFH 0032:0000H	SA10 (64kB)
0031:FFFFH 0031:0000H	SA9 (64kB)
0030:FFFFH 0030:0000H	SA8 (64kB)
002F:FFFFH 002F:E000H	SA7 (8kB)
002F:DFFFH 002F:C000H	SA6 (8kB)
002F:BFFFH 002F:A000H	SA5 (8kB)
002F:9FFFH 002F:8000H	SA4 (8kB)
002F:7FFFH 002F:6000H	SA3 (8kB)
002F:5FFFH 002F:4000H	SA2 (8kB)
002F:3FFFH 002F:2000H	SA1 (8kB)
002F:1FFFH 002F:0000H	SA0 (8kB)

16bit write mode	FA[1:0]=00	FA[1:0]=10
	DQ[15:0]	DQ[15:0]

Note: Always keep FA[0] = 0 and FA[21] = 1.

8.4.2 Pin connections in parallel programming mode

Resetting after setting the MD[4:0] pins to [00111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to general purpose ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	CPU mode	Flash memory mode	Normal function	Pin number
—	INITX	—	INITX	160
RESET	—	FRSTX	P13_2	19
—	—	MD2	MD2	157
—	—	MD1	MD1	156
—	—	MD0	MD0	155
RY/BY	FMCS:RDY	RY/BYX	P09_4	25
BYTE	"H"fixed	BYTEX	P13_1	18
WE	Internal bus control	WEX	P09_3	26
OE		OEX	P09_2	27
CE		CEX	P09_1	28
A-1	Internal address	FA0	P17_4	121
A0 to A7		FA1 to FA8	P17_5 to P17_7 P29_0 to P29_4	122 to 124 130 to 134
A8 to A15		FA9 to FA16	P29_5 to P29_7 P28_0 to P28_3 P16_3	135 to 141 10
A16 to A19		FA17 to FA21	P16_4 to P16_6 P22_4, P22_5	9 to 7 147, 148
DQ0 to DQ7	Internal data	DQ0 to DQ7	P36_2, P36_3 P39_0 to P39_5	106, 107 110 to 115
DQ8 to DQ15		DQ8 to DQ15	P39_6, P39_7 P38_0, P38_1 P16_7 P35_0 to P35_2	116 to 120 125 to 127

9. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

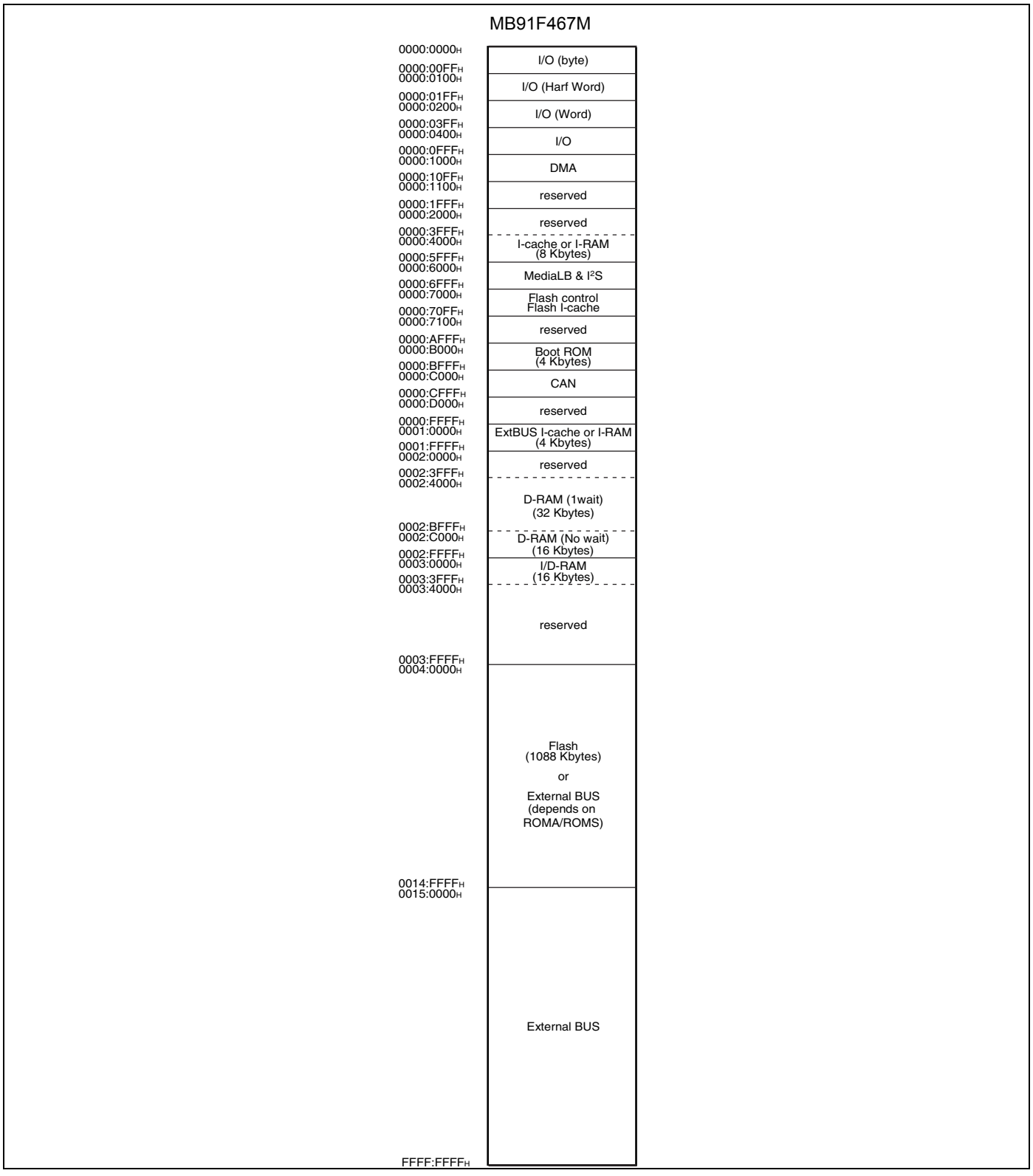
Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

10. Memory Map

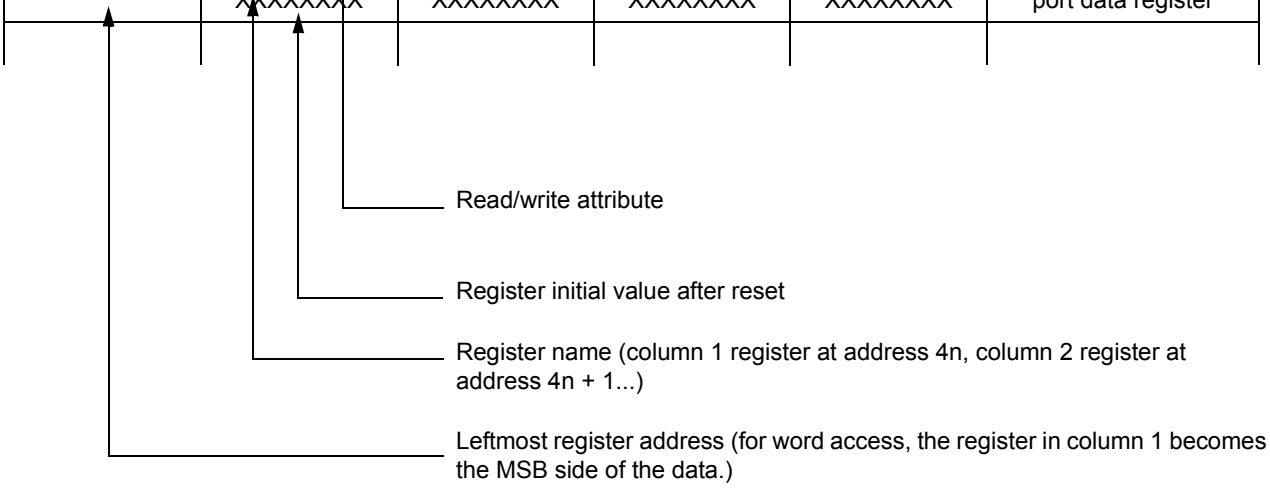
MB91F467M



11. I/O Map

1. MB91F467M

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:

" 1 " : Initial value " 1 "
" 0 " : Initial value " 0 "
" X " : Initial value " undefined "
" - " : No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved		Port Data Register [R-bus]
000004_H	Reserved	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] XXXX--XX	PDR09 [R/W] -XXXXXXX	PDR10 [R/W] -XXXXXXX	PDR11 [R/W] ------XX	
$00000C_H$	Reserved	PDR13 [R/W] -----XXX	PDR14 [R/W] ----XXXX	PDR15 [R/W] XX--XXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] -XXX-XXX	PDR19 [R/W] -XXX-XXX	
000014_H	PDR20 [R/W] -XXX-XXX	PDR21 [R/W] -XXX-XXX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] -X-XXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	Reserved			
$00001C_H$	PDR28 [R/W] ----XXXX	PDR29 [R/W] XXXXXXXX	Reserved		
000020_H	Reserved			PDR35 [R/W] -----XXX	
000024_H	PDR36 [R/W] XXX-XX--	Reserved	PDR38 [R/W] ------XX	PDR39 [R/W] XXXXXXXX	
000028_H	PDR40 [R/W] XXXXXXXX	Reserved			
$00002C_H$	Reserved				Reserved
000030_H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt
000034_H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		
000038_H	DICR [R/W] -------0	HRCL [R/W] 0--11111	RBSYNC [R] XXXXXXXX XXXXXXXX		Delay Interrupt I-unit
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W, W] 00000000	SMR00 [R/W, W] 00000000	SSR00 [R/W, R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W, R, W] -00000XX	Reserved		
000048_H	SCR01 [R/W, W] 00000000	SMR01 [R/W, W] 00000000	SSR01 [R/W, R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
$00004C_H$	ESCR01 [R/W] 00000X00	ECCR01 [R/W, R, W] -00000XX	Reserved		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000050_H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	Reserved		
000058_H	SCR03 [R/W, W] 00000000	SMR03 [R/W, W] 00000000	SSR03 [R/W, R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W, R, W] -00000XX	Reserved		
000060_H	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [R] ---00000	FCR04 [R/W] 0001-000	
000068_H	SCR05 [R/W, W] 00000000	SMR05 [R/W, W] 00000000	SSR05 [R/W, R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W, R, W] -00000XX	FSR05 [R] ---00000	FCR05 [R/W] 0001-000	
000070_H	SCR06 [R/W, W] 00000000	SMR06 [R/W, W] 00000000	SSR06 [R/W, R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W, R, W] -00000XX	FSR06 [R] ---00000	FCR06 [R/W] 0001-000	
000078_H	SCR07 [R/W, W] 00000000	SMR07 [R/W, W] 00000000	SSR07 [R/W, R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W, R, W] -00000XX	FSR07 [R] ---00000	FCR07 [R/W] 0001-000	
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baud rate Generator LIN-USART 0 to 7
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000090_H to $0000CC_H$	Reserved				Reserved
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] ------00	ITBAL0 [R/W] 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] 00----11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] -0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] -0011111	Reserved	
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] ------00	ITBAL1 [R/W] 00000000	I^2C 1
$0000E0_H$	ITMKH1 [R/W] 00----11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] -0000000	
$0000E4_H$	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] -0011111	Reserved	
$0000E8_H$ to $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] ----0000	PPG Control 0-3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] ----0000	PPG Control 4-7
000108_H, $00010C_H$	Reserved				Reserved
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000-	PCNL00 [R/W] 000000-0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000-	PCNL01 [R/W] 000000-0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000-	PCNL02 [R/W] 000000-0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000-	PCNL03 [R/W] 000000-0	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000-	PCNL04 [R/W] 000000-0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000-	PCNL05 [R/W] 000000-0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000-	PCNL06 [R/W] 000000-0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000-	PCNL07 [R/W] 000000-0	
000150_H to $00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] ---0--00 0000--00		OCS23 [R/W] ---0--00 0000--00		Input Capture 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H, $00019C_H$	Reserved				Reserved
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
$0001A4_H$	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] ---00000	ADECH [R/W] ---00000	
$0001AC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG0, PPG1)
$0001B4_H$	Reserved		TMCSRH0 [R/W] ---00000	TMCSRL0 [R/W] 0-000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG2, PPG3)
$0001BC_H$	Reserved		TMCSRH1 [R/W] ---00000	TMCSRL1 [R/W] 0-000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG4, PPG5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] ---00000	TMCSRL2 [R/W] 0-000000	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG6, PPG7)
$0001CC_H$	Reserved		TMCSRH3 [R/W] ---00000	TMCSRL3 [R/W] 0-000000	
$0001D0_H$ to $0001E4_H$	Reserved				Reserved
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (A/D Converter)
$0001EC_H$	Reserved		TMCSRH7 [R/W] ---00000	TMCSRL7 [R/W] 0-000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free-run Timer 0 (ICU0, ICU1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free-run Timer 1 (ICU2, ICU3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free-run Timer 2 (OCU0, OCU1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free-run Timer 3 (OCU2, OCU3)
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] 0--00000	Reserved			
000244_H to $00027C_H$	Reserved				Reserved
000280_H	SCR08 [R/W, W] 00000000	SMR08 [R/W, W] 00000000	SSR08 [R/W, R] 00001000	RDR08/TDR08 [R/W] 00000000	LIN-USART 8
000284_H	ESCR08 [R/W] 00000X00	ECCR08 [R/W, R, W] 000000XX	Reserved		
000288_H to $0002BC_H$	Reserved				Reserved
$0002C0_H$	BGR108 [R/W] 00000000	BGR008 [R/W] 00000000	Reserved		Baud rate Generator LIN-USART8
$0002C4_H$ to 000364_H	Reserved				Reserved
000368_H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] ------00	ITBAL2 [R/W] 00000000	I^2C 2
$00036C_H$	ITMKH2 [R/W] 00----11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] -0000000	
000370_H	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] -0011111	Reserved	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000374_H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] ------00	ITBAL3 [R/W] 00000000	I^2C 3
000378_H	ITMKH3 [R/W] 00----11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] -0000000	
$00037C_H$	Reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] -0011111	Reserved	
000380_H	IBCR4 [R/W] 00000000	IBSR4 [R] 00000000	ITBAH4 [R/W] ------00	ITBAL4 [R/W] 00000000	I^2C 4
000384_H	ITMKH4 [R/W] 00----11	ITMKL4 [R/W] 11111111	ISMK4 [R/W] 01111111	ISBA4 [R/W] -0000000	
000388_H	Reserved	IDAR4 [R/W] 00000000	ICCR4 [R/W] -0011111	Reserved	
$00038C_H$	Reserved				Reserved
000390_H	ROMS [R] 11111111 00000000		Reserved		ROM Select Register
000394_H	IBCR5 [R/W] 00000000	IBSR5 [R] 00000000	ITBAH5 [R/W] ------00	ITBAL5 [R/W] 00000000	I^2C 5
000398_H	ITMKH5 [R/W] 00----11	ITMKL5 [R/W] 11111111	ISMK5 [R/W] 01111111	ISBA5 [R/W] -0000000	
$00039C_H$	Reserved	IDAR5 [R/W] 00000000	ICCR5 [R/W] -0011111	Reserved	
$0003A0_H$	IBCR6 [R/W] 00000000	IBSR6 [R] 00000000	ITBAH6 [R/W] ------00	ITBAL6 [R/W] 00000000	I^2C 6
$0003A4_H$	ITMKH6 [R/W] 00----11	ITMKL6 [R/W] 11111111	ISMK6 [R/W] 01111111	ISBA6 [R/W] -0000000	
$0003A8_H$	Reserved	IDAR6 [R/W] 00000000	ICCR6 [R/W] -0011111	Reserved	
$0003AC_H$	IBCR7 [R/W] 00000000	IBSR7 [R] 00000000	ITBAH7 [R/W] ------00	ITBAL7 [R/W] 00000000	I^2C 7
$0003B0_H$	ITMKH7 [R/W] 00----11	ITMKL7 [R/W] 11111111	ISMK7 [R/W] 01111111	ISBA7 [R/W] -0000000	
$0003B4_H$	Reserved	IDAR7 [R/W] 00000000	ICCR7 [R/W] -0011111	Reserved	
$0003B8_H$, to $0003C0_H$	Reserved				Reserved
$0003C4_H$	Reserved			ISIZE [R/W] ------10	I-Cache

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0003C8_H$ to $0003E0_H$	Reserved				Reserved
$0003E4_H$	Reserved			ICHCR [R/W] 0-000000	I-Cache
$0003E8_H$, $0003EC_H$	Reserved				Reserved
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H to $00043C_H$	Reserved				Reserved
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	Reserved	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	Reserved		
000450_H	ICR16 [R/W] ---11111	Reserved		ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	Reserved	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	Reserved	ICR33 [R/W] ---11111	Reserved		
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000468_H	Reserved		ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	Interrupt Control Unit
$00046C_H$	Reserved				
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	Reserved				
000478_H	Reserved		ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	Reserved	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX-00	CTBR [W] XXXXXXXX	Clock Control Unit
000484_H	CLKR [R/W] ----0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				
$00048C_H$	PLLDIVM [R/W] ----0000	PLLDIVN [R/W] --000000	PLLDIVG [R/W] ----0000	PLLMULG [R/W] 00000000	PLL Clock Gear Unit
000490_H	PLLCTRL [R/W] ----0000	Reserved			
000494_H	Reserved				Reserved
000498_H	PORTEN [R/W] ------00	Reserved			Port Input Enable Control
$00049C_H$	Reserved				Reserved
$0004A0_H$	Reserved	WTCER [R/W] ------00	WTCR [R/W] 00000000 000-00-X		Real Time Clock (Watch Timer)
$0004A4_H$	Reserved	WTBR [R/W] ---XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] ---00000	WTMR [R/W] --000000	WTSR [R/W] --000000	Reserved	
$0004AC_H$	Reserved		CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock Monitor
$0004B0_H$	CUCR [R/W] -------- ---0--00		CUTD [R/W] 10000000 00000000		Sub-Oscillation Calibration Unit
$0004B4_H$	CUTR1 [R] -------- 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] --000010 11111101		Reserved	CMCR [R/W] -001--00	Clock Modulator
$0004BC_H$	CMT1 [R/W] 00000000 1---0000		CMT2 [R/W] --000000 --000000		
$0004C0_H$	CANPRE [R/W] 00000000	Reserved			CAN Clock Control

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0004C4_H$	Reserved		HWWDE [R/W] ------00	HWWD [R/W] 00011000	Hardware-Watchdog
$0004C8_H$	OSCRH [R/W] 000--001	Reserved	WPCRH [R/W] 000--001	Reserved	Main-/Sub-Oscillation Stabilization Timer
$0004CC_H$	OSCCR [R/W] ------00	Reserved			Main- Oscillation Standby Control
$0004D0_H$	Reserved				
$0004D4_H$	SHDE [R/W] 0-------	Reserved	EXTE [R/W] 00000000	EXTF [R/W] 00000000	Shutdown control
$0004D8_H$	EXTLV [R/W] 00000000 00000000		Reserved		
$0004DC_H$ to $0004E4_H$	Reserved				Reserved
$0004E8_H$	Reserved		MLBCNT [R/W] 000----0	MLBPRE [R/W] --000000	MediaLB Clock Control
$0004EC_H$, $0004F0_H$	Reserved				Reserved
$0004F4_H$	MPLLDIVM [R/W] ----0000	MPLLDIVN [R/W] --000000	MPLLDIVG [R/W] ----0000	MPLLMULG [R/W] 00000000	MediaLB PLL Clock Gear Unit
$0004F8_H$	MPLLCTRL [R/W] ----0000	Reserved			
$0004FC_H$ to $00063C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000*1		External bus Unit
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
$00065C_H$	Reserved				
000660_H	AWR0 [R/W] 01001111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
$00066C_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		Reserved		
000670_H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674_H	Reserved				
000678_H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
$00067C_H$	Reserved				
000680_H	CSER [R/W] -0000001	CHER [R/W] -1111111	Reserved	TCR [R/W] 0000**** *2	
000684_H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688_H to $0007F8_H$	Reserved				
$0007FC_H$	Reserved	MODR [W] XXXXXXXX	Reserved		Mode register
000800_H to $000CFC_H$	Reserved				Reserved

*1 : ACR0 [11:10] depends on the mode vector fetch information of bus width.

*2 : TCR [3:0] INIT value = 0000, and keeps the value after RST.

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		Port Data Direct Read Register [R-bus]
$000D04_H$	Reserved	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] XXXX--XX	PDRD09 [R] -XXXXXXX	PDRD10 [R] -XXXXXXX	PDRD11 [R] ------XX	
$000D0C_H$	Reserved	PDRD13 [R] -----XXX	PDRD14 [R] ----XXXX	PDRD15 [R] XX--XXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] -XXX-XXX	PDRD19 [R] -XXX-XXX	
$000D14_H$	PDRD20 [R] -XXX-XXX	PDRD21 [R] -XXX-XXX	PDRD22 [R] XXXXXXXX	PDRD23 [R] -X-XXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved			
$000D1C_H$	PDRD28 [R] ----XXXX	PDRD29 [R] XXXXXXXX	Reserved		
$000D20_H$	Reserved			PDRD35 [R] -----XXX	
$000D24_H$	PDRD36 [R] XXX-XX--	Reserved	PDRD38 [R] ------XX	PDRD39 [R] XXXXXXXX	
$000D28_H$	PDRD40 [R] XXXXXXXX	Reserved			
$000D2C_H$ to $000D3C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		Port Direction Register [R-bus]
$000D44_H$	Reserved	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] 0000--00	DDR09 [R/W] -0000000	DDR10 [R/W] -0000000	DDR11 [R/W] ------00	
$000D4C_H$	Reserved	DDR13 [R/W] -----000	DDR14 [R/W] ----0000	DDR15 [R/W] 00--0000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] -000-000	DDR19 [R/W] -000-000	
$000D54_H$	DDR20 [R/W] -000-000	DDR21 [R/W] -000-000	DDR22 [R/W] 00000000	DDR23 [R/W] -0-00000	
$000D58_H$	DDR24 [R/W] 00000000	Reserved			
$000D5C_H$	DDR28 [R/W] ----0000	DDR29 [R/W] 00000000	Reserved		
$000D60_H$	Reserved			DDR35 [R/W] -----000	
$000D64_H$	DDR36 [R/W] 000-00--	Reserved	DDR38 [R/W] ------00	DDR39 [R/W] 00000000	
$000D68_H$	DDR40 [R/W] 00000000	Reserved			
$000D6C_H$ to $000D7C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D80_H$	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		Port Function Register [R-bus]
$000D84_H$	Reserved	PFR05 [R/W] 11111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
$000D88_H$	PFR08 [R/W] 1111--11	PFR09 [R/W] -1111111	PFR10 [R/W] -1111111	PFR11 [R/W] ------00	
$000D8C_H$	Reserved	PFR13 [R/W] -----000	PFR14 [R/W] ----0000	PFR15 [R/W] 00--0000	
$000D90_H$	PFR16 [R/W] 0-------	PFR17 [R/W] 00000000	PFR18 [R/W] -000-000	PFR19 [R/W] -000-000	
$000D94_H$	PFR20 [R/W] -000-000	PFR21 [R/W] -000-000	PFR22 [R/W] 00000000	PFR23 [R/W] -0-00000	
$000D98_H$	PFR24 [R/W] 00000000	Reserved			
$000D9C_H$	PFR28 [R/W] ----0000	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$	Reserved			PFR35 [R/W] -----000	
$000DA4_H$	PFR36 [R/W] 000-00--	Reserved	PFR38 [R/W] ------00	PFR39 [R/W] 00000000	
$000DA8_H$	PFR40 [R/W] 00000000	Reserved			
$000DAC_H$ to $000DBC_H$	Reserved				Reserved
$000DC0_H$, $000DC4_H$	Reserved				Port Expansion Function Register [R-bus]
$000DC8_H$	Reserved		EPFR10 [R/W] --00---0	Reserved	
$000DCC_H$	Reserved	EPFR13 [R/W] ----0--	EPFR14 [R/W] ----0000	EPFR15 [R/W] ----0000	
$000DD0_H$	EPFR16 [R/W] 0-------	Reserved	EPFR18 [R/W] -00--00-	EPFR19 [R/W] -0---0--	
$000DD4_H$	EPFR20 [R/W] -0---0--	EPFR21 [R/W] -0---0--	EPFR22 [R/W] ----0-0-	Reserved	
$000DD8_H$, $000DDC_H$	Reserved				
$000DE0_H$	Reserved			EPFR35 [R/W] -----000	
$000DE4_H$ to $000DFC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000E00_H$ to $000E3C_H$	Reserved				Reserved
$000E40_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		Port Input Level Select Register [R-bus]
$000E44_H$	Reserved	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
$000E48_H$	PILR08 [R/W] 0000--00	PILR09 [R/W] -0000000	PILR10 [R/W] -0000000	PILR11 [R/W] ------00	
$000E4C_H$	Reserved	PILR13 [R/W] -----000	PILR14 [R/W] ----0000	PILR15 [R/W] 00--0000	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] -000-000	PILR19 [R/W] -000-000	
$000E54_H$	PILR20 [R/W] -000-000	PILR21 [R/W] -000-000	PILR22 [R/W] 00000000	PILR23 [R/W] -0-00000	
$000E58_H$	PILR24 [R/W] 00000000	Reserved			
$000E5C_H$	PILR28 [R/W] ----0000	PILR29 [R/W] 00000000	Reserved		
$000E60_H$	Reserved			PILR35 [R/W] -----000	
$000E64_H$	PILR36 [R/W] 000-00--	Reserved	PILR38 [R/W] ------00	PILR39 [R/W] 00000000	
$000E68_H$	PILR40 [R/W] 00000000	Reserved			
$000E6C_H$ to $000E7C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000E80_H$ to $000E88_H$	Reserved				Port Expansion Input Level Select Register [R-bus]
$000E8C_H$	Reserved		EPILR14 [R/W] ----0000	EPILR15 [R/W] ----0000	
$000E90_H$	Reserved	EPILR17 [R/W] ----0000	EPILR18 [R/W] -----000	EPILR19 [R/W] -000-000	
$000E94_H$	EPILR20 [R/W] -000-000	EPILR21 [R/W] -000-000	EPILR22 [R/W] 00000000	EPILR23 [R/W] -0-00000	
$000E98_H$	EPILR24 [R/W] 00000000	Reserved			
$000E9C_H$, $000EA0_H$	Reserved				
$000EA4_H$	EPILR36 [R/W] 000-----	Reserved			
$000EA8_H$	EPILR40 [R/W] 00000000	Reserved			
$000EAC_H$ to $000EBC_H$	Reserved				Reserved
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		Port Pull-Up/Down Enable Register [R-bus]
$000EC4_H$	Reserved	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 0000--00	PPER09 [R/W] -0000000	PPER10 [R/W] -0000000	PPER11 [R/W] ------00	
$000ECC_H$	Reserved	PPER13 [R/W] -----000	PPER14 [R/W] ----0000	PPER15 [R/W] 0---0000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] -000-000	PPER19 [R/W] -000-000	
$000ED4_H$	PPER20 [R/W] -000-000	PPER21 [R/W] -000-000	PPER22 [R/W] 00000000	PPER23 [R/W] -0-00000	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved			
$000EDC_H$	PPER28 [R/W] ----0000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$	Reserved			PPER35 [R/W] -----000	
$000EE4_H$	PPER36 [R/W] 000-00--	Reserved	PPER38 [R/W] ------00	PPER39 [R/W] 00000000	
$000EE8_H$	PPER40 [R/W] 00000000	Reserved			

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000EEC_H$ to $000EFC_H$	Reserved				Reserved
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		Port Pull-Up/Down Control Register [R-bus]
$000F04_H$	Reserved	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 1111--11	PPCR09 [R/W] -1111111	PPCR10 [R/W] -1111111	PPCR11 [R/W] ------11	
$000F0C_H$	Reserved	PPCR13 [R/W] -----111	PPCR14 [R/W] ----1111	PPCR15 [R/W] 1---1111	
$000F10_H$	PPCR16 [R/W] 11111111	PPCR17 [R/W] 11111111	PPCR18 [R/W] -111-111	PPCR19 [R/W] -111-111	
$000F14_H$	PPCR20 [R/W] -111-111	PPCR21 [R/W] -111-111	PPCR22 [R/W] 11111111	PPCR23 [R/W] -1-11111	
$000F18_H$	PPCR24 [R/W] 11111111	Reserved			
$000F1C_H$	PPCR28 [R/W] ----1111	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$	Reserved			PPCR35 [R/W] -----111	
$000F24_H$	PPCR36 [R/W] 111-11--	Reserved	PPCR38 [R/W] ------11	PPCR39 [R/W] 11111111	
$000F28_H$	PPCR40 [R/W] 11111111	Reserved			
$000F20_H$ to $000FFC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $005FFC_H$	Reserved				Reserved
006000_H	DCCR [R/W] 00000000 0------- -------- 00000000				MediaLB
006004_H	SSCR [R/W] -------- -------- -------- 00000000				
006008_H	SDCR [R/W] 00000000 00000000 00000000 0000000				
$00600C_H$	SMCR [R/W] -------- -------- -------- -1100000				
006010_H to 006018_H	Reserved				
$00601C_H$	VCCR [R] -------- 00000001 00000010 00000010				
006020_H to $00602C_H$	Reserved				
006030_H	CICR [R/W] -------- -------- -0000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006034_H to $00603C_H$	Reserved				MediaLB
006040_H	CECR0 [R/W] 0000000- 00000000 00000000 00000000				
006044_H	CSCR0 [R/W] 10------ ----0000 00000000 00000000				
006048_H	CCBCR0 [R] 00000000 00000000 00000000 00000000				
$00604C_H$	CNBCR0 [R/W] 00000000 00000000 00000000 00000000				
006050_H	CECR1 [R/W] 0000000- 00000000 00000000 00000000				
006054_H	CSCR1 [R/W] 10------ ----0000 00000000 00000000				
006058_H	CCBCR1 [R] 00000000 00000000 00000000 00000000				
$00605C_H$	CNBCR1 [R/W] 00000000 00000000 00000000 00000000				
006060_H	CECR2 [R/W] 0000000- 00000000 00000000 00000000				
006064_H	CSCR2 [R/W] 10------ ----0000 00000000 00000000				
006068_H	CCBCR2 [R] 00000000 00000000 00000000 00000000				
$00606C_H$	CNBCR2 [R/W] 00000000 00000000 00000000 00000000				
006070_H	CECR3 [R/W] 0000000- 00000000 00000000 00000000				
006074_H	CSCR3 [R/W] 10------ ----0000 00000000 00000000				
006078_H	CCBCR3 [R] 00000000 00000000 00000000 00000000				
$00607C_H$	CNBCR3 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006080_H	CECR4 [R/W] 0000000- 00000000 00000000 00000000				MediaLB
006084_H	CSCR4 [R/W] 10------ ----0000 00000000 00000000				
006088_H	CCBCR4 [R] 00000000 00000000 00000000 00000000				
$00608C_H$	CNBCR4 [R/W] 00000000 00000000 00000000 00000000				
006090_H	CECR5 [R/W] 0000000- 00000000 00000000 00000000				
006094_H	CSCR5 [R/W] 10------ ----0000 00000000 00000000				
006098_H	CCBCR5 [R] 00000000 00000000 00000000 00000000				
$00609C_H$	CNBCR5 [R/W] 00000000 00000000 00000000 00000000				
$0060A0_H$	CECR6 [R/W] 0000000- 00000000 00000000 00000000				
$0060A4_H$	CSCR6 [R/W] 10------ ----0000 00000000 00000000				
$0060A8_H$	CCBCR6 [R] 00000000 00000000 00000000 00000000				
$0060AC_H$	CNBCR6 [R/W] 00000000 00000000 00000000 00000000				
$0060B0_H$	CECR7 [R/W] 0000000- 00000000 00000000 00000000				
$0060B4_H$	CSCR7 [R/W] 10------ ----0000 00000000 00000000				
$0060B8_H$	CCBCR7 [R] 00000000 00000000 00000000 00000000				
$0060BC_H$	CNBCR7 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0060C0_H$	CECR8 [R/W] 0000000- 00000000 00000000 00000000				MediaLB
$0060C4_H$	CSCR8 [R/W] 10------ ----0000 00000000 00000000				
$0060C8_H$	CCBCR8 [R] 00000000 00000000 00000000 00000000				
$0060CC_H$	CNBCR8 [R/W] 00000000 00000000 00000000 00000000				
$0060D0_H$	CECR9 [R/W] 0000000- 00000000 00000000 00000000				
$0060D4_H$	CSCR9 [R/W] 10------ ----0000 00000000 00000000				
$0060D8_H$	CCBCR9 [R] 00000000 00000000 00000000 00000000				
$0060DC_H$	CNBCR9 [R/W] 00000000 00000000 00000000 00000000				
$0060E0_H$	CECR10 [R/W] 0000000- 00000000 00000000 00000000				
$0060E4_H$	CSCR10 [R/W] 10------ ----0000 00000000 00000000				
$0060E8_H$	CCBCR10 [R] 00000000 00000000 00000000 00000000				
$0060EC_H$	CNBCR10 [R/W] 00000000 00000000 00000000 00000000				
$0060F0_H$	CECR11 [R/W] 0000000- 00000000 00000000 00000000				
$0060F4_H$	CSCR11 [R/W] 10------ ----0000 00000000 00000000				
$0060F8_H$	CCBCR11 [R] 00000000 00000000 00000000 00000000				
$0060FC_H$	CNBCR11 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006100_H	CECR12 [R/W] 0000000- 00000000 00000000 00000000				MediaLB
006104_H	CSCR12 [R/W] 10------ ----0000 00000000 00000000				
006108_H	CCBCR12 [R] 00000000 00000000 00000000 00000000				
$00610C_H$	CNBCR12 [R/W] 00000000 00000000 00000000 00000000				
006110_H	CECR13 [R/W] 0000000- 00000000 00000000 00000000				
006114_H	CSCR13 [R/W] 10------ ----0000 00000000 00000000				
006118_H	CCBCR13 [R] 00000000 00000000 00000000 00000000				
$00611C_H$	CNBCR13 [R/W] 00000000 00000000 00000000 00000000				
006120_H	CECR14 [R/W] 0000000- 00000000 00000000 00000000				
006124_H	CSCR14 [R/W] 10------ ----0000 00000000 00000000				
006128_H	CCBCR14 [R] 00000000 00000000 00000000 00000000				
$00612C_H$	CNBCR14 [R/W] 00000000 00000000 00000000 00000000				
006130_H to $00627F_H$	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006280_H	LCBCR0 [R/W] 00000000 01000000 00000000 00000000				MediaLB
006284_H	LCBCR1 [R/W] 00000000 01000000 00000000 00000001				
006288_H	LCBCR2 [R/W] 00000000 01000000 00000000 00000010				
$00628C_H$	LCBCR3 [R/W] 00000000 01000000 00000000 00000011				
006290_H	LCBCR4 [R/W] 00000000 01000000 00000000 00000100				
006294_H	LCBCR5 [R/W] 00000000 01000000 00000000 00000101				
006298_H	LCBCR6 [R/W] 00000000 01000000 00000000 00000110				
$00629C_H$	LCBCR7 [R/W] 00000000 01000000 00000000 00000111				
$0062A0_H$	LCBCR8 [R/W] 00000000 01000000 00000000 00001000				
$0062A4_H$	LCBCR9 [R/W] 00000000 01000000 00000000 00001001				
$0062A8_H$	LCBCR10 [R/W] 00000000 01000000 00000000 00001010				
$0062AC_H$	LCBCR11 [R/W] 00000000 01000000 00000000 00001011				
$0062B0_H$	LCBCR12 [R/W] 00000000 01000000 00000000 00001100				
$0062B4_H$	LCBCR13 [R/W] 00000000 01000000 00000000 00001101				
$0062B8_H$	LCBCR14 [R/W] 00000000 01000000 00000000 00001110				
$0062BC_H$ to $00630F_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006310_H	I2SCCR [R/W] 00100000 0----000		I2SRSR [R/W] -------- 00000000		I^2S 0 to 9
006314_H	Reserved				
006318_H	I2SSCR0 [R/W] ----0000 0--00000		I2SBT0 [R] ----0000	I2SBCR0 [R/W] ---00000	I^2S 0
$00631C_H$	LTDT0 [R/W] 00000000 00000000		RTDT0 [R/W] 00000000 00000000		
006320_H	I2SSCR1 [R/W] ----0000 0--00000		I2SBT1 [R] ----0000	I2SBCR1 [R/W] ---00000	I^2S 1
006324_H	LTDT1 [R/W] 00000000 00000000		RTDT1 [R/W] 00000000 00000000		
006328_H	I2SSCR2 [R/W] ----0000 0--00000		I2SBT2 [R] ----0000	I2SBCR2 [R/W] ---00000	I^2S 2
$00632C_H$	LTDT2 [R/W] 00000000 00000000		RTDT2 [R/W] 00000000 00000000		
006330_H	I2SSCR3 [R/W] ----0000 0--00000		I2SBT3 [R] ----0000	I2SBCR3 [R/W] ---00000	I^2S 3
006334_H	LTDT3 [R/W] 00000000 00000000		RTDT3 [R/W] 00000000 00000000		
006338_H	I2SSCR4 [R/W] ----0000 0--00000		I2SBT4 [R] ----0000	I2SBCR4 [R/W] ---00000	I^2S 4
$00633C_H$	LTDT4 [R/W] 00000000 00000000		RTDT4 [R/W] 00000000 00000000		
006340_H	I2SSCR5 [R/W] ----0000 0--00000		I2SBT5 [R] ----0000	I2SBCR5 [R/W] ---00000	I^2S 5
006344_H	LTDT5 [R/W] 00000000 00000000		RTDT5 [R/W] 00000000 00000000		
006348_H	I2SSCR6 [R/W] ----0000 0--00000		I2SBT6 [R] ----0000	I2SBCR6 [R/W] ---00000	I^2S 6
$00634C_H$	LTDT6 [R/W] 00000000 00000000		RTDT6 [R/W] 00000000 00000000		
006350_H	I2SSCR7 [R/W] ----0000 0--00000		I2SBT7 [R] ----0000	I2SBCR7 [R/W] ---00000	I^2S 7
006354_H	LTDT7 [R/W] 00000000 00000000		RTDT7 [R/W] 00000000 00000000		
006358_H	I2SSCR8 [R/W] ----0000 0--00000		I2SBT8 [R] ----0000	I2SBCR8 [R/W] ---00000	I^2S 8
$00635C_H$	LTDT8 [R/W] 00000000 00000000		RTDT8 [R/W] 00000000 00000000		
006360_H	I2SSCR9 [R/W] ----0000 0--00000		I2SBT9 [R] ----0000	I2SBCR9 [R/W] ---00000	I^2S 9
006364_H	LTDT9 [R/W] 00000000 00000000		RTDT9 [R/W] 00000000 00000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006368_H to $00640C_H$	Reserved				Reserved
006410_H	BUFAR0 [R/W] 00000000 00000000 00000000 00000000				MediaLB
006414_H	BUFAR1 [R/W] 00000000 00000000 00000000 00000000				
006418_H	BUFAR2 [R/W] 00000000 00000000 00000000 00000000				
$00641C_H$	BUFAR3 [R/W] 00000000 00000000 00000000 00000000				
006420_H	BUFAR4 [R/W] 00000000 00000000 00000000 00000000				
006424_H	BUFAR5 [R/W] 00000000 00000000 00000000 00000000				
006428_H	BUFAR6 [R/W] 00000000 00000000 00000000 00000000				
$00642C_H$	BUFAR7 [R/W] 00000000 00000000 00000000 00000000				
006430_H	MSTD [R/W] -0000000 00000000		MBSYNC [R] XXXXXXXX XXXXXXXX		
006434_H	BUFAR8 [R/W] 00000000 00000000 00000000 00000000				
006438_H	BUFAR9 [R/W] 00000000 00000000 00000000 00000000				
$00643C_H$	BUFAR10 [R/W] 00000000 00000000 00000000 00000000				
006440_H	BUFAR11 [R/W] 00000000 00000000 00000000 00000000				
006444_H	BUFAR12 [R/W] 00000000 00000000 00000000 00000000				
006448_H	BUFAR13 [R/W] 00000000 00000000 00000000 00000000				
$00644C_H$	BUFAR14 [R/W] 00000000 00000000 00000000 00000000				
006450_H to $00649C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0064A0_H$	ASLR [R/W] 00000000 00000000 00000000 00000000				FIFO buffer
$0064A4_H$	BUFDCR [R/W] 00000000 00000000 00000000 00000000				
$0064A8_H$	BUFIER [R/W] 00000000 00000000 -0000000 00000000				
$0064AC_H$	BUFSR [R/W] 00000000 00000000 -0000000 00000000				
$0064B0_H$	BUFER [R/W] 00000000 00000000 -0000000 00000000				
$0064B4_H$	BUFRST [R/W] 00000000 00000000 -0000000 00000000				
$0064B8_H$, $0064BC_H$	Reserved				
$0064C0_H$	BUFCT0 [R/W] ----0000 00000000 ----0000 00000000				
$0064C4_H$	BUFCT1 [R/W] ----0000 00000000 ----0000 00000000				
$0064C8_H$	BUFCT2 [R/W] ----0000 00000000 ----0000 00000000				
$0064CC_H$	BUFCT3 [R/W] ----0000 00000000 ----0000 00000000				
$0064D0_H$	BUFCT4 [R/W] ----0000 00000000 ----0000 00000000				
$0064D4_H$	BUFCT5 [R/W] ----0000 00000000 ----0000 00000000				
$0064D8_H$	BUFCT6 [R/W] ----0000 00000000 ----0000 00000000				
$0064DC_H$	BUFCT7 [R/W] ----0000 00000000 ----0000 00000000				
$0064E0_H$ to $0064FC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006500_H	BUF0CR [R/W] 00000000 00000000 000----0 00000000				FIFO buffer
006504_H	BUF1CR [R/W] 00000000 00000000 000----0 00000000				
006508_H	BUF2CR [R/W] 00000000 00000000 000----0 00000000				
$00650C_H$	BUF3CR [R/W] 00000000 00000000 000----0 00000000				
006510_H	BUF4CR [R/W] 00000000 00000000 000----0 00000000				
006514_H	BUF5CR [R/W] 00000000 00000000 000----0 00000000				
006518_H	BUF6CR [R/W] 00000000 00000000 000----0 00000000				
$00651C_H$	BUF7CR [R/W] 00000000 00000000 000----0 00000000				
006520_H	BUF8CR [R/W] 00000000 00000000 000----0 00000000				
006524_H	BUF9CR [R/W] 00000000 00000000 000----0 00000000				
006528_H	BUF10CR [R/W] 00000000 00000000 000----0 00000000				
$00652C_H$	BUF11CR [R/W] 00000000 00000000 000----0 00000000				
006530_H	BUF12CR [R/W] 00000000 00000000 000----0 00000000				
006534_H	BUF13CR [R/W] 00000000 00000000 000----0 00000000				
006538_H	BUF14CR [R/W] 00000000 00000000 000----0 00000000				
$00653C_H$ to $00657C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006580_H	BUF0DTR [R/W] 00000000 00000000 00000000 00000000				FIFO buffer
006584_H	BUF1DTR [R/W] 00000000 00000000 00000000 00000000				
006588_H	BUF2DTR [R/W] 00000000 00000000 00000000 00000000				
$00658C_H$	BUF3DTR [R/W] 00000000 00000000 00000000 00000000				
006590_H	BUF4DTR [R/W] 00000000 00000000 00000000 00000000				
006594_H	BUF5DTR [R/W] 00000000 00000000 00000000 00000000				
006598_H	BUF6DTR [R/W] 00000000 00000000 00000000 00000000				
$00659C_H$	BUF7DTR [R/W] 00000000 00000000 00000000 00000000				
$0065A0_H$	BUF8DTR [R/W] 00000000 00000000 00000000 00000000				
$0065A4_H$	BUF9DTR [R/W] 00000000 00000000 00000000 00000000				
$0065A8_H$	BUF10DTR [R/W] 00000000 00000000 00000000 00000000				
$0065AC_H$	BUF11DTR [R/W] 00000000 00000000 00000000 00000000				
$0065B0_H$	BUF12DTR [R/W] 00000000 00000000 00000000 00000000				
$0065B4_H$	BUF13DTR [R/W] 00000000 00000000 00000000 00000000				
$0065B8_H$	BUF14DTR [R/W] 00000000 00000000 00000000 00000000				
$0065BC_H$	Reserved				Reserved
006600_H	MLBINTR [R] -0000-00 00000000 ------00 00000000				MediaLB I^2S FIFO buffer Interrupt
006604_H	BUFINTCH [R] 0---0000		Reserved		
006608_H	BUFPRI0001 [R/W] 11101101	BUFPRI0203 [R/W] 11001011	BUFPRI0405 [R/W] 10101001	BUFPRI0607 [R/W] 10000111	
$00660C_H$	BUFPRI0809 [R/W] 01100101	BUFPRI1011 [R/W] 01000011	BUFPRI1213 [R/W] 00100001	BUFPRI14 [R/W] 0000----	
006610_H to $0067FC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007000_H	FMCS [R/W] 01101000	FMCR [R/W] ---00000	FCHCR [R/W] ------00 10000011		Flash Memory/ Cache Control Register
007004_H	FMWT [R/W] 11111111 01011101		FMWT2 [R/W] -101----	FMPS [R/W] -----000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] -------- -0000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] -------- -0000000 00000000 00000000				
007014_H to $00AFFC_H$	Reserved				Reserved
$00B000_H$ to $00BFFC_H$	Boot ROM area				Boot ROM 4Kbytes
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		CBSYNC0 [R] XXXXXXXX XXXXXXXX		
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$, $00C02C_H$	Reserved				
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
$00C038_H$, $00C03C_H$	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$, $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved				
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved				
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved				
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		CBSYNC1 [R] XXXXXXXX XXXXXXXX		
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$, $00C12C_H$	Reserved				
$00C130_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
$00C134_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
$00C138_H$, $00C13C_H$	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$, $00C15C_H$	Reserved				
$00C160_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
$00C164_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
$00C168_H$ to $00C17C_H$	Reserved				
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN1 Status Flags
$00C184_H$	TREQR41 [R] 00000000 00000000		TREQR31 [R] 00000000 00000000		
$00C188_H$, $00C18C_H$	Reserved				
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$	NEWDT41 [R] 00000000 00000000		NEWDT31 [R] 00000000 00000000		
$00C198_H$, $00C19C_H$	Reserved				
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
$00C1A4_H$	INTPND41 [R] 00000000 00000000		INTPND31 [R] 00000000 00000000		
$00C1A8_H$, $00C1AC_H$	Reserved				
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$	MSGVAL41 [R] 00000000 00000000		MSGVAL31 [R] 00000000 00000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C1B8_H$ to $00C1FC_H$	Reserved				CAN1 Status Flags
$00C200_H$ to $00EFFC_H$	Reserved				Reserved
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ to $00FFFC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00010000_H to $000107FC_H$	TAG RAM (way1)				
00010800_H to $00013FFC_H$	Reserved				Reserved
00014000_H to $000147FC_H$	TAG RAM (way2)				
00014800_H to $00017FFC_H$	Reserved				Reserved
00018000_H to $000187FC_H$	CACHE RAM (way1) / I-RAM (2 Kbytes)				
00018800_H to $0001BFFC_H$	Reserved				Reserved
$0001C000_H$ to $0001C7FC_H$	CACHE RAM (way2) / I-RAM (2 Kbytes)				
$0001C800_H$ to $0001FFFC_H$	Reserved				Reserved
020000_H to $027FFC_H$	Reserved				RAM (64 Kbytes)
024000_H to $02BFFC_H$	D-RAM area (32 Kbytes) (It is not possible to use instruction access, data access is 1 wait cycle)				
$02C000_H$ to $02FFFC_H$	D-RAM area (16 Kbytes) (It is not possible to use instruction access, data access is 0 wait cycle)				
030000_H to $033FFC_H$	I/D-RAM area (16 Kbytes) (instruction access is 0 wait cycles, data access is 1 wait cycle)				
034000_H to $03FFFC_H$	Reserved				

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
040000_H to $05FFFC_H$	ROMS00 area (128 Kbytes)				Flash (1088 Kbytes)
060000_H to $07FFFC_H$	ROMS01 area (128 Kbytes)				
080000_H to $09FFFC_H$	ROMS02 area (128 Kbytes)				
$0A0000_H$ to $0BFFFC_H$	ROMS03 area (128 Kbytes)				
$0C0000_H$ to $0DFFFC_H$	ROMS04 area (128 Kbytes)				
$0E0000_H$ to $0FFFFC_H$	ROMS05 area (128 Kbytes) Mode Vector:$0FFFF8_H$ Reset Vector:$0FFFFC_H$				
100000_H to $13FFFC_H$	ROMS06 area (256 Kbytes)				
140000_H to $14FFFC_H$	ROMS07 area (64 Kbytes)				
150000_H to $17FFFC_H$	Reserved				

Note: It is not allowed to write into $0FFFF8_H$ and $0FFFFC_H$. When these addresses are read, values shown above will be read.

12. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	0_H	—	—	$3FC_H$	$000FFFFC_H$	
Mode vector	1	1_H	—	—	$3F8_H$	$000FFFF8_H$	
System reserved	2	2_H	—	—	$3F4_H$	$000FFFF4_H$	
System reserved	3	3_H	—	—	$3F0_H$	$000FFFF0_H$	
System reserved	4	4_H	—	—	$3EC_H$	$000FFFEC_H$	
CPU supervisor mode (INT #5 instruction)*6	5	5_H	—	—	$3E8_H$	$000FFFE8_H$	
Memory Protection exception	6	6_H	—	—	$3E4_H$	$000FFFE4_H$	
Co-processor fault trap*5	7	7_H	—	—	$3E0_H$	$000FFFE0_H$	
Co-processor error trap*5	8	8_H	—	—	$3DC_H$	$000FFFDC_H$	
INTE instruction*5	9	9_H	—	—	$3D8_{HH}$	$000FFFD8_H$	
Instruction break exception*5	10	$0A_H$	—	—	$3D4_H$	$000FFFD4_H$	
Operand break trap*5	11	$0B_H$	—	—	$3D0_H$	$000FFFD0_H$	
Step trace trap*5	12	$0C_H$	—	—	$3CC_H$	$000FFFCC_H$	
NMI request (tool) *5	13	$0D_H$	—	—	$3C8_H$	$000FFFC8_H$	
Undefined instruction exception	14	$0E_H$	—	—	$3C4_H$	$000FFFC4_H$	
NMI request	15	$0F_H$	F_H fixed		$3C0_H$	$000FFFC0_H$	
External Interrupt 0	16	10_H	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11_H			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12_H	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13_H			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14_H	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15_H			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16_H	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17_H			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18_H	ICR04	444_H	$39C_H$	$000FFF9C_H$	
External Interrupt 9	25	19_H			398_H	$000FFF98_H$	
External Interrupt 10	26	$1A_H$	ICR05	445_H	394_H	$000FFF94_H$	
External Interrupt 11	27	$1B_H$			390_H	$000FFF90_H$	
External Interrupt 12	28	$1C_H$	ICR06	446_H	$38C_H$	$000FFF8C_H$	
External Interrupt 13	29	$1D_H$			388_H	$000FFF88_H$	
External Interrupt 14	30	$1E_H$	ICR07	447_H	384_H	$000FFF84_H$	
External Interrupt 15	31	$1F_H$			380_H	$000FFF80_H$	

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 0	32	20_H	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21_H			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22_H	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23_H			370_H	$000FFF70_H$	35
Reserved	36	24_H	ICR10	$44A_H$	$36C_H$	$000FFF6C_H$	
Reserved	37	25_H			368_H	$000FFF68_H$	
Reserved	38	26_H	ICR11	$44B_H$	364_H	$000FFF64_H$	
Reload Timer 7	39	27_H			360_H	$000FFF60_H$	
Free Run Timer 0	40	28_H	ICR12	$44C_H$	$35C_H$	$000FFF5C_H$	40
Free Run Timer 1	41	29_H			358_H	$000FFF58_H$	41
Free Run Timer 2	42	$2A_H$	ICR13	$44D_H$	354_H	$000FFF54_H$	42
Free Run Timer 3	43	$2B_H$			350_H	$000FFF50_H$	43
Reserved	44	$2C_H$	ICR14	$44E_H$	$34C_H$	$000FFF4C_H$	
Reserved	45	$2D_H$			348_H	$000FFF48_H$	
Reserved	46	$2E_H$	ICR15	$44F_H$	344_H	$000FFF44_H$	
Reserved	47	$2F_H$			340_H	$000FFF40_H$	
CAN 0	48	30_H	ICR16	450_H	$33C_H$	$000FFF3C_H$	
CAN 1	49	31_H			338_H	$000FFF38_H$	
Reserved	50	32_H	ICR17	451_H	334_H	$000FFF34_H$	
Reserved	51	33_H			330_H	$000FFF30_H$	
Reserved	52	34_H	ICR18	452_H	$32C_H$	$000FFF2C_H$	
Reserved	53	35_H			328_H	$000FFF28_H$	
LIN-USART0 RX	54	36_H	ICR19	453_H	324_H	$000FFF24_H$	6, 48
LIN-USART0 TX	55	37_H			320_H	$000FFF20_H$	7, 49
LIN-USART1 RX	56	38_H	ICR20	454_H	$31C_H$	$000FFF1C_H$	8, 50
LIN-USART1 TX	57	39_H			318_H	$000FFF18_H$	9, 51
LIN-USART2 RX	58	$3A_H$	ICR21	455_H	314_H	$000FFF14_H$	52
LIN-USART2 TX	59	$3B_H$			310_H	$000FFF10_H$	53
LIN-USART3 RX	60	$3C_H$	ICR22	456_H	$30C_H$	$000FFF0C_H$	54
LIN-USART3 TX	61	$3D_H$			308_H	$000FFF08_H$	55
System reserved	62	$3E_H$	ICR23*4	457_H	304_H	$000FFF04_H$	
Delayed Interrupt	63	$3F_H$			300_H	$000FFF00_H$	

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved *3	64	40_H	(ICR24)	(458_H)	$2FC_H$	$000FFEFC_H$	
System reserved *3	65	41_H			$2F8_H$	$000FFEF8_H$	
LIN-USART (FIFO) 4 RX	66	42_H	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10, 56
LIN-USART (FIFO) 4 TX	67	43_H			$2F0_H$	$000FFEF0_H$	11, 57
LIN-USART (FIFO) 5 RX	68	44_H	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12, 58
LIN-USART (FIFO) 5 TX	69	45_H			$2E8_H$	$000FFEE8_H$	13, 59
LIN-USART (FIFO) 6 RX	70	46_H	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	60
LIN-USART (FIFO) 6 TX	71	47_H			$2E0_H$	$000FFEE0_H$	61
LIN-USART (FIFO) 7 RX	72	48_H	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	62
LIN-USART (FIFO) 7 TX	73	49_H			$2D8_H$	$000FFED8_H$	63
I^2C 0 / I^2C 2	74	$4A_H$	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	
I^2C 1 / I^2C 3	75	$4B_H$			$2D0_H$	$000FFED0_H$	
LIN-USART (LIN) 8 RX	76	$4C_H$	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
LIN-USART (LIN) 8 TX	77	$4D_H$			$2C8_H$	$000FFEC8_H$	65
I^2C 4 / I^2C 6	78	$4E_H$	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	
I^2C 5 / I^2C 7	79	$4F_H$			$2C0_H$	$000FFEC0_H$	
Reserved	80	50_H	ICR32	460_H	$2BC_H$	$000FFEBC_H$	
Reserved	81	51_H			$2B8_H$	$000FFEB8_H$	
FIFO buffer	82	52_H	ICR33	461_H	$2B4_H$	$000FFEB4_H$	
Reserved	83	53_H			$2B0_H$	$000FFEB0_H$	
Reserved	84	54_H	ICR34	462_H	$2AC_H$	$000FFEAC_H$	
Reserved	85	55_H			$2A8_H$	$000FFEA8_H$	
Reserved	86	56_H	ICR35	463_H	$2A4_H$	$000FFEA4_H$	
Reserved	87	57_H			$2A0_H$	$000FFEA0_H$	
MediaLB	88	58_H	ICR36	464_H	$29C_H$	$000FFE9C_H$	
I^2S ERROR	89	59_H			298_H	$000FFE98_H$	
I^2S EVEN	90	$5A_H$	ICR37	465_H	294_H	$000FFE94_H$	125
I^2S ODD	91	$5B_H$			290_H	$000FFE90_H$	126
Input Capture 0	92	$5C_H$	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	$5D_H$			288_H	$000FFE88_H$	81
Input Capture 2	94	$5E_H$	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	$5F_H$			280_H	$000FFE80_H$	83

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	96	60_H	ICR40	468_H	$27C_H$	$000FFE7C_H$	
Reserved	97	61_H			278_H	$000FFE78_H$	
Reserved	98	62_H	ICR41	469_H	274_H	$000FFE74_H$	
Reserved	99	63_H			270_H	$000FFE70_H$	
Output Compare 0	100	64_H	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	88
Output Compare 1	101	65_H			268_H	$000FFE68_H$	89
Output Compare 2	102	66_H	ICR43	$46B_H$	264_H	$000FFE64_H$	90
Output Compare 3	103	67_H			260_H	$000FFE60_H$	91
Reserved	104	68_H	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	
Reserved	105	69_H			258_H	$000FFE58_H$	
Reserved	106	$6A_H$	ICR45	$46D_H$	254_H	$000FFE54_H$	
Reserved	107	$6B_H$			250_H	$000FFE50_H$	
Reserved	108	$6C_H$	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	
Reserved	109	$6D_H$			248_H	$000FFE48_H$	
Reserved	110	$6E_H$	ICR47*4	$46F_H$	244_H	$000FFE44_H$	
Reserved	111	$6F_H$			240_H	$000FFE40_H$	
PPG0	112	70_H	ICR48	470_H	$23C_H$	$000FFE3C_H$	15, 96
PPG1	113	71_H			238_H	$000FFE38_H$	97
PPG2	114	72_H	ICR49	471_H	234_H	$000FFE34_H$	98
PPG3	115	73_H			230_H	$000FFE30_H$	99
PPG4	116	74_H	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG5	117	75_H			228_H	$000FFE28_H$	101
PPG6	118	76_H	ICR51	473_H	224_H	$000FFE24_H$	102
PPG7	119	77_H			220_H	$000FFE20_H$	103
Reserved	120	78_H	ICR52	474_H	$21C_H$	$000FFE1C_H$	
Reserved	121	79_H			218_H	$000FFE18_H$	
Reserved	122	$7A_H$	ICR53	475_H	214_H	$000FFE14_H$	
Reserved	123	$7B_H$			210_H	$000FFE10_H$	
Reserved	124	$7C_H$	ICR54	476_H	$20C_H$	$000FFE0C_H$	
Reserved	125	$7D_H$			208_H	$000FFE08_H$	
Reserved	126	$7E_H$	ICR55	477_H	204_H	$000FFE04_H$	
Reserved	127	$7F_H$			200_H	$000FFE00_H$	
Reserved	128	80_H	ICR56	478_H	$1FC_H$	$000FFDFC_H$	
Reserved	129	81_H			$1F8_H$	$000FFDF8_H$	

(Continued)

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	130	82_H	ICR57	479_H	$1F4_H$	$000FFDF4_H$	
Reserved	131	83_H			$1F0_H$	$000FFDF0_H$	
Real Time Clock	132	84_H	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	
Calibration Unit	133	85_H			$1E8_H$	$000FFDE8_H$	
A/D Converter 0	134	86_H	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
Reserved	135	87_H			$1E0_H$	$000FFDE0_H$	
Reserved	136	88_H	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	
Reserved	137	89_H			$1D8_H$	$000FFDD8_H$	
Low Voltage Detection	138	$8A_H$	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	
Reserved	139	$8B_H$			$1D0_H$	$000FFDD0_H$	
Timebase Overflow	140	$8C_H$	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	
PLL Clock Gear	141	$8D_H$			$1C8_H$	$000FFDC8_H$	
DMA Controller	142	$8E_H$	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	
Main/Sub OSC stability wait	143	$8F_H$			$1C0_H$	$000FFDC0_H$	
Reserved	144	90_H	—	—	$1BC_H$	$000FFDBC_H$	
Used by the INT instruction.	145 to 255	91_H to FF_H	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	

*1 : The ICRs set the interrupt level for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset.

*3 : Used by REALOS.

*4 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0xC03 : IOS[0])

*5 : System reserved.

*6 : Memory Protection Unit (MPU) support.

13. Recommended Settings

13.1 PLL and Clockgear settings

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

13.2 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a center clock frequency range from 32MHz up to 80 MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to center clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	$026F_H$	72	65.5	79.9	
1	3	$026F_H$	68	62	75.3	
1	3	$026F_H$	64	58.5	70.7	
1	5	$02AE_H$	64	55.3	75.9	
2	3	$046E_H$	64	55.3	75.9	
1	3	$026F_H$	60	54.9	66.1	
1	5	$02AE_H$	60	51.9	71	
1	7	$02ED_H$	60	49.3	76.7	
2	3	$046E_H$	60	51.9	71	
3	3	$066D_H$	60	49.3	76.7	
1	3	$026F_H$	56	51.4	61.6	
1	5	$02AE_H$	56	48.6	66.1	
1	7	$02ED_H$	56	46.1	71.4	
1	9	$032C_H$	56	43.8	77.6	
2	3	$046E_H$	56	48.6	66.1	
2	5	$04AC_H$	56	43.8	77.6	
3	3	$066D_H$	56	46.1	71.4	
4	3	$086C_H$	56	43.8	77.6	
1	3	$026F_H$	52	47.8	57	
1	5	$02AE_H$	52	45.2	61.2	
1	7	$02ED_H$	52	42.9	66.1	
1	9	$032C_H$	52	40.8	71.8	
1	11	$036B_H$	52	38.8	78.6	
2	3	$046E_H$	52	45.2	61.2	
2	5	$04AC_H$	52	40.8	71.8	
3	3	$066D_H$	52	42.9	66.1	
4	3	$086C_H$	52	40.8	71.8	
5	3	$0A6B_H$	52	38.8	78.6	
1	3	$026F_H$	48	44.2	52.5	
1	5	$02AE_H$	48	41.8	56.4	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	7	$02ED_H$	48	39.6	60.9	
1	9	$032C_H$	48	37.7	66.1	
1	11	$036B_H$	48	35.9	72.3	
1	13	$03AA_H$	48	34.3	79.9	
2	3	$046E_H$	48	41.8	56.4	
2	5	$04AC_H$	48	37.7	66.1	
2	7	$04EA_H$	48	34.3	79.9	
3	3	$066D_H$	48	39.6	60.9	
3	5	$06AA_H$	48	34.3	79.9	
4	3	$086C_H$	48	37.7	66.1	
5	3	$0A6B_H$	48	35.9	72.3	
6	3	$0C6A_H$	48	34.3	79.9	
1	3	$026F_H$	44	40.6	48.1	
1	5	$02AE_H$	44	38.4	51.6	
1	7	$02ED_H$	44	36.4	55.7	
1	9	$032C_H$	44	34.6	60.4	
1	11	$036B_H$	44	33	66.1	
1	13	$03AA_H$	44	31.5	73	
2	3	$046E_H$	44	38.4	51.6	
2	5	$04AC_H$	44	34.6	60.4	
2	7	$04EA_H$	44	31.5	73	
3	3	$066D_H$	44	36.4	55.7	
3	5	$06AA_H$	44	31.5	73	
4	3	$086C_H$	44	34.6	60.4	
5	3	$0A6B_H$	44	33	66.1	
6	3	$0C6A_H$	44	31.5	73	
1	3	$026F_H$	40	37	43.6	
1	5	$02AE_H$	40	34.9	46.8	
1	7	$02ED_H$	40	33.1	50.5	
1	9	$032C_H$	40	31.5	54.8	
1	11	$036B_H$	40	30	59.9	
1	13	$03AA_H$	40	28.7	66.1	
1	15	$03E9_H$	40	27.4	73.7	
2	3	$046E_H$	40	34.9	46.8	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	5	$04AC_H$	40	31.5	54.8	
2	7	$04EA_H$	40	28.7	66.1	
3	3	$066D_H$	40	33.1	50.5	
3	5	$06AA_H$	40	28.7	66.1	
4	3	$086C_H$	40	31.5	54.8	
5	3	$0A6B_H$	40	30	59.9	
6	3	$0C6A_H$	40	28.7	66.1	
7	3	$0E69_H$	40	27.4	73.7	
1	3	$026F_H$	36	33.3	39.2	
1	5	$02AE_H$	36	31.5	42	
1	7	$02ED_H$	36	29.9	45.3	
1	9	$032C_H$	36	28.4	49.2	
1	11	$036B_H$	36	27.1	53.8	
1	13	$03AA_H$	36	25.8	59.3	
1	15	$03E9_H$	36	24.7	66.1	
2	3	$046E_H$	36	31.5	42	
2	5	$04AC_H$	36	28.4	49.2	
2	7	$04EA_H$	36	25.8	59.3	
2	9	0528_H	36	23.7	74.7	
3	3	$066D_H$	36	29.9	45.3	
3	5	$06AA_H$	36	25.8	59.3	
4	3	$086C_H$	36	28.4	49.2	
4	5	$08A8_H$	36	23.7	74.7	
5	3	$0A6B_H$	36	27.1	53.8	
6	3	$0C6A_H$	36	25.8	59.3	
7	3	$0E69_H$	36	24.7	66.1	
8	3	1068_H	36	23.7	74.7	
1	3	$026F_H$	32	29.7	34.7	
1	5	$02AE_H$	32	28	37.3	
1	7	$02ED_H$	32	26.6	40.2	
1	9	$032C_H$	32	25.3	43.6	
1	11	$036B_H$	32	24.1	47.7	
1	13	$03AA_H$	32	23	52.5	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	$03E9_H$	32	22	58.6	
2	3	$046E_H$	32	28	37.3	
2	5	$04AC_H$	32	25.3	43.6	
2	7	$04EA_H$	32	23	52.5	
2	9	0528_H	32	21.1	66.1	
3	3	$066D_H$	32	26.6	40.2	
3	5	$06AA_H$	32	23	52.5	
3	7	$06E7_H$	32	20.3	75.9	
4	3	$086C_H$	32	25.3	43.6	
4	5	$08A8_H$	32	21.1	66.1	
5	3	$0A6B_H$	32	24.1	47.7	
6	3	$0C6A_H$	32	23	52.5	
7	3	$0E69_H$	32	22	58.6	
8	3	1068_H	32	21.1	66.1	
9	3	1267_H	32	20.3	75.9	

14. Electrical Characteristics

14.1 Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}3$	V_{SS} − 0.5	V_{SS} + 4.0	V	$V_{CC}5 \geq V_{CC}3$
	$V_{CC}5$	V_{SS} − 0.5	V_{SS} + 6.0	V	$V_{CC}5 \geq V_{CC}3$
	$AV_{CC}3$	V_{SS} − 0.5	V_{SS} + 4.0	V	$V_{CC}3 \geq AV_{CC}3 \geq AVRH$
	AVRH	V_{SS} − 0.5	V_{SS} + 4.0	V	$V_{CC}3 \geq AVRH$
Input voltage 1*1	V_{I1}	V_{SS} − 0.3	$V_{CC}3$ + 0.3	V	3 V pin group
Input voltage 2*1	V_{I2}	V_{SS} − 0.3	$V_{CC}5$ + 0.3	V	5 V pin group
Analog pin input voltage	V_{IA}	V_{SS} − 0.3	$AV_{CC}3$ + 0.3	V	
Output voltage 1*1	V_{O1}	V_{SS} − 0.3	$V_{CC}3$ + 0.3	V	3 V pin group
Output voltage 2*1	V_{O2}	V_{SS} − 0.3	$V_{CC}5$ + 0.3	V	5 V pin group
Maximum clamp current (+B input)	I_{CLAMP}	−2	2	mA	*2
Total maximum clamp current (+B input)	ΣI_{CLAMP}	−20	20	mA	*2
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	−10	mA	*3
“H” level average output current	I_{OHAV}	—	−4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	−50	mA	
“H” level total average output current	ΣI_{OHAV}	—	−20	mA	*5
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	−40	+ 105	°C	
Storage temperature	Tstg	−55	+ 150	°C	

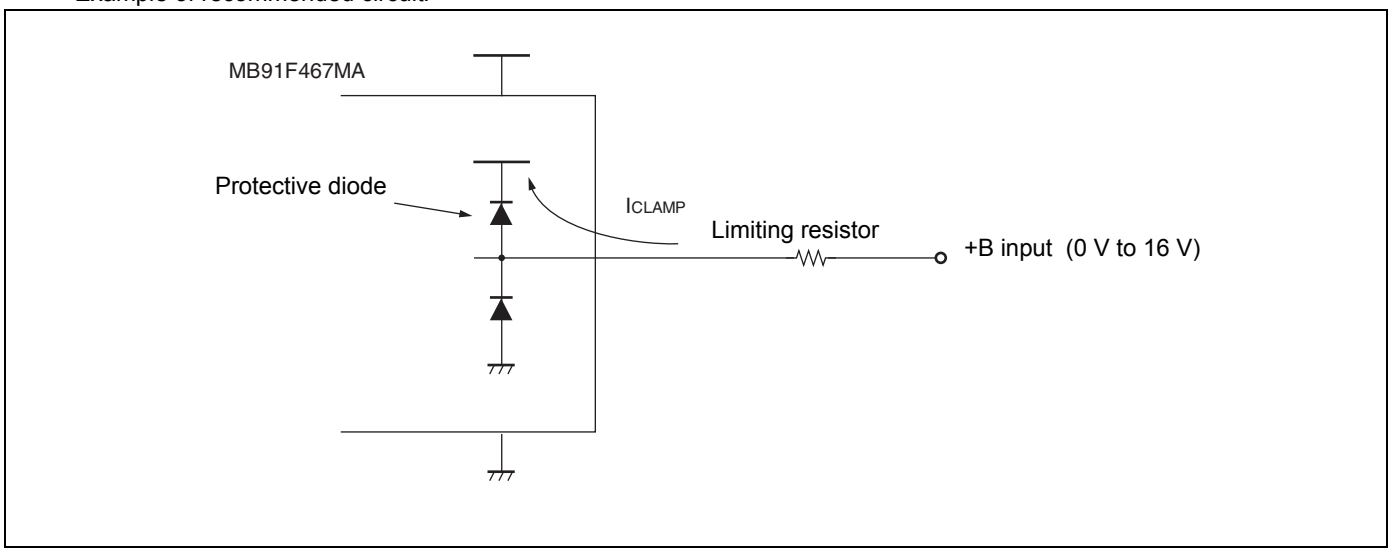
*1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V

*2 :
- This is a 5 V pin which works as a port or serves with a port.
- Use within recommended operating conditions.
- Use with DC voltage (current).
- The standard value of +B input is defined as the power supply flowing through any one of the corresponding pins.
- +B signals are input signals that exceed the $V_{CC}5$ voltage.
  Connect limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time , either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin VCC5, VCC3 via a protective diode, possibly affecting other devices.

(Continued)

(Continued)

- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit:



*3 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period. The average value is the operation current × the operation ratio.

*5 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period. The average value is the operation current × the operation ratio.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended operating conditions

(V_{SS} = AV_{SS} = 0.0 V)

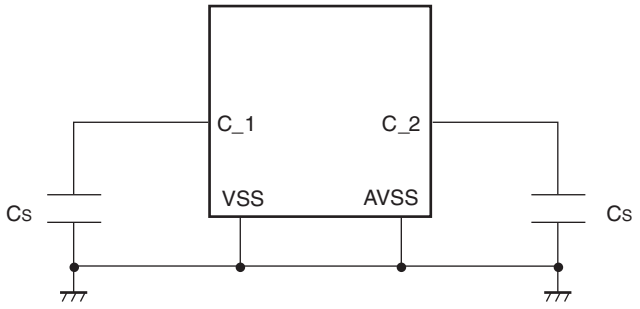
Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}5$	3.0	5.5	V	5 V operation guarantee range
	$V_{CC}3$	3.0	3.6	V	3 V operation guarantee range
	$AV_{CC}3$	3.0	3.6	V	Analog operation guarantee range
Smoothing capacitor at C_1, C_2 pin	C_S	4.7 (accuracy within ± 50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC5, VCC3 pins.
Power supply slew rate	—	1	50	V/ms	
Operating temperature	T_A	–40	+ 105	°C	
Main oscillation stabilization time	—	8	—	ms	
Look-up time PLL (4 MHz→16 ...80 MHz)	—	—	0.6	ms	
ESD Protection (Human body model)	Vsurge	2	—	kV	$R_{discharge}$ = 1.5 kΩ Cdischarge = 100 pF
RC Oscillator	fRC100kHz	50	200	kHz	
	fRC2MHz	1	4	MHz	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

C Pin Connection Diagram



14.3 DC characteristics

(T_A = –40°C to + 105°C, $V_{CC}5$ = 5.0 V ± 10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	CMOS-hys	—	0.8 $V_{CC}5$/3	—	$V_{CC}5$/3 + 0.3	V	CMOS hysteresis input pin
	V_{IH2}	CMOS-hys	—	0.7 $V_{CC}5$/3	—	$V_{CC}5$/3 + 0.3	V	CMOS hysteresis input pin
	V_{IH3}	CMOS	—	0.7 $V_{CC}5$	—	$V_{CC}5$ + 0.3	V	CMOS input pin
	V_{IH4}	Automotive	—	0.8 $V_{CC}5$	—	$V_{CC}5$ + 0.3	V	Automotive input pin
	V_{IH5}	MediaLB	—	1.7	—	$V_{CC}3$ + 0.3	V	MediaLB input pin
	V_{IHM}	MD4 to MD0	—	$V_{CC}5$ - 0.3	—	$V_{CC}5$ + 0.3	V	
	V_{IHX5}	INITX	—	0.8 $V_{CC}5$	—	$V_{CC}5$ + 0.3	V	
	V_{IHX3}	X0, X1, X0A, X1A, TRSTX	—	0.8 $V_{CC}3$	—	$V_{CC}3$ + 0.3	V	TRSTX can withstand 5 V.
"L" level input voltage	V_{IL1}	CMOS-hys	—	V_{SS} - 0.3	—	0.2 $V_{CC}5$/3	V	CMOS hysteresis input pin
	V_{IL2}	CMOS-hys	—	V_{SS} - 0.3	—	0.3 $V_{CC}5$/3	V	CMOS hysteresis input pin
	V_{IL3}	CMOS	—	V_{SS} - 0.3	—	0.3 $V_{CC}5$/3	V	CMOS input pin
	V_{IL4}	Automotive	—	V_{SS} - 0.3	—	0.5 $V_{CC}5$	V	Automotive input pin
	V_{IL5}	MediaLB	—	V_{SS} - 0.3	—	0.7	V	MediaLB input pin
	V_{ILM}	MD4 to MD0	—	V_{SS} - 0.3	—	V_{SS} + 0.3	V	MD pin
	V_{ILX5}	INITX	—	V_{SS} - 0.3	—	0.2 $V_{CC}5$	V	
	V_{ILX3}	X0, X1, X0A, X1A, TRSTX	—	V_{SS} - 0.3	—	0.2 $V_{CC}3$	V	

(Continued)

(T_A = –40°C to + 105°C, $V_{CC}5$ = 5.0 V ± 10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	VCC3	At Main RUN	—	110	140	mA	Core : 80 MHz Peripheral : 20 MHz External bus : 40 MHz CAN : 20 MHz MediaLB : 28 MHz (No load on the external bus)
	I_{CCS}	VCC3	At Main SLEEP	—	30	55	mA	Core : 80 MHz Peripheral : 20 MHz External bus : 40 MHz CAN : 20 MHz MediaLB : 28 MHz (No load on the external bus)
	I_{CCH}	VCC5, VCC3	T_A = + 25°C, $V_{CC}5$ = 5 V, $V_{CC}3$ = 3.3 V, At STOP mode	—	0.1	1	mA	Main oscillation/PLL stop Sub oscillation stop Main regulator stop Low voltage detector stop
	I_{CCHS}	VCC5, VCC3	T_A = + 25°C, $V_{CC}5$ = 5 V, $V_{CC}3$ = 3.3 V, At shutdown	—	10	50	µA	Shutdown mode Low voltage detector stop
	I_{CCL}	VCC3	Operation frequency F_{CP} = 32 kHz, T_A = + 25°C, $V_{CC}3$ = 3.3 V, At Sub RUN	—	1	2	mA	Main oscillation/PLL stop Low voltage detector stop
	I_{CTS4M1}	VCC3	Main clock frequency = 4 MHz, T_A = + 25°C, $V_{CC}3$ = 3.3 V, At stop (Real Time Clock Operation)	—	500	1000	µA	PLL/Sub oscillation stop Low voltage detector stop
	$I_{CTS32K1}$	VCC3	Sub clock frequency = 32 kHz, T_A = + 25°C, $V_{CC}3$ = 3.3 V At stop (Real Time Clock Operation)	—	200	700	µA	Main oscillation/PLL stop Low voltage detector stop
	I_{CTS4M2}	VCC3	Main clock frequency = 4 MHz, T_A = + 25°C, $V_{CC}3$ = 3.3 V, At stop (Real Time Clock Operation)	—	650	1150	µA	PLL/Sub oscillation stop
	$I_{CTS32K2}$	VCC3	Sub clock frequency = 32 kHz, T_A = + 25°C, $V_{CC}3$ = 3.3 V At stop (Real Time Clock Operation)	—	350	850	µA	Main oscillation/PLL stop

* : Power supply current is obtained when an external clock is supplied from X1/X1A pins.

(Continued)

(Continued)

(T_A = –40°C to + 105°C, $V_{CC}5$ = 5.0 V ± 10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	$V_{CC}5$ = 5 V $V_{CC}3$ = $AV_{CC}3$ = 3.3 V $V_{SS} < V_I < V_{CC}5/3$	–5	—	+ 5	µA	
Input capacitance 1	C_{IN}	Other than VCC5, VCC3, VSS, AVCC3, AVSS, AVRH, C_1, C_2	—	—	5	15	pF	
Pull-up resistance	R_{UP}	INITX, Pins with pull-up resistance	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	Pins with pull-down resistance	—	25	50	100	kΩ	
Output “H” voltage	V_{OH1}	5/3 V pin	$V_{CC}5$ = 5.0 V, I_{OH} = –5.0 mA $V_{CC}5$ = 3.3 V, I_{OH} = –2.0 mA	$V_{CC}5$ − 0.5	—	—	V	
	V_{OH2}	3 V pin	$V_{CC}3$ = 3.3 V, I_{OH} = –4.0 mA	$V_{CC}3$ − 0.5	—	—	V	
	V_{OH3}	MediaLB pin	$V_{CC}3$ = 3.3 V, I_{OH} = –6.0 mA	2.0	—	—	V	
Output “L” voltage	V_{OL1}	5/3 Vpin	$V_{CC}5$ = 5.0 V, I_{OL} = 5.0 mA $V_{CC}5$ = 3.3 V, I_{OL} = 2.0 mA	—	—	0.4	V	
	V_{OL2}	3 Vpin	$V_{CC}3$ = 3.3 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL3}	MediaLB pin	$V_{CC}3$ = 3.3 V, I_{OL} = 6.0 mA	—	—	0.4	V	

14.4 A/D converter characteristics

14.4.1 Electrical Characteristics

(T_A = –40°C to + 105°C, $V_{CC}3 = AV_{CC}3$ = 3.3 V ± 10%, $V_{SS} = AV_{SS}$ = 0.0 V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	Bit	
Total error	—	—	—	—	±3	LSB	$AV_{CC}3$ = 3.3 V AVRH = 3.3 V
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN11	AV_{SS} − 1.5LSB	AV_{SS} + 0.5LSB	AV_{SS} + 2.5LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN11	AVRH − 3.5LSB	AVRH − 1.5LSB	AVRH + 0.5LSB	V	
Sampling time	t_{SMP}	—	1000	—	—	ns	At R_{EXT} < 4.2 kΩ *1
Compare time	t_{CMP}	—	2200	—	—	ns	
A/D conversion time	t_{CNV}	—	3	—	1000	µs	$t_{SMP} + t_{CMP}$
Analog port input current	I_{AIN}	AN0 to AN11	—	—	10	µA	$AV_{CC}3 \geq V_{AIN} \geq AV_{SS}$
Analog input voltage	V_{AIN}	AN0 to AN11	AV_{SS}	—	AVRH	V	
Reference voltage	AVR +	AVRH	AV_{SS}	—	$AV_{CC}3$	V	
Power supply current	I_A	AVCC3	—	1.9	3.7	mA	
	I_{AH}		—	—	5	µA	*2
Reference voltage current	I_R	AVRH	—	500	900	µA	AVRH = 3.3 V
	I_{RH}	AVRH	—	—	5	µA	*2
Analog input equivalent capacitance	C_{SH}	AN0 to AN11	—	—	8.5	pF	
Analog input equivalent resistance	R_{IN}	AN0 to AN11	—	—	12.1	kΩ	
Offset between input channels	—	AN0 to AN11	—	—	5	LSB	

*1 : Assuming that output impedance at external analog signal source is 4.2 kΩ or less. If output impedance is more than 4.2 kΩ, it is necessary to take a long sampling time.
Set $t_{CNV} \leq t_{SMP} + t_{CMP}$ for actual use.

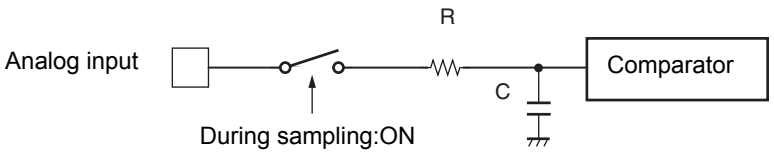
*2 : Assuming that A/D converter is inactive and power supply current is in CPU stop mode ($V_{CC}3 = AV_{CC}3$ = AVRH = 3.3 V)

Note:

< About the external impedance of analog input and its sampling time >

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model



R	C
12.1 kΩ (max)	8.5 pF(max)

Note: The values are reference values.

To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

<Countermeasure for noise which generates on reference power supply>

We recommend to put some µF of bypass capacitor into the reference power supply (AVRH pin).

<About errors>

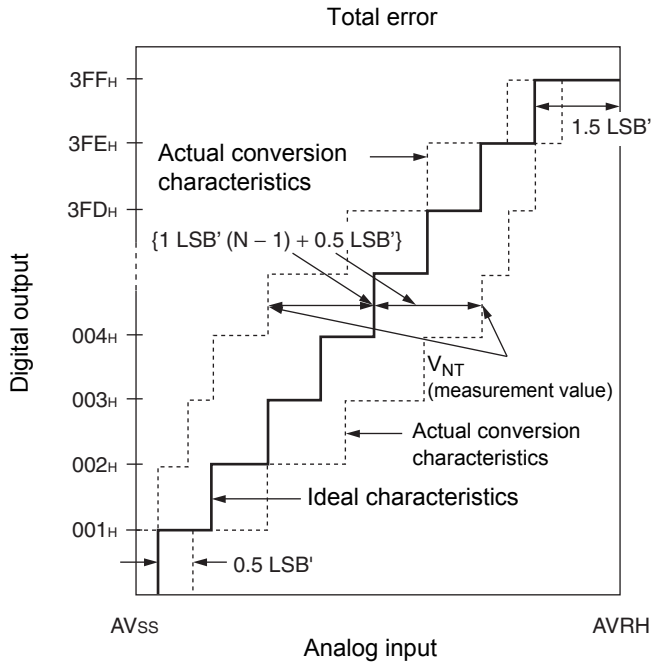
As |AVRH-AV_{SS}| becomes smaller, values of relative errors grow larger.

<Other>

- When inserting a capacitor for blocking direct current between an external circuit and an input pin, set the capacitance value to approximately some thousand times of C_{SH} in order to suppress any influence by the voltage divided depending on chip's internal sampling capacitance C_{SH}.

Definition of A/D converter terms

- Resolution
  Analog variation that is recognizable by the A/D converter.
- Nonlinearity error
  Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).
- Differential nonlinearity error
  Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error
  This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



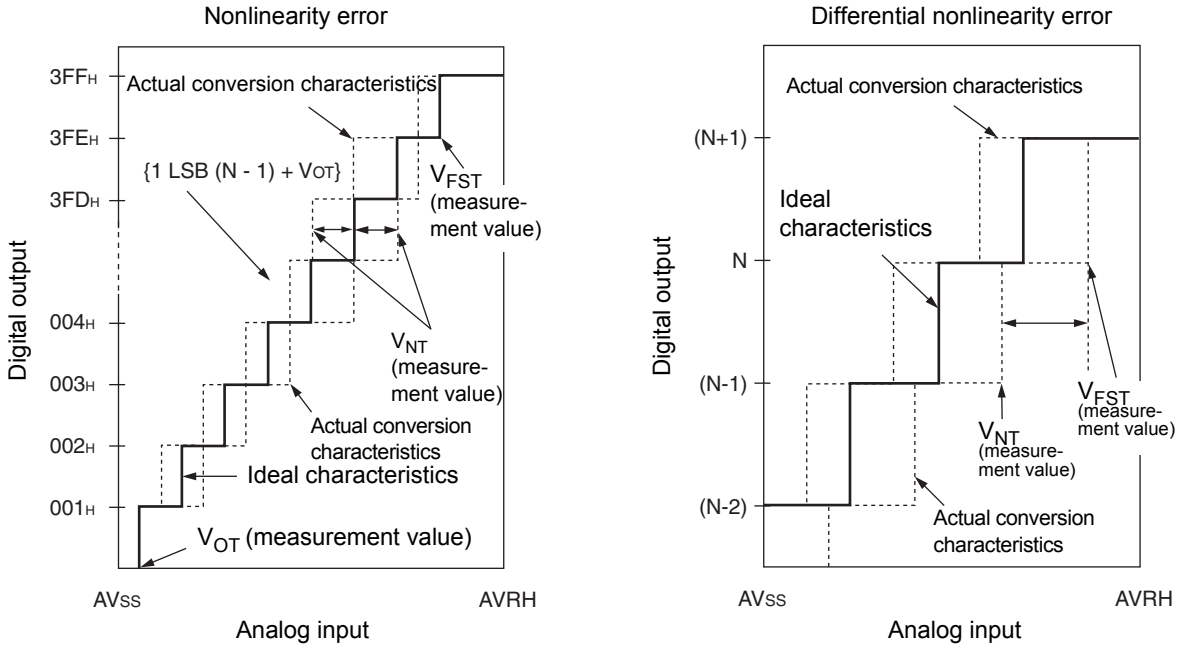
$$1LSB'\ (\text{ideal value}) = \frac{AVRH - AV_{SS}}{1024}\ [V]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = AV_{SS} + 0.5 LSB' [V]
V_{FST}' (ideal value) = AVRH − 1.5 LSB' [V]
V_{NT} : Voltage at which the digital output changes from (N + 1) to N

(Continued)

(Continued)



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

14.5 FLASH memory program/erase characteristics

(T_A = + 25°C, $V_{CC}5$ = 5.0 V, $V_{CC}3$ = 3.3 V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.5	—	s	Erasure programming time not included
Chip erase time	—	n*0.5	—	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	—	6	—	µs	System overhead time not included
Programme/Erase cycle	10000	—	—	cycle	
Flash data retention time	10	—	—	year	*

*: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at + 85°C).

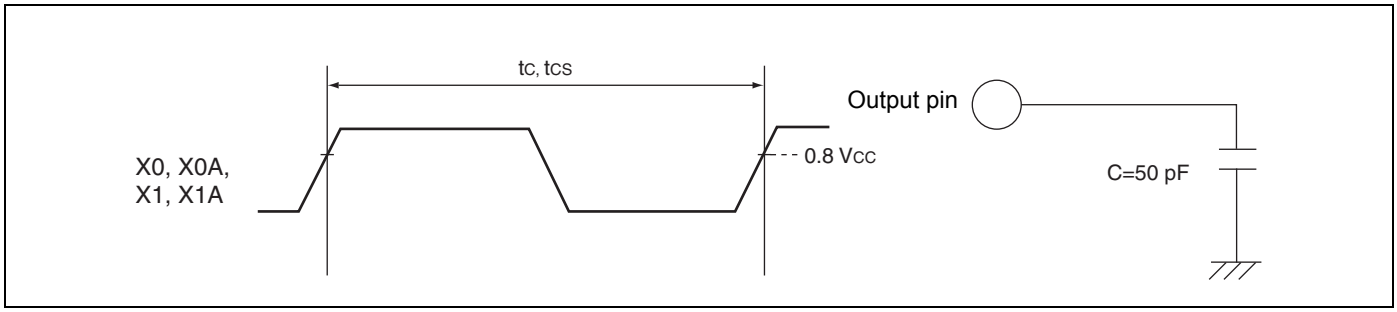
14.6 AC characteristics

14.6.1 Clock timing

($V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.4	—	4.2	MHz	Main clock
Clock cycle time	t_C	X0 X1	238	—	294	ns	
Clock frequency	f_{CS}	X0A X1A	32	—	100	kHz	Sub clock
Clock cycle time	t_{CS}	X0A X1A	10	—	31.25	µs	
Internal operation clock frequency	f_{CP}	—	0.032	—	80	MHz	CPU
	f_{CPP}		0.032	—	20	MHz	Peripheral
	f_{CPT}		0.032	—	40	MHz	External bus
	f_{CAN}		—	—	20	MHz	Clock after division by CAN prescaler
	f_{MLB}		—	—	26	MHz	MediaLB
Internal operation clock cycle time	t_{CP}	—	12.5	—	31250	ns	CPU
	t_{CPP}		50	—	31250	ns	Peripheral
	t_{CPT}		25	—	31250	ns	External bus
	t_{CAN}		50	—	—	ns	Clock after division by CAN prescaler
	t_{MLB}		38.5	—	—	ns	MediaLB

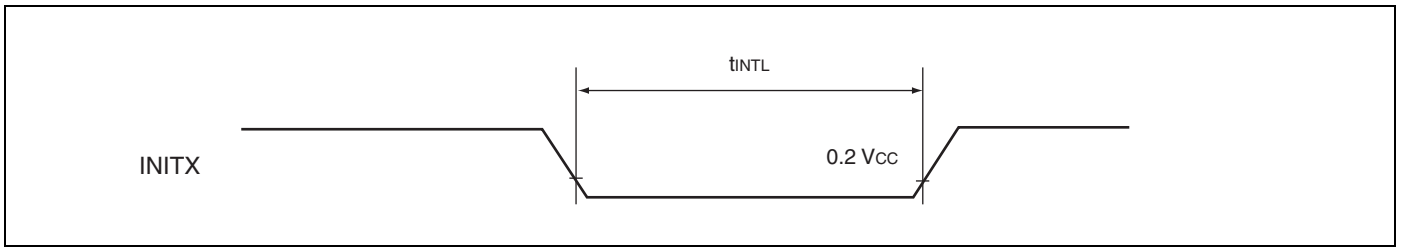
Clock timing condition



14.6.2 Reset input ratings

($V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on, when returning from shutdown)	t_{INTL}	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	µs



14.6.3 Interrupt characteristics for recover from shutdown

($V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40°C to + 105°C)

Parameter	Condition	Value		Unit
		Min	Max	
Interrupt input time (If using level interrupt during recover from shutdown)	—	500	—	µs

14.6.4 LIN-USART

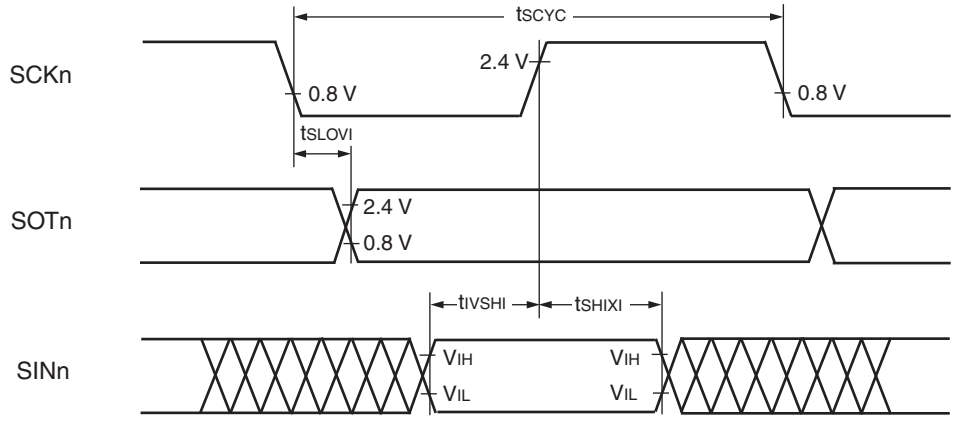
Bit setting : ESCR : SCES = 0, ECCR : SCDE = 0

(T_A = –40°C to + 105°C, $V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, Vss = 0.0 V)

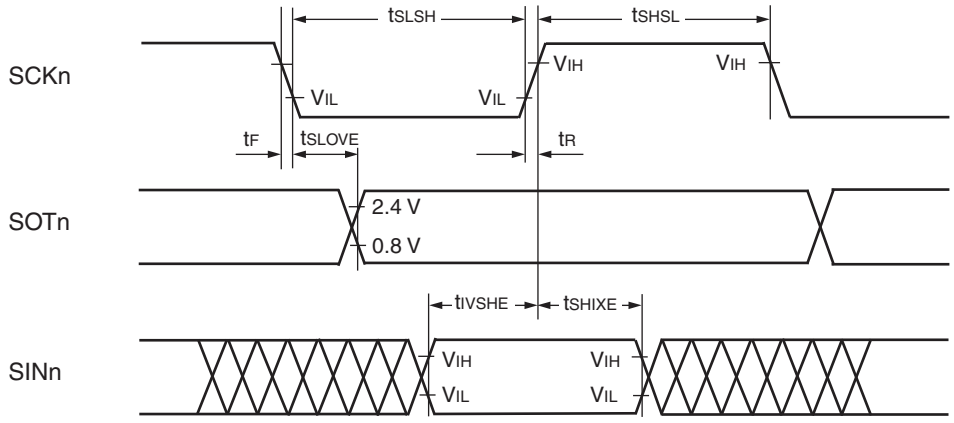
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin C_L = 80 pF + 1 TTL	5 t_{CP}	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		– 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCKn	External shift clock mode output pin C_L = 80 pF + 1 TTL	3 t_{CP} – t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCKn		t_{CP} + 10	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CP} + 30	—	ns
SCK rising time	t_F	SCKn		—	10	ns
SCK falling time	t_R	SCKn		—	10	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity of a pin during testing.
- t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).

Internal shift clock mode



External shift clock mode



Bit setting : ESCR : SCES = 1, ECCR : SCDE = 0

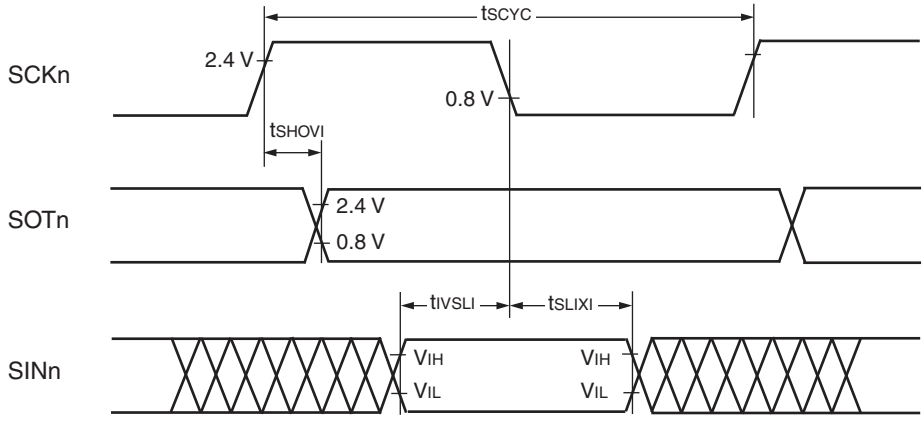
(T_A = –40°C to + 105°C, $V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, Vss = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin C_L = 80 pF + 1 TTL	5 t_{CP}	—	ns
SCK ↑ →SOT delay time	t_{SHOVI}	SCKn, SOTn		– 50	+ 50	ns
Valid SIN→SCK ↓	t_{IVSLI}	SCKn, SINn		t_{CP} + 80	—	ns
SCK ↓ →Valid SIN hold time	t_{SLIXI}	SCKn, SINn		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn	External shift clock mode output pin C_L = 80 pF + 1 TTL	3 t_{CP} – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn		t_{CP} + 10	—	ns
SCK ↑ →SOT delay time	t_{SHOVE}	SCKn, SOTn		—	2 t_{CP} + 60	ns
Valid SIN→SCK ↓	t_{IVSLE}	SCKn, SINn		30	—	ns
SCK ↓ →Valid SIN hold time	t_{SLIXE}	SCKn, SINn		t_{CP} + 30	—	ns
SCK rise	t_F	SCKn		—	10	ns
SCK fall	t_R	SCKn		—	10	ns

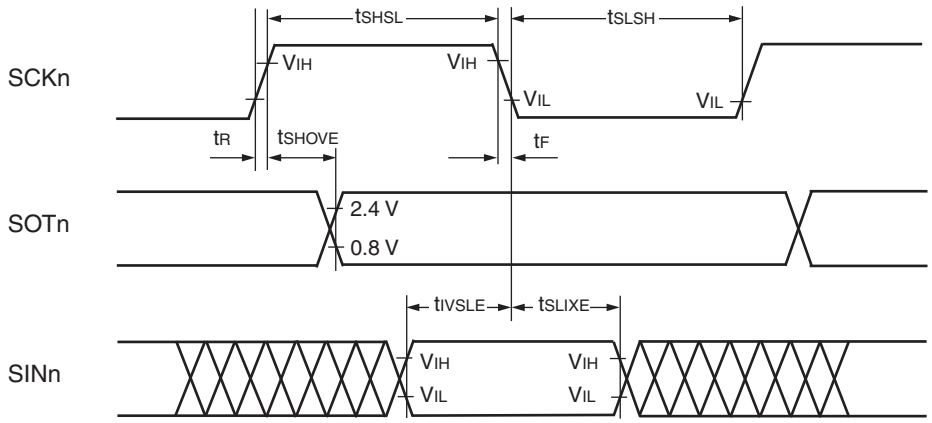
Notes: • C_L is the load capacity of a pin during testing.

• t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).

Internal shift clock mode



External shift clock mode



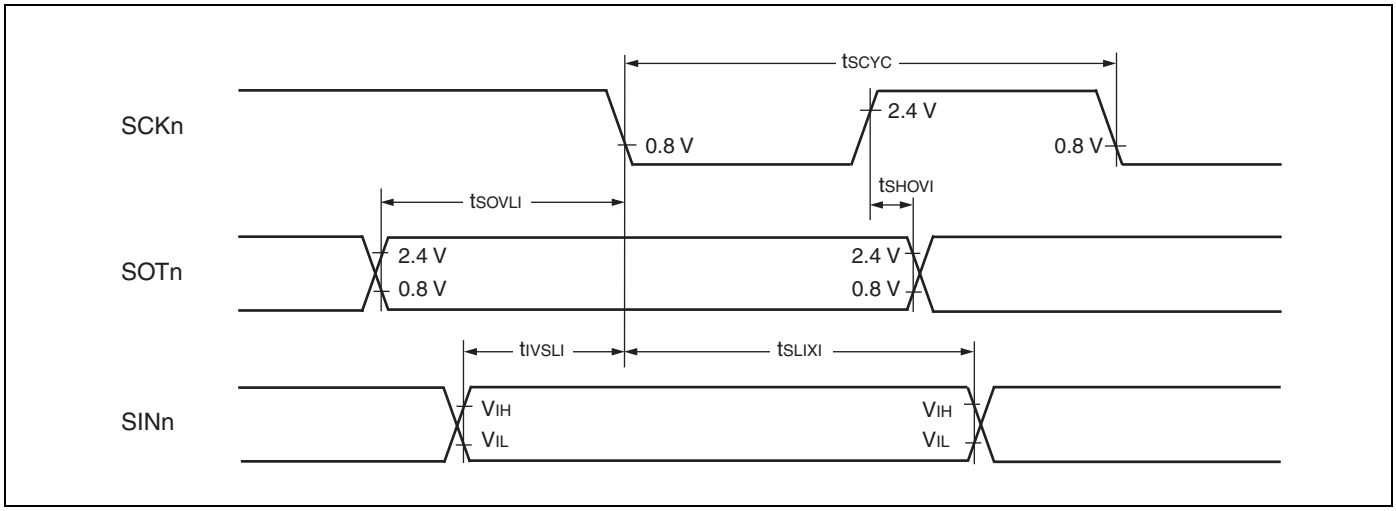
Bit setting:ESCR:SCES = 0, ECCR:SCDE = 1

(T_A = –40°C to + 105°C, $V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, Vss = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin C_L = 80 pF + 1 TTL	5 t_{CP}	—	ns
SCK ↑ →SOT delay time	t_{SHOVI}	SCKn, SOTn		− 50	+ 50	ns
Valid SIN→SCK ↓	t_{IVSLI}	SCKn, SINn		t_{CP} + 80	—	ns
SCK ↓ →Valid SIN hold time	t_{SLIXI}	SCKn, SINn		0	—	ns
SOT→SCK ↓ delay time	t_{SOVLI}	SCKn, SOTn		3 t_{CP} − 70	—	ns

Notes: • C_L is the load capacity of a pin during testing.

• t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).



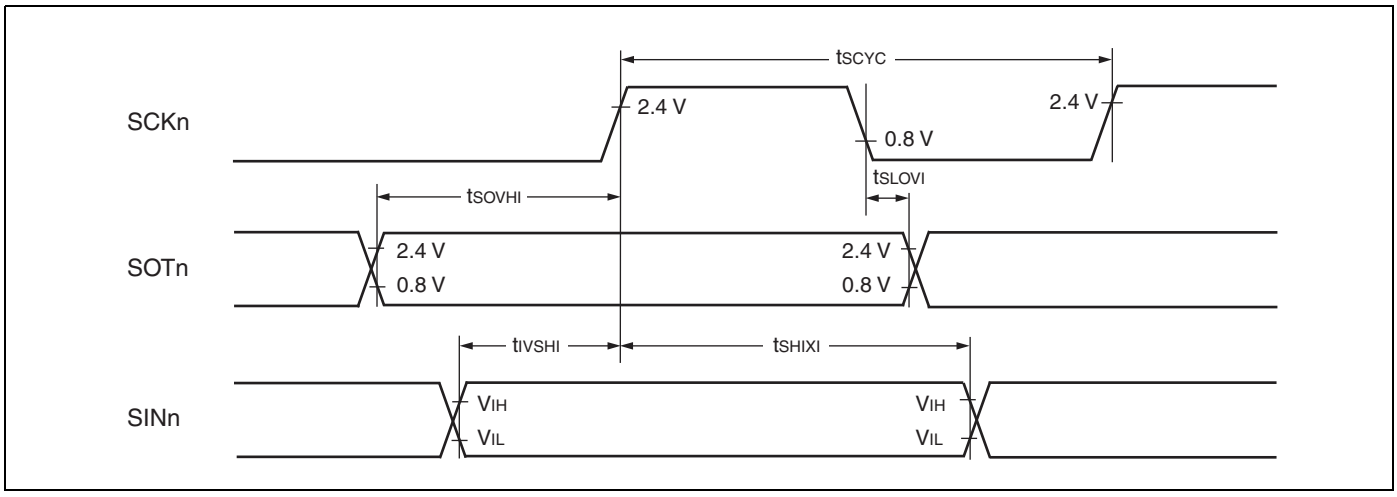
Bit setting:ESCR:SCES = 1, ECCR:SCDE = 1

(T_A = −40°C to + 105°C, $V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, Vss = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ →SOT delay time	t_{SLOVI}	SCKn, SOTn		− 50	+ 50	ns
Valid SIN→SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CP} + 80	—	ns
SCK ↑ →Valid SIN delay time	t_{SHIXI}	SCKn, SINn		0	—	ns
SOT→SCK ↑ delay time	t_{SOVHI}	SCKn, SOTn		3 t_{CP} − 70	—	ns

Notes: • C_L is the load capacity of a pin during testing.

• t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).

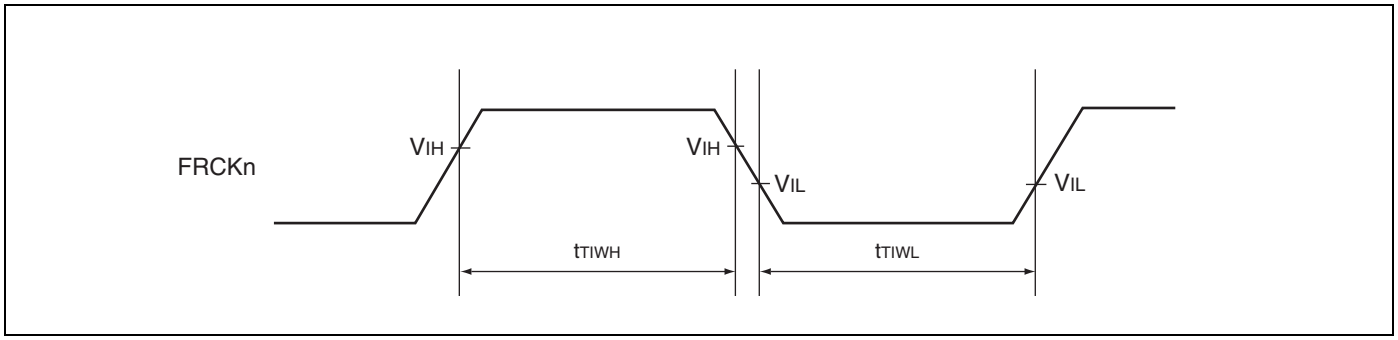


14.6.5 Free-run timer clock

($V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	FRCKn	—	$4t_{CLKP}$	—	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.

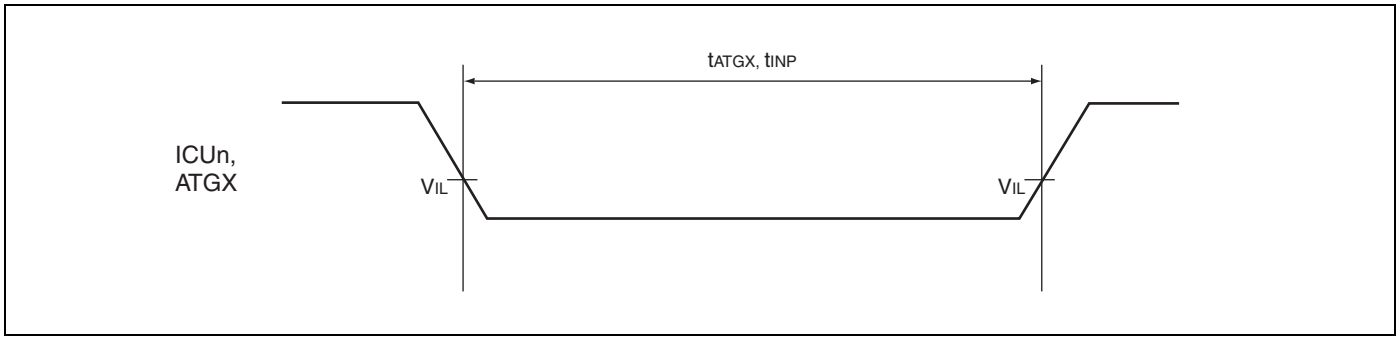


14.6.6 Trigger input timing

($V_{CC}5$ = 5.0 V ±10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40°C to + 105°C)

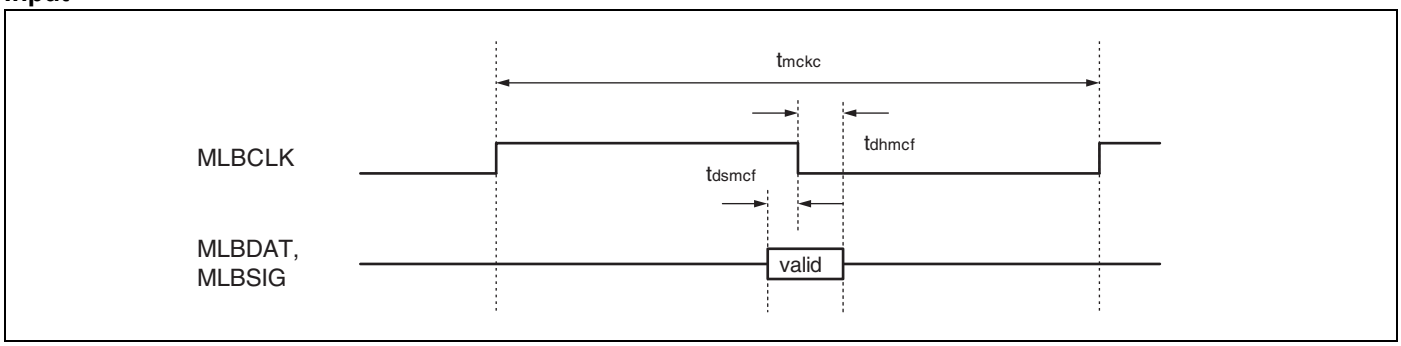
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.



MediaLB AC characteristics

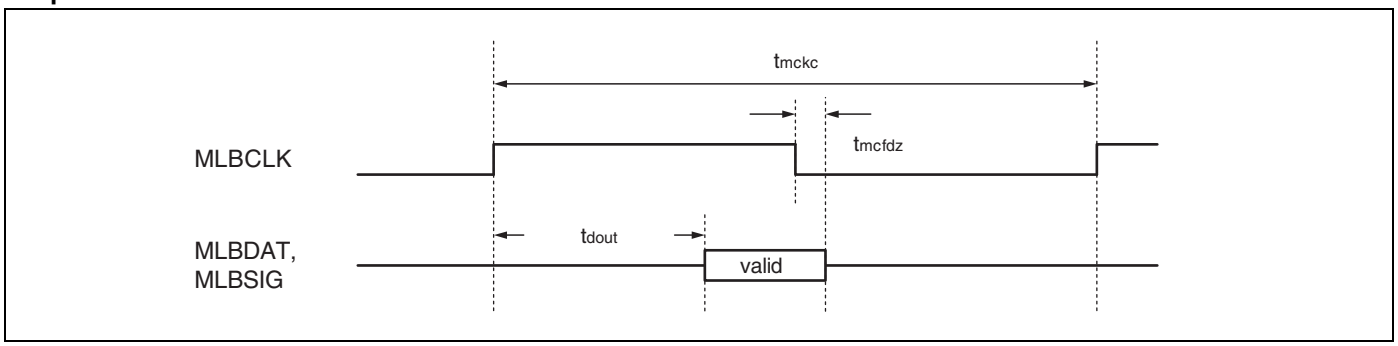
Input



($V_{CC}3$ = 3.3 V ± 10%, V_{SS} = 0.0 V, T_A = − 40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	—	—	40	—	ns	
MLBSIG, MLBDAT input setup	t_{dsmcf}	MLBSIG MLBDAT	—	1	—	—	ns	
MLBSIG, MLBDAT input hold	t_{dhmcf}	MLBSIG MLBDAT	—	4	—	—	ns	

Output



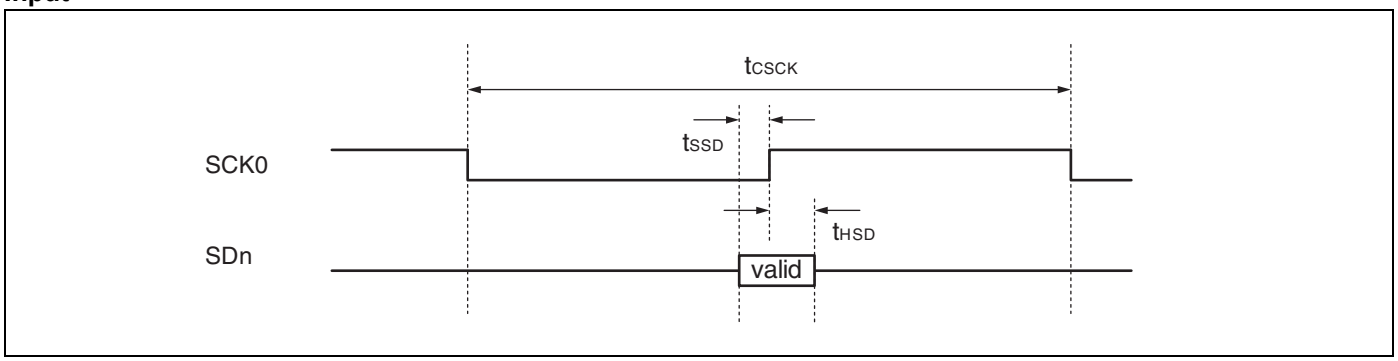
($V_{CC}3$ = 3.3 V ± 10%, V_{SS} = 0.0 V, T_A = − 40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	—	—	40	—	ns	
MLBSIG, MLBDAT output stop	t_{mcfdz}	MLBSIG MLBDAT	—	0	—	—	ns	
MLBSIG, MLBDAT output delay	t_{dout}	MLBSIG MLBDAT	—	—	—	11	ns	

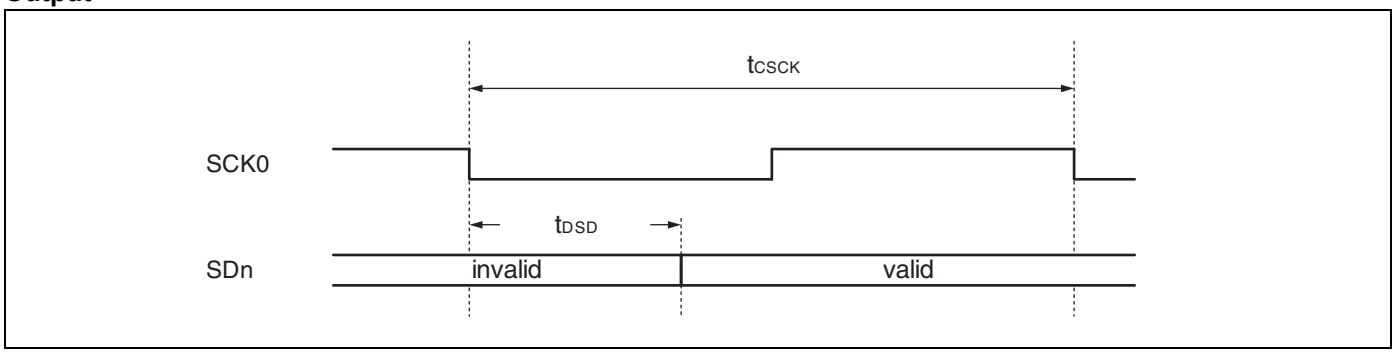
Note: Addition capacity 50 pF

I²S AC characteristics

Input



Output



($V_{CC}3$ = 3.3 V ± 10%, V_{SS} = 0.0 V, T_A = − 40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
SCK cycle	t_{CSCK}	SCK0	—	651	—	—	ns	
SD input setup	t_{SSD}	SDn	—	50	—	—	ns	
SD input hold	t_{HSD}	SDn	—	50	—	—	ns	
SD output delay	t_{DSD}	SDn	—	—	—	50	ns	

Note: Addition capacity 50 pF

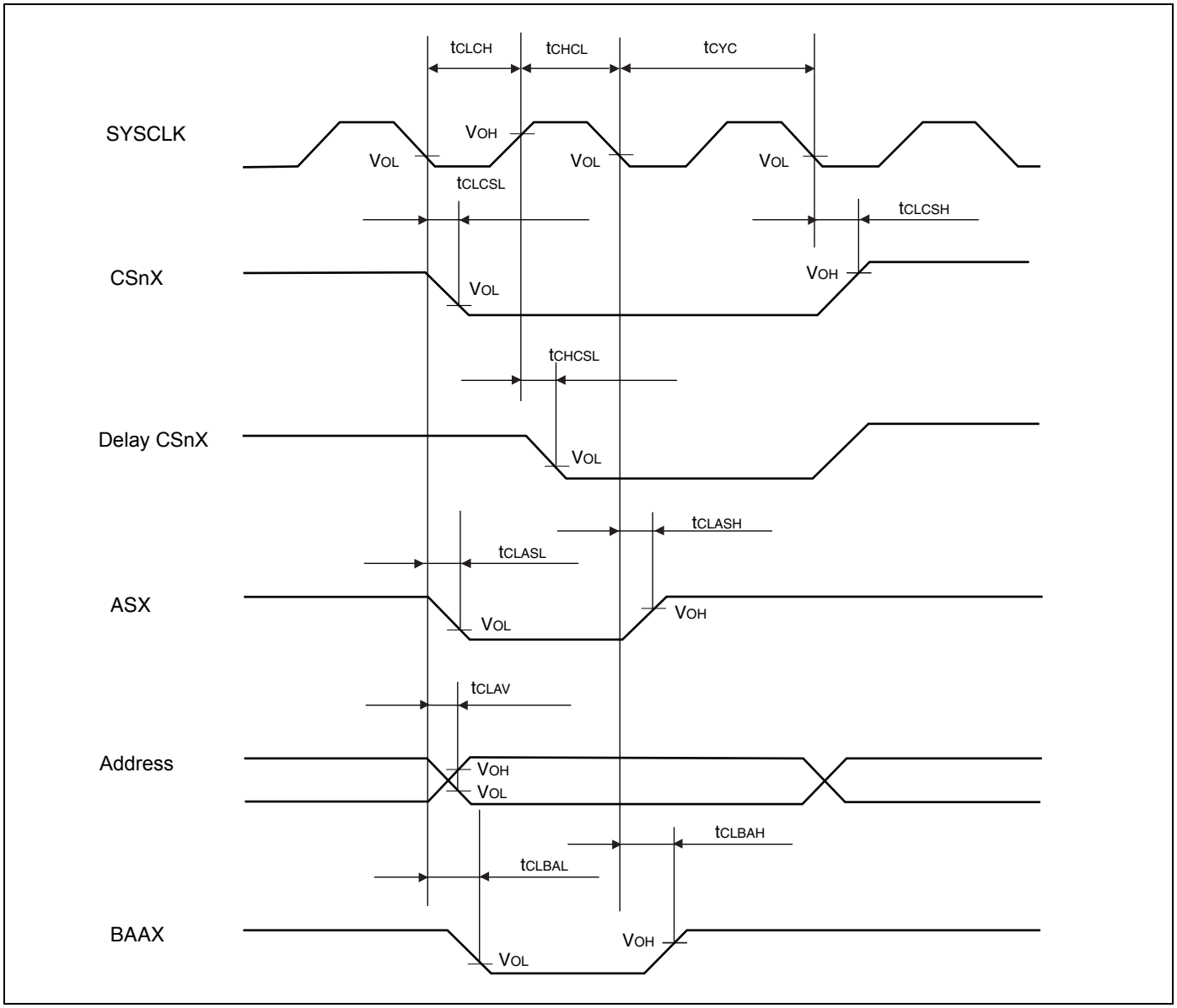
14.6.7 External Bus AC Timings

Basic Timing

(Vcc3 = 3.3 V ± 10%, Vss = 0.0 V, T_A = − 40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK	t_{CLCH}	SYSCLK	—	—	t_{CLKT} / 2	—	ns
	t_{CHCL}			—	t_{CLKT} / 2	—	
SYSCLK ↓ →CSnX delay	t_{CLCSL}	SYSCLK CSnX		− 6	—	+ 6	
	t_{CLCSH}			− 6	—	+ 6	
SYSCLK ↑ →CSnX delay when using CS delay function	t_{CHCSL}			− 6	—	+ 6	
SYSCLK ↓ →ASX delay	t_{CLASL}	SYSCLK ASX		− 6	—	+ 6	
	t_{CLASH}			− 6	—	+ 6	
SYSCLK ↓ →BAAX delay	t_{CLBAL}	SYSCLK BAAX		− 6	—	+ 6	
	t_{CLBAH}			− 6	—	+ 6	
SYSCLK ↓ →address output delay	t_{CLAV}	SYSCLK A23 to A00		− 6	—	+ 6	

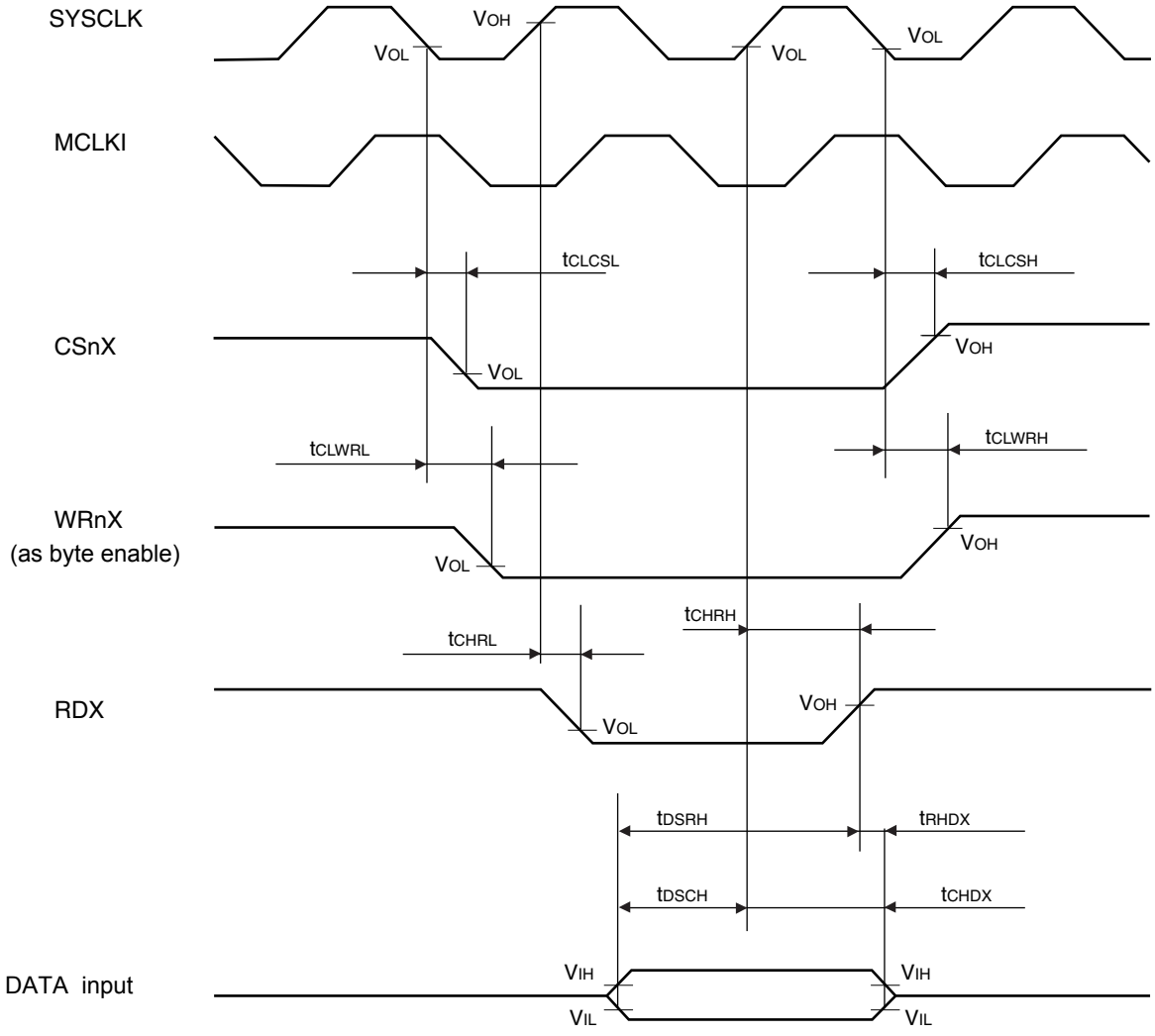
Note: t_{CLKT} is the cycle time of the external bus clock.


tCLCH
tCHCL
tCYC
SYSCLK
VOH
VOL
VOL
VOL
tCLCSL
tCLCSH
CSnX
VOL
VOH
tCHCSL
Delay CSnX
VOL
tCLASH
tCLASL
ASX
VOL
VOH
tCLAV
Address
VOH
VOL
tCLBAH
tCLBAL
BAAX
VOH
VOL

Read access

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

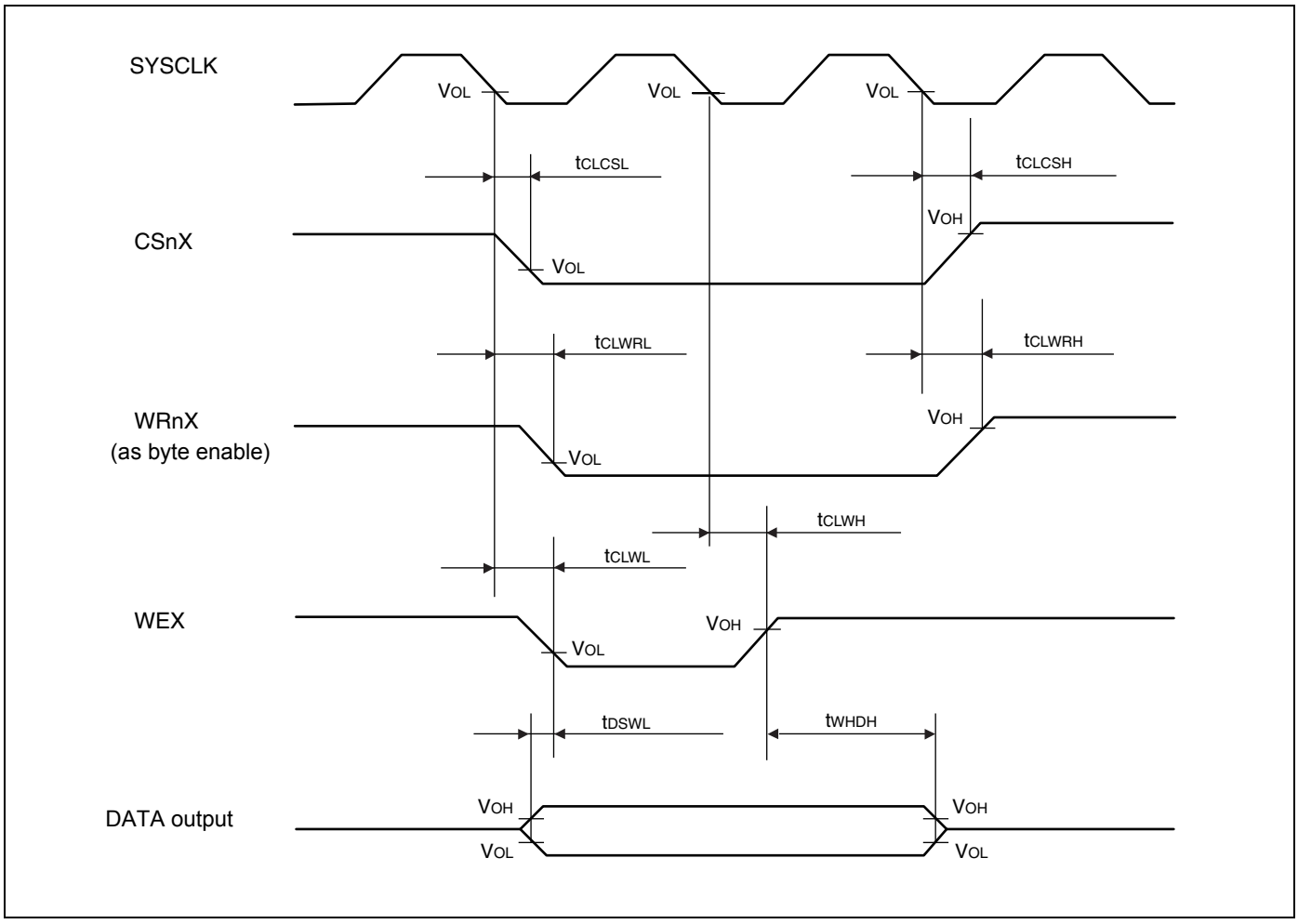
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↑ → RDX delay	t_{CHRL}	SYSCLK RDX	—	− 6	—	+ 6	ns
	t_{CHRH}			− 6	—	+ 6	
Data Valid → RDX ↑ setup	t_{DSRH}	RDX D31 to D16		30	—	—	
RDX ↑ → Valid data hold	t_{RHDX}	RDX D31 to D16		0	—	—	
Data Valid → SYSCLK ↑ setup	t_{DSCH}	MCLKI D31 to D16		6	—	—	
SYSCLK ↑ → Valid data hold	t_{CHDX}	MCLKI D31 to D16		6	—	—	
SYSCLK ↓ → WRnX delay (as byte enable)	t_{CLWRL}	MCLKO WRnX		—	3	—	
	t_{CLWRH}			—	3	—	
SYSCLK ↓ → CSnX delay	t_{CLCSL}	MCLKO CSnX		− 6	—	+ 6	
	t_{CLCSH}			− 6	—	+ 6	


SYSCLK
MCLKI
CSnX
WRnX
(as byte enable)
RDX
DATA input
VOH
VOL
tCLCSL
tCLCSH
tCLWRL
tCLWRH
tCHRL
tCHRH
tDSRH
tRHDX
tDSCH
tCHDX
VIH
VIL

Synchronous write access − Byte control type

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

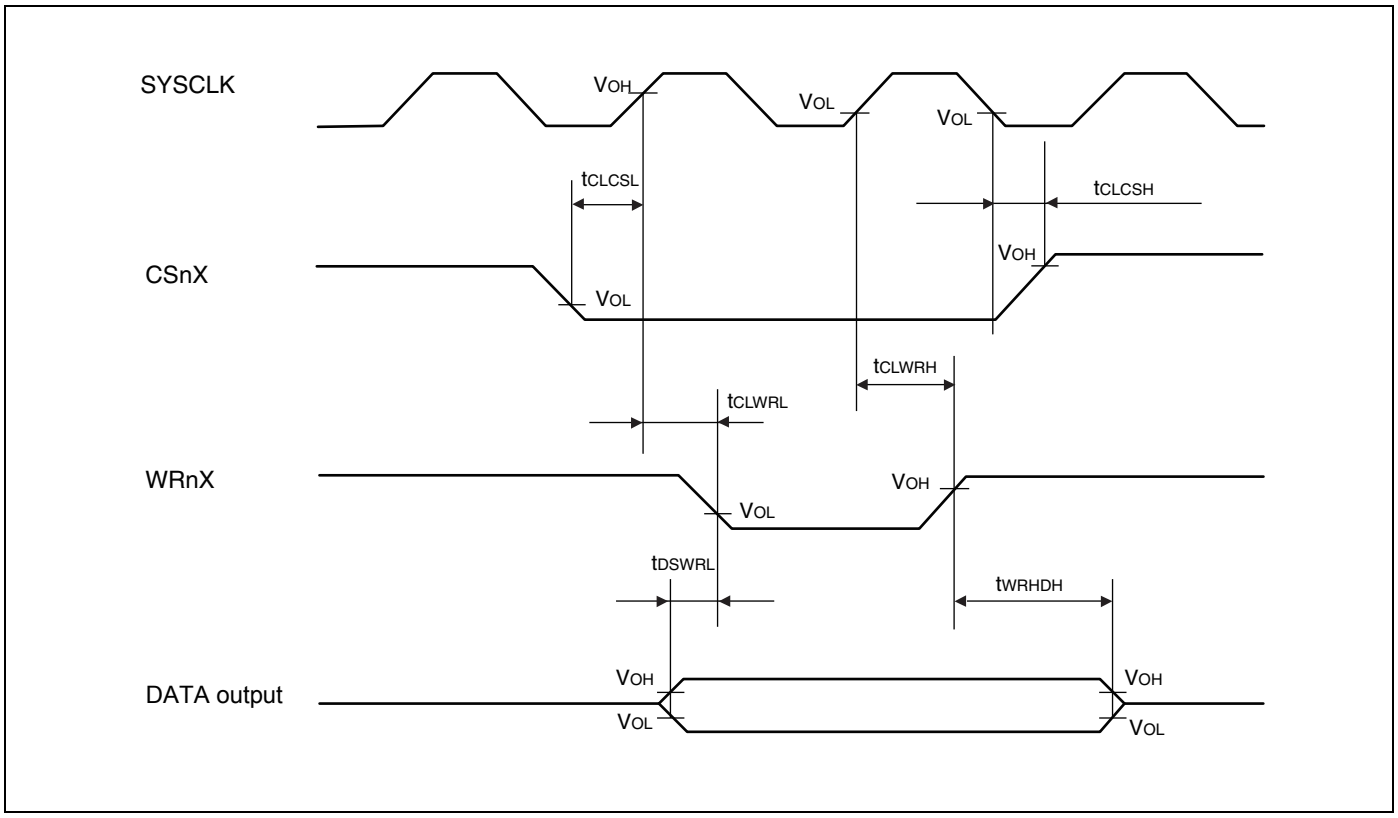
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↓ → WEX delay	t_{CLWL}	SYSCLK WEX	—	− 6	—	+ 6	ns
	t_{CLWH}			− 6	—	+ 6	
Data Valid → WEX ↓ setup	t_{DSWL}	WEX D31 to D16		—	0	—	
WEX ↑ → Valid data hold	t_{WHDH}	WEX D31 to D16		—	t_{CLKT}	—	
SYSCLK ↓ → WRnX delay (as byte enable)	t_{CLWRL}	SYSCLK WRnX		—	3	—	
	t_{CLWRH}			—	3	—	
SYSCLK ↓ → CSnX delay	t_{CLCSL}	SYSCLK CSnX		− 6	—	+ 6	
	t_{CLCSH}			− 6	—	+ 6	



Synchronous write access − Non-byte control type

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

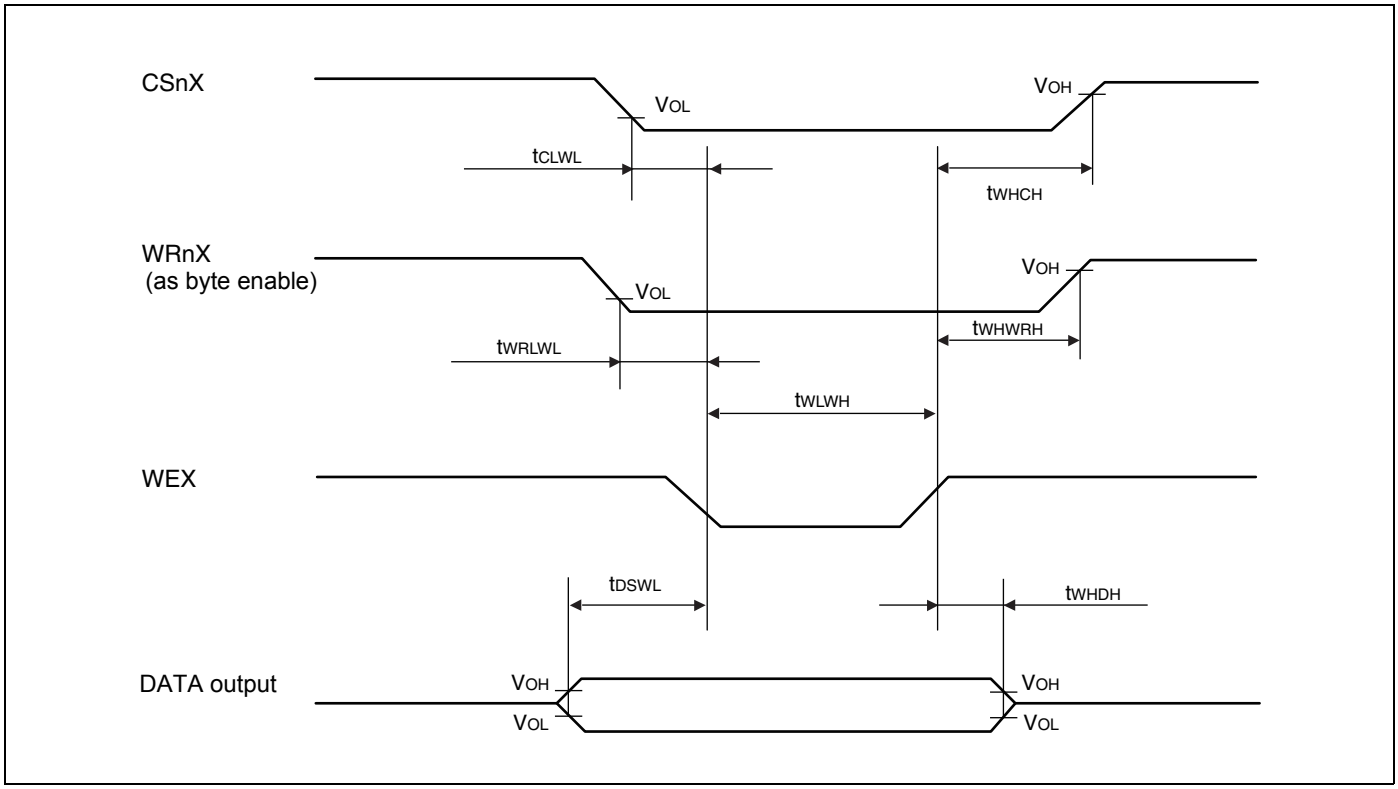
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↑ →WRnX delay	t_{CLWRL}	SYSCLK WEX	—	− 6	—	+ 6	ns
	t_{CLWRH}			− 6	—	+ 6	
Data Valid →WRnX ↓ setup	t_{DSWRL}	WEX D31 to D16		—	0	—	
WRnX ↑ →Valid data hold	t_{WRHDH}	WEX D31 to D16		—	t_{CLKT}	—	
SYSCLK ↓ →CSnX delay	t_{CLCSL}	SYSCLK CSnX		− 6	—	+ 6	
	t_{CLCSH}			− 6	—	+ 6	



Asynchronous write access − Byte control type

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

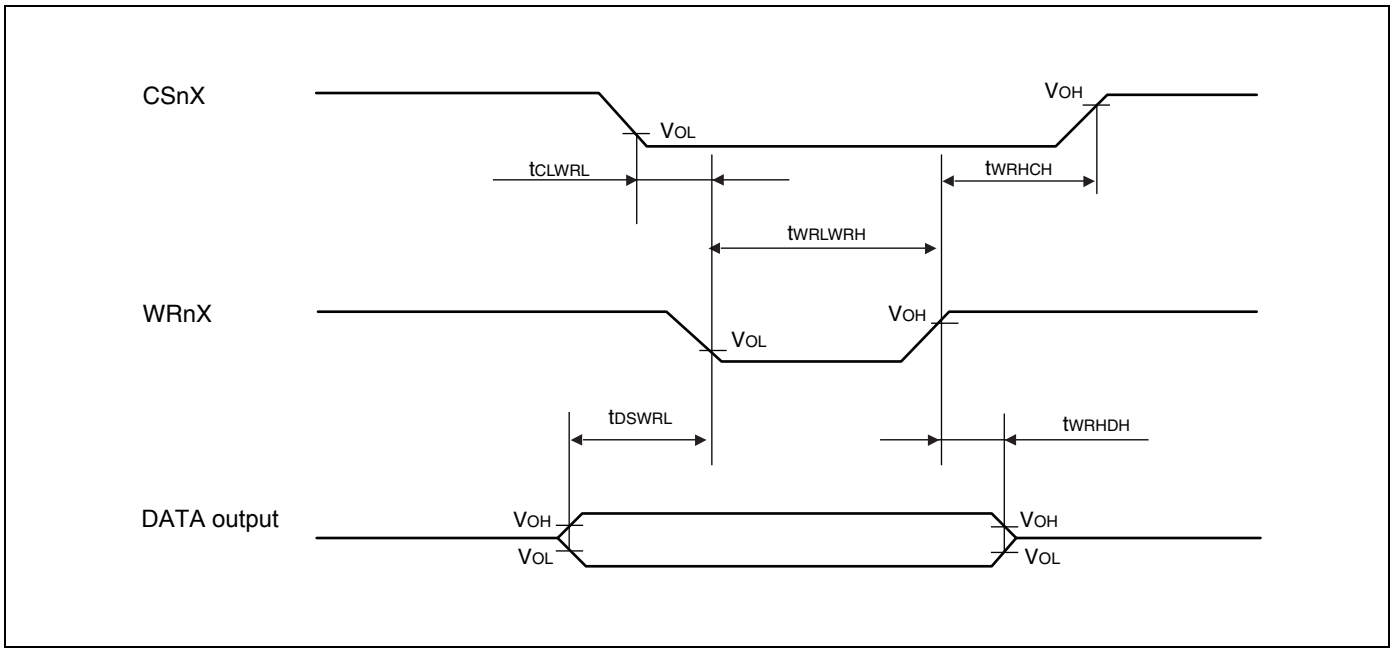
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
WEX ↓ →WEX ↑ pulse width	t_{WLWH}	WEX	—	—	t_{CLKT}	—	ns
Data Valid →WEX ↓ setup	t_{DSWL}	WEX D31 to D16		—	t_{CLKT} / 2	—	
WEX ↑ →Valid data hold	t_{WHDH}	WEX D31 to D16		—	t_{CLKT} / 2	—	
WEX→WRnX delay	t_{WRLWL}	WEX WRnX		—	t_{CLKT} / 2	—	
	t_{WHWRH}			—	t_{CLKT} / 2	—	
WEX→CSnX delay	t_{CLWL}	WEX CSnX		—	t_{CLKT} / 2	—	
	t_{WHCH}			—	t_{CLKT} / 2	—	



Asynchronous write access − Non-byte control type

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

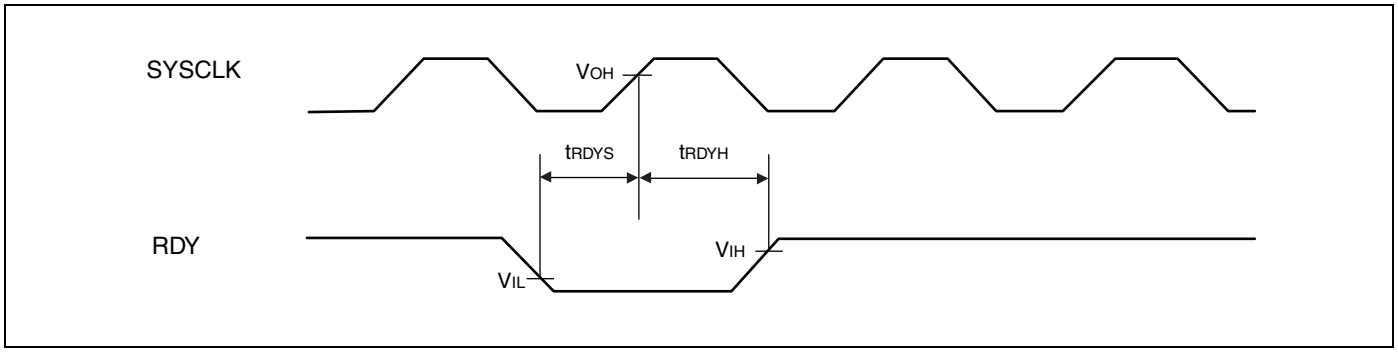
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
WRnX ↓ →WRnX ↑ pulse width	t_{WRLWRH}	WRnX	—	—	t_{CLKT}	—	ns
Data Valid →WRnX ↓ setup	t_{DSWRL}	WRnX D31 to D16		—	t_{CLKT} / 2	—	
WRnX ↑ →Valid data hold	t_{WRHDH}	WRnX D31 to D16		—	t_{CLKT} / 2	—	
WRnX→CSnX delay	t_{CLWRL}	WRnX CSnX		—	t_{CLKT} / 2	—	
	t_{WRHCH}			—	t_{CLKT} / 2	—	



RDY wait cycle insertion

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	t_{RDYS}	SYSCLK RDY	40	—	ns
RDY hold time	t_{RDYH}	SYSCLK RDY	0	—	ns

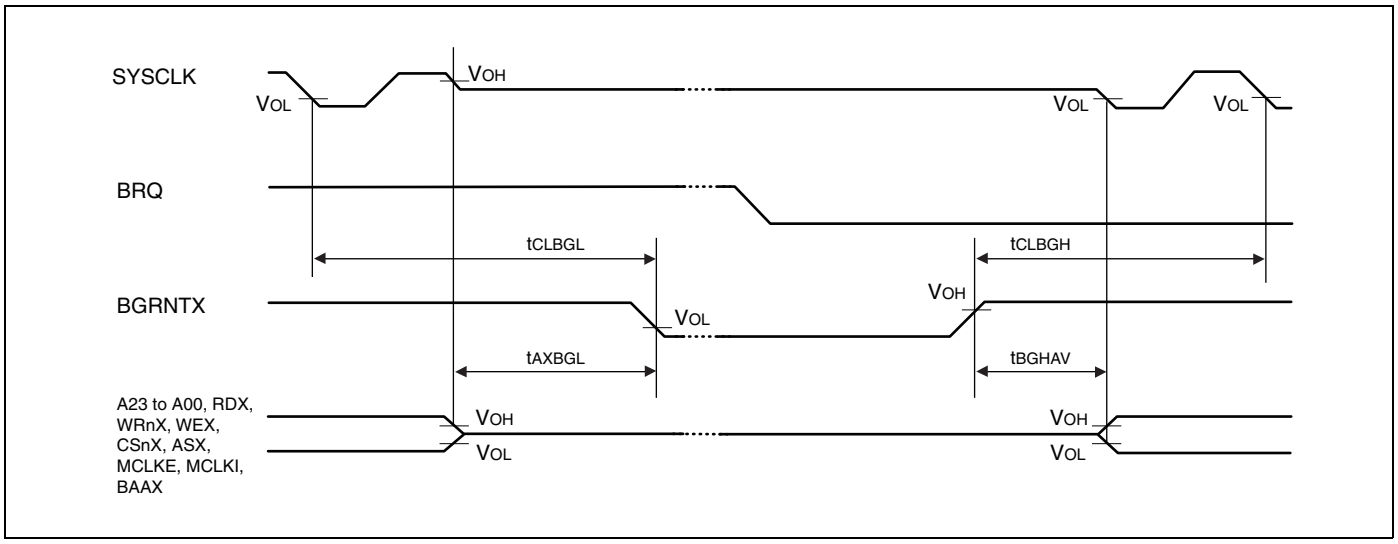


Bus hold timing

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↓ →BGRNTX delay	t_{CLBGL}	SYSCLK BGRNTX	—	—	2 × t_{CLKT}	—	ns
	t_{CLBGH}				2 × t_{CLKT}		
Bus High-Z→BGRNTX ↓	t_{AXBGL}	BGRNTX MCLKE, MCLKI A23 to A00 RDX, ASX WRnX, WEX CSnX, BAAX		—	t_{CLKT}	—	
	t_{BGHAV}			—	t_{CLKT}		

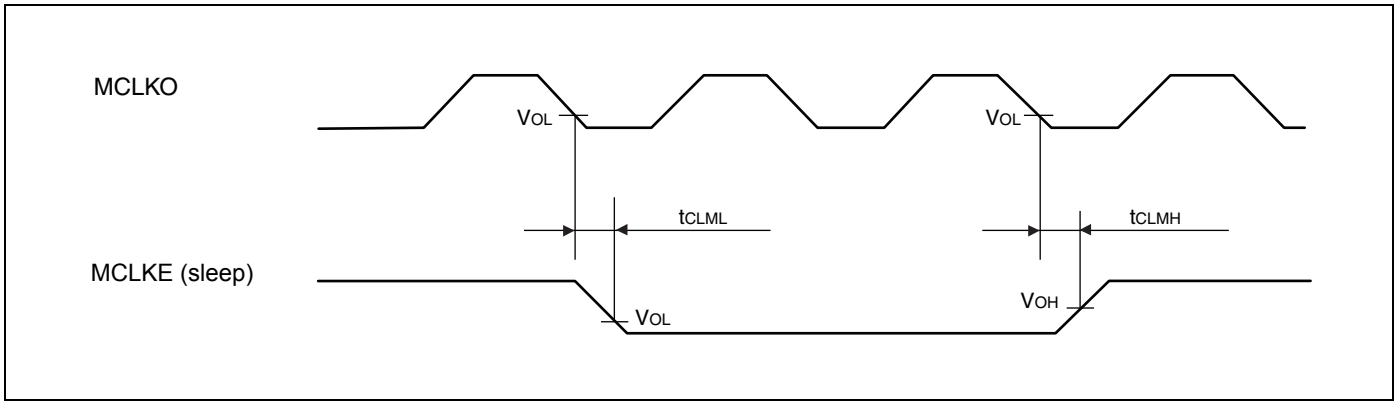
Note: Keep BRQ high until bus is enabled (recognized by the falling edge of BGRNTX). Keep BRQ high during the bus retention period.
The rising edge of BGRNTX recognizes whether bus is enabled after releasing the bus (setting BRQ to Low).



Correlation of clock

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

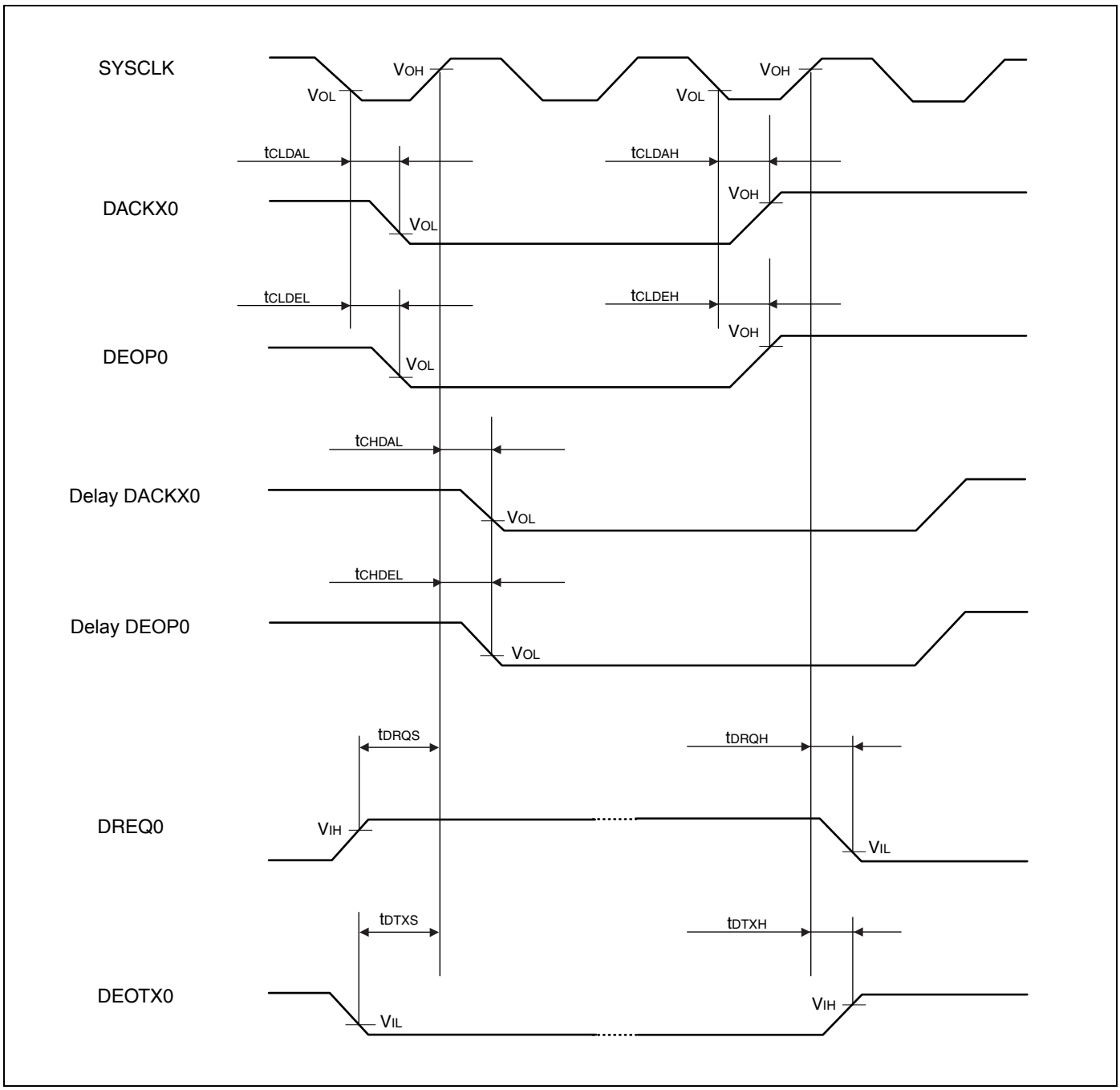
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
MCLKO ↓ →MCLKE (sleep mode)	t_{CLML}	MCLKO MCLKE	—	—	3	—	ns
	t_{CLMH}			—	3	—	



DMA transfer

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↓ →DACKX0 delay	t_{CLDAL}	SYSCLK DACKX0	—	—	3	—	ns
	t_{CLDAH}			—	3	—	
SYSCLK ↓ →DEOP0 delay	t_{CLDEL}	SYSCLK DEOP0		—	3	—	
	t_{CLDEH}			—	3	—	
SYSCLK ↑ →DACKX0 delay (when using CS delay function)	t_{CHDAL}	SYSCLK DACKX0		—	3	—	
SYSCLK ↑ →DEOP0 delay (when using CS delay function)	t_{CHDEL}	SYSCLK DEOP0		—	3	—	
DREQ0 SETUP	t_{DRQS}	SYSCLK DREQ0		—	40	—	
DREQ0 hold	t_{DRQH}	SYSCLK DREQ0		—	0	—	
DEOTX0 SETUP	t_{DTXS}	SYSCLK DEOTX0		—	40	—	
DEOTX0 hold	t_{DTXH}	SYSCLK DEOTX0		—	0	—	

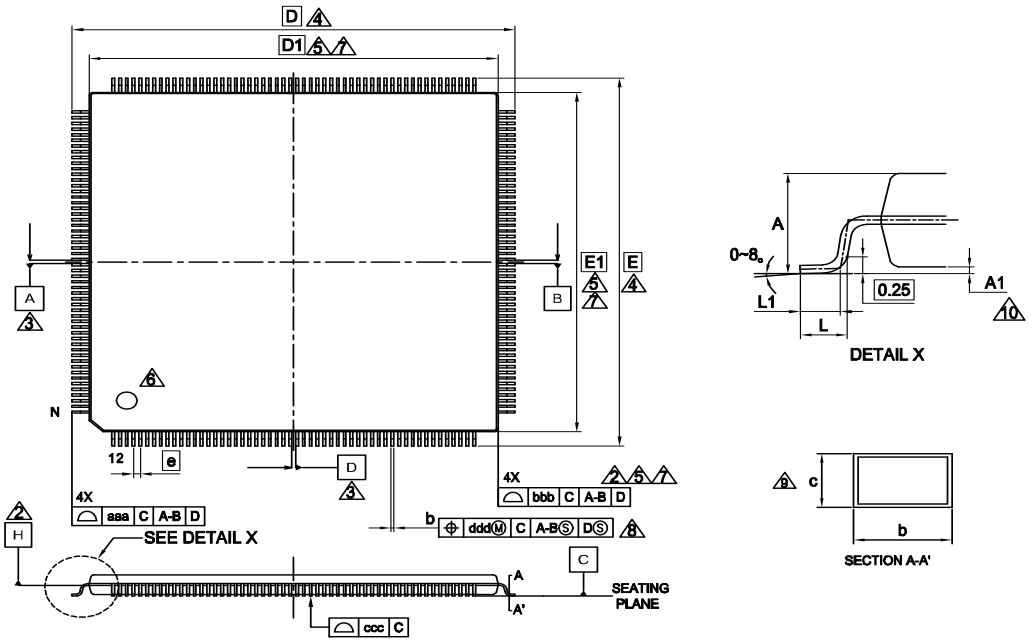

SYSCLK
VOH
VOL
VOH
VOL
tCLDAL
tCLDAH
DACKX0
VOH
VOL
tCLDEL
tCLDEH
DEOP0
VOH
VOL
tCHDAL
Delay DACKX0
VOL
tCHDEL
Delay DEOP0
VOL
tDRQS
tDRQH
DREQ0
VIH
VIL
tDTXS
tDTXH
DEOTX0
VIH
VIL

15. Ordering Information

Part number	Package	Remarks
MB91F467MAPMC-GSE2 MB91F467MAPMC-GSE1	216-pin plastic QFP (LQQ216)	Lead-free package

16. Package Dimension

LQQ216 , 216 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQQ216		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.13	0.18	0.23
c	0.09	——	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.40 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.07
N	216		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

17. Main Changes

Spansion Publication Number: DS07-16613-3E

Page	Section	Change Results
83	Interrupt Vector Table	Corrected the column of interrupt and RN in interrupt number 89 to 91 as follows; Interrupt: I^2S EVEN → I^2S ERROR / RN: 125 → None Interrupt: I^2S ODD → I^2S EVEN / RN: 126 → 125 Interrupt: I^2S error → I^2S ODD / RN: None → 126

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB91460M Series FR60 32-bit Microcontroller Document Number: 002-04615				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	05/18/2010	Migrated to Cypress and assigned document number 002-04615. No change to document contents or format.
*A	5210835	AKIH	05/18/2016	Updated to Cypress format.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for 32-bit Microcontrollers - MCU ***category:***

Click to view products by Cypress ***manufacturer:***

Other Similar products are found below :

MB91F575BHSPMC-GSE1 MB91F594BSPMC-GSE1 PIC32MX120F032B-50I/ML MB91F464AAPMC-GSE2 MB91F577BHSPMC-GSE1 MB91F579CHSPMC1-GSE1 MB91F528USCPMC-GSE2 MB91F248PFV-GE1 MB91F594BPMC-GSE1 MB91243PFV-GS-136E1 MB91F577BHSPMC1-GSE1 PIC32MM0032GPL020-E/ML PIC32MM0016GPL028-E/SS PIC32MM0016GPL028-E/ML PIC32MM0032GPL028-E/ML PIC32MM0032GPL028-E/M6 MB91F526KSEPMC-GSE1 FT902L-T R5F564MLCDFB#31 R5F564MLCDFC#31 R5F523E5ADFL#30 R5F524TAADFF#31 PIC32MM0064GPL028-I/ML PIC32MM0064GPL028-I/SP PIC32MM0064GPL028-I/SO PIC32MX120F032D-I/TL PIC32MX130F064D-I/ML PIC32MZ2064DAB288-I/4J ATUC256L4U-AUT R5F56318CDBG#U0 PIC32MX150F128C-I/TL PIC32MX130F064C-ITL PIC32MX154F128B-V/SO AT32UC3L0128-AUT PIC32MX150F128D-50I/TL PIC32MZ1064DAB288-I/4J PIC32MZ1064DAB169-I/HF ATUC64D4-Z1UT AT32UC3A3128S-CTUT ATUC64L3U-Z3UT MEC1428-SZ-C1 TMS320F28052FPNQ PIC32MX254F128B-V/SO AT32UC3L0256-ZAUT ATUC256L4U-ZAUT PIC32MM0256GPM036-I/M2 PIC32MZ2064DAA169-I/HF FIDO1100BGB208IR1 FIDO1100PQF208IR1 AT32UC3B1128-AUT