The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

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About Cypress

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MB95260H/270H/280H Series

New 8FX 8-bit Microcontrollers

MB95260H/270H/280H are series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral resources.

Features

F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock (main OSC clock and sub-OSC clock are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K)

- Selectable main clock source
  - Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main CR clock (1/8/10 MHz ±3%, maximum machine clock frequency: 10 MHz)
- Selectable subclock source
  - Sub-OSC clock (32.768 kHz)
  - External clock (32.768 kHz)
  - Sub CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

Timer

- 8/16-bit composite timer
- Time-base timer
- Watch prescaler

LIN-UART (only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K)

- Full duplex double buffer
- Capable of clock-synchronized serial data transfer and clock-asynchronized serial data transfer

External interrupt

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/10-bit A/D converter

- 8-bit or 10-bit resolution can be selected.

Low power consumption (standby) modes

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port (Max: 17) (MB95F262K/F263K/F264K)

- General-purpose I/O ports (Max):
  CMOS I/O: 15, N-ch open drain: 2

I/O port (Max: 16) (MB95F262H/F263H/F264H)

- General-purpose I/O ports (Max):
  CMOS I/O: 15, N-ch open drain: 1

I/O port (Max: 5) (MB95F272K/F273K/F274K)

- General-purpose I/O ports (Max):
  CMOS I/O: 3, N-ch open drain: 2

I/O port (Max: 4) (MB95F272H/F273H/F274H)

- General-purpose I/O ports (Max):
  CMOS I/O: 3, N-ch open drain: 1

I/O port (Max: 13) (MB95F282K/F283K/F284K)

- General-purpose I/O ports (Max):
  CMOS I/O: 11, N-ch open drain: 2

I/O port (Max: 12) (MB95F282H/F283H/F284H)

- General-purpose I/O ports (Max):
  CMOS I/O: 11, N-ch open drain: 1

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

Power-on reset

- A power-on reset is generated when the power is switched on.

Low-voltage detection reset circuit

- Built-in low-voltage detector

Clock supervisor counter

- Built-in clock supervisor counter function

Programmable port input voltage level

- CMOS input level / hysteresis input level

Dual operation Flash memory

- The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

- Protects the content of the Flash memory

Contents

1. Product Line-up

MB95260H Series

Part number / Parameter	MB95F262H	MB95F263H	MB95F264H	MB95F262K	MB95F263K	MB95F264K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected by software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 16 • CMOS I/O : 15 • N-ch open drain : 1			• I/O ports (Max) : 17 • CMOS I/O : 15 • N-ch open drain : 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. • The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	6 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	6 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					

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Part number / Parameter	MB95F262H	MB95F263H	MB95F264H	MB95F262K	MB95F263K	MB95F264K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-24P-M07 LCC-32P-M19 FPT-20P-M09 FPT-20P-M10					

MB95270H Series

Part number / Parameter	MB95F272H	MB95F273H	MB95F274H	MB95F272K	MB95F273K	MB95F274K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected by software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 4 • CMOS I/O : 3 • N-ch open drain : 1			• I/O ports (Max) : 5 • CMOS I/O : 3 • N-ch open drain : 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-internal CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	No LIN-UART					
8/10-bit A/D converter	2 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	1 channel					
	• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	2 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-8P-M03 FPT-8P-M08					

MB95280H Series

Part number / Parameter	MB95F282H	MB95F283H	MB95F284H	MB95F282K	MB95F283K	MB95F284K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected by software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 12 • CMOS I/O : 11 • N-ch open drain : 1			• I/O ports (Max) : 13 • CMOS I/O : 11 • N-ch open drain : 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-internal CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. • The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	5 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	1 channel					
	• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	6 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					

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Part number / Parameter	MB95F282H	MB95F283H	MB95F284H	MB95F282K	MB95F283K	MB95F284K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	LCC-32P-M19 DIP-16P-M06 FPT-16P-M06					

2. Packages and Corresponding Products

Package \ Part number	MB95F262H	MB95F262K	MB95F263H	MB95F263K	MB95F264H	MB95F264K	MB95F272H	MB95F272K	MB95F273H	MB95F273K	MB95F274H	MB95F274K
DIP-24P-M07	O	O	O	O	O	O	X	X	X	X	X	X
FPT-20P-M09	O	O	O	O	O	O	X	X	X	X	X	X
FPT-20P-M10	O	O	O	O	O	O	X	X	X	X	X	X
DIP-16P-M06	X	X	X	X	X	X	X	X	X	X	X	X
FPT-16P-M06	X	X	X	X	X	X	X	X	X	X	X	X
DIP-8P-M03	X	X	X	X	X	X	O	O	O	O	O	O
FPT-8P-M08	X	X	X	X	X	X	O	O	O	O	O	O
LCC-32P-M19	O	O	O	O	O	O	X	X	X	X	X	X

Package \ Part number	MB95F282H	MB95F282K	MB95F283H	MB95F283K	MB95F284H	MB95F284K
DIP-24P-M07	X	X	X	X	X	X
FPT-20P-M09	X	X	X	X	X	X
FPT-20P-M10	X	X	X	X	X	X
DIP-16P-M06	O	O	O	O	O	O
FPT-16P-M06	O	O	O	O	O	O
DIP-8P-M03	X	X	X	X	X	X
FPT-8P-M08	X	X	X	X	X	X
LCC-32P-M19	O	O	O	O	O	O

O: Available

X: Unavailable

3. Differences among Products and Notes on Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “24. Electrical Characteristics”.

Package

For details of information on each package, see “2. Packages and Corresponding Products” and “28. Package Dimension”.

Operating voltage

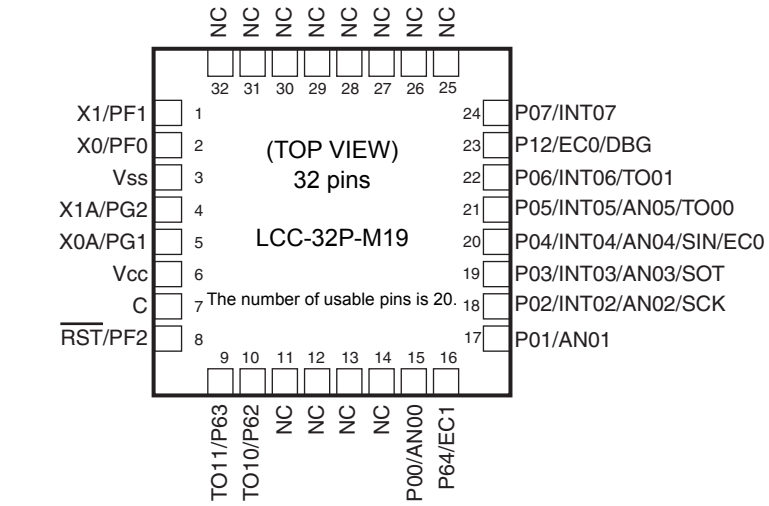
The operating voltage varies, depending on whether the on-chip debug function is used or not.

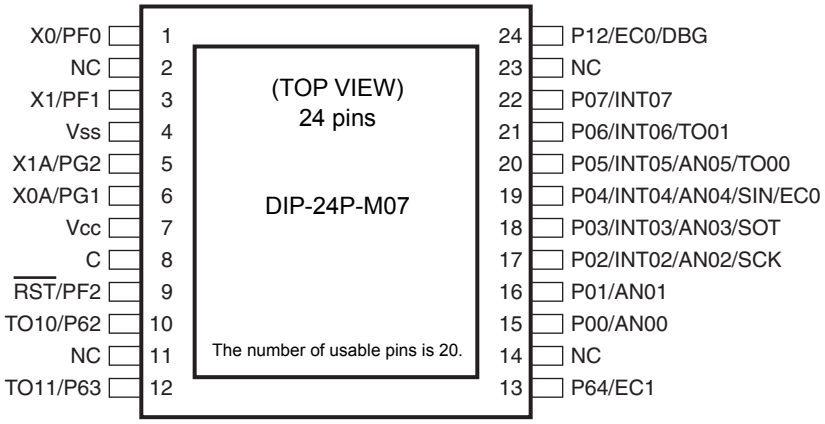
For details of the operating voltage, see “24. Electrical Characteristics”.

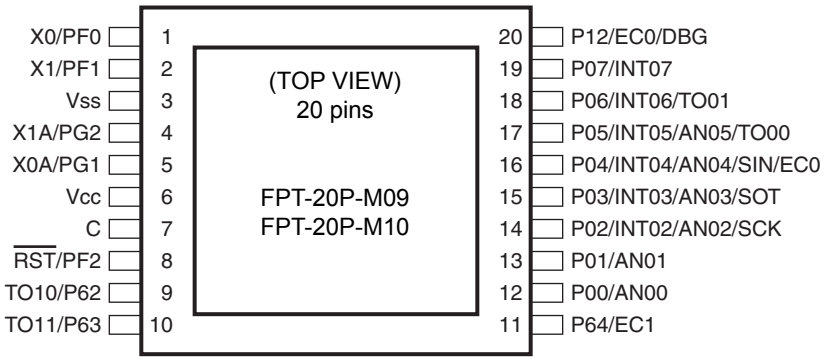
On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. In addition, if the Flash memory data has to be updated, the PF2/$\overline{RST}$ pin must also be connected to the same evaluation tool.

4. Pin Assignment







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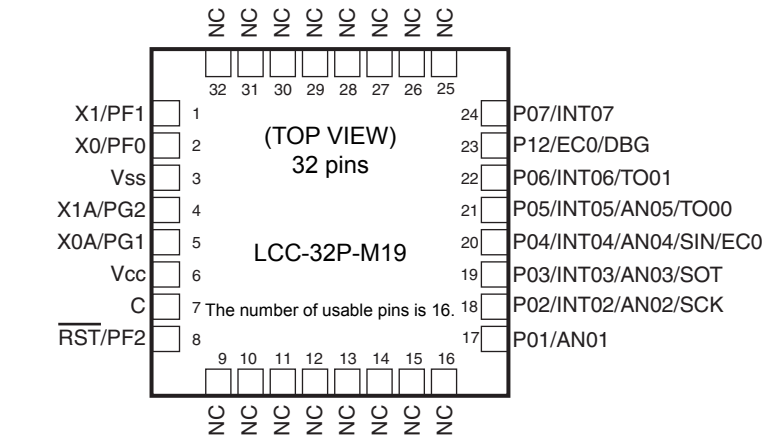
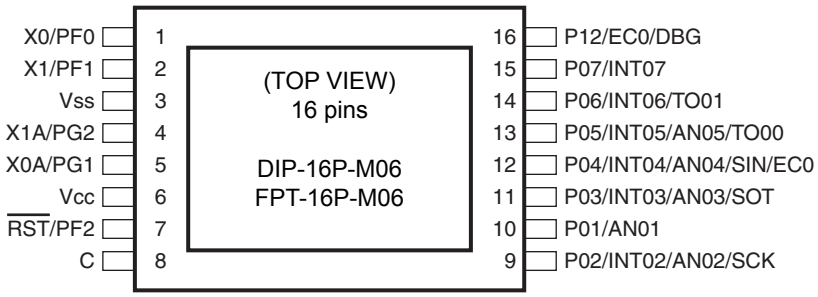
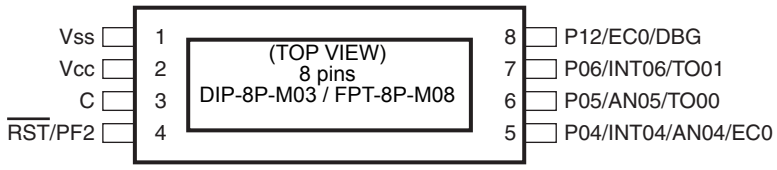

NC NC NC NC NC NC NC NC
32 31 30 29 28 27 26 25
X1/PF1 1
X0/PF0 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
C 7
RST/PF2 8
(TOP VIEW)
32 pins
LCC-32P-M19
The number of usable pins is 16.
24 P07/INT07
23 P12/EC0/DBG
22 P06/INT06/TO01
21 P05/INT05/AN05/TO00
20 P04/INT04/AN04/SIN/EC0
19 P03/INT03/AN03/SOT
18 P02/INT02/AN02/SCK
17 P01/AN01
9 10 11 12 13 14 15 16
NC NC NC NC NC NC NC NC


X0/PF0 1
X1/PF1 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
RST/PF2 7
C 8
(TOP VIEW)
16 pins
DIP-16P-M06
FPT-16P-M06
16 P12/EC0/DBG
15 P07/INT07
14 P06/INT06/TO01
13 P05/INT05/AN05/TO00
12 P04/INT04/AN04/SIN/EC0
11 P03/INT03/AN03/SOT
10 P01/AN01
9 P02/INT02/AN02/SCK


Vss 1
Vcc 2
C 3
RST/PF2 4
(TOP VIEW)
8 pins
DIP-8P-M03 / FPT-8P-M08
8 P12/EC0/DBG
7 P06/INT06/TO01
6 P05/AN05/TO00
5 P04/INT04/AN04/EC0

5. Pin Description (MB95260H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	Vss	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	Vcc	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.
9	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin
16	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

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Pin no.	Pin name	I/O circuit type*	Function
20	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
21	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
24	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
25	NC	—	It is an internally connected pin. Always leave it unconnected.
26	NC	—	It is an internally connected pin. Always leave it unconnected.
27	NC	—	It is an internally connected pin. Always leave it unconnected.
28	NC	—	It is an internally connected pin. Always leave it unconnected.
29	NC	—	It is an internally connected pin. Always leave it unconnected.
30	NC	—	It is an internally connected pin. Always leave it unconnected.
31	NC	—	It is an internally connected pin. Always leave it unconnected.
32	NC	—	It is an internally connected pin. Always leave it unconnected.

*: For the I/O circuit types, see “11. I/O Circuit Type”.

6. Pin Description (MB95260H Series, 24 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	NC	—	It is an internally connected pin. Always leave it unconnected.
3	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
4	V_{SS}	—	Power supply pin (GND)
5	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
6	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
7	V_{CC}	—	Power supply pin
8	C	—	Capacitor connection pin
9	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.
10	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
13	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin
16	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
17	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin

(Continued)

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
18	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
19	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
20	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
21	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
22	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
23	NC	—	It is an internally connected pin. Always leave it unconnected.
24	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “11. I/O Circuit Type”.

7. Pin Description (MB95260H Series, 20 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.
9	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
10	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
11	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
12	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin
13	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
14	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
15	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

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Pin no.	Pin name	I/O circuit type*	Function
16	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
17	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
18	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
19	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
20	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “11. I/O Circuit Type”.

8. Pin Description (MB95270H Series, 8 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	V_{SS}	—	Power supply pin (GND)
2	V_{CC}	—	Power supply pin
3	C	—	Capacitor connection pin
4	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This pin is a dedicated reset pin in MB95F272H/F273H/F274H.
5	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
6	P05	E	General-purpose I/O port High-current pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
7	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
8	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “11. I/O Circuit Type”.

9. Pin Description (MB95280H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	Vss	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	Vcc	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F282H/F283H/F284H.
9	NC	—	It is an internally connected pin. Always leave it unconnected.
10	NC	—	It is an internally connected pin. Always leave it unconnected.
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	NC	—	It is an internally connected pin. Always leave it unconnected.
16	NC	—	It is an internally connected pin. Always leave it unconnected.
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
20	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

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Pin no.	Pin name	I/O circuit type*	Function
21	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
24	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
25	NC	—	It is an internally connected pin. Always leave it unconnected.
26	NC	—	It is an internally connected pin. Always leave it unconnected.
27	NC	—	It is an internally connected pin. Always leave it unconnected.
28	NC	—	It is an internally connected pin. Always leave it unconnected.
29	NC	—	It is an internally connected pin. Always leave it unconnected.
30	NC	—	It is an internally connected pin. Always leave it unconnected.
31	NC	—	It is an internally connected pin. Always leave it unconnected.
32	NC	—	It is an internally connected pin. Always leave it unconnected.

*: For the I/O circuit types, see “11. I/O Circuit Type”.

10. Pin Description (MB95280H Series, 16 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This pin is a dedicated reset pin in MB95F282H/F283H/F284H.
8	C	—	Capacitor connection pin
9	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
10	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
11	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
12	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

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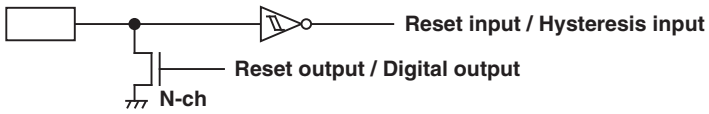
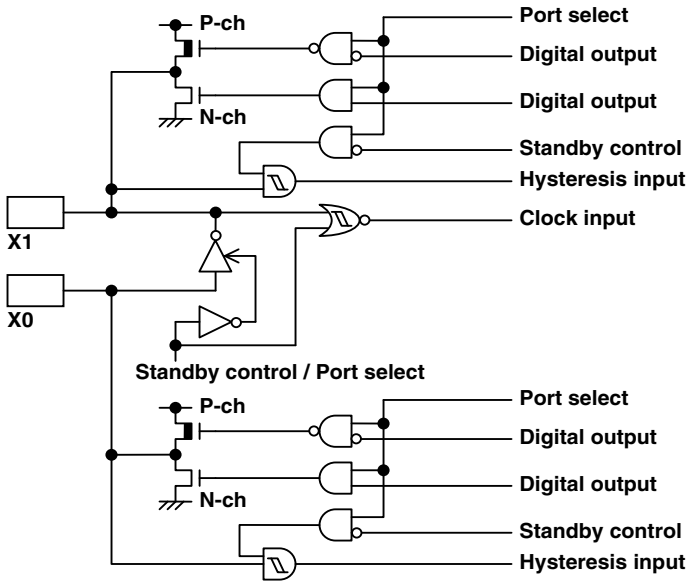
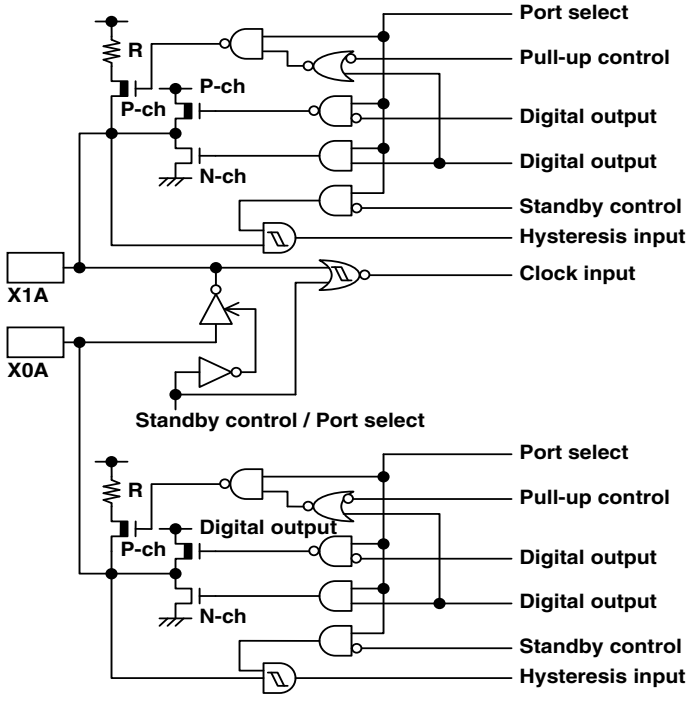
Pin no.	Pin name	I/O circuit type*	Function
13	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 clock input pin
14	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 clock input pin
15	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
16	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “11. I/O Circuit Type”.

11. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side • Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side • Feedback resistance: approx.10 MΩ • CMOS output • Hysteresis input • Pull-up control available

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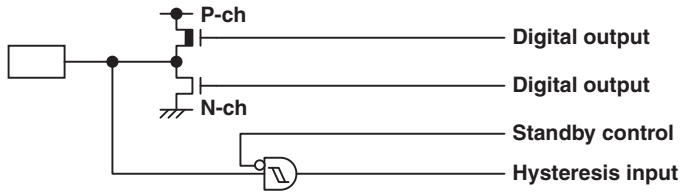
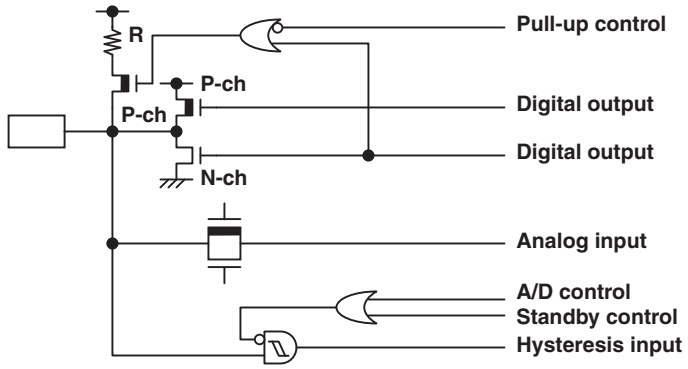
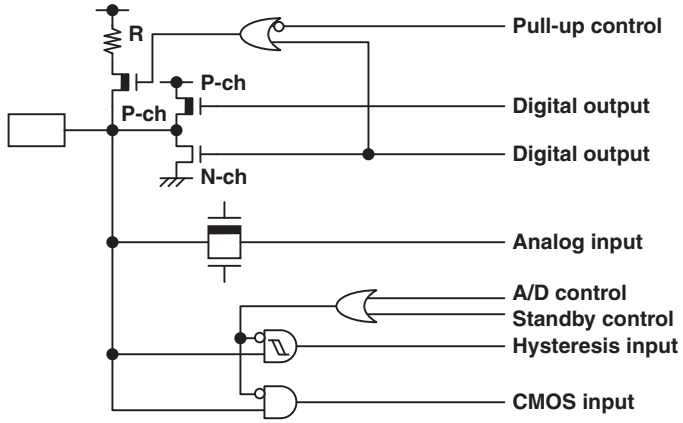
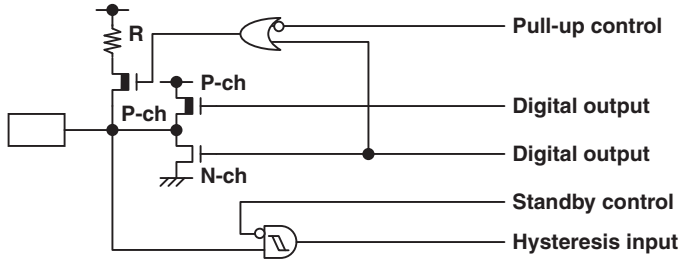
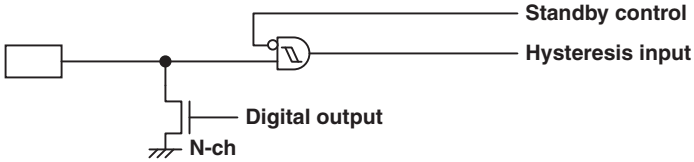
Type	Circuit	Remarks
D		• CMOS output • Hysteresis input
E		• CMOS output • Hysteresis input • Pull-up control available
F		• CMOS output • Hysteresis input • CMOS input • Pull-up control available
G		• Hysteresis input • CMOS output • Pull-up control available
H		• N-ch open drain output • Hysteresis input

12. Notes on Device Handling

Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “24.1 Absolute Maximum Ratings” of “24. Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

13. Pin Connection

Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

$\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.

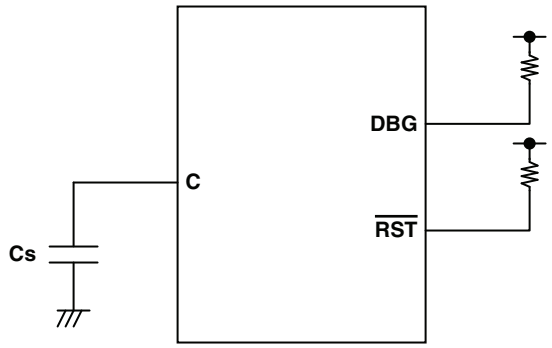
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit of the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit of the SYSC register.

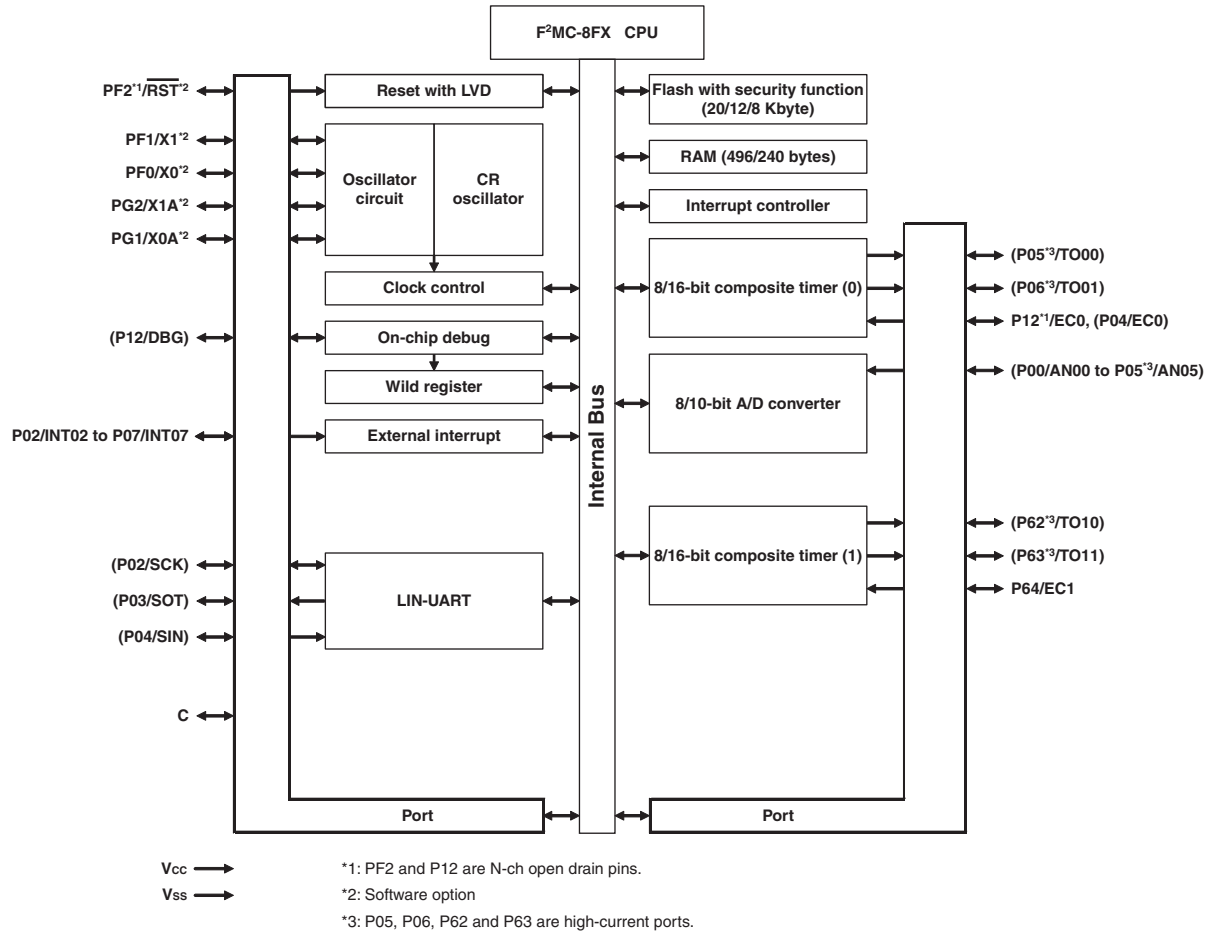
C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG/$\overline{\text{RST}}$/C pins connection diagram

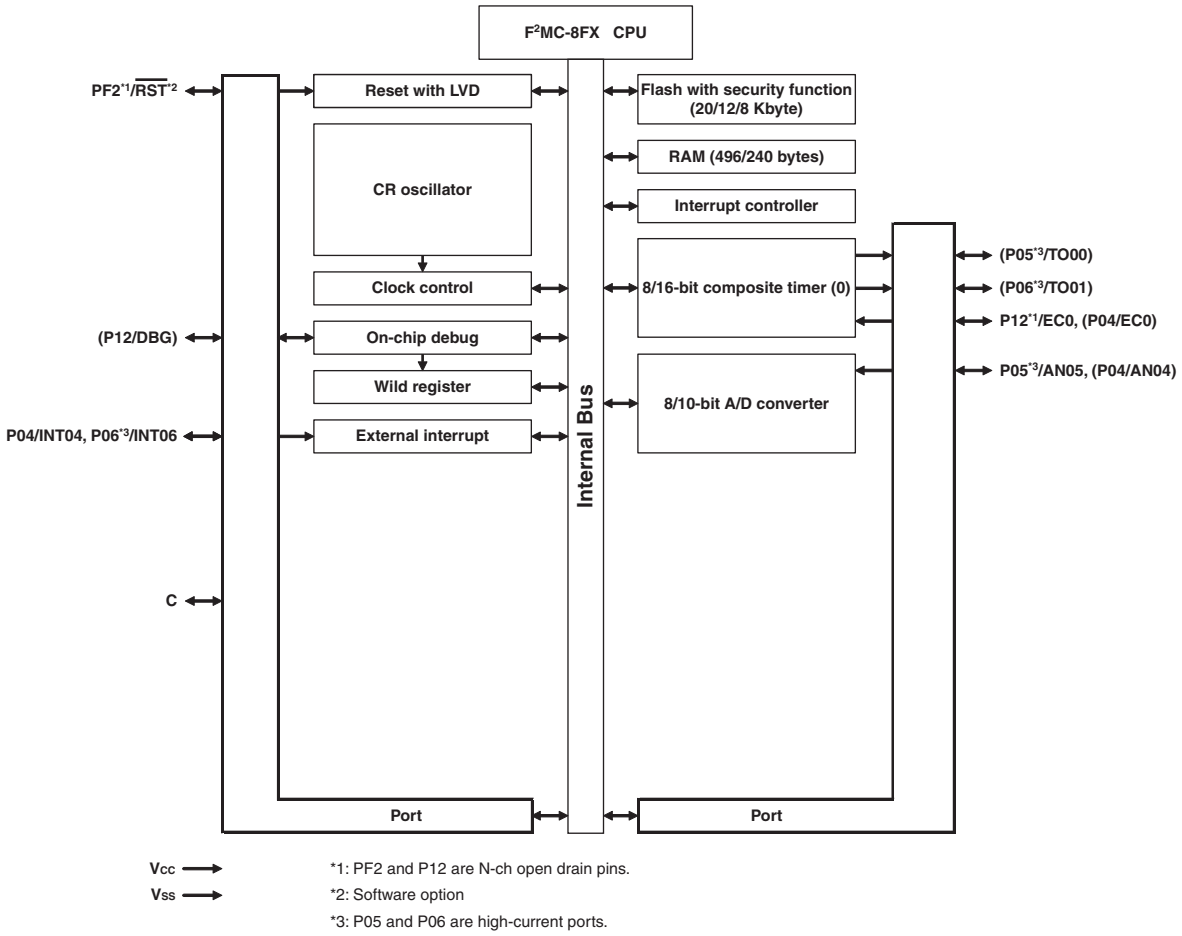


14. Block Diagram (MB95260H Series)



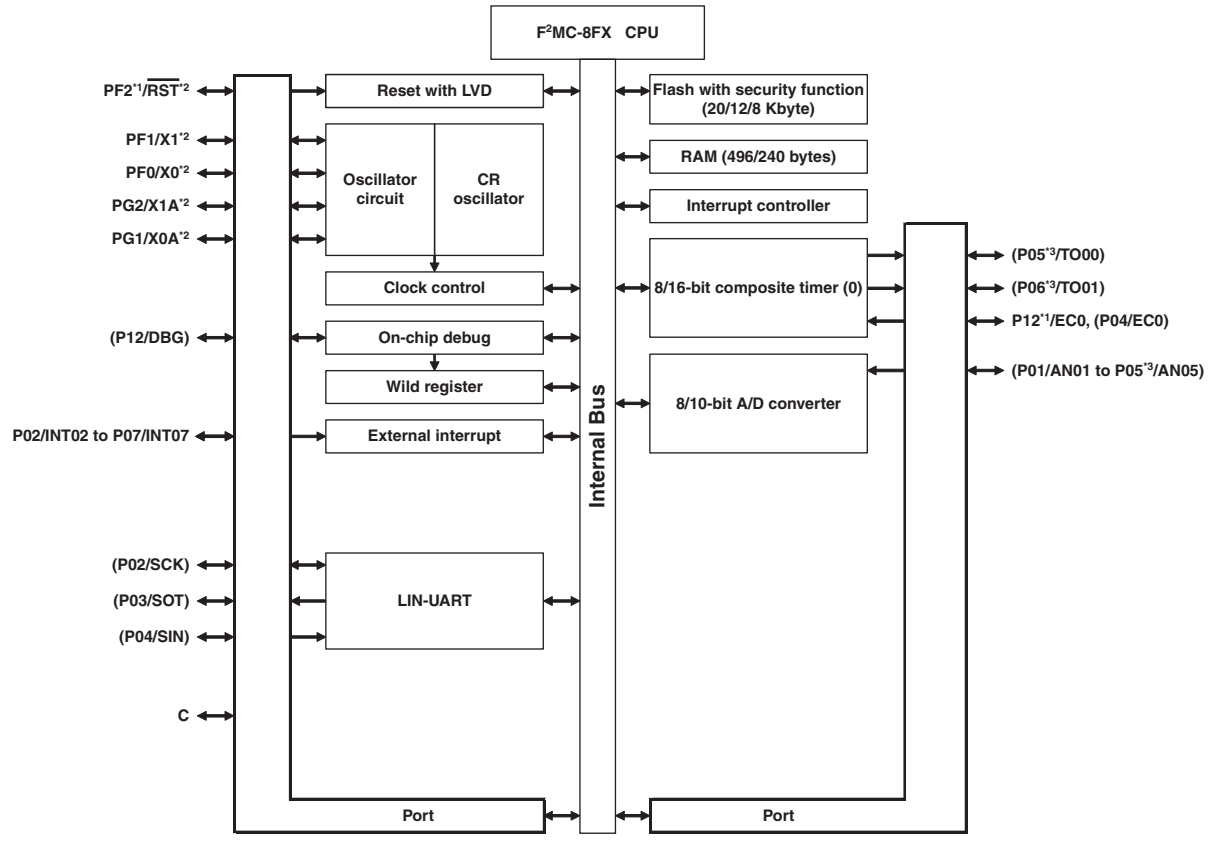
Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

15. Block Diagram (MB95270H Series)



Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

16. Block Diagram (MB95280H Series)



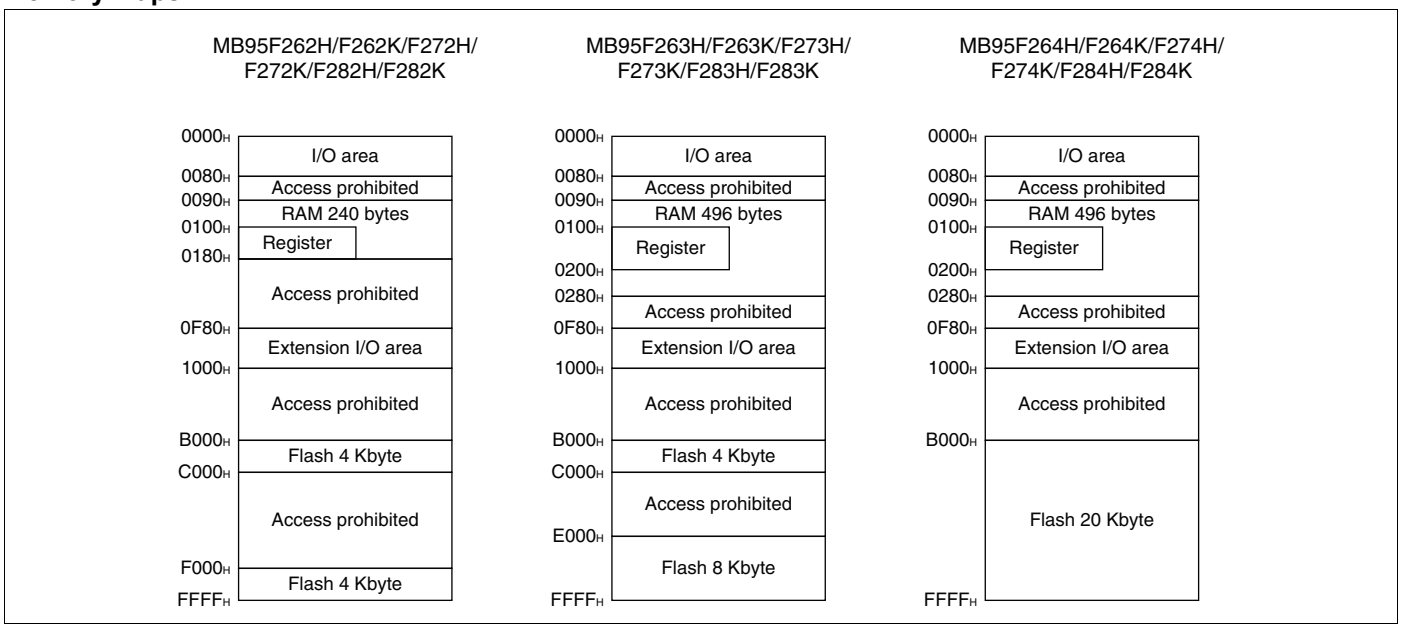
Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

17. CPU Core

Memory Space

The memory space of the MB95260H/270H/280H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95260H/270H/280H Series are shown below.

Memory Maps



18. I/O Map (MB95260H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000_B
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	$0000XXXX_B$
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FE6_H$, $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B
$0FE9_H$	CMCR	Clock monitoring control register	R/W	00000000_B
$0FEA_H$	CMDR	Clock monitoring data register	R/W	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (Upper)	R/W	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (Lower)	R/W	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$ to $0FFF_H$	—	(Disabled)	—	—

R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

19. I/O Map (MB95270H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	—	(Disabled)	—	—
0017_H	—	(Disabled)	—	—
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	—	(Disabled)	—	—
$002B_H$	—	(Disabled)	—	—
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	—	(Disabled)	—	—
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	—	(Disabled)	—	—
0039_H	—	(Disabled)	—	—
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	—	(Disabled)	—	—
0051_H	—	(Disabled)	—	—
0052_H	—	(Disabled)	—	—
0053_H	—	(Disabled)	—	—
0054_H	—	(Disabled)	—	—
0055_H	—	(Disabled)	—	—
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	$0000XXXX_B$
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	—	(Disabled)	—	—
$007C_H$	—	(Disabled)	—	—
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	—	(Disabled)	—	—
$0F98_H$	—	(Disabled)	—	—
$0F99_H$	—	(Disabled)	—	—
$0F9A_H$	—	(Disabled)	—	—
$0F9B_H$	—	(Disabled)	—	—
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	—	(Disabled)	—	—
$0FBD_H$	—	(Disabled)	—	—
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$
$0FE6_H$, $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FE9_H$	CMCR	Clock monitoring control register	R/W	00000000_B
$0FEA_H$	CMDR	Clock monitoring data register	R/W	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (Upper)	R/W	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (Lower)	R/W	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$ to $0FFF_H$	—	(Disabled)	—	—

R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

20. I/O Map (MB95280H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	—	(Disabled)	—	—
0017_H	—	(Disabled)	—	—
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	—	(Disabled)	—	—
0039_H	—	(Disabled)	—	—
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	$0000XXXX_B$
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F80_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	—	(Disabled)	—	—
$0F98_H$	—	(Disabled)	—	—
$0F99_H$	—	(Disabled)	—	—
$0F9A_H$	—	(Disabled)	—	—
$0F9B_H$	—	(Disabled)	—	—
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FE6_H$, $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B
$0FE9_H$	CMCR	Clock monitoring control register	R/W	00000000_B
$0FEA_H$	CMDR	Clock monitoring data register	R/W	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (Upper)	R/W	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (Lower)	R/W	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$ to $0FFF_H$	—	(Disabled)	—	—

R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

21. Interrupt Source Table (MB95260H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
—	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (Upper)	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
—	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (Lower)	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

22. Interrupt Source Table (MB95270H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
—	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
—	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
—	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
—					
—	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
—	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
—	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
—	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
—	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
—	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
—	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

23. Interrupt Source Table (MB95280H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
—	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
—	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
—	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
—	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

24. Electrical Characteristics

24.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} - 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} - 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} - 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	- 2	+ 2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63*4
	I_{OL2}		15		P05, P06, P62 and P63*4
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current= operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	- 15	mA	Other than P05, P06, P62 and P63*4
	I_{OH2}		- 15		P05, P06, P62 and P63*4
"H" level average current	I_{OHAV1}	—	- 4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OHAV2}		- 8		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	- 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	- 50	mA	Total average output current= operating current ´ operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	- 40	+ 85	°C	
Storage temperature	Tstg	- 55	+ 150	°C	

(Continued)

(Continued)

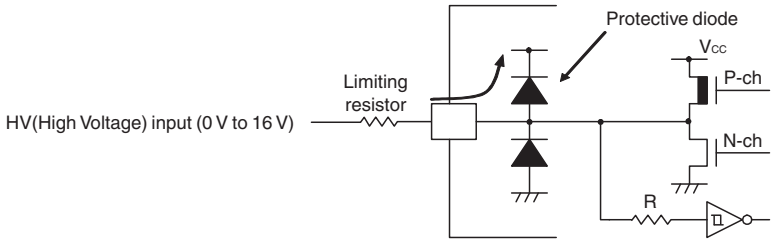
*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P62 to P64, PG1, PG2, PF0, PF1 (P00, P62, P63 and P64 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K. P01, P02, P03, P07, PG1, PG2, PF0 and PF1 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

Input/Output equivalent circuit



*4: P62 and P63 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

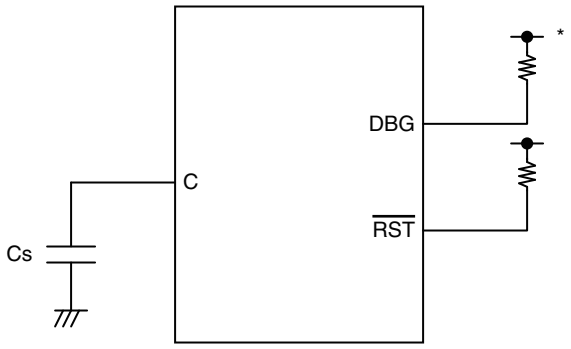
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	-40	+ 85	°C	Other than on-chip debug mode	
		+ 5	+ 35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

24.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P04	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04	*1	V_{SS} - 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	V_{SS} - 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} - 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	PF2, P12	—	V_{SS} - 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P05, P06, P12, P62, P63, PF2*2	I_{OH} = - 4 mA	V_{CC} - 0.5	—	—	V	
	V_{OH2}	P05, P06, P62, P63*2	I_{OH} = - 8 mA	V_{CC} - 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05, P06, P62, P63*2	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P05, P06, P62, P63*2	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	- 5	—	+ 5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00 to P07, PG1, PG2*3*4	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Except during Flash memory programming and erasing
				—	33.5	39.5	mA	During Flash memory programming and erasing
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = + 25°C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = + 25°C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25°C	—	5	30	µA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode	—	8.6	—	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = + 25°C	—	110	410	µA	

(Continued)

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(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Time-base timer mode T_A = + 25°C	—	1.1	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = + 25°C	—	3.5	22.5	µA	Main stop mode for single external clock selection
	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	37	54	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

*1: The input level of P04 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2: P62 and P63 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.

*3: P00 is only available on MB95F262H/F262K/F263H/F263K/F264H/F264K. P01, P02, P03, P07, PG1 and PG2 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K.

*4:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See “24.4. AC Characteristics: 24.4.1. Clock Timing” for F_{CH} and F_{CL}.
- See “24.4. AC Characteristics: 24.4.2. Source Clock / Machine Clock” for F_{MP} and F_{MPL}.

24.4 AC Characteristics

24.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1 : open	1	—	12	MHz	When the main external clock is used
		X0, X1	*1	1	—	32.5	MHz	
	F_{CRH}	—	—	9.7	10	10.3	MHz	When the main CR clock is used*2 3.3 V ≤ Vcc ≤ 5.5 V(-40 °C ≤ T_A ≤ + 40 °C) 2.4 V ≤ Vcc < 3.3 V(0 °C ≤ T_A ≤ + 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.55	10	10.45	MHz	When the main CR clock is used*2 3.3 V ≤ Vcc ≤ 5.5 V (+ 40 °C < T_A ≤ + 85 °C)
				7.64	8	8.36	MHz	
				0.955	1	1.045	MHz	
				9.5	10	10.5	MHz	When the main CR clock is used*2 2.4 V≤ Vcc < 3.3 V (-40 °C ≤ T_A < 0 °C, + 40 °C < T_A ≤ + 85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
				9.7	10	10.3	MHz	When the main CR clock is used*3 2.4 V ≤ Vcc ≤ 5.5 V(0 °C ≤ T_A ≤ + 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.5	10	10.5	MHz	When the main CR clock is used*3 2.4 V ≤ Vcc ≤ 5.5 V (-40 °C ≤ T_A < 0 °C, ＋40 °C < T_A ≤＋85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1 : open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*1	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used

(Continued)

(Continued)

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input clock pulse width	t_{WH1} t_{WL1}	X0	X1 : open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*1	12.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0	X1 : open	—	—	5	ns	When the external clock is used
		X0, X1	*1	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	80	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub CR clock is used

*1: The external clock signal is input to X0 and the inverted external clock signal to X1.

*2: These specifications are not applicable to the following products: MB95F272HPH, MB95F272KPH, MB95F273HPH, MB95F273KPH, MB95F274HPH, MB95F274KPH, MB95F282HPH, MB95F282KPH, MB95F283HPH, MB95F283KPH, MB95F284HPH and MB95F284KPH.

*3: These specifications are only applicable to the following products: MB95F272HPH, MB95F272KPH, MB95F273HPH, MB95F273KPH, MB95F274HPH, MB95F274KPH, MB95F282HPH, MB95F282KPH, MB95F283HPH, MB95F283KPH, MB95F284HPH and MB95F284KPH.

Input waveform generated when an external clock (main clock) is used

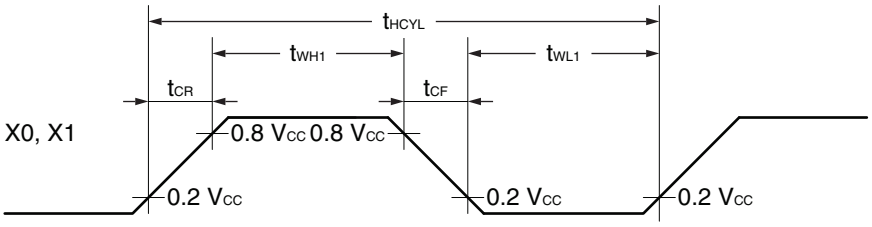
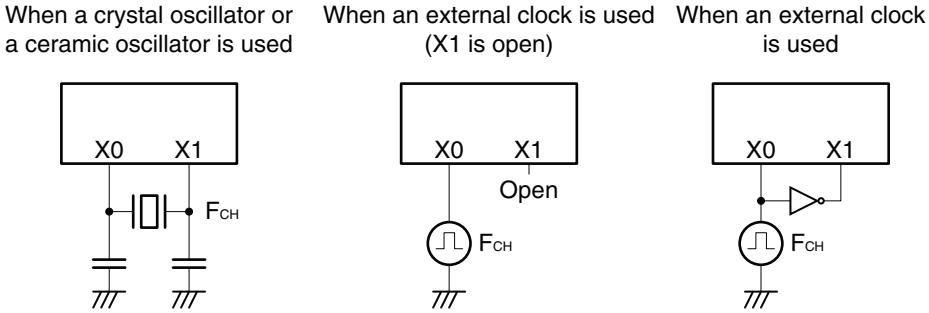


Figure of main clock input port external connection



Input waveform generated when an external clock (subclock) is used

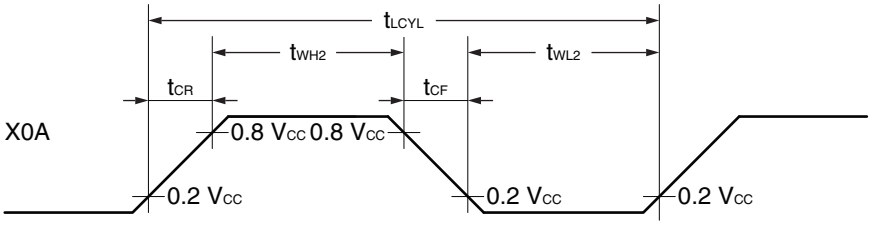
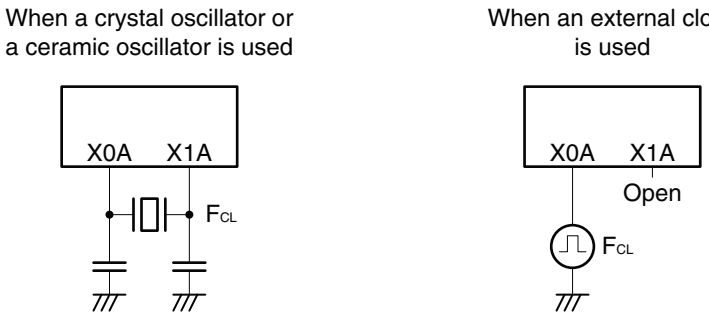


Figure of subclock input port external connection



24.4.2 Source Clock / Machine Clock

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			100	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 10 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	10	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			100	—	16000	ns	When the main CR clock is used Min: F_{SP} = 10 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	10	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

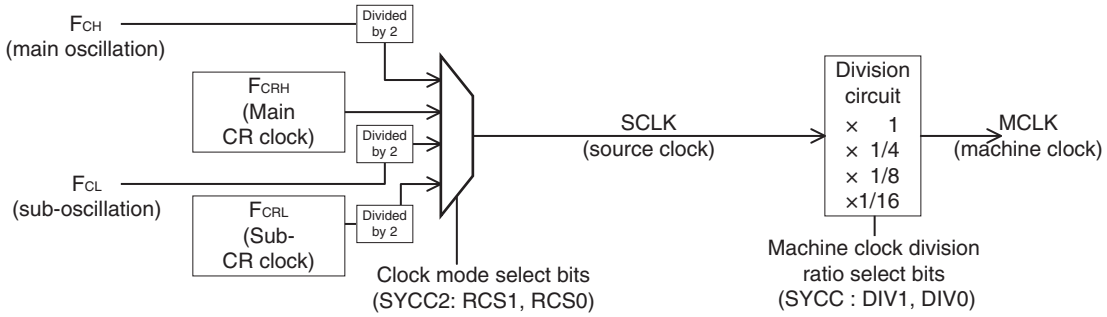
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC : DIV1 and DIV0) . This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC : DIV1 and DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

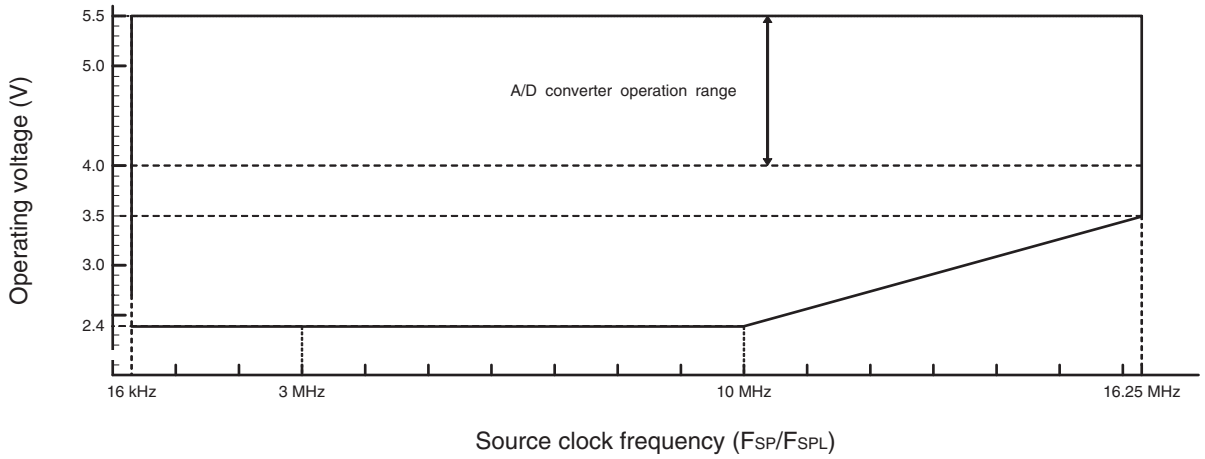
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

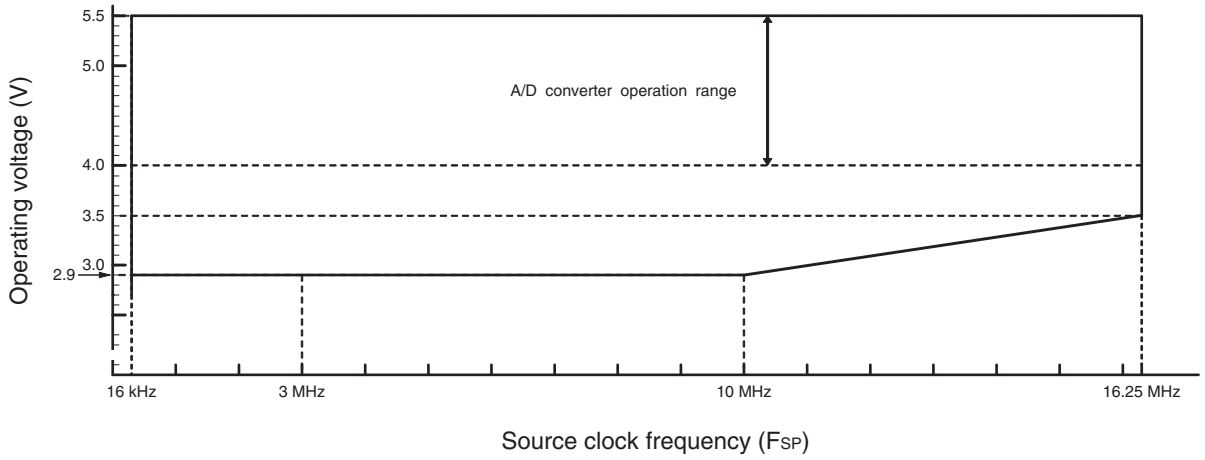
Schematic diagram of the clock generation block



Operating voltage - Operating frequency (When T_A = -40°C to + 85°C)
MB95260H/270H/280H (without the on-chip debug function)



Operating voltage - Operating frequency (When T_A = -40°C to + 85°C)
MB95260H/270H/280H (with the on-chip debug function)



24.4.3 External Reset

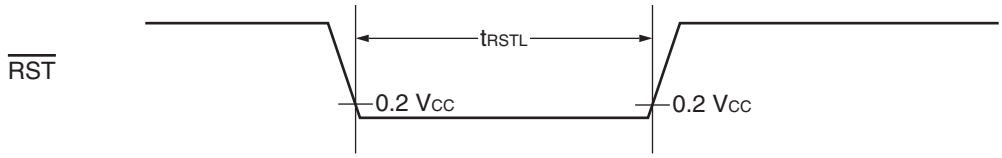
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, sub-sleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

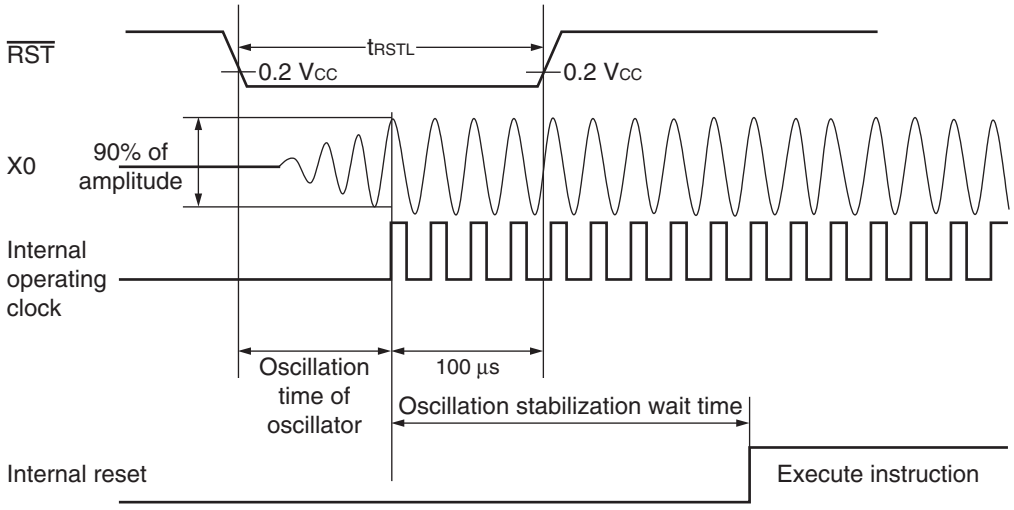
*1 : See "24.4.2. Source Clock / Machine Clock" for t_{MCLK}.

*2 : The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

In normal operation



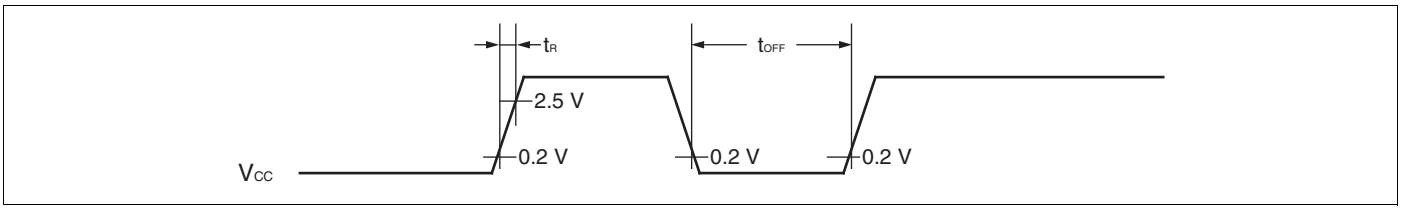
In stop mode, subclock mode,



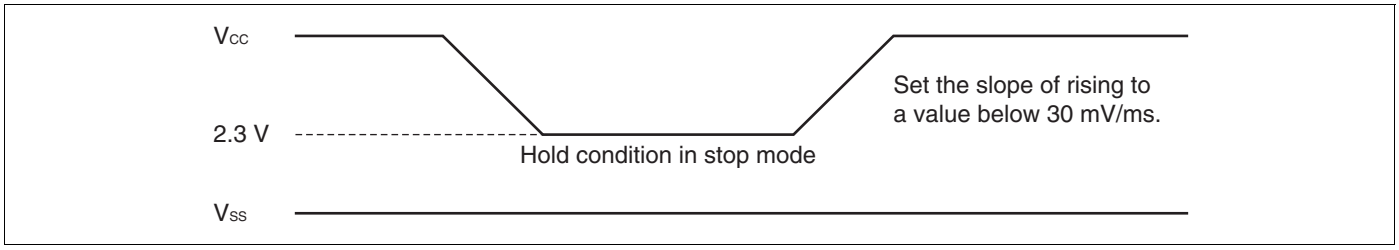
24.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



24.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

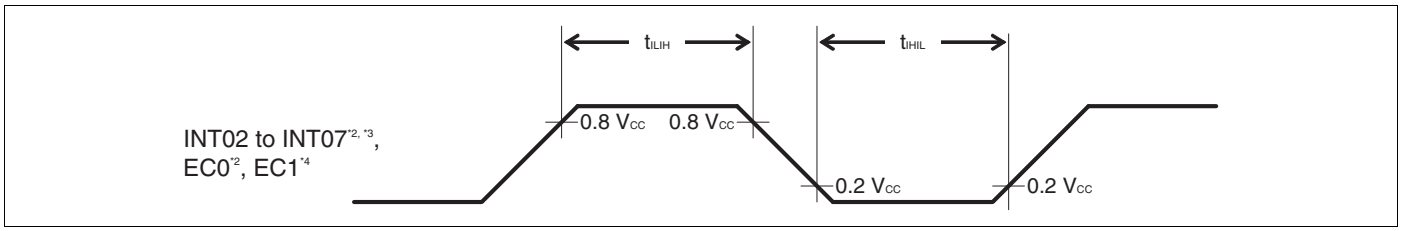
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT02 to INT07*2,*3, EC0*2, EC1*4	2 t_{MCLK}*1	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*1	—	ns

*1: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.

*2: INT04, INT06 and EC0 are available in all products.

*3: INT02, INT03, INT05 and INT07 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H /F283K/F284H/F284K.

*4: EC1 is only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.



24.4.6 LIN-UART Timing (only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H /F284K)

*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

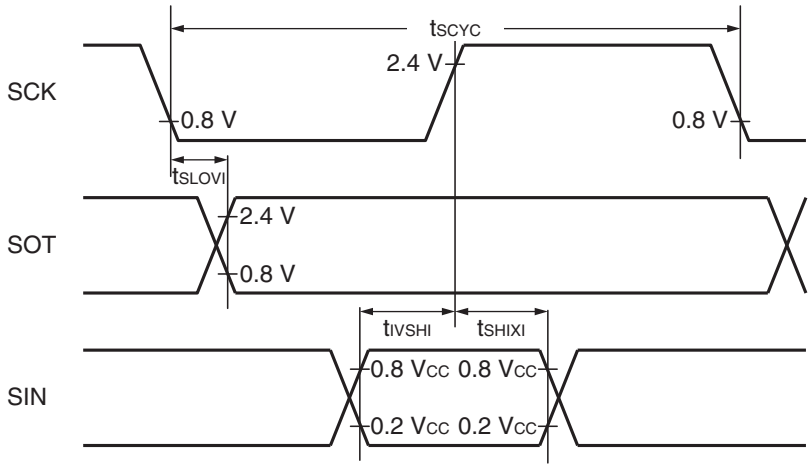
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 - t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

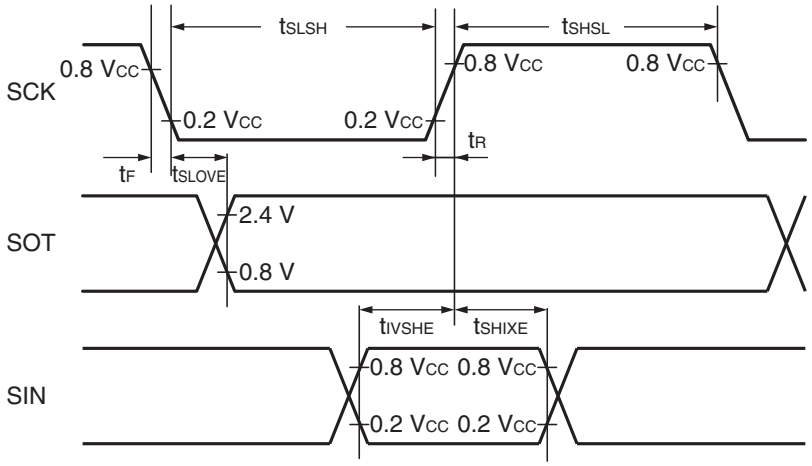
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.

Internal shift clock mode



External shift clock mode



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

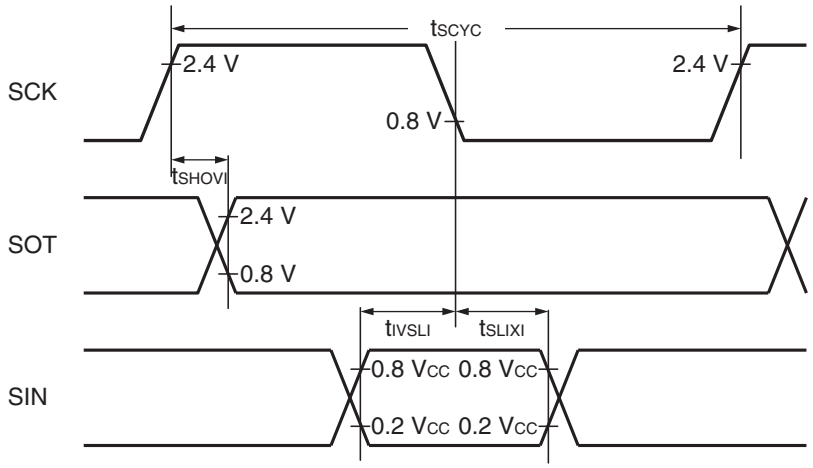
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 - t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑→ SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

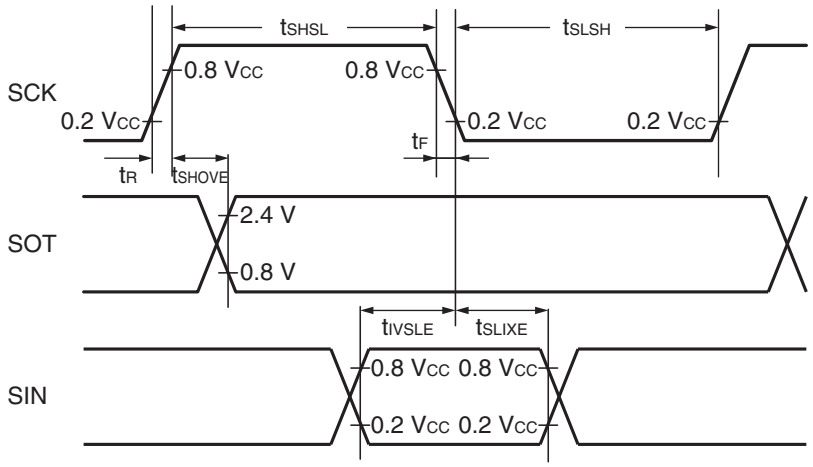
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.

Internal shift clock mode



External shift clock mode



*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

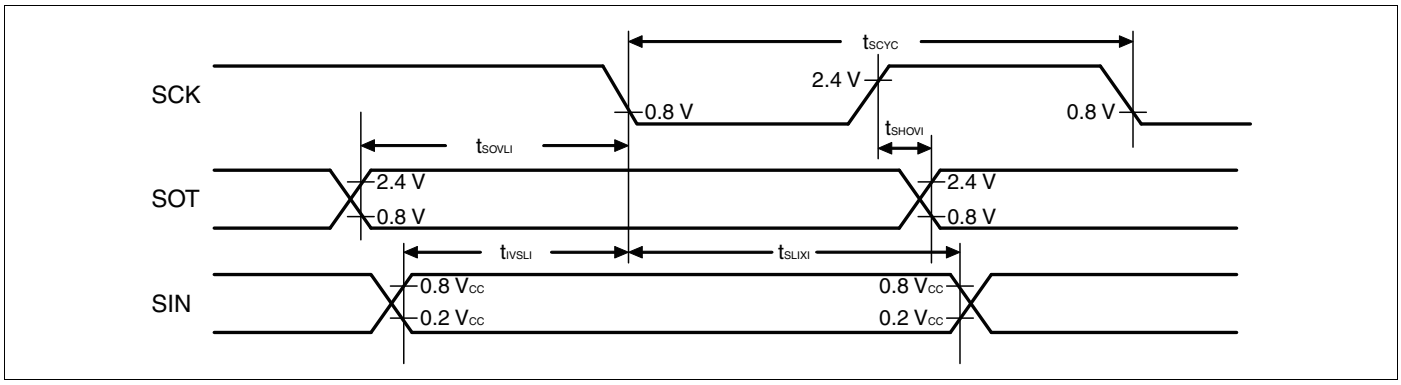
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

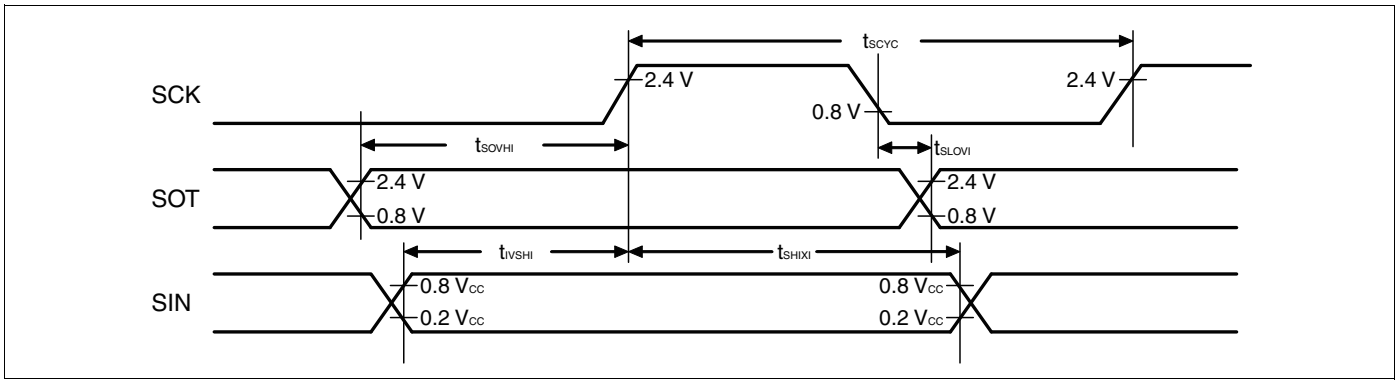
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1:There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

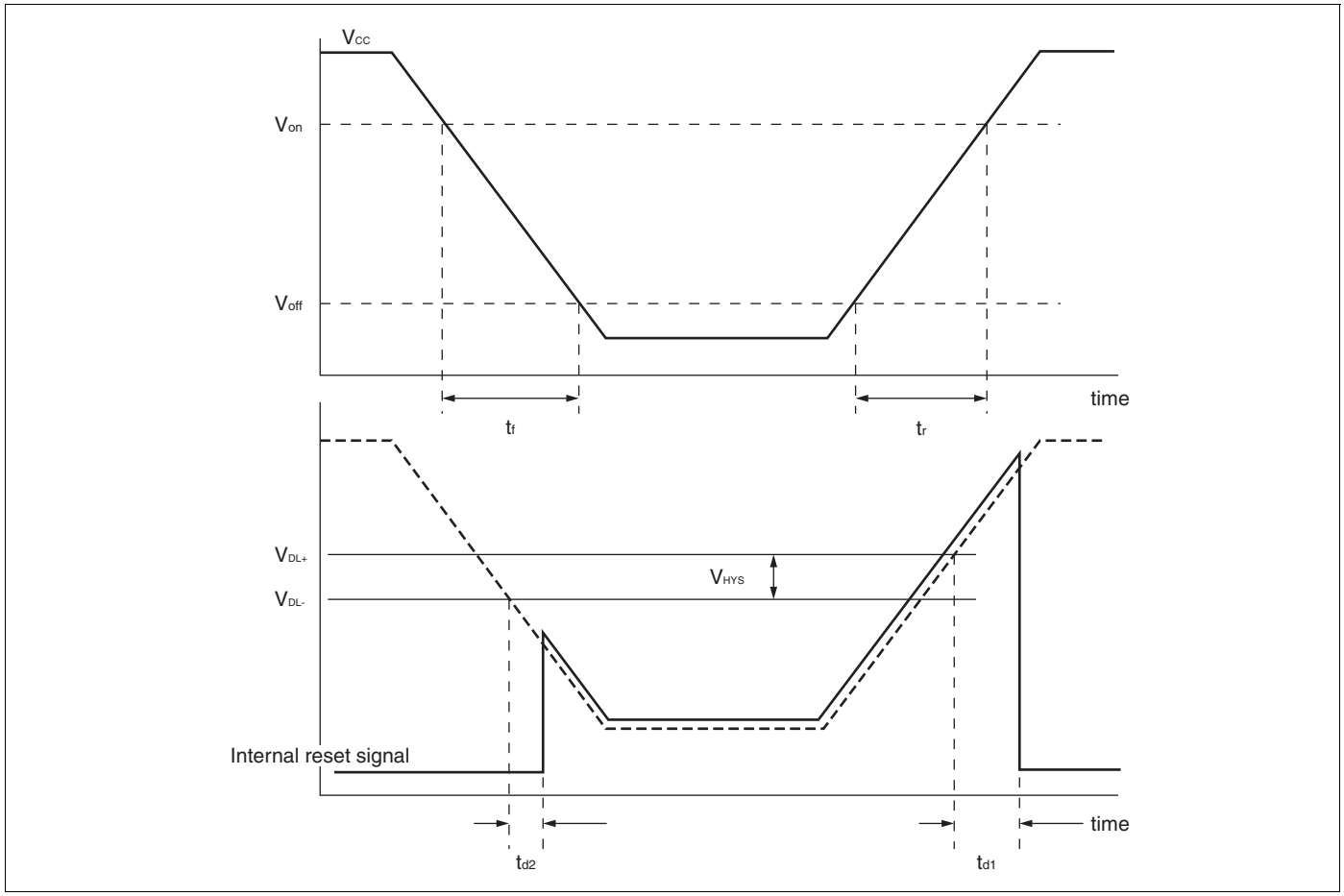
*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.



24.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	



24.5 A/D Converter

24.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

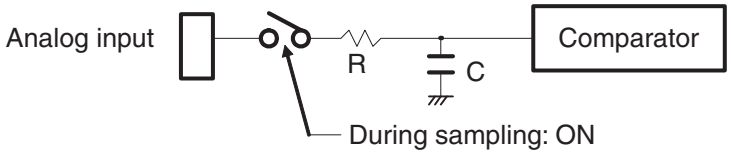
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		- 3	—	+ 3	LSB	
Linearity error		- 2.5	—	+ 2.5	LSB	
Differential linear error		- 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} - 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} - 4.5 LSB	V_{CC} - 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	- 0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

24.5.2 Notes on Using the A/D Converter

External impedance of analog input and its sampling time

The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

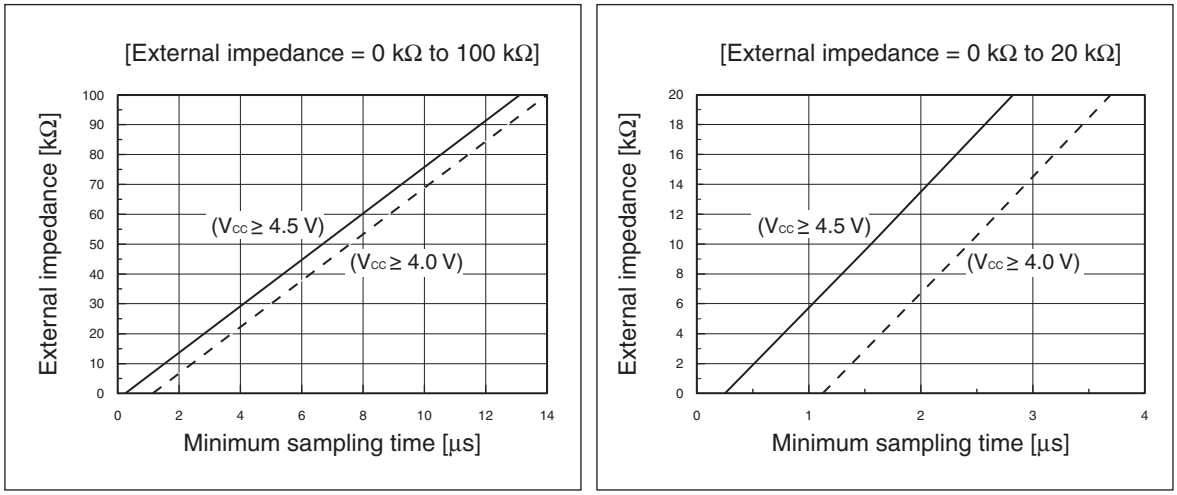
Analog input equivalent circuit



$4.5\ V \le V_{CC} \le 5.5\ V$: R ≈ 1.95 kΩ (Max), C ≈ 17 pF (Max)
$4.0\ V \le V_{CC} < 4.5\ V$: R ≈ 8.98 kΩ (Max), C ≈ 17 pF (Max)

Note: The values are reference values.

Relationship between external impedance and minimum sampling time



A/D conversion error

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

24.5.3 Definitions of A/D Converter Terms

Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.

Linearity error (unit: LSB)

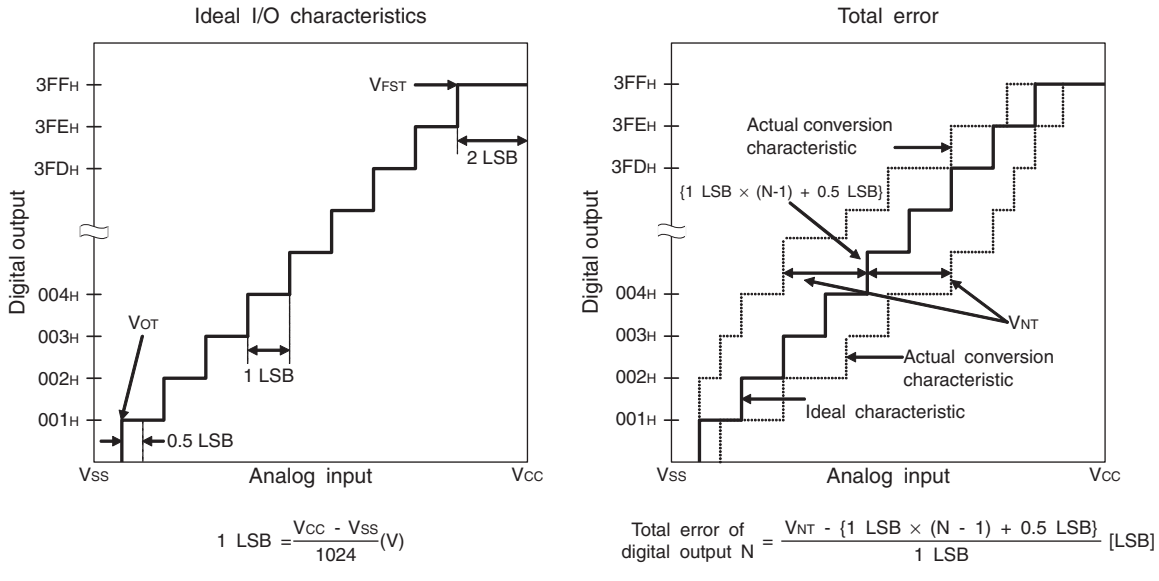
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") of the same device.

Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (V)$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

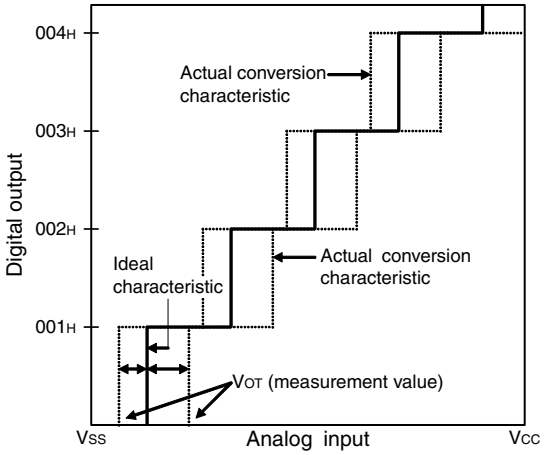
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

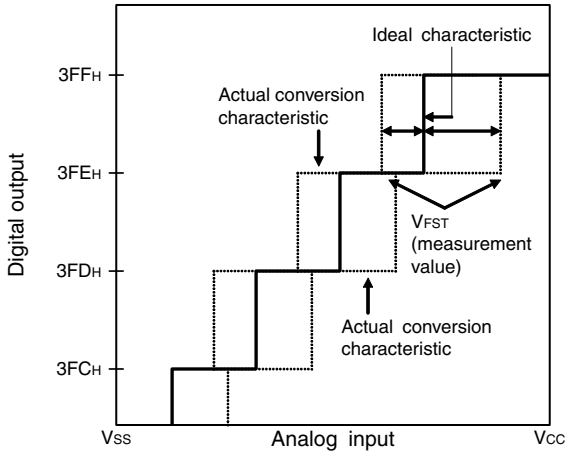
(Continued)

(Continued)

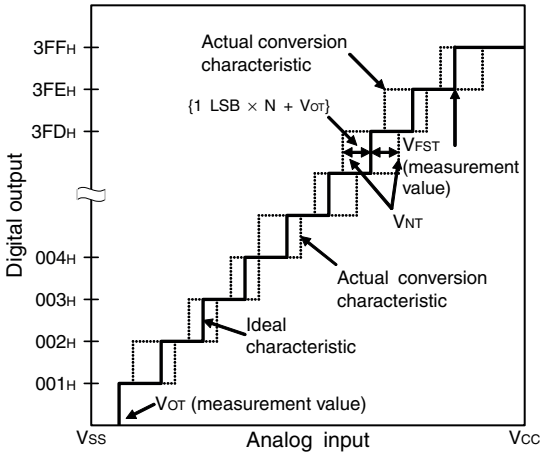
Zero transition error



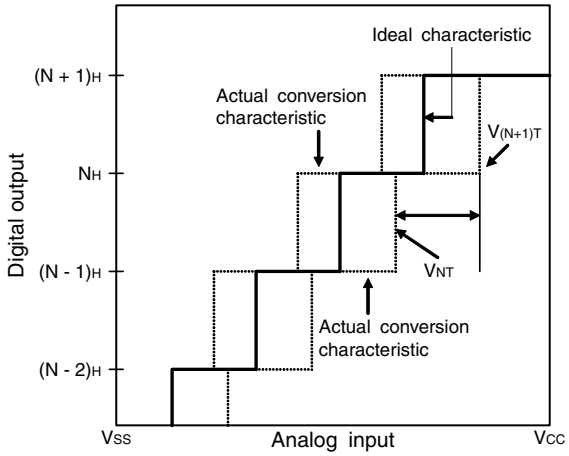
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

24.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of writing 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of writing 00_H prior to erasure is excluded.
Byte writing time	—	21	6100*2	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = + 85°C

*1: T_A = + 25°C, V_{CC} = 5.0 V, 100000 cycles

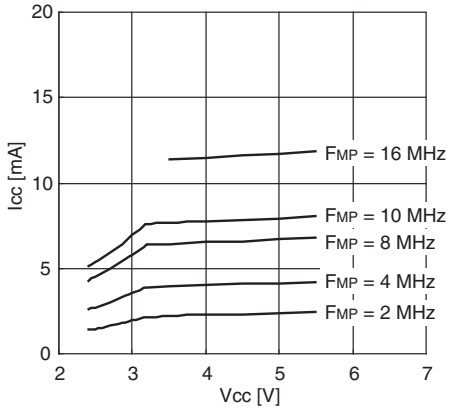
*2: T_A = + 85°C, V_{CC} = 3.0 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being + 85°C) .

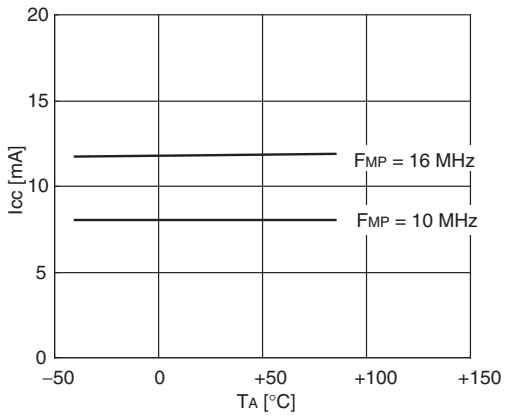
25. Sample Characteristics

Power supply current temperature

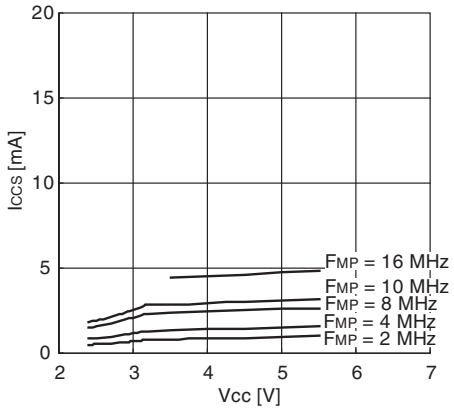
Icc - Vcc
T_A = + 25°C F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



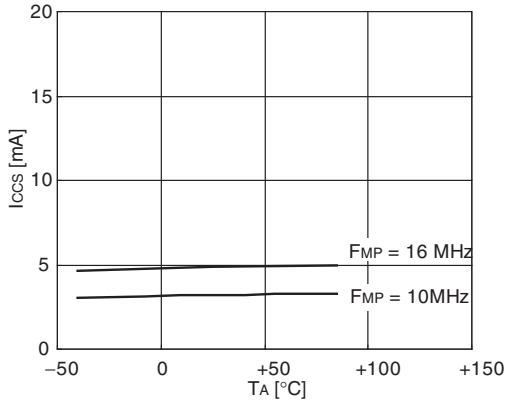
Icc - T_A
Vcc = 5.5 V F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



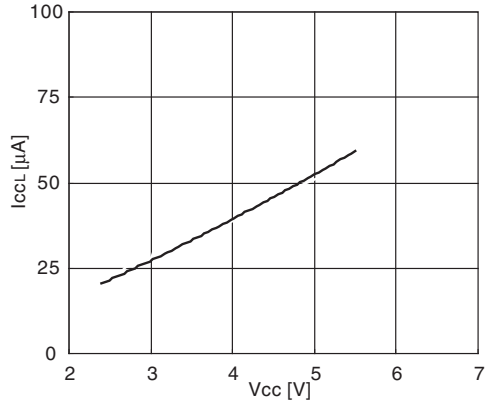
Iccs - Vcc
T_A = + 25°C F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



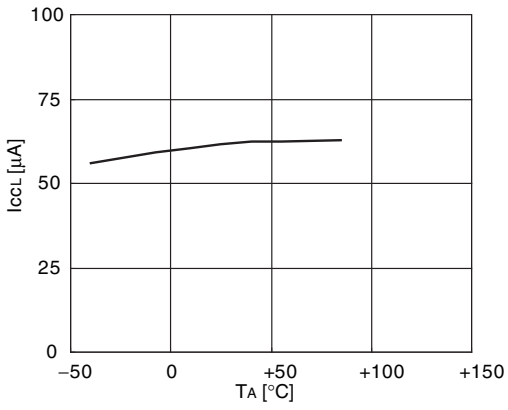
Iccs - T_A
Vcc = 5.5 V F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} - Vcc
T_A = + 25°C F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating

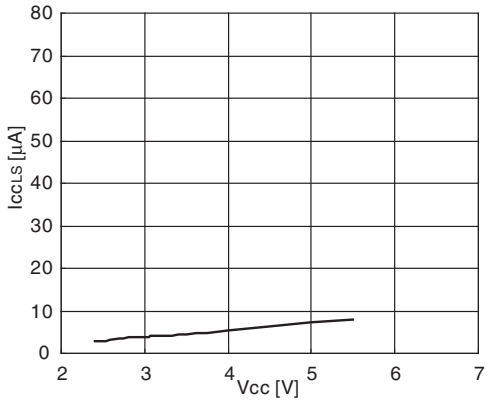


I_{CCL} - T_A
Vcc = 5.5 V F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating

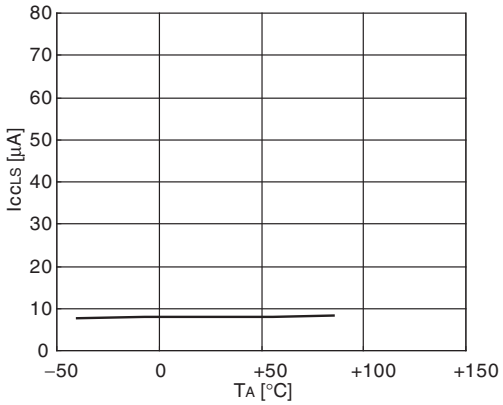


(Continued)

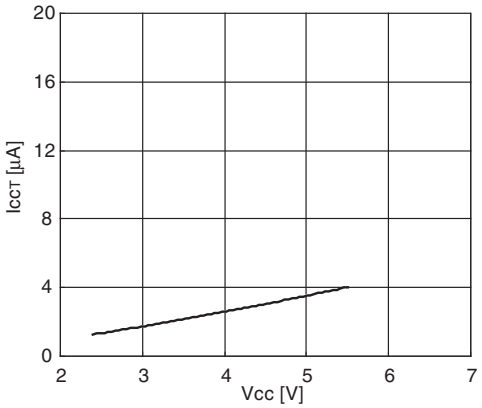
I_{CCLS} - Vcc
T_A = + 25°C F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



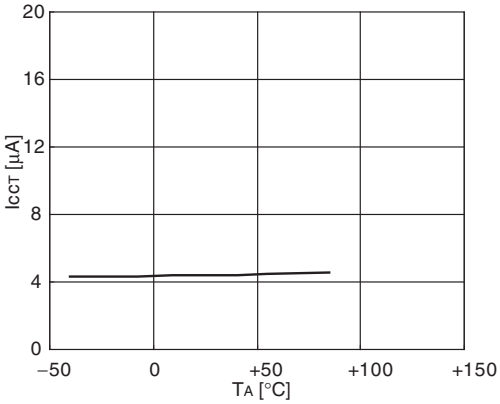
I_{CCLS} - T_A
Vcc = 5.5 V F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



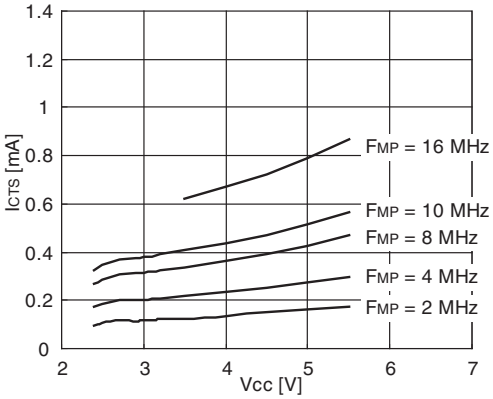
I_{CCT} - Vcc
T_A = + 25°C F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



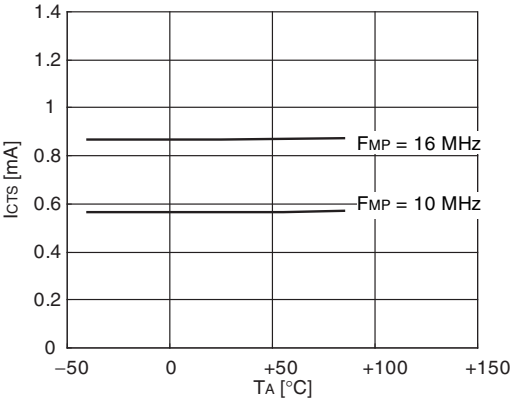
I_{CCT} - T_A
Vcc = 5.5 V F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CTS} - Vcc
T_A = + 25°C F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



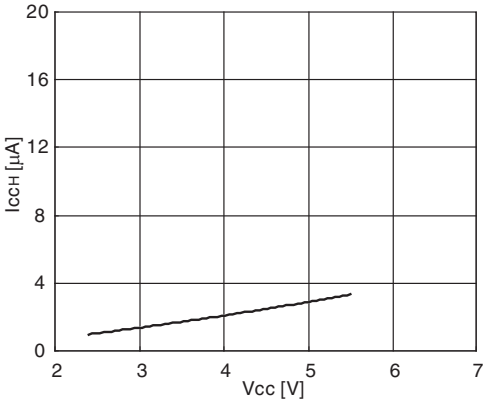
I_{CTS} - T_A
Vcc = 5.5 V F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



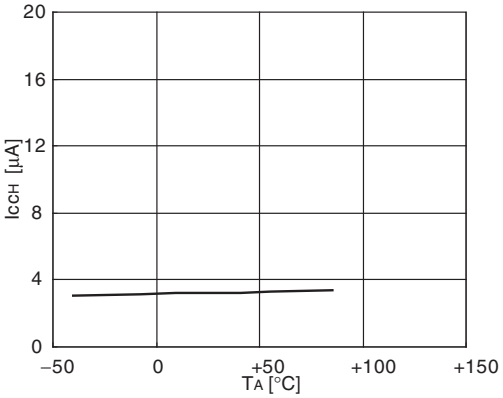
(Continued)

(Continued)

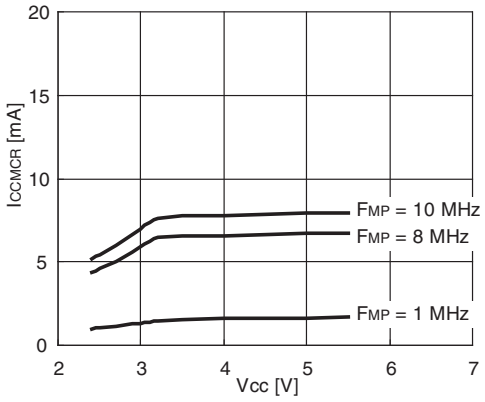
I_{CCH} - Vcc
T_A = + 25°C F_{MPL} = (stop)
Substop mode with the external clock stopping



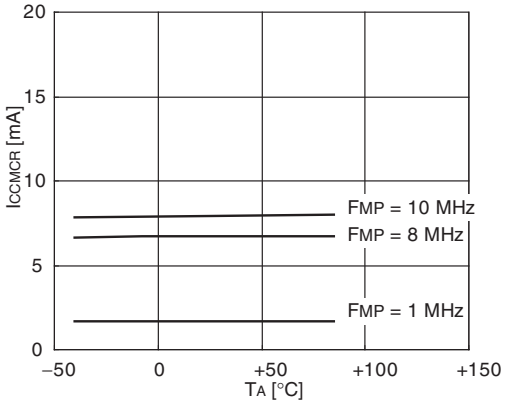
I_{CCH} - T_A
Vcc = 5.5 V F_{MPL} = (stop)
Substop mode with the external clock stopping



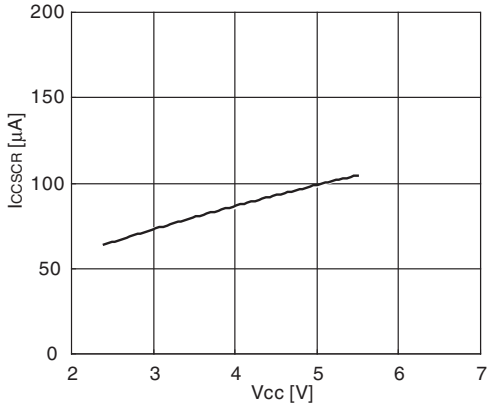
I_{CCMCR} - Vcc
T_A = + 25°C F_{MP} = 1, 8, 10 MHz (no division)
Main clock mode
with the main CR clock operating



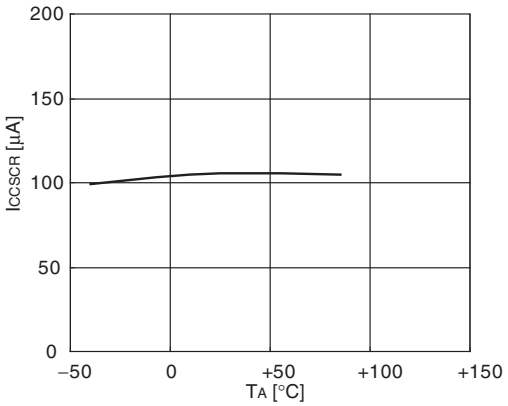
I_{CCMCR} - T_A
Vcc = 5.5 V F_{MP} = 1, 8, 10 MHz (no division)
Main clock mode
with the main CR clock operating



I_{CCSCR} - Vcc
T_A = + 25°C F_{MPL} = 50 kHz (divided by 2)
Subclock mode with
the sub-CR clock operating

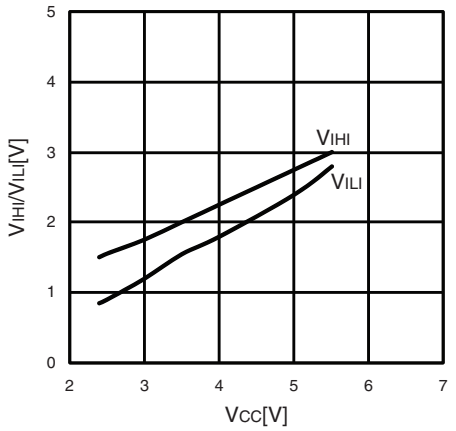


I_{CCSCR} - T_A
Vcc = 5.5 V F_{MPL} = 50 kHz (divided by 2)
Subclock mode with
the sub-CR clock operating

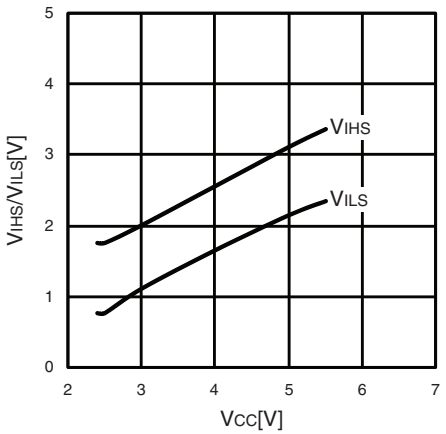


Input voltage

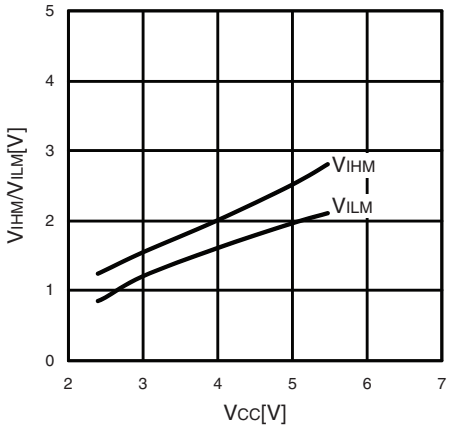
VIHI - VCC and VILI - VCC
TA=+25°C



VIHS - VCC and VILS - VCC
TA=+25°C

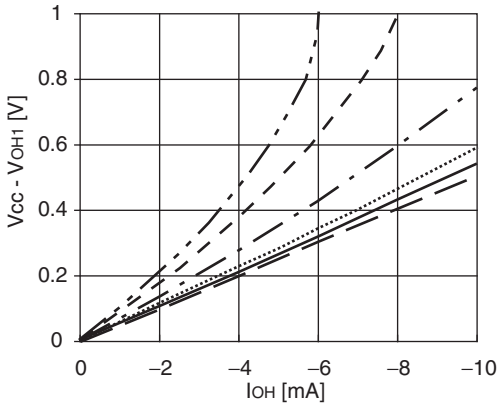


VIHM - VCC and VILM - VCC
TA=+25°C



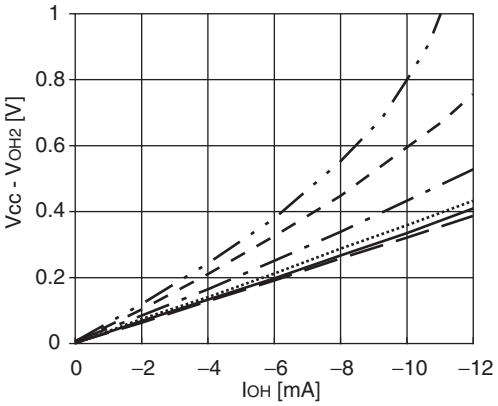
Output voltage

$(Vcc - V_{OH1}) - I_{OH}$
$T_A = +25°C$



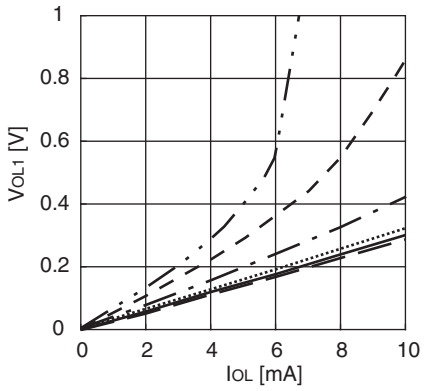
Vcc = 2.4 V
Vcc = 2.7 V
Vcc = 3.5 V
Vcc = 4.5 V
Vcc = 5.0 V
Vcc = 5.5 V

$(Vcc - V_{OH2}) - I_{OH}$
$T_A = +25°C$



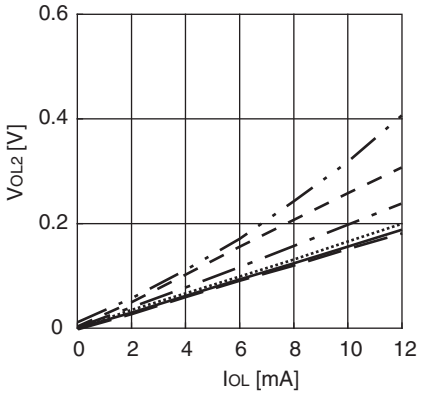
Vcc = 2.4 V
Vcc = 2.7 V
Vcc = 3.5 V
Vcc = 4.5 V
Vcc = 5.0 V
Vcc = 5.5 V

$V_{OL1} - I_{OL}$
$T_A = +25°C$



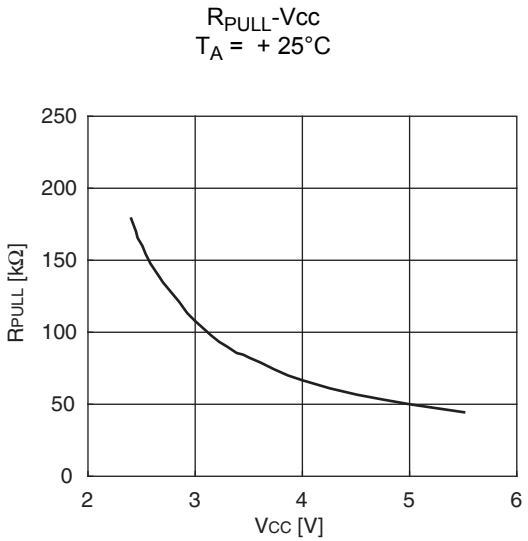
Vcc = 2.4 V
Vcc = 2.7 V
Vcc = 3.5 V
Vcc = 4.5 V
Vcc = 5.0 V
Vcc = 5.5 V

$V_{OL2} - I_{OL}$
$T_A = +25°C$



Vcc = 2.4 V
Vcc = 2.7 V
Vcc = 3.5 V
Vcc = 4.5 V
Vcc = 5.0 V
Vcc = 5.5 V

Pull-up



26. Mask Options

No.	Part Number	MB95F262H MB95F263H MB95F264H MB95F272H MB95F273H MB95F274H MB95F282H MB95F283H MB95F284H	MB95F262K MB95F263K MB95F264K MB95F272K MB95F273K MB95F274K MB95F282K MB95F283K MB95F284K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

27. Ordering Information

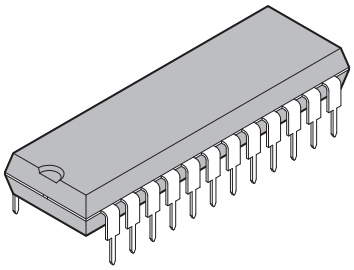
Part Number	Package
MB95F262HWQN-G-SNE1 MB95F262HWQN-G-SNERE1 MB95F262KWQN-G-SNE1 MB95F262KWQN-G-SNERE1 MB95F263HWQN-G-SNE1 MB95F263HWQN-G-SNERE1 MB95F263KWQN-G-SNE1 MB95F263KWQN-G-SNERE1 MB95F264HWQN-G-SNE1 MB95F264HWQN-G-SNERE1 MB95F264KWQN-G-SNE1 MB95F264KWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F262HP-G-SH-SNE2 MB95F262KP-G-SH-SNE2 MB95F263HP-G-SH-SNE2 MB95F263KP-G-SH-SNE2 MB95F264HP-G-SH-SNE2 MB95F264KP-G-SH-SNE2	24-pin plastic SDIP (DIP-24P-M07)
MB95F262HPF-G-SNE2 MB95F262KPF-G-SNE2 MB95F263HPF-G-SNE2 MB95F263KPF-G-SNE2 MB95F264HPF-G-SNE2 MB95F264KPF-G-SNE2	20-pin plastic SOP (FPT-20P-M09)
MB95F262HPFT-G-SNE2 MB95F262KPFT-G-SNE2 MB95F263HPFT-G-SNE2 MB95F263KPFT-G-SNE2 MB95F264HPFT-G-SNE2 MB95F264KPFT-G-SNE2	20-pin plastic TSSOP (FPT-20P-M10)
MB95F282HWQN-G-SNE1 MB95F282HWQN-G-SNERE1 MB95F282KWQN-G-SNE1 MB95F282KWQN-G-SNERE1 MB95F283HWQN-G-SNE1 MB95F283HWQN-G-SNERE1 MB95F283KWQN-G-SNE1 MB95F283KWQN-G-SNERE1 MB95F284HWQN-G-SNE1 MB95F284HWQN-G-SNERE1 MB95F284KWQN-G-SNE1 MB95F284KWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F282HPH-G-SNE2 MB95F282KPH-G-SNE2 MB95F283HPH-G-SNE2 MB95F283KPH-G-SNE2 MB95F284HPH-G-SNE2 MB95F284KPH-G-SNE2	16-pin plastic DIP (DIP-16P-M06)

(Continued)

(Continued)

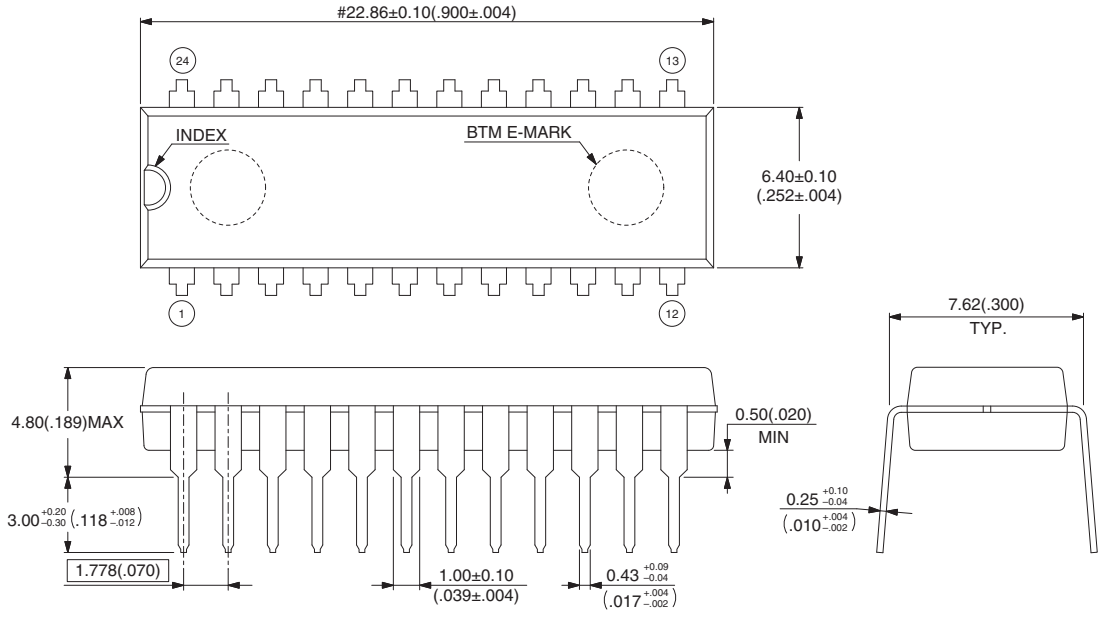
Part Number	Package
MB95F282HPF-G-SNE1 MB95F282KPF-G-SNE1 MB95F283HPF-G-SNE1 MB95F283KPF-G-SNE1 MB95F284HPF-G-SNE1 MB95F284KPF-G-SNE1	16-pin plastic SOP (FPT-16P-M06)
MB95F272HPH-G-SNE2 MB95F272KPH-G-SNE2 MB95F273HPH-G-SNE2 MB95F273KPH-G-SNE2 MB95F274HPH-G-SNE2 MB95F274KPH-G-SNE2	8-pin plastic DIP (DIP-8P-M03)
MB95F272HPF-G-SNE2 MB95F272KPF-G-SNE2 MB95F273HPF-G-SNE2 MB95F273KPF-G-SNE2 MB95F274HPF-G-SNE2 MB95F274KPF-G-SNE2	8-pin plastic SOP (FPT-8P-M08)

28. Package Dimension

24-pin plastic SDIP  (DIP-24P-M07)	Lead pitch	1.778 mm
	Package width × package length	6.40 mm × 22.86 mm
	Sealing method	Plastic mold
	Mounting height	4.80 mm Max

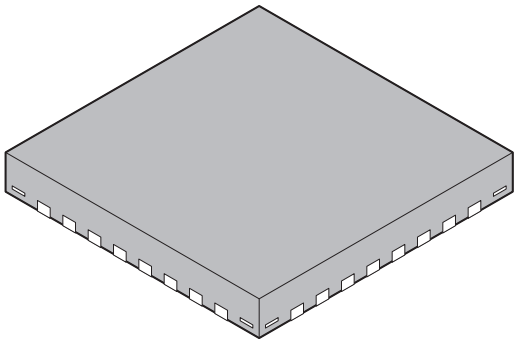
24-pin plastic SDIP
(DIP-24P-M07)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.

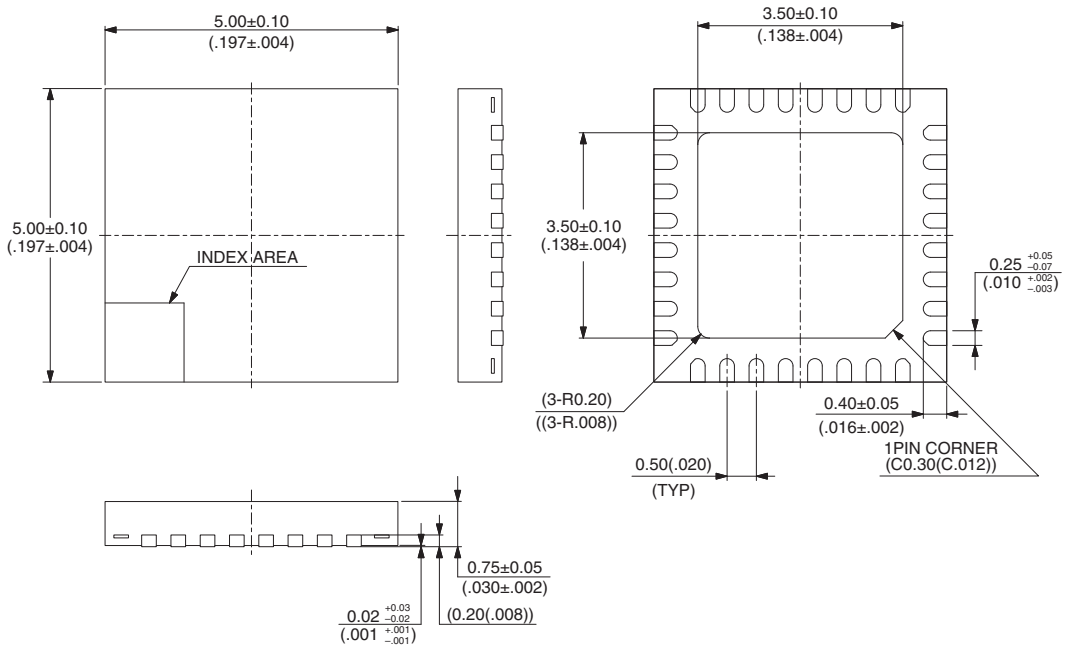


Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

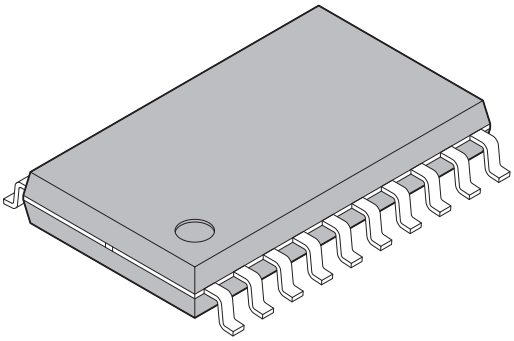
32-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g
(LCC-32P-M19)		

32-pin plastic QFN
(LCC-32P-M19)



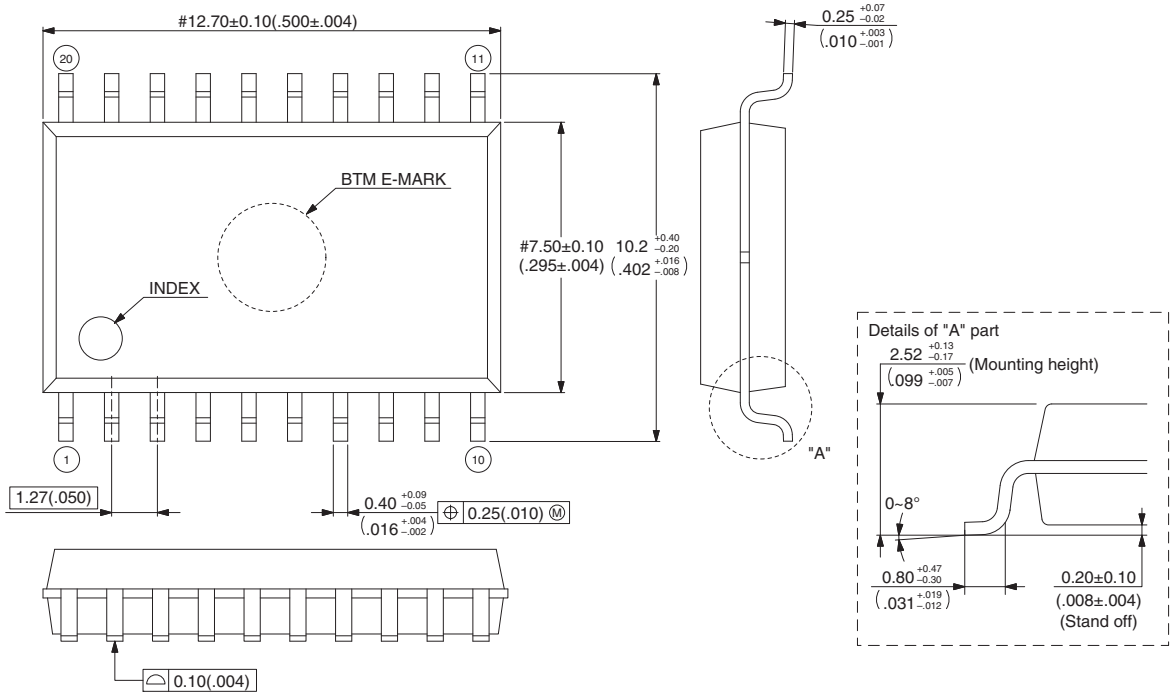
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

20-pin plastic SOP		
 (FPT-20P-M09)	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 12.70 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.65 mm Max

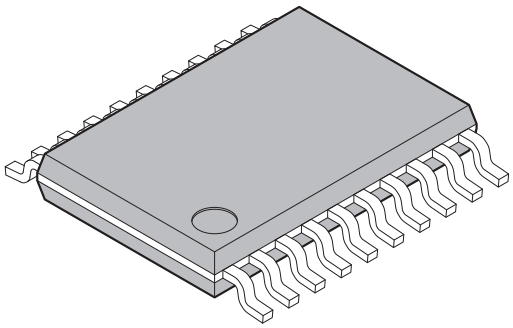
20-pin plastic SOP
(FPT-20P-M09)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



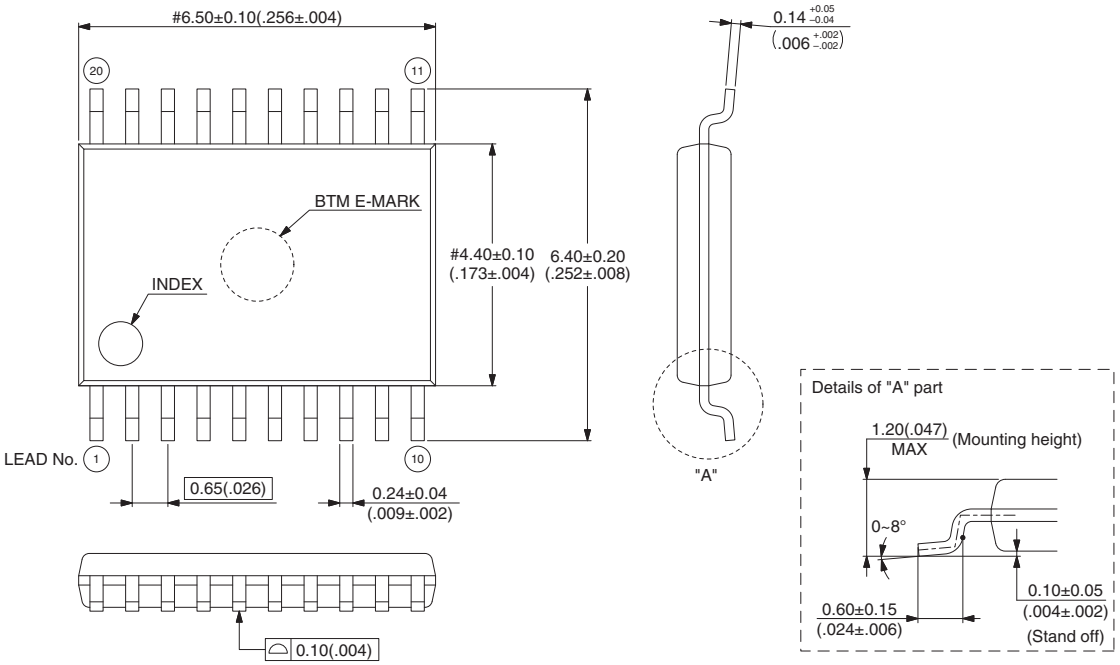
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

20-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.08 g
(FPT-20P-M10)		

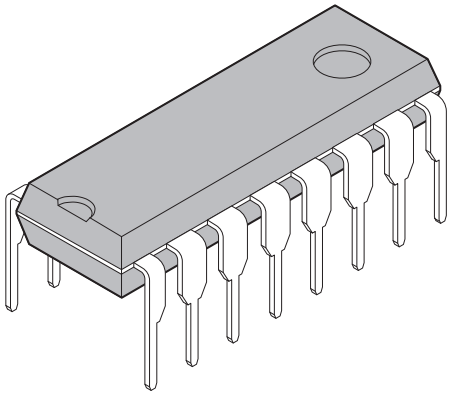
20-pin plastic TSSOP
(FPT-20P-M10)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.

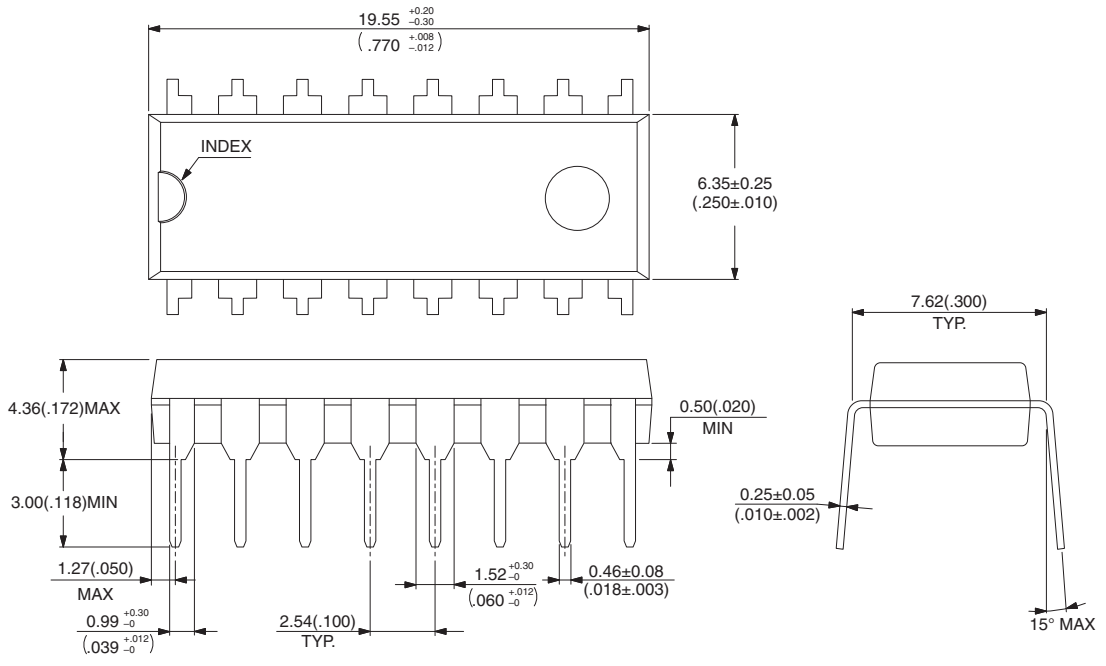


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

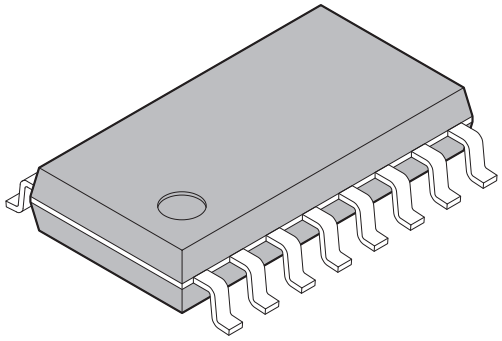
16-pin plastic DIP	Lead pitch	2.54 mm
	Sealing method	Plastic mold
(DIP-16P-M06)		

16-pin plastic DIP
(DIP-16P-M06)



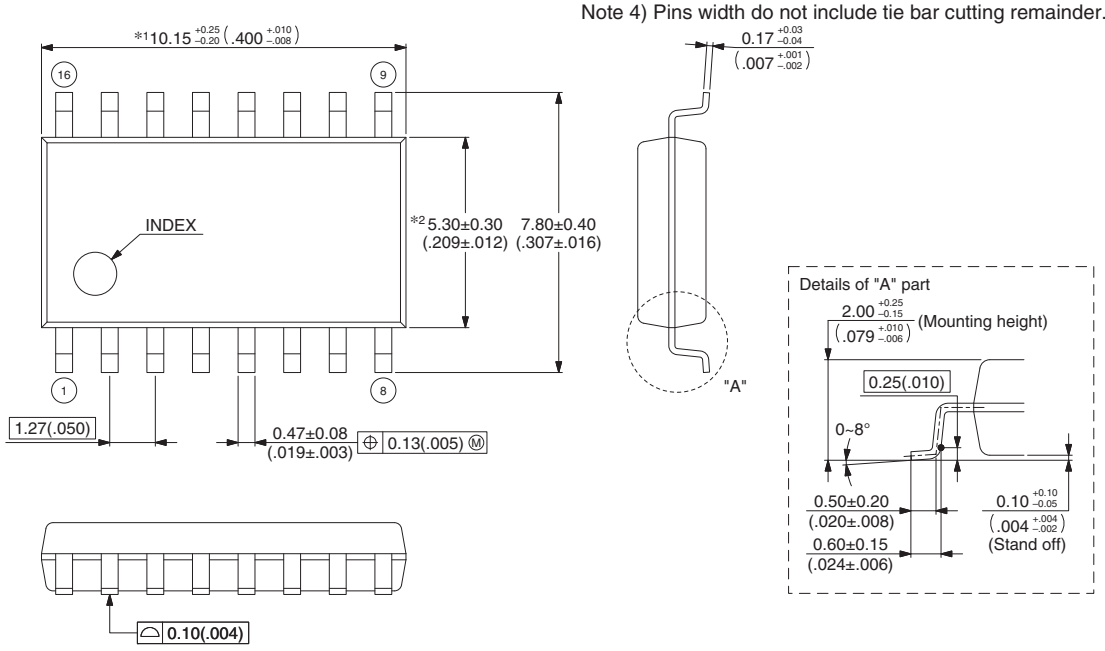
Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

16-pin plastic SOP		
	Lead pitch	1.27 mm
	Package width × package length	5.3 × 10.15 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	2.25 mm MAX
	Weight	0.20 g
(FPT-16P-M06)	Code (Reference)	P-SOP16-5.3×10.15-1.27

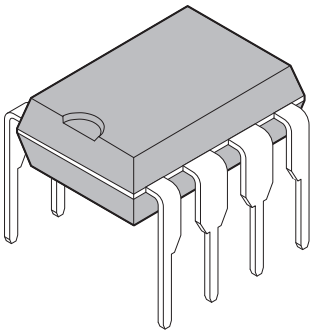
16-pin plastic SOP
(FPT-16P-M06)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.

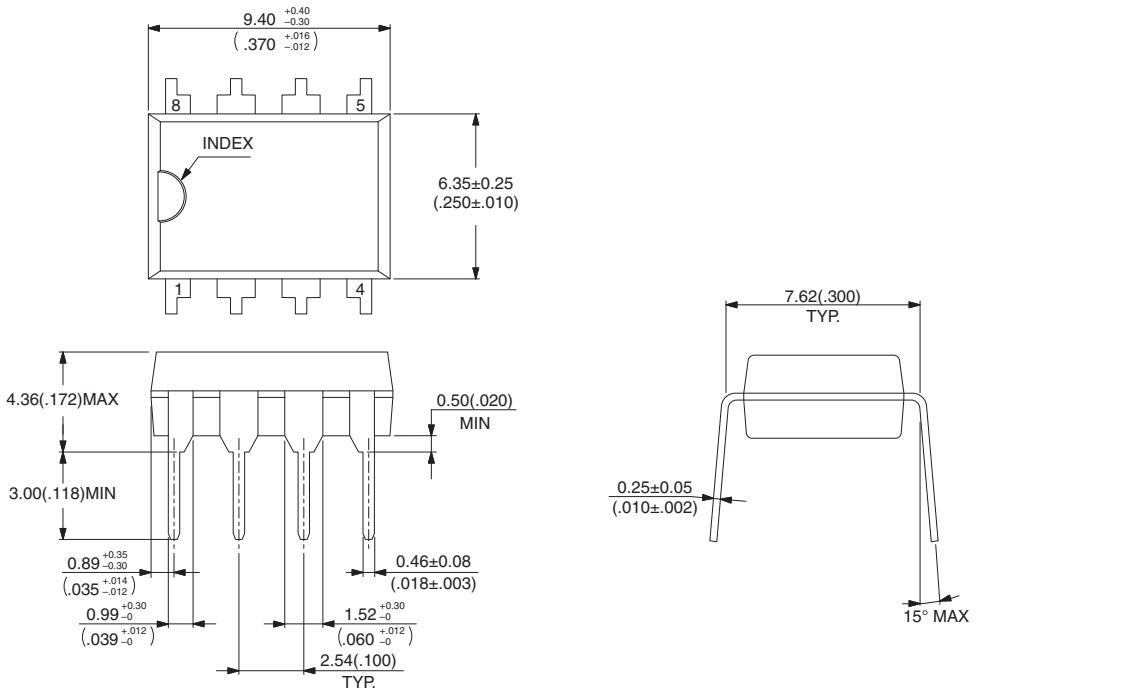


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

8-pin plastic DIP	Lead pitch	2.54 mm
	Sealing method	Plastic mold
(DIP-8P-M03)		

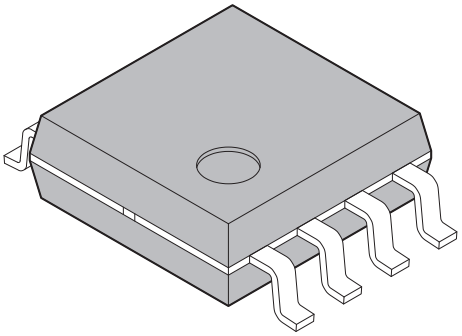
8-pin plastic DIP
(DIP-8P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values

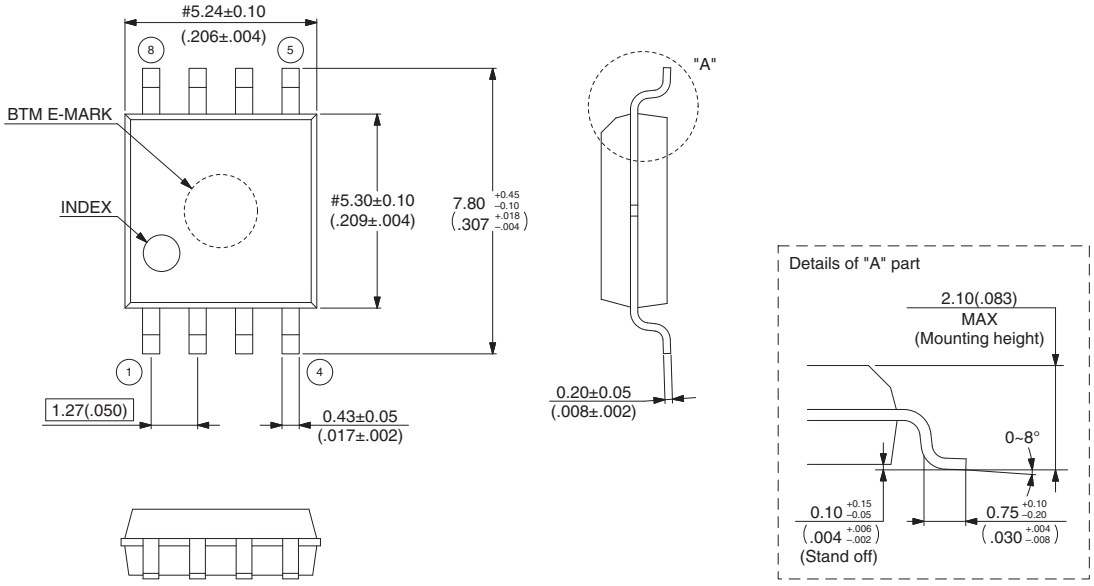
(Continued)

(Continued)

8-pin plastic SOP		
 (FPT-8P-M08)	Lead pitch	1.27 mm
	Package width × package length	5.30 mm × 5.24 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.10 mm Max

8-pin plastic SOP
(FPT-8P-M08)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

29. Major Changes

Spansion Publication Number: DS07–12627–7E

Page	Section	Details
1	—	Changed the family name. F^2MC-8FX → New 8FX
2	Features	Added “• Power-on reset”.
3	Product Line-up MB95260H Series	Added the parameter “Power-on reset”.
5	Product Line-up MB95270H Series	Added the parameter “Power-on reset”.
6	Product Line-up MB95280H Series	Added the parameter “Power-on reset”.
10	Pin Assignment	Deleted the HCLK1 pin and the HCLK2 pin.
11		Deleted the HCLK1 pin and the HCLK2 pin.
13	Pin Description (MB95260H Series, 32 pins)	Deleted the HCLK1 pin and the HCLK2 pin.
15	Pin Description (MB95260H Series, 24 pins)	Deleted the HCLK1 pin and the HCLK2 pin.
17	Pin Description (MB95260H Series, 20 pins)	Deleted the HCLK1 pin and the HCLK2 pin.
18	Pin Description (MB95270H Series, 8 pins)	Deleted the HCLK1 pin and the HCLK2 pin.
19	Pin Description (MB95280H Series, 32 pins)	Deleted the HCLK1 pin.
20		Deleted the HCLK2 pin.
21	Pin Description (MB95280H Series, 16 pins)	Deleted the HCLK1 pin.
22		Deleted the HCLK2 pin.
27	Block Diagram (MB95260H Series)	Deleted the HCLK1 pin and the HCLK2 pin.
28	Block Diagram (MB95270H Series)	Deleted the HCLK1 pin and the HCLK2 pin.
29	Block Diagram (MB95280H Series)	Deleted the HCLK1 pin and the HCLK2 pin.
52, 53	Electrical Characteristics 4. AC Characteristics (1) Clock Timing	Deleted all information about the HCLK1 pin and the HCLK2 pin in the table.
54		Deleted the HCLK1 pin and the HCLK2 pin in the “ Input waveform generated when an external clock (main clock) is used”. Deleted the external connection diagram for the HCLK1 pin and the HCLK2 pin in “ Figure of main clock input port external connection”.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB95260H/270H/280H Series New 8FX 8-bit Microcontrollers Document Number: 002-07516				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	07/04/2011	Migrated to Cypress and assigned document number 002-07516. No change to document contents or format.
*A	5199019	AKIH	04/04/2016	Updated to Cypress format.
*B	5861649	YSAT	08/24/2017	Adapted new Cypress logo

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