FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13809-1E

*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC-16FX MB96390 Series

# MB96F395*1

## ■ DESCRIPTION

MB96390 series is based on Fujitsu's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 40MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 25ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

Note: F²MC is the abbreviation of Fujitsu Flexible Microcontroller

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/


2009.7

## ■ FEATURES

| Feature | Description |
|---|---|
| Technology | • 0.18µm CMOS |
| CPU | • F²MC-16FX CPU<br>• Up to 40 MHz internal, 25 ns instruction cycle time<br>• Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)<br>• 8-byte instruction execution queue<br>• Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available |
| System clock | • On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)<br>• 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).<br>• Up to 40 MHz external clock<br>• 32-100 kHz subsystem quartz clock<br>• 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog<br>• Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.<br>• Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)<br>• Clock modulator |
| On-chip voltage regulator | • Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures |
| Low voltage reset | • Reset is generated when supply voltage is below minimum. |
| Code Security | • Protects ROM content from unintended read-out |
| Memory Patch Function | • Replaces ROM content<br>• Can also be used to implement embedded debug support |
| Interrupts | • Fast Interrupt processing<br>• 8 programmable priority levels<br>• Non-Maskable Interrupt (NMI) |
| Timers | • Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)<br>• Watchdog Timer |

| Feature | Description |
|---|---|
| CAN | • Supports CAN protocol version 2.0 part A and B<br>• ISO16845 certified<br>• Bit rates up to 1 Mbit/s<br>• 32 message objects<br>• Each message object has its own identifier mask<br>• Programmable FIFO mode (concatenation of message objects)<br>• Maskable interrupt<br>• Disabled Automatic Retransmission mode for Time Triggered CAN applications<br>• Programmable loop-back mode for self-test operation |
| USART | • Full duplex USARTs (SCI/LIN)<br>• Wide range of baud rate settings using a dedicated reload timer<br>• Special synchronous options for adapting to different synchronous serial protocols<br>• LIN functionality working either as master or slave LIN device |
| $I^2C$ | • Up to 400 kbps<br>• Master and Slave functionality, 8-bit and 10-bit addressing |
| A/D converter | • SAR-type<br>• 10-bit resolution<br>• Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer |
| Reload Timers | • 16-bit wide<br>• Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency<br>• Event count function |
| Free Running Timers | • Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency |
| Input Capture Units | • 16-bit wide<br>• Signals an interrupt upon external event<br>• Rising edge, falling edge or rising & falling edge sensitive |
| Output Compare Units | • 16-bit wide<br>• Signals an interrupt when a match with 16-bit I/O Timer occurs<br>• A pair of compare registers can be used to generate an output signal. |
| Programmable Pulse Generator | • 16-bit down counter, cycle and duty setting registers<br>• Interrupt at trigger, counter borrow and/or duty match<br>• PWM operation and one-shot operation<br>• Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input<br>• Can be triggered by software or reload timer |

| Feature | Description |
|---|---|
| Stepper Motor Controller | • Stepper Motor Controller with integrated high current output drivers<br>• Four high current outputs for each channel<br>• Two synchronized 8/10-bit PWMs per channel<br>• Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock<br>• Separate power supply for high current output drivers |
| LCD Controller | • LCD controller with up to 4 COM × SEG<br>• Internal or external voltage generation<br>• Duty cycle: Selectable from options: 1/2, 1/3 and 1/4<br>• Fixed 1/3 bias<br>• Programmable frame period<br>• Clock source selectable from three options (peripheral clock, subclock or RC oscillator clock)<br>• On-chip drivers for internal divider resistors or external divider resistors<br>• On-chip data memory for display<br>• LCD display can be operated in Timer Mode<br>• Blank display: selectable<br>• All SEG, COM and V pins can be switched between general and specialized purposes<br>• External divided resistors can be also used to shut off the current when LCD is deactivated |
| Sound Generator | • 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter<br>• PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock |
| Real Time Clock | • Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator<br>• Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)<br>• Read/write accessible second/minute/hour registers<br>• Can signal interrupts every half second/second/minute/hour/day<br>• Internal clock divider and prescaler provide exact 1s clock |
| External Interrupts | • Edge sensitive or level sensitive<br>• Interrupt mask and pending bit per channel<br>• Each available CAN channel RX has an external interrupt for wake-up<br>• Selected USART channels SIN have an external interrupt for wake-up |
| Non Maskable Interrupt | • Disabled after reset<br>• Once enabled, can not be disabled other than by reset.<br>• Level high or level low sensitive<br>• Pin shared with external interrupt 0. |

| Feature | Description |
|---|---|
| Alarm comparator | • Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds<br>• Threshold voltages defined externally or generated internally<br>• Status is readable, interrupts can be masked separately |
| I/O Ports | • Virtually all external pins can be used as general purpose I/O<br>• All push-pull outputs (except when used as I2C SDA/SCL line)<br>• Bit-wise programmable as input/output or peripheral signal<br>• Bit-wise programmable input enable<br>• Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL<br>• Bit-wise programmable pull-up resistor<br>• Bit-wise programmable output driving strength for EMI optimization |
| Packages | • 100-pin plastic LQFP |
| Flash Memory | • Supports automatic programming, Embedded Algorithm<br>• Write/Erase/Erase-Suspend/Resume commands<br>• A flag indicating completion of the algorithm<br>• Number of erase cycles: 10,000 times<br>• Data retention time: 20 years<br>• Erase can be performed on each sector individually<br>• Sector protection<br>• Flash Security feature to protect the content of the Flash<br>• Low voltage detection during Flash erase |

## ■ PRODUCT LINEUP

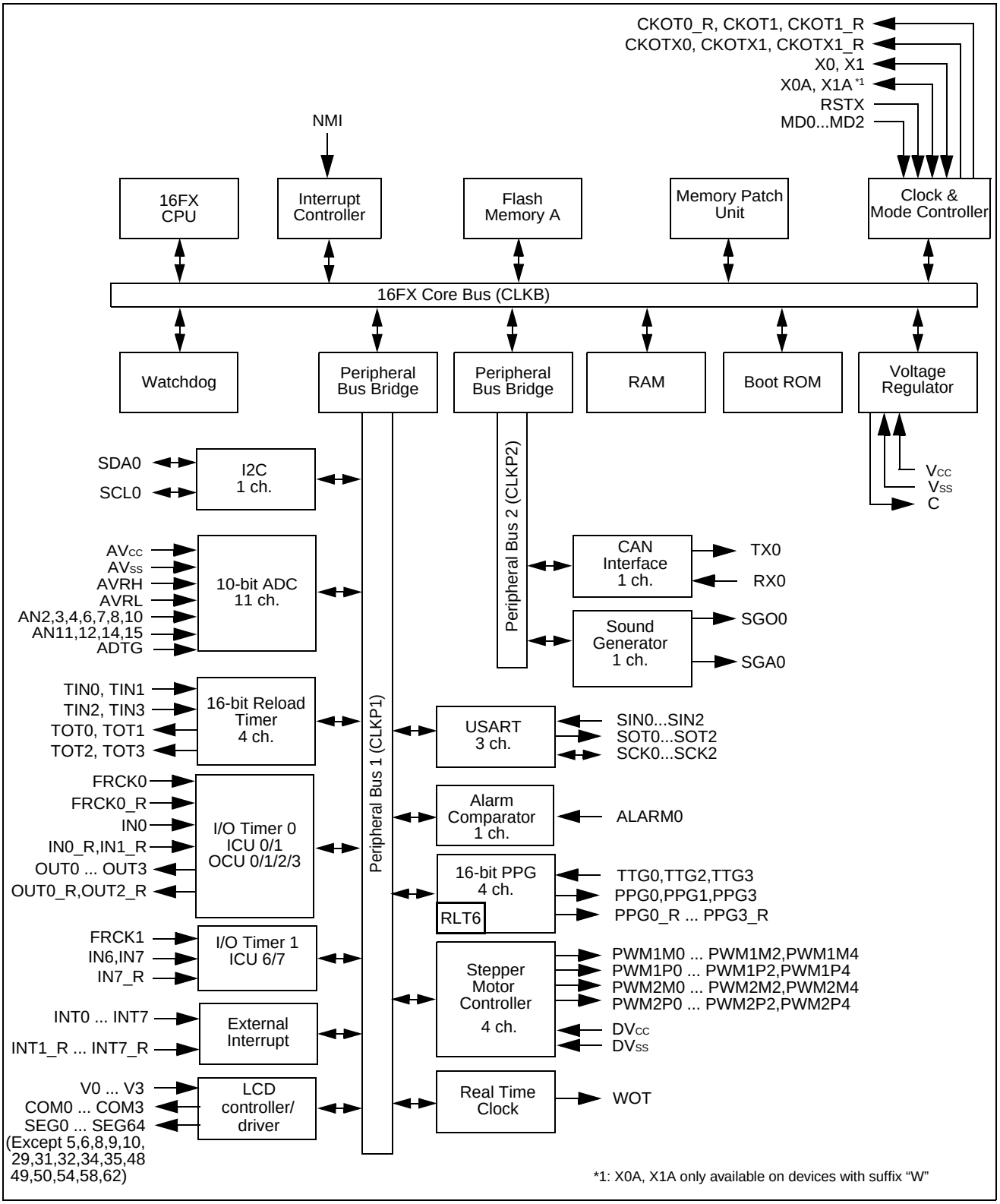
| Features | | MB96V300B | MB96(F)39x |
|---|---|---|---|
| Product type | | Evaluation sample | Flash product: MB96F39x<br>Mask ROM product: MB9639x |
| Product options | | | |
| YS | | NA | Low voltage reset persistently on / Single clock devices |
| RS | | | Low voltage reset can be disabled / Single clock devices |
| YW | | | Low voltage reset persistently on / Dual clock devices |
| RW | | | Low voltage reset can be disabled / Dual clock devices |
| Flash/ROM | RAM | | |
| 160KB | 5KB | ROM/Flash memory emulation by external RAM, 92KB internal RAM | MB96F395Y[*1], MB96F395R[*1], |
| Package | | BGA416 | FPT-100P-M20 |
| DMA | | 16 channels | 0 channels |
| USART | | 10 channels | 3 channels |
| I2C | | 2 channels | 1 channel |
| A/D Converter | | 40 channels | 11 channels |
| A/D Converter Reference Voltage switch | | yes | No |
| 16-bit Reload Timer | | 6 channels + 1 channel (for PPG) | 4 channels + 1 channel (for PPG) |
| 16-bit Free-Running Timer | | 4 channels | 2 channels |
| 16-bit Output Compare | | 12 channels | 4 channels |
| 16-bit Input Capture | | 12 channels | 4 channels |
| 16-bit Programmable Pulse Generator | | 20 channels | 4 channels |
| CAN Interface | | 5 channels | 1 channels |
| Stepping Motor Controller | | 6 channels | 4 channels |
| External Interrupts | | 16 channels | 8 channels |
| Non-Maskable Interrupt | | 1 channel | |
| Sound generator | | 2 channels | 1 channels |
| LCD Controller | | 4 COM x 72 SEG | 4 COM x 49 SEG |
| Real Time Clock | | 1 | |

| Features | MB96V300B | MB96(F)39x |
|---|---|---|
| I/O Ports | 136 | 74 for part number with suffix "W", 76 for part number with suffix "S" |
| Alarm comparator | 2 channels | 1 channels |
| External bus interface | Yes | No |
| Clock output function | 2 channels | |
| Low voltage reset | Yes | |
| On-chip RC-oscillator | Yes | |

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

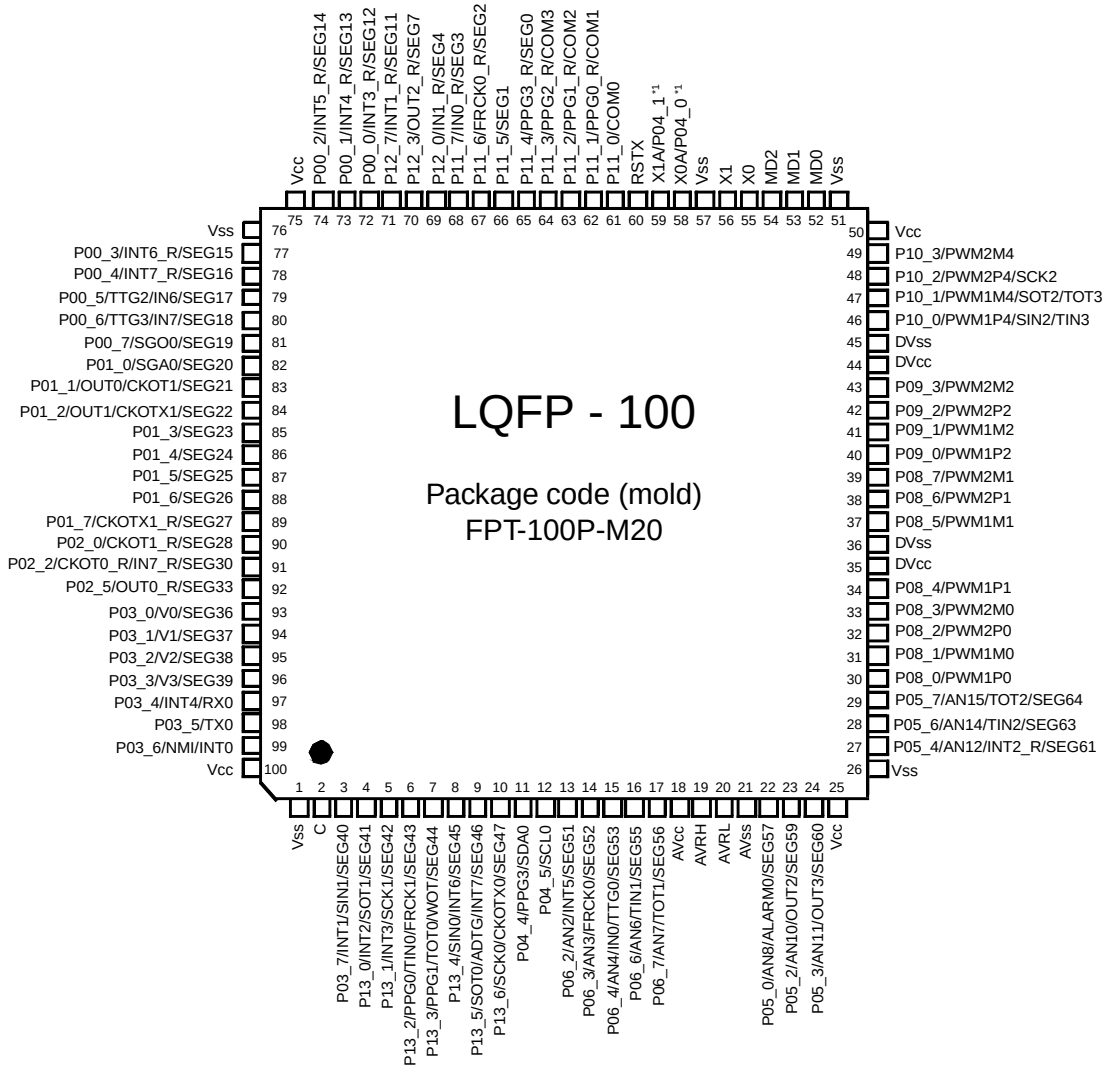
## ■ BLOCK DIAGRAMS

**Block diagram of MB96F39x**



## ■ PIN ASSIGNMENTS

**Pin assignment of MB96F39x**




*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1

(FPT-100P-M20)

## ■ PIN FUNCTION DESCRIPTION

**Pin Function description (1 of 2)**

| Pin name | Feature | Description |
|---|---|---|
| ADTG | ADC | A/D converter trigger input |
| ALARMn | Alarm comparator | Alarm Comparator n input |
| ANn | ADC | A/D converter channel n input |
| $AV_{CC}$ | Supply | Analog circuits power supply |
| AVRH | ADC | A/D converter high reference voltage input |
| AVRL | ADC | A/D converter low reference voltage input |
| $AV_{SS}$ | Supply | Analog circuits power supply |
| C | Voltage regulator | Internally regulated power supply stabilization capacitor pin |
| CKOTn | Clock output function | Clock Output function n output |
| CKOTn_R | Clock output function | Relocated Clock Output function n output |
| CKOTXn | Clock output function | Clock Output function n inverted output |
| CKOTXn_R | Clock output function | Relocated Clock Output function n inverted output |
| COMn | LCD | LCD COM pins |
| $DV_{CC}$ | Supply | SMC pins power supply |
| FRCKn | Free Running Timer | Free Running Timer n input |
| FRCKn_R | Free Running Timer | Relocated Free Running Timer n input |
| INn | ICU | Input Capture Unit n input |
| INn_R | ICU | Relocated Input Capture Unit n input |
| INTn | External Interrupt | External Interrupt n input |
| INTn_R | External Interrupt | Relocated External Interrupt n input |
| MDn | Core | Input pins for specifying the operating mode. |
| NMI | External Interrupt | Non-Maskable Interrupt input |
| OUTn | OCU | Output Compare Unit n waveform output |
| OUTn_R | OCU | Relocated Output Compare Unit n waveform output |
| Pxx_n | GPIO | General purpose IO |
| PPGn | PPG | Programmable Pulse Generator n output |
| PPGn_R | PPG | Relocated Programmable Pulse Generator n output |
| PWMn | SMC | SMC PWM high current |
| RSTX | Core | Reset input |

**Pin Function description (2 of 2)**

| Pin name | Feature | Description |
|---|---|---|
| RXn | CAN | CAN interface n RX input |
| SCKn | USART | USART n serial clock input/output |
| SCLn | I2C | I2C interface n clock I/O input/output |
| SDAn | I2C | I2C interface n serial data I/O input/output |
| SEGn | LCD | LCD segment n |
| SGA | Sound Generator | SG amplitude output |
| SGO | Sound Generator | SG sound/tone output |
| SINn | USART | USART n serial data input |
| SOTn | USART | USART n serial data output |
| TINn | Reload Timer | Reload Timer n event input |
| TOTn | Reload Timer | Reload Timer n output |
| TTGn | PPG | Programmable Pulse Generator n trigger input |
| TXn | CAN | CAN interface n TX output |
| Vn | LCD | LCD voltage references |
| $V_{CC}$ | Supply | Power supply |
| $V_{SS}$ | Supply | Power supply |
| WOT | RTC | Real Timer clock output |
| X0 | Clock | Oscillator input |
| X0A | Clock | Subclock Oscillator input (only for devices with suffix "W") |
| X1 | Clock | Oscillator output |
| X1A | Clock | Subclock Oscillator output (only for devices with suffix "W") |

## ■ PIN CIRCUIT TYPE

**Pin circuit types (1 of 2)**

| FPT-100P-M20 | |
|---|---|
| **Pin no.** | **Circuit type** *1 |
| 1 | Supply |
| 2 | F |
| 3 to 10 | J |
| 11,12 | N |
| 13 to 17 | K |
| 18 | Supply |
| 19 to 20 | G |
| 21 | Supply |
| 22 to 24 | K |
| 25,26 | Supply |
| 27 to 29 | K |
| 30 to 34 | M |
| 35,36 | Supply |
| 37 to 43 | M |
| 44,45 | Supply |
| 46 to 49 | M |
| 50, 51 | Supply |
| 52 to 54 | C |
| 55, 56 | A |
| 57 | Supply |
| 58,59 | B *2) |
| 58,59 | H *3 |
| 60 | E |
| 61 to 74 | J |
| 75 to 76 | Supply |
| 77 to 92 | J |
| 93 to 96 | L |
| 97 to 99 | H |

**Pin circuit types (2 of 2)**

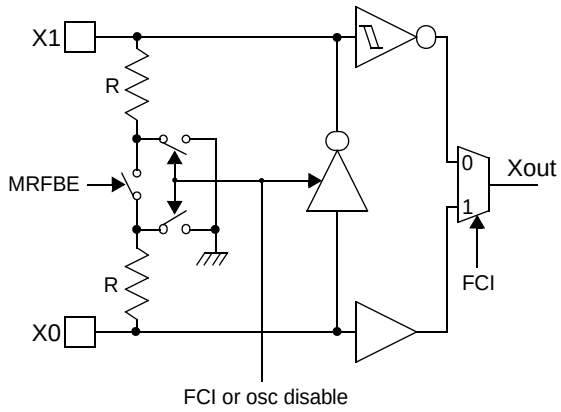
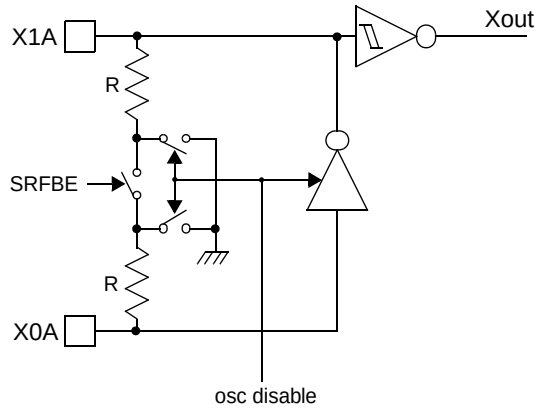
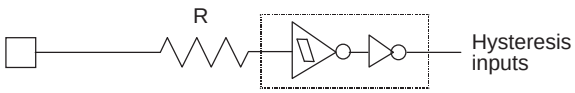
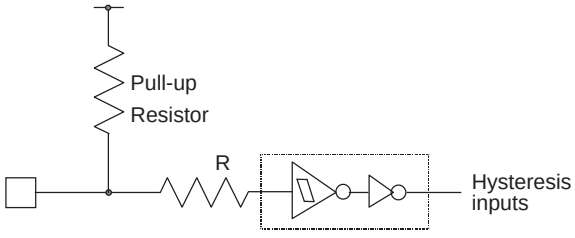
| FPT-100P-M20 | |
|---|---|
| **Pin no.** | **Circuit type** *1 |
| 100 | Supply |

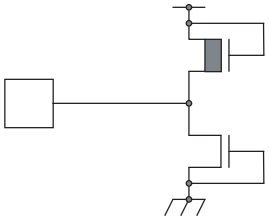
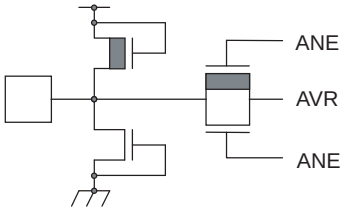
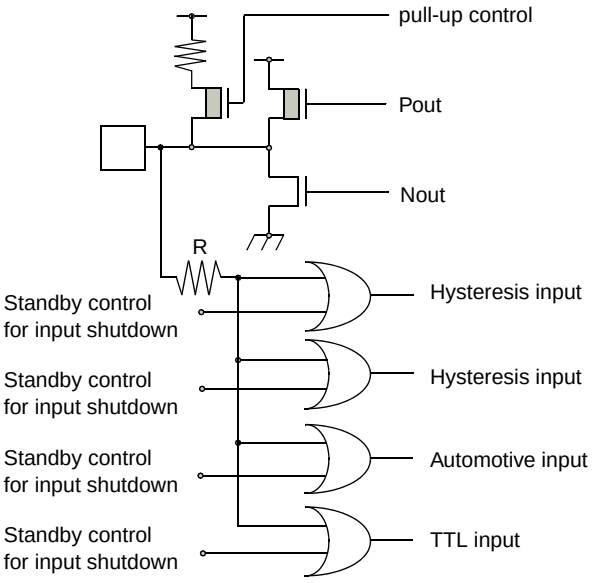
*1: Please refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types

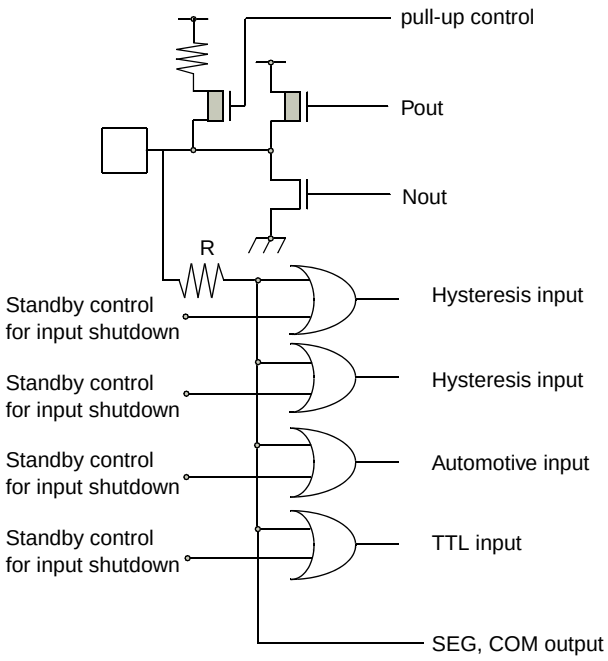
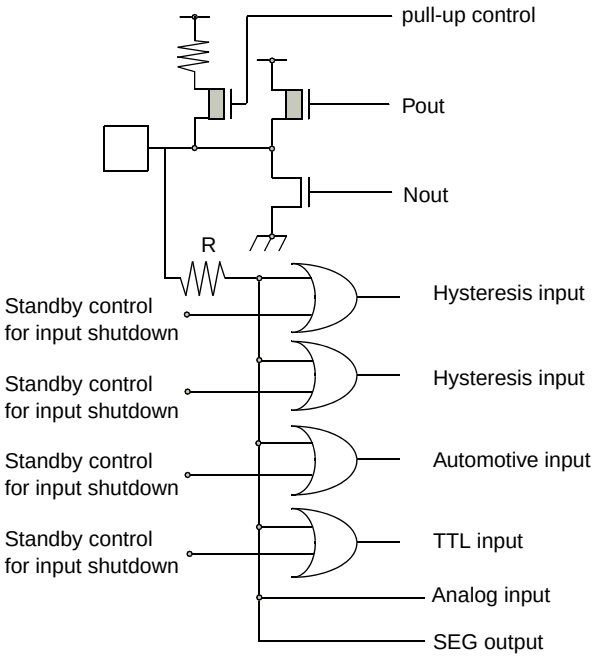
*2: Devices with suffix ”W”

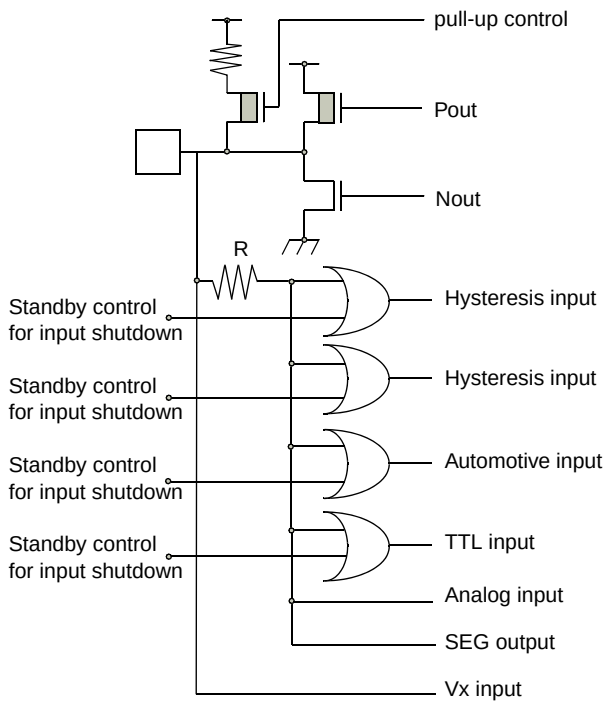
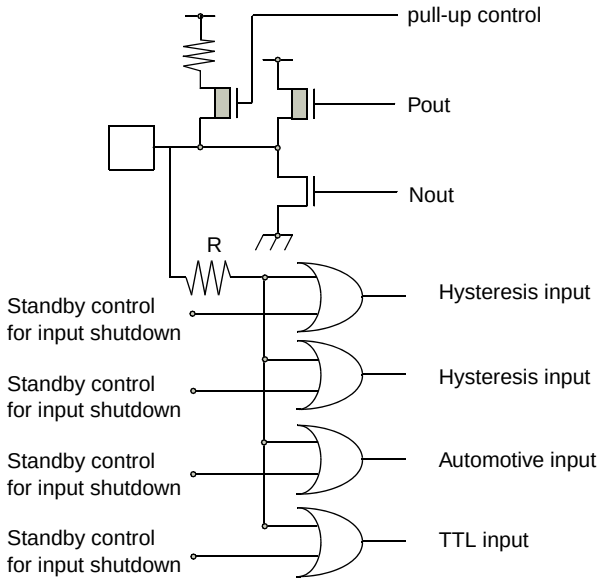
*3: Devices without suffix ”W”

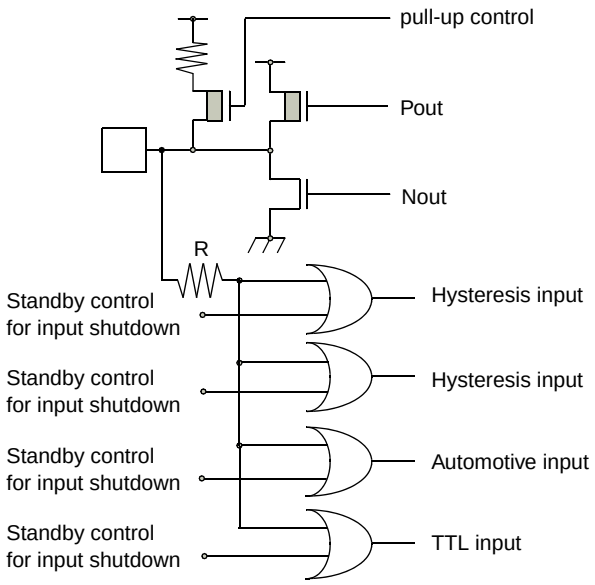
## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | High-speed oscillation circuit:<br>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)<br>• Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode |
| B |  | Low-speed oscillation circuit:<br>• Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled |
| C |  | • Mask ROM and EVA device: CMOS Hysteresis input pin<br>• Flash device: CMOS input pin |
| E |  | • CMOS Hysteresis input pin<br>• Pull-up resistor value: approx. 50 kΩ |

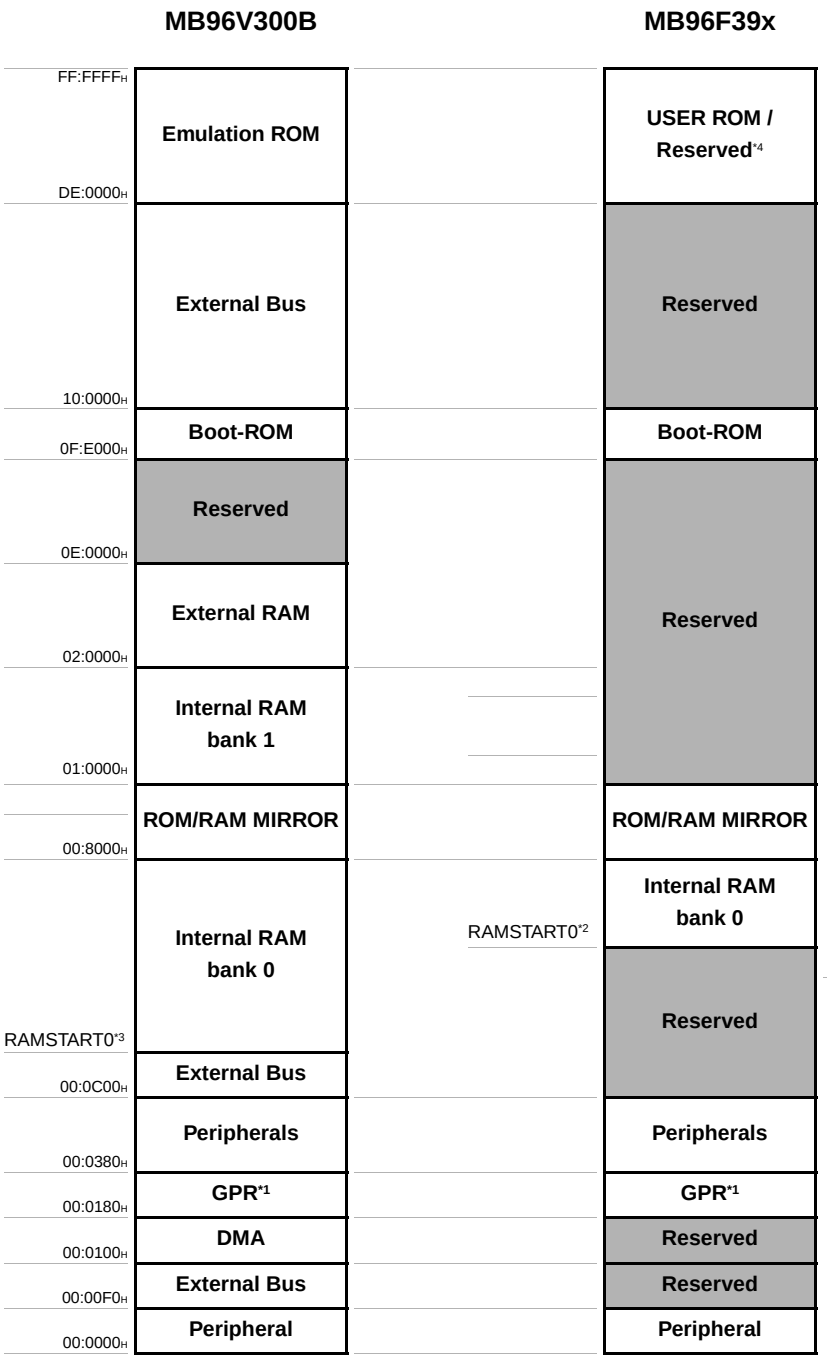
| Type | Circuit | Remarks |
|---|---|---|
| F |  | • Power supply input protection circuit |
| G |  | • A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit<br>• Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2<br>• Devices without AVRH reference switch do not have an analog switch for the AVRL pin |
| H |  | • CMOS level output (programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>• 2 different CMOS hysteresis inputs with input shutdown function<br>• Automotive input with input shutdown function<br>• TTL input with input shutdown function<br>• Programmable pull-up resistor: 50kΩ approx. |

| Type | Circuit | Remarks |
|---|---|---|
| J |  | • CMOS level output (programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>• 2 different CMOS hysteresis inputs with input shutdown function<br>• Automotive input with input shutdown function<br>• TTL input with input shutdown function<br>• Programmable pull-up resistor: 50kΩ approx.<br>• SEG or COM output |
| K |  | • CMOS level output (programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>• 2 different CMOS hysteresis inputs with input shutdown function<br>• Automotive input with input shutdown function<br>• TTL input with input shutdown function.<br>• Programmable pull-up resistor: 50kΩ approx.<br>• Analog input<br>• SEG output |

| Type | Circuit | Remarks |
|---|---|---|
| L |  | • CMOS level output (programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>• 2 different CMOS hysteresis inputs with input shutdown function<br>• Automotive input with input shutdown function<br>• TTL input with input shutdown function<br>• Programmable pull-up resistor: 50kΩ approx.<br>• Analog input<br>• Vx input<br>• SEG output |
| M |  | • CMOS level output (programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA, $I_{OL}$ = 30mA, $I_{OH}$ = -30mA)<br>• 2 different CMOS hysteresis inputs with input shutdown function<br>• Automotive input with input shutdown function<br>• TTL input with input shutdown function<br>• Programmable pull-up resistor: 50kΩ approx. |

| Type | Circuit | Remarks |
|---|---|---|
| N |  | • CMOS level output ($I_{OL}$ = 3mA, $I_{OH}$ = -3mA)<br>• 2 different CMOS hysteresis inputs with input shutdown function<br>• Automotive input with input shutdown function<br>• TTL input with input shutdown function<br>• Programmable pull-up resistor: 50kΩ approx. |

## ■ MEMORY MAP




*1: Unused GPR banks can be used as RAM area

*2: For RAMSTART0 addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the ■ USER ROM MEMORY MAP FOR FLASH DEVICES on the following pages.

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

## ■ RAMSTART/END AND EXTERNAL BUS END ADDRESSES

| Devices | Bank 0 RAM size | RAMSTART0 |
|---|---|---|
| MB96F395 | 5KByte | 00:6E40$_H$ |

## ■ USER ROM MEMORY MAP FOR FLASH DEVICES

**MB96F395R**
**MB96F395Y**

| Alternative mode CPU address | Flash memory mode address | Flash size 160kByte |
|---|---|---|
| FF:FFFF$_H$ | 3F:FFFF$_H$ | S39 - 64K |
| FF:0000$_H$ | 3F:0000$_H$ | |
| FE:FFFF$_H$ | 3E:FFFF$_H$ | S38 - 64K |
| FE:0000$_H$ | 3E:0000$_H$ | |
| FD:FFFF$_H$ | 3D:FFFF$_H$ | Reserved |
| FD:0000$_H$ | 3D:0000$_H$ | |
| FC:FFFF$_H$ | 3C:FFFF$_H$ | |
| FC:0000$_H$ | 3C:0000$_H$ | |
| FB:FFFF$_H$ | 3B:FFFF$_H$ | |
| FB:0000$_H$ | 3B:0000$_H$ | |
| FA:FFFF$_H$ | 3A:FFFF$_H$ | |
| FA:0000$_H$ | 3A:0000$_H$ | |
| F9:FFFF$_H$ | 39:FFFF$_H$ | |
| F9:0000$_H$ | 39:0000$_H$ | |
| F8:FFFF$_H$ | 38:FFFF$_H$ | |
| F8:0000$_H$ | 38:0000$_H$ | |
| F7:FFFF$_H$ | 37:FFFF$_H$ | |
| F7:0000$_H$ | 37:0000$_H$ | |
| F6:FFFF$_H$ | 36:FFFF$_H$ | |
| F6:0000$_H$ | 36:0000$_H$ | |
| F5:FFFF$_H$ | 35:FFFF$_H$ | |
| F5:0000$_H$ | 35:0000$_H$ | |
| F4:FFFF$_H$ | 34:FFFF$_H$ | |
| F4:0000$_H$ | 34:0000$_H$ | |
| F3:FFFF$_H$ | 33:FFFF$_H$ | |
| F3:0000$_H$ | 33:0000$_H$ | |
| F2:FFFF$_H$ | 32:FFFF$_H$ | |
| F2:0000$_H$ | 32:0000$_H$ | |
| F1:FFFF$_H$ | 31:FFFF$_H$ | |
| F1:0000$_H$ | 31:0000$_H$ | |
| F0:FFFF$_H$ | 30:FFFF$_H$ | |
| F0:0000$_H$ | 30:0000$_H$ | |
| E0:FFFF$_H$ | | |
| E0:0000$_H$ | | |
| DF:FFFF$_H$ | | |
| DF:8000$_H$ | | |
| DF:7FFF$_H$ | 1F:7FFF$_H$ | SA3 - 8K |
| DF:6000$_H$ | 1F:6000$_H$ | |
| DF:5FFF$_H$ | 1F:5FFF$_H$ | SA2 - 8K |
| DF:4000$_H$ | 1F:4000$_H$ | |
| DF:3FFF$_H$ | 1F:3FFF$_H$ | SA1 - 8K |
| DF:2000$_H$ | 1F:2000$_H$ | |
| DF:1FFF$_H$ | 1F:1FFF$_H$ | SA0 - 8K *1 |
| DF:0000$_H$ | 1F:0000$_H$ | |
| DE:FFFF$_H$ | | Reserved |
| DE:0000$_H$ | | |

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

## ■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

**USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)**

| MB96F39x | | |
|---|---|---|
| Pin number | USART Number | Normal function |
| LQFP-100 | | |
| 8 | USART0 | SIN0 |
| 9 | | SOT0 |
| 10 | | SCK0 |
| 3 | USART1 | SIN1 |
| 4 | | SOT1 |
| 5 | | SCK1 |
| 46 | USART2 | SIN2 |
| 47 | | SOT2 |
| 48 | | SCK2 |

Note: If a Flash programmer and its software needs to use a handshaking pin, Fujitsu suggests to the tool vendor to support at least port P00_1 on pin 88.
If handshaking is used by the tool but P00_1 is not available in customer's application, Fujitsu suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

## ■ I/O MAP

**I/O map MB96F39x (1 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000000H | I/O Port P00 - Port Data Register | PDR00 | | R/W |
| 000001H | I/O Port P01 - Port Data Register | PDR01 | | R/W |
| 000002H | I/O Port P02 - Port Data Register | PDR02 | | R/W |
| 000003H | I/O Port P03 - Port Data Register | PDR03 | | R/W |
| 000004H | I/O Port P04 - Port Data Register | PDR04 | | R/W |
| 000005H | I/O Port P05 - Port Data Register | PDR05 | | R/W |
| 000006H | I/O Port P06 - Port Data Register | PDR06 | | R/W |
| 000007H | Reserved | | | - |
| 000008H | I/O Port P08 - Port Data Register | PDR08 | | R/W |
| 000009H | I/O Port P09 - Port Data Register | PDR09 | | R/W |
| 00000AH | I/O Port P10 - Port Data Register | PDR10 | | R/W |
| 00000BH | I/O Port P11 - Port Data Register | PDR11 | | R/W |
| 00000CH | I/O Port P12 - Port Data Register | PDR12 | | R/W |
| 00000DH | I/O Port P13 - Port Data Register | PDR13 | | R/W |
| 00000EH-000017H | Reserved | | | - |
| 000018H | ADC0 - Control Status register Low | ADCSL | ADCS | R/W |
| 000019H | ADC0 - Control Status register High | ADCSH | | R/W |
| 00001AH | ADC0 - Data Register Low | ADCRL | ADCR | R |
| 00001BH | ADC0 - Data Register High | ADCRH | | R |
| 00001CH | ADC0 - Setting Register | | ADSR | R/W |
| 00001DH | ADC0 - Setting Register | | | R/W |
| 00001EH | ADC0 - Extended Configuration Register | ADECR | | R/W |
| 00001FH | Reserved | | | - |
| 000020H | FRT0 - Data register of free-running timer | | TCDT0 | R/W |
| 000021H | FRT0 - Data register of free-running timer | | | R/W |
| 000022H | FRT0 - Control status register of free-running timer Low | TCCSL0 | TCCS0 | R/W |
| 000023H | FRT0 - Control status register of free-running timer High | TCCSH0 | | R/W |

**I/O map MB96F39x (2 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000024H | FRT1 - Data register of free-running timer | | TCDT1 | R/W |
| 000025H | FRT1 - Data register of free-running timer | | | R/W |
| 000026H | FRT1 - Control status register of free-running timer Low | TCCSL1 | TCCS1 | R/W |
| 000027H | FRT1 - Control status register of free-running timer High | TCCSH1 | | R/W |
| 000028H | OCU0 - Output Compare Control Status | OCS0 | | R/W |
| 000029H | OCU1 - Output Compare Control Status | OCS1 | | R/W |
| 00002AH | OCU0 - Compare Register | | OCCP0 | R/W |
| 00002BH | OCU0 - Compare Register | | | R/W |
| 00002CH | OCU1 - Compare Register | | OCCP1 | R/W |
| 00002DH | OCU1 - Compare Register | | | R/W |
| 00002EH | OCU2 - Output Compare Control Status | OCS2 | | R/W |
| 00002FH | OCU3 - Output Compare Control Status | OCS3 | | R/W |
| 000030H | OCU2 - Compare Register | | OCCP2 | R/W |
| 000031H | OCU2 - Compare Register | | | R/W |
| 000032H | OCU3 - Compare Register | | OCCP3 | R/W |
| 000033H | OCU3 - Compare Register | | | R/W |
| 000034H-00003FH | Reserved | | | - |
| 000040H | ICU0/ICU1 - Control Status Register | ICS01 | | R/W |
| 000041H | ICU0/ICU1 - Edge register | ICE01 | | R/W |
| 000042H | ICU0 - Capture Register Low | IPCPL0 | IPCP0 | R |
| 000043H | ICU0 - Capture Register High | IPCPH0 | | R |
| 000044H | ICU1 - Capture Register Low | IPCPL1 | IPCP1 | R |
| 000045H | ICU1 - Capture Register High | IPCPH1 | | R |
| 000046H-000051H | Reserved | | | - |
| 000052H | ICU6/ICU7 - Control Status Register | ICS67 | | R/W |
| 000053H | ICU6/ICU7 - Edge register | ICE67 | | R/W |
| 000054H | ICU6 - Capture Register Low | IPCPL6 | IPCP6 | R |

**I/O map MB96F39x (3 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000055H | ICU6 - Capture Register High | IPCPH6 | | R |
| 000056H | ICU7 - Capture Register Low | IPCPL7 | IPCP7 | R |
| 000057H | ICU7 - Capture Register High | IPCPH7 | | R |
| 000058H | EXTINT0 - External Interrupt Enable Register | ENIR0 | | R/W |
| 000059H | EXTINT0 - External Interrupt Interrupt request Register | EIRR0 | | R/W |
| 00005AH | EXTINT0 - External Interrupt Level Select Low | ELVRL0 | ELVR0 | R/W |
| 00005BH | EXTINT0 - External Interrupt Level Select High | ELVRH0 | | R/W |
| 00005CH-00005FH | Reserved | | | - |
| 000060H | RLT0 - Timer Control Status Register Low | TMCSRL0 | TMCSR0 | R/W |
| 000061H | RLT0 - Timer Control Status Register High | TMCSRH0 | | R/W |
| 000062H | RLT0 - Reload Register - for writing | | TMRLR0 | W |
| 000062H | RLT0 - Reload Register - for reading | | TMR0 | R |
| 000063H | RLT0 - Reload Register - for writing | | | W |
| 000063H | RLT0 - Reload Register - for reading | | | R |
| 000064H | RLT1 - Timer Control Status Register Low | TMCSRL1 | TMCSR1 | R/W |
| 000065H | RLT1 - Timer Control Status Register High | TMCSRH1 | | R/W |
| 000066H | RLT1 - Reload Register - for writing | | TMRLR1 | W |
| 000066H | RLT1 - Reload Register - for reading | | TMR1 | R |
| 000067H | RLT1 - Reload Register - for writing | | | W |
| 000067H | RLT1 - Reload Register - for reading | | | R |
| 000068H | RLT2 - Timer Control Status Register Low | TMCSRL2 | TMCSR2 | R/W |
| 000069H | RLT2 - Timer Control Status Register High | TMCSRH2 | | R/W |
| 00006AH | RLT2 - Reload Register - for writing | | TMRLR2 | W |
| 00006AH | RLT2 - Reload Register - for reading | | TMR2 | R |
| 00006BH | RLT2 - Reload Register - for writing | | | W |
| 00006BH | RLT2 - Reload Register - for reading | | | R |
| 00006CH | RLT3 - Timer Control Status Register Low | TMCSRL3 | TMCSR3 | R/W |
| 00006DH | RLT3 - Timer Control Status Register High | TMCSRH3 | | R/W |
| 00006EH | RLT3 - Reload Register - for writing | | TMRLR3 | W |

**I/O map MB96F39x (4 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 00006E$_H$ | RLT3 - Reload Register - for reading | | TMR3 | R |
| 00006F$_H$ | RLT3 - Reload Register - for writing | | | W |
| 00006F$_H$ | RLT3 - Reload Register - for reading | | | R |
| 000070$_H$ | RLT6 - Timer Control Status Register Low (dedic. RLT for PPG) | TMCSRL6 | TMCSR6 | R/W |
| 000071$_H$ | RLT6 - Timer Control Status Register High (dedic. RLT for PPG) | TMCSRH6 | | R/W |
| 000072$_H$ | RLT6 - Reload Register (dedic. RLT for PPG) - for writing | | TMRLR6 | W |
| 000072$_H$ | RLT6 - Reload Register (dedic. RLT for PPG) - for reading | | TMR6 | R |
| 000073$_H$ | RLT6 - Reload Register (dedic. RLT for PPG) - for writing | | | W |
| 000073$_H$ | RLT6 - Reload Register (dedic. RLT for PPG) - for reading | | | R |
| 000074$_H$ | PPG3-PPG0 - General Control register 1 Low | GCN1L0 | GCN10 | R/W |
| 000075$_H$ | PPG3-PPG0 - General Control register 1 High | GCN1H0 | | R/W |
| 000076$_H$ | PPG3-PPG0 - General Control register 2 Low | GCN2L0 | GCN20 | R/W |
| 000077$_H$ | PPG3-PPG0 - General Control register 2 High | GCN2H0 | | R/W |
| 000078$_H$ | PPG0 - Timer register | | PTMR0 | R |
| 000079$_H$ | PPG0 - Timer register | | | R |
| 00007A$_H$ | PPG0 - Period setting register | | PCSR0 | W |
| 00007B$_H$ | PPG0 - Period setting register | | | W |
| 00007C$_H$ | PPG0 - Duty cycle register | | PDUT0 | W |
| 00007D$_H$ | PPG0 - Duty cycle register | | | W |
| 00007E$_H$ | PPG0 - Control status register Low | PCNL0 | PCN0 | R/W |
| 00007F$_H$ | PPG0 - Control status register High | PCNH0 | | R/W |
| 000080$_H$ | PPG1 - Timer register | | PTMR1 | R |
| 000081$_H$ | PPG1 - Timer register | | | R |
| 000082$_H$ | PPG1 - Period setting register | | PCSR1 | W |
| 000083$_H$ | PPG1 - Period setting register | | | W |
| 000084$_H$ | PPG1 - Duty cycle register | | PDUT1 | W |

**I/O map MB96F39x (5 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000085H | PPG1 - Duty cycle register | | | W |
| 000086H | PPG1 - Control status register Low | PCNL1 | PCN1 | R/W |
| 000087H | PPG1 - Control status register High | PCNH1 | | R/W |
| 000088H | PPG2 - Timer register | | PTMR2 | R |
| 000089H | PPG2 - Timer register | | | R |
| 00008AH | PPG2 - Period setting register | | PCSR2 | W |
| 00008BH | PPG2 - Period setting register | | | W |
| 00008CH | PPG2 - Duty cycle register | | PDUT2 | W |
| 00008DH | PPG2 - Duty cycle register | | | W |
| 00008EH | PPG2 - Control status register Low | PCNL2 | PCN2 | R/W |
| 00008FH | PPG2 - Control status register High | PCNH2 | | R/W |
| 000090H | PPG3 - Timer register | | PTMR3 | R |
| 000091H | PPG3 - Timer register | | | R |
| 000092H | PPG3 - Period setting register | | PCSR3 | W |
| 000093H | PPG3 - Period setting register | | | W |
| 000094H | PPG3 - Duty cycle register | | PDUT3 | W |
| 000095H | PPG3 - Duty cycle register | | | W |
| 000096H | PPG3 - Control status register Low | PCNL3 | PCN3 | R/W |
| 000097H | PPG3 - Control status register High | PCNH3 | | R/W |
| 000098H-0000ABH | Reserved | | | - |
| 0000ACH | I2C0 - Bus Status Register | IBSR0 | | R |
| 0000ADH | I2C0 - Bus Control Register | IBCR0 | | R/W |
| 0000AEH | I2C0 - Ten bit Slave address Register Low | ITBAL0 | ITBA0 | R/W |
| 0000AFH | I2C0 - Ten bit Slave address Register High | ITBAH0 | | R/W |
| 0000B0H | I2C0 - Ten bit Address mask Register Low | ITMKL0 | ITMK0 | R/W |
| 0000B1H | I2C0 - Ten bit Address mask Register High | ITMKH0 | | R/W |
| 0000B2H | I2C0 - Seven bit Slave address Register | ISBA0 | | R/W |
| 0000B3H | I2C0 - Seven bit Address mask Register | ISMK0 | | R/W |
| 0000B4H | I2C0 - Data Register | IDAR0 | | R/W |

**I/O map MB96F39x (6 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0000B5H | I2C0 - Clock Control Register | ICCR0 | | R/W |
| 0000B6H-0000BFH | Reserved | | | - |
| 0000C0H | USART0 - Serial Mode Register | SMR0 | | R/W |
| 0000C1H | USART0 - Serial Control Register | SCR0 | | R/W |
| 0000C2H | USART0 - TX Register | TDR0 | | W |
| 0000C2H | USART0 - RX Register | RDR0 | | R |
| 0000C3H | USART0 - Serial Status | SSR0 | | R/W |
| 0000C4H | USART0 - Control/Com. Register | ECCR0 | | R/W |
| 0000C5H | USART0 - Ext. Status Register | ESCR0 | | R/W |
| 0000C6H | USART0 - Baud Rate Generator Register Low | BGRL0 | BGR0 | R/W |
| 0000C7H | USART0 - Baud Rate Generator Register High | BGRH0 | | R/W |
| 0000C8H | USART0 - Extended Serial Interrupt Register | ESIR0 | | R/W |
| 0000C9H | Reserved | | | - |
| 0000CAH | USART1 - Serial Mode Register | SMR1 | | R/W |
| 0000CBH | USART1 - Serial Control Register | SCR1 | | R/W |
| 0000CCH | USART1 - TX Register | TDR1 | | W |
| 0000CCH | USART1 - RX Register | RDR1 | | R |
| 0000CDH | USART1 - Serial Status | SSR1 | | R/W |
| 0000CEH | USART1 - Control/Com. Register | ECCR1 | | R/W |
| 0000CFH | USART1 - Ext. Status Register | ESCR1 | | R/W |
| 0000D0H | USART1 - Baud Rate Generator Register Low | BGRL1 | BGR1 | R/W |
| 0000D1H | USART1 - Baud Rate Generator Register High | BGRH1 | | R/W |
| 0000D2H | USART1 - Extended Serial Interrupt Register | ESIR1 | | R/W |
| 0000D3H | Reserved | | | - |
| 0000D4H | USART2 - Serial Mode Register | SMR2 | | R/W |
| 0000D5H | USART2 - Serial Control Register | SCR2 | | R/W |
| 0000D6H | USART2 - TX Register | TDR2 | | W |
| 0000D6H | USART2 - RX Register | RDR2 | | R |
| 0000D7H | USART2 - Serial Status | SSR2 | | R/W |

**I/O map MB96F39x (7 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0000D8H | USART2 - Control/Com. Register | ECCR2 | | R/W |
| 0000D9H | USART2 - Ext. Status Register | ESCR2 | | R/W |
| 0000DAH | USART2 - Baud Rate Generator Register Low | BGRL2 | BGR2 | R/W |
| 0000DBH | USART2 - Baud Rate Generator Register High | BGRH2 | | R/W |
| 0000DCH | USART2 - Extended Serial Interrupt Register | ESIR2 | | R/W |
| 0000DDH-00017FH | Reserved | | | - |
| 000180H-00037FH | CPU - General Purpose registers (RAM access) | GPR_RAM | | R/W |
| 000380H-00039FH | Reserved | | | - |
| 0003A0H | Interrupt level register | ILR | ICR | R/W |
| 0003A1H | Interrupt index register | IDX | | R/W |
| 0003A2H | Interrupt vector table base register Low | TBRL | TBR | R/W |
| 0003A3H | Interrupt vector table base register High | TBRH | | R/W |
| 0003A4H | Delayed Interrupt register | DIRR | | R/W |
| 0003A5H | Non Maskable Interrupt register | NMI | | R/W |
| 0003A6H-0003ABH | Reserved | | | - |
| 0003ACH | EDSU communication interrupt selection Low | EDSU2L | EDSU2 | R/W |
| 0003ADH | EDSU communication interrupt selection High | EDSU2H | | R/W |
| 0003AEH | ROM mirror control register | ROMM | | R/W |
| 0003AFH | EDSU configuration register | EDSU | | R/W |
| 0003B0H | Memory patch control/status register ch 0/1 | | PFCS0 | R/W |
| 0003B1H | Memory patch control/status register ch 0/1 | | | R/W |
| 0003B2H | Memory patch control/status register ch 2/3 | | PFCS1 | R/W |
| 0003B3H | Memory patch control/status register ch 2/3 | | | R/W |
| 0003B4H | Memory patch control/status register ch 4/5 | | PFCS2 | R/W |
| 0003B5H | Memory patch control/status register ch 4/5 | | | R/W |
| 0003B6H | Memory patch control/status register ch 6/7 | | PFCS3 | R/W |
| 0003B7H | Memory patch control/status register ch 6/7 | | | R/W |

**I/O map MB96F39x (8 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0003B8H | Memory Patch function - Patch address 0 low | PFAL0 | | R/W |
| 0003B9H | Memory Patch function - Patch address 0 middle | PFAM0 | | R/W |
| 0003BAH | Memory Patch function - Patch address 0 high | PFAH0 | | R/W |
| 0003BBH | Memory Patch function - Patch address 1 low | PFAL1 | | R/W |
| 0003BCH | Memory Patch function - Patch address 1 middle | PFAM1 | | R/W |
| 0003BDH | Memory Patch function - Patch address 1 high | PFAH1 | | R/W |
| 0003BEH | Memory Patch function - Patch address 2 low | PFAL2 | | R/W |
| 0003BFH | Memory Patch function - Patch address 2 middle | PFAM2 | | R/W |
| 0003C0H | Memory Patch function - Patch address 2 high | PFAH2 | | R/W |
| 0003C1H | Memory Patch function - Patch address 3 low | PFAL3 | | R/W |
| 0003C2H | Memory Patch function - Patch address 3 middle | PFAM3 | | R/W |
| 0003C3H | Memory Patch function - Patch address 3 high | PFAH3 | | R/W |
| 0003C4H | Memory Patch function - Patch address 4 low | PFAL4 | | R/W |
| 0003C5H | Memory Patch function - Patch address 4 middle | PFAM4 | | R/W |
| 0003C6H | Memory Patch function - Patch address 4 high | PFAH4 | | R/W |
| 0003C7H | Memory Patch function - Patch address 5 low | PFAL5 | | R/W |
| 0003C8H | Memory Patch function - Patch address 5 middle | PFAM5 | | R/W |
| 0003C9H | Memory Patch function - Patch address 5 high | PFAH5 | | R/W |
| 0003CAH | Memory Patch function - Patch address 6 low | PFAL6 | | R/W |
| 0003CBH | Memory Patch function - Patch address 6 middle | PFAM6 | | R/W |
| 0003CCH | Memory Patch function - Patch address 6 high | PFAH6 | | R/W |
| 0003CDH | Memory Patch function - Patch address 7 low | PFAL7 | | R/W |
| 0003CEH | Memory Patch function - Patch address 7 middle | PFAM7 | | R/W |
| 0003CFH | Memory Patch function - Patch address 7 high | PFAH7 | | R/W |
| 0003D0H | Memory Patch function - Patch data 0 Low | PFDL0 | PFD0 | R/W |
| 0003D1H | Memory Patch function - Patch data 0 High | PFDH0 | | R/W |
| 0003D2H | Memory Patch function - Patch data 1 Low | PFDL1 | PFD1 | R/W |
| 0003D3H | Memory Patch function - Patch data 1 High | PFDH1 | | R/W |
| 0003D4H | Memory Patch function - Patch data 2 Low | PFDL2 | PFD2 | R/W |
| 0003D5H | Memory Patch function - Patch data 2 High | PFDH2 | | R/W |

**I/O map MB96F39x (9 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0003D6H | Memory Patch function - Patch data 3 Low | PFDL3 | PFD3 | R/W |
| 0003D7H | Memory Patch function - Patch data 3 High | PFDH3 | | R/W |
| 0003D8H | Memory Patch function - Patch data 4 Low | PFDL4 | PFD4 | R/W |
| 0003D9H | Memory Patch function - Patch data 4 High | PFDH4 | | R/W |
| 0003DAH | Memory Patch function - Patch data 5 Low | PFDL5 | PFD5 | R/W |
| 0003DBH | Memory Patch function - Patch data 5 High | PFDH5 | | R/W |
| 0003DCH | Memory Patch function - Patch data 6 Low | PFDL6 | PFD6 | R/W |
| 0003DDH | Memory Patch function - Patch data 6 High | PFDH6 | | R/W |
| 0003DEH | Memory Patch function - Patch data 7 Low | PFDL7 | PFD7 | R/W |
| 0003DFH | Memory Patch function - Patch data 7 High | PFDH7 | | R/W |
| 0003E0H-0003F0H | Reserved | | | - |
| 0003F1H | Memory Control Status Register A | MCSRA | | R/W |
| 0003F2H | Memory Timing Configuration Register A Low | MTCRAL | MTCRA | R/W |
| 0003F3H | Memory Timing Configuration Register A High | MTCRAH | | R/W |
| 0003F4H-0003F7H | Reserved | | | - |
| 0003F8H | Flash Memory Write Control register 0 | FMWC0 | | R/W |
| 0003F9H | Flash Memory Write Control register 1 | FMWC1 | | R/W |
| 0003FAH | Flash Memory Write Control register 2 | FMWC2 | | R/W |
| 0003FBH | Flash Memory Write Control register 3 | FMWC3 | | R/W |
| 0003FCH | Flash Memory Write Control register 4 | FMWC4 | | R/W |
| 0003FDH | Flash Memory Write Control register 5 | FMWC5 | | R/W |
| 0003FEH-0003FFH | Reserved | | | - |
| 000400H | Standby Mode control register | SMCR | | R/W |
| 000401H | Clock select register | CKSR | | R/W |
| 000402H | Clock Stabilisation select register | CKSSR | | R/W |
| 000403H | Clock monitor register | CKMR | | R |
| 000404H | Clock Frequency control register Low | CKFCRL | CKFCR | R/W |
| 000405H | Clock Frequency control register High | CKFCRH | | R/W |

**I/O map MB96F39x (10 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000406H | PLL Control register Low | PLLCRL | PLLCR | R/W |
| 000407H | PLL Control register High | PLLCRH | | R/W |
| 000408H | RC clock timer control register | RCTCR | | R/W |
| 000409H | Main clock timer control register | MCTCR | | R/W |
| 00040AH | Sub clock timer control register | SCTCR | | R/W |
| 00040BH | Reset cause and clock status register with clear function | RCCSRC | | R |
| 00040CH | Reset configuration register | RCR | | R/W |
| 00040DH | Reset cause and clock status register | RCCSR | | R |
| 00040EH | Watch dog timer configuration register | WDTC | | R/W |
| 00040FH | Watch dog timer clear pattern register | WDTCP | | W |
| 000410H-000414H | Reserved | | | - |
| 000415H | Clock output activation register | COAR | | R/W |
| 000416H | Clock output configuration register 0 | COCR0 | | R/W |
| 000417H | Clock output configuration register 1 | COCR1 | | R/W |
| 000418H | Clock Modulator control register | CMCR | | R/W |
| 000419H | Reserved | | | - |
| 00041AH | Clock Modulator Parameter register Low | CMPRL | CMPR | R/W |
| 00041BH | Clock Modulator Parameter register High | CMPRH | | R/W |
| 00041CH-00042BH | Reserved | | | - |
| 00042CH | Voltage Regulator Control register | VRCR | | R/W |
| 00042DH | Clock Input and LVD Control Register | CILCR | | R/W |
| 00042EH-00042FH | Reserved | | | - |
| 000430H | I/O Port P00 - Data Direction Register | DDR00 | | R/W |
| 000431H | I/O Port P01 - Data Direction Register | DDR01 | | R/W |
| 000432H | I/O Port P02 - Data Direction Register | DDR02 | | R/W |
| 000433H | I/O Port P03 - Data Direction Register | DDR03 | | R/W |
| 000434H | I/O Port P04 - Data Direction Register | DDR04 | | R/W |

**I/O map MB96F39x (11 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000435H | I/O Port P05 - Data Direction Register | DDR05 | | R/W |
| 000436H | I/O Port P06 - Data Direction Register | DDR06 | | R/W |
| 000437H | Reserved | | | - |
| 000438H | I/O Port P08 - Data Direction Register | DDR08 | | R/W |
| 000439H | I/O Port P09 - Data Direction Register | DDR09 | | R/W |
| 00043AH | I/O Port P10 - Data Direction Register | DDR10 | | R/W |
| 00043BH | I/O Port P11 - Data Direction Register | DDR11 | | R/W |
| 00043CH | I/O Port P12 - Data Direction Register | DDR12 | | R/W |
| 00043DH | I/O Port P13 - Data Direction Register | DDR13 | | R/W |
| 00043EH-000443H | Reserved | | | - |
| 000444H | I/O Port P00 - Port Input Enable Register | PIER00 | | R/W |
| 000445H | I/O Port P01 - Port Input Enable Register | PIER01 | | R/W |
| 000446H | I/O Port P02 - Port Input Enable Register | PIER02 | | R/W |
| 000447H | I/O Port P03 - Port Input Enable Register | PIER03 | | R/W |
| 000448H | I/O Port P04 - Port Input Enable Register | PIER04 | | R/W |
| 000449H | I/O Port P05 - Port Input Enable Register | PIER05 | | R/W |
| 00044AH | I/O Port P06 - Port Input Enable Register | PIER06 | | R/W |
| 00044BH | Reserved | | | - |
| 00044CH | I/O Port P08 - Port Input Enable Register | PIER08 | | R/W |
| 00044DH | I/O Port P09 - Port Input Enable Register | PIER09 | | R/W |
| 00044EH | I/O Port P10 - Port Input Enable Register | PIER10 | | R/W |
| 00044FH | I/O Port P11 - Port Input Enable Register | PIER11 | | R/W |
| 000450H | I/O Port P12 - Port Input Enable Register | PIER12 | | R/W |
| 000451H | I/O Port P13 - Port Input Enable Register | PIER13 | | R/W |
| 000452H-000457H | Reserved | | | - |
| 000458H | I/O Port P00 - Port Input Level Register | PILR00 | | R/W |
| 000459H | I/O Port P01 - Port Input Level Register | PILR01 | | R/W |
| 00045AH | I/O Port P02 - Port Input Level Register | PILR02 | | R/W |
| 00045BH | I/O Port P03 - Port Input Level Register | PILR03 | | R/W |

**I/O map MB96F39x (12 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 00045C$_H$ | I/O Port P04 - Port Input Level Register | PILR04 | | R/W |
| 00045D$_H$ | I/O Port P05 - Port Input Level Register | PILR05 | | R/W |
| 00045E$_H$ | I/O Port P06 - Port Input Level Register | PILR06 | | R/W |
| 00045F$_H$ | Reserved | | | - |
| 000460$_H$ | I/O Port P08 - Port Input Level Register | PILR08 | | R/W |
| 000461$_H$ | I/O Port P09 - Port Input Level Register | PILR09 | | R/W |
| 000462$_H$ | I/O Port P10 - Port Input Level Register | PILR10 | | R/W |
| 000463$_H$ | I/O Port P11 - Port Input Level Register | PILR11 | | R/W |
| 000464$_H$ | I/O Port P12 - Port Input Level Register | PILR12 | | R/W |
| 000465$_H$ | I/O Port P13 - Port Input Level Register | PILR13 | | R/W |
| 000466$_H$-00046B$_H$ | Reserved | | | - |
| 00046C$_H$ | I/O Port P00 - Extended Port Input Level Register | EPILR00 | | R/W |
| 00046D$_H$ | I/O Port P01 - Extended Port Input Level Register | EPILR01 | | R/W |
| 00046E$_H$ | I/O Port P02 - Extended Port Input Level Register | EPILR02 | | R/W |
| 00046F$_H$ | I/O Port P03 - Extended Port Input Level Register | EPILR03 | | R/W |
| 000470$_H$ | I/O Port P04 - Extended Port Input Level Register | EPILR04 | | R/W |
| 000471$_H$ | I/O Port P05 - Extended Port Input Level Register | EPILR05 | | R/W |
| 000472$_H$ | I/O Port P06 - Extended Port Input Level Register | EPILR06 | | R/W |
| 000473$_H$ | Reserved | | | - |
| 000474$_H$ | I/O Port P08 - Extended Port Input Level Register | EPILR08 | | R/W |
| 000475$_H$ | I/O Port P09 - Extended Port Input Level Register | EPILR09 | | R/W |
| 000476$_H$ | I/O Port P10 - Extended Port Input Level Register | EPILR10 | | R/W |
| 000477$_H$ | I/O Port P11 - Extended Port Input Level Register | EPILR11 | | R/W |
| 000478$_H$ | I/O Port P12 - Extended Port Input Level Register | EPILR12 | | R/W |
| 000479$_H$ | I/O Port P13 - Extended Port Input Level Register | EPILR13 | | R/W |
| 00047A$_H$-00047F$_H$ | Reserved | | | - |
| 000480$_H$ | I/O Port P00 - Port Output Drive Register | PODR00 | | R/W |
| 000481$_H$ | I/O Port P01 - Port Output Drive Register | PODR01 | | R/W |
| 000482$_H$ | I/O Port P02 - Port Output Drive Register | PODR02 | | R/W |

**I/O map MB96F39x (13 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000483H | I/O Port P03 - Port Output Drive Register | PODR03 | | R/W |
| 000484H | I/O Port P04 - Port Output Drive Register | PODR04 | | R/W |
| 000485H | I/O Port P05 - Port Output Drive Register | PODR05 | | R/W |
| 000486H | I/O Port P06 - Port Output Drive Register | PODR06 | | R/W |
| 000487H | Reserved | | | - |
| 000488H | I/O Port P08 - Port Output Drive Register | PODR08 | | R/W |
| 000489H | I/O Port P09 - Port Output Drive Register | PODR09 | | R/W |
| 00048AH | I/O Port P10 - Port Output Drive Register | PODR10 | | R/W |
| 00048BH | I/O Port P11 - Port Output Drive Register | PODR11 | | R/W |
| 00048CH | I/O Port P12 - Port Output Drive Register | PODR12 | | R/W |
| 00048DH | I/O Port P13 - Port Output Drive Register | PODR13 | | R/W |
| 00048EH-00049BH | Reserved | | | - |
| 00049CH | I/O Port P08 - Port High Drive Register | PHDR08 | | R/W |
| 00049DH | I/O Port P09 - Port High Drive Register | PHDR09 | | R/W |
| 00049EH | I/O Port P10 - Port High Drive Register | PHDR10 | | R/W |
| 00049FH-0004A7H | Reserved | | | - |
| 0004A8H | I/O Port P00 - Pull-Up resistor Control Register | PUCR00 | | R/W |
| 0004A9H | I/O Port P01 - Pull-Up resistor Control Register | PUCR01 | | R/W |
| 0004AAH | I/O Port P02 - Pull-Up resistor Control Register | PUCR02 | | R/W |
| 0004ABH | I/O Port P03 - Pull-Up resistor Control Register | PUCR03 | | R/W |
| 0004ACH | I/O Port P04 - Pull-Up resistor Control Register | PUCR04 | | R/W |
| 0004ADH | I/O Port P05 - Pull-Up resistor Control Register | PUCR05 | | R/W |
| 0004AEH | I/O Port P06 - Pull-Up resistor Control Register | PUCR06 | | R/W |
| 0004AFH | Reserved | | | - |
| 0004B0H | I/O Port P08 - Pull-Up resistor Control Register | PUCR08 | | R/W |
| 0004B1H | I/O Port P09 - Pull-Up resistor Control Register | PUCR09 | | R/W |
| 0004B2H | I/O Port P10 - Pull-Up resistor Control Register | PUCR10 | | R/W |
| 0004B3H | I/O Port P11 - Pull-Up resistor Control Register | PUCR11 | | R/W |
| 0004B4H | I/O Port P12 - Pull-Up resistor Control Register | PUCR12 | | R/W |

**I/O map MB96F39x (14 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0004B5H | I/O Port P13 - Pull-Up resistor Control Register | PUCR13 | | R/W |
| 0004B6H-0004BBH | Reserved | | | - |
| 0004BCH | I/O Port P00 - External Pin State Register | EPSR00 | | R |
| 0004BDH | I/O Port P01 - External Pin State Register | EPSR01 | | R |
| 0004BEH | I/O Port P02 - External Pin State Register | EPSR02 | | R |
| 0004BFH | I/O Port P03 - External Pin State Register | EPSR03 | | R |
| 0004C0H | I/O Port P04 - External Pin State Register | EPSR04 | | R |
| 0004C1H | I/O Port P05 - External Pin State Register | EPSR05 | | R |
| 0004C2H | I/O Port P06 - External Pin State Register | EPSR06 | | R |
| 0004C3H | Reserved | | | - |
| 0004C4H | I/O Port P08 - External Pin State Register | EPSR08 | | R |
| 0004C5H | I/O Port P09 - External Pin State Register | EPSR09 | | R |
| 0004C6H | I/O Port P10 - External Pin State Register | EPSR10 | | R |
| 0004C7H | I/O Port P11 - External Pin State Register | EPSR11 | | R |
| 0004C8H | I/O Port P12 - External Pin State Register | EPSR12 | | R |
| 0004C9H | I/O Port P13 - External Pin State Register | EPSR13 | | R |
| 0004CAH-0004CFH | Reserved | | | - |
| 0004D0H | ADC analog input enable register 0 | ADER0 | | R/W |
| 0004D1H | ADC analog input enable register 1 | ADER1 | | R/W |
| 0004D2H | ADC analog input enable register 2 | ADER2 | | R/W |
| 0004D3H | ADC analog input enable register 3 | ADER3 | | R/W |
| 0004D4H | ADC analog input enable register 4 | ADER4 | | R/W |
| 0004D5H | Reserved | | | - |
| 0004D6H | Peripheral Resource Relocation Register 0 | PRRR0 | | R/W |
| 0004D7H | Peripheral Resource Relocation Register 1 | PRRR1 | | R/W |
| 0004D8H | Peripheral Resource Relocation Register 2 | PRRR2 | | R/W |
| 0004D9H | Peripheral Resource Relocation Register 3 | PRRR3 | | R/W |
| 0004DAH | Peripheral Resource Relocation Register 4 | PRRR4 | | R/W |
| 0004DBH | Peripheral Resource Relocation Register 5 | PRRR5 | | R/W |

**I/O map MB96F39x (15 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0004DC$_H$ | Peripheral Resource Relocation Register 6 | PRRR6 | | R/W |
| 0004DD$_H$ | Peripheral Resource Relocation Register 7 | PRRR7 | | R/W |
| 0004DE$_H$ | Peripheral Resource Relocation Register 8 | PRRR8 | | R/W |
| 0004DF$_H$ | Peripheral Resource Relocation Register 9 | PRRR9 | | R/W |
| 0004E0$_H$ | RTC - Sub Second Register L | WTBRL0 | WTBR0 | R/W |
| 0004E1$_H$ | RTC - Sub Second Register M | WTBRH0 | | R/W |
| 0004E2$_H$ | RTC - Sub-Second Register H | WTBR1 | | R/W |
| 0004E3$_H$ | RTC - Second Register | WTSR | | R/W |
| 0004E4$_H$ | RTC - Minutes | WTMR | | R/W |
| 0004E5$_H$ | RTC - Hour | WTHR | | R/W |
| 0004E6$_H$ | RTC - Timer Control Extended Register | WTCER | | R/W |
| 0004E7$_H$ | RTC - Clock select register | WTCKSR | | R/W |
| 0004E8$_H$ | RTC - Timer Control Register Low | WTCRL | WTCR | R/W |
| 0004E9$_H$ | RTC - Timer Control Register High | WTCRH | | R/W |
| 0004EA$_H$ | CAL - Calibration unit Control register | CUCR | | R/W |
| 0004EB$_H$ | Reserved | | | - |
| 0004EC$_H$ | CAL - Duration Timer Data Register Low | CUTDL | CUTD | R/W |
| 0004ED$_H$ | CAL - Duration Timer Data Register High | CUTDH | | R/W |
| 0004EE$_H$ | CAL - Calibration Timer Register 2 Low | CUTR2L | CUTR2 | R |
| 0004EF$_H$ | CAL - Calibration Timer Register 2 High | CUTR2H | | R |
| 0004F0$_H$ | CAL - Calibration Timer Register 1 Low | CUTR1L | CUTR1 | R |
| 0004F1$_H$ | CAL - Calibration Timer Register 1 High | CUTR1H | | R |
| 0004F2$_H$-0004F9$_H$ | Reserved | | | - |
| 0004FA$_H$ | RLT - Timer input select (for Cascading) | TMISR | | R/W |
| 0004FB$_H$-00055F$_H$ | Reserved | | | - |
| 000560$_H$ | ALARM0 - Control Status Register | ACSR0 | | R/W |
| 000561$_H$ | ALARM0 - Extended Control Status Register | AECSR0 | | R/W |
| 000562$_H$-0005DF$_H$ | Reserved | | | - |

**I/O map MB96F39x (16 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0005E0H | SMC0 - PWM control register | PWC0 | | R/W |
| 0005E1H | SMC0 - Extended control register (Output enable) | PWEC0 | | R/W |
| 0005E2H | SMC0 - PWM compare register PWM 1 | | PWC10 | R/W |
| 0005E3H | SMC0 - PWM compare register PWM 1 | | | R/W |
| 0005E4H | SMC0 - PWM compare register PWM 2 | | PWC20 | R/W |
| 0005E5H | SMC0 - PWM compare register PWM 2 | | | R/W |
| 0005E6H | SMC0 - PWM Select register | PWS10 | | R/W |
| 0005E7H | SMC0 - PWM Select register | PWS20 | | R/W |
| 0005E8H-0005E9H | Reserved | | | - |
| 0005EAH | SMC1 - PWM control register | PWC1 | | R/W |
| 0005EBH | SMC1 - Extended control register (Output enable) | PWEC1 | | R/W |
| 0005ECH | SMC1 - PWM compare register PWM 1 | | PWC11 | R/W |
| 0005EDH | SMC1 - PWM compare register PWM 1 | | | R/W |
| 0005EEH | SMC1 - PWM compare register PWM 2 | | PWC21 | R/W |
| 0005EFH | SMC1 - PWM compare register PWM 2 | | | R/W |
| 0005F0H | SMC1 - PWM Select register | PWS11 | | R/W |
| 0005F1H | SMC1 - PWM Select register | PWS21 | | R/W |
| 0005F2H-0005F3H | Reserved | | | - |
| 0005F4H | SMC2 - PWM control register | PWC2 | | R/W |
| 0005F5H | SMC2 - Extended control register (Output enable) | PWEC2 | | R/W |
| 0005F6H | SMC2 - PWM compare register PWM 1 | | PWC12 | R/W |
| 0005F7H | SMC2 - PWM compare register PWM 1 | | | R/W |
| 0005F8H | SMC2 - PWM compare register PWM 2 | | PWC22 | R/W |
| 0005F9H | SMC2 - PWM compare register PWM 2 | | | R/W |
| 0005FAH | SMC2 - PWM Select register | PWS12 | | R/W |
| 0005FBH | SMC2 - PWM Select register | PWS22 | | R/W |
| 0005FCH-000607H | Reserved | | | - |
| 000608H | SMC4 - PWM control register | PWC4 | | R/W |

**I/O map MB96F39x (17 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000609H | SMC4 - Extended control register (Output enable) | PWEC4 | | R/W |
| 00060AH | SMC4 - PWM compare register PWM 1 | | PWC14 | R/W |
| 00060BH | SMC4 - PWM compare register PWM 1 | | | R/W |
| 00060CH | SMC4 - PWM compare register PWM 2 | | PWC24 | R/W |
| 00060DH | SMC4 - PWM compare register PWM 2 | | | R/W |
| 00060EH | SMC4 - PWM Select register | PWS14 | | R/W |
| 00060FH | SMC4 - PWM Select register | PWS24 | | R/W |
| 000610H-00061BH | Reserved | | | - |
| 00061CH | LCD - Output Enable Register 0 (Seg 7-0) | LCDER0 | | R/W |
| 00061DH | LCD - Output Enable Register 1 (Seg 15-8) | LCDER1 | | R/W |
| 00061EH | LCD - Output Enable Register 2 (Seg 23-16) | LCDER2 | | R/W |
| 00061FH | LCD - Output Enable Register 3 (Seg 31-24) | LCDER3 | | R/W |
| 000620H | LCD - Output Enable Register 4 (Seg 39-32) | LCDER4 | | R/W |
| 000621H | LCD - Output Enable Register 5 (Seg 47-40) | LCDER5 | | R/W |
| 000622H | LCD - Output Enable Register 6 (Seg 55-48) | LCDER6 | | R/W |
| 000623H | LCD - Output Enable Register 7 (Seg 63-56) | LCDER7 | | R/W |
| 000624H | LCD - Output Enable Register 8 (Seg 71-64) | LCDER8 | | R/W |
| 000625H | Reserved | | | - |
| 000626H | LCD - Output Enable Register V (Vx) | LCDVER | | R/W |
| 000627H | LCD - Extended Control Register | LECR | | R/W |
| 000628H | LCD - Common pin switching register | LCDCMR | | R/W |
| 000629H | LCD - Control Register | LCR | | R/W |
| 00062AH | LCD - Data register for Segment 1-0 | VRAM0 | | R/W |
| 00062BH | LCD - Data register for Segment 3-2 | VRAM1 | | R/W |
| 00062CH | LCD - Data register for Segment 5-4 | VRAM2 | | R/W |
| 00062DH | LCD - Data register for Segment 7-6 | VRAM3 | | R/W |
| 00062EH | LCD - Data register for Segment 9-8 | VRAM4 | | R/W |
| 00062FH | LCD - Data register for Segment 11-10 | VRAM5 | | R/W |
| 000630H | LCD - Data register for Segment 13-12 | VRAM6 | | R/W |

**I/O map MB96F39x (18 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000631H | LCD - Data register for Segment 15-14 | VRAM7 | | R/W |
| 000632H | LCD - Data register for Segment 17-16 | VRAM8 | | R/W |
| 000633H | LCD - Data register for Segment 19-18 | VRAM9 | | R/W |
| 000634H | LCD - Data register for Segment 21-20 | VRAM10 | | R/W |
| 000635H | LCD - Data register for Segment 23-22 | VRAM11 | | R/W |
| 000636H | LCD - Data register for Segment 25-24 | VRAM12 | | R/W |
| 000637H | LCD - Data register for Segment 27-26 | VRAM13 | | R/W |
| 000638H | LCD - Data register for Segment 29-28 | VRAM14 | | R/W |
| 000639H | LCD - Data register for Segment 31-30 | VRAM15 | | R/W |
| 00063AH | LCD - Data register for Segment 33-32 | VRAM16 | | R/W |
| 00063BH | LCD - Data register for Segment 35-34 | VRAM17 | | R/W |
| 00063CH | LCD - Data register for Segment 37-36 | VRAM18 | | R/W |
| 00063DH | LCD - Data register for Segment 39-38 | VRAM19 | | R/W |
| 00063EH | LCD - Data register for Segment 41-40 | VRAM20 | | R/W |
| 00063FH | LCD - Data register for Segment 43-42 | VRAM21 | | R/W |
| 000640H | LCD - Data register for Segment 45-44 | VRAM22 | | R/W |
| 000641H | LCD - Data register for Segment 47-46 | VRAM23 | | R/W |
| 000642H | LCD - Data register for Segment 49-48 | VRAM24 | | R/W |
| 000643H | LCD - Data register for Segment 51-50 | VRAM25 | | R/W |
| 000644H | LCD - Data register for Segment 53-52 | VRAM26 | | R/W |
| 000645H | LCD - Data register for Segment 55-54 | VRAM27 | | R/W |
| 000646H | LCD - Data register for Segment 57-56 | VRAM28 | | R/W |
| 000647H | LCD - Data register for Segment 59-58 | VRAM29 | | R/W |
| 000648H | LCD - Data register for Segment 61-60 | VRAM30 | | R/W |
| 000649H | LCD - Data register for Segment 63-62 | VRAM31 | | R/W |
| 00064AH | LCD - Data register for Segment 65-64 | VRAM32 | | R/W |
| 00064BH-00065FH | Reserved | | | - |
| 000660H | Peripheral Resource Relocation Register 10 | PRRR10 | | R/W |
| 000661H | Peripheral Resource Relocation Register 11 | PRRR11 | | R/W |

**I/O map MB96F39x (19 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000662H | Peripheral Resource Relocation Register 12 | PRRR12 | | R/W |
| 000663H | Peripheral Resource Relocation Register 13 | PRRR13 | | W |
| 000664H-0006FFH | Reserved | | | - |
| 000700H | CAN0 - Control register Low | CTRLRL0 | CTRLR0 | R/W |
| 000701H | CAN0 - Control register High (reserved) | CTRLRH0 | | R |
| 000702H | CAN0 - Status register Low | STATRL0 | STATR0 | R/W |
| 000703H | CAN0 - Status register High (reserved) | STATRH0 | | R |
| 000704H | CAN0 - Error Counter Low (Transmit) | ERRCNTL0 | ERRCNT0 | R |
| 000705H | CAN0 - Error Counter High (Receive) | ERRCNTH0 | | R |
| 000706H | CAN0 - Bit Timing Register Low | BTRL0 | BTR0 | R/W |
| 000707H | CAN0 - Bit Timing Register High | BTRH0 | | R/W |
| 000708H | CAN0 - Interrupt Register Low | INTRL0 | INTR0 | R |
| 000709H | CAN0 - Interrupt Register High | INTRH0 | | R |
| 00070AH | CAN0 - Test Register Low | TESTRL0 | TESTR0 | R/W |
| 00070BH | CAN0 - Test Register High (reserved) | TESTRH0 | | R |
| 00070CH | CAN0 - BRP Extension register Low | BRPERL0 | BRPER0 | R/W |
| 00070DH | CAN0 - BRP Extension register High (reserved) | BRPERH0 | | R |
| 00070EH-00070FH | Reserved | | | - |
| 000710H | CAN0 - IF1 Command request register Low | IF1CREQL0 | IF1CREQ0 | R/W |
| 000711H | CAN0 - IF1 Command request register High | IF1CREQH0 | | R/W |
| 000712H | CAN0 - IF1 Command Mask register Low | IF1CMSKL0 | IF1CMSK0 | R/W |
| 000713H | CAN0 - IF1 Command Mask register High (reserved) | IF1CMSKH0 | | R |
| 000714H | CAN0 - IF1 Mask 1 Register Low | IF1MSK1L0 | IF1MSK10 | R/W |
| 000715H | CAN0 - IF1 Mask 1 Register High | IF1MSK1H0 | | R/W |
| 000716H | CAN0 - IF1 Mask 2 Register Low | IF1MSK2L0 | IF1MSK20 | R/W |
| 000717H | CAN0 - IF1 Mask 2 Register High | IF1MSK2H0 | | R/W |
| 000718H | CAN0 - IF1 Arbitration 1 Register Low | IF1ARB1L0 | IF1ARB10 | R/W |
| 000719H | CAN0 - IF1 Arbitration 1 Register High | IF1ARB1H0 | | R/W |

**I/O map MB96F39x (20 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 00071A$_H$ | CAN0 - IF1 Arbitration 2 Register Low | IF1ARB2L0 | IF1ARB20 | R/W |
| 00071B$_H$ | CAN0 - IF1 Arbitration 2 Register High | IF1ARB2H0 | | R/W |
| 00071C$_H$ | CAN0 - IF1 Message Control Register Low | IF1MCTRL0 | IF1MCTR0 | R/W |
| 00071D$_H$ | CAN0 - IF1 Message Control Register High | IF1MCTRH0 | | R/W |
| 00071E$_H$ | CAN0 - IF1 Data A1 Low | IF1DTA1L0 | IF1DTA10 | R/W |
| 00071F$_H$ | CAN0 - IF1 Data A1 High | IF1DTA1H0 | | R/W |
| 000720$_H$ | CAN0 - IF1 Data A2 Low | IF1DTA2L0 | IF1DTA20 | R/W |
| 000721$_H$ | CAN0 - IF1 Data A2 High | IF1DTA2H0 | | R/W |
| 000722$_H$ | CAN0 - IF1 Data B1 Low | IF1DTB1L0 | IF1DTB10 | R/W |
| 000723$_H$ | CAN0 - IF1 Data B1 High | IF1DTB1H0 | | R/W |
| 000724$_H$ | CAN0 - IF1 Data B2 Low | IF1DTB2L0 | IF1DTB20 | R/W |
| 000725$_H$ | CAN0 - IF1 Data B2 High | IF1DTB2H0 | | R/W |
| 000726$_H$-00073F$_H$ | Reserved | | | - |
| 000740$_H$ | CAN0 - IF2 Command request register Low | IF2CREQL0 | IF2CREQ0 | R/W |
| 000741$_H$ | CAN0 - IF2 Command request register High | IF2CREQH0 | | R/W |
| 000742$_H$ | CAN0 - IF2 Command Mask register Low | IF2CMSKL0 | IF2CMSK0 | R/W |
| 000743$_H$ | CAN0 - IF2 Command Mask register High (reserved) | IF2CMSKH0 | | R |
| 000744$_H$ | CAN0 - IF2 Mask 1 Register Low | IF2MSK1L0 | IF2MSK10 | R/W |
| 000745$_H$ | CAN0 - IF2 Mask 1 Register High | IF2MSK1H0 | | R/W |
| 000746$_H$ | CAN0 - IF2 Mask 2 Register Low | IF2MSK2L0 | IF2MSK20 | R/W |
| 000747$_H$ | CAN0 - IF2 Mask 2 Register High | IF2MSK2H0 | | R/W |
| 000748$_H$ | CAN0 - IF2 Arbitration 1 Register Low | IF2ARB1L0 | IF2ARB10 | R/W |
| 000749$_H$ | CAN0 - IF2 Arbitration 1 Register High | IF2ARB1H0 | | R/W |
| 00074A$_H$ | CAN0 - IF2 Arbitration 2 Register Low | IF2ARB2L0 | IF2ARB20 | R/W |
| 00074B$_H$ | CAN0 - IF2 Arbitration 2 Register High | IF2ARB2H0 | | R/W |
| 00074C$_H$ | CAN0 - IF2 Message Control Register Low | IF2MCTRL0 | IF2MCTR0 | R/W |
| 00074D$_H$ | CAN0 - IF2 Message Control Register High | IF2MCTRH0 | | R/W |
| 00074E$_H$ | CAN0 - IF2 Data A1 Low | IF2DTA1L0 | IF2DTA10 | R/W |
| 00074F$_H$ | CAN0 - IF2 Data A1 High | IF2DTA1H0 | | R/W |

**I/O map MB96F39x (21 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 000750H | CAN0 - IF2 Data A2 Low | IF2DTA2L0 | IF2DTA20 | R/W |
| 000751H | CAN0 - IF2 Data A2 High | IF2DTA2H0 | | R/W |
| 000752H | CAN0 - IF2 Data B1 Low | IF2DTB1L0 | IF2DTB10 | R/W |
| 000753H | CAN0 - IF2 Data B1 High | IF2DTB1H0 | | R/W |
| 000754H | CAN0 - IF2 Data B2 Low | IF2DTB2L0 | IF2DTB20 | R/W |
| 000755H | CAN0 - IF2 Data B2 High | IF2DTB2H0 | | R/W |
| 000756H-00077FH | Reserved | | | - |
| 000780H | CAN0 - Transmission Request 1 Register Low | TREQR1L0 | TREQR10 | R |
| 000781H | CAN0 - Transmission Request 1 Register High | TREQR1H0 | | R |
| 000782H | CAN0 - Transmission Request 2 Register Low | TREQR2L0 | TREQR20 | R |
| 000783H | CAN0 - Transmission Request 2 Register High | TREQR2H0 | | R |
| 000784H-00078FH | Reserved | | | - |
| 000790H | CAN0 - New Data 1 Register Low | NEWDT1L0 | NEWDT10 | R |
| 000791H | CAN0 - New Data 1 Register High | NEWDT1H0 | | R |
| 000792H | CAN0 - New Data 2 Register Low | NEWDT2L0 | NEWDT20 | R |
| 000793H | CAN0 - New Data 2 Register High | NEWDT2H0 | | R |
| 000794H-00079FH | Reserved | | | - |
| 0007A0H | CAN0 - Interrupt Pending 1 Register Low | INTPND1L0 | INTPND10 | R |
| 0007A1H | CAN0 - Interrupt Pending 1 Register High | INTPND1H0 | | R |
| 0007A2H | CAN0 - Interrupt Pending 2 Register Low | INTPND2L0 | INTPND20 | R |
| 0007A3H | CAN0 - Interrupt Pending 2 Register High | INTPND2H0 | | R |
| 0007A4H-0007AFH | Reserved | | | - |
| 0007B0H | CAN0 - Message Valid 1 Register Low | MSGVAL1L0 | MSGVAL10 | R |
| 0007B1H | CAN0 - Message Valid 1 Register High | MSGVAL1H0 | | R |
| 0007B2H | CAN0 - Message Valid 2 Register Low | MSGVAL2L0 | MSGVAL20 | R |
| 0007B3H | CAN0 - Message Valid 2 Register High | MSGVAL2H0 | | R |
| 0007B4H-0007CDH | Reserved | | | - |

**I/O map MB96F39x (22 of 22)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| 0007CE$_H$ | CAN0 - Output enable register | COER0 | | R/W |
| 0007CF$_H$ | Reserved | | | - |
| 0007D0$_H$ | SG0 - Sound Generator Control Register Low | SGCRL0 | SGCR0 | R/W |
| 0007D1$_H$ | SG0 - Sound Generator Control Register High | SGCRH0 | | R/W |
| 0007D2$_H$ | SG0 - Sound Generator Frequency Register | SGFR0 | | R/W |
| 0007D3$_H$ | SG0 - Sound Generator Amplitude Register | SGAR0 | | R/W |
| 0007D4$_H$ | SG0 - Sound Generator Decrement Register | SGDR0 | | R/W |
| 0007D5$_H$ | SG0 - Sound Generator Tone Register | SGTR0 | | R/W |
| 0007D6$_H$-000BFF$_H$ | Reserved | | | - |

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

## ■ INTERRUPT VECTOR TABLE

**Interrupt vector table MB96(F)39x (1 of 3)**

| Vector number | Offset in vector table | Vector name | Index in ICR to program | Description |
|---|---|---|---|---|
| 0 | 3FC$_H$ | CALLV0 | - | |
| 1 | 3F8$_H$ | CALLV1 | - | |
| 2 | 3F4$_H$ | CALLV2 | - | |
| 3 | 3F0$_H$ | CALLV3 | - | |
| 4 | 3EC$_H$ | CALLV4 | - | |
| 5 | 3E8$_H$ | CALLV5 | - | |
| 6 | 3E4$_H$ | CALLV6 | - | |
| 7 | 3E0$_H$ | CALLV7 | - | |
| 8 | 3DC$_H$ | RESET | - | |
| 9 | 3D8$_H$ | INT9 | - | |
| 10 | 3D4$_H$ | EXCEPTION | - | |
| 11 | 3D0$_H$ | NMI | - | Non-Maskable Interrupt |
| 12 | 3CC$_H$ | DLY | 12 | Delayed Interrupt |
| 13 | 3C8$_H$ | RC_TIMER | 13 | RC Timer |
| 14 | 3C4$_H$ | MC_TIMER | 14 | Main Clock Timer |
| 15 | 3C0$_H$ | SC_TIMER | 15 | Sub Clock Timer |
| 16 | 3BC$_H$ | | | Reserved |
| 17 | 3B8$_H$ | EXTINT0 | 17 | External Interrupt 0 |
| 18 | 3B4$_H$ | EXTINT1 | 18 | External Interrupt 1 |
| 19 | 3B0$_H$ | EXTINT2 | 19 | External Interrupt 2 |
| 20 | 3AC$_H$ | EXTINT3 | 20 | External Interrupt 3 |
| 21 | 3A8$_H$ | EXTINT4 | 21 | External Interrupt 4 |
| 22 | 3A4$_H$ | EXTINT5 | 22 | External Interrupt 5 |
| 23 | 3A0$_H$ | EXTINT6 | 23 | External Interrupt 6 |
| 24 | 39C$_H$ | EXTINT7 | 24 | External Interrupt 7 |
| 25 | 398$_H$ | CAN0 | 25 | CAN Controller 0 |
| 26 | 394$_H$ | | | Reserved |
| 27 | 390$_H$ | PPG0 | 27 | Programmable Pulse Generator 0 |
| 28 | 38C$_H$ | PPG1 | 28 | Programmable Pulse Generator 1 |
| 29 | 388$_H$ | PPG2 | 29 | Programmable Pulse Generator 2 |
| 30 | 384$_H$ | PPG3 | 30 | Programmable Pulse Generator 3 |
| 31 | 380$_H$ | | | Reserved |
| 32 | 37C$_H$ | | | Reserved |

**Interrupt vector table MB96(F)39x (2 of 3)**

| Vector number | Offset in vector table | Vector name | Index in ICR to program | Description |
|---|---|---|---|---|
| 33 | 378H | | | Reserved |
| 34 | 374H | | | Reserved |
| 35 | 370H | RLT0 | 35 | Reload Timer 0 |
| 36 | 36CH | RLT1 | 36 | Reload Timer 1 |
| 37 | 368H | RLT2 | 37 | Reload Timer 2 |
| 38 | 364H | RLT3 | 38 | Reload Timer 3 |
| 39 | 360H | PPGRLT | 39 | Reload Timer 6 - dedicated for PPG |
| 40 | 35CH | ICU0 | 40 | Input Capture Unit 0 |
| 41 | 358H | ICU1 | 41 | Input Capture Unit 1 |
| 42 | 354H | | | Reserved |
| 43 | 350H | | | Reserved |
| 44 | 34CH | | | Reserved |
| 45 | 348H | | | Reserved |
| 46 | 344H | ICU6 | 46 | Input Capture Unit 6 |
| 47 | 340H | ICU7 | 47 | Input Capture Unit 7 |
| 48 | 33CH | OCU0 | 48 | Output Compare Unit 0 |
| 49 | 338H | OCU1 | 49 | Output Compare Unit 1 |
| 50 | 334H | OCU2 | 50 | Output Compare Unit 2 |
| 51 | 330H | OCU3 | 51 | Output Compare Unit 3 |
| 52 | 32CH | FRT0 | 52 | Free Running Timer 0 |
| 53 | 328H | FRT1 | 53 | Free Running Timer 1 |
| 54 | 324H | RTC0 | 54 | Real Timer Clock |
| 55 | 320H | CAL0 | 55 | Clock Calibration Unit |
| 56 | 31CH | SG0 | 56 | Sound Generator 0 |
| 57 | 318H | | | Reserved |
| 58 | 314H | IIC0 | 58 | I2C interface |
| 59 | 310H | ADC0 | 59 | A/D Converter |
| 60 | 30CH | ALARM0 | 60 | Alarm Comparator 0 |
| 61 | 308H | | | Reserved |
| 62 | 304H | LINR0 | 62 | LIN USART 0 RX |
| 63 | 300H | LINT0 | 63 | LIN USART 0 TX |
| 64 | 2FCH | LINR1 | 64 | LIN USART 1 RX |
| 65 | 2F8H | LINT1 | 65 | LIN USART 1 TX |
| 66 | 2F4H | LINR2 | 66 | LIN USART 2 RX |
| 67 | 2F0H | LINT2 | 67 | LIN USART 2 TX |

**Interrupt vector table MB96(F)39x (3 of 3)**

| Vector number | Offset in vector table | Vector name | Index in ICR to program | Description |
|---|---|---|---|---|
| 68 | 2EC$_H$ | | | Reserved |
| 69 | 2E8$_H$ | | | Reserved |
| 70 | 2E4$_H$ | | | Reserved |
| 71 | 2E0$_H$ | | | Reserved |
| 72 | 2DC$_H$ | FLASH_A | 72 | Flash memory A (only Flash devices) |
| 73 | 2D8$_H$ | | | Reserved |

## ■ HANDLING DEVICES

### Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins ($V_{CC}$/$V_{SS}$)
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication

### 1. Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between $V_{CC}$ pins and $V_{SS}$ pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

### 2. Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

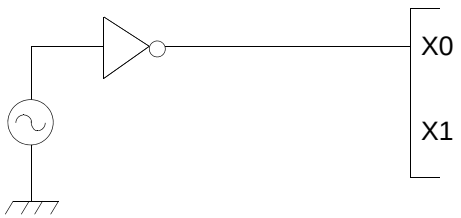
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

### 3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

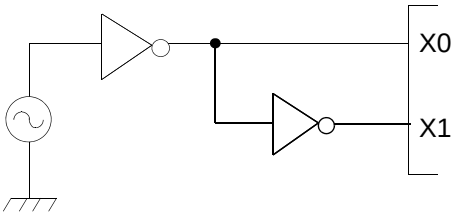
**1. Single phase external clock**

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.



**2. Opposite phase external clock**

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.




## 4. Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

## 5. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

## 6. Power supply pins ($V_{CC}$/$V_{SS}$)

It is required that all $V_{CC}$-level as well as all $V_{SS}$-level power supply pins are at the same potential. If there is more than one $V_{CC}$ or $V_{SS}$ level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

$V_{CC}$ and $V_{SS}$ must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between $V_{CC}$ and $V_{SS}$ as close as possible to $V_{CC}$ and $V_{SS}$ pins.

## 7. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

## 8. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply ($V_{CC}$) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or $AV_{CC}$ (turning the analog and digital power supplies simultaneously on or off is acceptable).

## 9. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS}$ = AVRH = AVRL = $V_{SS}$.

## 10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

## 11. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

## 12. SMC power supply pins

All $DV_{SS}$ pins must be set to the same level as the $V_{SS}$ pins.

The $DV_{CC}$ power supply level can be set independently of the $V_{CC}$ power supply level. However note that the SMC I/O pin state is undefined if $DV_{CC}$ is powered on and $V_{CC}$ is below 3V. To avoid this, we recommend to always power $V_{CC}$ before $DV_{CC}$.

## 13. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

## ■ ELECTRICAL CHARACTERISTICS

## 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC} = AV_{CC}$ *1 |
| AD Converter voltage references | AVRH, AVRL | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL $\geq AV_{SS}$ |
| SMC Power supply | $DV_{CC}$ | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | See *7 |
| LCD power supply voltage | V0 to V3 | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | V0 to V3 must not exceed $V_{CC}$ |
| Input voltage | $V_I$ | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $V_I \leq$ (D)$V_{CC}$ + 0.3V *2 |
| Output voltage | $V_O$ | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $V_O \leq$ (D)$V_{CC}$ + 0.3V *2 |
| Maximum Clamp Current | $I_{CLAMP}$ | -4.0 | +4.0 | mA | Applicable to general purpose I/O pins *3 |
| Total Maximum Clamp Current | $\Sigma\|I_{CLAMP}\|$ | - | 40 | mA | Applicable to general purpose I/O pins *3 |
| “L” level maximum output current | $I_{OL1}$ | - | 15 | mA | Normal outputs with driving strength set to 5mA |
| | $I_{OLSMC}$ | - | 40 | mA | High current outputs with driving strength set to 30mA |
| “L” level average output current | $I_{OLAV1}$ | - | 5 | mA | Normal outputs with driving strength set to 5mA |
| | $I_{OLAVSMC}$ | - | 30 | mA | High current outputs with driving strength set to 30mA |
| “L” level maximum overall output current | $\Sigma I_{OL1}$ | - | 100 | mA | Normal outputs |
| | $\Sigma I_{OLSMC}$ | - | 330 | mA | High current outputs |
| “L” level average overall output current | $\Sigma I_{OLAV1}$ | - | 50 | mA | Normal outputs |
| | $\Sigma I_{OLAVSMC}$ | - | 250 | mA | High current outputs |
| ”H” level maximum output current | $I_{OH1}$ | - | -15 | mA | Normal outputs with driving strength set to 5mA |
| | $I_{OHSMC}$ | - | -40 | mA | High current outputs with driving strength set to 30mA |
| ”H” level average output current | $I_{OHAV1}$ | - | -5 | mA | Normal outputs with driving strength set to 5mA |
| | $I_{OHAVSMC}$ | - | -30 | mA | High current outputs with driving strength set to 30mA |
| ”H” level maximum overall output current | $\Sigma I_{OH1}$ | - | -100 | mA | Normal outputs |
| | $\Sigma I_{OHSMC}$ | - | -330 | mA | High current outputs |
| ”H” level average overall output current | $\Sigma I_{OHAV1}$ | - | -50 | mA | Normal outputs |
| | $\Sigma I_{OHASMC}$ | - | -250 | mA | High current outputs |

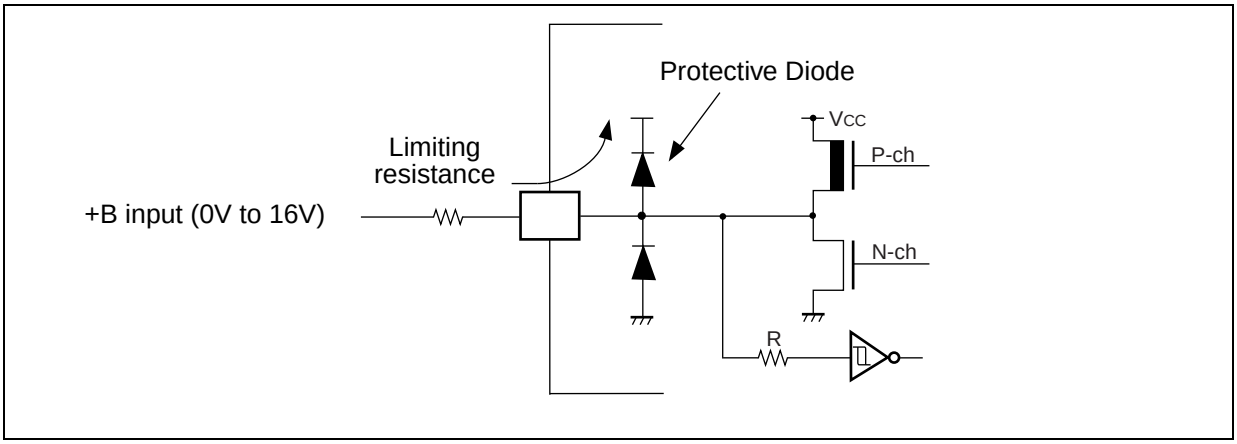
| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Permitted Power dissipation (MB96F395) *4 | $P_D$ | - | 255*5 | mW | $T_A$=105°C |
| | | - | 510*5 | mW | $T_A$=85°C |
| | | - | 830*5 | mW | $T_A$=60°C |
| | | - | 320*5 | mW | $T_A$=125°C, no Flash program/ erase *6 |
| | | - | 575*5 | mW | $T_A$=105°C, no Flash program/ erase *6 |
| Operating ambient temperature | $T_A$ | 0 | +70 | °C | MB96V300B |
| | | -40 | +105 | | |
| | | -40 | +125 | | *6 |
| Storage temperature | $T_{STG}$ | -55 | +150 | °C | |

*1: $AV_{CC}$ and $V_{CC}$ must be set to the same voltage. It is required that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ neither when the power is switched on.

*2: $V_I$ and $V_O$ should not exceed (D)$V_{CC}$ + 0.3 V. $V_I$ should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating. Input/output voltages of high current ports depend on $DV_{CC}$. Input/output voltages of standard ports depend on $V_{CC}$.

*3: • Applicable to all general purpose I/O pins (Pnn_m) except I/O pins with SEG or COM functionality.
• Use within recommended operating conditions.
• Use at DC voltage (current)
• The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
• Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
• Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
• No +B signal must be applied to any LCD I/O pin (including unused SEG/COM pins).

• Sample recommended circuits:




*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
$I_{CC}$ is the total core current consumption into $V_{CC}$ as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
$I_A$ is the analog current consumption into $AV_{CC}$.

*5: Worst case value for a package mounted on single layer PCB at specified $T_A$ without air flow.

*6: Please contact Fujitsu for reliability limitations when using under these conditions.

*7: If $DV_{CC}$ is powered before $V_{CC}$, then SMC I/O pins state is undefined. To avoid this, we recommend to always power $V_{CC}$ before $DV_{CC}$. It is not necessary to set $V_{CC}$ and $DV_{CC}$ to the same value.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $DV_{CC}$ | 3.0 | - | 5.5 | V | |
| Smoothing capacitor at C pin | $C_S$ | 3.5 | 4.7 - 10 | 15 | µF | Use a low inductance capacitor (for example X7R ceramic capacitor) |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## 3. DC characteristics

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input H voltage | $V_{IH}$ | Port inputs Pnn_m | CMOS Hysteresis 0.8/0.2 input selected | 0.8 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | |
| | | | CMOS Hysteresis 0.7/0.3 input selected | 0.7 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | (D)$V_{CC}$ ≥ 4.5V |
| | | | | 0.74 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | (D)$V_{CC}$ < 4.5V |
| | | | AUTOMOTIVE Hysteresis input selected | 0.8 $V_{CC}$ | - | (D)$V_{CC}$ + 0.3 | V | |
| | | | TTL input selected | 2.0 | - | (D)$V_{CC}$ + 0.3 | V | |
| | $V_{IHX0F}$ | X0 | External clock in “Fast Clock Input mode” | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | |
| | $V_{IHX0S}$ | X0,X1, X0A,X1A | External clock in “oscillation mode” | 2.5 | - | $V_{CC}$ + 0.3 | V | |
| | $V_{IHR}$ | RSTX | - | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | CMOS Hysteresis input |
| | $V_{IHM}$ | MD2-MD0 | - | $V_{CC}$ - 0.3 | - | $V_{CC}$ + 0.3 | V | |
| Input L voltage | $V_{IL}$ | Port inputs Pnn_m | CMOS Hysteresis 0.8/0.2 input selected | $V_{SS}$ - 0.3 | - | 0.2 (D)$V_{CC}$ | V | |
| | | | CMOS Hysteresis 0.7/0.3 input selected | $V_{SS}$ - 0.3 | - | 0.3 (D)$V_{CC}$ | V | |
| | | | AUTOMOTIVE Hysteresis input selected | $V_{SS}$ - 0.3 | - | 0.5 (D)$V_{CC}$ | V | (D)$V_{CC}$ ≥ 4.5V |
| | | | | $V_{SS}$ - 0.3 | - | 0.46 (D)$V_{CC}$ | | (D)$V_{CC}$ < 4.5V |
| | | | TTL input selected | $V_{SS}$ - 0.3 | - | 0.8 | V | |
| | $V_{ILX0F}$ | X0 | External clock in “Fast Clock Input mode” | $V_{SS}$ - 0.3 | - | 0.2 $V_{CC}$ | V | |
| | $V_{ILX0S}$ | X0,X1, X0A,X1A | External clock in “oscillation mode” | $V_{SS}$ - 0.3 | - | 0.4 | V | |
| | $V_{ILR}$ | RSTX | - | $V_{SS}$ - 0.3 | - | 0.2 $V_{CC}$ | V | CMOS Hysteresis input |
| | $V_{ILM}$ | MD2-MD0 | - | $V_{SS}$ - 0.3 | - | $V_{SS}$ + 0.3 | V | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Output H voltage | $V_{OH2}$ | Normaland High Current outputs | 4.5V ≤ (D)$V_{CC}$ ≤ 5.5V<br>$I_{OH}$ = -2mA<br>3.0V ≤ (D)$V_{CC}$ < 4.5V<br>$I_{OH}$ = -1.6mA | (D)$V_{CC}$ - 0.5 | - | - | V | Driving strength set to 2mA |
| | $V_{OH5}$ | Normaland High Current outputs | 4.5V ≤ (D)$V_{CC}$ ≤ 5.5V<br>$I_{OH}$ = -5mA<br>3.0V ≤ (D)$V_{CC}$ < 4.5V<br>$I_{OH}$ = -3mA | (D)$V_{CC}$ - 0.5 | - | - | V | Driving strength set to 5mA |
| | $V_{OH30}$ | High current outputs | 4.5V ≤ $DV_{CC}$ ≤ 5.5V<br>$I_{OH}$ = -30mA<br>3.0V ≤ $DV_{CC}$ < 4.5V<br>$I_{OH}$ = -20mA | $DV_{CC}$ - 0.5 | - | - | V | Driving strength set to 30mA |
| | $V_{OH3}$ | 3mA outputs | 4.5V ≤ $V_{CC}$ ≤ 5.5V<br>$I_{OH}$ = -3mA<br>3.0V ≤ $V_{CC}$ < 4.5V<br>$I_{OH}$ = -2mA | $V_{CC}$ - 0.5 | - | - | V | |
| Output L voltage | $V_{OL2}$ | Normaland High Current outputs | 4.5V ≤ (D)$V_{CC}$ ≤ 5.5V<br>$I_{OL}$ = +2mA<br>3.0V ≤ (D)$V_{CC}$ < 4.5V<br>$I_{OL}$ = +1.6mA | - | - | 0.4 | V | Driving strength set to 2mA |
| | $V_{OL5}$ | Normaland High Current outputs | 4.5V ≤ (D)$V_{CC}$ ≤ 5.5V<br>$I_{OL}$ = +5mA<br>3.0V ≤ (D)$V_{CC}$ < 4.5V<br>$I_{OL}$ = +3mA | - | - | 0.4 | V | Driving strength set to 5mA |
| | $V_{OL30}$ | High current outputs | 4.5V ≤ $DV_{CC}$ ≤ 5.5V<br>$I_{OL}$ = +30mA<br>3.0V ≤ $DV_{CC}$ < 4.5V<br>$I_{OL}$ = +20mA | - | - | 0.5 | V | Driving strength set to 30mA |
| | $V_{OL3}$ | 3mA outputs | 3.0V ≤ $V_{CC}$ ≤ 5.5V<br>$I_{OL}$ = +3mA | - | - | 0.4 | V | |
| Input leak current | $I_{IL}$ | Pnn_m | $V_{SS}$ < $V_I$ < $V_{CC}$<br>$AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH | -1 | - | +1 | µA | Single port pin |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Total LCD leak current | $\Sigma\lvert I_{ILCD}\rvert$ | all SEG/ COM pins | $V_{CC}$ = 5.0V | - | 0.5 | 10 | µA | Maximum leakage current of all LCD pins |
| Internal LCD divide resistance | $R_{LCD}$ | Between V3 and $V_{SS}$ | $V_{CC}$ = 5.0V | 25 | 40 | 65 | kΩ | |
| Pull-up resistance | $R_{UP}$ | Pnn_m, RSTX | $V_{CC}$ = 3.3V ± 10% | 40 | 100 | 160 | kΩ | |
| | | | $V_{CC}$ = 5.0V ± 10% | 25 | 50 | 100 | kΩ | |

Note: Input/output voltages of high current ports depend on $DV_{CC}$, of other ports on $V_{CC}$.

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Run modes* | $I_{CCPLL}$ | PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V) | +25°C | 35 | 44 | mA | MB96F395 at 0 Flash wait states |
| | | | +125°C | 36 | 47 | | |
| | | PLL Run mode with CLKS1/2 = 80MHz, CLKB = CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V) | +25°C | 43 | 55 | mA | MB96F395 at 1 Flash wait state |
| | | | +125°C | 44 | 57 | | |
| | $I_{CCMAIN}$ | Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped) | +25°C | 4.5 | 5.5 | mA | MB96F395 at 1 Flash wait state |
| | | | +125°C | 5.1 | 7.5 | | |
| | $I_{CCRCH}$ | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped) | +25°C | 2.5 | 3.6 | mA | MB96F395 at 1 Flash wait state |
| | | | +125°C | 3.1 | 5.1 | | |
| | $I_{CCRCL}$ | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25°C | 0.4 | 0.6 | | MB96F395 at 1 ROM/ Flash wait state |
| | | | +125°C | 0.9 | 2 | | |
| | | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed) | +25°C | 0.15 | 0.25 | mA | MB96F395 at 1 ROM/ Flash wait state |
| | | | +125°C | 0.65 | 1.75 | | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Run modes* | $I_{CCSUB}$ | Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed) | +25°C | 0.1 | 0.2 | mA | MB96F395 at 1 ROM/ Flash wait state |
| | | | +125°C | 0.6 | 1.7 | | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Sleep modes* | $I_{CCSPLL}$ | PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V) | +25°C | 7.5 | 9 | mA | MB96F395 |
| | | | +125°C | 8.2 | 10.5 | | |
| | | PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V) | +25°C | 13 | 14.5 | mA | MB96F395 |
| | | | +125°C | 13.8 | 16 | | |
| | $I_{CCSMAIN}$ | Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped) | +25°C | 1.5 | 1.8 | mA | MB96F395 |
| | | | +125°C | 2 | 3.3 | | |
| | $I_{CCSRCH}$ | RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped) | +25°C | 0.9 | 1.4 | mA | MB96F395 |
| | | | +125°C | 1.5 | 2.8 | | |
| | $I_{CCSRCL}$ | RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25°C | 0.3 | 0.5 | mA | MB96F395 |
| | | | +125°C | 0.8 | 2 | | |
| | | RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode) | +25°C | 0.06 | 0.15 | mA | MB96F395 |
| | | | +125°C | 0.56 | 1.6 | | |
| | $I_{CCSSUB}$ | Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped) | +25°C | 0.04 | 0.12 | mA | MB96F395 |
| | | | +125°C | 0.54 | 1.55 | | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Timer modes* | $I_{CCTPLL}$ | PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V) | +25°C | 1.6 | 2 | mA | MB96F395 |
| | | | +125°C | 2.1 | 3.5 | | |
| | $I_{CCTMAIN}$ | Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode) | +25°C | 0.35 | 0.5 | mA | MB96F395 |
| | | | +125°C | 0.85 | 2 | | |
| | | Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode) | +25°C | 0.1 | 0.18 | | MB96F395 |
| | | | +125°C | 0.6 | 1.6 | | |
| | $I_{CCTRCH}$ | RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25°C | 0.35 | 0.5 | mA | MB96F395 |
| | | | +125°C | 0.85 | 2 | | |
| | | RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode) | +25°C | 0.1 | 0.15 | mA | MB96F395 |
| | | | +125°C | 0.6 | 1.6 | | |

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Power supply current in Timer modes* | $I_{CCTRCL}$ | RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25°C | 0.3 | 0.45 | mA | MB96F395 |
| | | | +125°C | 0.8 | 1.95 | | |
| | | RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode) | +25°C | 0.05 | 0.1 | mA | MB96F395 |
| | | | +125°C | 0.55 | 1.55 | | |
| | $I_{CCTSUB}$ | Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped) | +25°C | 0.03 | 0.1 | mA | MB96F395 |
| | | | +125°C | 0.53 | 1.55 | | |
| Power supply current in Stop Mode | $I_{CCH}$ | VRCR:LPMB[2:0] = $110_B$ (Core voltage at 1.8V) | +25°C | 0.02 | 0.08 | mA | MB96F395 |
| | | | +125°C | 0.52 | 1.5 | | |
| | | VRCR:LPMB[2:0] = $000_B$ (Core voltage at 1.2V) | +25°C | 0.015 | 0.06 | mA | MB96F395 |
| | | | +125°C | 0.4 | 1.2 | | |
| Power supply current for active Low Voltage detector | $I_{CCLVD}$ | Low voltage detector enabled (RCR:LVDE = 1) | +25°C | 90 | 140 | µA | This current must be added to all Power supply currents above |
| | | | +125°C | 100 | 150 | | |
| Power supply current for active Clock modulator | $I_{CCCLOMO}$ | Clock modulator enabled (CMCR:PDX = 1) | - | 3 | 4.5 | mA | Must be added to all current above |
| Flash Write/Erase current | $I_{CCFLASH}$ | Current for one Flash module | - | 15 | 40 | mA | Must be added to all current above |
| Input capacitance | $C_{IN}$ | - | | 15 | 30 | pF | High current outputs |
| Input capacitance | $C_{IN}$ | - | - | 5 | 15 | pF | Other than C, $AV_{CC}$, $AV_{SS}$, AVRH, AVRL, $V_{CC}$, $V_{SS}$, $DV_{CC}$, $DV_{SS}$, High current outputs |

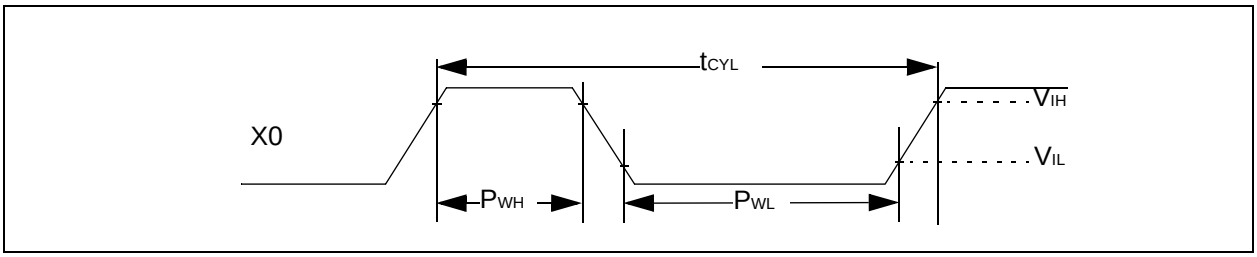
* The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.

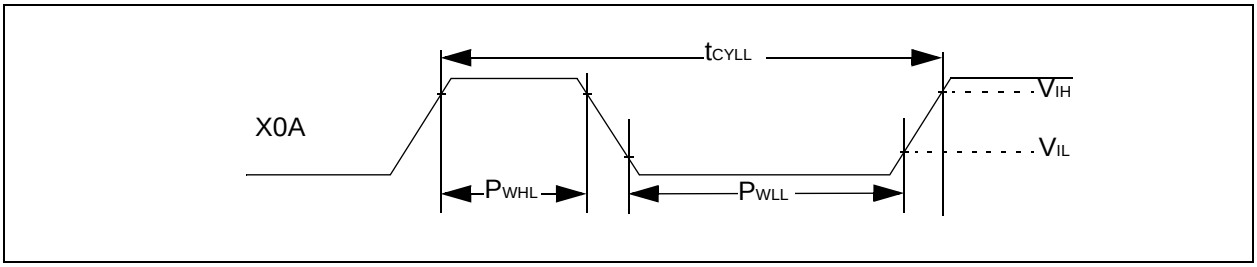
## 4. AC Characteristics

### Source Clock timing

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0, X1 | 3 | - | 16 | MHz | When using a crystal oscillator, PLL off |
| | | | 0 | - | 16 | MHz | When using an opposite phase external clock, PLL off |
| | | | 3.5 | - | 16 | MHz | When using a crystal oscillator or opposite phase external clock, PLL on |
| Clock frequency | $f_{FCI}$ | X0 | 0 | - | 56 | MHz | When using a single phase external clock in “Fast Clock Input mode” , PLL off |
| | | | 3.5 | - | 56 | MHz | When using a single phase external clock in “Fast Clock Input mode” , PLL on |
| Clock frequency | $f_{CL}$ | X0A, X1A | 32 | 32.768 | 100 | kHz | When using an oscillation circuit |
| | | | 0 | - | 100 | kHz | When using an opposite phase external clock |
| | | X0A | 0 | - | 50 | kHz | When using a single phase external clock |
| Clock frequency | $f_{CR}$ | - | 50 | 100 | 200 | kHz | When using slow frequency of RC oscillator |
| | | | 1 | 2 | 4 | MHz | When using fast frequency of RC oscillator |
| PLL Clock frequency | $f_{CLKVCO}$ | - | 64 | - | 200 | MHz | Permitted VCO output frequency of PLL (CLKVCO) |
| PLL Phase Jitter | $T_{PSKEW}$ | - | - | - | ± 5 | ns | For CLKMC (PLL input clock) ≥ 4MHz |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0,X1 | 8 | - | - | ns | Duty ratio is about 30% to 70% |
| Input clock pulse width | $P_{WHL}$, $P_{WLL}$ | X0A,X1A | 5 | - | - | µs | |


tCYL
X0
VIH
VIL
PWH
PWL


tCYLL
X0A
VIH
VIL
PWHL
PWLL

## Internal Clock timing

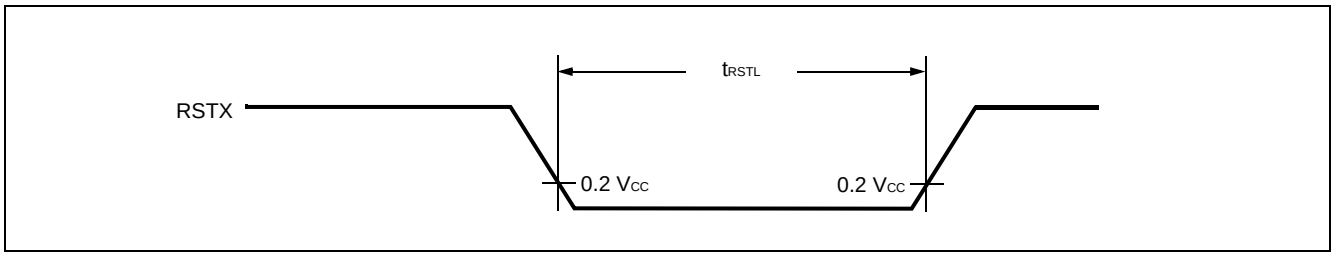
($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Core Voltage Settings | | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | 1.8V | | 1.9V | | | |
| | | Min | Max | Min | Max | | |
| Internal System clock frequency (CLKS1 and CLKS2) | $f_{CLKS1}$, $f_{CLKS2}$ | 0 | 92 | 0 | 96 | MHz | Others than below |
| | | 0 | 72 | 0 | 80 | MHz | MB96F395 |
| Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1) | $f_{CLKB}$, $f_{CLKP1}$ | 0 | 52 | 0 | 56 | MHz | Others than below |
| | | 0 | 36 | 0 | 40 | MHz | MB96F395 |
| Internal peripheral clock frequency (CLKP2) | $f_{CLKP2}$ | 0 | 28 | 0 | 32 | MHz | |

## External Reset timing

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

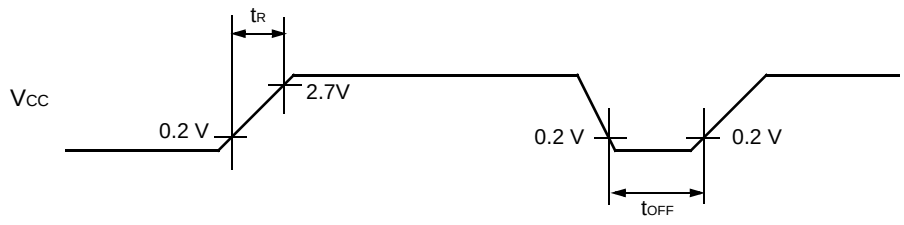
| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Reset input time | $t_{RSTL}$ | RSTX | 500 | - | - | ns | |



## Power On Reset timing

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Power on rise time | $t_R$ | Vcc | 0.05 | - | 30 | ms | |
| Power off time | $t_{OFF}$ | Vcc | 1 | - | - | ms | |



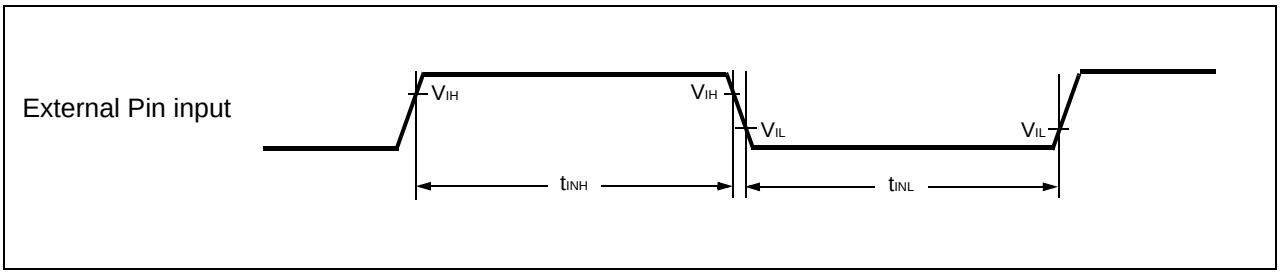

If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

## External Input timing

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Used Pin input function |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{INH}$ $t_{INL}$ | INTn(_R) | — | 200 | — | ns | External Interrupt |
| | | NMI(_R) | | | | | NMI |
| | | Pnn_m | | $2*t_{CLKP1}$ + 200 ($t_{CLKP1}$=1/ $f_{CLKP1}$) | — | ns | General Purpose IO |
| | | TINn(_R) | | | | | Reload Timer |
| | | TTGn(_R) | | | | | PPG Trigger input |
| | | ADTG(_R) | | | | | AD Converter Trigger |
| | | FRCKn(_R) | | | | | Free Running Timer external clock |
| | | INn(_R) | | | | | Input Capture |

Note : Relocated Resource Inputs have same characteristics



## Slew Rate High Current Outputs

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Output rise/fall time | $t_{R30}$<br>$t_{F30}$ | I/O circuit type M | Output driving strength set to “30mA” | 15 | — | ns | |

Note : Relocated Resource Inputs have same characteristics

- Slew rate output timing


$V_H = V_{OL30} + 0.9 \times (V_{OH30} - V_{OL30})$
$V_L = V_{OL30} + 0.1 \times (V_{OH30} - V_{OL30})$

## USART timing

WARNING: The values given below are for an I/O driving strength $IO_{drive}$ = 5mA. If $IO_{drive}$ is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

($T_A$ = -40°C to 125°C, $V_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

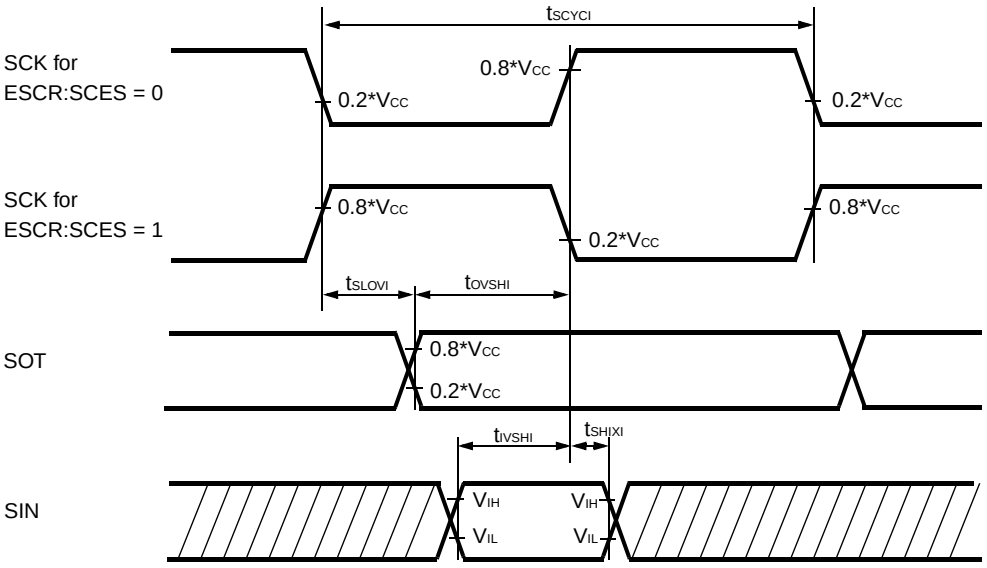
| Parameter | Symbol | Pin | Condition | $V_{CC}$ = $AV_{CC}$= 4.5V to 5.5V | | $V_{CC}$ = $AV_{CC}$= 3.0V to 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYCI}$ | SCKn | Internal Shift Clock Mode | 4 $t_{CLKP1}$ | — | 4 $t_{CLKP1}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCKn, SOTn | | -20 | +20 | -30 | +30 | ns |
| SOT → SCK ↑ delay time | $t_{OVSHI}$ | SCKn, SOTn | | N*$t_{CLKP1}$ - 20 *1 | — | N*$t_{CLKP1}$ - 30 *1 | — | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCKn, SINn | | $t_{CLKP1}$ + 45 | — | $t_{CLKP1}$ + 55 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCKn, SINn | | 0 | — | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SLSHE}$ | SCKn | External Shift Clock Mode | $t_{CLKP1}$ + 10 | — | $t_{CLKP1}$ + 10 | — | ns |
| Serial clock “H” pulse width | $t_{SHSLE}$ | SCKn | | $t_{CLKP1}$ + 10 | — | $t_{CLKP1}$ + 10 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCKn, SOTn | | — | 2 $t_{CLKP1}$ + 45 | — | 2 $t_{CLKP1}$ + 55 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCKn, SINn | | $t_{CLKP1}$/2 + 10 | — | $t_{CLKP1}$/2 + 10 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | SCKn, SINn | | $t_{CLKP1}$ + 10 | — | $t_{CLKP1}$ + 10 | — | ns |
| SCK fall time | $t_{FE}$ | SCKn | | — | 20 | — | 20 | ns |
| SCK rise time | $t_{RE}$ | SCKn | | — | 20 | — | 20 | ns |

Notes:
- AC characteristic in CLK synchronized mode.
- $C_L$ is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”
- $t_{CLKP1}$ is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

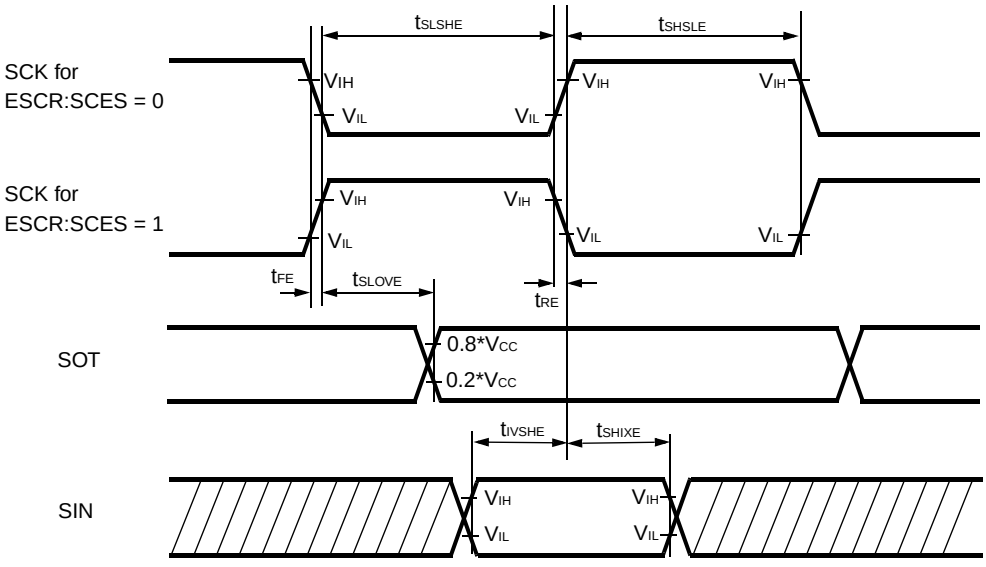
*1: Parameter N depends on $t_{SCYCI}$ and can be calculated as follows:
- if $t_{SCYCI}$ = 2*k*$t_{CLKP1}$, then N = k, where k is an integer > 2
- if $t_{SCYCI}$ = (2*k+1)*$t_{CLKP1}$, then N = k+1, where k is an integer > 1

Examples:

| $t_{SCYCI}$ | N |
|---|---|
| 4*$t_{CLKP1}$ | 2 |
| 5*$t_{CLKP1}$, 6*$t_{CLKP1}$ | 3 |
| 7*$t_{CLKP1}$, 8*$t_{CLKP1}$ | 4 |
| ... | ... |




**Internal Shift Clock Mode**




**External Shift Clock Mode**

## I²C Timing

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

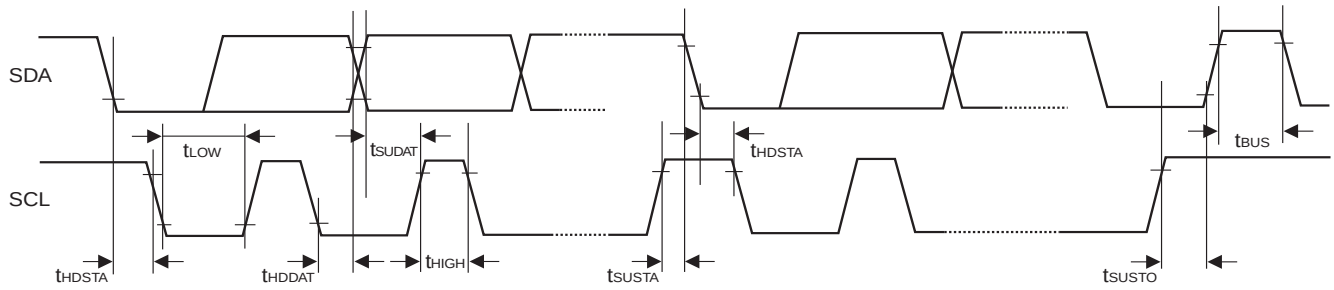
| Parameter | Symbol | Condition | Standard-mode | | Fast-mode*4 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| Hold time (repeated) START condition SDA↓→SCL↓ | $t_{HDSTA}$ | | 4.0 | — | 0.6 | — | µs |
| "L" width of the SCL clock | $t_{LOW}$ | | 4.7 | — | 1.3 | — | µs |
| "H" width of the SCL clock | $t_{HIGH}$ | | 4.0 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition SCL↑→SDA↓ | $t_{SUSTA}$ | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL↓→SDA↓↑ | $t_{HDDAT}$ | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data set-up time SDA↓↑→SCL↑ | $t_{SUDAT}$ | | 250 | — | 100 | — | ns |
| Set-up time for STOP condition SCL↑→SDA↑ | $t_{SUSTO}$ | | 4.0 | — | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{BUS}$ | | 4.7 | — | 1.3 | — | µs |

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HDDAT}$ have only to be met if the device does not stretch the "L" width ($t_{LOW}$) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



## 5. Analog Digital Converter

($T_A$ = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 10 | bit | |
| Total error | - | - | -3 | - | +3 | LSB | |
| Nonlinearity error | - | - | -2.5 | - | +2.5 | LSB | |
| Differential nonlinearity error | - | - | -1.9 | - | +1.9 | LSB | |
| Zero reading voltage | $V_{OT}$ | ANn | AVRL - 1.5 LSB | AVRL+ 0.5 LSB | AVRL + 2.5 LSB | V | |
| Full scale reading voltage | $V_{FST}$ | ANn | AVRH - 3.5 LSB | AVRH - 1.5 LSB | AVRH + 0.5 LSB | V | |
| Compare time | - | - | 1.0 | - | 16,500 | µs | 4.5V ≤ $AV_{CC}$ ≤ 5.5V |
| | | | 2.0 | - | - | µs | 3.0V ≤ $AV_{CC}$ < 4.5V |
| Sampling time | - | - | 0.5 | - | - | µs | 4.5V ≤ $AV_{CC}$ ≤ 5.5V |
| | | | 1.2 | - | - | µs | 3.0V ≤ $AV_{CC}$ < 4.5V |
| Analog port input current | $I_{AIN}$ | ANn | -3 | - | +3 | µA | $AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH |
| Analog port input current | $I_{AIN}$ | ANn | -1 | - | +1 | µA | $T_A$ = 25 °C, $AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH |
| | | | -3 | - | +3 | µA | $T_A$ = 125 °C, $AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH |
| Analog input voltage range | $V_{AIN}$ | ANn | AVRL | - | AVRH | V | |
| Reference voltage range | AVRH | AVRH | 0.75 AVcc | - | AVcc | V | |
| | AVRL | AVRL | $AV_{SS}$ | - | 0.25 $AV_{CC}$ | V | |
| Power supply current | $I_A$ | AVcc | - | 2.5 | 5 | mA | A/D Converter active |
| | $I_{AH}$ | AVcc | - | - | 5 | µA | A/D Converter not operated |
| Reference voltage current | $I_R$ | AVRH/ AVRL | - | 0.7 | 1 | mA | A/D Converter active |
| | $I_{RH}$ | AVRH/ AVRL | - | - | 5 | µA | A/D Converter not operated |
| Offset between input channels | - | ANn | - | - | 4 | LSB | |

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

## Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

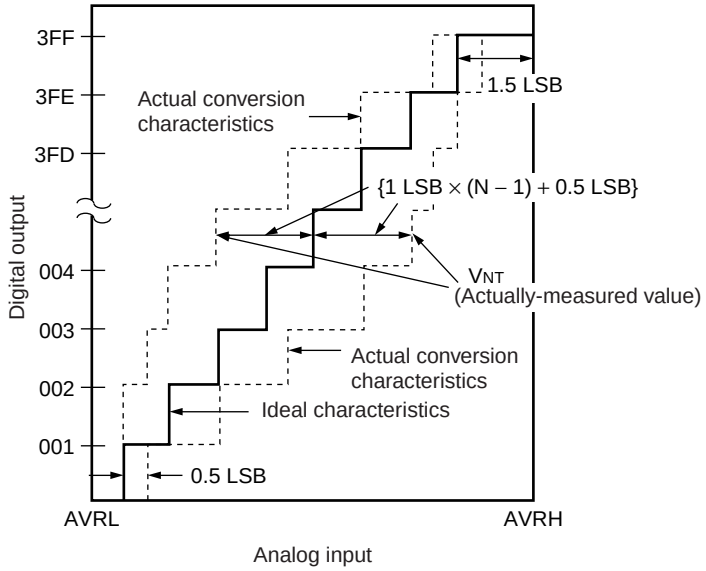
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error




$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

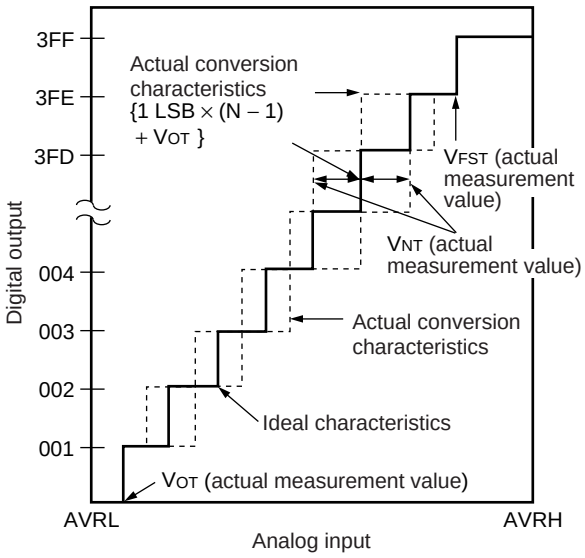
N: A/D converter digital output value

$V_{OT}$ (Ideal value) = AVRL + 0.5 LSB [V]

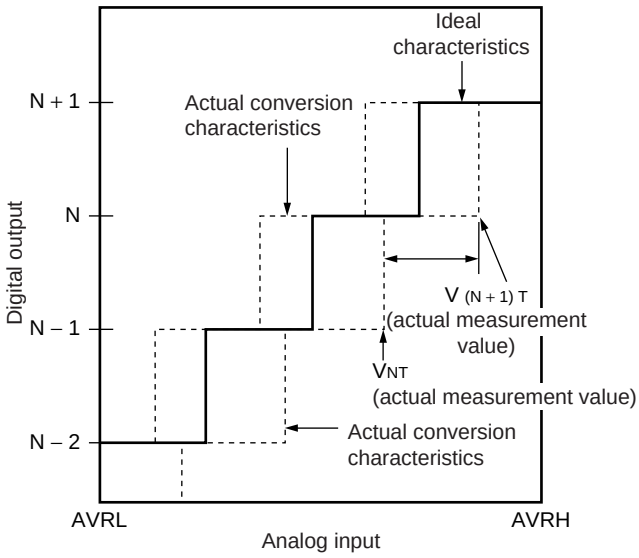
$V_{FST}$ (Ideal value) = AVRH – 1.5 LSB [V]

$V_{NT}$ : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error




Differential nonlinearity error




$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times\ (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)\,T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

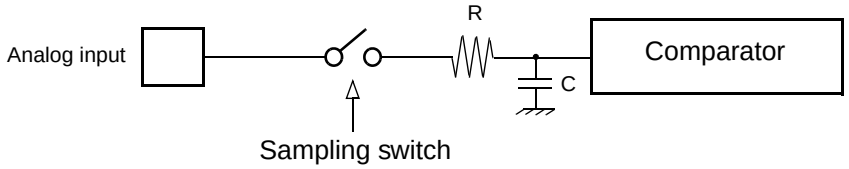
N : A/D converter digital output value
$V_{OT}$ : Voltage at which digital output transits from “$000_H$” to “$001_H$.”
$V_{FST}$ : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

**Notes on A/D Converter Section**

- About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- analog input circuit model:




**Reference value:**

- C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time ($T_{samp}$) is longer than the minimum value. Usually, this value is set to $7\tau$, where $\tau = RC$. If the external input resistance ($R_{ext}$) connected to the analog input is included, the sampling time is expressed as follows:

$T_{samp}$ [min] = $7 \times (R_{ext} + 2.6k\Omega) \times C$ for $4.5 \leq AV_{cc} \leq 5.5$

$T_{samp}$ [min] = $7 \times (R_{ext} + 12.1k\Omega) \times C$ for $3.0 \leq AV_{cc} \leq 4.5$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

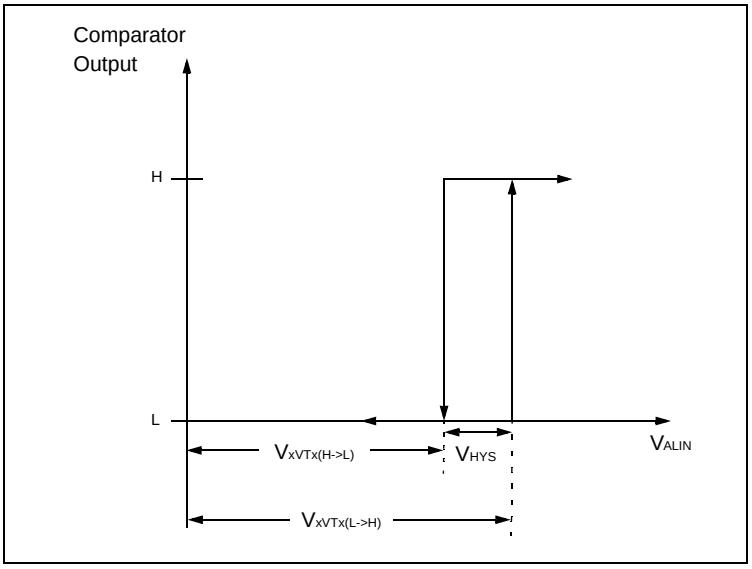
- About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

## 6. Alarm Comparator

($T_A$ = -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 3.0V - 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Power supply current | $I_{A5ALMF}$ | $AV_{CC}$ | - | 25 | 45 | µA | Alarm comparator enabled in fast mode (one channel) |
| | $I_{A5ALMS}$ | | - | 7 | 13 | µA | Alarm comparator enabled in slow mode (one channel) |
| | $I_{A5ALMH}$ | | - | - | 5 | µA | Alarm comparator disabled |
| ALARM pin input current | $I_{ALIN}$ | ALARM0, ALARM1 | -1 | - | +1 | µA | $T_A$ = 25 °C |
| | | | -3 | - | +3 | µA | $T_A$ = 125 °C |
| ALARM pin input voltage range | $V_{ALIN}$ | | 0 | - | $AV_{CC}$ | V | |
| External low threshold high->low transition | $V_{EVTL(H->L)}$ | | 0.36 * $AV_{CC}$ -0.25 | 0.36 * $AV_{CC}$ -0.1 | - | V | INTREF = 0 |
| External low threshold low->high transition | $V_{EVTL(L->H)}$ | | - | 0.36 * $AV_{CC}$ +0.1 | 0.36 * $AV_{CC}$ +0.25 | V | |
| External high threshold high->low transition | $V_{EVTH(H->L)}$ | | 0.78 * $AV_{CC}$ -0.25 | 0.78 * $AV_{CC}$ -0.1 | - | V | |
| External high threshold low->high transition | $V_{EVTH(L->H)}$ | | | 0.78 * $AV_{CC}$ +0.1 | 0.78 * $AV_{CC}$ +0.25 | V | |
| Internal low threshold high->low transition | $V_{IVTL(H->L)}$ | | 0.9 | 1.1 | - | V | INTREF = 1 |
| Internal low threshold low->high transition | $V_{IVTL(L->H)}$ | | - | 1.3 | 1.55 | V | |
| Internal high threshold high->low transition | $V_{IVTH(H->L)}$ | | 2.2 | 2.4 | - | V | |
| Internal high threshold low->high transition | $V_{IVTH(L->H)}$ | | - | 2.6 | 2.85 | V | |
| Switching hysteresis | $V_{HYS}$ | | 50 | - | 300 | mV | |
| Comparison time | $t_{COMPF}$ | | - | 0.1 | 1 | µs | CMD = 1 (fast) |
| | $t_{COMPS}$ | | - | 1 | 10 | µs | CMD = 0 (slow) |
| Power-up stabilization time after enabling alarm comparator | $t_{PD}$ | | - | 1 | 5 | ms | Threshold levels specified above are not guaranteed within this time |
| Slow/Fast mode transition time | $t_{CMD}$ | | - | 100 | 500 | µs | |


Comparator
Output
H
L
VxVTx(H->L)
VHYS
VALIN
VxVTx(L->H)

## 7. Low Voltage Detector characteristics

($T_A$ = -40 °C to +125 °C, $V_{cc}$ = $AV_{cc}$ = 3.0V - 5.5V, $V_{ss}$ = $AV_{ss}$ = 0V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Stabilization time | $T_{LVDSTAB}$ | - | 75 | µs | After power-up or change of detection level |
| Level 0 | $V_{DL0}$ | 2.7 | 2.9 | V | CILCR:LVL[3:0]="0000" |
| Level 1 | $V_{DL1}$ | 2.9 | 3.1 | V | CILCR:LVL[3:0]="0001" |
| Level 2 | $V_{DL2}$ | 3.1 | 3.3 | V | CILCR:LVL[3:0]="0010" |
| Level 3 | $V_{DL3}$ | 3.5 | 3.75 | V | CILCR:LVL[3:0]="0011" |
| Level 4 | $V_{DL4}$ | 3.6 | 3.85 | V | CILCR:LVL[3:0]="0100" |
| Level 5 | $V_{DL5}$ | 3.7 | 3.95 | V | CILCR:LVL[3:0]="0101" |
| Level 6 | $V_{DL6}$ | 3.8 | 4.05 | V | CILCR:LVL[3:0]="0110" |
| Level 7 | $V_{DL7}$ | 3.9 | 4.15 | V | CILCR:LVL[3:0]="0111" |
| Level 8 | $V_{DL8}$ | 4.0 | 4.25 | V | CILCR:LVL[3:0]="1000" |
| Level 9 | $V_{DL9}$ | 4.1 | 4.35 | V | CILCR:LVL[3:0]="1001" |
| Level 10 | $V_{DL10}$ | not used | | | |
| Level 11 | $V_{DL11}$ | not used | | | |
| Level 12 | $V_{DL12}$ | not used | | | |
| Level 13 | $V_{DL13}$ | not used | | | |
| Level 14 | $V_{DL14}$ | not used | | | |
| Level 15 | $V_{DL15}$ | not used | | | |

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

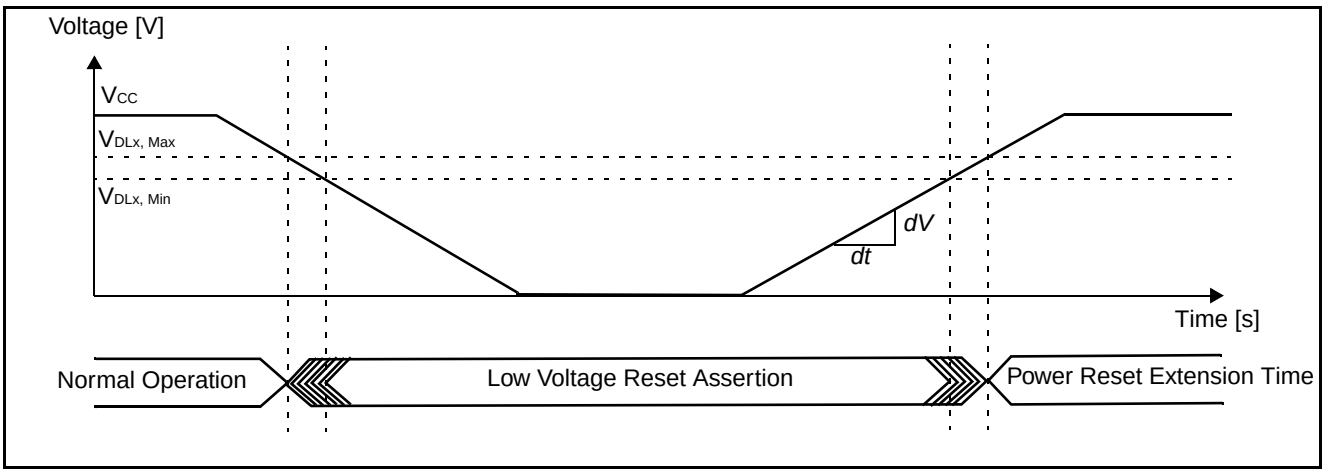
For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004 \frac{V}{\mu s}$ .

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

## Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



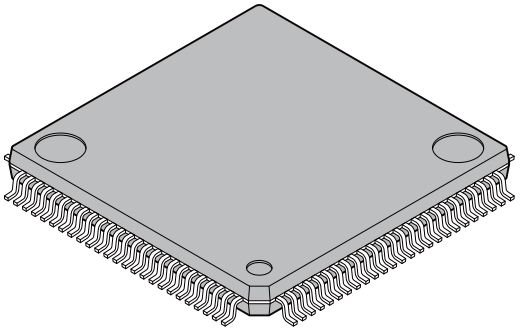
## 8. FLASH memory program/erase characteristics

($T_A$ = -40°C to 105°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $DV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V)

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 0.9 | 3.6 | s | Without erasure pre-programming time |
| Chip erase time | - | n*0.9 | n*3.6 | s | Without erasure pre-programming time (n is the number of Flash sector of the device) |
| Word (16-bit width) programming time | - | 23 | 370 | us | Without overhead time for submitting write command |
| Program/Erase cycle | 10 000 | - | - | cycle | |
| Flash data retention time | 20 | - | - | year | *1 |

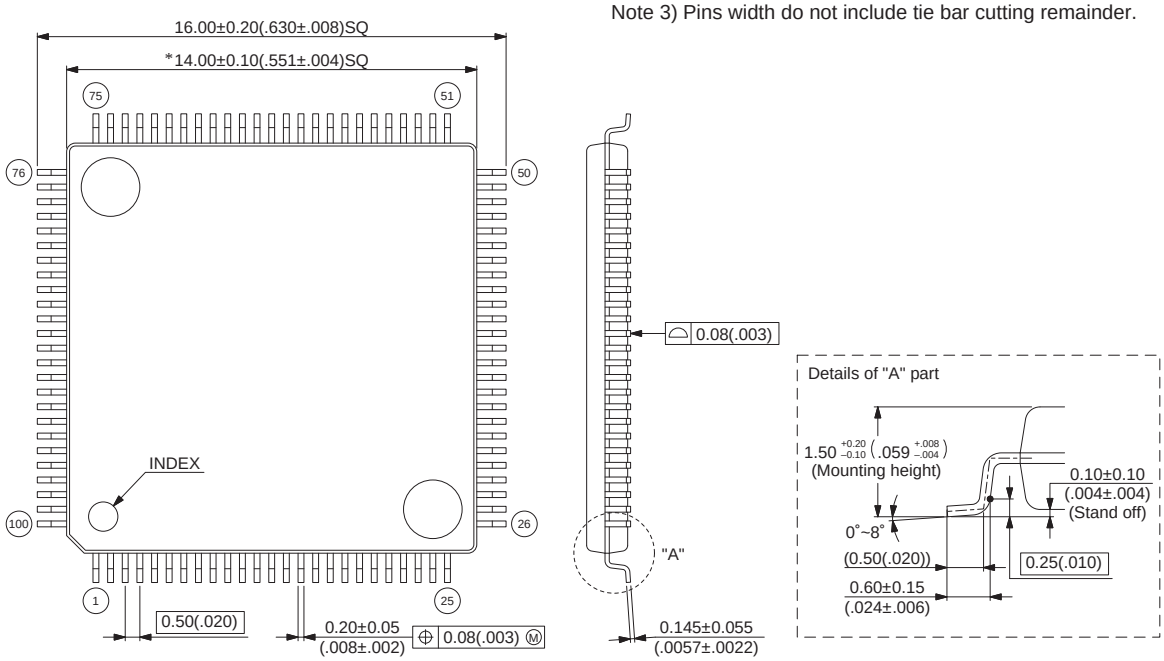
*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

## ■ PACKAGE DIMENSION MB96F39x LQFP 100P

| 100-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 14.0 mm × 14.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm Max |
| | Weight | 0.65 g |
| (FPT-100P-M20) | Code (Reference) | P-LFQFP100-14×14-0.50 |

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values

## ■ ORDERING INFORMATION

| Part number | Flash/ROM | Subclock | Persistent Low Voltage Reset | Package |
|---|---|---|---|---|
| MB96F395YSA PMC-GSE2 *1 | Flash A (160KB) | No | Yes | 100 pin Plastic LQFP (FPT-100P-M20) |
| MB96F395RSA PMC-GSE2 *1 | | | No | |
| MB96F395YWA PMC-GSE2 *1 | | Yes | Yes | |
| MB96F395RWA PMC-GSE2 *1 | | | No | |
| MB96V300BRB-ES (for evaluation) | Emulated by ext. RAM | Yes | No | 416 pin Plastic BGA (BGA-416P-M02) |

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

## ■ REVISION HISTORY

| Revision | Date | Modification |
|---|---|---|
| Prelim 1 | 2008-04-18 | Initial Draft |
| Prelim 2 | 2009-01-09 | • Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added)<br>• specified AD converter channel offset to 4LSB<br>• package code of MB96V300 corrected in ordering information<br>• Internal LCD divider resistance value corrected: Typ 35kOhm -> 40kOhm, Max 50kOhm -> 65kOhm<br>• Added voltage condition to pull-up resistance and LCD divide resistance spec<br>• Ordering information: column “Flash/ROM” added, column “Remarks” removed<br>• Official package dimension drawing with additional notes added<br>• Empty pages removed<br>• Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added<br>• Handling devices: Notes added about Serial communication and about using ceramic resonators.<br>• Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor<br>• AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz<br>• VOL3 spec improved: spec valid for 3mA load for full Vcc range<br>• All ICC (Run/Sleep/Timer/Stop mode) currents adjusted to evaluation results<br>• IO map cleaned up (removed not available resources)<br>• Absolute maximum ratings: Pd spec corrected<br>• C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted |

## ■ MAIN CHANGES IN THIS EDITION

| Page | Section | Change Results |
|---|---|---|
| 73 | ■ ELECTRICAL CHARACTERISTICS<br>5. Analog Digital Converter | Corrected “Value” and “Unit” of Zero reading voltage.<br>(AVRL - 1.5 → AVRL - 1.5 LSB<br>AVRL + 0.5 → AVRL + 0.5 LSB<br>AVRL + 2.5 → AVRL + 2.5 LSB<br>LSB → V)<br>Corrected “Value” and “Unit” of Full scale reading voltage.<br>(AVRH - 3.5 → AVRH - 3.5 LSB<br>AVRH - 1.5 → AVRH - 1.5 LSB<br>AVRH + 0.5 → AVRH + 0.5 LSB<br>LSB → V) |

The vertical lines marked in the left side of the page show the changes.

# MEMO

# MEMO

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