Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

S27KL0643/S27KS0643

3.0 V/1.8 V, 64 Mb (8 MB) HyperRAM Self-Refresh DRAM

Features

Interface

- xSPI (Octal) Interface
- 1.8 V / 3.0 V Interface support
  - Single ended clock (CK) - 11 bus signals
  - Optional Differential clock (CK, CK#) - 12 bus signals
- Chip Select (CS#)
- 8-bit data bus (DQ[7:0])
- Hardware reset (RESET#)
- Bidirectional Read-Write Data Strobe (RWDS)
  - Output at the start of all transactions to indicate refresh latency
  - Output during read transactions as Read Data Strobe
  - Input during write transactions as Write Data Mask
- Optional DDR Center-Aligned Read Strobe (DCARS)
  - During read transactions RWDS is offset by a second clock, phase shifted from CK
  - The Phase Shifted Clock is used to move the RWDS transition edge within the read data eye

Performance, Power, and Packages

- 200 MHz maximum clock rate
- DDR - transfers data on both edges of the clock
- Data throughput up to 400 MBps (3,200 Mbps)
- Configurable Burst Characteristics
  - Linear burst
  - Wrapped burst lengths:
    - 16 bytes (8 clocks)
    - 32 bytes (16 clocks)
    - 64 bytes (32 clocks)
    - 128 bytes (64 clocks)
  - Hybrid option - one wrapped burst followed by linear burst
- Configurable output drive strength
- Power Modes
  - Hybrid Sleep Mode
  - Deep Power Down
- Array Refresh
  - Partial Memory Array (1/8, 1/4, 1/2, and so on)
  - Full
- Package
  - 24-ball FBGA
- Operating Temperature Range
  - Industrial (I): –40 °C to +85 °C
  - Industrial Plus (V): –40 °C to +105 °C
  - Automotive, AEC-Q100 Grade 3: –40 °C to +85 °C
  - Automotive, AEC-Q100 Grade 2: –40 °C to +105°C

Technology

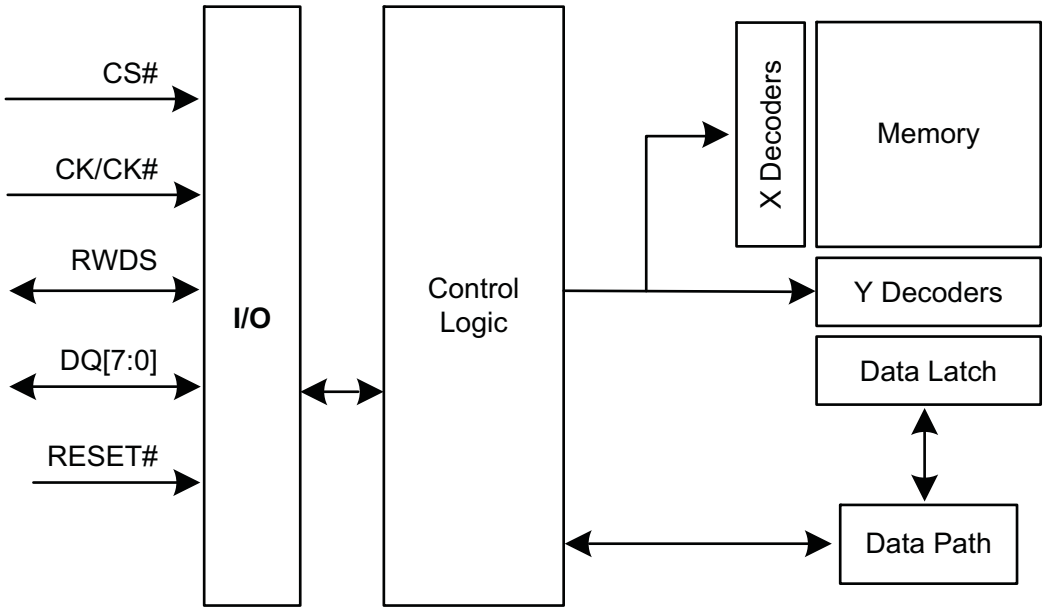
- 38 nm DRAM

Performance Summary

Read Transaction Timings	Unit
Maximum Clock Rate at 1.8 V $V_{CC}/V_{CC}Q$	200 MHz
Maximum Clock Rate at 3.0 V $V_{CC}/V_{CC}Q$	200 MHz
Maximum Access Time, (t_{ACC})	35 ns

Maximum Current Consumption	Unit
Burst Read or Write (linear burst at 200 MHz, 1.8 V)	25 mA
Burst Read or Write (linear burst at 200 MHz, 3.0 V)	30 mA
Standby (CS# = V_{CC} = 3.6 V, 105 °C)	360 µA
Deep Power Down (CS# = V_{CC} = 3.6 V, 105 °C)	15 µA
Standby (CS# = V_{CC} = 2.0 V, 105 °C)	330 µA
Deep Power Down (CS# = V_{CC} = 2.0 V, 105 °C)	12 µA

Logic Block Diagram



Contents

General Description

The Cypress 64 Mb HyperRAM device is a high-speed CMOS, self-refresh DRAM, with xSPI (Octal) interface. The DRAM array uses dynamic cells that require periodic refresh. Refresh control logic within the device manages the refresh operations on the DRAM array when the memory is not being actively read or written by the xSPI interface master (host). Since the host is not required to manage any refresh operations, the DRAM array appears to the host as though the memory uses static cells that retain data without refresh. Hence, the memory is more accurately described as Pseudo Static RAM (PSRAM).

Since the DRAM cells cannot be refreshed during a read or write transaction, there is a requirement that the host limit read or write burst transfers lengths to allow internal logic refresh operations when they are needed. The host must confine the duration of transactions and allow additional initial access latency, at the beginning of a new transaction, if the memory indicates a refresh operation is needed.

xSPI (Octal) Interface

xSPI (Octal) is a SPI-compatible low signal count, DDR interface supporting eight I/Os. The DDR protocol in xSPI (Octal) transfers two data bytes per clock cycle on the DQ input/output signals. A read or write transaction on xSPI (Octal) consists of a series of 16-bit wide, one clock cycle data transfers at the internal RAM array with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible. Device are available as 1.8 V $V_{CC}/V_{CC}Q$ or 3.0 V $V_{CC}/V_{CC}Q$ (nominal) for array (V_{CC}) and I/O buffer ($V_{CC}Q$) supplies, through different Ordering Part Number (OPN).

Each transaction on xSPI (Octal) must include a command whereas address and data are optional. The transactions are structures as follows:

- Each transaction begins with CS# going LOW and ends with CS# returning HIGH.
- The serial clock (CK) marks the transfer of each bit or group of bits between the host and memory. All transfers occur on every CK edge (DDR mode).
- Each transaction has a 16-bit command which selects the type of device operation to perform. The 16-bit command is based on two 8-bit opcodes. The same 8-bit opcode is sent on both edges of the clock.
- A command may be stand-alone or may be followed by address bits to select a memory location in the device to access data.
- Read transactions require a latency period after the address bits and can be zero to several CK cycles. CK must continue to toggle during any read transaction latency period. During the command and address parts of a transaction, the memory can indicate whether an additional latency period is needed for a required refresh time (t_{RFH}) which is added to the initial latency period; by driving the RWDS signal to the HIGH state.
- Write transactions to registers do not require a latency period.
- Write transactions to the memory array require a latency period after the address bits and can be zero to several CK cycles. CK must continue to toggle during any write transaction latency period. During the command and address parts of a transaction, the memory can indicate whether an additional latency period is needed for a required refresh time (t_{RFH}) which is added to the initial latency period by driving the RWDS signal to the HIGH state.
- In all transactions, command and address bits are shifted in the device with the most significant bits (MSb) first. The individual data bits within a data byte are shifted in and out of the device MSb first as well. All data bytes are transferred with the lowest address byte sent out first.

Figure 1. xSPI (Octal) Command only Transaction (DDR)

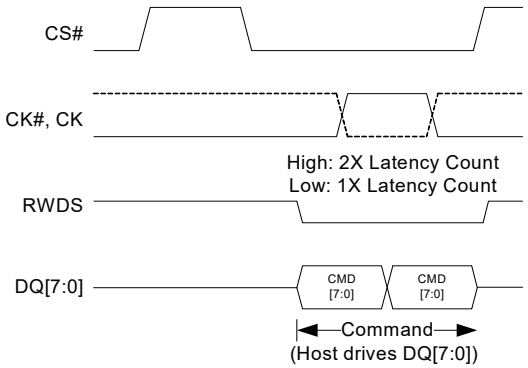


Figure 2. xSPI (Octal) Write with No Latency Transaction (DDR) (Register Writes)[1]

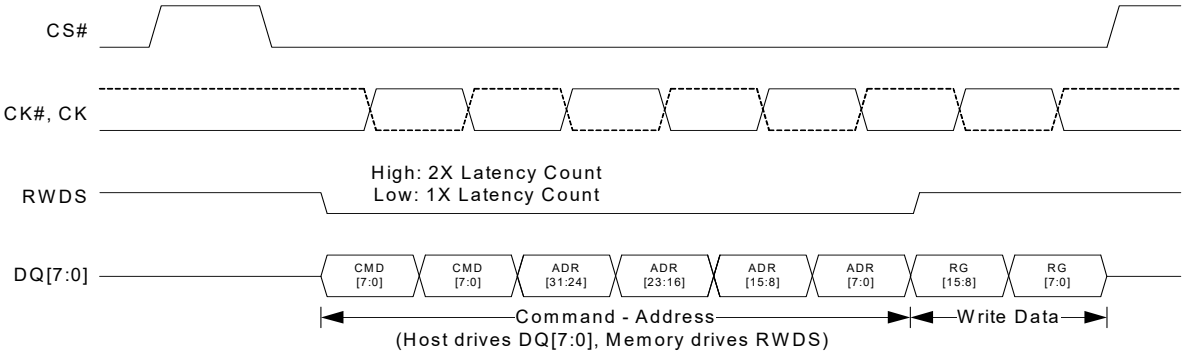
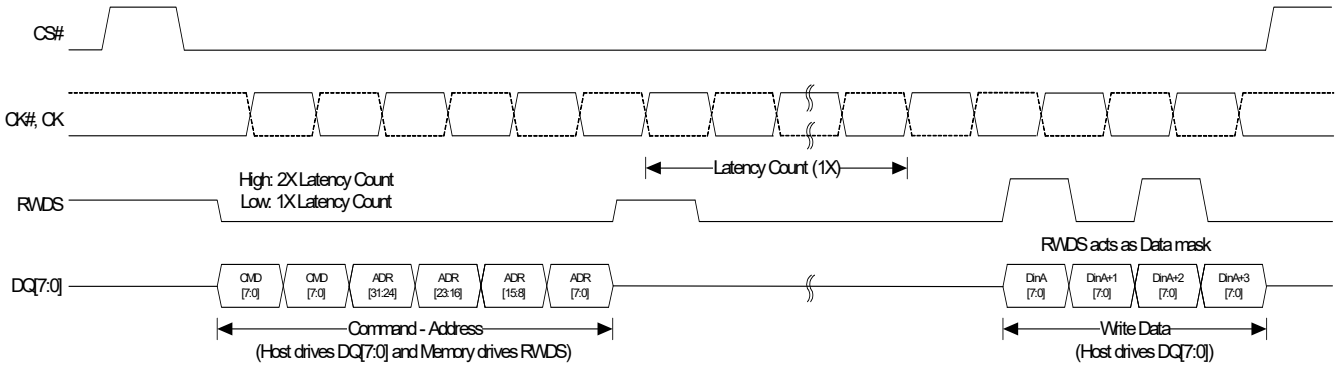


Figure 3. xSPI (Octal) Write with 1X Latency Transaction (DDR) (Memory Array Writes)[2, 3]



Notes
1. Write with no latency transaction is used for register writes only.
2. RWDS driven by the host.
3. Data DinA and DinA+2 are masked.

Figure 4. xSPI (Octal) Write with 2X Latency Transaction (DDR) (Memory Array Writes)[4, 5]

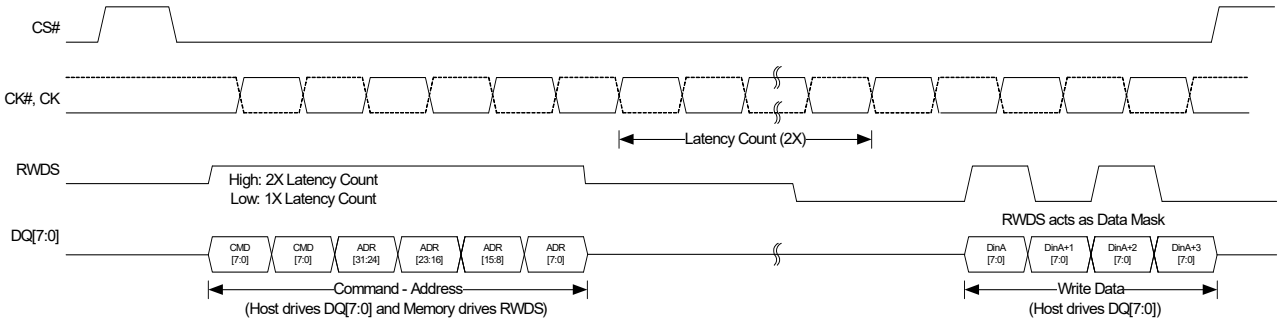


Figure 5. xSPI (Octal) Read with 1X Latency Transaction (DDR) (All Reads)[6]

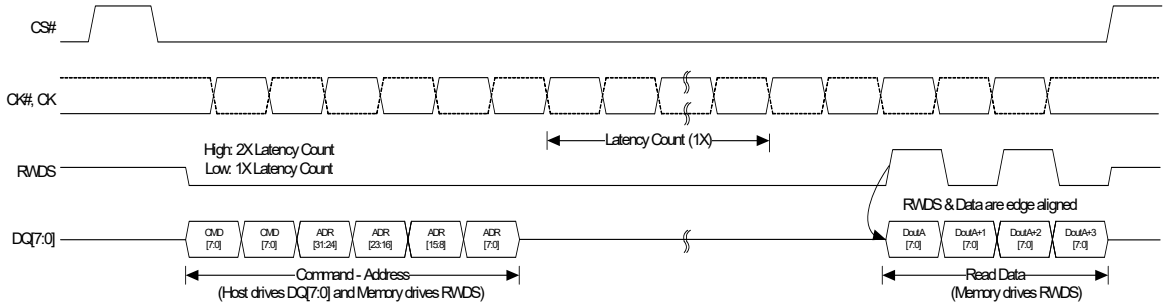
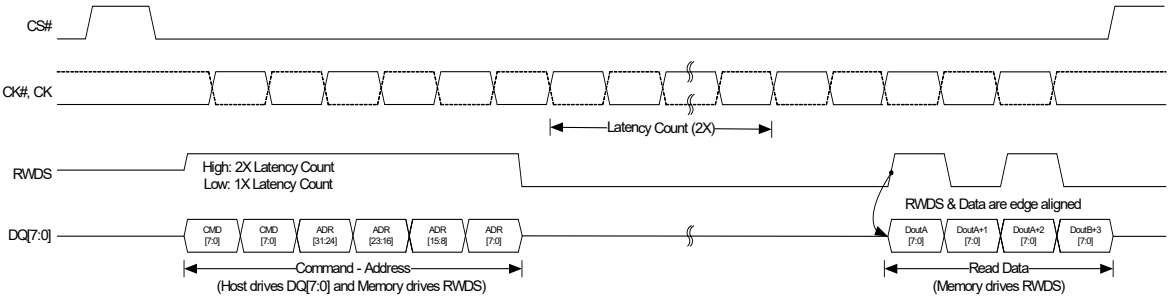


Figure 6. xSPI (Octal) Read with 2X Latency Transaction (DDR) (All Reads)[7]

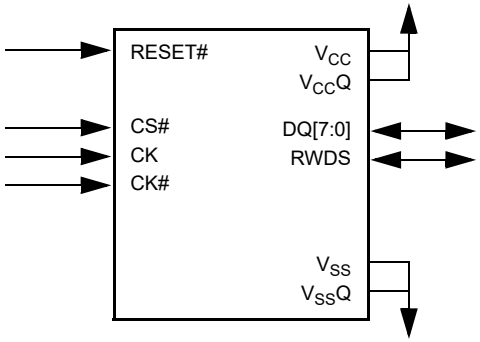


Notes
4. RWDS driven by HyperRAM during Command & Address cycles for 2X latency and then driven by the host for data masking.
5. Data DinA and DinA+2 are masked.
6. RWDS is driven by HyperRAM phase aligned with data.
7. RWDS is driven by HyperRAM during Command & Address cycles for 2X latency and then driven again phase aligned with data.

Product Overview

The 64 Mb HyperRAM device is 1.8 V or 3.0 V array and I/O, synchronous self-refresh Dynamic RAM (DRAM). The HyperRAM device provides an xSPI (Octal) slave interface to the host system. The xSPI (Octal) interface has an 8-bit (1 byte) wide DDR data bus and use only word-wide (16-bit data) address boundaries. Read transactions provide 16 bits of data during each clock cycle (8 bits on both clock edges). Write transactions take 16 bits of data from each clock cycle (8 bits on each clock edge).

Figure 7. xSPI (Octal) HyperRAM Interface[8]



xSPI (Octal) Interface

Read and write transactions require three clock cycles to define the target row/column address and then an initial access latency of t_{ACC}. During the CA part of a transaction, the memory will indicate whether an additional latency for a required refresh time (t_{RFH}) is added to the initial latency; by driving the RWDS signal to the HIGH state. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped or linear sequence. When configured in linear burst mode, the device will automatically fetch the next sequential row from the memory array to support a continuous linear burst. Simultaneously accessing the next row in the array while the read or write data transfer is in progress, allows for a linear sequential burst operation that can provide a sustained data rate of 400 MBps *(1 byte (8 bit data bus) * 2 (data clock edges) * 200 MHz = 400 MBps)*.

Note
8. CK# is used in Differential Clock mode, but optional.

Signal Description

Input/Output Summary

The xSPI (Octal) HyperRAM signals are shown in Table 1. Active Low signal names have a hash symbol (#) suffix.

Table 1. I/O Summary[10]

Symbol	Type	Description
CS#	Master Output, Slave Input	**Chip Select.** Bus transactions are initiated with a HIGH to LOW transition. Bus transactions are terminated with a Low to High transition. The master device has a separate CS# for each slave.
CK, CK#[9]	Master Output, Slave Input	**Differential Clock**. Command, address, and data information is output with respect to the crossing of the CK and CK# signals. Use of differential clock is optional. **Single Ended Clock.** CK# is not used, only a single ended CK is used. The clock is not required to be free-running.
DQ[7:0]	Input/Output	**Data Input/Output.** Command, Address, and Data information is transferred on these signals during Read and Write transactions.
RWDS	Input/Output	**Read-Write Data Strobe.** During the Command/Address portion of all bus transactions RWDS is a slave output and indicates whether additional initial latency is required. Slave output during read data transfer, data is edge aligned with RWDS. Slave input during data transfer in write transactions to function as a data mask. (HIGH = additional latency, LOW = no additional latency).
RESET#	Master Output, Slave Input, Internal Pull-up	**Hardware RESET**. When LOW, the slave device will self initialize and return to the Standby state. RWDS and DQ[7:0] are placed into the HIGH-Z state when RESET# is LOW. The slave RESET# input includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the HIGH state.
V_{CC}	Power Supply	**Array Power.**
$V_{CC}Q$	Power Supply	**Input/Output Power.**
V_{SS}	Power Supply	**Array Ground.**
$V_{SS}Q$	Power Supply	**Input/Output Ground.**
RFU	No Connect	**Reserved for Future Use**. May or may not be connected internally, the signal/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The signal/ball may be used by a signal in the future.

Notes
9. CK# is used in Differential Clock mode, but optional connection. Tie the CK# input pin to either VccQ or VssQ if not connected to the host controller, but do not leave it floating.
10. Optional DCARS pinout and pin description are outlined in section DDR Center-Aligned Read Strobe (DCARS) Functionality on page 42.

xSPI (Octal) Transaction Details

The xSPI (Octal) master begins a transaction by driving CS# LOW while clock is idle. Then the clock begins toggling while CA words are transferred.

For memory Read and Write transactions, the xSPI (Octal) master then continues clocking for a number of cycles defined by the latency count setting in configuration register 0 (Register Write transactions do not require any latency count). The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is LOW during the CA cycles, one latency count is inserted. If RWDS is HIGH during the CA cycles, an additional latency count is inserted. Once these latency clocks have been completed the memory starts to simultaneously transition the RWDS and output the target data.

During the read data transfers, read data is output edge aligned with every transition of RWDS. Data will continue to be output as long as the host continues to transition the clock while CS# is LOW. Note that burst transactions should not be so long as to prevent the memory from doing distributed refreshes.

During the write data transfers, write data is center-aligned with the clock edges. The first byte of data in each word is captured by the memory on the rising edge of CK and the second byte is captured on the falling edge of CK. RWDS is driven by the host master interface as a data mask. When data is being written and RWDS is HIGH the byte will be masked and the array will not be altered. When data is being written and RWDS is LOW the data will be placed into the array. Because the master is driving RWDS during write data transfers, neither the master nor the HyperRAM device are able to indicate a need for latency within the data transfer portion of a write transaction. The acceptable write data burst length setting is also shown in configuration register 0.

Wrapped bursts will continue to wrap within the burst length and linear burst will output data in a sequential manner across row boundaries. When a linear burst read reaches the last address in the array, continuing the burst beyond the last address will provide data from the beginning of the address range. Read transfers can be ended at any time by bringing CS# HIGH when the clock is idle.

The clock is not required to be free-running. The clock may remain idle while CS# is HIGH.

Command/Address/Data Bit Assignments

Table 2. Command Set[11, 12, 13, 14, 15]

Command	Code	CA-Data	Address (Bytes)	Latency Cycles	Data (Bytes)	Prerequisite
Software Reset						
REST ENABLE	0x66	8-0-0	0	0	0	
RESET	0x99	8-0-0	0	0	0	RESET ENABLE
Identification						
READ ID[11]	0x9F	8-8-8	4 (0x00)	3-7	4	
Power Modes						
DEEP POWER DOWN	0xB9	8-0-0	0	0	0	
Read Memory Array						
READ (DDR)	0xEE	8-8-8	4	3-7	1 to ∞	
Write Memory Array						
WRITE (DDR)	0xDE	8-8-8	4	3-7	1 to ∞	WRITE ENABLE
Write Enable / Disable						
WRITE ENABLE	0x06	8-0-0	0	0	0	
WRITE DISABLE	0x04	8-0-0	0	0	0	
Read Registers						

Notes
11. The two identification registers contents are read together - identification 0 followed by identification 1.
12. Write Enable provides protection against inadvertent changes to memory or register values. It sets the internal write enable latch (WEL) which allows write transactions to execute afterwards.
13. Write Disable can be used to disable write transactions from execution. It resets the internal write enable latch (WEL).
14. The WEL latch stays set to '1' at the end of any successful memory write transaction. After a power down / power up sequence, or a hardware/software reset, WEL latch is cleared to '0'.
15. The internal WEL latch is cleared to '0' at the end of any successful register write transaction.

Table 2. Command Set[11, 12, 13, 14, 15] (Continued)

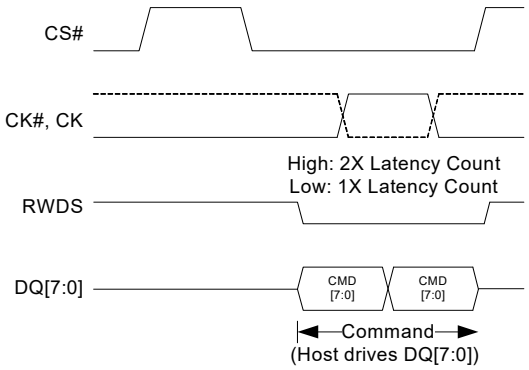
Command	Code	CA-Data	Address (Bytes)	Latency Cycles	Data (Bytes)	Prerequisite
READ ANY REGISTER	0x65	8-8-8	4	3-7	2	
Write Registers						
WRITE ANY REGISTER	0x71	8-8-8	4	0	2	WRITE ENABLE

Notes
11. The two identification registers contents are read together - identification 0 followed by identification 1.
12. Write Enable provides protection against inadvertent changes to memory or register values. It sets the internal write enable latch (WEL) which allows write transactions to execute afterwards.
13. Write Disable can be used to disable write transactions from execution. It resets the internal write enable latch (WEL).
14. The WEL latch stays set to '1' at the end of any successful memory write transaction. After a power down / power up sequence, or a hardware/software reset, WEL latch is cleared to '0'.
15. The internal WEL latch is cleared to '0' at the end of any successful register write transaction.

RESET ENABLE Transaction

The RESET ENABLE transaction is required immediately before a RESET transaction. Any transaction other than RESET following RESET ENABLE will clear the reset enable condition and prevent a later RESET transaction from being recognized.

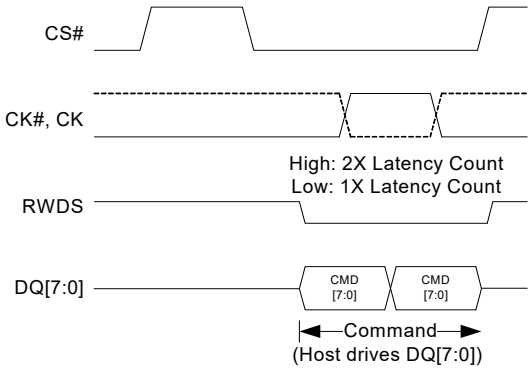
Figure 8. RESET ENABLE Transaction (DDR)



RESET Transaction

The RESET transaction immediately following a RESET ENABLE will initiate the software reset process.

Figure 9. RESET Transaction (DDR)



READ ID Transaction

The READ ID transaction provides read access to device identification registers 0 and 1. The registers contain the manufacturer's identification along with device identification. The read data sequence is as follows.

Table 3. READ ID Data Sequence

Address Space	Byte Order	Byte Position	Word Data Bit	DQ
Register 0	Big-endian	A	15	7
			14	6
			13	5
			12	4
			11	3
			10	2
			9	1
			8	0
		B	7	7
			6	6
			5	5
			4	4
			3	3
			2	2
			1	1
			0	0
Register 1	Big-endian	A	15	7
			14	6
			13	5
			12	4
			11	3
			10	2
			9	1
			8	0
		B	7	7
			6	6
			5	5
			4	4
			3	3
			2	2
			1	1
			0	0

Figure 10. READ ID with 1X Latency Transaction (DDR)[16]

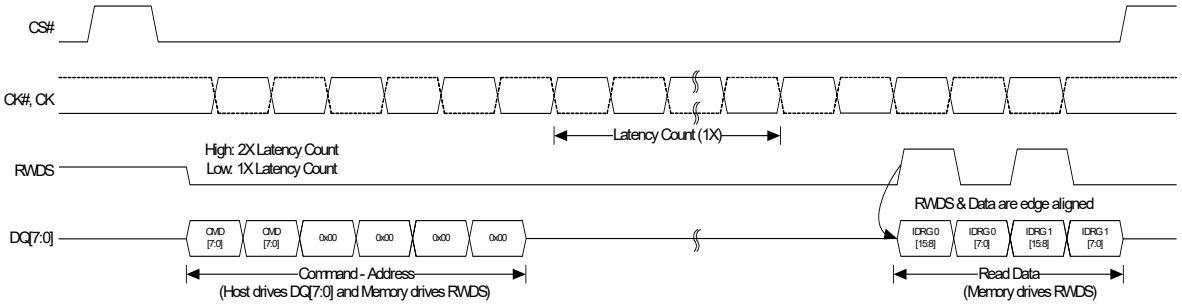
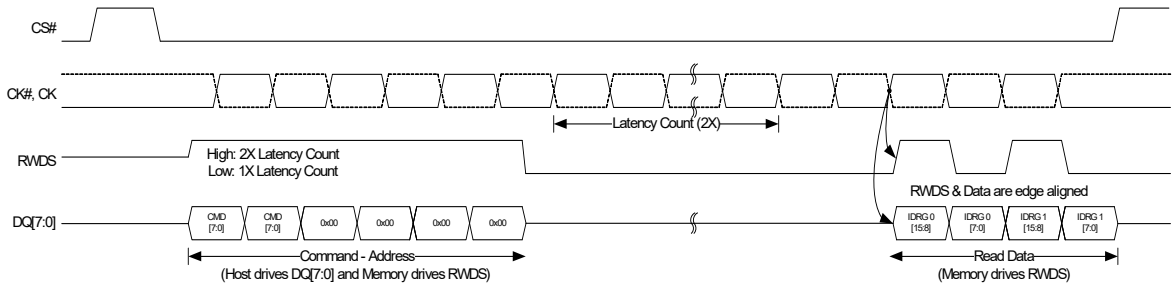


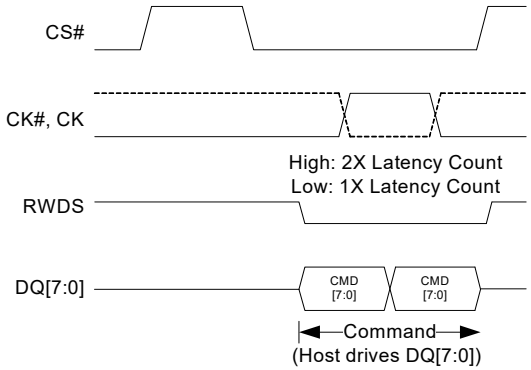
Figure 11. READ ID with 2X Latency Transaction (DDR)[17]



DEEP POWER DOWN Transaction

DEEP POWER DOWN transaction brings the device into Deep Power Down state which is the lowest power consumption state. Writing a “0” to CR0[15] will also bring the device in Deep Power Down State. All register contents are lost in Deep Power Down State and the device powers-up in its default state.

Figure 12. DEEP POWER DOWN Transaction (DDR)



Notes
16. RWDS is driven by HyperRAM phase aligned with data.
17. RWDS is driven by HyperRAM during Command & Address cycles for 2X latency and then is driven again phase aligned with data.

READ Transaction

The READ transaction reads data from the memory array. It has a latency requirement (dummy cycles) which allows the device's internal circuitry enough time to access the addressed memory location. During these latency cycles, the host can tristate the data bus DQ[7:0].

Figure 13. READ with 1X Latency Transaction (DDR)[18]

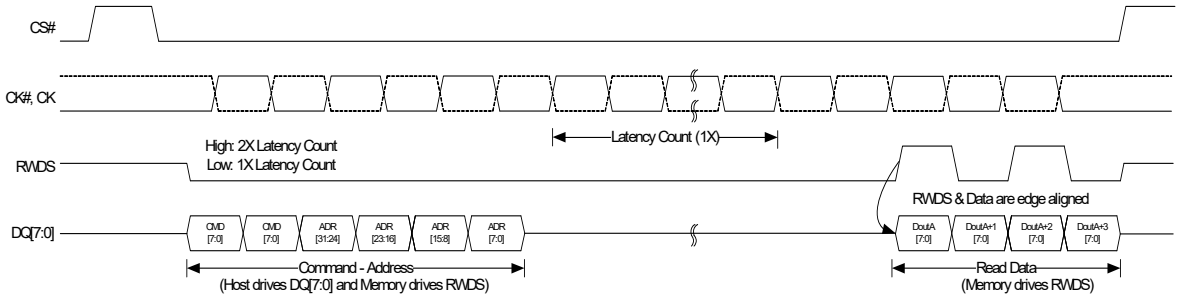
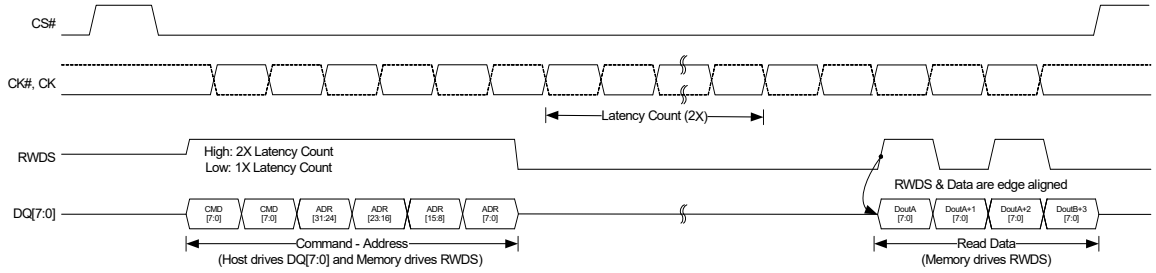


Figure 14. READ with 2X Latency Transaction (DDR)[19]

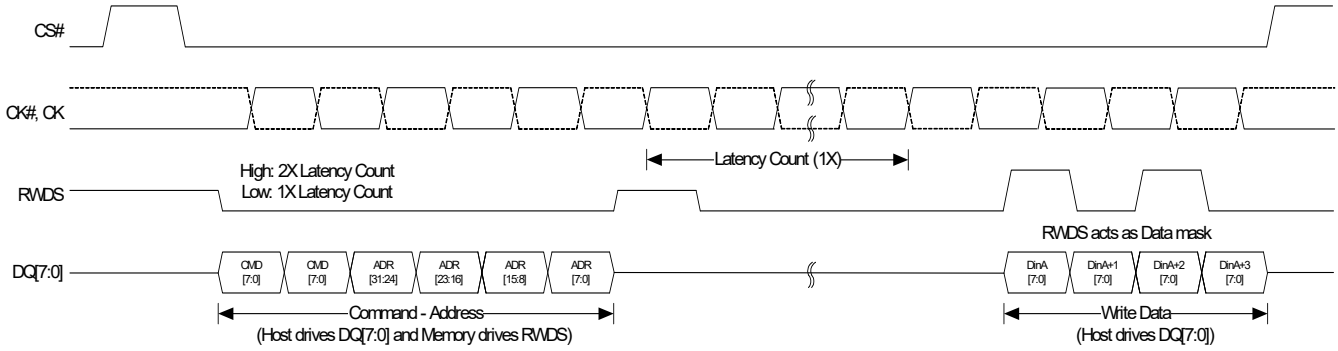


WRITE Transaction

The WRITE transaction writes data to the memory array. It has a latency requirement (dummy cycles) which allows the device's internal circuitry enough time to access the addressed memory location. During these latency cycles, the host can tristate the data bus DQ[7:0].

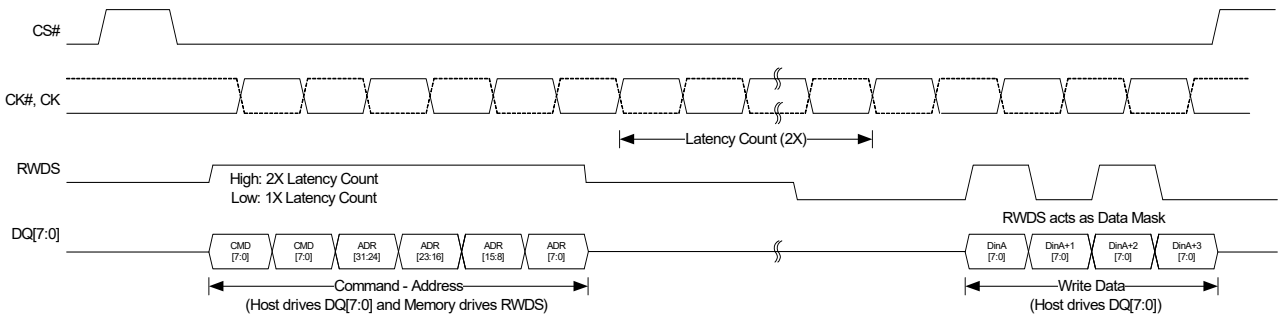
WRITE ENABLE transaction which sets the WEL latch must be executed before the first WRITE. The WEL latch stays set to '1' at the end of any successful memory write transaction. It must be reset by WRITE DISABLE transaction to prevent any inadvertent writes to the memory array.

Figure 15. WRITE with 1X Latency Transaction (DDR)[20, 21]



Notes
18. RWDS is driven by HyperRAM phase aligned with data.
19. RWDS is driven by HyperRAM during Command & Address cycles for 2X latency and then is driven again phase aligned with data.
20. RWDS is driven by the host.
21. Data DinA and DinA+2 are masked.

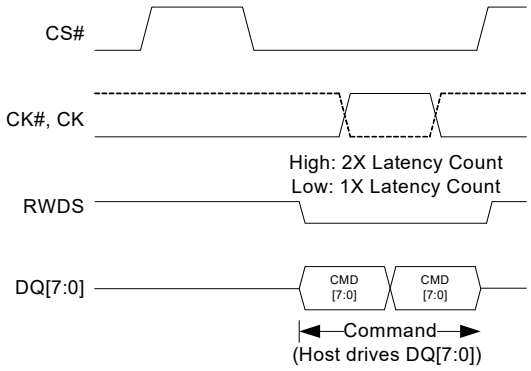
Figure 16. WRITE with 2X Latency Transaction (DDR)[22, 23]



WRITE ENABLE Transaction

The WRITE ENABLE transaction must be executed prior to any transaction that modifies data either in the memory array or the registers.

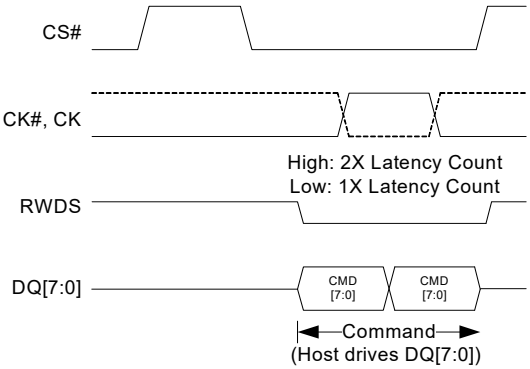
Figure 17. WRITE ENABLE Transaction (DDR)



WRITE DISABLE Transaction

The WRITE DISABLE transaction inhibits writing data either in the memory array or the registers.

Figure 18. WRITE DISABLE Transaction (DDR)



Notes
22. RWDS is driven by HyperRAM during Command and Address cycles for 2X latency and then is driven by the host for data masking.
23. Data DinA and DinA+2 are masked.

READ ANY REGISTER Transaction

The READ ANY REGISTER transaction reads all the device registers. It has a latency requirement (dummy cycles) which allows the device's internal circuitry enough time to access the addressed register location. During these latency cycles, the host can tristate the data bus DQ[7:0].

Figure 19. READ ANY REGISTER with 1X Latency Transaction (DDR)[24]

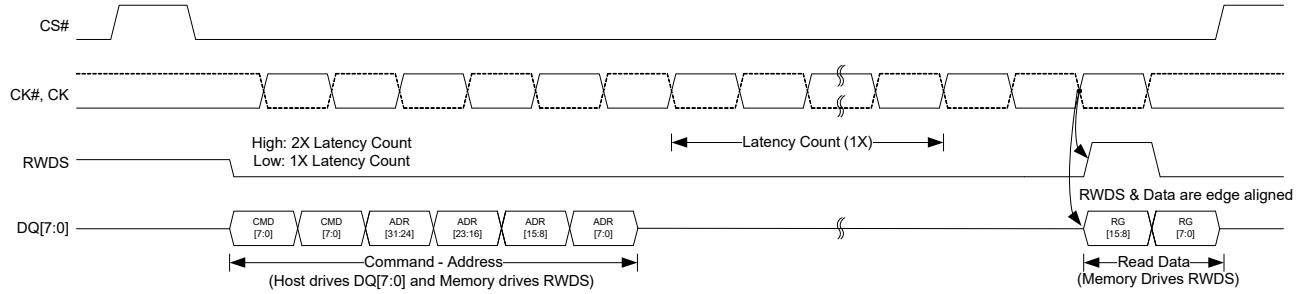
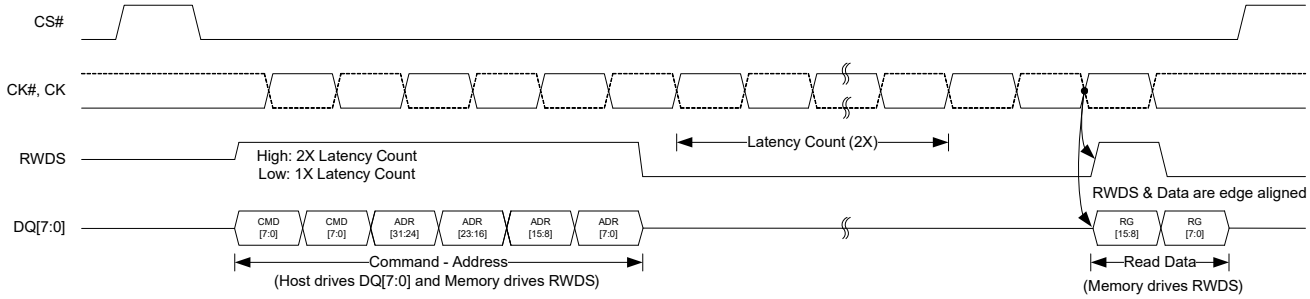


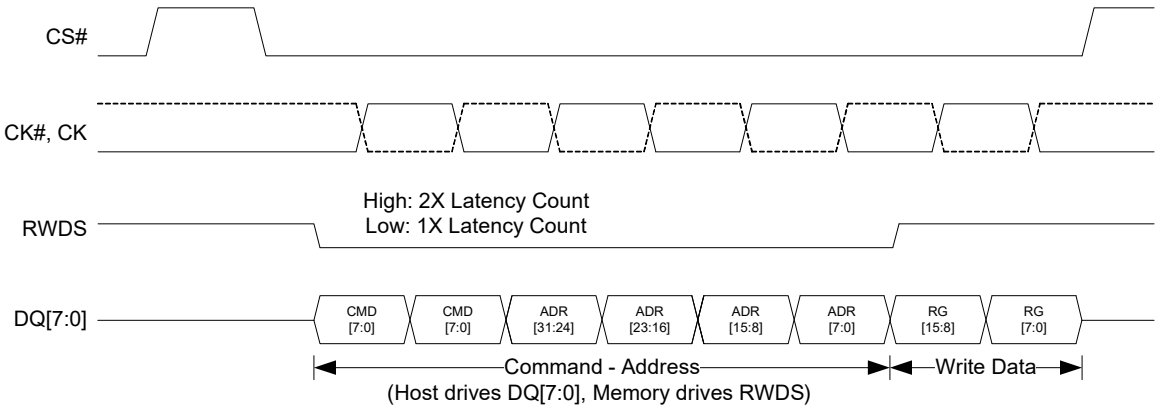
Figure 20. READ ANY REGISTER with 2X Latency Transaction (DDR)[25]



WRITE ANY REGISTER Transaction

The WRITE ANY REGISTER transaction writes to the device registers. It does not have a latency requirement (dummy cycles).

Figure 21. xSPI (Octal) Write with No Latency Transaction (DDR) (Register Writes)[26, 27]



Notes
24. RWDS is driven by HyperRAM phase aligned with data.
25. RWDS is driven by HyperRAM during Command & Address cycles for 2X latency and then driven again phase aligned with data.
26. Write with no latency transaction is used for register writes only.
27. Data Mask on RWDS is not supported.

Data Placement During Memory READ/WRITE Transactions

Data placement during memory Read/Write is dependent upon the host. The device will output data (read) as it was written in (write). Hence both Big Endian and Little Endian are supported for the memory array.

Table 4. Data Placement during Memory READ and WRITE

Address Space	Byte Order	Byte Position	Word Data Bit	DQ	Bit Order
Memory	Big-endian	A	15	7	When data is being accessed in memory space: *The first byte of each word read or written is the "A" byte and the second is the "B" byte.* *The bits of the word within the A and B bytes depend on how the data was written. If the word lower address bits 7-0 are written in the A byte position and bits 15-8 are written into the B byte position, or vice versa, they will be read back in the same order.* So, memory space can be stored and read in either little-endian or big-endian order.
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	
		B	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	
	Little-endian	A	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	
		B	15	7	
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	

Data Placement During Register READ/WRITE Transactions

Data placement during register Read/Write is Big Endian.

Table 5. Data Placement during Register READ/WRITE Transactions

Address Space	Byte Order	Byte Position	Word Data Bit	DQ	Bit Order
Register	Big-endian	A	15	7	When data is being accessed in register space: During a Read transaction on the xSPI (Octal) two bytes are transferred on each clock cycle. The upper order byte A (Word[15:8]) is transferred between the rising and falling edges of RWDS (edge aligned). The lower order byte B (Word[7:0]) is transferred between the falling and rising edges of RWDS. During a write, the upper order byte A (Word[15:8]) is transferred on the CK rising edge and the lower order byte B (Word[7:0]) is transferred on the CK falling edge. So, register space is always read and written in Big-endian order because registers have device dependent fixed bit location and meaning definitions.
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	
		B	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	

Memory Space

xSPI (Octal) Interface

Table 6. Memory Space Address Map (byte based - 8 bits with least significant bit A(0) always set to '0')

Unit Type	Count	System Byte Address Bits	Address Bits	Notes
Rows within 64 Mb device	8192 (rows)	A22 - A10	22 - 10	
Row	1 (row)	A9 - A4	9 - 4	512 (16-bit word) or 1 KB
Half-page	16 (byte addresses)	A3 - A0	3 - 0	16 bytes (8 words) A0 always set to "0"

Density and Row Boundaries

The DRAM array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the Row Address Bit Count and Column Address Bit Count fields in the ID0 register. For example: a 64 Mb HyperRAM device has 10 column address bits and 13 row address bits for a total of 23 address bits (byte address) = 2^{23} = 8MB (4M words). The 10 column address bits indicate that each row holds 2^{10} = 512 words = 1KB. The row address bit count indicates there are 8196 rows to be refreshed within each array refresh interval. The row count is used in calculating the refresh interval.

Register Space Access

xSPI (Octal) Interface

Table 7. Register Space Address Map (Address bit A0 always set to '0')

Registers	Address (Byte Addressable)
Identification Registers 0 (ID0[15:0])	0x00000000
Identification Registers 1 (ID1[15:0])	0x00000002
Configuration Registers 0 (ID0[15:0])	0x00000004
Configuration Registers 1 (ID1[15:0])	0x00000006
Die Manufacture Information Register (Registers 0 to Register 17)	0x00000008, 0x0000000A to 0x0000002A

Device Identification Registers

There are two read-only, nonvolatile, word registers, that provide information on the device selected when CS# is LOW. The device information fields identify:

- Manufacturer
- Type
- Density
  - Row address bit count
  - Column address bit count
- Refresh Type

Table 8. Identification Register 0 (ID0) Bit Assignments

Bits	Function	Settings (Binary)
[15:14]	Reserved	00 - Default
13	Reserved	0 - Default
[12:8]	Row Address Bit Count	00000 - One row address bit ... 11111 - Thirty-two row address bits ... 01100 - 64 Mb - Thirteen row address bits (default)
[7:4]	Column Address Bit Count	0000 - One column address bits ... 1000 - Nine column address bits (default) ... 1111 - Sixteen column address bits
[3:0]	Manufacturer	0000 - Reserved 0001 - Cypress (default) 0010 to 1111 - Reserved

Table 9. Identification Register 1 (ID1) Bit Assignments

Bits	Function	Settings (Binary)
[15:4]	Reserved	0000_0000_0000 (default)
[3:0]	Device Type	0001 - HyperRAM 2.0 0000, 0010 to 1111 - Reserved

Device Configuration Registers

Configuration Register 0 (CR0)

Configuration Register 0 (CR0) is used to define the power state and access protocol operating conditions for the HyperRAM device. Configurable characteristics include:

- Wrapped Burst Length (16, 32, 64, or 128 byte aligned and length data group)
- Wrapped Burst Type
  - Legacy wrap (sequential access with wrap around within a selected length and aligned group)
  - Hybrid wrap (Legacy wrap once then linear burst at start of the next sequential group)
- Initial Latency
- Variable Latency
  - Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output Drive Strength
- Deep Power Down (DPD) Mode

Table 10. Configuration Register 0 (CR0) Bit Assignments

CR0 Bit	Function	Settings (Binary)
[15]	Deep Power Down Enable	1 - Normal operation (default). HyperRAM will automatically set this value to '1' after DPD exit 0 - Writing 0 causes the device to enter Deep Power Down
[14:12]	Drive Strength	000 - 34 ohms (default) 001 - 115 ohms 010 - 67 ohms 011 - 46 ohms 100 - 34 ohms 101 - 27 ohms 110 - 22 ohms 111 - 19 ohms
[11:8]	Reserved	1 - Reserved (default) Reserved for Future Use. When writing this register, these bits should be set to 1 for future compatibility.
[7:4]	Initial Latency	0000 - 5 Clock Latency @ 133 Max Frequency 0001 - 6 Clock Latency @ 166 Max Frequency 0010 - 7 Clock Latency @ 200 MHz/166 MHz Max Frequency (default) 0011 - Reserved 0100 - Reserved ... 1101 - Reserved 1110 - 3 Clock Latency @ 85 Max Frequency 1111 - 4 Clock Latency @ 104 Max Frequency
[3]	Fixed Latency Enable	0 - Variable Latency - 1 or 2 times Initial Latency depending on RWDS during CA cycles. 1 - Fixed 2 times Initial Latency (default)
[2]	Hybrid Burst Enable	0: Wrapped burst sequence to follow hybrid burst sequencing 1: Wrapped burst sequence in legacy wrapped burst manner (default)
[1:0]	Burst Length	00 - 128 bytes 01 - 64 bytes 10- 16 bytes 11 - 32 bytes (default)

Wrapped Burst

A wrapped burst transaction accesses memory within a group of words aligned on a word boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, or 128 bytes alignment and length. During wrapped transactions, access starts at the CA selected location within the group, continues to the end of the configured word group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses.

Hybrid Burst

The beginning of a hybrid burst will wrap within the target address wrapped burst group length before continuing to the next half-page of data beyond the end of the wrap group. Continued access is in linear burst order until the transfer is ended by returning CS# HIGH. This hybrid of a wrapped burst followed by a linear burst starting at the beginning of the next burst group, allows multiple sequential address cache lines to be filled in a single access. The first cache line is filled starting at the critical word. Then the next sequential line in memory can be read in to the cache while the first line is being processed.

Table 11. CR0[2] Control of Wrapped Burst Sequence

Bit	Default Value	Setting Details
CR0[2]	1b	Hybrid Burst Enable CR0[2] = 0: Wrapped burst sequence to follow hybrid burst sequencing CR0[2] = 1: Wrapped burst sequence in legacy wrapped burst manner

Table 12. Example Wrapped Burst Sequences (Addressing)

Burst Type	Wrap Boundary (bytes)	Start Address (Hex)	Sequence of Byte Addresses (Hex) of Data Words
Hybrid 64	64 Wrap once then Linear	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, 2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00 (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 40, 42, 44, 46, 48, 4A, 4C, 4E, 50, 52, ...
Hybrid 64	64 Wrap once then Linear	XXXXXX2E	2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00, 02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 40, 42, 44, 46, 48, 4A, 4B, 4C, 4D, 4E, 4F, 50, 52, ...
Hybrid 16	16 Wrap once then Linear	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 00 (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 10, 12, 14, 16, 18, 1A, ..
Hybrid 16	16 Wrap once then Linear	XXXXXX0C	0C, 0E, 00, 02, 04, 06, 08, 0A (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 10, 12, 14, 16, 18, 1A, ...
Hybrid 32	32 Wrap once then Linear	XXXXXX0A	0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 00, 02, 04, 06, 08 (wrap complete, now linear beyond the end of the initial 32 byte wrap group) 20, 22, 24, 26, 28, 2A, ...
Wrap 64	64	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, 2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00, ...
Wrap 64	64	XXXXXX2E	2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00, 02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, 2E, 30, ….
Wrap 16	16	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 00, ...
Wrap 16	16	XXXXXX0C	0C, 0E, 00, 02, 04, 06, 08, 0A, ...
Wrap 32	32	XXXXXX0A	0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 00, 02, 04, 06, 08, ...
Linear	Linear Burst	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, ...

Initial Latency

Memory Space read and write transactions or Register Space read transactions require some initial latency to open the row selected by the CA. This initial latency is t_{ACC}. The number of latency clocks needed to satisfy t_{ACC} depends on the clock input frequency can vary from 3 to 7 clocks. The value in CR0[7:4] selects the number of clocks for initial latency. The default value is 7 clocks, allowing for operation up to a maximum frequency of 200MHz prior to the host system setting a lower initial latency value that may be more optimal for the system.

In the event a distributed refresh is required at the time a Memory Space read or write transaction or Register Space read transaction begins, the RWDS signal goes High during the CA to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Register Space write transactions always have zero initial latency. RWDS may be HIGH or LOW during the CA period. The level of RWDS during the CA period does not affect the placement of register data immediately after the CA, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

Fixed Latency

A configuration register option bit CR0[3] is provided to make all Memory Space read and write transactions or Register Space read transactions require the same initial latency by always driving RWDS HIGH during the CA to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh, it simply provides a fixed (deterministic) initial latency for all of these transaction types. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven HIGH only when additional latency for a refresh is required.

Drive Strength

DQ and RWDS signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the DQ[7:0] and RWDS signal output impedance to customize the DQ and RWDS signal impedance to the system conditions to minimize high speed signal behaviors such as overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b to select the mid point of the available output impedance options.

The impedance values shown are typical for both pull-up and pull-down drivers at typical silicon process conditions, nominal operating voltage (1.8 V or 3.0 V) and 50°C. The impedance values may vary from the typical values depending on the Process, Voltage, and Temperature (PVT) conditions. Impedance will increase with slower process, lower voltage, or higher temperature. Impedance will decrease with faster process, higher voltage, or lower temperature.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

Deep Power Down

When the HyperRAM device is not needed for system operation, it may be placed in a very low power consuming state called Deep Power Down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD state within t_{DPDIN} time and all refresh operations stop. The data in RAM is lost, (becomes invalid without refresh) during DPD state. Exiting DPD requires driving CS# LOW then HIGH, POR, or a reset. Only CS# and RESET# signals are monitored during DPD mode. For additional details, see Deep Power Down on page 27.

Configuration Register 1

Configuration Register 1 (CR1) is used to define the refresh array size, refresh rate and hybrid sleep for the HyperRAM device. Configurable characteristics include:

- Partial Array Refresh
- Hybrid Sleep State
- Refresh Rate

Table 13. Configuration Register 1 (CR1) Bit Assignments

CR1 Bit	Function	Setting(Binary)
[15:8]	Reserved	FFh - Reserved (default) These bits should always be set to FFh
[7]	Burst Type	1 - Linear Burst (default) 0 - Wrapped Burst
[6]	Master Clock Type	1 - Single Ended - CK (default) 0 - Differential - CK#, CK
[5]	Hybrid Sleep	1 - Causes the device to enter Hybrid Sleep State 0 - Normal operation (default)
[4:2]	Partial Array Refresh	000 - Full Array (default) 001 - Bottom 1/2 Array 010 - Bottom 1/4 Array 011 - Bottom 1/8 Array 100 - none 101 - Top 1/2 Array 110 - Top 1/4 Array 111 - Top 1/8 Array
[1:0]	Distributed Refresh Interval	10 - 1µs t_{CSM} (Industrial Plus temperature range devices) 11 - Reserved 00 - Reserved 01 - 4µs t_{CSM} (Industrial temperature range devices)

Burst Type

Two burst types, namely Linear and Wrapped, are supported in xSPI (Octal) mode by HyperRAM. CR1[7] selects which type to use.

Master Clock Type

Two clock types, namely single ended and differential, are supported. CR1[6] selects which type to use.

Partial Array Refresh

The partial array refresh configuration restricts the refresh operation in HyperRAM to a portion of the memory array specified by CR1[5:3]. This reduces the standby current. The default configuration refreshes the whole array.

Hybrid Sleep (HS)

When the HyperRAM is not needed for system operation but data in the device needs to be retained, it may be placed in Hybrid Sleep state to save more power. Enter Hybrid Sleep state by writing 0 to CR1[5]. Bringing CS# LOW will cause the device to exit HS state and set CR1[5] to 1. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost.

Distributed Refresh Interval

The DRAM array requires periodic refresh of all bits in the array. This can be done by the host system by reading or writing a location in each row within a specified time limit. The read or write access copies a row of bits to an internal buffer. At the end of the access the bits in the buffer are written back to the row in memory, thereby recharging (refreshing) the bits in the row of DRAM memory cells.

HyperRAM devices include self-refresh logic that will refresh rows automatically. The automatic refresh of a row can only be done when the memory is not being actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS HIGH during the CA period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access.

The required refresh interval for the entire memory array varies with temperature as shown in Table 14. This is the time within which all rows must be refreshed. Refresh of all rows could be done as a single batch of accesses at the beginning of each interval, in groups (burst refresh) of several rows at a time, spread throughout each interval, or as single row refreshes evenly distributed throughout the interval. The self-refresh logic distributes single row refresh operations throughout the interval so that the memory is not busy doing a burst of refresh operations for a long period, such that the burst refresh would delay host access for a long period.

Table 14. Array Refresh Interval per Temperature

Device Temperature (°C)	Array Refresh Interval (ms)	Array Rows	Recommended t_{CSM} (µs)
85	64	8192	4
105	16	8192	1

The distributed refresh method requires that the host does not do burst transactions that are so long as to prevent the memory from doing the distributed refreshes when they are needed. This sets an upper limit on the length of read and write transactions so that the refresh logic can insert a refresh between transactions. This limit is called the CS# LOW maximum time (t_{CSM}). The t_{CSM} value is determined by the array refresh interval divided by the number of rows in the array, then reducing this calculation by half to ensure that a distributed refresh interval cannot be entirely missed by a maximum length host access starting immediately before a distributed refresh is needed. Because t_{CSM} is set to half the required distributed refresh interval, any series of maximum length host accesses that delay refresh operations will catch up on refresh operations at twice the rate required by the refresh interval divided by the number of rows.

The host system is required to respect the t_{CSM} value by ending each transaction before violating t_{CSM}. This can be done by host memory controller logic splitting long transactions when reaching the t_{CSM} limit, or by host system hardware or software not performing a single read or write transaction that would be longer than t_{CSM}.

As noted in Table 14 the array refresh interval is longer at lower temperatures such that t_{CSM} could be increased to allow longer transactions. The host system can either use the t_{CSM} value from the table for the maximum operating temperature or, may determine the current operating temperature from a temperature sensor in the system in order to set a longer distributed refresh interval.

Interface States

Table 15 describes the required value of each signal for each interface state.

Table 15. Interface States

Interface State	V_{CC} / $V_{CC}Q$	CS#	CK, CK#	DQ7-DQ0	RWDS	RESET#
Power-Off	< V_{LKO}	X	X	HIGH-Z	HIGH-Z	X
Power-On (Cold) Reset	≥ V_{CC} / $V_{CC}Q$ min	X	X	HIGH-Z	HIGH-Z	X
Hardware (Warm) Reset	≥ V_{CC} / $V_{CC}Q$ min	X	X	HIGH-Z	HIGH-Z	L
Interface Standby	≥ V_{CC} / $V_{CC}Q$ min	H	X	HIGH-Z	HIGH-Z	H
CA	≥ V_{CC} / $V_{CC}Q$ min	L	T	Master Output Valid	Y	H
Read Initial Access Latency (data bus turn around period)	≥ V_{CC} / $V_{CC}Q$ min	L	T	HIGH-Z	L	H
Write Initial Access Latency (RWDS turn around period)	≥ V_{CC} / $V_{CC}Q$ min	L	T	HIGH-Z	HIGH-Z	H
Read data transfer	≥ V_{CC} / $V_{CC}Q$ min	L	T	Slave Output Valid	Slave Output Valid Z or T	H
Write data transfer with Initial Latency	≥ V_{CC} / $V_{CC}Q$ min	L	T	Master Output Valid	Master Output Valid X or T	H
Write data transfer without Initial Latency [28]	≥ V_{CC} / $V_{CC}Q$ min	L	T	Master Output Valid	Slave Output L or HIGH-Z	H
Active Clock Stop [29]	≥ V_{CC} / $V_{CC}Q$ min	L	Idle	Master or Slave Output Valid or HIGH-Z	Y	H
Deep Power Down	≥ V_{CC} / $V_{CC}Q$ min	H	X or T	HIGH-Z	HIGH-Z	H
Hybrid Sleep	≥ V_{CC} / $V_{CC}Q$ min	H	X or T	HIGH-Z	HIGH-Z	H

Legend
L = V_{IL}
H = V_{IH}
X = either V_{IL} or V_{IH}
Y= either V_{IL} or V_{IH} or V_{OL} or V_{OH}
Z = either V_{OL} or V_{OH}
L/H = rising edge
H/L = falling edge
T = Toggling during information transfer
Idle = CK is LOW and CK# is HIGH
Valid = all bus signals have stable L or H level

Notes
28. Writes without initial latency (with zero initial latency), do not have a turn around period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required. Since master write data immediately follows the CA period the HyperRAM device may continue to drive RWDS LOW or may take RWDS to HIGH-Z. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).
29. Active Clock Stop is described in Active Clock Stop on page 26. DPD is described in Hybrid Sleep on page 26.

Power Conservation Modes

Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CS# = HIGH). All inputs, and outputs other than CS# and RESET# are ignored in this state.

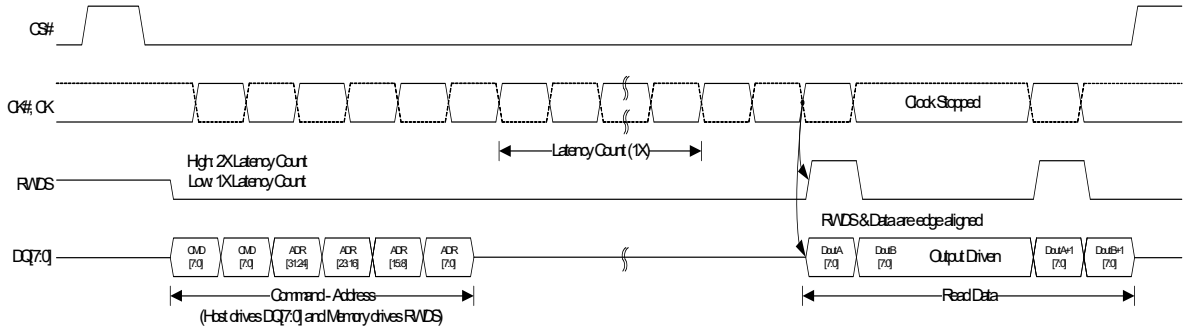
Active Clock Stop

Design Note: Active Clock Stop feature is pending device characterization to determine if it will be supported.

The Active Clock Stop state reduces device interface energy consumption to the I_{CC6} level during the data transfer portion of a read or write operation. The device automatically enables this state when clock remains stable for t_{ACC} + 30 ns. While in Active Clock Stop state, read data is latched and always driven onto the data bus. I_{CC6} shown in DC Characteristics on page 30.

Active Clock Stop state helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be LOW throughout these extended data transfer cycles, the memory device host interface will go into the Active Clock Stop current level at t_{ACC} + 30 ns. This allows the device to transition into a lower current state if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. The Active Clock Stop state must not be used in violation of the t_{CSM} limit. CS# must go HIGH before t_{CSM} is violated. Clock can be stopped during any portion of the active transaction as long as it is in the LOW state. Note that it is recommended to avoid stopping the clock during register access.

Figure 22. Active Clock Stop During Read Transaction (DDR)[30]



Hybrid Sleep

In the Hybrid Sleep (HS) state, the current consumption is reduced (I_{HS}). HS state is entered by writing a 0 to CR1[5]. The device reduces power within t_{HSIN} time. The data in Memory Space and Register Space is retained during HS state. Bringing CS# LOW will cause the device to exit HS state and set CR1[5] to 1. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost. Returning to Standby state requires t_{EXITHS} time. Following the exit from HS due to any of these events, the device is in the same state as entering Hybrid Sleep.

Figure 23. Enter HS Transaction

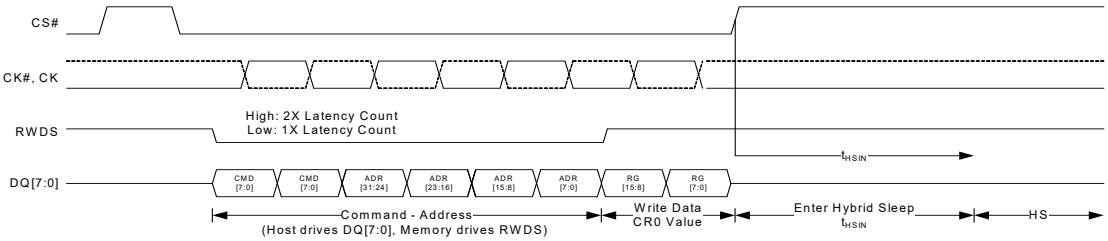
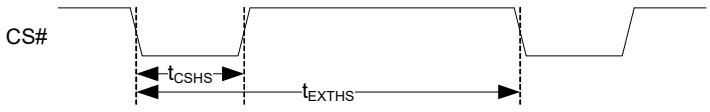


Figure 24. Exit HS Transaction



Note

30. RWDS is LOW during the CA cycles. In this Read Transaction there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.

Table 16. Hybrid Sleep Timing Parameters

Parameter	Description	Min	Max	Unit
t_{HSIN}	Hybrid Sleep CR1[5] = 0 register write to DPD power level	–	3	µs
t_{CSHS}	CS# Pulse Width to Exit HS	60	3000	ns
t_{EXTHS}	CS# Exit Hybrid Sleep to Standby wakeup time	–	100	µs

Deep Power Down

In the Deep Power Down (DPD) state, current consumption is driven to the lowest possible level (I_{DPD}). DPD state is entered by writing a 0 to CR0[15]. The device reduces power within t_{DPDIN} time and all refresh operations stop. The data in Memory Space is lost, (becomes invalid without refresh) during DPD state. Driving CS# LOW then HIGH will cause the device to exit DPD state. Also, POR, or a hardware reset will cause the device to exit DPD state. Returning to Standby state requires t_{EXTDPD} time. Returning to Standby state following a POR requires t_{VCS} time, as with any other POR. Following the exit from DPD due to any of these events, the device is in the same state as following POR.

Note In xSPI (Octal), Deep Power Down transaction or Write Any register transaction can be used to enter DPD.

Figure 25. Enter DPD Transaction

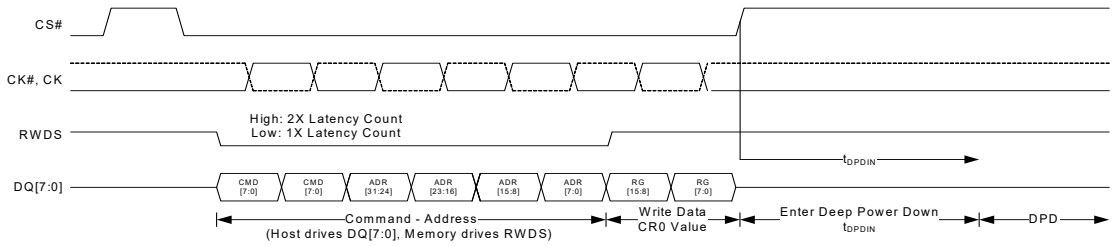


Figure 26. Exit DPD Transaction

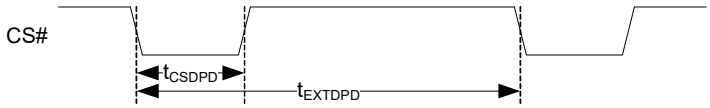


Table 17. Deep Power Down Timing Parameters

Parameter	Description	Min	Max	Unit
t_{DPDIN}	Deep Power Down CR0[15] = 0 register write to DPD power level	–	3	µs
t_{CSDPD}	CS# Pulse Width to Exit DPD	200	3000	ns
t_{EXTDPD}	CS# Exit Deep Power Down to Standby wakeup time	–	150	µs

Notes
31. For a complete list of supported MCPs, refer to Ordering Information on page 45.
32. No extra leakage current will be generated will VCCQ DIE_STK[1:0] connections.

Electrical Specifications

Absolute Maximum Ratings

Storage Temperature Plastic Packages	–65 °C to +150 °C
Ambient Temperature with Power Applied	–65 °C to +115 °C
Voltage with Respect to Ground	
All signals[33]	–0.5V to +(V_{CC} + 0.5V)
Output Short Circuit Current[34]	100 mA
V_{CC}, $V_{CC}Q$	–0.5V to +4.0V

Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may negative overshoot V_{SS} to –1.0V or positive overshoot to V_{CC} +1.0V, for periods up to 20 ns.

Figure 27. Maximum Negative Overshoot Waveform

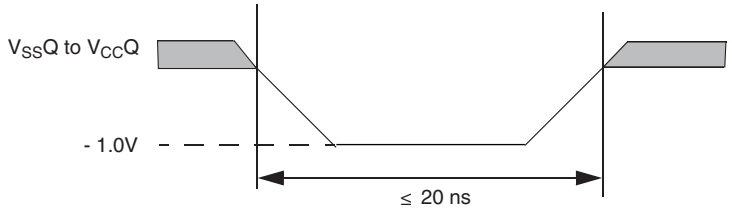
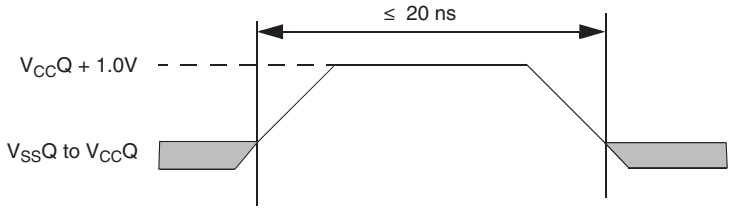


Figure 28. Maximum Positive Overshoot Waveform



Latch-up Characteristics

Table 18. Latch-up Specification[36]

Description	Min	Max	Unit
Input voltage with respect to $V_{SS}Q$ on all input only connections	– 1.0	$V_{CC}Q$ + 1.0	V
Input voltage with respect to $V_{SS}Q$ on all I/O connections	–1.0	$V_{CC}Q$ + 1.0	V
$V_{CC}Q$ Current	–100	+100	mA

Notes

33. Minimum DC voltage on input or I/O signal is -1.0V. During voltage transitions, input or I/O signals may undershoot V_{SS} to -1.0V for periods of up to 20 ns. See Figure 27. Maximum DC voltage on input or I/O signals is V_{CC} +1.0V. During voltage transitions, input or I/O signals may overshoot to V_{CC} +1.0V for periods up to 20 ns. See Figure 28.
34. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
35. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
36. Excludes power supplies $V_{CC}/V_{CC}Q$. Test conditions: $V_{CC} = V_{CC}Q$, one connection at a time tested, connections not being tested are at V_{SS}.

Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

Temperature Ranges

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial (I)	–40	85	°C
		Industrial Plus (V)	–40	105	°C
		Automotive, AEC-Q100 Grade 3 (A)	–40	85	°C
		Automotive, AEC-Q100 Grade 2 (B)	–40	105	°C

Power Supply Voltages

Description	Min	Max	Unit
1.8 V V_{CC} Power Supply	1.7	2.0	V
3.0 V V_{CC} Power Supply	2.7	3.6	V

DC Characteristics

Table 19. DC Characteristics (CMOS Compatible)

Parameter	Description	Test Conditions	64 Mb			Unit
			Min	Typ[37]	Max	
I_{LI1}	Input Leakage Current 3.0 V Device Reset Signal High Only	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	–0.1	µA
I_{LI2}	Input Leakage Current 1.8 V Device Reset Signal High Only	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	–0.1	µA
I_{LI3}	Input Leakage Current 3.0 V Device Reset Signal Low Only[38]	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	+15.0	µA
I_{LI4}	Input Leakage Current 1.8 V Device Reset Signal Low Only[38]	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	+15.0	µA
I_{CC1}	V_{CC} Active Read Current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	– –	15	25	mA
		CS# = V_{IL}, @166 MHz, V_{CC} = 3.6 V	–	15	28	mA
		CS# = VSS, @200 MHz, V_{CC} = 3.6V	–	15	30	mA
I_{CC2}	V_{CC} Active Write Current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	– –	15	25	mA
		CS# = V_{IL}, @166 MHz, V_{CC} = 3.6 V	–	15	28	mA
		CS# = V_{SS}, @200 MHz, V_{CC} = 3.6V	–	15	30	mA
I_{CC4I}	V_{CC} Standby Current (–40 °C to +85 °C)	CS# = V_{IH}, V_{CC} = 2.0 V CS# = V_{IH}, V_{CC} = 3.6 V	–	80 90	220 250	µA
I_{CC4IP}	V_{CC} Standby Current (–40 °C to +105 °C)	CS# = V_{IH}, V_{CC} = 2.0 V CS# = VI_H, V_{CC} = 3.6 V	–	80 90	330 360	µA
I_{CC5}	Reset Current	CS# = V_{IH}, RESET# = V_{IL}, $V_{CC} = V_{CC}$ max	–	–	1	mA
I_{CC6I}	Active Clock Stop Current (–40 °C to +85 °C)	CS# = V_{IL}, RESET# = V_{IH}, $V_{CC} = V_{CC}$ max	–	5	8	mA
I_{CC6IP}	Active Clock Stop Current (–40 °C to +105 °C)	CS# = V_{IL}, RESET# = V_{IH}, $V_{CC} = V_{CC}$ max	–	8	12	mA
I_{CC7}	V_{CC} Current during power up[37]	CS# = V_{IH}, $V_{CC} = V_{CC}$ max, $V_{CC} = V_{CCQ}$ = 2.0 V or 3.6 V	–	–	35	mA
I_{DPD}	Deep Power Down Current 3.0 V (–40 °C to +85 °C)	CS# = V_{IH}, V_{CC} = 3.6 V	–	–	12	µA
I_{DPD}	Deep Power Down Current 1.8 V (–40 °C to +85 °C)	CS# = V_{IH}, V_{CC} = 2.0 V	–	–	10	µA
I_{DPD}	Deep Power Down Current 3.0 V (–40 °C to +105 °C)	CS# = V_{IH}, V_{CC} = 3.6 V	–	–	15	µA
I_{DPD}	Deep Power Down Current 1.8 V (–40 °C to +105 °C)	CS# = V_{IH}, V_{CC} = 2.0 V	–	–	12	µA

Notes
37. Not 100% tested.
38. RESET# LOW initiates exits from DPD state and initiates the draw of ICC5 reset current, making ILI during Reset# LOW insignificant.

Table 19. DC Characteristics (CMOS Compatible) (Continued)

Parameter	Description	Test Conditions	64 Mb			Unit
			Min	Typ[37]	Max	
I_{HS}	Hybrid Sleep Current 3.0 V (–40 °C to +85 °C)	CS# = V_{IH}, V_{CC} = 3.6 V	–	35	230	µA
I_{HS}	Hybrid Sleep Current 1.8 V (–40 °C to +85 °C)	CS# = V_{IH}, V_{CC} = 2.0 V	–	25	200	µA
I_{HS}	Hybrid Sleep Current 3.0 V (–40 °C to +105 °C)	CS# = V_{IH}, V_{CC} = 3.6 V	–	35	310	µA
I_{HS}	Hybrid Sleep Current 1.8 V (–40 °C to +105 °C)	CS# = V_{IH}, V_{CC} = 2.0 V	–	25	300	µA
V_{IL}	Input Low Voltage	–	–0.15 x V_{CCQ}	–	0.35 x V_{CCQ}	V
V_{IH}	Input High Voltage	–	0.70 x V_{CCQ}	–	1.15 x V_{CCQ}	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA for DQ[7:0]	–	–	0.20	V
V_{OH}	Output High Voltage	I_{OH} = 100 µA for DQ[7:0]	V_{CCQ}-0.20	–	–	V

Notes
37. Not 100% tested.
38. RESET# LOW initiates exits from DPD state and initiates the draw of ICC5 reset current, making ILI during Reset# LOW insignificant.

Capacitance Characteristics

Table 20. 1.8 V Capacitive Characteristics[39, 40, 41]

Description	Parameter	64 Mb	Unit
		Max	
Input Capacitance (CK, CK#, CS#)	CI	3.0	pF
Delta Input Capacitance (CK, CK#)	CID	0.25	pF
Output Capacitance (RWDS)	CO	3.0	pF
IO Capacitance (DQx)	CIO	3.0	pF
IO Capacitance Delta (DQx)	CIOD	0.25	pF

Table 21. 3.0 V Capacitive Characteristics[39, 40, 41]

Description	Parameter	64 Mb	Unit
		Max	
Input Capacitance (CK, CK#, CS#)	CI	3.0	pF
Delta Input Capacitance (CK, CK#)	CID	0.25	pF
Output Capacitance (RWDS)	CO	3.0	pF
IO Capacitance (DQx)	CIO	3.0	pF
IO Capacitance Delta (DQx)	CIOD	0.25	pF

Notes
39. These values are guaranteed by design and are tested on a sample basis only.
40. Contact capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, V_{CC}Q are applied and all other signals (except the signal under test) floating. DQ's should be in the high impedance state.
41. Note that the capacitance values for the CK, CK#, RWDS and DQx signals must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (LOW) and data being presented on the DQs bus.

Power-up Initialization

HyperRAM products include an on-chip voltage sensor used to launch the power-up initialization process. V_{CC} and $V_{CC}Q$ must be applied simultaneously. When the power supply reaches a stable level at or above V_{CC}(min), the device will require t_{VCS} time to complete its self-initialization process.

The device must not be selected during power-up. CS# must follow the voltage applied on $V_{CC}Q$ until V_{CC} (min) is reached during power-up, and then CS# must remain high for a further delay of t_{VCS}. A simple pull-up resistor from $V_{CC}Q$ to Chip Select (CS#) can be used to insure safe and proper power-up.

If RESET# is LOW during power up, the device delays start of the t_{VCS} period until RESET# is HIGH. The t_{VCS} period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.

Figure 29. Power-up with RESET# HIGH

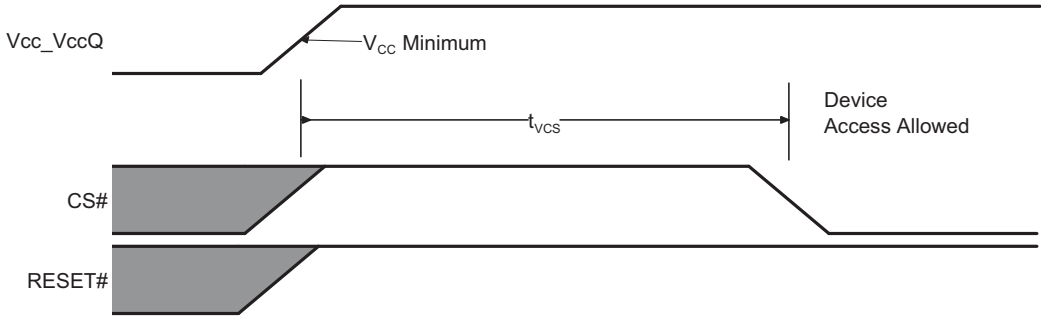


Figure 30. Power-up with RESET# LOW

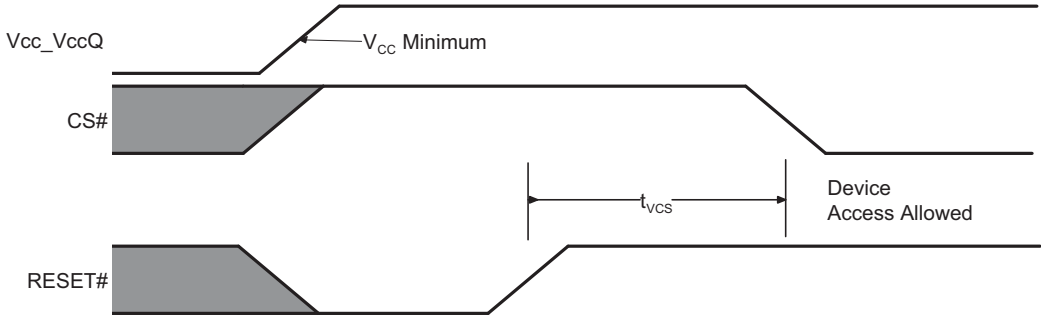


Table 22. Power Up and Reset Parameters[42, 43, 44]

Parameter	Description	Min	Max	Unit
V_{CC}	1.8 V V_{CC} Power Supply	1.7	2.0	V
V_{CC}	3.0 V V_{CC} Power Supply	2.7	3.6	V
t_{VCS}	V_{CC} and $V_{CC}Q \geq$ minimum and RESET# HIGH to first access	–	150	µs

Notes
42. Bus transactions (read and write) are not allowed during the power-up reset time (t_{VCS}).
43. $V_{CC}Q$ must be the same voltage as V_{CC}.
44. V_{CC} ramp rate may be non-linear.

Power Down

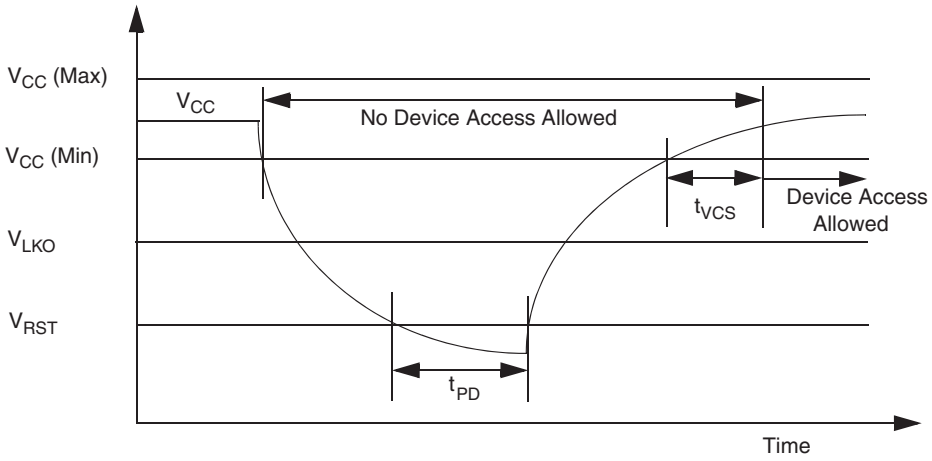
HyperRAM devices are considered to be powered-off when the array power supply (V_{CC}) drops below the V_{CC} Lock-Out voltage (V_{LKO}). During a power supply transition down to the V_{SS} level, $V_{CC}Q$ should remain less than or equal to V_{CC}. At the V_{LKO} level, the HyperRAM device will have lost configuration or array data.

V_{CC} must always be greater than or equal to $V_{CC}Q$ ($V_{CC} \geq V_{CC}Q$).

During Power-Down or voltage drops below V_{LKO}, the array power supply voltages must also drop below V_{CC} Reset (V_{RST}) for a Power Down period (t_{PD}) for the part to initialize correctly when the power supply again rises to V_{CC} minimum. See Figure 31.

If during a voltage drop the V_{CC} stays above V_{LKO} the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If V_{CC} does not go below and remain below V_{RST} for greater than t_{PD}, then there is no assurance that the POR process will be performed. In this case, a hardware reset will be required ensure the device is properly initialized.

Figure 31. Power Down or Voltage Drop



The following section describes HyperRAM device dependent aspects of power down specifications.

Table 23. 1.8 V Power-Down Voltage and Timing[45]

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	1.7	2.0	V
V_{LKO}	V_{CC} Lock-out below which re-initialization is required	1.5	–	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.7	–	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	50	–	µs

Table 24. 3.0 V Power-Down Voltage and Timing[45]

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	2.7	3.6	V
V_{LKO}	V_{CC} Lock-out below which re-initialization is required	2.4	–	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.7	–	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	50	–	µs

Note
45. V_{CC} ramp rate can be non-linear.

Hardware Reset

The RESET# input provides a hardware method of returning the device to the standby state.

During t_{RPH} the device will draw I_{CC5} current. If RESET# continues to be held LOW beyond t_{RPH}, the device draws CMOS standby current (I_{CC4}). While RESET# is LOW (during t_{RP}), and during t_{RPH}, bus transactions are not allowed.

A hardware reset will do the following:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while RESET# is LOW - memory array data is considered as invalid
- Force the device to exit the Hybrid Sleep state
- Force the device to exit the Deep Power Down state

After RESET# returns HIGH, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# LOW, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per Table 14. This may result in the loss of DRAM array data during or immediately following a hardware reset. The host system should assume DRAM array data is lost after a hardware reset and reload any required data.

Figure 32. Hardware Reset Timing Diagram

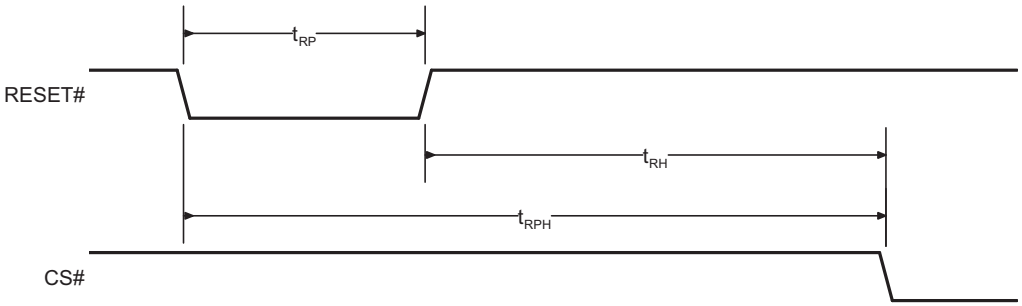


Table 25. Power-Up and Reset Parameters

Parameter	Description	Min	Max	Unit
t_{RP}	RESET# Pulse Width	200	–	ns
t_{RH}	Time between RESET# (HIGH) and CS# (LOW)	200	–	ns
t_{RPH}	RESET# LOW to CS# LOW	400	–	ns

Software Reset

The software reset provides a software method of returning the device to the standby state. During t_{SR} the device will draw I_{CC5} current.

A software reset will do the following:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation during the software reset process - memory array data is considered as invalid

After software reset finishes, the self-refresh operation will resume. Because self-refresh operation is stopped, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per Table 14. This may result in the loss of DRAM array data during or immediately following a software reset. The host system should assume DRAM array data is lost after a software reset and reload any required data.

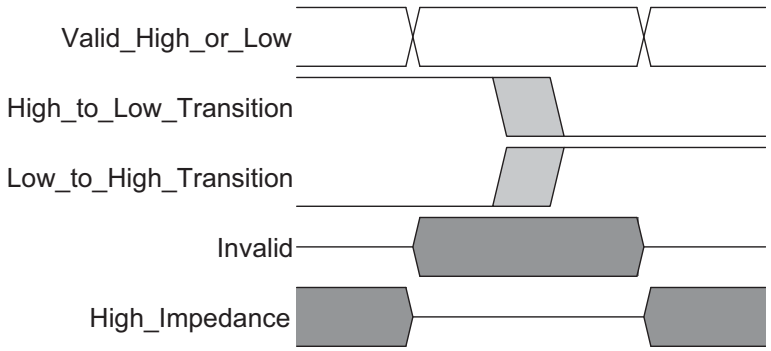
Table 26. Software Reset Timing

Parameter	Description	Min	Max	Unit
t_{SR}	Software Reset transaction CS# HIGH to Device in Standby	–	400	ns

Timing Specifications

The following section describes HyperRAM device dependent aspects of timing specifications.

Key to Switching Waveforms



AC Test Conditions

Figure 33. Test Setup

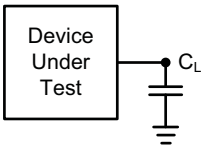
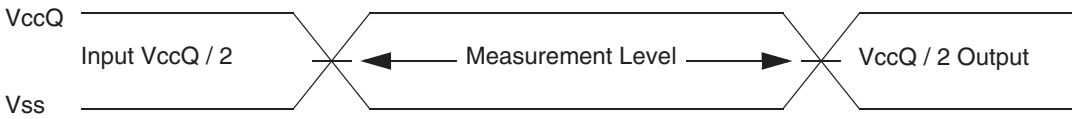


Table 27. Test Specification[47]

Parameter	All Speeds	Units
Output Load Capacitance, C_L	15	pF
Minimum Input Rise and Fall Slew Rates (1.8 V)[46]	1.13	V/ns
Minimum Input Rise and Fall Slew Rates (3.0 V)[46]	2.06	V/ns
Input Pulse Levels	0.0-$V_{CC}Q$	V
Input timing measurement reference levels	$V_{CC}Q/2$	V
Output timing measurement reference levels	$V_{CC}Q/2$	V

Figure 34. Input Waveforms and Measurement Levels[48]



Notes
46. All AC timings assume this input slew rate.
47. Input and output timing is referenced to $V_{CC}Q/2$ or to the crossing of CK/CK#.
48. Input timings for the differential CK/CK# pair are measured from clock crossings.

CLK Characteristics

Figure 35. Clock Characteristics

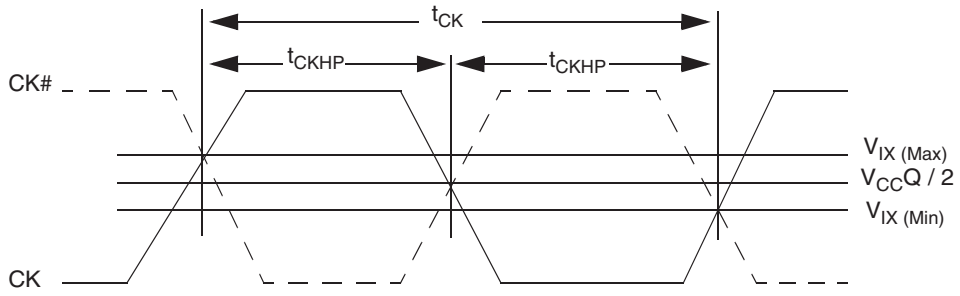


Table 28. Clock Timings[49, 50, 51]

Parameter	Symbol	200 MHZ		166 MHZ		Unit
		Min	Max	Min	Max	
CK Period	t_{CK}	5	–	6	–	ns
CK Half Period - Duty Cycle	t_{CKHP}	0.45	0.55	0.45	0.55	t_{CK}
CK Half Period at Frequency Min = 0.45 t_{CK} Min Max = 0.55 t_{CK} Min	t_{CKHP}	2.25	2.75	2.7	3.3	ns

1. *CK# is only used on the 1.8V device and is shown as a dashed waveform.*
2. The 3V device uses a single ended clock input.

Table 29. Clock AC/DC Electrical Characteristics[52, 53]

Parameter	Symbol	Min	Max	Unit
DC Input Voltage	V_{IN}	–0.3	$V_{CC}Q$ + 0.3	V
DC Input Differential Voltage	$V_{ID(DC)}$	$V_{CC}Q$ x 0.4	$V_{CC}Q$ + 0.6	V
AC Input Differential Voltage	$V_{ID(AC)}$	$V_{CC}Q$ x 0.6	$V_{CC}Q$ + 0.6	V
AC Differential Crossing Voltage	V_{IX}	$V_{CC}Q$ x 0.4	$V_{CC}Q$ x 0.6	V

Notes
49. Clock jitter of ±5% is permitted
50. Minimum Frequency (Maximum tCK) is dependent upon maximum CS# Low time (t_{CSM}), Initial Latency, and Burst Length.
51. CK and CK# input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).
52. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
53. The value of VIX is expected to equal $V_{CC}Q/2$ of the transmitting device and must track variations in the DC level of $V_{CC}Q$.

AC Characteristics

Read Transactions

Table 30. HyperRAM Specific Read Timing Parameters

Parameter	Symbol	200 MHZ		166 MHZ		Unit
		Min	Max	Min	Max	
Chip Select High Between Transactions - 1.8V	t_{CSHI}	6	–	6	–	ns
Chip Select High Between Transactions - 3.0V		6	–	6	–	
HyperRAM Read-Write Recovery Time - 1.8V	t_{RWR}	35	–	36	–	ns
HyperRAM Read-Write Recovery Time - 3.0V		35	–	36	–	
Chip Select Setup to next CK Rising Edge	t_{CSS}	4.0	–	3	–	ns
Data Strobe Valid - 1.8V	t_{DSV}	–	5.0	–	12	ns
Data Strobe Valid - 3.0V		–	6.5	–	12	
Input Setup - 1.8V	t_{IS}	0.5	–	0.6	–	ns
Input Setup - 3.0V		0.5	–	0.6	–	
Input Hold - 1.8V	t_{IH}	0.5	–	0.6	–	ns
Input Hold - 3.0V		0.5	–	0.6	–	
HyperRAM Read Initial Access Time - 1.8V	t_{ACC}	35	–	36	–	ns
HyperRAM Read Initial Access Time- 3.0V		35	–	36	–	
Clock to DQs Low Z	t_{DQLZ}	0	–	0	–	ns
CK transition to DQ Valid - 1.8V	t_{CKD}	1	5.0	1	5.5	ns
CK transition to DQ Valid - 3.0V		1	6.5	1	7	
CK transition to DQ Invalid - 1.8V	t_{CKDI}	0	4.2	0	4.6	ns
CK transition to DQ Invalid - 3.0V		0.5	5.7	0.5	5.6	
Data Valid (t_{DV} min = the lesser of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min) - 1.8V	t_{DV}	1.45	–	1.8	–	ns
Data Valid (t_{DV} min = the lesser of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min) - 3.0V		1.45	–	1.3	–	
CK transition to RWDS Valid - 1.8V	t_{CKDS}	–	5.0	1	5.5	ns
CK transition to RWDS Valid - 3.0V		–	6.5	1	7	
RWDS transition to DQ Valid - 1.8V	t_{DSS}	–0.4	+0.4	–0.45	+0.45	ns
RWDS transition to DQ Valid - 3.0V		–0.4	+0.4	–0.8	+0.8	
RWDS transition to DQ Invalid - 1.8V	t_{DSH}	–0.4	+0.4	–0.45	+0.45	ns
RWDS transition to DQ Invalid - 3.0V		–0.4	+0.4	–0.8	+0.8	
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	0	–	ns
Chip Select Inactive to RWDS High-Z - 1.8V	t_{DSZ}	–	5.0	–	6	ns
Chip Select Inactive to RWDS High-Z - 3.0V		–	6.5	–	7	
Chip Select Inactive to DQ High-Z - 1.8V	t_{OZ}	–	5	–	6	ns
Chip Select Inactive to DQ High-Z - 3.0V		–	6.5	–	7	
Refresh Time - 1.8V	t_{RFH}	35	–	36	–	ns
Refresh Time - 3.0V		35	–	36	–	
CK transition to RWDS Low @CA phase @Read - 1.8V	t_{CKDSR}	1	5.5	1	5.5	ns
CK transition to RWDS Low @CA phase @Read - 3.0V		1	7	1	7	

Figure 36. Read Timing Diagram — No Additional Latency Required

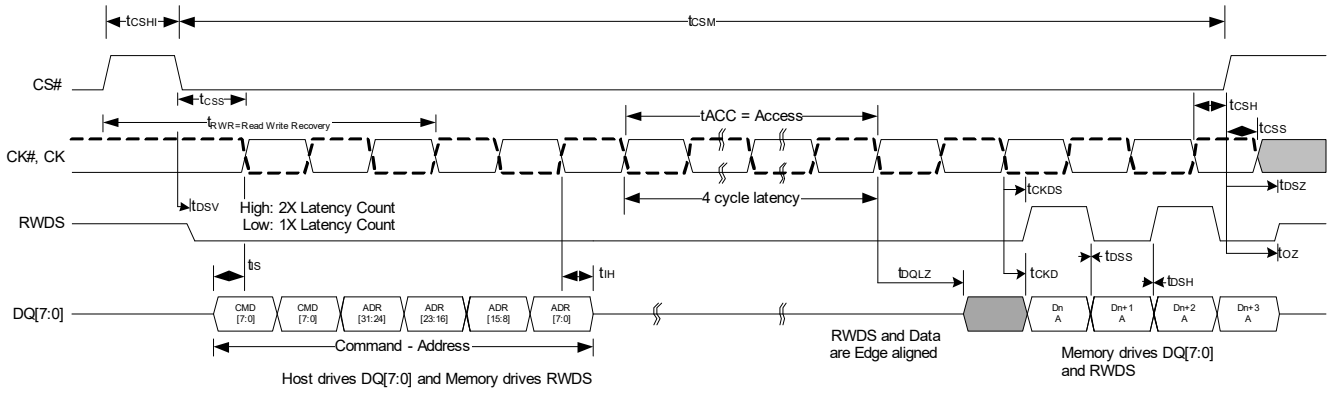
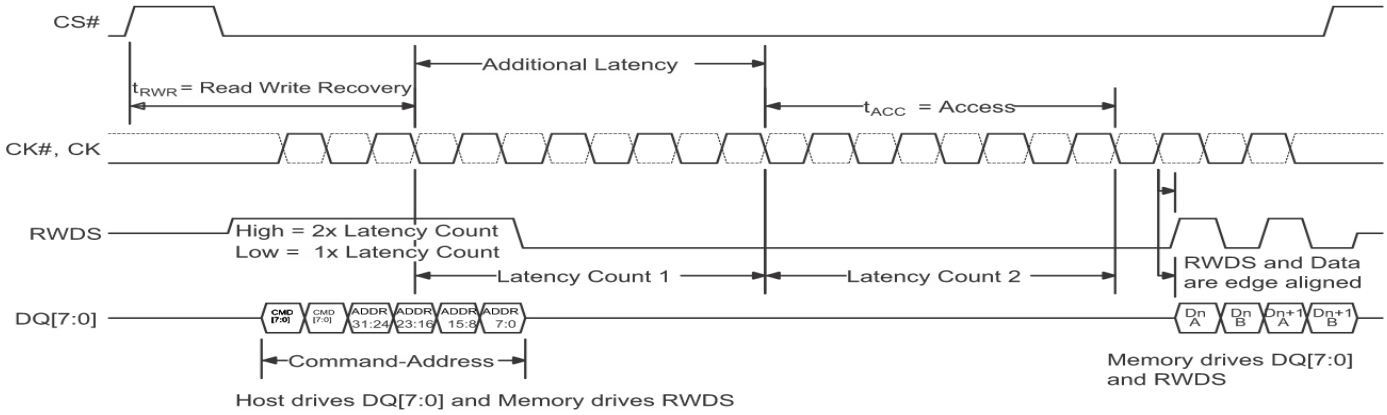


Figure 37. Read Timing Diagram — With Additional Latency Required

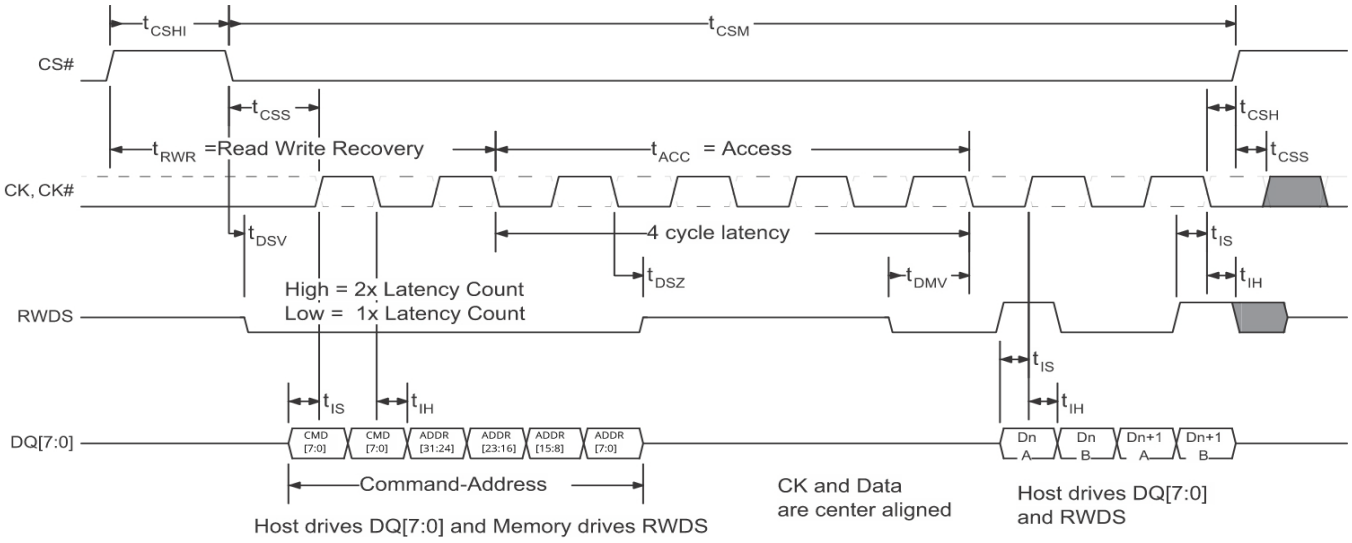


Write Transactions

Table 31. Write Timing Parameters

Parameter	Symbol	200 MHz		166 MHz		Unit
		Min	Max	Min	Max	
Read-Write Recovery Time	t_{RWR}	35	–	36	–	ns
Access Time	t_{ACC}	35	–	36	–	ns
Refresh Time	t_{RFH}	35	–	36	–	ns
Chip Select Maximum Low Time (85 °C)	t_{CSM}	–	4	–	4	µs
Chip Select Maximum Low Time (105 °C)	t_{CSM}	–	1	–	1	µs
RWDS Data Mask Valid	t_{DMV}	0	–	0	–	µs

Figure 38. Write Timing Diagram — No Additional Latency

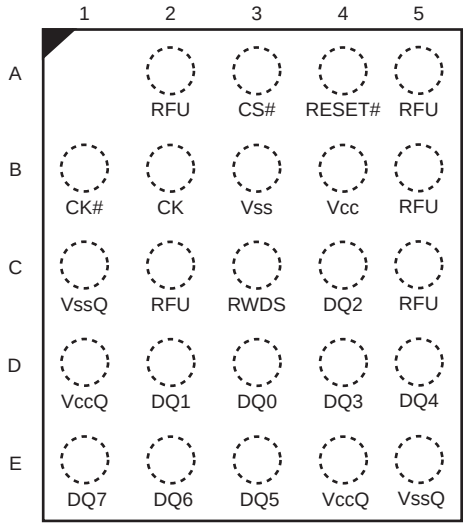


Physical Interface

FBGA 24-Ball 5 x 5 Array Footprint

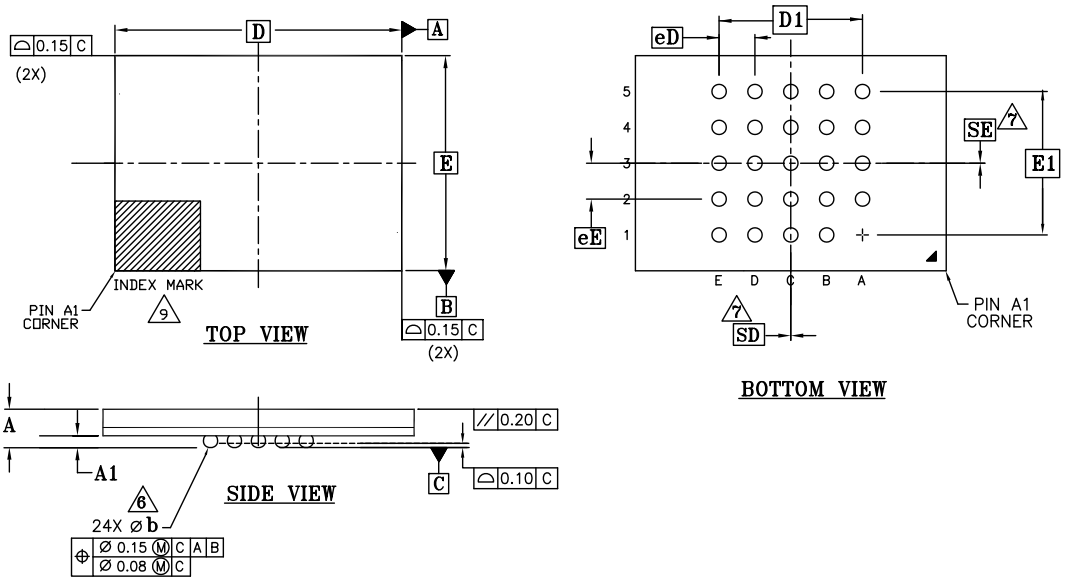
HyperRAM devices are provided in Fortified Ball Grid Array (FBGA), 1 mm pitch, 24-ball, 5 x 5 ball array footprint, with 6mm x 8mm body.

Figure 39. 24-Ball FBGA, 6 x 8 mm, 5 x 5 Ball Footprint, Top View



Physical Diagrams

Figure 40. Fortified Ball Grid Array 24-ball 6 x 8 x 1.0 mm (VAA024)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
Ø b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

002-15550 *A

DDR Center-Aligned Read Strobe (DCARS) Functionality

The HyperRAM device offers an optional feature that enables independent skewing (phase shifting) of the RWDS signal with respect to the read data outputs. This feature is provided in certain devices, based on the Ordering Part Number (OPN).

When the DCARS feature is provided, a second differential Phase Shifted Clock input PSC/PSC# is used as the reference for RWDS edges instead of CK/CK#. The second clock is generally a copy of CK/CK# that is phase shifted 90 degrees to place the RWDS edges centered within the DQ signals valid data window. However, other degrees of phase shift between CK/CK# and PSC/PSC# may be used to optimize the position of RWDS edges within the DQ signals valid data window so that RWDS provides the desired amount of data setup and hold time in relation to RWDS edges.

PSC/PSC# is not used during a write transaction. PSC and PSC# may be driven LOW and HIGH respectively or, both may be driven LOW during write transactions.

The PSC/PSC# is used in xSPI (Octal) devices. If single-ended mode is selected, then PSC# must be driven LOW but must not be left floating (leakage concerns).

xSPI HyperRAM Products with DCARS Signal Descriptions

Figure 41. xSPI Product with DCARS Signal Diagram

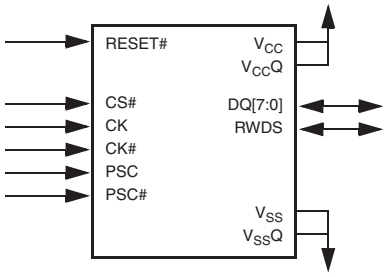
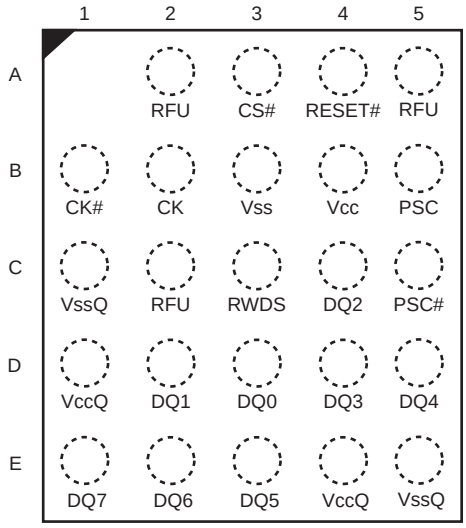


Table 32. Signal Description

Symbol	Type	Description
CS#	Input	**Chip Select.** xSPI transactions are initiated with a HIGH to LOW transition. xSPI transactions are terminated with a LOW to HIGH transition.
CK, CK#	Input	**Differential Clock**. Command, address, and data information is output with respect to the crossing of the CK and CK# signals. Use of differential clock is optional. **Single Ended Clock.** CK# is not used, only a single ended CK is used. The clock is not required to be free-running.
PSC, PSC#	Input	**Phase Shifted Clock.** PSC/PSC# allows independent skewing of the RWDS signal with respect to the CK/CK# inputs. If the CK/CK# (differential mode) is configured, then PSC/PSC# are used. Otherwise, only PSC is used (Single Ended). PSC (and PSC#) may be driven HIGH and LOW respectively or both may be driven LOW during write transactions.
RWDS	Output	**Read-Write Data Strobe.** Data bytes output during read transactions are aligned with RWDS based on the phase shift from CK, CK# to PSC, PSC#. PSC, PSC# cause the transitions of RWDS, thus the phase shift from CK, CK# to PSC, PSC# is used to place RWDS edges within the data valid window. RWDS is an input during write transactions to function as a data mask. At the beginning of all bus transactions RWDS is an output and indicates whether additional initial latency count is required (1 = additional latency count, 0 = no additional latency count).
DQ[7:0]	Input/Output	**Data Input/Output.** CA/Data information is transferred on these DQs during Read and Write transactions.
RESET#	Input	**Hardware RESET**. When LOW, the device will self initialize and return to the idle state. RWDS and DQ[7:0] are placed into the HIGH-Z state when RESET# is LOW. RESET# includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the HIGH state.
V_{CC}	Power Supply	**Array Power.**
$V_{CC}Q$	Power Supply	**Input/Output Power.**
V_{SS}	Power Supply	**Array Ground.**
$V_{SS}Q$	Power Supply	**Input/Output Ground.**

HyperRAM Products with DCARS — FBGA 24-ball, 5 x 5 Array Footprint

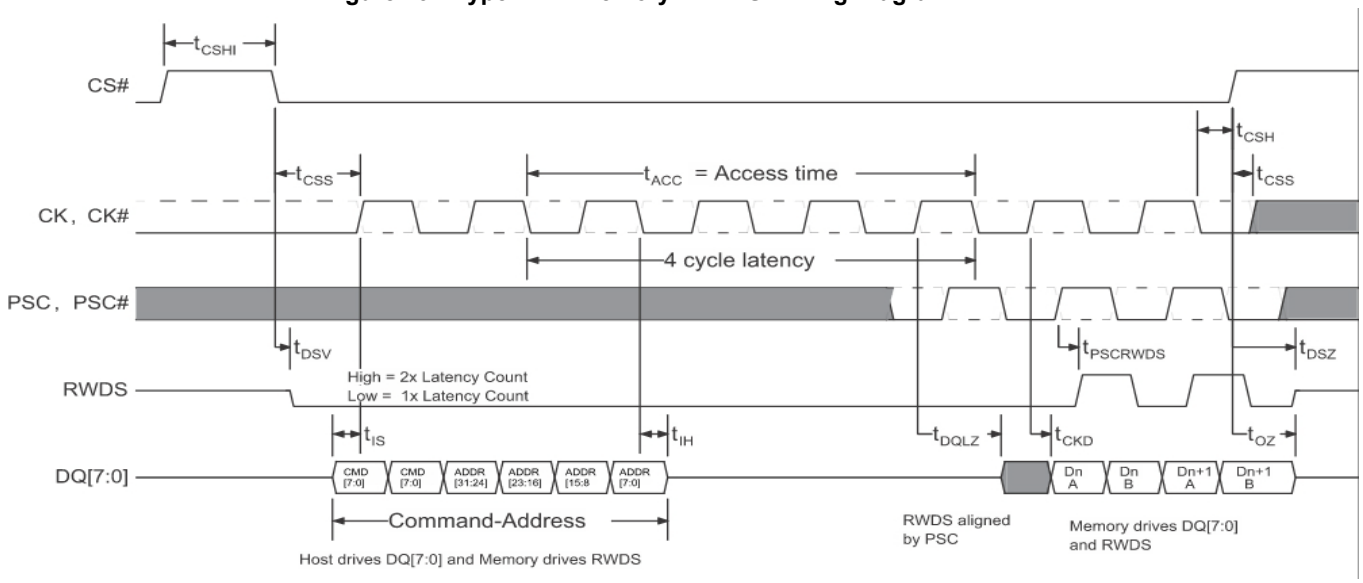
Figure 42. 24-ball FBGA, 5 x 5 Ball Footprint, Top View



HyperRAM Memory with DCARS Timing

The illustrations and parameters shown here are only those needed to define the DCARS feature and show the relationship between the Phase Shifted Clock, RWDS, and data.

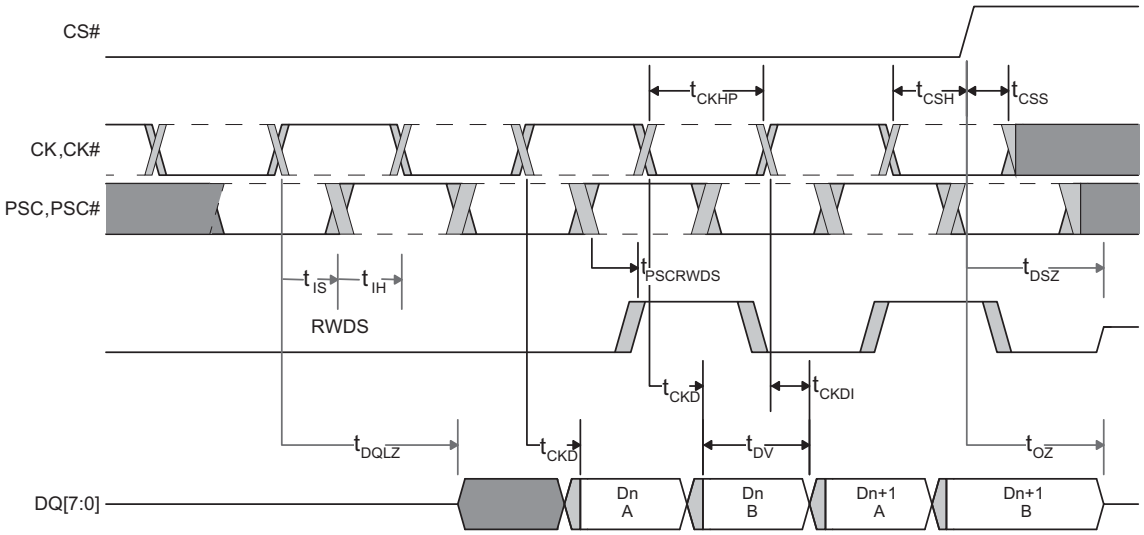
Figure 43. HyperRAM Memory DCARS Timing Diagram[54, 55, 56]



Notes

54. Transactions must be initiated with CK = LOW and CK# = HIGH. CS# must return HIGH before a new transaction is initiated.
55. The memory drives RWDS during read transactions.
56. This example demonstrates a latency code setting of four clocks and no additional initial latency required.

Figure 44. DCARS Data Valid Timing[57, 58, 59, 60]



RWDS and Data are driven by the memory

Table 33. DCARS Read Timing

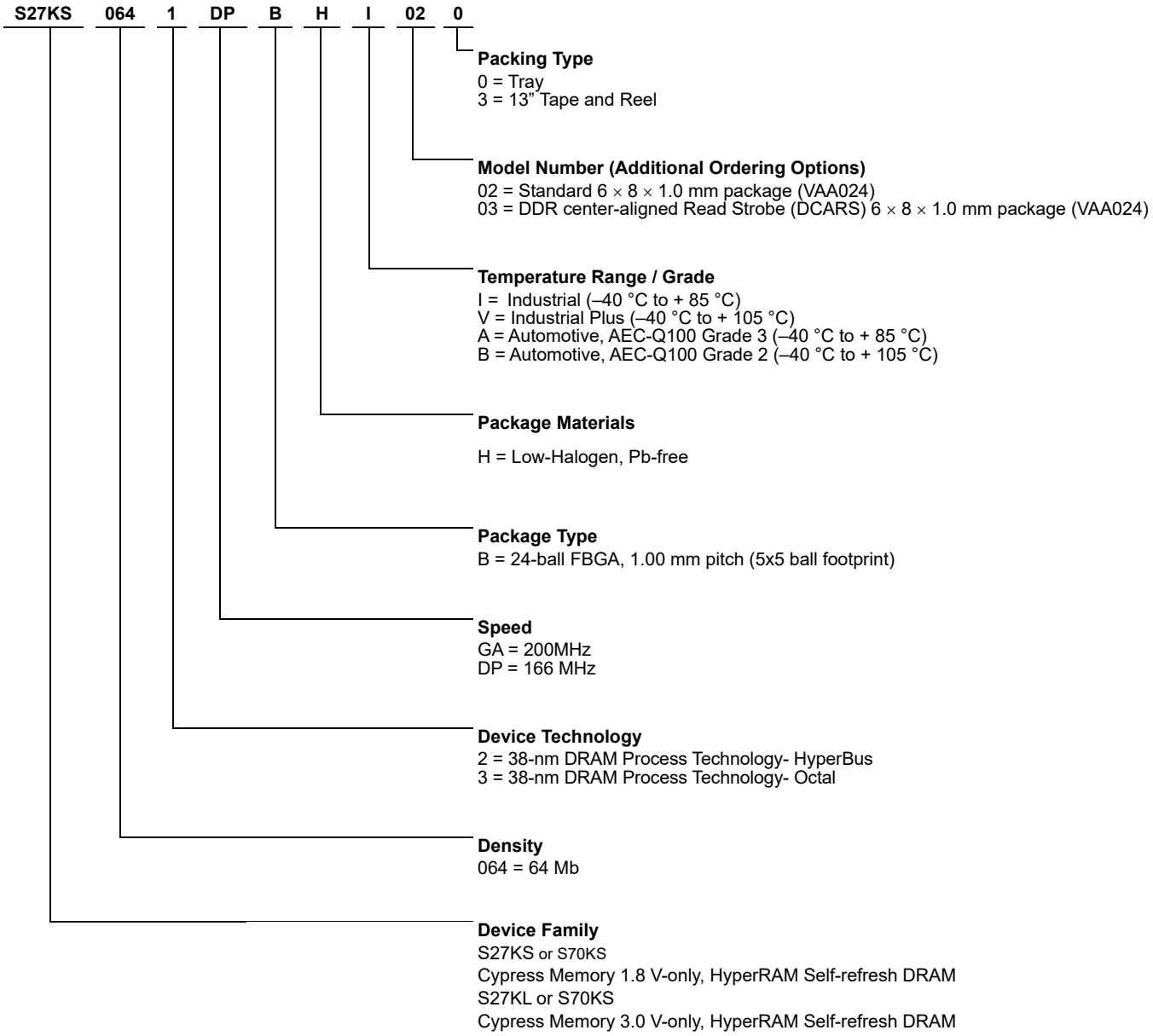
Parameter	Symbol	200 MHZ		166 MHZ		Unit
		Min	Max	Min	Max	
Input Setup - CK/CK# setup w.r.t PSC/PSC# (edge to edge)	t_{IS}	0.5	–	0.6	–	ns
CK Half Period - Duty Cycle (edge to edge)	t_{IH}	0.5	–	0.6	–	ns
HyperRAM PSC transition to RWDS transition	$t_{PSCRWDS}$	–	5	–	6.5	ns
Time delta between CK to DQ valid and PSC to RWDS[61]	$t_{PSCRWDS} - t_{CKD}$	–1.0	+0.5	–1.0	+0.5	ns

Notes
57. Transactions must be initiated with CK = LOW and CK# = HIGH. CS# must return HIGH before a new transaction is initiated.
58. This figure shows a closer view of the data transfer portion of Figure 41 in order to more clearly show the Data Valid period as affected by clock jitter and clock to output delay uncertainty.
59. The delay (phase shift) from CK to PSC is controlled by the xSPI master interface (Host) and is generally between 40 and 140 degrees in order to place the RWDS edge within the data valid window with sufficient set-up and hold time of data to RWDS. The requirements for data set-up and hold time to RWDS are determined by the xSPI master interface design and are not addressed by the xSPI slave timing parameters.
60. The xSPI timing parameters of t_{CKD}, and t_{CKDI} define the beginning and end position of the data valid period. The t_{CKD} and t_{CKDI} values track together (vary by the same ratio) because RWDS and Data are outputs from the same device under the same voltage and temperature conditions.
61. Sampled, not 100% tested.

Ordering Information

Ordering Part Number

The ordering part number is formed by a valid combination of the following:



Valid Combinations

The Recommended Combinations table lists configurations planned to be available in volume. Table 34 and Table 35 will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Table 34. Valid Combinations — Standard

Device Family	Density	Technology	Speed	Package, Material, and Temperature	Model Number	Packing Type	Ordering Part Number	Package Marking
S27KL	064	3	DP	BHI	02	0	S27KL0643BPBHI020	7KL0643BPHI02
S27KL	064	3	GA	BHI	02	0	S27KL0643GABHI020	7KL0643GAHI02
S27KL	064	3	GA	BHI	02	0	S27KL0643GABHI020	7KL0643GAHI02
S27KL	064	3	DP	BHI	02	3	S27KL0643BPBHI023	7KL0643BPHI02
S27KL	064	3	DP	BHV	02	0	S27KL0643BPBHV020	7KL0643BPHV02
S27KL	064	3	DP	BHV	02	3	S27KL0643GABHI023	7KL0643GAHI02
S27KS	064	3	GA	BHI	02	0	S27KS0643GABHI020	7KS0643GAHI02
S27KS	064	3	GA	BHI	02	3	S27KS0643GABHI023	7KS0643GAHI02
S27KS	064	3	GA	BHV	02	0	S27KS0643GABHV020	7KS0643GAHV02
S27KS	064	3	GA	BHV	02	3	S27KS0643GABHV023	7KS0643GAHV02

Table 35. Valid Combinations — DCARS

Device Family	Density	Technology	Speed	Package, Material, and Temperature	Model Number	Packing Type	Ordering Part Number	Package Marking
S27KL	064	3	DP	BHI	03	0	S27KL0643DPBHI030	7KL0643DPHI03
S27KL	064	3	DP	BHI	03	3	S27KL0643DPBHI033	7KL0643DPHI03
S27KL	064	3	DP	BHV	03	0	S27KL0643DPBHV030	7KL0643DPHV03
S27KL	064	3	DP	BHV	03	3	S27KL0643DPBHV033	7KL0643DPHV03
S27KS	064	3	GA	BHI	03	0	S27KS0643GABHI030	7KS0643GAHI03
S27KS	064	3	GA	BHI	03	3	S27KS0643GABHI033	7KS0643GAHI03
S27KS	064	3	GA	BHV	03	0	S27KS0643GABHV030	7KS0643GAHV03
S27KS	064	3	GA	BHV	03	3	S27KS0643GABHV033	7KS0643GAHV03

Valid Combinations — Automotive Grade / AEC-Q100

Table 36 and Table 37 lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 36. Valid Combinations — Automotive Grade / AEC-Q100

Device Family	Density	Technology	Speed	Package, Material, and Temperature	Model Number	Packing Type	Ordering Part Number	Package Marking
S27KL	064	3	DP	BHA	02	0	S27KL0643DPBHA020	7KL0643DPHA02
S27KL	064	3	DP	BHA	02	3	S27KL0643DPBHA023	7KL0643DPHA02
S27KL	064	3	DP	BHB	02	0	S27KL0643DPBHB020	7KL0643DPHB02
S27KL	064	3	DP	BHB	02	3	S27KL0643DPBHB023	7KL0643DPHB02
S27KL	064	3	GA	BHB	02	3	S27KL0643DPBHB023	7KL0643DPHB02
S27KL	064	3	GA	BHB	02	3	S27KL0643GABHB023	7KL0643GABHB02
S27KS	064	3	GA	BHA	02	0	S27KS0643GABHA020	7KS0643GAHA02
S27KS	064	3	GA	BHA	02	3	S27KS0643GABHA023	7KS0643GAHA02
S27KS	064	3	GA	BHB	02	0	S27KL0643GABHB020	7KL0643GABHB02
S27KS	064	3	GA	BHB	02	3	S27KS0643GABHB023	7KS0643GAHB02

Table 37. Valid Combinations — DCARS Automotive Grade / AEC-Q100

Device Family	Density	Technology	Speed	Package, Material, and Temperature	Model Number	Packing Type	Ordering Part Number	Package Marking
S27KL	064	3	DP	BHA	03	0	S27KL0643DPBHA030	7KL0643DPHA03
S27KL	064	3	DP	BHA	03	3	S27KL0643DPBHA033	7KL0643DPHA03
S27KL	064	3	DP	BHB	03	0	S27KL0643DPBHB030	7KL0643DPHB03
S27KL	064	3	DP	BHB	03	3	S27KL0643DPBHB033	7KL0643DPHB03
S27KS	064	3	GA	BHA	03	0	S27KS0643GABHA030	7KS0643GAHA03
S27KS	064	3	GA	BHA	03	3	S27KS0643GABHA033	7KS0643GAHA03
S27KS	064	3	GA	BHB	03	0	S27KS0643GABHB030	7KS0643GAHB03
S27KS	064	3	GA	BHB	03	3	S27KS0643GABHB033	7KS0643GAHB03

Acronyms

Table 38. Acronyms Used in this Document

Acronym	Description
CMOS	complementary metal oxide semiconductor
DCARS	DDR Center-Aligned Read Strobe
DDR	double data rate
DPD	deep power down
DRAM	dynamic RAM
HS	hybrid sleep
MSb	most significant bit
POR	power-on reset
PSRAM	pseudo static RAM
PVT	process, voltage, and temperature
RWDS	read-write data strobe
SPI	serial peripheral interface
xSPI	expanded serial peripheral interface

Document Conventions

Units of Measure

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Revision History

Document Title: S27KL0643/S27KS0643, 3.0 V/1.8 V, 64 Mb (8 MB), HyperRAM Self-Refresh DRAM Document Number: 002-24693			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*D	6713022	11/25/2019	Changed document status to Final.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for DRAM ***category:***

Click to view products by Cypress ***manufacturer:***

Other Similar products are found below :

CT51264BF160B M366S0924FTS-C7A00 AS4C16M32MD1-5BCN HM514100AZ-80 K4S560432C-TC75 K4S641632H-UC60 AS4C16M32MD1-5BIN AS4C64M8D1-5TCN ATCA-7360-MEM-4G MN41C4256A-07 IS43LR16800G-6BLI MT48LC8M16A2F4-6A IT:L DEMT46H128M16LFCK6ITA W972GG6KB-25 TR W97AH2KBVX2I IS43LD16640C-25BLI AS4C64M16D1A-6TCN AS4C256M8D2-25BIN AS4C64M8D1-5BCN MT52L256M32D1PF-107 WT:B TR AS4C128M16MD2-25BCN AS4C8M16D1-5BCN AS4C64M32MD2-25BCN AS4C128M16MD2A-25BIN AS4C128M32MD2-18BCN AS4C32M32MD2-25BCN IS43LR16800G-6BL W971GG6SB-18 AS4C64M16D3B-12BINTR MT44K16M36RB-125E:A TR MT44K16M36RB-107E:A TR AS4C128M8D2A-25BIN AS4C128M8D2A-25BCN NT5AD256M16D4-HR AS4C256M16D3C-93BCN AS4C128M16D3LC-12BIN AS4C128M16D3LC-12BCN AS4C64M32MD1A-5BIN MT40A512M8SA-062E:F TR IS45S32800J-7TLA2 AS4C256M16D3LC-12BCN AS4C16M16SB-6TIN AS4C16M16SB-7TCN K4B2G1646F-BCNB AS4C2M32SA-6TINTR AS4C16M16SB-6BIN IS46TR16640CL-125JBLA2-TR MT48LC64M8A2P-75:C TR MT40A2G8JC-062E IT:E MT40A1G16KH-062E AIT:E