

# S29GL-A MirrorBit® Flash Family

**S29GL064A, S29GL032A, and S29GL016A**  
**64 Megabit, 32 Megabit, and 16 Megabit**  
**3.0-Volt only Page Mode Flash Memory**  
**Featuring 200 nm MirrorBit Process Technology**



## *Data Sheet*

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This product family has been retired and is not recommended for designs. For new and current designs, the S29AL016J, S29GL032N, and S29GL064N supersede S29GL016A, S29GL032A, and S29GL064A respectively. These are the factory-recommended migration paths. Please refer to the S29AL016J, S29GL032N, and S29GL064N data sheets for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

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## Distinctive Characteristics

### Architectural Advantages

- **Single power supply operation**
  - 3-Volt read, erase, and program operations
- **Manufactured on 200 nm MirrorBit process technology**
- **Secured Silicon Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - 64Mb (uniform sector models): 128 32 Kword (64 KB) sectors
  - 64 Mb (boot sector models): 127 32 Kword (64 KB) sectors + 8 4Kword (8KB) boot sectors
  - 32 Mb (uniform sector models): 64 32Kword (64 KB) sectors
  - 32 Mb (boot sector models): 63 32Kword (64 KB) sectors + 8 4Kword (8KB) boot sectors
  - 16 Mb (boot sector models): 31 31Kword (64 KB) sectors + 8 4Kword (8 KB) boot sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **100,000 erase cycles typical per sector**
- **20-year data retention typical**

### Performance Characteristics

- **High performance**
  - 90 ns access time
  - 4-word/8-byte page read buffer
  - 25 ns page read times
  - 16-word/32-byte write buffer which reduces overall programming time for multiple-word updates

- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 18 mA typical active read current
  - 50 mA typical erase/program current
  - 1  $\mu$ A typical standby mode current
- **Package options**
  - 48-pin TSOP
  - 56-pin TSOP
  - 64-ball Fortified BGA
  - 48-ball fine-pitch BGA
  - 56-ball fine pitch BGA (MCP-compatible for cellular handsets)

### Software & Hardware Features

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
  - Unlock Bypass Program command reduces overall multiple-word programming time
- **Hardware features**
  - Sector Group Protection: hardware-level method of preventing write operations within a sector group
  - Temporary Sector Unprotect:  $V_{ID}$ -level method of changing code in locked sectors
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings on uniform sector models
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

## General Description

The S29GL-A family of devices are 3.0-Volt single-power Flash memory manufactured using 200 nm MirrorBit technology. The S29GL064A is a 64-Mb device organized as 4,194,304 words or 8,388,608 bytes. The S29GL032A is a 32-Mb device organized as 2,097,152 words or 4,194,304 bytes. The S29GI016A is a 16-Mb device organized as 1,048,576 words or 2,097,152 bytes. Depending on the model number, the devices have an 8-bit wide data bus only, 16-bit wide data bus only, or a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The devices can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 90 ns are available. Note that each access time has a specific operating voltage range ( $V_{CC}$ ) as specified in the [Product Selector Guide on page 9](#) and the [Ordering Information on page 19](#). Package offerings include 48-pin TSOP, 56-pin TSOP, 48-ball fine-pitch BGA and 64-ball Fortified BGA, depending on model number. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0-Volt power supply** for both read and write functions. In addition to a  $V_{CC}$  input, a high-voltage **accelerated program (ACC)** feature provides shorter programming times through increased current on the WP#/ACC input. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation begins, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

**Hardware data protection** measures include a low  $V_{CC}$  detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses are stable for a specified period of time.

The **Write Protect (WP#)** feature protects the first or last sector by asserting a logic low on the WP#/ACC pin or WP# pin, depending on model number. The protected sector is still protected even during accelerated programming.

The **Secured Silicon Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

Spansion MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

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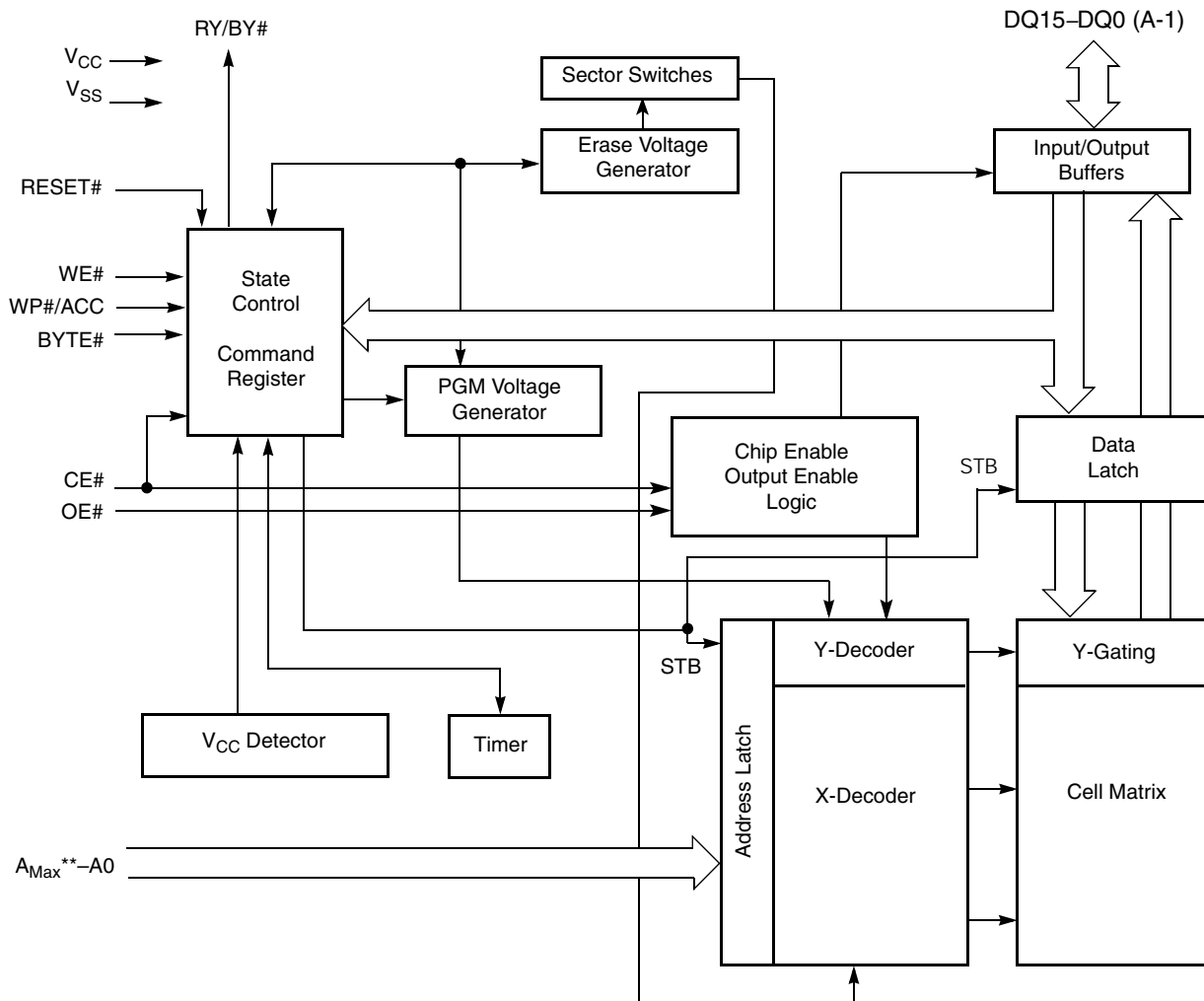


# 1. Product Selector Guide

Table 1.1 S29GL064A, S29GL032A, S29GL016A

| Part Number                | S29GL064A |     |     | S29GL032A |     |     | S29GL016A |     |
|----------------------------|-----------|-----|-----|-----------|-----|-----|-----------|-----|
| Speed Option               | 90        | 10  | 11  | 90        | 10  | 11  | 90        | 10  |
| Max. Access Time (ns)      | 90        | 100 | 110 | 90        | 100 | 110 | 90        | 100 |
| Max. CE# Access Time (ns)  | 90        | 100 | 110 | 90        | 100 | 110 | 90        | 100 |
| Max. Page Access Time (ns) | 25        | 30  | 30  | 25        | 30  | 30  | 25        | 30  |
| Max. OE# Access Time (ns)  | 25        | 30  | 30  | 25        | 30  | 30  | 25        | 30  |

# 2. Block Diagram



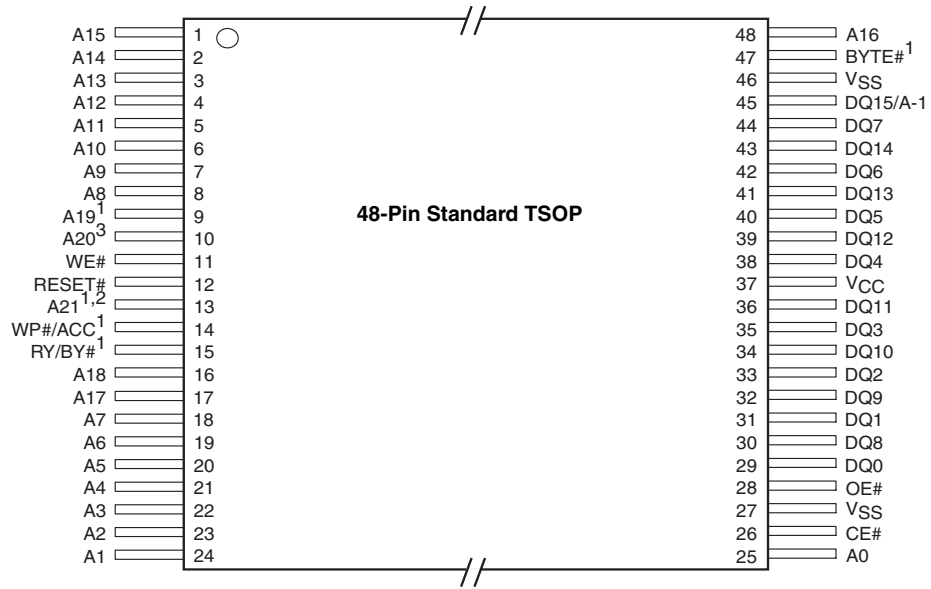
**Note**  
 \*\*A<sub>MAX</sub> GL064A = A21.  
 \*\*A<sub>MAX</sub> GL032A = A20.  
 \*\*A<sub>MAX</sub> GL016A = A19.

### 3. Connection Diagrams

#### 3.1 Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP and BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Figure 3.1 48-Pin Standard TSOP



**Notes**

1. Pin 9 is A21, Pin 13 is ACC, Pin 14 is WP#, Pin 15 is A19, and Pin 47 is V<sub>IO</sub> on S29GL064A (models R6, R7).
2. Pin 13 is NC on S29GL032A, and S29GL016A.
3. Pin 10 is NC on S29GL016A.

Figure 3.2 56-Pin Standard TSOP

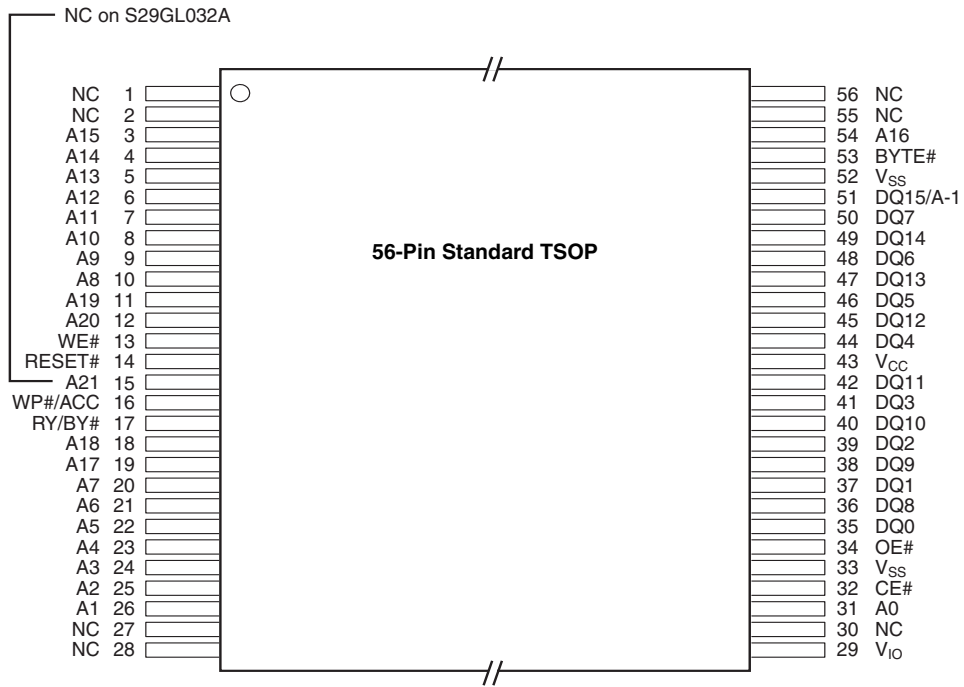
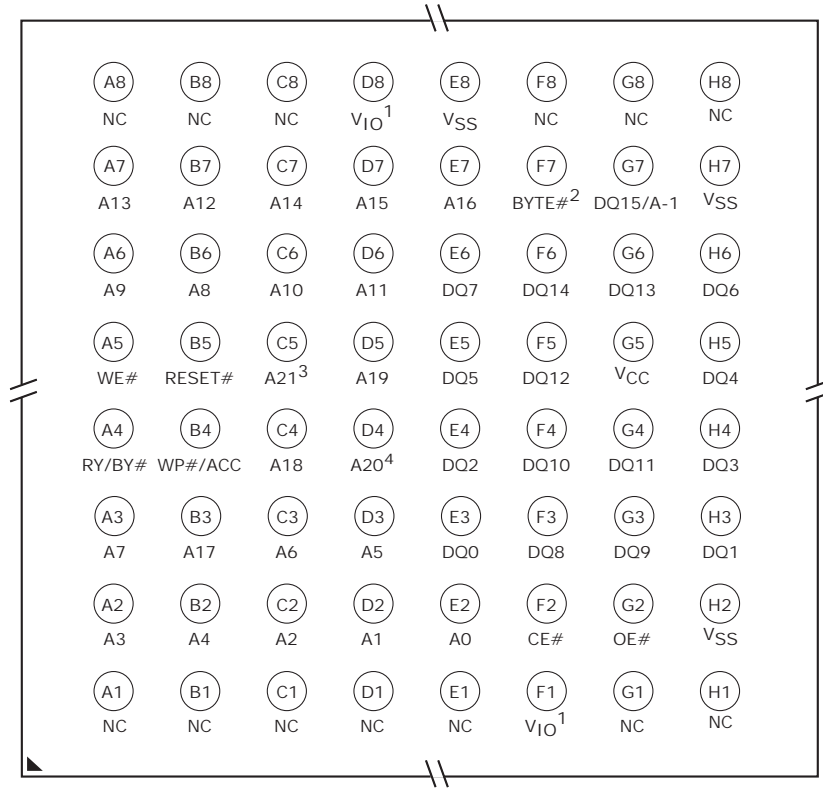


Figure 3.3 64-ball Fortified BGA

64-ball Fortified BGA  
Top View, Balls Facing Down

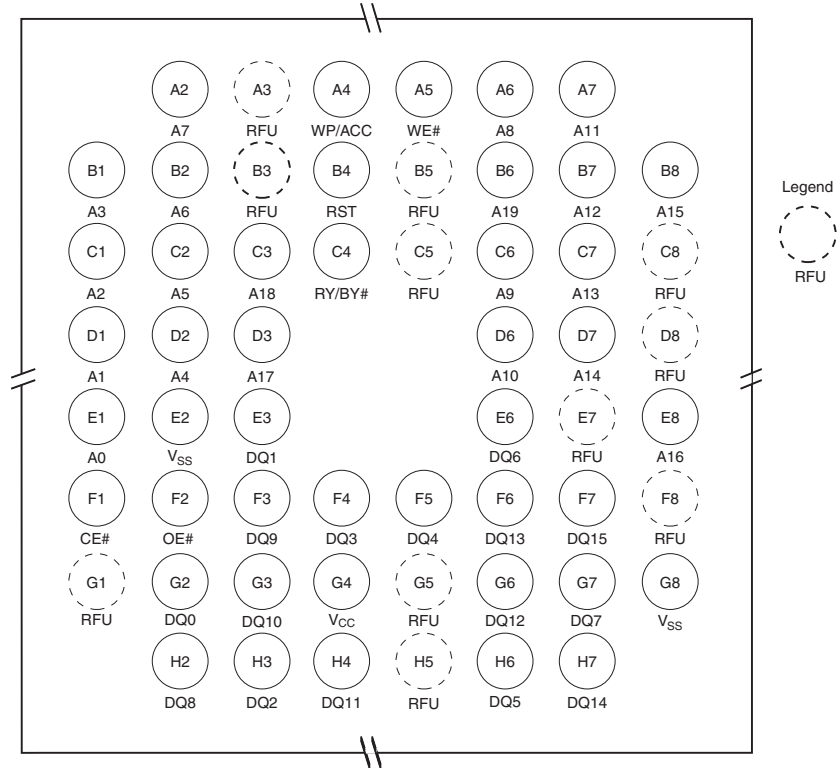


**Notes**

1. Ball D8 and Ball F1 are NC on S29GL064A (models R3, R4) and S29GL016A (Models 01, 02, R1, R2).
2. Ball F7 is NC on S29GL064A (model R5).
3. Ball C5 is NC on S29GL032A and S29GL016A.
4. Ball D4 is NC on S29GL016A.

**Figure 3.4** 56-Ball Fine-Pitch Ball Grid Array

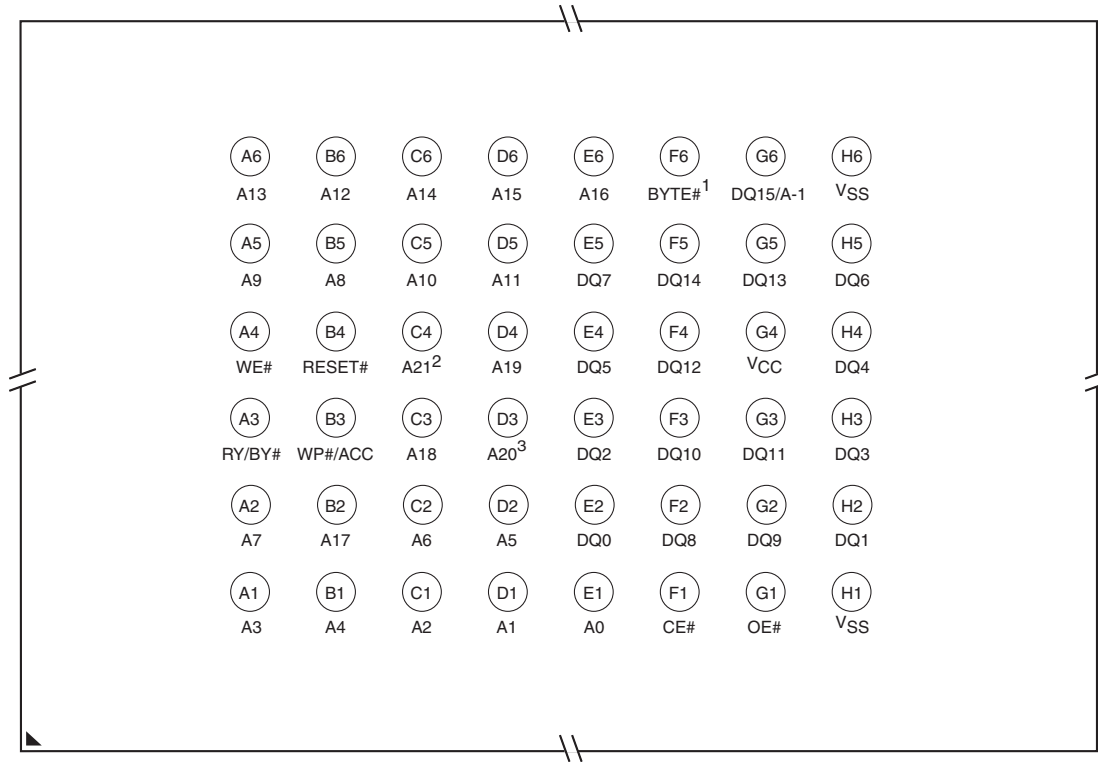
**56-Ball Fine-Pitch Ball Grid Array**  
Top View, Balls Facing Down



**Note**  
MCP-compatible Connection Diagram for cellular handsets only.

Figure 3.5 48-ball Fine-pitch BGA

48-ball Fine-pitch BGA  
Top View, Balls Facing Down



**Notes**

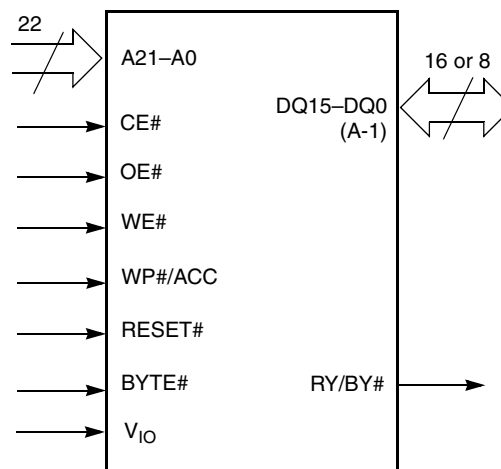
1. Ball F6 is  $V_{IO}$  on S29GL064A (model R5).
2. Ball C4 is NC on S29GL032A and S29GL016A.
3. Ball D3 is NC on S29GL016A.

## 4. Pin Descriptions

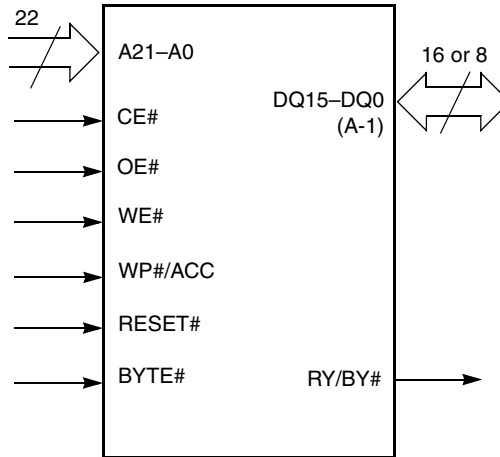
|                 |   |
|-----------------|---|
| A21–A0          | 22 Address inputs   |
| A20–A0          | 21 Address inputs   |
| A19–A0          | 20 Address inputs   |
| DQ7–DQ0         | 8 Data inputs/outputs   |
| DQ14–DQ0        | 15 Data inputs/outputs  |
| DQ15/A-1        | DQ15 (Data input/output, word mode), A-1 (LSB Address input, byte mode)   |
| CE#             | Chip Enable input   |
| OE#             | Output Enable input   |
| WE#             | Write Enable input  |
| WP#/ACC         | Hardware Write Protect input/Programming Acceleration input   |
| ACC             | Acceleration input  |
| WP#             | Hardware Write Protect input  |
| RESET#          | Hardware Reset Pin input  |
| RY/BY#          | Ready/Busy output   |
| BYTE#           | Selects 8-bit or 16-bit mode  |
| V <sub>CC</sub> | 3.0 volt-only single power supply<br>(See <a href="#">Product Selector Guide on page 9</a> for speed options and voltage supply tolerances) |
| V <sub>SS</sub> | Device Ground   |
| NC              | Pin Not Connected Internally  |
| V <sub>IO</sub> | Output Buffer Power   |

## 5. Logic Symbols

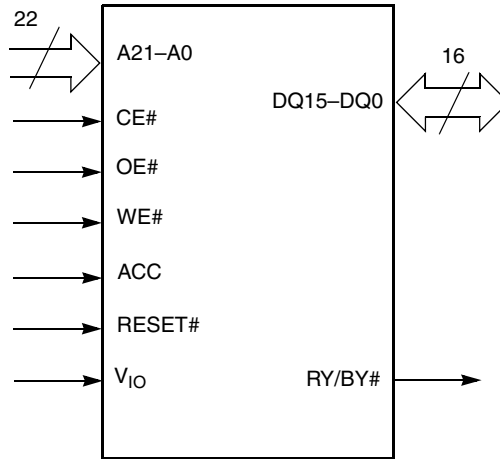
### 5.1 Logic Symbol–S29GL064A (Models R1, R2, R8, R9)



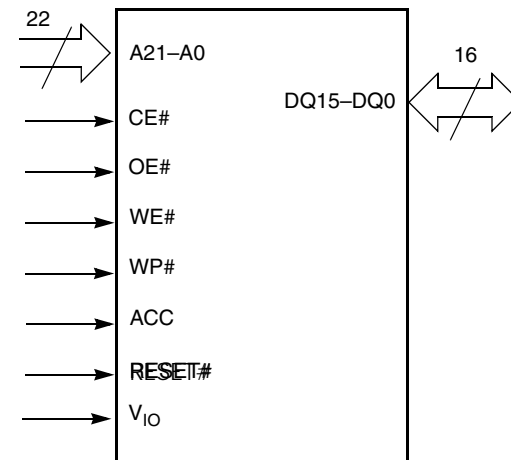
### 5.2 Logic Symbol–S29GL064A (Models R3, R4)



### 5.3 Logic Symbol–S29GL064A (Model R5)

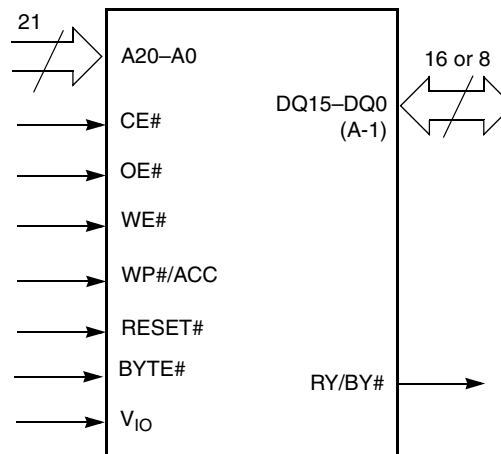


### 5.4 Logic Symbol–S29GL064A (Models R6, R7)

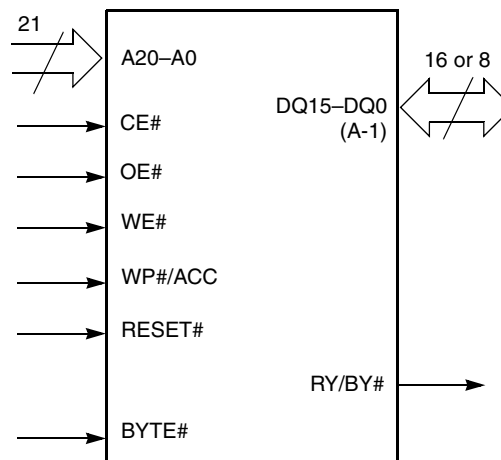




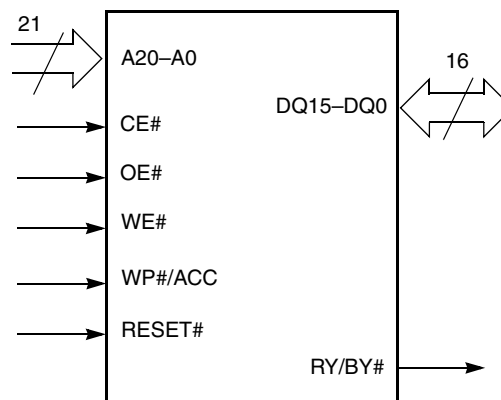
### 5.5 Logic Symbol–S29GL032A (Models R1, R2)



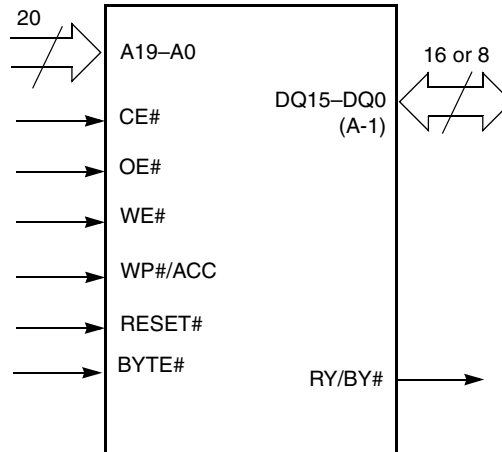
### 5.6 Logic Symbol–S29GL032A (Models R3, R4)



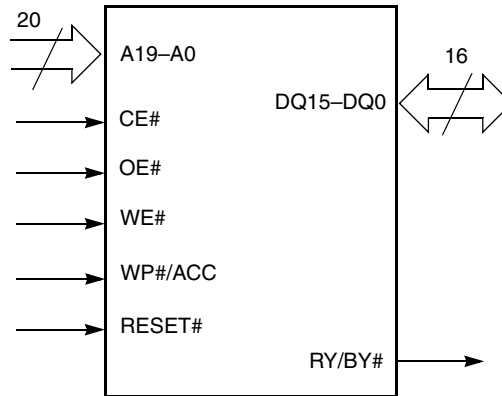
### 5.7 Logic Symbol–S29GL032A (Models W3, W4)



### 5.8 Logic Symbol–S29GL016A (Models R1, R2)



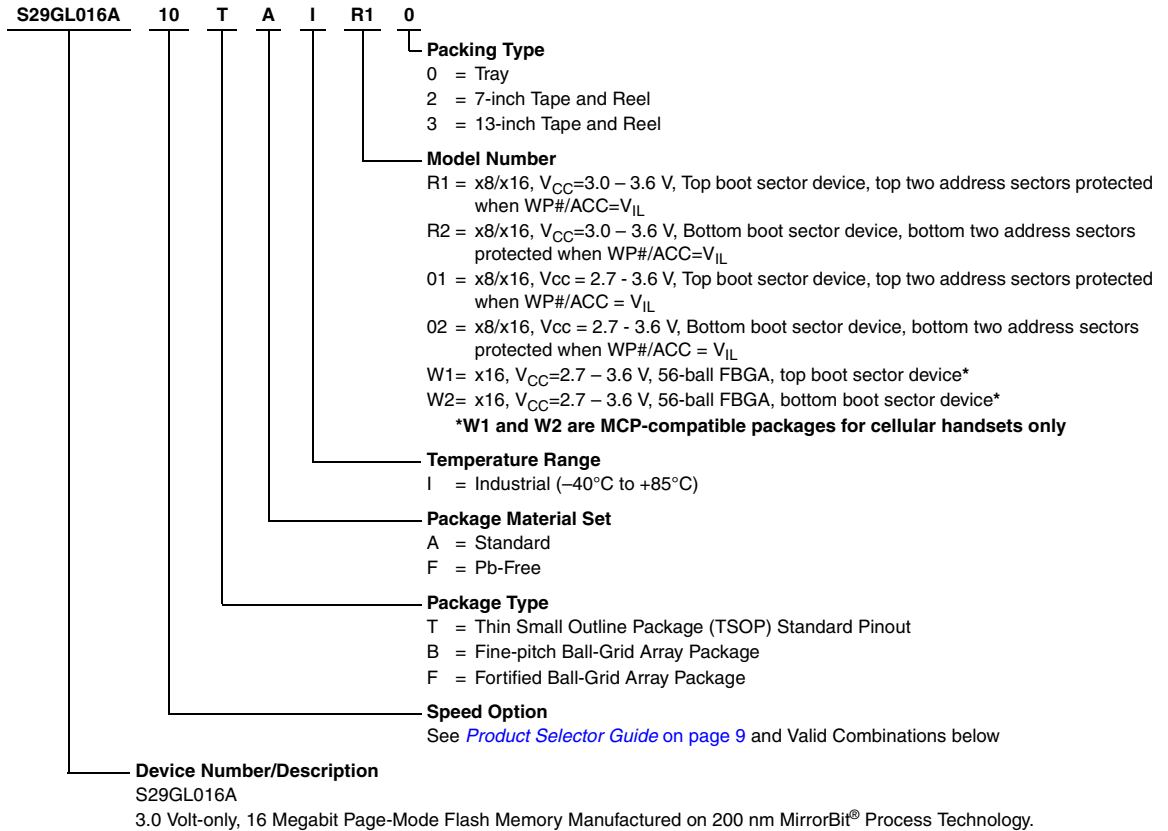
### 5.9 Logic Symbol–S29GL016A (Models W1, W2)



## 6. Ordering Information

### 6.1 S29GL016A Standard Products

Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



**Table 6.1 S29GL016A Ordering Options**

| S29GL016A Valid Combinations |              |  |              |                       | Package Description (Notes) |   |
|------------------------------|--------------|--|--------------|-----------------------|-----------------------------|---|
| Device Number                | Speed Option | Package, Material, & Temperature Range | Model Number | Packing Type (Note 1) |                             |   |
| S29GL016A                    | 90, 10       | TAI, TFI                               | R1, R2       | 0, 3                  | TS048 (Note 2)              | TSOP  |
|                              |              | BAI, BFI                               |              | 0, 2, 3               | VBK048 (Note 3)             | Fine-Pitch BGA                              |
|                              |              | FAI, FFI                               |              |                       | LAA064 (Note 3)             | Fortified BGA                               |
|                              | 10           | BAI, BFI                               | W1, W2       |                       | VBU056 (Note 3)             | Fine-Pitch BGA (For cellular handsets only) |
|                              | 10           | TAI, TFI                               | 01, 02       | 0, 3                  | TS048 (Note 2)              | TSOP  |
|                              |              | BAI, BFI                               |              | 0, 2, 3               | VBK048 (Note 3)             | Fine-Pitch BGA                              |
| FAI, FFI                     |              | LAA064 (Note 3)                        |              |                       | Fortified BGA               |   |

**Notes**

- Type 0 is standard. Specify others as required: TSOPs can be packed in Types 0 and 3; BGAs can be packed in Types 0, 2, or 3.
- TSOP package marking omits packing type designator from ordering part number.
- BGA package marking omits leading S29 and packing type designator from ordering part number.

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## 6.2 S29GL032A Standard Products

Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

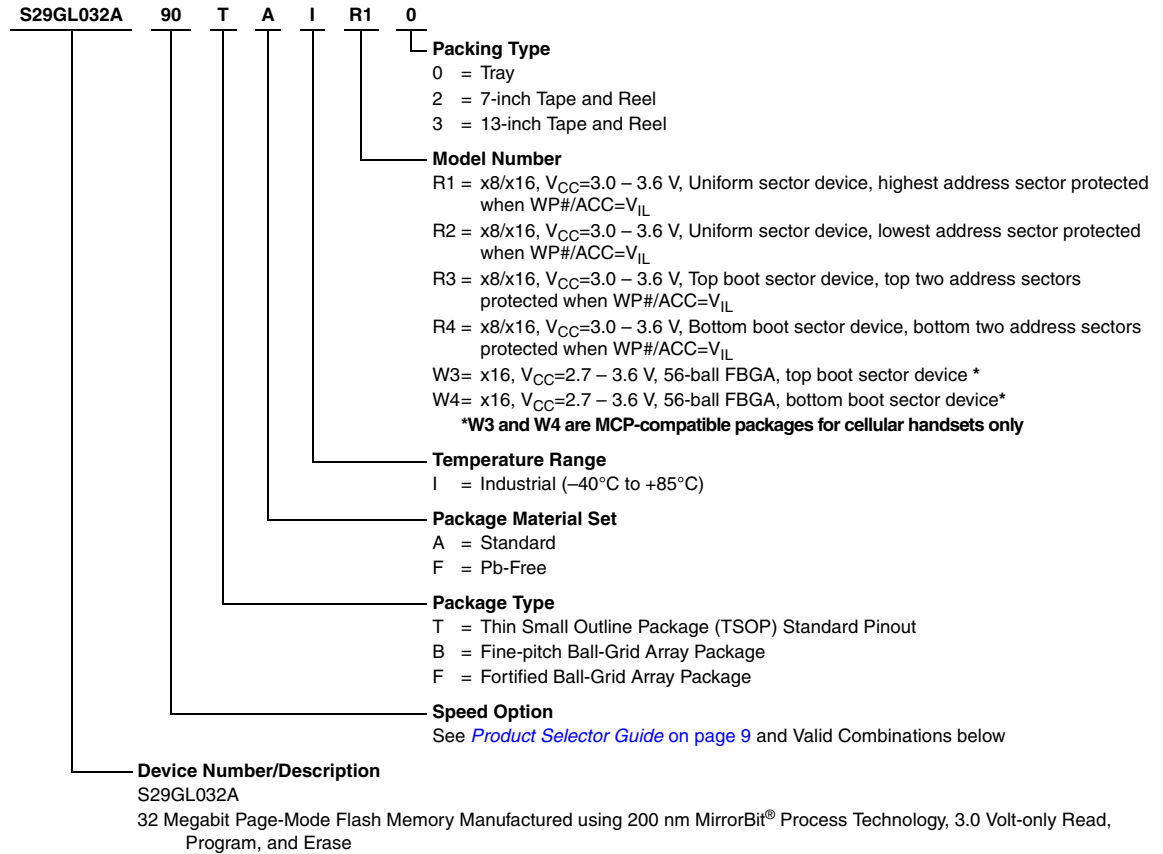


Table 6.2 S29GL032A Ordering Options

| S29GL032A Valid Combinations |              |  |              |                   | Package Description (Notes) |   |
|------------------------------|--------------|--|--------------|-------------------|-----------------------------|---|
| Device Number                | Speed Option | Package, Material, & Temperature Range | Model Number | Packing Type      |                             |   |
| S29GL032A                    | 90, 10, 11   | TAI,TFI                                | R1, R2       | 0,2,3<br>(Note 1) | TS056 (Note 2)              | TSOP  |
|                              |              | FAI,FFI                                |              |                   | LAA064 (Note 3)             | Fortified BGA                               |
|                              |              | TAI,TFI                                | R3,R4        |                   | TS048 (Note 2)              | TSOP  |
|                              |              | BAI,BFI                                |              |                   | VBK048 (Note 3)             | Fine-Pitch BGA                              |
|                              |              | FAI,FFI                                |              |                   | LAA064 (Note 3)             | Fortified BGA                               |
|                              | 10, 11       | BAI,BFI                                | W3,W4        |                   | VBU056 (Note 3)             | Fine-Pitch BGA (For cellular handsets only) |

**Notes**

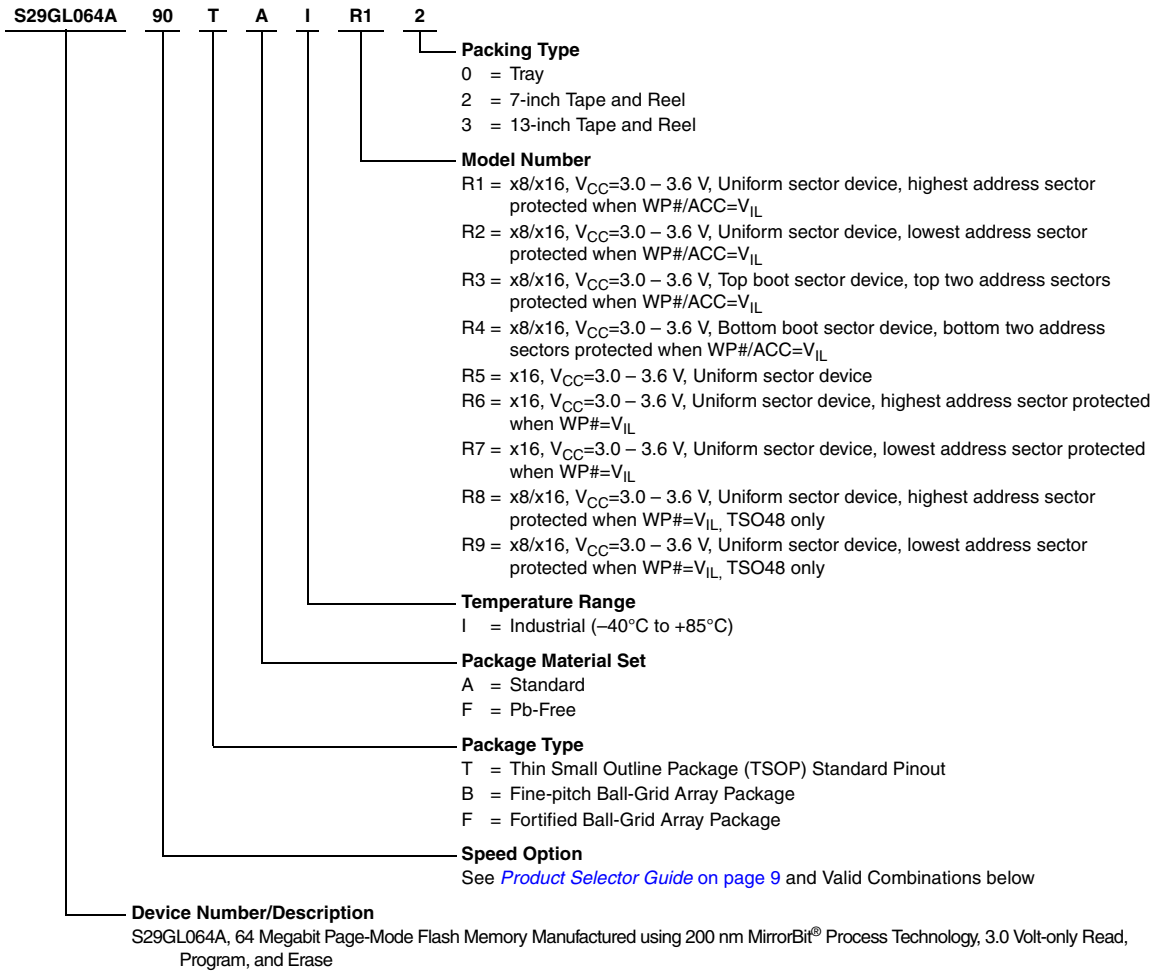
- Type 0 is standard. Specify others as required: TSOPs can be packed in Types 0 and 3; BGAs can be packed in Types 0, 2, or 3.
- TSOP package marking omits packing type designator from ordering part number.
- BGA package marking omits leading S29 and packing type designator from ordering part number.

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

### 6.3 S29GL064A Standard Products

Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



**Table 6.3** S29GL064A Valid Combinations

| S29GL064A Valid Combinations |              |                                       |                        |              | Package Description |                |
|------------------------------|--------------|---------------------------------------|------------------------|--------------|---------------------|----------------|
| Device Number                | Speed Option | Package, Material & Temperature Range | Model Number           | Packing Type |                     |                |
| S29GL064A                    | 90, 10, 11   | TAI, TFI                              | R3, R4, R6, R7, R8, R9 | (Note 1)     | TS048 (Note 2)      | TSOP           |
|                              |              |                                       | R1, R2                 |              | TS056 (Note 2)      | TSOP           |
|                              |              | BAI, BFI                              | R3, R4, R5             |              | VBN048 (Note 3)     | Fine-pitch BGA |
|                              |              | FAI, FFI                              | R1, R2, R3, R4, R5     |              | LAA064 (Note 3)     | Fortified BGA  |

**Notes**

- Type 0 is standard. Specify others as required: TSOPs can be packed in Types 0 and 3; BGAs can be packed in Types 0, 2, or 3.
- TSOP package marking omits packing type designator from ordering part number.
- BGA package marking omits leading S29 and packing type designator from ordering part number.

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## 7. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. [Table 7.1](#) lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

**Table 7.1** Device Bus Operations

| Operation                           | CE#                     | OE# | WE# | RESET#                     | WP#      | ACC             | Addresses<br>(Note 1)                  | DQ0–<br>DQ7      | DQ8–DQ15                   |                                     |
|-------------------------------------|-------------------------|-----|-----|----------------------------|----------|-----------------|--|------------------|----------------------------|-------------------------------------|
|                                     |                         |     |     |                            |          |                 |  |                  | BYTE#<br>= V <sub>IH</sub> | BYTE#<br>= V <sub>IL</sub>          |
| Read                                | L                       | L   | H   | H                          | X        | X               | A <sub>IN</sub>                        | D <sub>OUT</sub> | D <sub>OUT</sub>           | DQ8–DQ14<br>= High-Z,<br>DQ15 = A-1 |
| Write (Program/Erase)               | L                       | H   | L   | H                          | (Note 3) | X               | A <sub>IN</sub>                        | (Note 4)         | (Note 4)                   |                                     |
| Accelerated Program                 | L                       | H   | L   | H                          | (Note 3) | V <sub>HH</sub> | A <sub>IN</sub>                        | (Note 4)         | (Note 4)                   |                                     |
| Standby                             | V <sub>CC</sub> ± 0.3 V | X   | X   | V <sub>CC</sub> ±<br>0.3 V | X        | H               | X                                      | High-Z           | High-Z                     | High-Z                              |
| Output Disable                      | L                       | H   | H   | H                          | X        | X               | X                                      | High-Z           | High-Z                     | High-Z                              |
| Reset                               | X                       | X   | X   | L                          | X        | X               | X                                      | High-Z           | High-Z                     | High-Z                              |
| Sector Group Protect<br>(Note 2)    | L                       | H   | L   | V <sub>ID</sub>            | H        | X               | SA, A6=L,<br>A3=L, A2=L,<br>A1=H, A0=L | (Note 4)         | X                          | X                                   |
| Sector Group Unprotect<br>(Note 2)  | L                       | H   | L   | V <sub>ID</sub>            | H        | X               | SA, A6=H,<br>A3=L, A2=L,<br>A1=H, A0=L | (Note 4)         | X                          | X                                   |
| Temporary Sector Group<br>Unprotect | X                       | X   | X   | V <sub>ID</sub>            | H        | X               | A <sub>IN</sub>                        | (Note 4)         | (Note 4)                   | High-Z                              |

**Legend**

L = Logic Low = V<sub>IL</sub>, H = Logic High = V<sub>IH</sub>, X = Don't Care, V<sub>ID</sub> = 11.5–12.5 V, V<sub>HH</sub> = 11.5–12.5 V, SA = Sector Address, A<sub>IN</sub> = Address In, D<sub>IN</sub> = Data In, D<sub>OUT</sub> = Data Out

**Notes**

- Addresses are Amax:A0 in word mode; Amax: A-1 in byte mode. Sector addresses are Amax:A15 in both modes.
- The sector protect and sector unprotect functions may also be implemented via programming equipment. See [Sector Group Protection and Unprotection on page 41](#).
- If WP# = V<sub>IL</sub>, the first or last sector remains protected (for uniform sector devices), and the two outer boot sectors are protected (for boot sector devices). If WP# = V<sub>IH</sub>, the first or last sector, or the two outer boot sectors are protected or unprotected as determined by the method described in [Sector Group Protection and Unprotection on page 41](#). All sectors are unprotected when shipped from the factory (The Secured Silicon Sector may be factory protected depending on version ordered.)
- D<sub>IN</sub> or D<sub>OUT</sub> as required by command sequence, data polling, or sector protect algorithm (see [Figure 10.3 on page 64](#)).

## 7.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic 1, the device is in word configuration, DQ0–DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic 0, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

## 7.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to  $V_{IL}$ . CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at  $V_{IH}$ .

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See [Reading Array Data on page 52](#) for more information. Refer to the AC Read-Only Operations table in [AC Characteristics on page 72](#) for timing specifications and the timing diagram. Refer to [DC Characteristics on page 70](#) for the active current specification on reading array data.

### 7.2.1 Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words/8 bytes. The appropriate page is selected by the higher address bits A(max)–A2. Address bits A1–A0 in word mode (A1–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to  $t_{ACC}$  or  $t_{CE}$  and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to  $t_{PACC}$ . When CE# is deasserted and reasserted for a subsequent access, the access time is  $t_{ACC}$  or  $t_{CE}$ . Fast page mode accesses are obtained by keeping the *read-page addresses* constant and changing the *intra-read page addresses*.

## 7.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to  $V_{IL}$ , and OE# to  $V_{IH}$ .

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The [Word Program Command Sequence on page 53](#) contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. [Table 7.4 on page 27](#) to [Table 7.22 on page 45](#) indicate the address space that each sector occupies.

Refer to [DC Characteristics on page 70](#) for the active current specification for the write mode. [AC Characteristics on page 72](#) contains timing specification tables and timing diagrams for write operations.

### 7.3.1 Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See [Write Buffer on page 24](#) for more information.

### 7.3.2 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC or ACC pin, depending on model number. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts  $V_{HH}$  on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sector groups, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing  $V_{HH}$  from the WP#/ACC or ACC pin, depending on model number, returns the device to normal operation. *Note that the WP#/ACC or ACC pin must not be at  $V_{HH}$  for operations other than accelerated programming, or device damage may result. WP# contains an internal pull-up; when unconnected, WP# is at  $V_{IH}$ .*

### 7.3.3 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to [Autoselect Mode on page 40](#) and [Autoselect Command Sequence on page 53](#) for more information.

## 7.4 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at  $V_{IO} \pm 0.3$  V. (Note that this is a more restricted voltage range than  $V_{IH}$ .) If CE# and RESET# are held at  $V_{IH}$ , but not within  $V_{IO} \pm 0.3$  V, the device is in the standby mode, but the standby current is greater. The device requires standard access time ( $t_{CE}$ ) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to [DC Characteristics on page 70](#) for the standby current specification.

## 7.5 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for  $t_{ACC} + 30$  ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to [DC Characteristics on page 70](#) for the automatic sleep mode current specification.



## 7.6 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of  $t_{RP}$ , the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at  $V_{SS} \pm 0.3$  V, the device draws CMOS standby current ( $I_{CC5}$ ). If RESET# is held at  $V_{IL}$  but not within  $V_{SS} \pm 0.3$  V, the standby current is greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the tables in [AC Characteristics on page 72](#) for RESET# parameters and to [Figure 16.4 on page 75](#) for the timing diagram.

## 7.7 Output Disable Mode

When the OE# input is at  $V_{IH}$ , output from the device is disabled. The output pins are placed in the high impedance state.

**Table 7.2** S29GL016A (Model R1, W1) Top Boot Sector Addresses

| Sector | A19–A12   | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|-----------|--------------------------|---------------------|----------------------|
| SA0    | 000000xxx | 64/32                    | 000000h–00FFFFh     | 00000h–07FFFh        |
| SA1    | 000001xxx | 64/32                    | 010000h–01FFFFh     | 08000h–0FFFFh        |
| SA2    | 000010xxx | 64/32                    | 020000h–02FFFFh     | 10000h–17FFFh        |
| SA3    | 000011xxx | 64/32                    | 030000h–03FFFFh     | 18000h–1FFFFh        |
| SA4    | 000100xxx | 64/32                    | 040000h–04FFFFh     | 20000h–27FFFh        |
| SA5    | 000101xxx | 64/32                    | 050000h–05FFFFh     | 28000h–2FFFFh        |
| SA6    | 000110xxx | 64/32                    | 060000h–06FFFFh     | 30000h–37FFFh        |
| SA7    | 000111xxx | 64/32                    | 070000h–07FFFFh     | 38000h–3FFFFh        |
| SA8    | 001000xxx | 64/32                    | 080000h–08FFFFh     | 40000h–47FFFh        |
| SA9    | 001001xxx | 64/32                    | 090000h–09FFFFh     | 48000h–4FFFFh        |
| SA10   | 001010xxx | 64/32                    | 0A0000h–0AFFFFh     | 50000h–57FFFh        |
| SA11   | 001011xxx | 64/32                    | 0B0000h–0BFFFFh     | 58000h–5FFFFh        |
| SA12   | 001100xxx | 64/32                    | 0C0000h–0CFFFFh     | 60000h–67FFFh        |
| SA13   | 001101xxx | 64/32                    | 0D0000h–0DFFFFh     | 68000h–6FFFFh        |
| SA14   | 001101xxx | 64/32                    | 0E0000h–0EFFFFh     | 70000h–77FFFh        |
| SA15   | 001111xxx | 64/32                    | 0F0000h–0FFFFFh     | 78000h–7FFFFh        |
| SA16   | 010000xxx | 64/32                    | 100000h–0FFFFFh     | 80000h–87FFFh        |
| SA17   | 010001xxx | 64/32                    | 110000h–11FFFFh     | 88000h–8FFFFh        |
| SA18   | 010010xxx | 64/32                    | 120000h–12FFFFh     | 90000h–97FFFh        |
| SA19   | 010011xxx | 64/32                    | 130000h–13FFFFh     | 98000h–9FFFFh        |
| SA20   | 010100xxx | 64/32                    | 140000h–14FFFFh     | A0000h–A7FFFh        |
| SA21   | 010101xxx | 64/32                    | 150000h–15FFFFh     | A8000h–AFFFFh        |
| SA22   | 010110xxx | 64/32                    | 160000h–16FFFFh     | B0000h–B7FFFh        |
| SA23   | 010111xxx | 64/32                    | 170000h–17FFFFh     | B8000h–BFFFFh        |
| SA24   | 011000xxx | 64/32                    | 180000h–18FFFFh     | C0000h–C7FFFh        |
| SA25   | 011001xxx | 64/32                    | 190000h–19FFFFh     | C8000h–CFFFFh        |
| SA26   | 011010xxx | 64/32                    | 1A0000h–1AFFFFh     | D0000h–D7FFFh        |
| SA27   | 011011xxx | 64/32                    | 1B0000h–1BFFFFh     | D8000h–DFFFFh        |
| SA28   | 011000xxx | 64/32                    | 1C0000h–1CFFFFh     | E0000h–E7FFFh        |
| SA29   | 011101xxx | 64/32                    | 1D0000h–1DFFFFh     | E8000h–EFFFFh        |
| SA30   | 011110xxx | 64/32                    | 1E0000h–1EFFFFh     | F0000h–F7FFFh        |
| SA31   | 111111000 | 8/4                      | 1F0000h–1F1FFFh     | 0F8000h–0F8FFFh      |
| SA32   | 111111001 | 8/4                      | 1F2000h–1F3FFFh     | 0F9000h–0F9FFFh      |
| SA33   | 111111010 | 8/4                      | 1F4000h–1F5FFFh     | 0FA000h–0FAFFFh      |
| SA34   | 111111011 | 8/4                      | 1F6000h–1F7FFFh     | 0FB000h–0FBFFFh      |
| SA35   | 111111100 | 8/4                      | 1F8000h–1F9FFFh     | 0FC000h–0FCFFFh      |
| SA36   | 111111101 | 8/4                      | 1FA000h–1FBFFFh     | 0FD000h–0FDFFFh      |
| SA37   | 111111110 | 8/4                      | 1FC000h–1FDFFFh     | 0FE000h–0FEFFFh      |
| SA38   | 111111111 | 8/4                      | 1FE000h–1FFFFFFh    | 0FF000h–0FFFFFFh     |

**Table 7.3** S29GL016A (Model R2, W2) Bottom Boot Sector Addresses

| Sector | A19–A12   | Sector Size (KB/Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|-----------|-------------------------|---------------------|----------------------|
| SA0    | 000000000 | 8/4                     | 000000h–001FFFh     | 00000h–00FFFh        |
| SA1    | 000000001 | 8/4                     | 002000h–003FFFh     | 01000h–01FFFh        |
| SA2    | 000000010 | 8/4                     | 004000h–005FFFh     | 02000h–02FFFh        |
| SA3    | 000000011 | 8/4                     | 006000h–007FFFh     | 03000h–03FFFh        |
| SA4    | 000000100 | 8/4                     | 008000h–009FFFh     | 04000h–04FFFh        |
| SA5    | 000000101 | 8/4                     | 00A000h–00BFFFh     | 05000h–05FFFh        |
| SA6    | 000000110 | 8/4                     | 00C000h–00DFFFh     | 06000h–06FFFh        |
| SA7    | 000000111 | 8/4                     | 00E000h–00FFFFh     | 07000h–07FFFh        |
| SA8    | 000001xxx | 64/32                   | 010000h–01FFFFh     | 08000h–0FFFFh        |
| SA9    | 000010xxx | 64/32                   | 020000h–02FFFFh     | 10000h–17FFFh        |
| SA10   | 000011xxx | 64/32                   | 030000h–03FFFFh     | 18000h–1FFFFh        |
| SA11   | 000100xxx | 64/32                   | 040000h–04FFFFh     | 20000h–27FFFh        |
| SA12   | 000101xxx | 64/32                   | 050000h–05FFFFh     | 28000h–2FFFFh        |
| SA13   | 000110xxx | 64/32                   | 060000h–06FFFFh     | 30000h–37FFFh        |
| SA14   | 000111xxx | 64/32                   | 070000h–07FFFFh     | 38000h–3FFFFh        |
| SA15   | 001000xxx | 64/32                   | 080000h–08FFFFh     | 40000h–47FFFh        |
| SA16   | 001001xxx | 64/32                   | 090000h–09FFFFh     | 48000h–4FFFFh        |
| SA17   | 001010xxx | 64/32                   | 0A0000h–0AFFFFh     | 50000h–57FFFh        |
| SA18   | 001011xxx | 64/32                   | 0B0000h–0BFFFFh     | 58000h–5FFFFh        |

| Sector | A19–A12   | Sector Size (KB/Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|-----------|-------------------------|---------------------|----------------------|
| SA19   | 001100xxx | 64/32                   | 0C0000h–0CFFFFh     | 60000h–67FFFh        |
| SA20   | 001101xxx | 64/32                   | 0D0000h–0DFFFFh     | 68000h–6FFFFh        |
| SA21   | 001101xxx | 64/32                   | 0E0000h–0EFFFFh     | 70000h–77FFFh        |
| SA22   | 001111xxx | 64/32                   | 0F0000h–0FFFFFh     | 78000h–7FFFFh        |
| SA23   | 010000xxx | 64/32                   | 100000h–00FFFFh     | 80000h–87FFFh        |
| SA24   | 010001xxx | 64/32                   | 110000h–11FFFFh     | 88000h–8FFFFh        |
| SA25   | 010010xxx | 64/32                   | 120000h–12FFFFh     | 90000h–97FFFh        |
| SA26   | 010011xxx | 64/32                   | 130000h–13FFFFh     | 98000h–9FFFFh        |
| SA27   | 010100xxx | 64/32                   | 140000h–14FFFFh     | A0000h–A7FFFh        |
| SA28   | 010101xxx | 64/32                   | 150000h–15FFFFh     | A8000h–AFFFFh        |
| SA29   | 010110xxx | 64/32                   | 160000h–16FFFFh     | B0000h–B7FFFh        |
| SA30   | 010111xxx | 64/32                   | 170000h–17FFFFh     | B8000h–BFFFFh        |
| SA31   | 011000xxx | 64/32                   | 180000h–18FFFFh     | C0000h–C7FFFh        |
| SA32   | 011001xxx | 64/32                   | 190000h–19FFFFh     | C8000h–CFFFFh        |
| SA33   | 011010xxx | 64/32                   | 1A0000h–1AFFFFh     | D0000h–D7FFFh        |
| SA34   | 011011xxx | 64/32                   | 1B0000h–1BFFFFh     | D8000h–DFFFFh        |
| SA35   | 011000xxx | 64/32                   | 1C0000h–1CFFFFh     | E0000h–E7FFFh        |
| SA36   | 011101xxx | 64/32                   | 1D0000h–1DFFFFh     | E8000h–EFFFFh        |
| SA37   | 011110xxx | 64/32                   | 1E0000h–1EFFFFh     | F0000h–F7FFFh        |
| SA38   | 011111xxx | 64/32                   | 1F0000h–1FFFFFh     | F8000h–FFFFFh        |

Table 7.4 S29GL032A (Models R1, R2) Sector Addresses

| Sector | A20-A15     | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|-------------|--------------------------|---------------------|----------------------|
| SA0    | 0 0 0 0 0 0 | 64/32                    | 000000–00FFFF       | 000000–007FFF        |
| SA1    | 0 0 0 0 0 1 | 64/32                    | 010000–01FFFF       | 008000–00FFFF        |
| SA2    | 0 0 0 0 1 0 | 64/32                    | 020000–02FFFF       | 010000–017FFF        |
| SA3    | 0 0 0 0 1 1 | 64/32                    | 030000–03FFFF       | 018000–01FFFF        |
| SA4    | 0 0 0 1 0 0 | 64/32                    | 040000–04FFFF       | 020000–027FFF        |
| SA5    | 0 0 0 1 0 1 | 64/32                    | 050000–05FFFF       | 028000–02FFFF        |
| SA6    | 0 0 0 1 1 0 | 64/32                    | 060000–06FFFF       | 030000–037FFF        |
| SA7    | 0 0 0 1 1 1 | 64/32                    | 070000–07FFFF       | 038000–03FFFF        |
| SA8    | 0 0 1 0 0 0 | 64/32                    | 080000–08FFFF       | 040000–047FFF        |
| SA9    | 0 0 1 0 0 1 | 64/32                    | 090000–09FFFF       | 048000–04FFFF        |
| SA10   | 0 0 1 0 1 0 | 64/32                    | 0A0000–0AFFFF       | 050000–057FFF        |
| SA11   | 0 0 1 0 1 1 | 64/32                    | 0B0000–0BFFFF       | 058000–05FFFF        |
| SA12   | 0 0 1 1 0 0 | 64/32                    | 0C0000–0CFFFF       | 060000–067FFF        |
| SA13   | 0 0 1 1 0 1 | 64/32                    | 0D0000–0DFFFF       | 068000–06FFFF        |
| SA14   | 0 0 1 1 1 0 | 64/32                    | 0E0000–0EFFFF       | 070000–077FFF        |
| SA15   | 0 0 1 1 1 1 | 64/32                    | 0F0000–0FFFFF       | 078000–07FFFF        |
| SA16   | 0 1 0 0 0 0 | 64/32                    | 100000–10FFFF       | 080000–087FFF        |
| SA17   | 0 1 0 0 0 1 | 64/32                    | 110000–11FFFF       | 088000–08FFFF        |
| SA18   | 0 1 0 0 1 0 | 64/32                    | 120000–12FFFF       | 090000–097FFF        |
| SA19   | 0 1 0 0 1 1 | 64/32                    | 130000–13FFFF       | 098000–09FFFF        |
| SA20   | 0 1 0 1 0 0 | 64/32                    | 140000–14FFFF       | 0A0000–0A7FFF        |
| SA21   | 0 1 0 1 0 1 | 64/32                    | 150000–15FFFF       | 0A8000–0AFFFF        |
| SA22   | 0 1 0 1 1 0 | 64/32                    | 160000–16FFFF       | 0B0000–0B7FFF        |
| SA23   | 0 1 0 1 1 1 | 64/32                    | 170000–17FFFF       | 0B8000–0BFFFF        |
| SA24   | 0 1 1 0 0 0 | 64/32                    | 180000–18FFFF       | 0C0000–0C7FFF        |
| SA25   | 0 1 1 0 0 1 | 64/32                    | 190000–19FFFF       | 0C8000–0CFFFF        |
| SA26   | 0 1 1 0 1 0 | 64/32                    | 1A0000–1AFFFF       | 0D0000–0D7FFF        |
| SA27   | 0 1 1 0 1 1 | 64/32                    | 1B0000–1BFFFF       | 0D8000–0DFFFF        |
| SA28   | 0 1 1 1 0 0 | 64/32                    | 1C0000–1CFFFF       | 0E0000–0E7FFF        |
| SA29   | 0 1 1 1 0 1 | 64/32                    | 1D0000–1DFFFF       | 0E8000–0EFFFF        |
| SA30   | 0 1 1 1 1 0 | 64/32                    | 1E0000–1EFFFF       | 0F0000–0F7FFF        |
| SA31   | 0 1 1 1 1 1 | 64/32                    | 1F0000–1FFFFF       | 0F8000–0FFFFF        |
| SA32   | 1 0 0 0 0 0 | 64/32                    | 200000–20FFFF       | 100000–107FFF        |
| SA33   | 1 0 0 0 0 1 | 64/32                    | 210000–21FFFF       | 108000–10FFFF        |
| SA34   | 1 0 0 0 1 0 | 64/32                    | 220000–22FFFF       | 110000–117FFF        |
| SA35   | 1 0 0 0 1 1 | 64/32                    | 230000–23FFFF       | 118000–11FFFF        |
| SA36   | 1 0 0 1 0 0 | 64/32                    | 240000–24FFFF       | 120000–127FFF        |
| SA37   | 1 0 0 1 0 1 | 64/32                    | 250000–25FFFF       | 128000–12FFFF        |
| SA38   | 1 0 0 1 1 0 | 64/32                    | 260000–26FFFF       | 130000–137FFF        |
| SA39   | 1 0 0 1 1 1 | 64/32                    | 270000–27FFFF       | 138000–13FFFF        |
| SA40   | 1 0 1 0 0 0 | 64/32                    | 280000–28FFFF       | 140000–147FFF        |
| SA41   | 1 0 1 0 0 1 | 64/32                    | 290000–29FFFF       | 148000–14FFFF        |
| SA42   | 1 0 1 0 1 0 | 64/32                    | 2A0000–2AFFFF       | 150000–157FFF        |
| SA43   | 1 0 1 0 1 1 | 64/32                    | 2B0000–2BFFFF       | 158000–15FFFF        |
| SA44   | 1 0 1 1 0 0 | 64/32                    | 2C0000–2CFFFF       | 160000–167FFF        |
| SA45   | 1 0 1 1 0 1 | 64/32                    | 2D0000–2DFFFF       | 168000–16FFFF        |
| SA46   | 1 0 1 1 1 0 | 64/32                    | 2E0000–2EFFFF       | 170000–177FFF        |
| SA47   | 1 0 1 1 1 1 | 64/32                    | 2F0000–2FFFFF       | 178000–17FFFF        |
| SA48   | 1 1 0 0 0 0 | 64/32                    | 300000–30FFFF       | 180000–187FFF        |
| SA49   | 1 1 0 0 0 1 | 64/32                    | 310000–31FFFF       | 188000–18FFFF        |
| SA50   | 1 1 0 0 1 0 | 64/32                    | 320000–32FFFF       | 190000–197FFF        |
| SA51   | 1 1 0 0 1 1 | 64/32                    | 330000–33FFFF       | 198000–19FFFF        |
| SA52   | 1 1 0 1 0 0 | 64/32                    | 340000–34FFFF       | 1A0000–1A7FFF        |
| SA53   | 1 1 0 1 0 1 | 64/32                    | 350000–35FFFF       | 1A8000–1AFFFF        |
| SA54   | 1 1 0 1 1 0 | 64/32                    | 360000–36FFFF       | 1B0000–1B7FFF        |
| SA55   | 1 1 0 1 1 1 | 64/32                    | 370000–37FFFF       | 1B8000–1BFFFF        |
| SA56   | 1 1 1 0 0 0 | 64/32                    | 380000–38FFFF       | 1C0000–1C7FFF        |
| SA57   | 1 1 1 0 0 1 | 64/32                    | 390000–39FFFF       | 1C8000–1CFFFF        |
| SA58   | 1 1 1 0 1 0 | 64/32                    | 3A0000–3AFFFF       | 1D0000–1D7FFF        |
| SA59   | 1 1 1 0 1 1 | 64/32                    | 3B0000–3BFFFF       | 1D8000–1DFFFF        |
| SA60   | 1 1 1 1 0 0 | 64/32                    | 3C0000–3CFFFF       | 1E0000–1E7FFF        |
| SA61   | 1 1 1 1 0 1 | 64/32                    | 3D0000–3DFFFF       | 1E8000–1EFFFF        |
| SA62   | 1 1 1 1 1 0 | 64/32                    | 3E0000–3EFFFF       | 1F0000–1F7FFF        |
| SA63   | 1 1 1 1 1 1 | 64/32                    | 3F0000–3FFFFF       | 1F8000–1FFFFF        |

Table 7.5 S29GL032A (Model R3, W3) Top Boot Sector Addresses

| Sector | A20–A12   | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range | Sector | A20–A12   | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|-----------|--------------------------|---------------------|----------------------|--------|-----------|--------------------------|---------------------|----------------------|
| SA0    | 00000xxx  | 64/32                    | 00000h–00FFFFh      | 0000h–07FFFh         | SA36   | 100100xxx | 64/32                    | 24000h–24FFFFh      | 12000h–127FFFh       |
| SA1    | 00001xxx  | 64/32                    | 01000h–01FFFFh      | 0800h–0FFFFh         | SA37   | 100101xxx | 64/32                    | 25000h–25FFFFh      | 12800h–12FFFFh       |
| SA2    | 000010xxx | 64/32                    | 02000h–02FFFFh      | 1000h–17FFFh         | SA38   | 100110xxx | 64/32                    | 26000h–26FFFFh      | 13000h–137FFFh       |
| SA3    | 000011xxx | 64/32                    | 03000h–03FFFFh      | 1800h–1FFFFh         | SA39   | 100111xxx | 64/32                    | 27000h–27FFFFh      | 13800h–13FFFFh       |
| SA4    | 000100xxx | 64/32                    | 04000h–04FFFFh      | 2000h–27FFFh         | SA40   | 101000xxx | 64/32                    | 28000h–28FFFFh      | 14000h–147FFFh       |
| SA5    | 000101xxx | 64/32                    | 05000h–05FFFFh      | 2800h–2FFFFh         | SA41   | 101001xxx | 64/32                    | 29000h–29FFFFh      | 14800h–14FFFFh       |
| SA6    | 000110xxx | 64/32                    | 06000h–06FFFFh      | 3000h–37FFFh         | SA42   | 101010xxx | 64/32                    | 2A000h–2AFFFFh      | 15000h–157FFFh       |
| SA7    | 000111xxx | 64/32                    | 07000h–07FFFFh      | 3800h–3FFFFh         | SA43   | 101011xxx | 64/32                    | 2B000h–2BFFFFh      | 15800h–15FFFFh       |
| SA8    | 001000xxx | 64/32                    | 08000h–08FFFFh      | 4000h–47FFFh         | SA44   | 101100xxx | 64/32                    | 2C000h–2CFFFFh      | 16000h–167FFFh       |
| SA9    | 001001xxx | 64/32                    | 09000h–09FFFFh      | 4800h–4FFFFh         | SA45   | 101101xxx | 64/32                    | 2D000h–2DFFFFh      | 16800h–16FFFFh       |
| SA10   | 001010xxx | 64/32                    | 0A000h–0AFFFFh      | 5000h–57FFFh         | SA46   | 101110xxx | 64/32                    | 2E000h–2EFFFFh      | 17000h–177FFFh       |
| SA11   | 001011xxx | 64/32                    | 0B000h–0BFFFFh      | 5800h–5FFFFh         | SA47   | 101111xxx | 64/32                    | 2F000h–2FFFFh       | 17800h–17FFFFh       |
| SA12   | 001100xxx | 64/32                    | 0C000h–0CFFFFh      | 6000h–67FFFh         | SA48   | 110000xxx | 64/32                    | 30000h–30FFFFh      | 18000h–187FFFh       |
| SA13   | 001101xxx | 64/32                    | 0D000h–0DFFFFh      | 6800h–6FFFFh         | SA49   | 110001xxx | 64/32                    | 31000h–31FFFFh      | 18800h–18FFFFh       |
| SA14   | 001101xxx | 64/32                    | 0E000h–0EFFFFh      | 7000h–77FFFh         | SA50   | 110010xxx | 64/32                    | 32000h–32FFFFh      | 19000h–197FFFh       |
| SA15   | 001111xxx | 64/32                    | 0F000h–0FFFFh       | 7800h–7FFFFh         | SA51   | 110011xxx | 64/32                    | 33000h–33FFFFh      | 19800h–19FFFFh       |
| SA16   | 010000xxx | 64/32                    | 10000h–00FFFFh      | 8000h–87FFFh         | SA52   | 100100xxx | 64/32                    | 34000h–34FFFFh      | 1A000h–1A7FFFh       |
| SA17   | 010001xxx | 64/32                    | 11000h–11FFFFh      | 8800h–8FFFFh         | SA53   | 110101xxx | 64/32                    | 35000h–35FFFFh      | 1A800h–1AFFFFh       |
| SA18   | 010010xxx | 64/32                    | 12000h–12FFFFh      | 9000h–97FFFh         | SA54   | 110110xxx | 64/32                    | 36000h–36FFFFh      | 1B000h–1B7FFFh       |
| SA19   | 010011xxx | 64/32                    | 13000h–13FFFFh      | 9800h–9FFFFh         | SA55   | 110111xxx | 64/32                    | 37000h–37FFFFh      | 1B800h–1BFFFFh       |
| SA20   | 010100xxx | 64/32                    | 14000h–14FFFFh      | A000h–A7FFFh         | SA56   | 111000xxx | 64/32                    | 38000h–38FFFFh      | 1C000h–1C7FFFh       |
| SA21   | 010101xxx | 64/32                    | 15000h–15FFFFh      | A800h–AFFFFh         | SA57   | 111001xxx | 64/32                    | 39000h–39FFFFh      | 1C800h–1CFFFFh       |
| SA22   | 010110xxx | 64/32                    | 16000h–16FFFFh      | B000h–B7FFFh         | SA58   | 111010xxx | 64/32                    | 3A000h–3AFFFFh      | 1D000h–1D7FFFh       |
| SA23   | 010111xxx | 64/32                    | 17000h–17FFFFh      | B800h–BFFFFh         | SA59   | 111011xxx | 64/32                    | 3B000h–3BFFFFh      | 1D800h–1DFFFFh       |
| SA24   | 011000xxx | 64/32                    | 18000h–18FFFFh      | C000h–C7FFFh         | SA60   | 111100xxx | 64/32                    | 3C000h–3CFFFFh      | 1E000h–1E7FFFh       |
| SA25   | 011001xxx | 64/32                    | 19000h–19FFFFh      | C800h–CFFFFh         | SA61   | 111101xxx | 64/32                    | 3D000h–3DFFFFh      | 1E800h–1EFFFFh       |
| SA26   | 011010xxx | 64/32                    | 1A000h–1AFFFFh      | D000h–D7FFFh         | SA62   | 111110xxx | 64/32                    | 3E000h–3EFFFFh      | 1F000h–1F7FFFh       |
| SA27   | 011011xxx | 64/32                    | 1B000h–1BFFFFh      | D800h–DFFFFh         | SA63   | 111111000 | 8/4                      | 3F000h–3F1FFFh      | 1F800h–1F8FFFh       |
| SA28   | 011100xxx | 64/32                    | 1C000h–1CFFFFh      | E000h–E7FFFh         | SA64   | 111111001 | 8/4                      | 3F200h–3F3FFFh      | 1F900h–1F9FFFh       |
| SA29   | 011101xxx | 64/32                    | 1D000h–1DFFFFh      | E800h–EFFFFh         | SA65   | 111111010 | 8/4                      | 3F400h–3F5FFFh      | 1FA00h–1FAFFFh       |
| SA30   | 011110xxx | 64/32                    | 1E000h–1EFFFFh      | F000h–F7FFFh         | SA66   | 111111011 | 8/4                      | 3F600h–3F7FFFh      | 1FB00h–1FBFFFh       |
| SA31   | 011111xxx | 64/32                    | 1F000h–1FFFFh       | F800h–FFFFh          | SA67   | 111111100 | 8/4                      | 3F800h–3F9FFFh      | 1FC00h–1FCFFFh       |
| SA32   | 100000xxx | 64/32                    | 20000h–20FFFFh      | F900h–107FFFh        | SA68   | 111111101 | 8/4                      | 3FA00h–3FBFFFh      | 1FD00h–1FDFFFh       |
| SA33   | 100001xxx | 64/32                    | 21000h–21FFFFh      | 10800h–10FFFFh       | SA69   | 111111110 | 8/4                      | 3FC00h–3FDFFFh      | 1FE00h–1FEFFFh       |
| SA34   | 100010xxx | 64/32                    | 22000h–22FFFFh      | 11000h–117FFFh       | SA70   | 111111111 | 8/4                      | 3FE00h–3FFFFh       | 1FF00h–1FFFFh        |
| SA35   | 101011xxx | 64/32                    | 23000h–23FFFFh      | 11800h–11FFFFh       |        |           |                          |                     |                      |

Table 7.6 S29GL032A (Model R4, W4) Bottom Boot Sector Addresses

| Sector | A20–A12   | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range | Sector | A20–A12   | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|-----------|--------------------------|---------------------|----------------------|--------|-----------|--------------------------|---------------------|----------------------|
| SA0    | 00000000  | 8/4                      | 00000h–001FFFh      | 00000h–00FFFh        | SA19   | 001100xxx | 64/32                    | 0C0000h–0CFFFFh     | 60000h–67FFFh        |
| SA1    | 00000001  | 8/4                      | 002000h–003FFFh     | 01000h–01FFFh        | SA20   | 001101xxx | 64/32                    | 0D0000h–0DFFFFh     | 68000h–6FFFFh        |
| SA2    | 00000010  | 8/4                      | 004000h–005FFFh     | 02000h–02FFFh        | SA21   | 001101xxx | 64/32                    | 0E0000h–0EFFFFh     | 70000h–77FFFh        |
| SA3    | 00000011  | 8/4                      | 006000h–007FFFh     | 03000h–03FFFh        | SA22   | 001111xxx | 64/32                    | 0F0000h–0FFFFFh     | 78000h–7FFFFh        |
| SA4    | 00000100  | 8/4                      | 008000h–009FFFh     | 04000h–04FFFh        | SA23   | 010000xxx | 64/32                    | 100000h–00FFFFh     | 80000h–87FFFh        |
| SA5    | 00000101  | 8/4                      | 00A000h–00BFFFh     | 05000h–05FFFh        | SA24   | 010001xxx | 64/32                    | 110000h–11FFFFh     | 88000h–8FFFFh        |
| SA6    | 00000110  | 8/4                      | 00C000h–00DFFFh     | 06000h–06FFFh        | SA25   | 010010xxx | 64/32                    | 120000h–12FFFFh     | 90000h–97FFFh        |
| SA7    | 00000111  | 8/4                      | 00E000h–00FFFFh     | 07000h–07FFFh        | SA26   | 010011xxx | 64/32                    | 130000h–13FFFFh     | 98000h–9FFFFh        |
| SA8    | 000001xxx | 64/32                    | 010000h–01FFFFh     | 08000h–0FFFFh        | SA27   | 010100xxx | 64/32                    | 140000h–14FFFFh     | A0000h–A7FFFh        |
| SA9    | 000010xxx | 64/32                    | 020000h–02FFFFh     | 10000h–17FFFh        | SA28   | 010101xxx | 64/32                    | 150000h–15FFFFh     | A8000h–AFFFFh        |
| SA10   | 000011xxx | 64/32                    | 030000h–03FFFFh     | 18000h–1FFFFh        | SA29   | 010110xxx | 64/32                    | 160000h–16FFFFh     | B0000h–B7FFFh        |
| SA11   | 000100xxx | 64/32                    | 040000h–04FFFFh     | 20000h–27FFFh        | SA30   | 010111xxx | 64/32                    | 170000h–17FFFFh     | B8000h–BFFFFh        |
| SA12   | 000101xxx | 64/32                    | 050000h–05FFFFh     | 28000h–2FFFFh        | SA31   | 011000xxx | 64/32                    | 180000h–18FFFFh     | C0000h–C7FFFh        |
| SA13   | 000110xxx | 64/32                    | 060000h–06FFFFh     | 30000h–37FFFh        | SA32   | 011001xxx | 64/32                    | 190000h–19FFFFh     | C8000h–CFFFFh        |
| SA14   | 000111xxx | 64/32                    | 070000h–07FFFFh     | 38000h–3FFFFh        | SA33   | 011010xxx | 64/32                    | 1A0000h–1AFFFFh     | D0000h–D7FFFh        |
| SA15   | 001000xxx | 64/32                    | 080000h–08FFFFh     | 40000h–47FFFh        | SA34   | 011011xxx | 64/32                    | 1B0000h–1BFFFFh     | D8000h–DFFFFh        |
| SA16   | 001001xxx | 64/32                    | 090000h–09FFFFh     | 48000h–4FFFFh        | SA35   | 011000xxx | 64/32                    | 1C0000h–1CFFFFh     | E0000h–E7FFFh        |
| SA17   | 001010xxx | 64/32                    | 0A0000h–0AFFFFh     | 50000h–57FFFh        | SA36   | 011101xxx | 64/32                    | 1D0000h–1DFFFFh     | E8000h–EFFFFh        |
| SA18   | 001011xxx | 64/32                    | 0B0000h–0BFFFFh     | 58000h–5FFFFh        | SA37   | 011110xxx | 64/32                    | 1E0000h–1EFFFFh     | F0000h–F7FFFh        |
| SA38   | 011111xxx | 64/32                    | 1F0000h–1FFFFFh     | F8000h–FFFFFh        | SA55   | 110000xxx | 64/32                    | 300000h–30FFFFh     | 180000h–187FFFh      |
| SA39   | 100000xxx | 64/32                    | 200000h–20FFFFh     | F9000h–107FFFh       | SA56   | 110001xxx | 64/32                    | 310000h–31FFFFh     | 188000h–18FFFFh      |
| SA40   | 100001xxx | 64/32                    | 210000h–21FFFFh     | 108000h–10FFFFh      | SA57   | 110010xxx | 64/32                    | 320000h–32FFFFh     | 190000h–197FFFh      |
| SA41   | 100010xxx | 64/32                    | 220000h–22FFFFh     | 110000h–117FFFh      | SA58   | 110011xxx | 64/32                    | 330000h–33FFFFh     | 198000h–19FFFFh      |
| SA42   | 101011xxx | 64/32                    | 230000h–23FFFFh     | 118000h–11FFFFh      | SA59   | 100100xxx | 64/32                    | 340000h–34FFFFh     | 1A0000h–1A7FFFh      |
| SA43   | 100100xxx | 64/32                    | 240000h–24FFFFh     | 120000h–127FFFh      | SA60   | 110101xxx | 64/32                    | 350000h–35FFFFh     | 1A8000h–1AFFFFh      |
| SA44   | 100101xxx | 64/32                    | 250000h–25FFFFh     | 128000h–12FFFFh      | SA61   | 110110xxx | 64/32                    | 360000h–36FFFFh     | 1B0000h–1B7FFFh      |
| SA45   | 100110xxx | 64/32                    | 260000h–26FFFFh     | 130000h–137FFFh      | SA62   | 110111xxx | 64/32                    | 370000h–37FFFFh     | 1B8000h–1BFFFFh      |
| SA46   | 100111xxx | 64/32                    | 270000h–27FFFFh     | 138000h–13FFFFh      | SA63   | 111000xxx | 64/32                    | 380000h–38FFFFh     | 1C0000h–1C7FFFh      |
| SA47   | 101000xxx | 64/32                    | 280000h–28FFFFh     | 140000h–147FFFh      | SA64   | 111001xxx | 64/32                    | 390000h–39FFFFh     | 1C8000h–1CFFFFh      |
| SA48   | 101001xxx | 64/32                    | 290000h–29FFFFh     | 148000h–14FFFFh      | SA65   | 111010xxx | 64/32                    | 3A0000h–3AFFFFh     | 1D0000h–1D7FFFh      |
| SA49   | 101010xxx | 64/32                    | 2A0000h–2AFFFFh     | 150000h–157FFFh      | SA66   | 111011xxx | 64/32                    | 3B0000h–3BFFFFh     | 1D8000h–1DFFFFh      |
| SA50   | 101011xxx | 64/32                    | 2B0000h–2BFFFFh     | 158000h–15FFFFh      | SA67   | 111100xxx | 64/32                    | 3C0000h–3CFFFFh     | 1E0000h–1E7FFFh      |
| SA51   | 101100xxx | 64/32                    | 2C0000h–2CFFFFh     | 160000h–167FFFh      | SA68   | 111101xxx | 64/32                    | 3D0000h–3DFFFFh     | 1E8000h–1EFFFFh      |
| SA52   | 101101xxx | 64/32                    | 2D0000h–2DFFFFh     | 168000h–16FFFFh      | SA69   | 111110xxx | 64/32                    | 3E0000h–3EFFFFh     | 1F0000h–1F7FFFh      |
| SA53   | 101110xxx | 64/32                    | 2E0000h–2EFFFFh     | 170000h–177FFFh      | SA70   | 111111xxx | 64/32                    | 3F0000h–3FFFFFh     | 1F8000h–1FFFFFh      |
| SA54   | 101111xxx | 64/32                    | 2F0000h–2FFFFFh     | 178000h–17FFFFh      |        |           |                          |                     |                      |

Table 7.7 S29GL064A (Models R1, R2, R8, R9) Sector Addresses (Sheet 1 of 2)

| Sector | A21-A15 | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|---------|--------------------------|---------------------|----------------------|
| SA0    | 0000000 | 64/32                    | 000000-00FFFF       | 000000-007FFF        |
| SA1    | 0000001 | 64/32                    | 010000-01FFFF       | 008000-00FFFF        |
| SA2    | 0000010 | 64/32                    | 020000-02FFFF       | 010000-017FFF        |
| SA3    | 0000011 | 64/32                    | 030000-03FFFF       | 018000-01FFFF        |
| SA4    | 0000100 | 64/32                    | 040000-04FFFF       | 020000-027FFF        |
| SA5    | 0000101 | 64/32                    | 050000-05FFFF       | 028000-02FFFF        |
| SA6    | 0000110 | 64/32                    | 060000-06FFFF       | 030000-037FFF        |
| SA7    | 0000111 | 64/32                    | 070000-07FFFF       | 038000-03FFFF        |
| SA8    | 0001000 | 64/32                    | 080000-08FFFF       | 040000-047FFF        |
| SA9    | 0001001 | 64/32                    | 090000-09FFFF       | 048000-04FFFF        |
| SA10   | 0001010 | 64/32                    | 0A0000-0AFFFF       | 050000-057FFF        |
| SA11   | 0001011 | 64/32                    | 0B0000-0BFFFF       | 058000-05FFFF        |
| SA12   | 0001100 | 64/32                    | 0C0000-0CFFFF       | 060000-067FFF        |
| SA13   | 0001101 | 64/32                    | 0D0000-0DFFFF       | 068000-06FFFF        |
| SA14   | 0001110 | 64/32                    | 0E0000-0EFFFF       | 070000-077FFF        |
| SA15   | 0001111 | 64/32                    | 0F0000-0FFFFF       | 078000-07FFFF        |
| SA16   | 0010000 | 64/32                    | 100000-10FFFF       | 080000-087FFF        |
| SA17   | 0010001 | 64/32                    | 110000-11FFFF       | 088000-08FFFF        |
| SA18   | 0010010 | 64/32                    | 120000-12FFFF       | 090000-097FFF        |
| SA19   | 0010011 | 64/32                    | 130000-13FFFF       | 098000-09FFFF        |
| SA20   | 0010100 | 64/32                    | 140000-14FFFF       | 0A0000-0A7FFF        |
| SA21   | 0010101 | 64/32                    | 150000-15FFFF       | 0A8000-0AFFFF        |
| SA22   | 0010110 | 64/32                    | 160000-16FFFF       | 0B0000-0B7FFF        |
| SA23   | 0010111 | 64/32                    | 170000-17FFFF       | 0B8000-0BFFFF        |
| SA24   | 0011000 | 64/32                    | 180000-18FFFF       | 0C0000-0C7FFF        |
| SA25   | 0011001 | 64/32                    | 190000-19FFFF       | 0C8000-0CFFFF        |
| SA26   | 0011010 | 64/32                    | 1A0000-1AFFFF       | 0D0000-0D7FFF        |
| SA27   | 0011011 | 64/32                    | 1B0000-1BFFFF       | 0D8000-0DFFFF        |
| SA28   | 0011100 | 64/32                    | 1C0000-1CFFFF       | 0E0000-0E7FFF        |
| SA29   | 0011101 | 64/32                    | 1D0000-1DFFFF       | 0E8000-0EFFFF        |
| SA30   | 0011110 | 64/32                    | 1E0000-1EFFFF       | 0F0000-0F7FFF        |
| SA31   | 0011111 | 64/32                    | 1F0000-1FFFFF       | 0F8000-0FFFFF        |
| SA32   | 0100000 | 64/32                    | 200000-20FFFF       | 100000-107FFF        |
| SA33   | 0100001 | 64/32                    | 210000-21FFFF       | 108000-10FFFF        |
| SA34   | 0100010 | 64/32                    | 220000-22FFFF       | 110000-117FFF        |
| SA35   | 0100011 | 64/32                    | 230000-23FFFF       | 118000-11FFFF        |
| SA36   | 0100100 | 64/32                    | 240000-24FFFF       | 120000-127FFF        |
| SA37   | 0100101 | 64/32                    | 250000-25FFFF       | 128000-12FFFF        |
| SA38   | 0100110 | 64/32                    | 260000-26FFFF       | 130000-137FFF        |
| SA39   | 0100111 | 64/32                    | 270000-27FFFF       | 138000-13FFFF        |
| SA40   | 0101000 | 64/32                    | 280000-28FFFF       | 140000-147FFF        |
| SA41   | 0101001 | 64/32                    | 290000-29FFFF       | 148000-14FFFF        |
| SA42   | 0101010 | 64/32                    | 2A0000-2AFFFF       | 150000-157FFF        |
| SA43   | 0101011 | 64/32                    | 2B0000-2BFFFF       | 158000-15FFFF        |
| SA44   | 0101100 | 64/32                    | 2C0000-2CFFFF       | 160000-167FFF        |
| SA45   | 0101101 | 64/32                    | 2D0000-2DFFFF       | 168000-16FFFF        |
| SA46   | 0101110 | 64/32                    | 2E0000-2EFFFF       | 170000-177FFF        |
| SA47   | 0101111 | 64/32                    | 2F0000-2FFFFF       | 178000-17FFFF        |
| SA48   | 0110000 | 64/32                    | 300000-30FFFF       | 180000-187FFF        |
| SA49   | 0110001 | 64/32                    | 310000-31FFFF       | 188000-18FFFF        |
| SA50   | 0110010 | 64/32                    | 320000-32FFFF       | 190000-197FFF        |
| SA51   | 0110011 | 64/32                    | 330000-33FFFF       | 198000-19FFFF        |
| SA52   | 0110100 | 64/32                    | 340000-34FFFF       | 1A0000-1A7FFF        |
| SA53   | 0110101 | 64/32                    | 350000-35FFFF       | 1A8000-1AFFFF        |
| SA54   | 0110110 | 64/32                    | 360000-36FFFF       | 1B0000-1B7FFF        |
| SA55   | 0110111 | 64/32                    | 370000-37FFFF       | 1B8000-1BFFFF        |
| SA56   | 0111000 | 64/32                    | 380000-38FFFF       | 1C0000-1C7FFF        |
| SA57   | 0111001 | 64/32                    | 390000-39FFFF       | 1C8000-1CFFFF        |
| SA58   | 0111010 | 64/32                    | 3A0000-3AFFFF       | 1D0000-1D7FFF        |
| SA59   | 0111011 | 64/32                    | 3B0000-3BFFFF       | 1D8000-1DFFFF        |
| SA60   | 0111100 | 64/32                    | 3C0000-3CFFFF       | 1E0000-1E7FFF        |
| SA61   | 0111101 | 64/32                    | 3D0000-3DFFFF       | 1E8000-1EFFFF        |
| SA62   | 0111110 | 64/32                    | 3E0000-3EFFFF       | 1F0000-1F7FFF        |
| SA63   | 0111111 | 64/32                    | 3F0000-3FFFFF       | 1F8000-1FFFFF        |
| SA64   | 1000000 | 64/32                    | 400000-40FFFF       | 200000-207FFF        |
| SA65   | 1000001 | 64/32                    | 410000-41FFFF       | 208000-20FFFF        |
| SA66   | 1000010 | 64/32                    | 420000-42FFFF       | 210000-217FFF        |
| SA67   | 1000011 | 64/32                    | 430000-43FFFF       | 218000-21FFFF        |
| SA68   | 1000100 | 64/32                    | 440000-44FFFF       | 220000-227FFF        |
| SA69   | 1000101 | 64/32                    | 450000-45FFFF       | 228000-22FFFF        |
| SA70   | 1000110 | 64/32                    | 460000-46FFFF       | 230000-237FFF        |
| SA71   | 1000111 | 64/32                    | 470000-47FFFF       | 238000-23FFFF        |
| SA72   | 1001000 | 64/32                    | 480000-48FFFF       | 240000-247FFF        |
| SA73   | 1001001 | 64/32                    | 490000-49FFFF       | 248000-24FFFF        |

Table 7.7 S29GL064A (Models R1, R2, R8, R9) Sector Addresses (Sheet 2 of 2)

| Sector | A21–A15 | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|---------|--------------------------|---------------------|----------------------|
| SA74   | 1001010 | 64/32                    | 4A0000–4AFFFF       | 250000–257FFF        |
| SA75   | 1001011 | 64/32                    | 4B0000–4BFFFF       | 258000–25FFFF        |
| SA76   | 1001100 | 64/32                    | 4C0000–4CFFFF       | 260000–267FFF        |
| SA77   | 1001101 | 64/32                    | 4D0000–4DFFFF       | 268000–26FFFF        |
| SA78   | 1001110 | 64/32                    | 4E0000–4EFFFF       | 270000–277FFF        |
| SA79   | 1001111 | 64/32                    | 4F0000–4FFFFF       | 278000–27FFFF        |
| SA80   | 1010000 | 64/32                    | 500000–50FFFF       | 280000–287FFF        |
| SA81   | 1010001 | 64/32                    | 510000–51FFFF       | 288000–28FFFF        |
| SA82   | 1010010 | 64/32                    | 520000–52FFFF       | 290000–297FFF        |
| SA83   | 1010011 | 64/32                    | 530000–53FFFF       | 298000–29FFFF        |
| SA84   | 1010100 | 64/32                    | 540000–54FFFF       | 2A0000–2A7FFF        |
| SA85   | 1010101 | 64/32                    | 550000–55FFFF       | 2A8000–2AFFFF        |
| SA86   | 1010110 | 64/32                    | 560000–56FFFF       | 2B0000–2B7FFF        |
| SA87   | 1010111 | 64/32                    | 570000–57FFFF       | 2B8000–2BFFFF        |
| SA88   | 1011000 | 64/32                    | 580000–58FFFF       | 2C0000–2C7FFF        |
| SA89   | 1011001 | 64/32                    | 590000–59FFFF       | 2C8000–2CFFFF        |
| SA90   | 1011010 | 64/32                    | 5A0000–5AFFFF       | 2D0000–2D7FFF        |
| SA91   | 1011011 | 64/32                    | 5B0000–5BFFFF       | 2D8000–2DFFFF        |
| SA92   | 1011100 | 64/32                    | 5C0000–5CFFFF       | 2E0000–2E7FFF        |
| SA93   | 1011101 | 64/32                    | 5D0000–5DFFFF       | 2E8000–2EFFFF        |
| SA94   | 1011110 | 64/32                    | 5E0000–5EFFFF       | 2F0000–2F7FFF        |
| SA95   | 1011111 | 64/32                    | 5F0000–5FFFFF       | 2F8000–2FFFFF        |
| SA96   | 1100000 | 64/32                    | 600000–60FFFF       | 300000–307FFF        |
| SA97   | 1100001 | 64/32                    | 610000–61FFFF       | 308000–30FFFF        |
| SA98   | 1100010 | 64/32                    | 620000–62FFFF       | 310000–317FFF        |
| SA99   | 1100011 | 64/32                    | 630000–63FFFF       | 318000–31FFFF        |
| SA100  | 1100100 | 64/32                    | 640000–64FFFF       | 320000–327FFF        |
| SA101  | 1100101 | 64/32                    | 650000–65FFFF       | 328000–32FFFF        |
| SA102  | 1100110 | 64/32                    | 660000–66FFFF       | 330000–337FFF        |
| SA103  | 1100111 | 64/32                    | 670000–67FFFF       | 338000–33FFFF        |
| SA104  | 1101000 | 64/32                    | 680000–68FFFF       | 340000–347FFF        |
| SA105  | 1101001 | 64/32                    | 690000–69FFFF       | 348000–34FFFF        |
| SA106  | 1101010 | 64/32                    | 6A0000–6AFFFF       | 350000–357FFF        |
| SA107  | 1101011 | 64/32                    | 6B0000–6BFFFF       | 358000–35FFFF        |
| SA108  | 1101100 | 64/32                    | 6C0000–6CFFFF       | 360000–367FFF        |
| SA109  | 1101101 | 64/32                    | 6D0000–6DFFFF       | 368000–36FFFF        |
| SA110  | 1101110 | 64/32                    | 6E0000–6EFFFF       | 370000–377FFF        |
| SA111  | 1101111 | 64/32                    | 6F0000–6FFFFF       | 378000–37FFFF        |
| SA112  | 1110000 | 64/32                    | 700000–70FFFF       | 380000–387FFF        |
| SA113  | 1110001 | 64/32                    | 710000–71FFFF       | 388000–38FFFF        |
| SA114  | 1110010 | 64/32                    | 720000–72FFFF       | 390000–397FFF        |
| SA115  | 1110011 | 64/32                    | 730000–73FFFF       | 398000–39FFFF        |
| SA116  | 1110100 | 64/32                    | 740000–74FFFF       | 3A0000–3A7FFF        |
| SA117  | 1110101 | 64/32                    | 750000–75FFFF       | 3A8000–3AFFFF        |
| SA118  | 1110110 | 64/32                    | 760000–76FFFF       | 3B0000–3B7FFF        |
| SA119  | 1110111 | 64/32                    | 770000–77FFFF       | 3B8000–3BFFFF        |
| SA120  | 1111000 | 64/32                    | 780000–78FFFF       | 3C0000–3C7FFF        |
| SA121  | 1111001 | 64/32                    | 790000–79FFFF       | 3C8000–3CFFFF        |
| SA122  | 1111010 | 64/32                    | 7A0000–7AFFFF       | 3D0000–3D7FFF        |
| SA123  | 1111011 | 64/32                    | 7B0000–7BFFFF       | 3D8000–3DFFFF        |
| SA124  | 1111100 | 64/32                    | 7C0000–7CFFFF       | 3E0000–3E7FFF        |
| SA125  | 1111101 | 64/32                    | 7D0000–7DFFFF       | 3E8000–3EFFFF        |
| SA126  | 1111110 | 64/32                    | 7E0000–7EFFFF       | 3F0000–3F7FFF        |
| SA127  | 1111111 | 64/32                    | 7F0000–7FFFFF       | 3F8000–3FFFFF        |

Table 7.8 S29GL064A (Model R3) Top Boot Sector Addresses (Sheet 1 of 2)

| Sector | A21-A12    | Sector Size (KB/Kwords) | 8-bit Address Range | 16-bit Address Range | Sector | A21-A12    | Sector Size (KB/Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|------------|-------------------------|---------------------|----------------------|--------|------------|-------------------------|---------------------|----------------------|
| SA0    | 0000000xxx | 64/32                   | 000000h-00FFFFh     | 00000h-07FFFh        | SA34   | 0100010xxx | 64/32                   | 220000h-22FFFFh     | 110000h-117FFFh      |
| SA1    | 0000001xxx | 64/32                   | 010000h-01FFFFh     | 08000h-0FFFFh        | SA35   | 0101011xxx | 64/32                   | 230000h-23FFFFh     | 118000h-11FFFFh      |
| SA2    | 0000010xxx | 64/32                   | 020000h-02FFFFh     | 10000h-17FFFh        | SA36   | 0100100xxx | 64/32                   | 240000h-24FFFFh     | 120000h-127FFFh      |
| SA3    | 0000011xxx | 64/32                   | 030000h-03FFFFh     | 18000h-1FFFFh        | SA37   | 0100101xxx | 64/32                   | 250000h-25FFFFh     | 128000h-12FFFFh      |
| SA4    | 0000100xxx | 64/32                   | 040000h-04FFFFh     | 20000h-27FFFh        | SA38   | 0100110xxx | 64/32                   | 260000h-26FFFFh     | 130000h-137FFFh      |
| SA5    | 0000101xxx | 64/32                   | 050000h-05FFFFh     | 28000h-2FFFFh        | SA39   | 0100111xxx | 64/32                   | 270000h-27FFFFh     | 138000h-13FFFFh      |
| SA6    | 0000110xxx | 64/32                   | 060000h-06FFFFh     | 30000h-37FFFh        | SA40   | 0101000xxx | 64/32                   | 280000h-28FFFFh     | 140000h-147FFFh      |
| SA7    | 0000111xxx | 64/32                   | 070000h-07FFFFh     | 38000h-3FFFFh        | SA41   | 0101001xxx | 64/32                   | 290000h-29FFFFh     | 148000h-14FFFFh      |
| SA8    | 0001000xxx | 64/32                   | 080000h-08FFFFh     | 40000h-47FFFh        | SA42   | 0101010xxx | 64/32                   | 2A0000h-2AFFFFh     | 150000h-157FFFh      |
| SA9    | 0001001xxx | 64/32                   | 090000h-09FFFFh     | 48000h-4FFFFh        | SA43   | 0101011xxx | 64/32                   | 2B0000h-2BFFFFh     | 158000h-15FFFFh      |
| SA10   | 0001010xxx | 64/32                   | 0A0000h-0AFFFFh     | 50000h-57FFFh        | SA44   | 0101100xxx | 64/32                   | 2C0000h-2CFFFFh     | 160000h-167FFFh      |
| SA11   | 0001011xxx | 64/32                   | 0B0000h-0BFFFFh     | 58000h-5FFFFh        | SA45   | 0101101xxx | 64/32                   | 2D0000h-2DFFFFh     | 168000h-16FFFFh      |
| SA12   | 0001100xxx | 64/32                   | 0C0000h-0CFFFFh     | 60000h-67FFFh        | SA46   | 0101110xxx | 64/32                   | 2E0000h-2EFFFFh     | 170000h-177FFFh      |
| SA13   | 0001101xxx | 64/32                   | 0D0000h-0DFFFFh     | 68000h-6FFFFh        | SA47   | 0101111xxx | 64/32                   | 2F0000h-2FFFFFh     | 178000h-17FFFFh      |
| SA14   | 0001101xxx | 64/32                   | 0E0000h-0EFFFFh     | 70000h-77FFFh        | SA48   | 0110000xxx | 64/32                   | 300000h-30FFFFh     | 180000h-187FFFh      |
| SA15   | 0001111xxx | 64/32                   | 0F0000h-0FFFFFh     | 78000h-7FFFFh        | SA49   | 0110001xxx | 64/32                   | 310000h-31FFFFh     | 188000h-18FFFFh      |
| SA16   | 0010000xxx | 64/32                   | 100000h-00FFFFh     | 80000h-87FFFh        | SA50   | 0110010xxx | 64/32                   | 320000h-32FFFFh     | 190000h-197FFFh      |
| SA17   | 0010001xxx | 64/32                   | 110000h-11FFFFh     | 88000h-8FFFFh        | SA51   | 0110011xxx | 64/32                   | 330000h-33FFFFh     | 198000h-19FFFFh      |
| SA18   | 0010010xxx | 64/32                   | 120000h-12FFFFh     | 90000h-97FFFh        | SA52   | 0100100xxx | 64/32                   | 340000h-34FFFFh     | 1A0000h-1A7FFFh      |
| SA19   | 0010011xxx | 64/32                   | 130000h-13FFFFh     | 98000h-9FFFFh        | SA53   | 0110101xxx | 64/32                   | 350000h-35FFFFh     | 1A8000h-1AFFFFh      |
| SA20   | 0010100xxx | 64/32                   | 140000h-14FFFFh     | A0000h-A7FFFh        | SA54   | 0110110xxx | 64/32                   | 360000h-36FFFFh     | 1B0000h-1B7FFFh      |
| SA21   | 0010101xxx | 64/32                   | 150000h-15FFFFh     | A8000h-AFFFFh        | SA55   | 0110111xxx | 64/32                   | 370000h-37FFFFh     | 1B8000h-1BFFFFh      |
| SA22   | 0010110xxx | 64/32                   | 160000h-16FFFFh     | B0000h-B7FFFh        | SA56   | 0111000xxx | 64/32                   | 380000h-38FFFFh     | 1C0000h-1C7FFFh      |
| SA23   | 0010111xxx | 64/32                   | 170000h-17FFFFh     | B8000h-BFFFFh        | SA57   | 0111001xxx | 64/32                   | 390000h-39FFFFh     | 1C8000h-1CFFFFh      |
| SA24   | 0011000xxx | 64/32                   | 180000h-18FFFFh     | C0000h-C7FFFh        | SA58   | 0111010xxx | 64/32                   | 3A0000h-3AFFFFh     | 1D0000h-1D7FFFh      |
| SA25   | 0011001xxx | 64/32                   | 190000h-19FFFFh     | C8000h-CFFFFh        | SA59   | 0111011xxx | 64/32                   | 3B0000h-3BFFFFh     | 1D8000h-1DFFFFh      |
| SA26   | 0011010xxx | 64/32                   | 1A0000h-1AFFFFh     | D0000h-D7FFFh        | SA60   | 0111100xxx | 64/32                   | 3C0000h-3CFFFFh     | 1E0000h-1E7FFFh      |
| SA27   | 0011011xxx | 64/32                   | 1B0000h-1BFFFFh     | D8000h-DFFFFh        | SA61   | 0111101xxx | 64/32                   | 3D0000h-3DFFFFh     | 1E8000h-1EFFFFh      |
| SA28   | 0011000xxx | 64/32                   | 1C0000h-1CFFFFh     | E0000h-E7FFFh        | SA62   | 0111110xxx | 64/32                   | 3E0000h-3EFFFFh     | 1F0000h-1F7FFFh      |
| SA29   | 0011101xxx | 64/32                   | 1D0000h-1DFFFFh     | E8000h-EFFFFh        | SA63   | 0111111xxx | 64/32                   | 3F0000h-3FFFFFh     | 1F8000h-1FFFFFh      |
| SA30   | 0011110xxx | 64/32                   | 1E0000h-1EFFFFh     | F0000h-F7FFFh        | SA64   | 1000000xxx | 64/32                   | 400000h-40FFFFh     | 200000h-207FFFh      |
| SA31   | 0011111xxx | 64/32                   | 1F0000h-1FFFFFh     | F8000h-FFFFFh        | SA65   | 1000001xxx | 64/32                   | 410000h-41FFFFh     | 208000h-20FFFFh      |
| SA32   | 0100000xxx | 64/32                   | 200000h-20FFFFh     | F9000h-107FFFh       | SA66   | 1000010xxx | 64/32                   | 420000h-42FFFFh     | 210000h-217FFFh      |
| SA33   | 0100001xxx | 64/32                   | 210000h-21FFFFh     | 108000h-10FFFFh      | SA67   | 1000011xxx | 64/32                   | 430000h-43FFFFh     | 218000h-21FFFFh      |



Table 7.8 S29GL064A (Model R3) Top Boot Sector Addresses (Sheet 2 of 2)

| Sector | A21-A12    | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range | Sector | A21-A12     | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|------------|--------------------------|---------------------|----------------------|--------|-------------|--------------------------|---------------------|----------------------|
| SA68   | 1000100xxx | 64/32                    | 440000h-44FFFFh     | 220000h-227FFFh      | SA102  | 1100110xxx  | 64/32                    | 660000h-66FFFFh     | 330000h-337FFFh      |
| SA69   | 1000101xxx | 64/32                    | 450000h-45FFFFh     | 228000h-22FFFFh      | SA103  | 1100111xxx  | 64/32                    | 670000h-67FFFFh     | 338000h-33FFFFh      |
| SA70   | 1000110xxx | 64/32                    | 460000h-46FFFFh     | 230000h-237FFFh      | SA104  | 1101000xxx  | 64/32                    | 680000h-68FFFFh     | 340000h-347FFFh      |
| SA71   | 1000111xxx | 64/32                    | 470000h-47FFFFh     | 238000h-23FFFFh      | SA105  | 1101001xxx  | 64/32                    | 690000h-69FFFFh     | 348000h-34FFFFh      |
| SA72   | 1001000xxx | 64/32                    | 480000h-48FFFFh     | 240000h-247FFFh      | SA106  | 1101010xxx  | 64/32                    | 6A0000h-6AFFFFh     | 350000h-357FFFh      |
| SA73   | 1001001xxx | 64/32                    | 490000h-49FFFFh     | 248000h-24FFFFh      | SA107  | 1101011xxx  | 64/32                    | 6B0000h-6BFFFFh     | 358000h-35FFFFh      |
| SA74   | 1001010xxx | 64/32                    | 4A0000h-4AFFFFh     | 250000h-257FFFh      | SA108  | 1101100xxx  | 64/32                    | 6C0000h-6CFFFFh     | 360000h-367FFFh      |
| SA75   | 1001011xxx | 64/32                    | 4B0000h-4BFFFFh     | 258000h-25FFFFh      | SA109  | 1101101xxx  | 64/32                    | 6D0000h-6DFFFFh     | 368000h-36FFFFh      |
| SA76   | 1001100xxx | 64/32                    | 4C0000h-4CFFFFh     | 260000h-267FFFh      | SA110  | 1101110xxx  | 64/32                    | 6E0000h-6EFFFFh     | 370000h-377FFFh      |
| SA77   | 1001101xxx | 64/32                    | 4D0000h-4DFFFFh     | 268000h-26FFFFh      | SA111  | 1101111xxx  | 64/32                    | 6F0000h-6FFFFFh     | 378000h-37FFFFh      |
| SA78   | 1001110xxx | 64/32                    | 4E0000h-4EFFFFh     | 270000h-277FFFh      | SA112  | 1110000xxx  | 64/32                    | 700000h-70FFFFh     | 380000h-387FFFh      |
| SA79   | 1001111xxx | 64/32                    | 4F0000h-4FFFFFh     | 278000h-277FFFh      | SA113  | 1110001xxx  | 64/32                    | 710000h-71FFFFh     | 388000h-38FFFFh      |
| SA80   | 1010000xxx | 64/32                    | 500000h-50FFFFh     | 280000h-28FFFFh      | SA114  | 1110010xxx  | 64/32                    | 720000h-72FFFFh     | 390000h-397FFFh      |
| SA81   | 1010001xxx | 64/32                    | 510000h-51FFFFh     | 288000h-28FFFFh      | SA115  | 1110011xxx  | 64/32                    | 730000h-73FFFFh     | 398000h-39FFFFh      |
| SA82   | 1010010xxx | 64/32                    | 520000h-52FFFFh     | 290000h-297FFFh      | SA116  | 1110100xxx  | 64/32                    | 740000h-74FFFFh     | 3A0000h-3A7FFFh      |
| SA83   | 1010011xxx | 64/32                    | 530000h-53FFFFh     | 298000h-29FFFFh      | SA117  | 1110101xxx  | 64/32                    | 750000h-75FFFFh     | 3A8000h-3AFFFFh      |
| SA84   | 1010100xxx | 64/32                    | 540000h-54FFFFh     | 2A0000h-2A7FFFh      | SA118  | 1110110xxx  | 64/32                    | 760000h-76FFFFh     | 3B0000h-3B7FFFh      |
| SA85   | 1010101xxx | 64/32                    | 550000h-55FFFFh     | 2A8000h-2AFFFFh      | SA119  | 1110111xxx  | 64/32                    | 770000h-77FFFFh     | 3B8000h-3BFFFFh      |
| SA86   | 1010110xxx | 64/32                    | 560000h-56FFFFh     | 2B0000h-2B7FFFh      | SA120  | 1111000xxx  | 64/32                    | 780000h-78FFFFh     | 3C0000h-3C7FFFh      |
| SA87   | 1010111xxx | 64/32                    | 570000h-57FFFFh     | 2B8000h-2BFFFFh      | SA121  | 1111001xxx  | 64/32                    | 790000h-79FFFFh     | 3C8000h-3CFFFFh      |
| SA88   | 1011000xxx | 64/32                    | 580000h-58FFFFh     | 2C0000h-2C7FFFh      | SA122  | 1111010xxx  | 64/32                    | 7A0000h-7AFFFFh     | 3D0000h-3D7FFFh      |
| SA89   | 1011001xxx | 64/32                    | 590000h-59FFFFh     | 2C8000h-2CFFFFh      | SA123  | 1111011xxx  | 64/32                    | 7B0000h-7BFFFFh     | 3D8000h-3DFFFFh      |
| SA90   | 1011010xxx | 64/32                    | 5A0000h-5AFFFFh     | 2D0000h-2D7FFFh      | SA124  | 1111100xxx  | 64/32                    | 7C0000h-7CFFFFh     | 3E0000h-3E7FFFh      |
| SA91   | 1011011xxx | 64/32                    | 5B0000h-5BFFFFh     | 2D8000h-2DFFFFh      | SA125  | 1111101xxx  | 64/32                    | 7D0000h-7DFFFFh     | 3E8000h-3EFFFFh      |
| SA92   | 1011100xxx | 64/32                    | 5C0000h-5CFFFFh     | 2E0000h-2E7FFFh      | SA126  | 1111110xxx  | 64/32                    | 7E0000h-7EFFFFh     | 3F0000h-3F7FFFh      |
| SA93   | 1011101xxx | 64/32                    | 5D0000h-5DFFFFh     | 2E8000h-2EFFFFh      | SA127  | 1111111000  | 8/4                      | 7F0000h-7F1FFFh     | 3F8000h-3F8FFFh      |
| SA94   | 1011110xxx | 64/32                    | 5E0000h-5EFFFFh     | 2F0000h-2FFFFFh      | SA128  | 11111111001 | 8/4                      | 7F2000h-7F3FFFh     | 3F9000h-3F9FFFh      |
| SA95   | 1011111xxx | 64/32                    | 5F0000h-5FFFFFh     | 2F8000h-2FFFFFh      | SA129  | 11111111010 | 8/4                      | 7F4000h-7F5FFFh     | 3FA000h-3FAFFFh      |
| SA96   | 1100000xxx | 64/32                    | 600000h-60FFFFh     | 300000h-307FFFh      | SA130  | 11111111011 | 8/4                      | 7F6000h-7F7FFFh     | 3FB000h-3FBFFFh      |
| SA97   | 1100001xxx | 64/32                    | 610000h-61FFFFh     | 308000h-30FFFFh      | SA131  | 11111111100 | 8/4                      | 7F8000h-7F9FFFh     | 3FC000h-3FCFFFh      |
| SA98   | 1100010xxx | 64/32                    | 620000h-62FFFFh     | 310000h-317FFFh      | SA132  | 11111111101 | 8/4                      | 7FA000h-7FBFFFh     | 3FD000h-3FDFFFh      |
| SA99   | 1100011xxx | 64/32                    | 630000h-63FFFFh     | 318000h-31FFFFh      | SA133  | 11111111110 | 8/4                      | 7FC000h-7FDFFFh     | 3FE000h-3FEFFFh      |
| SA100  | 1100100xxx | 64/32                    | 640000h-64FFFFh     | 320000h-327FFFh      | SA134  | 11111111111 | 8/4                      | 7FE000h-7FFFFFh     | 3FF000h-3FFFFFh      |
| SA101  | 1100101xxx | 64/32                    | 650000h-65FFFFh     | 328000h-32FFFFh      |        |             |                          |                     |                      |

Table 7.9 S29GL064A (Model R4) Bottom Boot Sector Addresses (Sheet 1 of 2)

| Sector | A21–A12    | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range | Sector | A21–A12    | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|------------|--------------------------|---------------------|----------------------|--------|------------|--------------------------|---------------------|----------------------|
| SA0    | 0000000000 | 8/4                      | 00000h–001FFFh      | 00000h–00FFFh        | SA27   | 0010100xxx | 64/32                    | 140000h–14FFFFh     | A0000h–A7FFFh        |
| SA1    | 0000000001 | 8/4                      | 002000h–003FFFh     | 01000h–01FFFh        | SA28   | 0010101xxx | 64/32                    | 150000h–15FFFFh     | A8000h–AFFFFh        |
| SA2    | 0000000010 | 8/4                      | 004000h–005FFFh     | 02000h–02FFFh        | SA29   | 0010110xxx | 64/32                    | 160000h–16FFFFh     | B0000h–B7FFFh        |
| SA3    | 0000000011 | 8/4                      | 006000h–007FFFh     | 03000h–03FFFh        | SA30   | 0010111xxx | 64/32                    | 170000h–17FFFFh     | B8000h–BFFFFh        |
| SA4    | 0000000100 | 8/4                      | 008000h–009FFFh     | 04000h–04FFFh        | SA31   | 0011000xxx | 64/32                    | 180000h–18FFFFh     | C0000h–C7FFFh        |
| SA5    | 0000000101 | 8/4                      | 00A000h–00BFFFh     | 05000h–05FFFh        | SA32   | 0011001xxx | 64/32                    | 190000h–19FFFFh     | C8000h–CFFFFh        |
| SA6    | 0000000110 | 8/4                      | 00C000h–00DFFFh     | 06000h–06FFFh        | SA33   | 0011010xxx | 64/32                    | 1A0000h–1AFFFFh     | D0000h–D7FFFh        |
| SA7    | 0000000111 | 8/4                      | 00E000h–00FFFFh     | 07000h–07FFFh        | SA34   | 0011011xxx | 64/32                    | 1B0000h–1BFFFFh     | D8000h–DFFFFh        |
| SA8    | 0000001xxx | 64/32                    | 010000h–01FFFh      | 08000h–0FFFFh        | SA35   | 0011000xxx | 64/32                    | 1C0000h–1CFFFFh     | E0000h–E7FFFh        |
| SA9    | 0000010xxx | 64/32                    | 020000h–02FFFh      | 10000h–17FFFh        | SA36   | 0011101xxx | 64/32                    | 1D0000h–1DFFFFh     | E8000h–EFFFFh        |
| SA10   | 0000011xxx | 64/32                    | 030000h–03FFFh      | 18000h–1FFFFh        | SA37   | 0011110xxx | 64/32                    | 1E0000h–1EFFFFh     | F0000h–F7FFFh        |
| SA11   | 0000100xxx | 64/32                    | 040000h–04FFFh      | 20000h–27FFFh        | SA38   | 0011111xxx | 64/32                    | 1F0000h–1FFFFh      | F8000h–FFFFh         |
| SA12   | 0000101xxx | 64/32                    | 050000h–05FFFh      | 28000h–2FFFFh        | SA39   | 0100000xxx | 64/32                    | 200000h–20FFFFh     | F9000h–107FFFh       |
| SA13   | 0000110xxx | 64/32                    | 060000h–06FFFh      | 30000h–37FFFh        | SA40   | 0100001xxx | 64/32                    | 210000h–21FFFFh     | 108000h–10FFFFh      |
| SA14   | 0000111xxx | 64/32                    | 070000h–07FFFh      | 38000h–3FFFFh        | SA41   | 0100010xxx | 64/32                    | 220000h–22FFFFh     | 110000h–117FFFh      |
| SA15   | 0001000xxx | 64/32                    | 080000h–08FFFh      | 40000h–47FFFh        | SA42   | 0101011xxx | 64/32                    | 230000h–23FFFFh     | 118000h–11FFFFh      |
| SA16   | 0001001xxx | 64/32                    | 090000h–09FFFh      | 48000h–4FFFFh        | SA43   | 0100100xxx | 64/32                    | 240000h–24FFFFh     | 120000h–127FFFh      |
| SA17   | 0001010xxx | 64/32                    | 0A0000h–0AFFFh      | 50000h–57FFFh        | SA44   | 0100101xxx | 64/32                    | 250000h–25FFFFh     | 128000h–12FFFFh      |
| SA18   | 0001011xxx | 64/32                    | 0B0000h–0BFFFh      | 58000h–5FFFFh        | SA45   | 0100110xxx | 64/32                    | 260000h–26FFFFh     | 130000h–137FFFh      |
| SA19   | 0001100xxx | 64/32                    | 0C0000h–0CFFFh      | 60000h–67FFFh        | SA46   | 0100111xxx | 64/32                    | 270000h–27FFFFh     | 138000h–13FFFFh      |
| SA20   | 0001101xxx | 64/32                    | 0D0000h–0DFFFh      | 68000h–6FFFFh        | SA47   | 0101000xxx | 64/32                    | 280000h–28FFFFh     | 140000h–147FFFh      |
| SA21   | 0001101xxx | 64/32                    | 0E0000h–0EFFFh      | 70000h–77FFFh        | SA48   | 0101001xxx | 64/32                    | 290000h–29FFFFh     | 148000h–14FFFFh      |
| SA22   | 0001111xxx | 64/32                    | 0F0000h–0FFFFh      | 78000h–77FFFh        | SA49   | 0101010xxx | 64/32                    | 2A0000h–2AFFFFh     | 150000h–157FFFh      |
| SA23   | 0010000xxx | 64/32                    | 100000h–00FFFh      | 80000h–87FFFh        | SA50   | 0101011xxx | 64/32                    | 2B0000h–2BFFFFh     | 158000h–15FFFFh      |
| SA24   | 0010001xxx | 64/32                    | 110000h–11FFFh      | 88000h–8FFFFh        | SA51   | 0101100xxx | 64/32                    | 2C0000h–2CFFFFh     | 160000h–167FFFh      |
| SA25   | 0010010xxx | 64/32                    | 120000h–12FFFh      | 90000h–97FFFh        | SA52   | 0101101xxx | 64/32                    | 2D0000h–2DFFFFh     | 168000h–16FFFFh      |
| SA26   | 0010011xxx | 64/32                    | 130000h–13FFFh      | 98000h–9FFFFh        | SA53   | 0101110xxx | 64/32                    | 2E0000h–2EFFFFh     | 170000h–177FFFh      |

Table 7.9 S29GL064A (Model R4) Bottom Boot Sector Addresses (Sheet 2 of 2)

| Sector | A21–A12    | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range | Sector | A21–A12    | Sector Size (KB/ Kwords) | 8-bit Address Range | 16-bit Address Range |
|--------|------------|--------------------------|---------------------|----------------------|--------|------------|--------------------------|---------------------|----------------------|
| SA54   | 0101111xxx | 64/32                    | 2F0000h–2FFFFFh     | 178000h–17FFFFh      | SA95   | 1011000xxx | 64/32                    | 580000h–58FFFFh     | 2C0000h–2C7FFFh      |
| SA55   | 0110000xxx | 64/32                    | 300000h–30FFFFh     | 180000h–187FFFh      | SA96   | 1011001xxx | 64/32                    | 590000h–59FFFFh     | 2C8000h–2CFFFFh      |
| SA56   | 0110001xxx | 64/32                    | 310000h–31FFFFh     | 188000h–18FFFFh      | SA97   | 1011010xxx | 64/32                    | 5A0000h–5AFFFFh     | 2D0000h–2D7FFFh      |
| SA57   | 0110010xxx | 64/32                    | 320000h–32FFFFh     | 190000h–197FFFh      | SA98   | 1011011xxx | 64/32                    | 5B0000h–5BFFFFh     | 2D8000h–2DFFFFh      |
| SA58   | 0110011xxx | 64/32                    | 330000h–33FFFFh     | 198000h–19FFFFh      | SA99   | 1011100xxx | 64/32                    | 5C0000h–5CFFFFh     | 2E0000h–2E7FFFh      |
| SA59   | 0100100xxx | 64/32                    | 340000h–34FFFFh     | 1A0000h–1A7FFFh      | SA100  | 1011101xxx | 64/32                    | 5D0000h–5DFFFFh     | 2E8000h–2EFFFFh      |
| SA60   | 0110101xxx | 64/32                    | 350000h–35FFFFh     | 1A8000h–1AFFFFh      | SA101  | 1011110xxx | 64/32                    | 5E0000h–5EFFFFh     | 2F0000h–2FFFFFh      |
| SA61   | 0110110xxx | 64/32                    | 360000h–36FFFFh     | 1B0000h–1B7FFFh      | SA102  | 1011111xxx | 64/32                    | 5F0000h–5FFFFFh     | 2F8000h–2FFFFFh      |
| SA62   | 0110111xxx | 64/32                    | 370000h–37FFFFh     | 1B8000h–1BFFFFh      | SA103  | 1100000xxx | 64/32                    | 600000h–60FFFFh     | 300000h–307FFFh      |
| SA63   | 0111000xxx | 64/32                    | 380000h–38FFFFh     | 1C0000h–1C7FFFh      | SA104  | 1100001xxx | 64/32                    | 610000h–61FFFFh     | 308000h–30FFFFh      |
| SA64   | 0111001xxx | 64/32                    | 390000h–39FFFFh     | 1C8000h–1CFFFFh      | SA105  | 1100010xxx | 64/32                    | 620000h–62FFFFh     | 310000h–317FFFh      |
| SA65   | 0111010xxx | 64/32                    | 3A0000h–3AFFFFh     | 1D0000h–1D7FFFh      | SA106  | 1100011xxx | 64/32                    | 630000h–63FFFFh     | 318000h–31FFFFh      |
| SA66   | 0111011xxx | 64/32                    | 3B0000h–3BFFFFh     | 1D8000h–1DFFFFh      | SA107  | 1100100xxx | 64/32                    | 640000h–64FFFFh     | 320000h–327FFFh      |
| SA67   | 0111100xxx | 64/32                    | 3C0000h–3CFFFFh     | 1E0000h–1E7FFFh      | SA108  | 1100101xxx | 64/32                    | 650000h–65FFFFh     | 328000h–32FFFFh      |
| SA68   | 0111101xxx | 64/32                    | 3D0000h–3DFFFFh     | 1E8000h–1EFFFFh      | SA109  | 1100110xxx | 64/32                    | 660000h–66FFFFh     | 330000h–337FFFh      |
| SA69   | 0111110xxx | 64/32                    | 3E0000h–3EFFFFh     | 1F0000h–1F7FFFh      | SA110  | 1100111xxx | 64/32                    | 670000h–67FFFFh     | 338000h–33FFFFh      |
| SA70   | 0111111xxx | 64/32                    | 3F0000h–3FFFFFh     | 1F8000h–1FFFFFh      | SA111  | 1101000xxx | 64/32                    | 680000h–68FFFFh     | 340000h–347FFFh      |
| SA71   | 1000000xxx | 64/32                    | 400000h–40FFFFh     | 200000h–207FFFh      | SA112  | 1101001xxx | 64/32                    | 690000h–69FFFFh     | 348000h–34FFFFh      |
| SA72   | 1000001xxx | 64/32                    | 410000h–41FFFFh     | 208000h–20FFFFh      | SA113  | 1101010xxx | 64/32                    | 6A0000h–6AFFFFh     | 350000h–357FFFh      |
| SA73   | 1000010xxx | 64/32                    | 420000h–42FFFFh     | 210000h–217FFFh      | SA114  | 1101011xxx | 64/32                    | 6B0000h–6BFFFFh     | 358000h–35FFFFh      |
| SA74   | 1000011xxx | 64/32                    | 430000h–43FFFFh     | 218000h–21FFFFh      | SA115  | 1101100xxx | 64/32                    | 6C0000h–6CFFFFh     | 360000h–367FFFh      |
| SA75   | 1000100xxx | 64/32                    | 440000h–44FFFFh     | 220000h–227FFFh      | SA116  | 1101101xxx | 64/32                    | 6D0000h–6DFFFFh     | 368000h–36FFFFh      |
| SA76   | 1000101xxx | 64/32                    | 450000h–45FFFFh     | 228000h–22FFFFh      | SA117  | 1101110xxx | 64/32                    | 6E0000h–6EFFFFh     | 370000h–377FFFh      |
| SA77   | 1000110xxx | 64/32                    | 460000h–46FFFFh     | 230000h–237FFFh      | SA118  | 1101111xxx | 64/32                    | 6F0000h–6FFFFFh     | 378000h–37FFFFh      |
| SA78   | 1000111xxx | 64/32                    | 470000h–47FFFFh     | 238000h–23FFFFh      | SA119  | 1110000xxx | 64/32                    | 700000h–70FFFFh     | 380000h–387FFFh      |
| SA79   | 1001000xxx | 64/32                    | 480000h–48FFFFh     | 240000h–247FFFh      | SA120  | 1110001xxx | 64/32                    | 710000h–71FFFFh     | 388000h–38FFFFh      |
| SA80   | 1001001xxx | 64/32                    | 490000h–49FFFFh     | 248000h–24FFFFh      | SA121  | 1110010xxx | 64/32                    | 720000h–72FFFFh     | 390000h–397FFFh      |
| SA81   | 1001010xxx | 64/32                    | 4A0000h–4AFFFFh     | 250000h–257FFFh      | SA122  | 1110011xxx | 64/32                    | 730000h–73FFFFh     | 398000h–39FFFFh      |
| SA82   | 1001011xxx | 64/32                    | 4B0000h–4BFFFFh     | 258000h–25FFFFh      | SA123  | 1110100xxx | 64/32                    | 740000h–74FFFFh     | 3A0000h–3A7FFFh      |
| SA83   | 1001100xxx | 64/32                    | 4C0000h–4CFFFFh     | 260000h–267FFFh      | SA124  | 1110101xxx | 64/32                    | 750000h–75FFFFh     | 3A8000h–3AFFFFh      |
| SA84   | 1001101xxx | 64/32                    | 4D0000h–4DFFFFh     | 268000h–26FFFFh      | SA125  | 1110110xxx | 64/32                    | 760000h–76FFFFh     | 3B0000h–3B7FFFh      |
| SA85   | 1001110xxx | 64/32                    | 4E0000h–4EFFFFh     | 270000h–277FFFh      | SA126  | 1110111xxx | 64/32                    | 770000h–77FFFFh     | 3B8000h–3BFFFFh      |
| SA86   | 1001111xxx | 64/32                    | 4F0000h–4FFFFFh     | 278000h–27FFFFh      | SA127  | 1111000xxx | 64/32                    | 780000h–78FFFFh     | 3C0000h–3C7FFFh      |
| SA87   | 1010000xxx | 64/32                    | 500000h–50FFFFh     | 280000h–287FFFh      | SA128  | 1111001xxx | 64/32                    | 790000h–79FFFFh     | 3C8000h–3CFFFFh      |
| SA88   | 1010001xxx | 64/32                    | 510000h–51FFFFh     | 288000h–28FFFFh      | SA129  | 1111010xxx | 64/32                    | 7A0000h–7AFFFFh     | 3D0000h–3D7FFFh      |
| SA89   | 1010010xxx | 64/32                    | 520000h–52FFFFh     | 290000h–297FFFh      | SA130  | 1111011xxx | 64/32                    | 7B0000h–7BFFFFh     | 3D8000h–3DFFFFh      |
| SA90   | 1010011xxx | 64/32                    | 530000h–53FFFFh     | 298000h–29FFFFh      | SA131  | 1111100xxx | 64/32                    | 7C0000h–7CFFFFh     | 3E0000h–3E7FFFh      |
| SA91   | 1010100xxx | 64/32                    | 540000h–54FFFFh     | 2A0000h–2A7FFFh      | SA132  | 1111101xxx | 64/32                    | 7D0000h–7DFFFFh     | 3E8000h–3EFFFFh      |
| SA92   | 1010101xxx | 64/32                    | 550000h–55FFFFh     | 2A8000h–2AFFFFh      | SA133  | 1111110xxx | 64/32                    | 7E0000h–7EFFFFh     | 3F0000h–3F7FFFh      |
| SA93   | 1010110xxx | 64/32                    | 560000h–56FFFFh     | 2B0000h–2B7FFFh      | SA134  | 1111111000 | 64/32                    | 7F0000h–7FFFFFh     | 3F8000h–3FFFFFh      |
| SA94   | 1010111xxx | 64/32                    | 570000h–57FFFFh     | 2B8000h–2BFFFFh      |        |            |                          |                     |                      |

**Table 7.10** S29GL064A (Model R5) Sector Addresses (Sheet 1 of 2)

| Sector | A21–A15 | 16-bit Address Range |
|--------|---------|----------------------|
| SA0    | 0000000 | 000000–007FFF        |
| SA1    | 0000001 | 008000–00FFFF        |
| SA2    | 0000010 | 010000–017FFF        |
| SA3    | 0000011 | 018000–01FFFF        |
| SA4    | 0000100 | 020000–027FFF        |
| SA5    | 0000101 | 028000–02FFFF        |
| SA6    | 0000110 | 030000–037FFF        |
| SA7    | 0000111 | 038000–03FFFF        |
| SA8    | 0001000 | 040000–047FFF        |
| SA9    | 0001001 | 048000–04FFFF        |
| SA10   | 0001010 | 050000–057FFF        |
| SA11   | 0001011 | 058000–05FFFF        |
| SA12   | 0001100 | 060000–067FFF        |
| SA13   | 0001101 | 068000–06FFFF        |
| SA14   | 0001110 | 070000–077FFF        |
| SA15   | 0001111 | 078000–07FFFF        |
| SA16   | 0010000 | 080000–087FFF        |
| SA17   | 0010001 | 088000–08FFFF        |
| SA18   | 0010010 | 090000–097FFF        |
| SA19   | 0010011 | 098000–09FFFF        |
| SA20   | 0010100 | 0A0000–0A7FFF        |

| Sector | A21–A15 | 16-bit Address Range |
|--------|---------|----------------------|
| SA21   | 0010101 | 0A8000–0AFFFF        |
| SA22   | 0010110 | 0B0000–0B7FFF        |
| SA23   | 0010111 | 0B8000–0BFFFF        |
| SA24   | 0011000 | 0C0000–0C7FFF        |
| SA25   | 0011001 | 0C8000–0CFFFF        |
| SA26   | 0011010 | 0D0000–0D7FFF        |
| SA27   | 0011011 | 0D8000–0DFFFF        |
| SA28   | 0011100 | 0E0000–0E7FFF        |
| SA29   | 0011101 | 0E8000–0EFFFF        |
| SA30   | 0011110 | 0F0000–0F7FFF        |
| SA31   | 0011111 | 0F8000–0FFFFF        |
| SA32   | 0100000 | 200000–207FFF        |
| SA33   | 0100001 | 208000–20FFFF        |
| SA34   | 0100010 | 210000–217FFF        |
| SA35   | 0100011 | 218000–21FFFF        |
| SA36   | 0100100 | 220000–227FFF        |
| SA37   | 0100101 | 228000–22FFFF        |
| SA38   | 0100110 | 230000–237FFF        |
| SA39   | 0100111 | 238000–23FFFF        |
| SA40   | 0101000 | 240000–247FFF        |
| SA41   | 0101001 | 248000–24FFFF        |

Table 7.10 S29GL064A (Model R5) Sector Addresses (Sheet 2 of 2)

| Sector | A21–A15 | 16-bit Address Range |
|--------|---------|----------------------|
| SA42   | 0101010 | 250000–257FFF        |
| SA43   | 0101011 | 258000–25FFFF        |
| SA44   | 0101100 | 260000–267FFF        |
| SA45   | 0101101 | 268000–26FFFF        |
| SA46   | 0101110 | 270000–277FFF        |
| SA47   | 0101111 | 278000–27FFFF        |
| SA48   | 0110000 | 280000–287FFF        |
| SA49   | 0110001 | 288000–28FFFF        |
| SA50   | 0110010 | 290000–297FFF        |
| SA51   | 0110011 | 298000–29FFFF        |
| SA52   | 0110100 | 2A0000–2A7FFF        |
| SA53   | 0110101 | 2A8000–2AFFFF        |
| SA54   | 0110110 | 2B0000–2B7FFF        |
| SA55   | 0110111 | 2B8000–2BFFFF        |
| SA56   | 0111000 | 2C0000–2C7FFF        |
| SA57   | 0111001 | 2C8000–2CFFFF        |
| SA58   | 0111010 | 2D0000–2D7FFF        |
| SA59   | 0111011 | 2D8000–2DFFFF        |
| SA60   | 0111100 | 2E0000–2E7FFF        |
| SA61   | 0111101 | 2E8000–2EFFFF        |
| SA62   | 0111110 | 2F0000–2F7FFF        |
| SA63   | 0111111 | 2F8000–2FFFFF        |
| SA64   | 1000000 | 100000–107FFF        |
| SA65   | 1000001 | 108000–10FFFF        |
| SA66   | 1000010 | 110000–117FFF        |
| SA67   | 1000011 | 118000–11FFFF        |
| SA68   | 1000100 | 120000–127FFF        |
| SA69   | 1000101 | 128000–12FFFF        |
| SA70   | 1000110 | 130000–137FFF        |
| SA71   | 1000111 | 138000–13FFFF        |
| SA72   | 1001000 | 140000–147FFF        |
| SA73   | 1001001 | 148000–14FFFF        |
| SA74   | 1001010 | 150000–157FFF        |
| SA75   | 1001011 | 158000–15FFFF        |
| SA76   | 1001100 | 160000–167FFF        |
| SA77   | 1001101 | 168000–16FFFF        |
| SA78   | 1001110 | 170000–177FFF        |
| SA79   | 1001111 | 178000–17FFFF        |
| SA80   | 1010000 | 180000–187FFF        |
| SA81   | 1010001 | 188000–18FFFF        |
| SA82   | 1010010 | 190000–197FFF        |
| SA83   | 1010011 | 198000–19FFFF        |
| SA84   | 1010100 | 1A0000–1A7FFF        |

| Sector | A21–A15 | 16-bit Address Range |
|--------|---------|----------------------|
| SA85   | 1010101 | 1A8000–1AFFFF        |
| SA86   | 1010110 | 1B0000–1B7FFF        |
| SA87   | 1010111 | 1B8000–1BFFFF        |
| SA88   | 1011000 | 1C0000–1C7FFF        |
| SA89   | 1011001 | 1C8000–1CFFFF        |
| SA90   | 1011010 | 1D0000–1D7FFF        |
| SA91   | 1011011 | 1D8000–1DFFFF        |
| SA92   | 1011100 | 1E0000–1E7FFF        |
| SA93   | 1011101 | 1E8000–1EFFFF        |
| SA94   | 1011110 | 1F0000–1F7FFF        |
| SA95   | 1011111 | 1F8000–1FFFFF        |
| SA96   | 1100000 | 300000–307FFF        |
| SA97   | 1100001 | 308000–30FFFF        |
| SA98   | 1100010 | 310000–317FFF        |
| SA99   | 1100011 | 318000–31FFFF        |
| SA100  | 1100100 | 320000–327FFF        |
| SA101  | 1100101 | 328000–32FFFF        |
| SA102  | 1100110 | 330000–337FFF        |
| SA103  | 1100111 | 338000–33FFFF        |
| SA104  | 1101000 | 340000–347FFF        |
| SA105  | 1101001 | 348000–34FFFF        |
| SA106  | 1101010 | 350000–357FFF        |
| SA107  | 1101011 | 358000–35FFFF        |
| SA108  | 1101100 | 360000–367FFF        |
| SA109  | 1101101 | 368000–36FFFF        |
| SA110  | 1101110 | 370000–377FFF        |
| SA111  | 1101111 | 378000–37FFFF        |
| SA112  | 1110000 | 380000–387FFF        |
| SA113  | 1110001 | 388000–38FFFF        |
| SA114  | 1110010 | 390000–397FFF        |
| SA115  | 1110011 | 398000–39FFFF        |
| SA116  | 1110100 | 3A0000–3A7FFF        |
| SA117  | 1110101 | 3A8000–3AFFFF        |
| SA118  | 1110110 | 3B0000–3B7FFF        |
| SA119  | 1110111 | 3B8000–3BFFFF        |
| SA120  | 1111000 | 3C0000–3C7FFF        |
| SA121  | 1111001 | 3C8000–3CFFFF        |
| SA122  | 1111010 | 3D0000–3D7FFF        |
| SA123  | 1111011 | 3D8000–3DFFFF        |
| SA124  | 1111100 | 3E0000–3E7FFF        |
| SA125  | 1111101 | 3E8000–3EFFFF        |
| SA126  | 1111110 | 3F0000–3F7FFF        |
| SA127  | 1111111 | 3F8000–3FFFFF        |

**Table 7.11** S29GL064A (Models R6, R7) Sector Addresses (Sheet 1 of 2)

| Sector | A21–A15 | 16-bit Address Range | Sector | A21–A15 | 16-bit Address Range |
|--------|---------|----------------------|--------|---------|----------------------|
| SA0    | 0000000 | 000000–007FFF        | SA21   | 0010101 | 0A8000–0AFFFF        |
| SA1    | 0000001 | 008000–00FFFF        | SA22   | 0010110 | 0B0000–0B7FFF        |
| SA2    | 0000010 | 010000–017FFF        | SA23   | 0010111 | 0B8000–0BFFFF        |
| SA3    | 0000011 | 018000–01FFFF        | SA24   | 0011000 | 0C0000–0C7FFF        |
| SA4    | 0000100 | 020000–027FFF        | SA25   | 0011001 | 0C8000–0CFFFF        |
| SA5    | 0000101 | 028000–02FFFF        | SA26   | 0011010 | 0D0000–0D7FFF        |
| SA6    | 0000110 | 030000–037FFF        | SA27   | 0011011 | 0D8000–0DFFFF        |
| SA7    | 0000111 | 038000–03FFFF        | SA28   | 0011100 | 0E0000–0E7FFF        |
| SA8    | 0001000 | 040000–047FFF        | SA29   | 0011101 | 0E8000–0EFFFF        |
| SA9    | 0001001 | 048000–04FFFF        | SA30   | 0011110 | 0F0000–0F7FFF        |
| SA10   | 0001010 | 050000–057FFF        | SA31   | 0011111 | 0F8000–0FFFFF        |
| SA11   | 0001011 | 058000–05FFFF        | SA32   | 0100000 | 100000–107FFF        |
| SA12   | 0001100 | 060000–067FFF        | SA33   | 0100001 | 108000–10FFFF        |
| SA13   | 0001101 | 068000–06FFFF        | SA34   | 0100010 | 110000–117FFF        |
| SA14   | 0001110 | 070000–077FFF        | SA35   | 0100011 | 118000–11FFFF        |
| SA15   | 0001111 | 078000–07FFFF        | SA36   | 0100100 | 120000–127FFF        |
| SA16   | 0010000 | 080000–087FFF        | SA37   | 0100101 | 128000–12FFFF        |
| SA17   | 0010001 | 088000–08FFFF        | SA38   | 0100110 | 130000–137FFF        |
| SA18   | 0010010 | 090000–097FFF        | SA39   | 0100111 | 138000–13FFFF        |
| SA19   | 0010011 | 098000–09FFFF        | SA40   | 0101000 | 140000–147FFF        |
| SA20   | 0010100 | 0A0000–0A7FFF        | SA41   | 0101001 | 148000–14FFFF        |

Table 7.11 S29GL064A (Models R6, R7) Sector Addresses (Sheet 2 of 2)

| Sector | A21–A15 | 16-bit Address Range | Sector | A21–A15 | 16-bit Address Range |
|--------|---------|----------------------|--------|---------|----------------------|
| SA42   | 0101010 | 150000–157FFF        | SA85   | 1010101 | 2A8000–2AFFFF        |
| SA43   | 0101011 | 158000–15FFFF        | SA86   | 1010110 | 2B0000–2B7FFF        |
| SA44   | 0101100 | 160000–167FFF        | SA87   | 1010111 | 2B8000–2BFFFF        |
| SA45   | 0101101 | 168000–16FFFF        | SA88   | 1011000 | 2C0000–2C7FFF        |
| SA46   | 0101110 | 170000–177FFF        | SA89   | 1011001 | 2C8000–2CFFFF        |
| SA47   | 0101111 | 178000–17FFFF        | SA90   | 1011010 | 2D0000–2D7FFF        |
| SA48   | 0110000 | 180000–187FFF        | SA91   | 1011011 | 2D8000–2DFFFF        |
| SA49   | 0110001 | 188000–18FFFF        | SA92   | 1011100 | 2E0000–2E7FFF        |
| SA50   | 0110010 | 190000–197FFF        | SA93   | 1011101 | 2E8000–2EFFFF        |
| SA51   | 0110011 | 198000–19FFFF        | SA94   | 1011110 | 2F0000–2F7FFF        |
| SA52   | 0110100 | 1A0000–1A7FFF        | SA95   | 1011111 | 2F8000–2FFFFF        |
| SA53   | 0110101 | 1A8000–1AFFFF        | SA96   | 1100000 | 300000–307FFF        |
| SA54   | 0110110 | 1B0000–1B7FFF        | SA97   | 1100001 | 308000–30FFFF        |
| SA55   | 0110111 | 1B8000–1BFFFF        | SA98   | 1100010 | 310000–317FFF        |
| SA56   | 0111000 | 1C0000–1C7FFF        | SA99   | 1100011 | 318000–31FFFF        |
| SA57   | 0111001 | 1C8000–1CFFFF        | SA100  | 1100100 | 320000–327FFF        |
| SA58   | 0111010 | 1D0000–1D7FFF        | SA101  | 1100101 | 328000–32FFFF        |
| SA59   | 0111011 | 1D8000–1DFFFF        | SA102  | 1100110 | 330000–337FFF        |
| SA60   | 0111100 | 1E0000–1E7FFF        | SA103  | 1100111 | 338000–33FFFF        |
| SA61   | 0111101 | 1E8000–1EFFFF        | SA104  | 1101000 | 340000–347FFF        |
| SA62   | 0111110 | 1F0000–1F7FFF        | SA105  | 1101001 | 348000–34FFFF        |
| SA63   | 0111111 | 1F8000–1FFFFF        | SA106  | 1101010 | 350000–357FFF        |
| SA64   | 1000000 | 200000–207FFF        | SA107  | 1101011 | 358000–35FFFF        |
| SA65   | 1000001 | 208000–20FFFF        | SA108  | 1101100 | 360000–367FFF        |
| SA66   | 1000010 | 210000–217FFF        | SA109  | 1101101 | 368000–36FFFF        |
| SA67   | 1000011 | 218000–21FFFF        | SA110  | 1101110 | 370000–377FFF        |
| SA68   | 1000100 | 220000–227FFF        | SA111  | 1101111 | 378000–37FFFF        |
| SA69   | 1000101 | 228000–22FFFF        | SA112  | 1110000 | 380000–387FFF        |
| SA70   | 1000110 | 230000–237FFF        | SA113  | 1110001 | 388000–38FFFF        |
| SA71   | 1000111 | 238000–23FFFF        | SA114  | 1110010 | 390000–397FFF        |
| SA72   | 1001000 | 240000–247FFF        | SA115  | 1110011 | 398000–39FFFF        |
| SA73   | 1001001 | 248000–24FFFF        | SA116  | 1110100 | 3A0000–3A7FFF        |
| SA74   | 1001010 | 250000–257FFF        | SA117  | 1110101 | 3A8000–3AFFFF        |
| SA75   | 1001011 | 258000–25FFFF        | SA118  | 1110110 | 3B0000–3B7FFF        |
| SA76   | 1001100 | 260000–267FFF        | SA119  | 1110111 | 3B8000–3BFFFF        |
| SA77   | 1001101 | 268000–26FFFF        | SA120  | 1111000 | 3C0000–3C7FFF        |
| SA78   | 1001110 | 270000–277FFF        | SA121  | 1111001 | 3C8000–3CFFFF        |
| SA79   | 1001111 | 278000–27FFFF        | SA122  | 1111010 | 3D0000–3D7FFF        |
| SA80   | 1010000 | 280000–287FFF        | SA123  | 1111011 | 3D8000–3DFFFF        |
| SA81   | 1010001 | 288000–28FFFF        | SA124  | 1111100 | 3E0000–3E7FFF        |
| SA82   | 1010010 | 290000–297FFF        | SA125  | 1111101 | 3E8000–3EFFFF        |
| SA83   | 1010011 | 298000–29FFFF        | SA126  | 1111110 | 3F0000–3F7FFF        |
| SA84   | 1010100 | 2A0000–2A7FFF        | SA127  | 1111111 | 3F8000–3FFFFF        |

## 7.8 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector group protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires  $V_{ID}$  on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in [Table 7.12](#). In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see [Table 7.4 on page 27](#) to [Table 7.22 on page 45](#)). [Table 7.12](#) shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#). This method does not require  $V_{ID}$ . Refer to [Autoselect Command Sequence on page 53](#) for more information.

**Table 7.12** Autoselect Codes, (High Voltage Method)

| Description   | CE# | OE# | WE# | A22 to A15 | A14 to A10 | A9       | A8 to A7 | A6 | A5 to A4 | A3 to A2 | A1 | A0 | DQ8 to DQ15      |                  | DQ7 to DQ0  |   |            |
|---|-----|-----|-----|------------|------------|----------|----------|----|----------|----------|----|----|------------------|------------------|---|---|------------|
|   |     |     |     |            |            |          |          |    |          |          |    |    | BYTE# = $V_{IH}$ | BYTE# = $V_{IL}$ | Model Number  |   |            |
|   |     |     |     |            |            |          |          |    |          |          |    |    |                  |                  | X1, X2, R8, R9  | X3, X4  | R5, R6, R7 |
| Manufacturer ID: Spansion Products  | L   | L   | H   | X          | X          | $V_{ID}$ | X        | L  | X        | L        | L  | L  | 00               | X                | 01h   | 01h   | 01h        |
| S29GL064A   | L   | L   | H   | X          | X          | $V_{ID}$ | X        | L  | X        | L        | L  | H  | 22               | X                | 7Eh   | 7Eh   | 7Eh        |
|   |     |     |     |            |            |          |          |    |          | H        | H  | L  | 22               | X                | 0Ch   | 10h   | 13h        |
|   |     |     |     |            |            |          |          |    |          | H        | H  | H  | 22               | X                | 01h   | 00h (-R4, bottom boot)<br>01h (-R3, top boot) | 01h        |
| S29GL032A   | L   | L   | H   | X          | X          | $V_{ID}$ | X        | L  | X        | L        | L  | H  | 22               | X                | 7Eh   | 7Eh   |            |
|   |     |     |     |            |            |          |          |    |          | H        | H  | L  | 22               | X                | 1Dh   | 1Ah   |            |
|   |     |     |     |            |            |          |          |    |          | H        | H  | H  | 22               | X                | 00h (-R4/W4, bottom boot)<br>01h (-R3/W3, top boot)   |   |            |
| S29GL016A   | L   | L   | H   | X          | X          | $V_{ID}$ | X        | X  | X        | X        | L  | H  | 22               | X                | 49h (-R2/02/W2, bottom boot)<br>C4h (-R1/01/W1, top boot)   |   |            |
| Sector Group Protection Verification  | L   | L   | H   | SA         | X          | $V_{ID}$ | X        | L  | X        | L        | H  | L  | X                | X                | 01h (protected),<br>00h (unprotected)   |   |            |
| Secured Silicon Sector Indicator Bit (DQ7), WP# protects highest address sector | L   | L   | H   | X          | X          | $V_{ID}$ | X        | L  | X        | L        | H  | H  | X                | X                | For S29GL064A and S29GL032A:<br>99h (factory locked),<br>19h (not factory locked)<br>For S29GL016A: 94h (factory locked),<br>14h (not factory locked) |   |            |
| Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest address sector  | L   | L   | H   | X          | X          | $V_{ID}$ | X        | L  | X        | L        | H  | H  | X                | X                | For S29GL064A and S29GL032A:<br>89h (factory locked),<br>09h (not factory locked)<br>For S29GL016A: 84h (factory locked),<br>04h (not factory locked) |   |            |

**Legend**

L = Logic Low =  $V_{IL}$   
H = Logic High =  $V_{IH}$   
SA = Sector Address  
X = Don't care.



## 7.9 Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group (see [Table 7.11 on page 38](#) to [Table 7.22 on page 45](#)). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector protection/unprotection requires  $V_{ID}$  on the RESET# pin only, and can be implemented either in-system or via programming equipment. [Figure 7.2 on page 46](#) shows the algorithms and [Figure 16.13 on page 86](#) shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

The device is shipped with all sector groups unprotected. Spansion offers the option of programming and protecting sector groups at its factory prior to shipping the device through Spansion Programming Service. Contact a Spansion representative for details.

It is possible to determine whether a sector group is protected or unprotected. See [Autoselect Mode on page 40](#) for details.

**Table 7.13** S29GL016A (Model R1, 01) Sector Group Protection/Unprotection Addresses

| Sector    | A19–A12  | Sector/Sector Block Size (Kbytes) | Sector | A19–A12   | Sector/Sector Block Size (Kbytes) |
|-----------|----------|-----------------------------------|--------|-----------|-----------------------------------|
| SA0-SA3   | 000XXXXh | 256 (4x64)                        | SA31   | 11111000h | 8                                 |
| SA4-SA7   | 001XXXXh | 256 (4x64)                        | SA32   | 11111001h | 8                                 |
| SA8-SA11  | 010XXXXh | 256 (4x64)                        | SA33   | 11111010h | 8                                 |
| SA12-SA15 | 011XXXXh | 256 (4x64)                        | SA34   | 11111011h | 8                                 |
| SA16-SA19 | 100XXXXh | 256 (4x64)                        | SA35   | 11111100h | 8                                 |
| SA20-SA23 | 101XXXXh | 256 (4x64)                        | SA36   | 11111101h | 8                                 |
| SA24-SA27 | 110XXXXh | 256 (4x64)                        | SA37   | 11111110h | 8                                 |
| SA28-SA30 | 11100XXh | 192 (3x64)                        | SA38   | 11111111h | 8                                 |
|           | 11101XXh |                                   |        |           |                                   |
|           | 11110XXh |                                   |        |           |                                   |

**Table 7.14** S29GL016A (Model R2, 02) Sector Group Protection/Unprotection Addresses

| Sector | A19–A12   | Sector/Sector Block Size (Kbytes) | Sector    | A19–A12  | Sector/Sector Block Size (Kbytes) |
|--------|-----------|-----------------------------------|-----------|----------|-----------------------------------|
| SA0    | 00000000h | 8                                 | SA8–SA10  | 00001XXh | 192 (3x64)                        |
| SA1    | 00000001h | 8                                 |           | 00010XXh |                                   |
| SA2    | 00000010h | 8                                 |           | 00011XXh |                                   |
| SA3    | 00000011h | 8                                 | SA11–SA14 | 001XXXXh | 256 (4x64)                        |
| SA4    | 00000100h | 8                                 | SA15–SA18 | 010XXXXh | 256 (4x64)                        |
| SA5    | 00000101h | 8                                 | SA19–SA22 | 011XXXXh | 256 (4x64)                        |
| SA6    | 00000110h | 8                                 | SA23–SA26 | 100XXXXh | 256 (4x64)                        |
| SA7    | 00000111h | 8                                 | SA27–SA30 | 101XXXXh | 256 (4x64)                        |
|        |           |                                   | SA31–SA34 | 110XXXXh | 256 (4x64)                        |
|        |           |                                   | SA35–SA38 | 111XXXXh | 256 (4x64)                        |

**Table 7.15** S29GL032A (Models R1, R2) Sector Group Protection/Unprotection Addresses

| Sector    | A20–A15 | Sector /Sector Block Size (Kbytes) | Sector    | A20–A15 | Sector /Sector Block Size (Kbytes) | Sector    | A20–A15 | Sector /Sector Block Size (Kbytes) |
|-----------|---------|------------------------------------|-----------|---------|------------------------------------|-----------|---------|------------------------------------|
| SA0       | 000000  | 64                                 | SA20–SA23 | 0101xx  | 256 (4x64)                         | SA48–SA51 | 1100xx  | 256 (4x64)                         |
| SA1       | 000001  | 64                                 | SA24–SA27 | 0110xx  | 256 (4x64)                         | SA52–SA55 | 1101xx  | 256 (4x64)                         |
| SA2       | 000010  | 64                                 | SA28–SA31 | 0111xx  | 256 (4x64)                         | SA56–SA59 | 1110xx  | 256 (4x64)                         |
| SA3       | 000011  | 64                                 | SA32–SA35 | 1000xx  | 256 (4x64)                         | SA60      | 111100  | 64                                 |
| SA4–SA7   | 0001xx  | 256 (4x64)                         | SA36–SA39 | 1001xx  | 256 (4x64)                         | SA61      | 111101  | 64                                 |
| SA8–SA11  | 0010xx  | 256 (4x64)                         | SA40–SA43 | 1010xx  | 256 (4x64)                         | SA62      | 111110  | 64                                 |
| SA12–SA15 | 0011xx  | 256 (4x64)                         | SA44–SA47 | 1011xx  | 256 (4x64)                         | SA63      | 111111  | 64                                 |
| SA16–SA19 | 0100xx  | 256 (4x64)                         |           |         |                                    |           |         |                                    |

**Table 7.16** S29GL032A (Model R3, W3) Sector Group Protection/Unprotection Address Table

| Sector    | A20–A12    | Sector/Sector Block Size (Kbytes) | Sector    | A20–A12    | Sector/Sector Block Size (Kbytes) |
|-----------|------------|-----------------------------------|-----------|------------|-----------------------------------|
| SA0-SA3   | 0000XXXXXh | 256 (4x64)                        | SA52-SA55 | 1101XXXXXh | 256 (4x64)                        |
| SA4-SA7   | 0001XXXXXh | 256 (4x64)                        | SA56-SA59 | 1110XXXXXh | 256 (4x64)                        |
| SA8-SA11  | 0010XXXXXh | 256 (4x64)                        | SA60-SA62 | 111100XXXh | 192 (3x64)                        |
| SA12-SA15 | 0011XXXXXh | 256 (4x64)                        |           | 111101XXXh |                                   |
| SA16-SA19 | 0100XXXXXh | 256 (4x64)                        |           | 111110XXXh |                                   |
| SA20-SA23 | 0101XXXXXh | 256 (4x64)                        | SA63      | 111111000h | 8                                 |
| SA24-SA27 | 0110XXXXXh | 256 (4x64)                        | SA64      | 111111001h | 8                                 |
| SA28-SA31 | 0111XXXXXh | 256 (4x64)                        | SA65      | 111111010h | 8                                 |
| SA32–SA35 | 1000XXXXXh | 256 (4x64)                        | SA66      | 111111011h | 8                                 |
| SA36–SA39 | 1001XXXXXh | 256 (4x64)                        | SA67      | 111111100h | 8                                 |
| SA40–SA43 | 1010XXXXXh | 256 (4x64)                        | SA68      | 111111101h | 8                                 |
| SA44–SA47 | 1011XXXXXh | 256 (4x64)                        | SA69      | 111111110h | 8                                 |
| SA48–SA51 | 1100XXXXXh | 256 (4x64)                        | SA70      | 111111111h | 8                                 |

**Table 7.17** S29GL032A (Model R4, W4) Sector Group Protection/Unprotection Address Table

| Sector    | A20–A12    | Sector/Sector Block Size (Kbytes) | Sector    | A20–A12    | Sector/Sector Block Size (Kbytes) |
|-----------|------------|-----------------------------------|-----------|------------|-----------------------------------|
| SA0       | 000000000h | 8                                 | SA19–SA22 | 0011XXXXXh | 256 (4x64)                        |
| SA1       | 000000001h | 8                                 | SA23–SA26 | 0100XXXXXh | 256 (4x64)                        |
| SA2       | 000000010h | 8                                 | SA27–SA30 | 0101XXXXXh | 256 (4x64)                        |
| SA3       | 000000011h | 8                                 | SA31–SA34 | 0110XXXXXh | 256 (4x64)                        |
| SA4       | 000000100h | 8                                 | SA35–SA38 | 0111XXXXXh | 256 (4x64)                        |
| SA5       | 000000101h | 8                                 | SA39–SA42 | 1000XXXXXh | 256 (4x64)                        |
| SA6       | 000000110h | 8                                 | SA43–SA46 | 1001XXXXXh | 256 (4x64)                        |
| SA7       | 000000111h | 8                                 | SA47–SA50 | 1010XXXXXh | 256 (4x64)                        |
| SA8–SA10  | 000001XXXh | 192 (3x64)                        | SA51–SA54 | 1011XXXXXh | 256 (4x64)                        |
|           | 000010XXXh |                                   | SA55–SA58 | 1100XXXXXh | 256 (4x64)                        |
|           | 000011XXXh |                                   | SA59–SA62 | 1101XXXXXh | 256 (4x64)                        |
| SA11–SA14 | 0001XXXXXh | 256 (4x64)                        | SA63–SA66 | 1110XXXXXh | 256 (4x64)                        |
| SA15–SA18 | 0010XXXXXh | 256 (4x64)                        | SA67–SA70 | 1111XXXXXh | 256 (4x64)                        |

**Table 7.18** S29GL064A (Models R1, R2, R8, R9) Sector Group Protection/Unprotection Addresses

| Sector    | A21–A15 | Sector/<br>Sector<br>Block Size<br>(Kbytes) | Sector    | A21–A15 | Sector/<br>Sector<br>Block Size<br>(Kbytes) | Sector      | A21–A15 | Sector/<br>Sector<br>Block Size<br>(Kbytes) |
|-----------|---------|---|-----------|---------|---|-------------|---------|---|
| SA0       | 0000000 | 64  | SA40–SA43 | 01010xx | 256 (4x64)                                  | SA92–SA95   | 10111xx | 256 (4x64)                                  |
| SA1       | 0000001 | 64  | SA44–SA47 | 01011xx | 256 (4x64)                                  | SA96–SA99   | 11000xx | 256 (4x64)                                  |
| SA2       | 0000010 | 64  | SA48–SA51 | 01100xx | 256 (4x64)                                  | SA100–SA103 | 11001xx | 256 (4x64)                                  |
| SA3       | 0000011 | 64  | SA52–SA55 | 01101xx | 256 (4x64)                                  | SA104–SA107 | 11010xx | 256 (4x64)                                  |
| SA4–SA7   | 00001xx | 256 (4x64)                                  | SA56–SA59 | 01110xx | 256 (4x64)                                  | SA108–SA111 | 11011xx | 256 (4x64)                                  |
| SA8–SA11  | 00010xx | 256 (4x64)                                  | SA60–SA63 | 01111xx | 256 (4x64)                                  | SA112–SA115 | 11100xx | 256 (4x64)                                  |
| SA12–SA15 | 00011xx | 256 (4x64)                                  | SA64–SA67 | 10000xx | 256 (4x64)                                  | SA116–SA119 | 11101xx | 256 (4x64)                                  |
| SA16–SA19 | 00100xx | 256 (4x64)                                  | SA68–SA71 | 10001xx | 256 (4x64)                                  | SA120–SA123 | 11110xx | 256 (4x64)                                  |
| SA20–SA23 | 00101xx | 256 (4x64)                                  | SA72–SA75 | 10010xx | 256 (4x64)                                  | SA124       | 1111100 | 64  |
| SA24–SA27 | 00110xx | 256 (4x64)                                  | SA76–SA79 | 10011xx | 256 (4x64)                                  | SA125       | 1111101 | 64  |
| SA28–SA31 | 00111xx | 256 (4x64)                                  | SA80–SA83 | 10100xx | 256 (4x64)                                  | SA126       | 1111110 | 64  |
| SA32–SA35 | 01000xx | 256 (4x64)                                  | SA84–SA87 | 10101xx | 256 (4x64)                                  | SA127       | 1111111 | 64  |
| SA36–SA39 | 01001xx | 256 (4x64)                                  | SA88–SA91 | 10110xx | 256 (4x64)                                  |             |         |   |

**Table 7.19** S29GL064A (Model R3) Top Boot Sector Protection/Unprotection Addresses

| Sector    | A21–A12    | Sector/Sector<br>Block Size<br>(Kbytes) | Sector      | A20–A12                                | Sector/Sector<br>Block Size<br>(Kbytes) |
|-----------|------------|---|-------------|--|---|
| SA0-SA3   | 00000XXXXX | 256 (4x64)                              | SA80-SA83   | 10100XXXXX                             | 256 (4x64)                              |
| SA4-SA7   | 00001XXXXX | 256 (4x64)                              | SA84-SA87   | 10101XXXXX                             | 256 (4x64)                              |
| SA8-SA11  | 00010XXXXX | 256 (4x64)                              | SA88-SA91   | 10110XXXXX                             | 256 (4x64)                              |
| SA12-SA15 | 00011XXXXX | 256 (4x64)                              | SA92-SA95   | 10111XXXXX                             | 256 (4x64)                              |
| SA16-SA19 | 00100XXXXX | 256 (4x64)                              | SA96-SA99   | 11000XXXXX                             | 256 (4x64)                              |
| SA20-SA23 | 00101XXXXX | 256 (4x64)                              | SA100-SA103 | 11001XXXXX                             | 256 (4x64)                              |
| SA24-SA27 | 00110XXXXX | 256 (4x64)                              | SA104-SA107 | 11010XXXXX                             | 256 (4x64)                              |
| SA28-SA31 | 00111XXXXX | 256 (4x64)                              | SA108-SA111 | 11011XXXXX                             | 256 (4x64)                              |
| SA32-SA35 | 01000XXXXX | 256 (4x64)                              | SA112-SA115 | 11100XXXXX                             | 256 (4x64)                              |
| SA36-SA39 | 01001XXXXX | 256 (4x64)                              | SA116-SA119 | 11101XXXXX                             | 256 (4x64)                              |
| SA40-SA43 | 01010XXXXX | 256 (4x64)                              | SA120-SA123 | 11110XXXXX                             | 256 (4x64)                              |
| SA44-SA47 | 01011XXXXX | 256 (4x64)                              | SA124-SA126 | 1111100XXX<br>1111101XXX<br>1111110XXX | 192 (3x64)                              |
| SA48-SA51 | 01100XXXXX | 256 (4x64)                              | SA127       | 111111000                              | 8                                       |
| SA52-SA55 | 01101XXXXX | 256 (4x64)                              | SA128       | 1111111001                             | 8                                       |
| SA56-SA59 | 01110XXXXX | 256 (4x64)                              | SA129       | 1111111010                             | 8                                       |
| SA60-SA63 | 01111XXXXX | 256 (4x64)                              | SA130       | 1111111011                             | 8                                       |
| SA64-SA67 | 10000XXXXX | 256 (4x64)                              | SA131       | 1111111100                             | 8                                       |
| SA68-SA71 | 10001XXXXX | 256 (4x64)                              | SA132       | 1111111101                             | 8                                       |
| SA72-SA75 | 10010XXXXX | 256 (4x64)                              | SA133       | 1111111110                             | 8                                       |
| SA76-SA79 | 10011XXXXX | 256 (4x64)                              | SA134       | 1111111111                             | 8                                       |

**Table 7.20** S29GL064A (Model R4) Bottom Boot Sector Protection/Unprotection Addresses

| Sector    | A21-A12                                   | Sector/Sector Block Size (Kbytes) | Sector      | A20-A12    | Sector/Sector Block Size (Kbytes) |
|-----------|---|-----------------------------------|-------------|------------|-----------------------------------|
| SA0       | 0000000000                                | 8                                 | SA55-SA58   | 01100XXXXX | 256 (4x64)                        |
| SA1       | 0000000001                                | 8                                 | SA59-SA62   | 01101XXXXX | 256 (4x64)                        |
| SA2       | 0000000010                                | 8                                 | SA63-SA66   | 01110XXXXX | 256 (4x64)                        |
| SA3       | 0000000011                                | 8                                 | SA67-SA70   | 01111XXXXX | 256 (4x64)                        |
| SA4       | 0000000100                                | 8                                 | SA71-SA74   | 10000XXXXX | 256 (4x64)                        |
| SA5       | 0000000101                                | 8                                 | SA75-SA78   | 10001XXXXX | 256 (4x64)                        |
| SA6       | 0000000110                                | 8                                 | SA79-SA82   | 10010XXXXX | 256 (4x64)                        |
| SA7       | 0000000111                                | 8                                 | SA83-SA86   | 10011XXXXX | 256 (4x64)                        |
| SA8-SA10  | 0000001XXX,<br>0000010XXX,<br>0000011XXX, | 192 (3x64)                        | SA87-SA90   | 10100XXXXX | 256 (4x64)                        |
| SA11-SA14 | 00001XXXXX                                | 256 (4x64)                        | SA91-SA94   | 10101XXXXX | 256 (4x64)                        |
| SA15-SA18 | 00010XXXXX                                | 256 (4x64)                        | SA95-SA98   | 10110XXXXX | 256 (4x64)                        |
| SA19-SA22 | 00011XXXXX                                | 256 (4x64)                        | SA99-SA102  | 10111XXXXX | 256 (4x64)                        |
| SA23-SA26 | 00100XXXXX                                | 256 (4x64)                        | SA103-SA106 | 11000XXXXX | 256 (4x64)                        |
| SA27-SA30 | 00101XXXXX                                | 256 (4x64)                        | SA107-SA110 | 11001XXXXX | 256 (4x64)                        |
| SA31-SA34 | 00110XXXXX                                | 256 (4x64)                        | SA111-SA114 | 11010XXXXX | 256 (4x64)                        |
| SA35-SA38 | 00111XXXXX                                | 256 (4x64)                        | SA115-SA118 | 11011XXXXX | 256 (4x64)                        |
| SA39-SA42 | 01000XXXXX                                | 256 (4x64)                        | SA119-SA122 | 11100XXXXX | 256 (4x64)                        |
| SA43-SA46 | 01001XXXXX                                | 256 (4x64)                        | SA123-SA126 | 11101XXXXX | 256 (4x64)                        |
| SA47-SA50 | 01010XXXXX                                | 256 (4x64)                        | SA127-SA130 | 11110XXXXX | 256 (4x64)                        |
| SA51-SA54 | 01011XXXXX                                | 256 (4x64)                        | SA131-SA134 | 11111XXXXX | 256 (4x64)                        |

**Table 7.21** S29GL064A (Model R5) Sector Group Protection/Unprotection Addresses

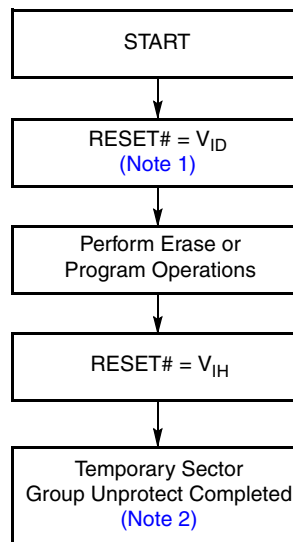
| Sector    | A21-A15 | Sector/ Sector Block Size (Kbytes) | Sector    | A21-A15 | Sector/ Sector Block Size (Kbytes) | Sector      | A21-A15 | Sector/ Sector Block Size (Kbytes) |
|-----------|---------|------------------------------------|-----------|---------|------------------------------------|-------------|---------|------------------------------------|
| SA0-SA3   | 00000   | 256 (4x64)                         | SA44-SA47 | 01011   | 256 (4x64)                         | SA88-SA91   | 10110   | 256 (4x64)                         |
| SA4-SA7   | 00001   | 256 (4x64)                         | SA48-SA51 | 01100   | 256 (4x64)                         | SA92-SA95   | 10111   | 256 (4x64)                         |
| SA8-SA11  | 00010   | 256 (4x64)                         | SA52-SA55 | 01101   | 256 (4x64)                         | SA96-SA99   | 11000   | 256 (4x64)                         |
| SA12-SA15 | 00011   | 256 (4x64)                         | SA56-SA59 | 01110   | 256 (4x64)                         | SA100-SA103 | 11001   | 256 (4x64)                         |
| SA16-SA19 | 00100   | 256 (4x64)                         | SA60-SA63 | 01111   | 256 (4x64)                         | SA104-SA107 | 11010   | 256 (4x64)                         |
| SA20-SA23 | 00101   | 256 (4x64)                         | SA64-SA67 | 10000   | 256 (4x64)                         | SA108-SA111 | 11011   | 256 (4x64)                         |
| SA24-SA27 | 00110   | 256 (4x64)                         | SA68-SA71 | 10001   | 256 (4x64)                         | SA112-SA115 | 11100   | 256 (4x64)                         |
| SA28-SA31 | 00111   | 256 (4x64)                         | SA72-SA75 | 10010   | 256 (4x64)                         | SA116-SA119 | 11101   | 256 (4x64)                         |
| SA32-SA35 | 01000   | 256 (4x64)                         | SA76-SA79 | 10011   | 256 (4x64)                         | SA120-SA123 | 11110   | 256 (4x64)                         |
| SA36-SA39 | 01001   | 256 (4x64)                         | SA80-SA83 | 10100   | 256 (4x64)                         | SA124-SA127 | 11111   | 256 (4x64)                         |
| SA40-SA43 | 01010   | 256 (4x64)                         | SA84-SA87 | 10101   | 256 (4x64)                         |             |         |                                    |

**Table 7.22** S29GL064A (Models R6, R7) Sector Group Protection/Unprotection Addresses

| Sector    | A21–A15 | Sector/<br>Sector<br>Block Size<br>(Kbytes) | Sector    | A21–A15 | Sector/<br>Sector<br>Block Size<br>(Kbytes) | Sector      | A21–A15 | Sector/<br>Sector<br>Block Size<br>(Kbytes) |
|-----------|---------|---|-----------|---------|---|-------------|---------|---|
| SA0–SA3   | 00000   | 256 (4x64)                                  | SA44–SA47 | 01011   | 256 (4x64)                                  | SA88–SA91   | 10110   | 256 (4x64)                                  |
| SA4–SA7   | 00001   | 256 (4x64)                                  | SA48–SA51 | 01100   | 256 (4x64)                                  | SA92–SA95   | 10111   | 256 (4x64)                                  |
| SA8–SA11  | 00010   | 256 (4x64)                                  | SA52–SA55 | 01101   | 256 (4x64)                                  | SA96–SA99   | 11000   | 256 (4x64)                                  |
| SA12–SA15 | 00011   | 256 (4x64)                                  | SA56–SA59 | 01110   | 256 (4x64)                                  | SA100–SA103 | 11001   | 256 (4x64)                                  |
| SA16–SA19 | 00100   | 256 (4x64)                                  | SA60–SA63 | 01111   | 256 (4x64)                                  | SA104–SA107 | 11010   | 256 (4x64)                                  |
| SA20–SA23 | 00101   | 256 (4x64)                                  | SA64–SA67 | 10000   | 256 (4x64)                                  | SA108–SA111 | 11011   | 256 (4x64)                                  |
| SA24–SA27 | 00110   | 256 (4x64)                                  | SA68–SA71 | 10001   | 256 (4x64)                                  | SA112–SA115 | 11100   | 256 (4x64)                                  |
| SA28–SA31 | 00111   | 256 (4x64)                                  | SA72–SA75 | 10010   | 256 (4x64)                                  | SA116–SA119 | 11101   | 256 (4x64)                                  |
| SA32–SA35 | 01000   | 256 (4x64)                                  | SA76–SA79 | 10011   | 256 (4x64)                                  | SA120–SA123 | 11110   | 256 (4x64)                                  |
| SA36–SA39 | 01001   | 256 (4x64)                                  | SA80–SA83 | 10100   | 256 (4x64)                                  | SA124–SA127 | 11111   | 256 (4x64)                                  |
| SA40–SA43 | 01010   | 256 (4x64)                                  | SA84–SA87 | 10101   | 256 (4x64)                                  |             |         |   |

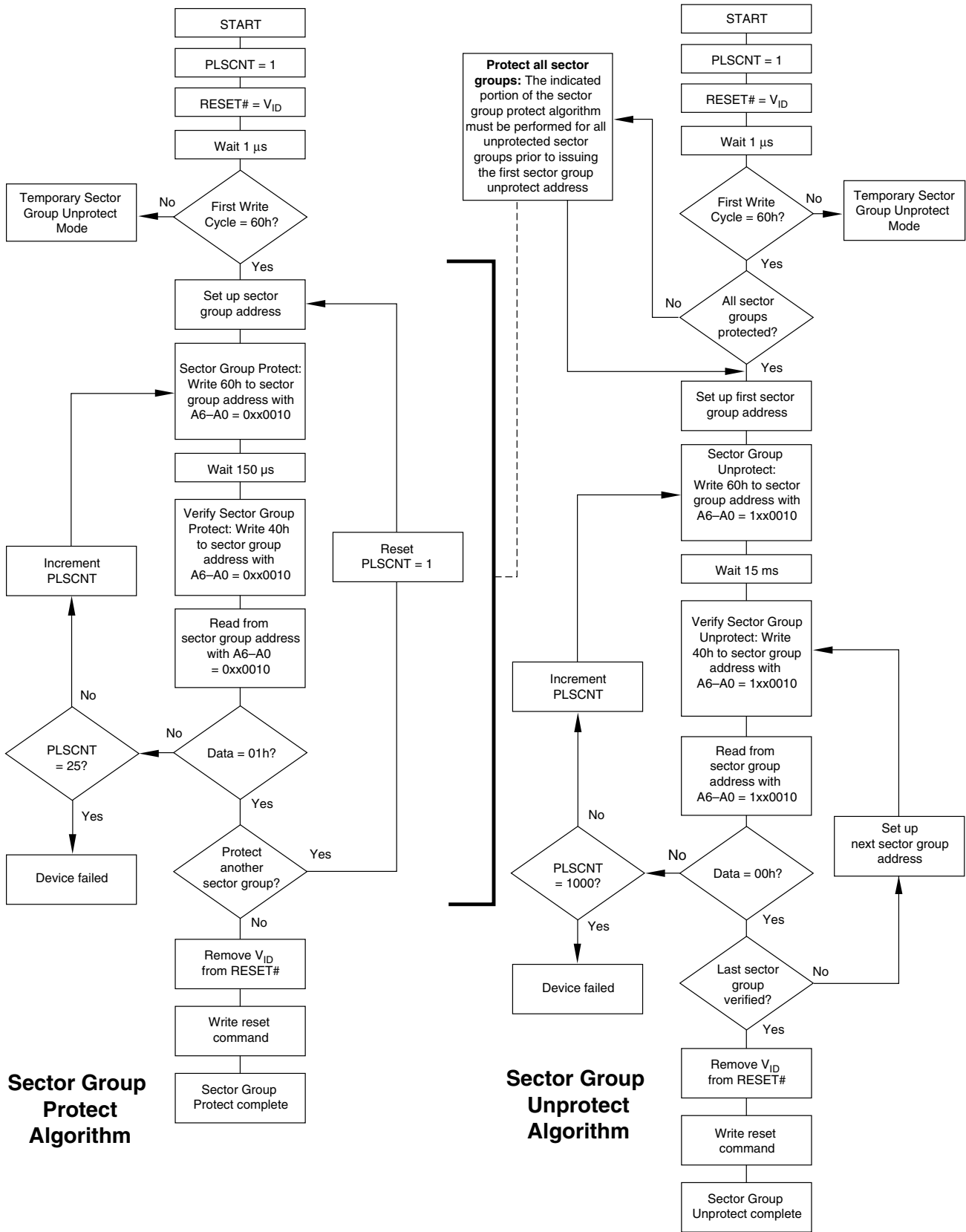
## 7.10 Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to  $V_{ID}$ . During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once  $V_{ID}$  is removed from the RESET# pin, all the previously protected sector groups are protected again. [Figure 7.1](#) shows the algorithm, and [Figure 16.11 on page 82](#) shows the timing diagrams, for this feature.

**Figure 7.1** Temporary Sector Group Unprotect Operation**Notes**

1. All protected sector groups unprotected (If  $WP# = V_{IL}$ , the highest or lowest address sector remains protected for uniform sector devices; the top or bottom two address sectors remains protected for boot sector devices).
2. All previously protected sector groups are protected once again.

Figure 7.2 In-System Sector Group Protect/Unprotect Algorithms



## 7.11 Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 bytes in length, and uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the Secured Silicon Sector either customer lockable (standard shipping option) or factory locked (contact a Spansion sales representative for ordering information). The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also contains the Secured Silicon Sector Indicator Bit permanently set to a 0. The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a 1. Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

The Secured Silicon sector address space in this device is allocated as follows:

| Secured Silicon Sector Address Range |                 | Standard Factory Locked | ExpressFlash Factory Locked   | Customer Lockable      |
|--------------------------------------|-----------------|-------------------------|-------------------------------|------------------------|
| x16                                  | x8              |                         |                               |                        |
| 000000h-000007h                      | 000000h-00000Fh | ESN                     | ESN or determined by customer | Determined by customer |
| 000008h-00007Fh                      | 000010h-0000FFh | Unavailable             | Determined by customer        |                        |

The system accesses the Secured Silicon Sector through a command sequence (see [Write Protect \(WP#\) on page 48](#)). After the system writes the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

### 7.11.1 Customer Lockable: Secured Silicon Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte Secured Silicon sector.

The system may program the Secured Silicon Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See [Command Definitions on page 52](#).

Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in [Figure 7.2 on page 46](#), except that *RESET# may be at either  $V_{IH}$  or  $V_{ID}$* . This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then use the alternate method of sector protection described in [Sector Group Protection and Unprotection on page 41](#).

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing within the remainder of the array.

### 7.11.2 Factory Locked: Secured Silicon Sector Programmed and Protected At the Factory

In devices with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the factory through the Spansion programming service (Customer Factory Locked). The devices are then shipped from the factory with the Secured Silicon Sector permanently locked. Contact your sales representative for details on using the Spansion programming service.

## 7.12 Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the first or last sector group without using  $V_{ID}$ . Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts  $V_{IL}$  on the WP#/ACC pin, the device disables program and erase functions in the first or last sector group independently of whether those sector groups were protected or unprotected. Note that if WP#/ACC is at  $V_{IL}$  when the device is in the standby mode, the maximum input load current is increased. See the table in [DC Characteristics on page 70](#).

**If the system asserts  $V_{IH}$  on the WP#/ACC pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in [Sector Group Protection and Unprotection on page 41](#). Note that WP# contains an internal pull-up; when unconnected, WP# is at  $V_{IH}$ .**

## 7.13 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during  $V_{CC}$  power-up and power-down transitions, or from system noise.

### 7.13.1 Low $V_{CC}$ Write Inhibit

When  $V_{CC}$  is less than  $V_{LKO}$ , the device does not accept any write cycles. This protects data during  $V_{CC}$  power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until  $V_{CC}$  is greater than  $V_{LKO}$ . The system must provide the proper signals to the control pins to prevent unintentional writes when  $V_{CC}$  is greater than  $V_{LKO}$ .

### 7.13.2 Write Pulse *Glitch* Protection

Noise pulses of less than 3 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

### 7.13.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# =  $V_{IL}$ , CE# =  $V_{IH}$  or WE# =  $V_{IH}$ . To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

### 7.13.4 Power-Up Write Inhibit

If WE# = CE# =  $V_{IL}$  and OE# =  $V_{IH}$  during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.



## 8. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in [Table 8.1 to Table 8.4 on page 51](#). To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in [Table 8.1 to Table 8.4 on page 51](#). The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Alternatively, contact your sales representative for copies of these documents.

**Table 8.1** CFI Query Identification String

| Addresses (x16)   | Addresses (x8)    | Data                    | Description  |
|-------------------|-------------------|-------------------------|--|
| 10h<br>11h<br>12h | 20h<br>22h<br>24h | 0051h<br>0052h<br>0059h | Query Unique ASCII string "QRY"                              |
| 13h<br>14h        | 26h<br>28h        | 0002h<br>0000h          | Primary OEM Command Set                                      |
| 15h<br>16h        | 2Ah<br>2Ch        | 0040h<br>0000h          | Address for Primary Extended Table                           |
| 17h<br>18h        | 2Eh<br>30h        | 0000h<br>0000h          | Alternate OEM Command Set (00h = none exists)                |
| 19h<br>1Ah        | 32h<br>34h        | 0000h<br>0000h          | Address for Alternate OEM Extended Table (00h = none exists) |

**Table 8.2** System Interface String

| Addresses (x16) | Addresses (x8) | Data  | Description   |
|-----------------|----------------|-------|---|
| 1Bh             | 36h            | 0027h | V <sub>CC</sub> Min. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt             |
| 1Ch             | 38h            | 0036h | V <sub>CC</sub> Max. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt             |
| 1Dh             | 3Ah            | 0000h | V <sub>PP</sub> Min. voltage (00h = no V <sub>PP</sub> pin present)                 |
| 1Eh             | 3Ch            | 0000h | V <sub>PP</sub> Max. voltage (00h = no V <sub>PP</sub> pin present)                 |
| 1Fh             | 3Eh            | 0007h | Reserved for future use   |
| 20h             | 40h            | 0007h | Typical timeout for Min. size buffer write 2 <sup>N</sup> μs (00h = not supported)  |
| 21h             | 42h            | 000Ah | Typical timeout per individual block erase 2 <sup>N</sup> ms                        |
| 22h             | 44h            | 0000h | Typical timeout for full chip erase 2 <sup>N</sup> ms (00h = not supported)         |
| 23h             | 46h            | 0001h | Reserved for future use   |
| 24h             | 48h            | 0005h | Max. timeout for buffer write 2 <sup>N</sup> times typical                          |
| 25h             | 4Ah            | 0004h | Max. timeout per individual block erase 2 <sup>N</sup> times typical                |
| 26h             | 4Ch            | 0000h | Max. timeout for full chip erase 2 <sup>N</sup> times typical (00h = not supported) |

**Note**

CFI data related to V<sub>CC</sub> and time-outs may differ from actual V<sub>CC</sub> and time-outs of the product. Please consult the Ordering Information tables to obtain the V<sub>CC</sub> range for particular part numbers. Please consult the Erase and Programming Performance table for typical timeout specifications.

**Table 8.3** Device Geometry Definition

| Addresses (x16)          | Addresses (x8)           | Data                             | Description   |
|--------------------------|--------------------------|----------------------------------|---|
| 27h                      | 4Eh                      | 00xxh                            | Device Size = 2 <sup>N</sup> byte<br>0017h = 64 Mb, 0016h = 32Mb, 0015h = 16Mb  |
| 28h<br>29h               | 50h<br>52h               | 000xh<br>0000h                   | Flash Device Interface description (refer to CFI publication 100)<br>0000h = x8-only bus devices<br>0001h = x16-only bus devices<br>0002h = x8/x16 bus devices  |
| 2Ah<br>2Bh               | 54h<br>56h               | 0005h<br>0000h                   | Max. number of byte in multi-byte write = 2 <sup>N</sup><br>(00h = not supported)   |
| 2Ch                      | 58h                      | 00xxh                            | Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)   |
| 2Dh<br>2Eh<br>2Fh<br>30h | 5Ah<br>5Ch<br>5Eh<br>60h | 00xxh<br>000xh<br>00x0h<br>000xh | Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)<br>0000h, 0020h, 0000h, 0007h = 16 Mb (-R1, -R2)<br>003Fh, 0000h, 0000h, 0001h = 32 Mb (-R1, -R2)<br>0007h, 0000h, 0020h, 0000h = 32 Mb (-R3, R4)<br>007Fh, 0000h, 0000h, 0001h = 64 Mb (-R1, -R2, -R8, -R9)<br>0007h, 0000h, 0020h, 0000h = 64 Mb (-R3, -R4, -R5, -R6, -R7) |
| 31h<br>32h<br>33h<br>34h | 60h<br>64h<br>66h<br>68h | 00xxh<br>0000h<br>0000h<br>000xh | Erase Block Region 2 Information (refer to CFI publication 100)<br>0001h, 0000h, 0000h, 001Eh = 16 Mb (-R1, -R2)<br>0000h, 0000h, 0000h, 0000h = all others<br>007Eh, 0000h, 0000h, 0001h = 64 Mb (-R3, -R4)<br>003Eh, 0000h, 0000h, 0001h = 32 Mb (-R3, R4)  |
| 35h<br>36h<br>37h<br>38h | 6Ah<br>6Ch<br>6Eh<br>70h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 3 Information (refer to CFI publication 100)   |
| 39h<br>3Ah<br>3Bh<br>3Ch | 72h<br>74h<br>76h<br>78h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 4 Information (refer to CFI publication 100)   |

Table 8.4 Primary Vendor-Specific Extended Query

| Addresses (x16)   | Addresses (x8)    | Data                    | Description   |
|-------------------|-------------------|-------------------------|---|
| 40h<br>41h<br>42h | 80h<br>82h<br>84h | 0050h<br>0052h<br>0049h | Query-unique ASCII string "PRI"   |
| 43h               | 86h               | 0031h                   | Major version number, ASCII   |
| 44h               | 88h               | 0033h                   | Minor version number, ASCII   |
| 45h               | 8Ah               | 000xh                   | Address Sensitive Unlock (Bits 1-0)<br>0 = Required, 1 = Not Required<br>Process Technology (Bits 7-2) 0010b = 200 nm MirrorBit<br>0009h = x8-only bus devices<br>0008h = all other devices |
| 46h               | 8Ch               | 0002h                   | Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write   |
| 47h               | 8Eh               | 0001h                   | Sector Protect<br>0 = Not Supported, X = Number of sectors in smallest sector group   |
| 48h               | 90h               | 0001h                   | Sector Temporary Unprotect<br>00 = Not Supported, 01 = Supported  |
| 49h               | 92h               | 0004h                   | Sector Protect/Unprotect scheme<br>0004h = Standard Mode (Refer to Text)  |
| 4Ah               | 94h               | 0000h                   | Simultaneous Operation<br>00 = Not Supported, X = Number of Sectors in Bank   |
| 4Bh               | 96h               | 0000h                   | Burst Mode Type<br>00 = Not Supported, 01 = Supported   |
| 4Ch               | 98h               | 0001h                   | Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page  |
| 4Dh               | 9Ah               | 00B5h                   | ACC (Acceleration) Supply Minimum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV  |
| 4Eh               | 9Ch               | 00C5h                   | ACC (Acceleration) Supply Maximum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV  |
| 4Fh               | 9Eh               | 00xxh                   | Top/Bottom Boot Sector Flag<br>02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors<br>bottom WP# protect, 05h = Uniform sectors top WP# protect                          |
| 50h               | A0h               | 0001h                   | Program Suspend<br>00h = Not Supported, 01h = Supported   |

## 9. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) define the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to [AC Characteristics on page 72](#) for timing diagrams.

### 9.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See [Erase Suspend/Erase Resume Commands on page 60](#) for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See [Reset Command on page 52](#) for more information.

See also Requirements for Reading Array Data in [Device Bus Operations on page 22](#) for more information. The Read-Only Operations—[AC Characteristics on page 72](#) provide the read parameters, and [Figure 16.2 on page 74](#) shows the timing diagram.

### 9.2 Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

### 9.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to read several identifier codes at specific addresses:

| Identifier Code                        | A7:A0 (x16) | A6:A-1 (x8) |
|--|-------------|-------------|
| Manufacturer ID                        | 00h         | 00h         |
| Device ID, Cycle 1                     | 01h         | 02h         |
| Device ID, Cycle 2                     | 0Eh         | 1Ch         |
| Device ID, Cycle 3                     | 0Fh         | 1Eh         |
| Secured Silicon Sector Factory Protect | 03h         | 06h         |
| Sector Protect Verify                  | (SA)02h     | (SA)04h     |

**Note**

The device ID is read over three cycles. SA = Sector Address

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

### 9.4 Enter/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) show the address and data requirements for both command sequences. See also [Secured Silicon Sector Flash Memory Region on page 47](#) for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

#### 9.4.1 Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) show the address and data requirements for the word program command sequence, respectively.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to [Write Operation Status on page 63](#) for information on these status bits. Any commands written to the device during the Embedded Program Algorithm are ignored. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.* Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device returns to the read mode, to ensure data integrity.

Programming is allowed in any sequence of address locations and across sector boundaries. Programming to the same word address multiple times without intervening erases (incremental bit programming) requires a modified programming method. For such application requirements, please contact your local Spansion representative. Word programming is supported for backward compatibility with existing Flash driver software and for occasional writing of individual words. Use of write buffer programming (see below) is strongly recommended for general programming use when more than a few words are to be programmed. The effective word programming time using write buffer programming is approximately four times shorter than the single word programming time.

**Any bit in a word cannot be programmed from 0 back to a 1.** Attempting to do so may cause the device to set DQ5=1, or cause DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still 0. Only erase operations can convert a 0 to a 1.

### 9.4.2 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass mode command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

### 9.4.3 Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system programs six unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits  $A_{MAX}-A_4$ . All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages.) This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation aborts.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter is decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address is programmed.

Once the specified number of write buffer locations are loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.

- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by  $DQ1 = 1$ ,  $DQ7 = DATA\#$  (for the last address location loaded),  $DQ6 =$  toggle, and  $DQ5 = 0$ . A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation.

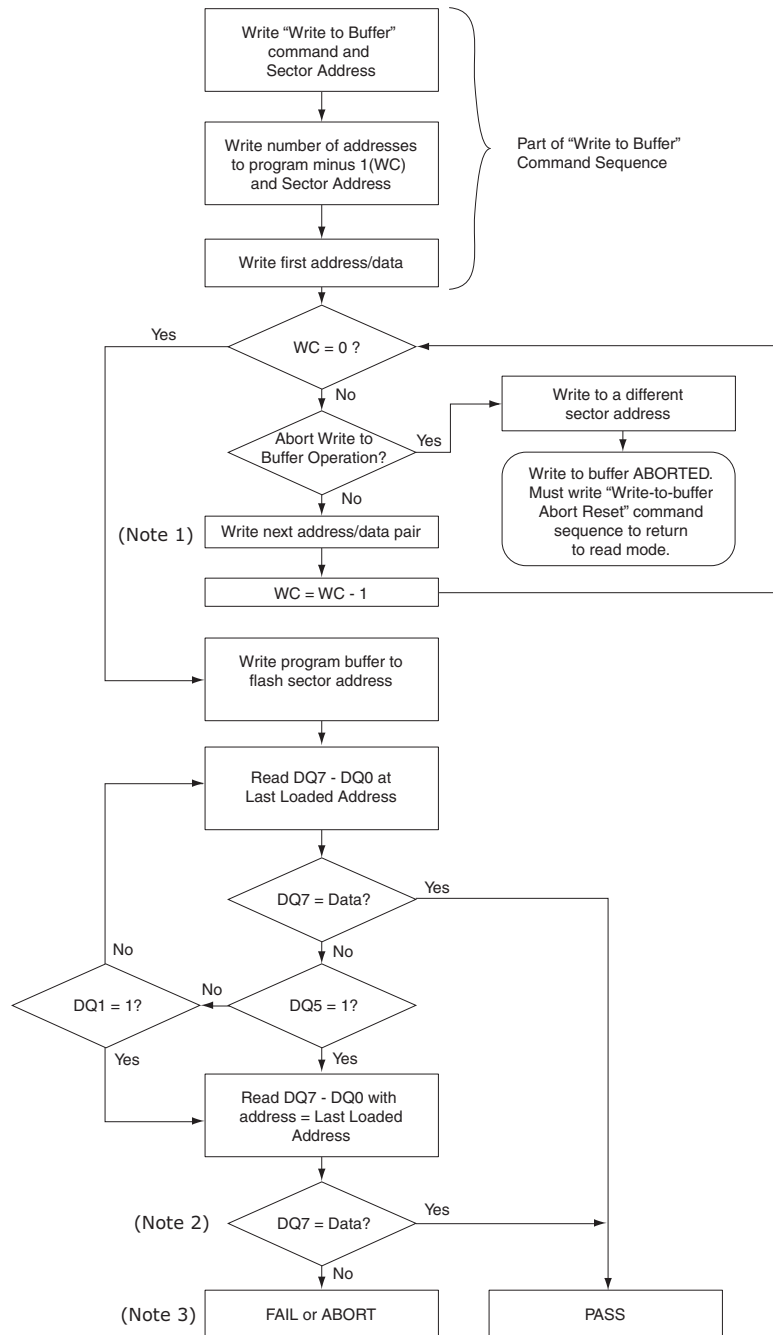
*Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.* This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. For applications requiring incremental bit programming, a modified programming method is required; please contact your local Spansion representative. **Any bit in a write buffer address range cannot be programmed from 0 back to a 1.** Attempting to do so may cause the device to set  $DQ5=1$ , or cause the  $DQ7$  and  $DQ6$  status bits to indicate the operation was successful. However, a succeeding read shows that the data is still 0. Only erase operations can convert a 0 to a 1.

#### 9.4.4 Accelerated Program

The device offers accelerated program operations through the  $WP\#/ACC$  or  $ACC$  pin depending on the particular product. When the system asserts  $V_{HH}$  on the  $WP\#/ACC$  or  $ACC$  pin. The device uses the higher voltage on the  $WP\#/ACC$  or  $ACC$  pin to accelerate the operation. *Note that the  $WP\#/ACC$  pin must not be at  $V_{HH}$  for operations other than accelerated programming, or device damage may result.  $WP\#$  contains an internal pull-up; when unconnected,  $WP\#$  is at  $V_{IH}$ .*

[Figure 9.1 on page 56](#) illustrates the algorithm for the program operation. Refer to the Erase and Program Operations—[AC Characteristics on page 72](#) for parameters, and [Figure 16.3 on page 74](#) for timing diagrams.

Figure 9.1 Write Buffer Programming Operation

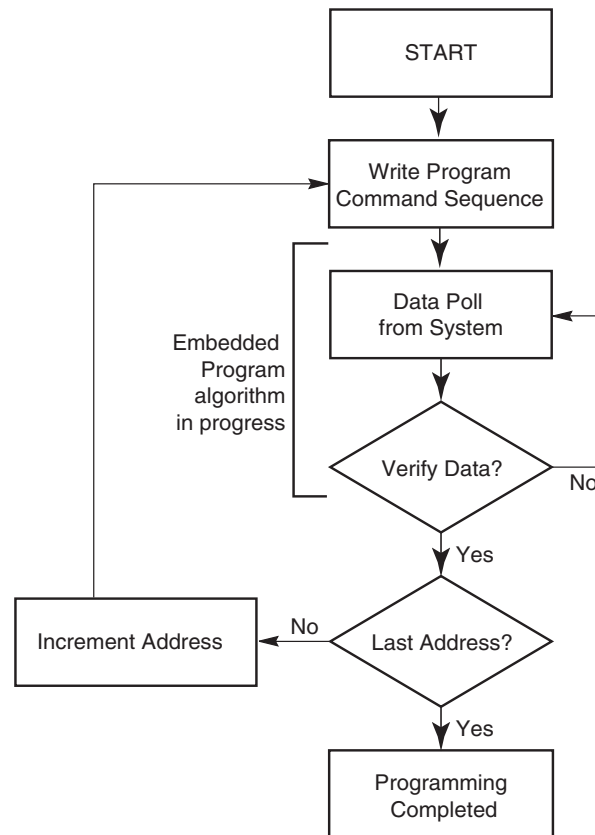


**Notes**

1. When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.
2. DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.
3. If this flowchart location was reached because DQ5= 1, then the device FAILED. If this flowchart location was reached because DQ1= 1, then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1= 1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5= 1, write the Reset command.
4. See Table 10.2 on page 61 and Table 10.1 on page 62 for command sequences required for write buffer programming.



Figure 9.2 Program Operation



Note

See [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) for program command sequence.

## 9.5 Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15  $\mu\text{s}$  maximum (5 $\mu\text{s}$  typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

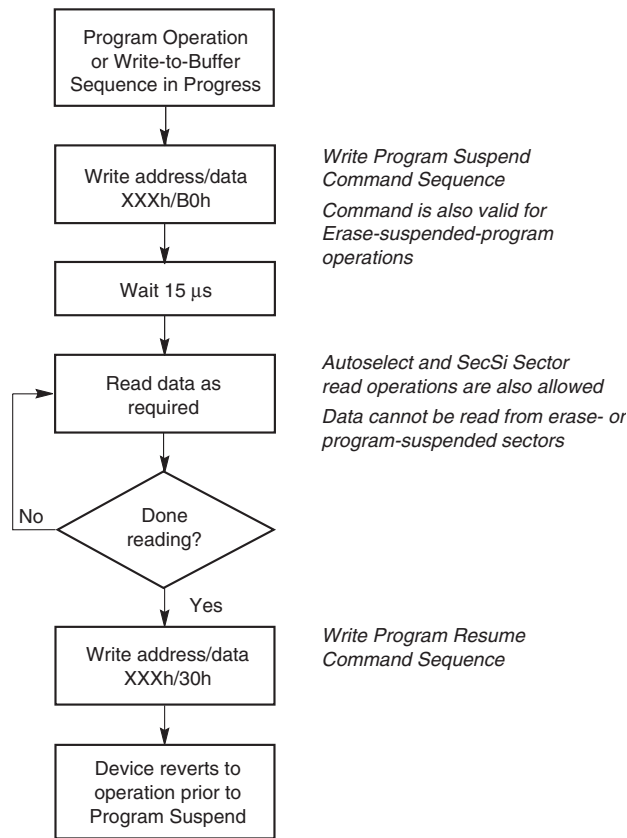
After the programming operation is suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region. Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See [Autoselect Command Sequence on page 53](#) for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See [Write Operation Status on page 63](#) for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

**Figure 9.3** Program Suspend/Program Resume



## 9.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to [Write Operation Status on page 63](#) for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If this occurs, the chip erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

[Figure 10.1 on page 59](#) illustrates the algorithm for the erase operation. Refer to [Table 16.5 on page 76](#) for parameters, and [Figure 16.7 on page 80](#) for timing diagrams.

## 10. Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50  $\mu$ s occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50  $\mu$ s, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode. Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.** The system must rewrite the command sequence and any additional addresses and commands.

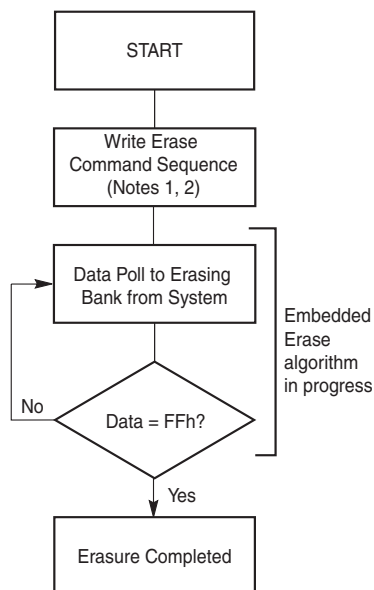
The system can monitor DQ3 to determine if the sector erase timer has timed out (See [DQ3: Sector Erase Timer on page 67](#)). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to [Write Operation Status on page 63](#) for information on these status bits.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

[Figure 10.1](#) illustrates the algorithm for the erase operation. Refer to [Table 16.5 on page 76](#) for parameters, and [Figure 16.7 on page 80](#) for timing diagrams.

**Figure 10.1** Erase Operation



### Notes

1. See [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) for program command sequence.
2. See [DQ3: Sector Erase Timer on page 67](#) for information on the sector erase timer.

## 10.1 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50  $\mu$ s time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5  $\mu$ s (maximum of 20  $\mu$ s) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation is suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device *erases suspends* all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to [Write Operation Status on page 63](#) for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to [Write Operation Status on page 63](#) for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to [Autoselect Mode on page 40](#) and [Autoselect Command Sequence on page 53](#) sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip resumes erasing.

### Note

During an erase operation, this flash device performs multiple internal operations which are invisible to the system. When an erase operation is suspended, any of the internal operations that were not fully completed must be restarted. As such, if this flash device is continually issued suspend/resume commands in rapid succession, erase progress is impeded as a function of the number of suspends. The result is a longer cumulative erase time than without suspends. Note that the additional suspends do not affect device reliability or future performance. In most systems rapid erase/suspend activity occurs only briefly. In such cases, erase performance is not significantly impacted.

## 10.2 Command Definitions

Figure 10.2 Command Definitions (x16 Mode, BYTE# = V<sub>IH</sub>)

| Command Sequence (Note 1)             | Cycles                                 | Bus Cycles (Notes 2–5) |     |        |     |       |     |         |       |           |     |           |     |           |  |
|---------------------------------------|--|------------------------|-----|--------|-----|-------|-----|---------|-------|-----------|-----|-----------|-----|-----------|--|
|                                       |  | First                  |     | Second |     | Third |     | Fourth  |       | Fifth     |     | Sixth     |     |           |  |
| Read (Note 5)                         | 1                                      | RA                     | RD  |        |     |       |     |         |       |           |     |           |     |           |  |
| Reset (Note 6)                        | 1                                      | XXX                    | F0  |        |     |       |     |         |       |           |     |           |     |           |  |
| Autoselect (Note 7)                   | Manufacturer ID                        | 4                      | 555 | AA     | 2AA | 55    | 555 | 90      | X00   | 0001      |     |           |     |           |  |
|                                       | Device ID (Note 8)                     | 6                      | 555 | AA     | 2AA | 55    | 555 | 90      | X01   | 227E      | X0E | (Note 19) | X0F | (Note 19) |  |
|                                       | Device ID (Note 9)                     | 4                      | 555 | AA     | 2AA | 55    | 555 | 90      | X01   | (Note 18) |     |           |     |           |  |
|                                       | Secured Silicon Sector Factory Protect | 4                      | 555 | AA     | 2AA | 55    | 555 | 90      | X03   | (Note 10) |     |           |     |           |  |
| Sector Group Protect Verify (Note 11) | 4                                      | 555                    | AA  | 2AA    | 55  | 555   | 90  | (SA)X02 | 00/01 |           |     |           |     |           |  |
| Enter Secured Silicon Sector Region   | 3                                      | 555                    | AA  | 2AA    | 55  | 555   | 88  |         |       |           |     |           |     |           |  |
| Exit Secured Silicon Sector Region    | 4                                      | 555                    | AA  | 2AA    | 55  | 555   | 90  | XXX     | 00    |           |     |           |     |           |  |
| Program                               | 4                                      | 555                    | AA  | 2AA    | 55  | 555   | A0  | PA      | PD    |           |     |           |     |           |  |
| Write to Buffer (Note 12)             | 3                                      | 555                    | AA  | 2AA    | 55  | SA    | 25  | SA      | WC    | PA        | PD  | WBL       | PD  |           |  |
| Program Buffer to Flash               | 1                                      | SA                     | 29  |        |     |       |     |         |       |           |     |           |     |           |  |
| Write to Buffer Abort Reset (Note 13) | 3                                      | 555                    | AA  | 2AA    | 55  | 555   | F0  |         |       |           |     |           |     |           |  |
| Unlock Bypass                         | 3                                      | 555                    | AA  | 2AA    | 55  | 555   | 20  |         |       |           |     |           |     |           |  |
| Unlock Bypass Program (Note 14)       | 2                                      | XXX                    | A0  | PA     | PD  |       |     |         |       |           |     |           |     |           |  |
| Unlock Bypass Reset (Note 15)         | 2                                      | XXX                    | 90  | XXX    | 00  |       |     |         |       |           |     |           |     |           |  |
| Chip Erase                            | 6                                      | 555                    | AA  | 2AA    | 55  | 555   | 80  | 555     | AA    | 2AA       | 55  | 555       | 10  |           |  |
| Sector Erase                          | 6                                      | 555                    | AA  | 2AA    | 55  | 555   | 80  | 555     | AA    | 2AA       | 55  | SA        | 30  |           |  |
| Program/Erase Suspend (Note 16)       | 1                                      | XXX                    | B0  |        |     |       |     |         |       |           |     |           |     |           |  |
| Program/Erase Resume (Note 17)        | 1                                      | XXX                    | 30  |        |     |       |     |         |       |           |     |           |     |           |  |
| CFI Query (Note 18)                   | 1                                      | 55                     | 98  |        |     |       |     |         |       |           |     |           |     |           |  |

### Legend

X = Don't care

RA = Read Address of memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

### Notes

1. See Table 7.1 on page 22 for description of bus operations.

2. All values are in hexadecimal.

3. Shaded cells indicate read cycles. All others are write cycles.

4. During unlock and command cycles, when lower address bits are 555 or 2AA as shown in table, address bits above A11 and data bits above DQ7 are don't care.

5. No unlock or command cycles required when device is in read mode.

6. Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.

7. Fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. Except for RD, PD and WC. See Autoselect Command Sequence on page 53 for more information.

8. For S29GL064A and S29GL032A, Device ID must be read in three cycles.

9. For S29GL016A, Device ID must be read in one cycle.

10. Refer to Table 7.12 on page 40 for data indicating Secured Silicon Sector factory protect status.

11. Data is 00h for an unprotected sector group and 01h for a protected sector group.

12. Total number of cycles in command sequence is determined by number of words written to write buffer. Maximum number of cycles in command sequence is 21, including Program Buffer to Flash command.

13. Command sequence resets device for next command after aborted write-to-buffer operation.

14. Unlock Bypass command is required prior to Unlock Bypass Program command.

15. Unlock Bypass Reset command is required to return to read mode when device is in unlock bypass mode.

16. System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.

17. Erase Resume command is valid only during Erase Suspend mode.

18. Command is valid when device is ready to read array data or when device is in autoselect mode.

19. Refer to Table 7.12 on page 40, for individual Device IDs per device density and model number.

**Table 10.1** Command Definitions (x8 Mode, BYTE# = V<sub>IL</sub>)

| Command Sequence<br>(Note 1)         | Cycles                                 | Bus Cycles (Notes 2–5) |      |        |      |       |      |        |         |          |      |          |      |          |
|--------------------------------------|--|------------------------|------|--------|------|-------|------|--------|---------|----------|------|----------|------|----------|
|                                      |  | First                  |      | Second |      | Third |      | Fourth |         | Fifth    |      | Sixth    |      |          |
|                                      |  | Addr                   | Data | Addr   | Data | Addr  | Data | Addr   | Data    | Addr     | Data | Addr     | Data |          |
| Read (Note 6)                        | 1                                      | RA                     | RD   |        |      |       |      |        |         |          |      |          |      |          |
| Reset (Note 7)                       | 1                                      | XXX                    | F0   |        |      |       |      |        |         |          |      |          |      |          |
| Autoselect (Note 8)                  | Manufacturer ID                        | 4                      | AAA  | AA     | 555  | 55    | AAA  | 90     | X00     | 01       |      |          |      |          |
|                                      | Device ID (Note 9)                     | 6                      | AAA  | AA     | 555  | 55    | AAA  | 90     | X02     | 7E       | X1C  | (Note 9) | X1E  | (Note 9) |
|                                      | Device ID (Note 1)                     | 4                      | AAA  | AA     | 555  | 55    | AAA  | 90     | X02     | (Note 2) |      |          |      |          |
|                                      | Secured Silicon Sector Factory Protect | 4                      | AAA  | AA     | 555  | 55    | AAA  | 90     | X06     | (Note 1) |      |          |      |          |
|                                      | Sector Group Protect Verify (Note 3)   | 4                      | AAA  | AA     | 555  | 55    | AAA  | 90     | (SA)X04 | 00/01    |      |          |      |          |
| Enter Secured Silicon Sector Region  | 3                                      | AAA                    | AA   | 555    | 55   | AAA   | 88   |        |         |          |      |          |      |          |
| Exit Secured Silicon Sector Region   | 4                                      | AAA                    | AA   | 555    | 55   | AAA   | 90   | XXX    | 00      |          |      |          |      |          |
| Write to Buffer (Note 4)             | 3                                      | AAA                    | AA   | 555    | 55   | SA    | 25   | SA     | BC      | PA       | PD   | WBL      | PD   |          |
| Program Buffer to Flash              | 1                                      | SA                     | 29   |        |      |       |      |        |         |          |      |          |      |          |
| Write to Buffer Abort Reset (Note 5) | 3                                      | AAA                    | AA   | 555    | 55   | AAA   | F0   |        |         |          |      |          |      |          |
| Chip Erase                           | 6                                      | AAA                    | AA   | 555    | 55   | AAA   | 80   | AAA    | AA      | 555      | 55   | AAA      | 10   |          |
| Sector Erase                         | 6                                      | AAA                    | AA   | 555    | 55   | AAA   | 80   | AAA    | AA      | 555      | 55   | SA       | 30   |          |
| Program/Erase Suspend (Note 6)       | 1                                      | XXX                    | B0   |        |      |       |      |        |         |          |      |          |      |          |
| Program/Erase Resume (Note 7)        | 1                                      | XXX                    | 30   |        |      |       |      |        |         |          |      |          |      |          |
| CFI Query (Note 8)                   | 1                                      | AA                     | 98   |        |      |       |      |        |         |          |      |          |      |          |

**Legend**

X = Don't care  
 RA = Read Address of memory location to be read.  
 RD = Read Data read from location RA during read operation.  
 PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.  
 PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.  
 WBL = Write Buffer Location. Address must be within same write buffer page as PA.  
 BC = Byte Count. Number of write buffer locations to load minus 1.

**Notes**

- See Table 7.1 on page 22 for description of bus operations.
- All values are in hexadecimal.
- Shaded cells indicate read cycles. All others are write cycles.
- During unlock and command cycles, when lower address bits are 555 or AAA as shown in table, address bits above A11 are don't care.
- Unless otherwise noted, address bits A21–A11 are don't cares.
- No unlock or command cycles required when device is in read mode.
- Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.
- Fourth cycle of autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See Autoselect Command Sequence on page 53 or more information.
- For S29GL064A and S29GL032A Device ID must be read in three cycles.
- For S29GL016A, Device ID must be read in one cycle.
- Refer to Table 7.12 on page 40, for data indicating Secured Silicon Sector factory protect status.
- Data is 00h for an unprotected sector group and 01h for a protected sector group.
- Total number of cycles in command sequence is determined by number of bytes written to write buffer. Maximum number of cycles in command sequence is 37, including Program Buffer to Flash command.
- Command sequence resets device for next command after aborted write-to-buffer operation.
- System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.
- Erase Resume command is valid only during Erase Suspend mode.
- Command is valid when device is ready to read array data or when device is in autoselect mode.
- Refer to Table 7.12 on page 40, for individual Device IDs per device density and model number.

### 10.3 Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. [Table 10.2 on page 68](#) and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or is completed.

### 10.4 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1  $\mu$ s, then the device returns to the read mode.

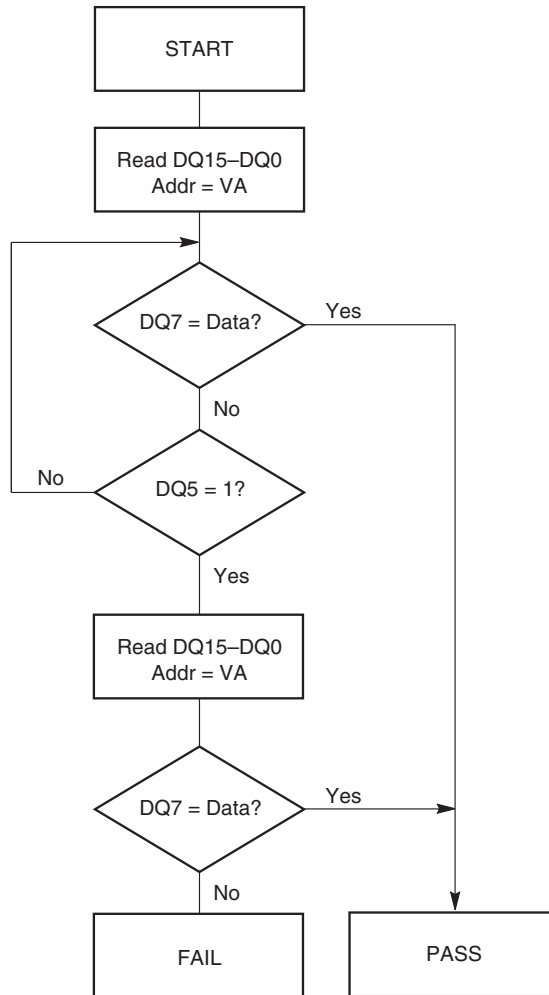
During the Embedded Erase algorithm, Data# Polling produces a 0 on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a 1 on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100  $\mu$ s, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 appears on successive read cycles.

[Table 10.2 on page 68](#) shows the outputs for Data# Polling on DQ7. [Figure 10.3 on page 64](#) shows the Data# Polling algorithm. [Figure 16.8 on page 80](#) shows the Data# Polling timing diagram.

**Figure 10.3** Data# Polling Algorithm



**Notes**

1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

## 10.5 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V<sub>CC</sub>.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. [Table 10.2 on page 68](#) shows the outputs for RY/BY#.



## 10.6 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100  $\mu$ s, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

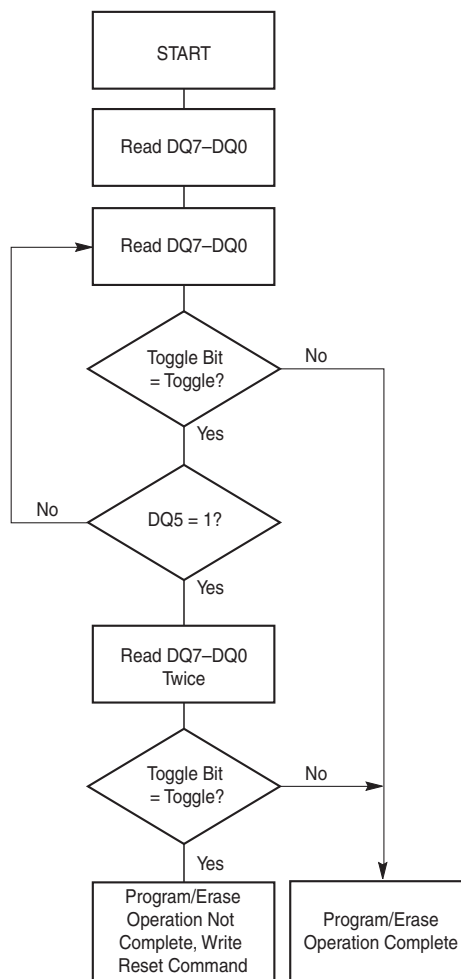
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see [DQ7: Data# Polling on page 63](#)).

If a program address falls within a protected sector, DQ6 toggles for approximately 1  $\mu$ s after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

[Table 10.2 on page 68](#) shows the outputs for Toggle Bit I on DQ6. [Figure 10.4 on page 66](#) shows the toggle bit algorithm. [Figure 16.9 on page 81](#) shows the toggle bit timing diagrams. [Figure 16.10 on page 81](#) shows the differences between DQ2 and DQ6 in graphical form. See [DQ2: Toggle Bit II on page 66](#).

Figure 10.4 Toggle Bit Algorithm



**Note**

The system should recheck the toggle bit even if DQ5 = 1 because the toggle bit may stop toggling as DQ5 changes to 1. See [DQ6: Toggle Bit I on page 65](#) and [DQ2: Toggle Bit II on page 66](#) for more information.

## 10.7 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that were selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to [Table 10.2 on page 68](#) to compare outputs for DQ2 and DQ6.

[Figure 10.4 on page 66](#) shows the toggle bit algorithm in flowchart form, and [DQ2: Toggle Bit II on page 66](#) explains the algorithm. See also [RY/BY#: Ready/Busy# on page 64](#). [Figure 16.9 on page 81](#) shows the toggle bit timing diagram. [Figure 16.10 on page 81](#) shows the differences between DQ2 and DQ6 in graphical form.

## 10.8 Reading Toggle Bits DQ6/DQ2

Refer to [Figure 10.4 on page 66](#) for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see [DQ5: Exceeded Timing Limits on page 67](#)). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of [Figure 10.4 on page 66](#)).

## 10.9 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*, indicating that the program or erase cycle was not successfully completed.

The device may output a *1* on DQ5 if the system tries to program a *1* to a location that was previously programmed to *0*. **Only an erase operation can change a *0* back to a *1*.** Under this condition, the device halts the operation, and when the timing limit is exceeded, DQ5 produces a *1*.

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

## 10.10 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure began. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a *0* to a *1*. If the time between additional sector erase commands from the system can be assumed to be less than 50  $\mu$ s, the system need not monitor DQ3. See [Sector Erase Command Sequence on page 59](#).

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device accepted the command sequence, and then read DQ3. If DQ3 is *1*, the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device accepts additional sector erase commands. To ensure the command is accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

[Table 10.2 on page 68](#) shows the status of DQ3 relative to the other status bits.

### 10.11 DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a 1. The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See [Write Buffer on page 24](#) for more details.

**Table 10.2** Write Operation Status

| Status               |                            | DQ7<br>(Note 2)                          | DQ6                   | DQ5<br>(Note 1) | DQ3 | DQ2<br>(Note 2) | DQ1    | RY/BY# |   |
|----------------------|----------------------------|--|-----------------------|-----------------|-----|-----------------|--------|--------|---|
| Standard Mode        | Embedded Program Algorithm | DQ7#                                     | Toggle                | 0               | N/A | No toggle       | 0      | 0      |   |
|                      | Embedded Erase Algorithm   | 0  | Toggle                | 0               | 1   | Toggle          | N/A    | 0      |   |
| Program Suspend Mode | Program-Suspend Read       | Program-Suspended Sector                 | Invalid (not allowed) |                 |     |                 |        | 1      |   |
|                      |                            | Non-Program Suspended Sector             | Data                  |                 |     |                 |        | 1      |   |
| Erase Suspend Mode   | Erase-Suspend Read         | Erase-Suspended Sector                   | 1                     | No toggle       | 0   | N/A             | Toggle | N/A    | 1 |
|                      |                            | Non-Erase Suspended Sector               | Data                  |                 |     |                 |        | 1      |   |
|                      |                            | Erase-Suspend-Program (Embedded Program) | DQ7#                  | Toggle          | 0   | N/A             | N/A    | N/A    | 0 |
| Write-to-Buffer      | Busy (Note 3)              | DQ7#                                     | Toggle                | 0               | N/A | N/A             | 0      | 0      |   |
|                      | Abort (Note 4)             | DQ7#                                     | Toggle                | 0               | N/A | N/A             | 1      | 0      |   |

**Notes**

1. DQ5 switches to 1 when an Embedded Program, Embedded Erase, or Write-to-Buffer operation exceeded the maximum timing limits. Refer to [DQ5: Exceeded Timing Limits on page 67](#) for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.
4. DQ1 switches to 1 when the device aborts the write-to-buffer operation.

## 11. Absolute Maximum Ratings

| Description                            |                                  | Rating                   |
|--|----------------------------------|--------------------------|
| Storage Temperature, Plastic Packages  |                                  | -65°C to +150°C          |
| Ambient Temperature with Power Applied |                                  | -65°C to +125°C          |
| Voltage with Respect to Ground         | $V_{CC}$ (Note 1)                | -0.5 V to +4.0 V         |
|  | A9, OE#, ACC and RESET# (Note 2) | -0.5 V to +12.5 V        |
|  | All other pins (Note 1)          | -0.5 V to $V_{CC}+0.5$ V |
| Output Short Circuit Current (Note 3)  |                                  | 200 mA                   |

### Notes

- Minimum DC voltage on input or I/Os is -0.5 V. During voltage transitions, inputs or I/Os may overshoot  $V_{SS}$  to -2.0 V for periods of up to 20 ns. See [Figure 11.1 on page 69](#). Maximum DC voltage on input or I/Os is  $V_{CC} + 0.5$  V. During voltage transitions, input or I/O pins may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns. See [Figure 11.2 on page 69](#).
- Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is -0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot  $V_{SS}$  to -2.0 V for periods of up to 20 ns. See [Figure 11.1 on page 69](#). Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0V for periods up to 20 ns.
- No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 11.1 Maximum Negative Overshoot Waveform

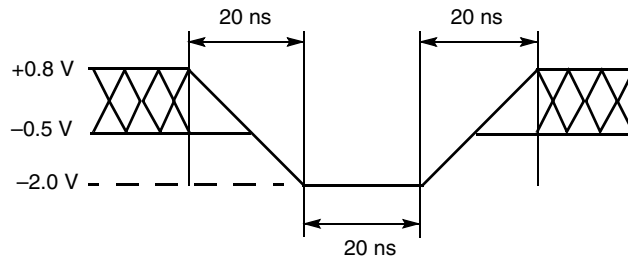
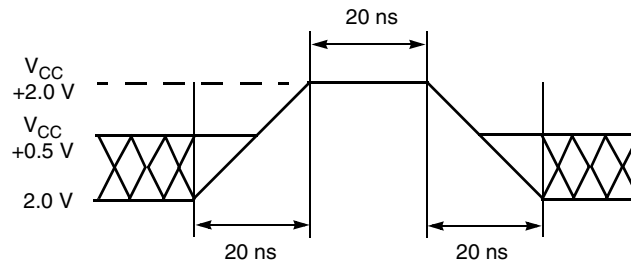


Figure 11.2 Maximum Positive Overshoot Waveform



## 12. Operating Ranges

| Description   |                                      | Range            |
|---|--------------------------------------|------------------|
| Ambient Temperature ( $T_A$ ), Industrial (I) Devices |                                      | -40°C to +85°C   |
| Supply Voltages                                       | $V_{CC}$ for full voltage range      | +2.7 V to +3.6 V |
|   | $V_{CC}$ for regulated voltage range | +3.0 V to +3.6 V |
| $V_{IO}$  |                                      | $V_{CC}$         |

### Note

Operating ranges define those limits between which the functionality of the device is guaranteed.

### 13. DC Characteristics

#### 13.1 CMOS Compatible

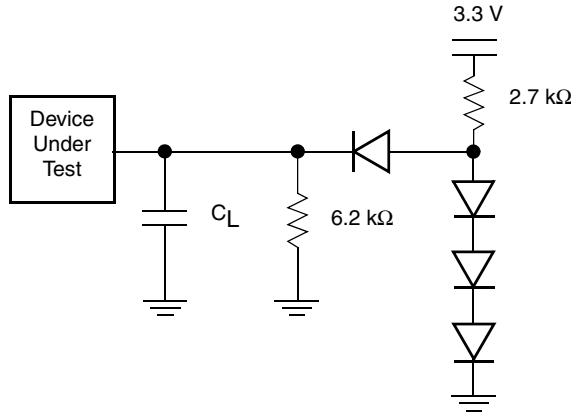
| Parameter Symbol | Parameter Description (Notes)                         | Test Conditions  | Min            | Typ  | Max            | Unit |
|------------------|---|--|----------------|------|----------------|------|
| $I_{LI}$         | Input Load Current (Note 1)                           | $V_{IN} = V_{SS}$ to $V_{CC}$ ,<br>$V_{CC} = V_{CC\ max}$                      |                |      | ±1.0           | µA   |
| $I_{LIT}$        | A9, ACC Input Load Current                            | $V_{CC} = V_{CC\ max}$ ; A9 = 12.5 V   | -40°C to 0°C   |      | 250            | µA   |
|                  |   |  | 0°C to 85°C    |      | 35             |      |
| $I_{LR}$         | Reset Leakage Current                                 | $V_{CC} = V_{CC\ max}$ ; RESET# = 12.5 V                                       |                |      | 35             | µA   |
| $I_{LO}$         | Output Leakage Current                                | $V_{OUT} = V_{SS}$ to $V_{CC}$ ,<br>$V_{CC} = V_{CC\ max}$                     |                |      | ±1.0           | µA   |
| $I_{CC1}$        | $V_{CC}$ Initial Read Current (Notes 2, 3)            | CE# = $V_{IL}$ , OE# = $V_{IH}$  | 1 MHz          | 5    | 20             | mA   |
|                  |   |  | 5 MHz          | 18   | 25             |      |
|                  |   |  | 10 MHz         | 35   | 50             |      |
| $I_{CC2}$        | $V_{CC}$ Intra-Page Read Current (Notes 2, 3)         | CE# = $V_{IL}$ , OE# = $V_{IH}$  | 10 MHz         | 5    | 20             | mA   |
|                  |   |  | 40 MHz         | 10   | 40             |      |
| $I_{CC3}$        | $V_{CC}$ Active Write Current (Note 3)                | CE# = $V_{IL}$ , OE# = $V_{IH}$  |                | 50   | 60             | mA   |
| $I_{CC4}$        | $V_{CC}$ Standby Current (Note 3)                     | CE#, RESET# = $V_{CC} \pm 0.3\ V$ ,<br>WP# = $V_{IH}$                          |                | 1    | 5              | µA   |
| $I_{CC5}$        | $V_{CC}$ Reset Current (Note 3)                       | RESET# = $V_{SS} \pm 0.3\ V$ , WP# = $V_{IH}$                                  |                | 1    | 5              | µA   |
| $I_{CC6}$        | Automatic Sleep Mode (Notes 3, 5)                     | $V_{IH} = V_{CC} \pm 0.3\ V$ ;<br>$-0.1 < V_{IL} \leq 0.3\ V$ , WP# = $V_{IH}$ |                | 1    | 5              | µA   |
| $V_{IL}$         | Input Low Voltage 1 (Note 6)                          |  | -0.5           |      | 0.8            | V    |
| $V_{IH}$         | Input High Voltage 1 (Note 6)                         |  | 0.7 $V_{CC}$   |      | $V_{CC} + 0.5$ | V    |
| $V_{HH}$         | Voltage for ACC Program Acceleration                  | $V_{CC} = 2.7 - 3.6\ V$  | 11.5           | 12.0 | 12.5           | V    |
| $V_{ID}$         | Voltage for Autoselect and Temporary Sector Unprotect | $V_{CC} = 2.7 - 3.6\ V$  | 11.5           | 12.0 | 12.5           | V    |
| $V_{OL}$         | Output Low Voltage (Note 6)                           | $I_{OL} = 4.0\ mA$ , $V_{CC} = V_{CC\ min}$                                    |                |      | 0.45           | V    |
| $V_{OH1}$        | Output High Voltage                                   | $I_{OH} = -2.0\ mA$ , $V_{CC} = V_{CC\ min}$                                   | 0.85 $V_{CC}$  |      |                | V    |
| $V_{OH2}$        |   | $I_{OH} = -100\ \mu A$ , $V_{CC} = V_{CC\ min}$                                | $V_{CC} - 0.4$ |      |                | V    |
| $V_{LKO}$        | Low $V_{CC}$ Lock-Out Voltage (Note 7)                |  | 2.3            |      | 2.5            | V    |

**Notes**

1. On the WP#/ACC pin only, the maximum input load current when WP# =  $V_{IL}$  is ± 5.0 µA.
2. The  $I_{CC}$  current listed is typically less than 3.5 mA/MHz, with OE# at  $V_{IH}$ .
3. Maximum  $I_{CC}$  specifications are tested with  $V_{CC} = V_{CC\ max}$ .
4.  $I_{CC}$  active while Embedded Erase or Embedded Program is in progress.
5. Automatic sleep mode enables the low power mode when addresses remain stable for  $t_{ACC} + 30\ ns$ .
6.  $V_{CC}$  voltage requirements.
7. Not 100% tested.

## 14. Test Conditions

Figure 14.1 Test Setup



**Note**  
Diodes are IN3064 or equivalent.

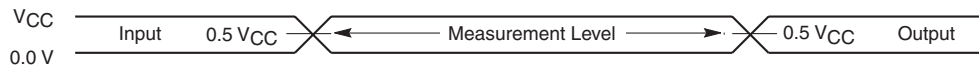
Table 14.1 Test Specifications

| Test Condition  | All Speeds      | Unit |
|---|-----------------|------|
| Output Load   | 1 TTL gate      |      |
| Output Load Capacitance, $C_L$<br>(including jig capacitance) | 30              | pF   |
| Input Rise and Fall Times                                     | 5               | ns   |
| Input Pulse Levels  | 0.0 or $V_{CC}$ | V    |
| Input timing measurement reference levels                     | $0.5 V_{CC}$    | V    |
| Output timing measurement reference levels                    | $0.5 V_{CC}$    | V    |

## 15. Key to Switching Waveforms

| Waveform | Inputs                           | Outputs                                      |
|----------|----------------------------------|--|
|          | Steady                           |  |
|          | Changing from H to L             |  |
|          | Changing from L to H             |  |
|          | Don't Care, Any Change Permitted | Changing, State Unknown                      |
|          | Does Not Apply                   | Center Line is High Impedance State (High Z) |

Figure 15.1 Input Waveforms and Measurement Levels



## 16. AC Characteristics

**Table 16.1** Read-Only Operations-S29GL064A Only

| Parameter         |                   | Description   | Test Setup                 |     | Speed Options |     |     | Unit |
|-------------------|-------------------|---|----------------------------|-----|---------------|-----|-----|------|
| JEDEC             | Std.              |   |                            |     | 90            | 10  | 11  |      |
| t <sub>AVAV</sub> | t <sub>RC</sub>   | Read Cycle Time (Note 1)  |                            | Min | 90            | 100 | 110 | ns   |
| t <sub>AVQV</sub> | t <sub>ACC</sub>  | Address to Output Delay   | CE#, OE# = V <sub>IL</sub> | Max | 90            | 100 | 110 | ns   |
| t <sub>ELQV</sub> | t <sub>CE</sub>   | Chip Enable to Output Delay   | OE# = V <sub>IL</sub>      | Max | 90            | 100 | 110 | ns   |
|                   | t <sub>PACC</sub> | Page Access Time  |                            | Max | 25            | 30  | 30  | ns   |
| t <sub>GLQV</sub> | t <sub>OE</sub>   | Output Enable to Output Delay                                       |                            | Max | 25            | 30  | 30  | ns   |
| t <sub>EHQZ</sub> | t <sub>DF</sub>   | Chip Enable to Output High Z (Note 1)                               |                            | Max | 16            |     |     | ns   |
| t <sub>GHQZ</sub> | t <sub>DF</sub>   | Output Enable to Output High Z (Note 1)                             |                            | Max | 16            |     |     | ns   |
| t <sub>AXQX</sub> | t <sub>OH</sub>   | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First |                            | Min | 0             |     |     | ns   |
|                   | t <sub>OEH</sub>  | Output Enable Hold Time (Note 1)                                    | Read                       | Min | 0             |     |     | ns   |
|                   |                   |   | Toggle and Data# Polling   | Min | 10            |     |     | ns   |

**Notes**

1. Not 100% tested.
2. See Figure 14.1 on page 71 and Table 14.1 on page 71 for test specifications

**Table 16.2** Read-Only Operations-S29GL032A Only

| Parameter         |                   | Description   | Test Setup                 |     | Speed Options |     |     | Unit |
|-------------------|-------------------|---|----------------------------|-----|---------------|-----|-----|------|
| JEDEC             | Std.              |   |                            |     | 90            | 10  | 11  |      |
| t <sub>AVAV</sub> | t <sub>RC</sub>   | Read Cycle Time (Note 1)  |                            | Min | 90            | 100 | 110 | ns   |
| t <sub>AVQV</sub> | t <sub>ACC</sub>  | Address to Output Delay   | CE#, OE# = V <sub>IL</sub> | Max | 90            | 100 | 110 | ns   |
| t <sub>ELQV</sub> | t <sub>CE</sub>   | Chip Enable to Output Delay   | OE# = V <sub>IL</sub>      | Max | 90            | 100 | 110 | ns   |
|                   | t <sub>PACC</sub> | Page Access Time  |                            | Max | 25            | 30  | 30  | ns   |
| t <sub>GLQV</sub> | t <sub>OE</sub>   | Output Enable to Output Delay                                       |                            | Max | 25            | 30  | 30  | ns   |
| t <sub>EHQZ</sub> | t <sub>DF</sub>   | Chip Enable to Output High Z (Note 1)                               |                            | Max | 16            |     |     | ns   |
| t <sub>GHQZ</sub> | t <sub>DF</sub>   | Output Enable to Output High Z (Note 1)                             |                            | Max | 16            |     |     | ns   |
| t <sub>AXQX</sub> | t <sub>OH</sub>   | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First |                            | Min | 0             |     |     | ns   |
|                   | t <sub>OEH</sub>  | Output Enable Hold Time (Note 1)                                    | Read                       | Min | 0             |     |     | ns   |
|                   |                   |   | Toggle and Data# Polling   | Min | 10            |     |     | ns   |

**Notes**

1. Not 100% tested.
2. See Figure 14.1 on page 71 and Table 14.1 on page 71 for test specifications.



**Table 16.3** Read-Only Operation-S29GL016A Only

| Parameter  |            | Description   | Test Setup          |     | Speed Options |     | Unit |
|------------|------------|---|---------------------|-----|---------------|-----|------|
| JEDEC      | Std.       |   |                     |     | 90            | 10  |      |
| $t_{AVAV}$ | $t_{RC}$   | Read Cycle Time (Note 1)  |                     | Min | 90            | 100 | ns   |
| $t_{AVQV}$ | $t_{ACC}$  | Address to Output Delay   | CE#, OE# = $V_{IL}$ | Max | 90            | 100 | ns   |
| $t_{ELQV}$ | $t_{CE}$   | Chip Enable to Output Delay   | OE# = $V_{IL}$      | Max | 90            | 100 | ns   |
|            | $t_{PACC}$ | Page Access Time  |                     | Max | 25            | 30  | ns   |
| $t_{GLQV}$ | $t_{OE}$   | Output Enable to Output Delay                                       |                     | Max | 25            | 30  | ns   |
| $t_{EHQZ}$ | $t_{DF}$   | Chip Enable to Output High Z (Note 1)                               |                     | Max | 16            |     | ns   |
| $t_{GHQZ}$ | $t_{DF}$   | Output Enable to Output High Z (Note 1)                             |                     | Max | 16            |     | ns   |
| $t_{AXQX}$ | $t_{OH}$   | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First |                     | Min | 0             |     | ns   |
|            | $t_{OEh}$  | Output Enable Hold Time (Note 1)                                    | Read                | Min | 0             |     | ns   |
|            |            | Toggle and Data# Polling  |                     | Min | 10            |     | ns   |

**Notes**

1. Not 100% tested.
2. See Figure 14.1 on page 71 and Table 14.1 on page 71 for test specifications.

**Figure 16.1**  $V_{CC}$  Power-up Diagram

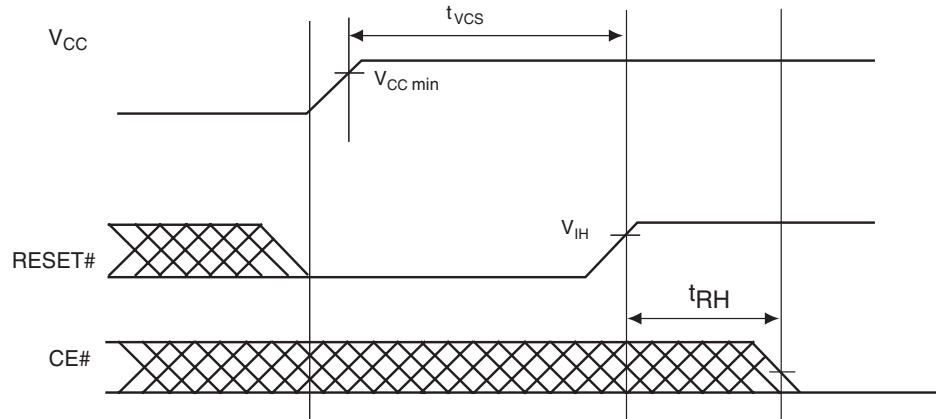


Figure 16.2 Read Operation Timings

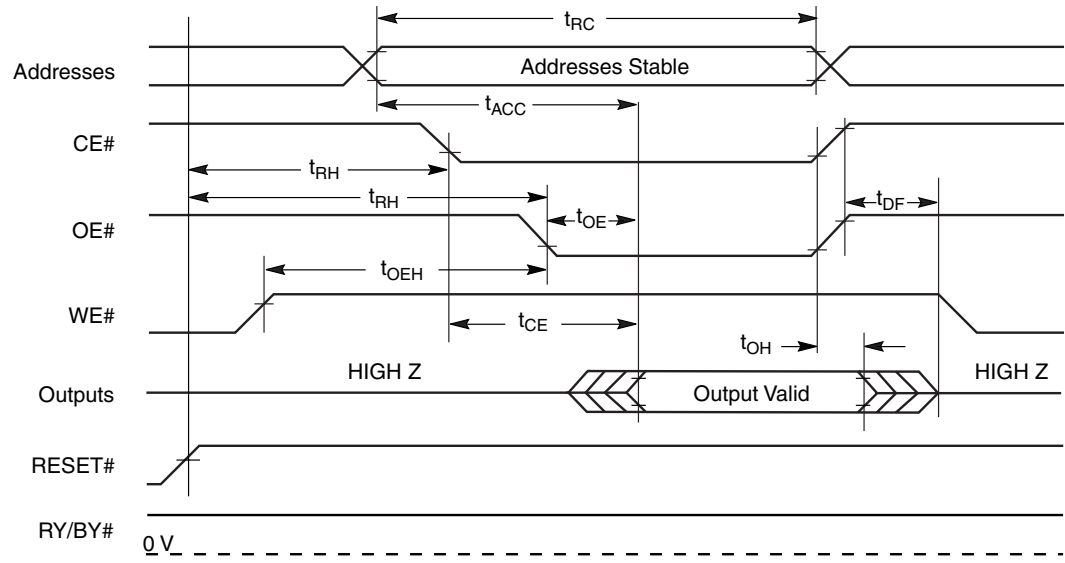
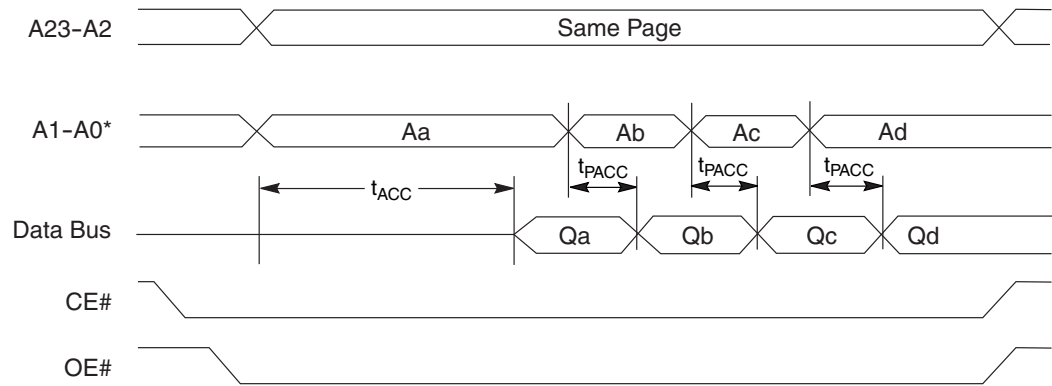


Figure 16.3 Page Read Timings



**Note**

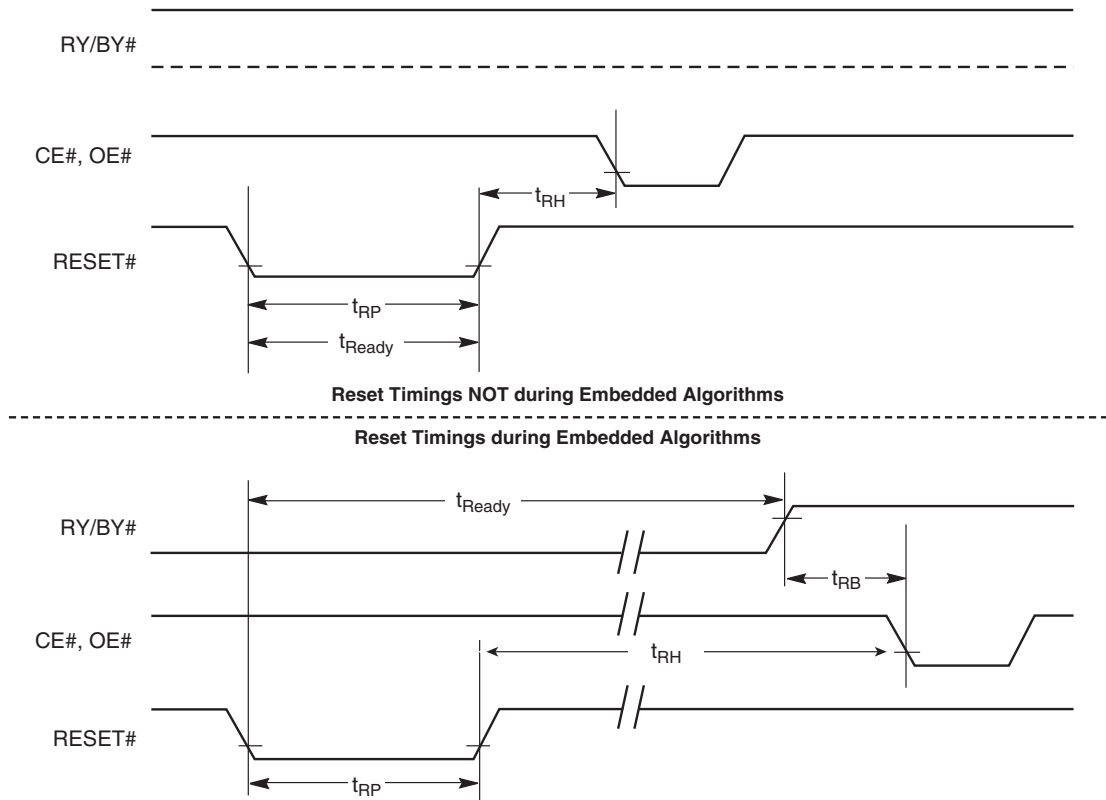
\* Figure shows device in word mode. Addresses are A1-A-1 for byte mode.

**Table 16.4** Hardware Reset (RESET#)

| Parameter |             | Description  |     | All Speed Options | Unit    |
|-----------|-------------|--|-----|-------------------|---------|
| JEDEC     | Std.        |  |     |                   |         |
|           | $t_{Ready}$ | RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)    | Max | 20                | $\mu s$ |
|           | $t_{Ready}$ | RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode(See Note) | Max | 500               | ns      |
|           | $t_{RP}$    | RESET# Pulse Width   | Min | 500               | ns      |
|           | $t_{RH}$    | Reset High Time Before Read (See Note)                                 | Min | 50                | ns      |
|           | $t_{RPD}$   | RESET# Input Low to Standby Mode (See Note)                            | Min | 20                | $\mu s$ |
|           | $t_{RB}$    | RY/BY# Output High to CE#, OE# pin Low                                 | Min | 0                 | ns      |

**Note**  
Not 100% tested.

**Figure 16.4** Reset Timings



- Notes**
1. Not 100% tested.
  2. See the [Erase And Programming Performance on page 87](#) for more information.
  3. For 1–16 words/1–32 bytes programmed.

Table 16.5 Erase and Program Operations-S29GL064A

| Parameter   |             | Description  |     | Speed Options |     |     | Unit    |
|-------------|-------------|--|-----|---------------|-----|-----|---------|
| JEDEC       | Std.        |  |     | 90            | 10  | 11  |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)  | Min | 90            | 100 | 110 | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time   | Min | 0             |     |     | ns      |
|             | $t_{ASO}$   | Address Setup Time to OE# low during toggle bit polling          | Min | 15            |     |     | ns      |
| $t_{WLAX}$  | $t_{AH}$    | Address Hold Time  | Min | 45            |     |     | ns      |
|             | $t_{AHT}$   | Address Hold Time From CE# or OE# high during toggle bit polling | Min | 0             |     |     | ns      |
| $t_{DVWH}$  | $t_{DS}$    | Data Setup Time  | Min | 35            |     |     | ns      |
| $t_{WHDX}$  | $t_{DH}$    | Data Hold Time   | Min | 0             |     |     | ns      |
|             | $t_{CEPH}$  | CE# High during toggle bit polling                               | Min | 20            |     |     | ns      |
|             | $t_{OEPH}$  | OE# High during toggle bit polling                               | Min | 20            |     |     | ns      |
| $t_{GHWL}$  | $t_{GHWL}$  | Read Recovery Time Before Write (OE# High to WE# Low)            | Min | 0             |     |     | ns      |
| $t_{ELWL}$  | $t_{CS}$    | CE# Setup Time   | Min | 0             |     |     | ns      |
| $t_{WHEH}$  | $t_{CH}$    | CE# Hold Time  | Min | 0             |     |     | ns      |
| $t_{WLWH}$  | $t_{WP}$    | Write Pulse Width  | Min | 35            |     |     | ns      |
| $t_{WHDL}$  | $t_{WPH}$   | Write Pulse Width High   | Min | 30            |     |     | ns      |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Note 2, 3)                       | Typ | 240           |     |     | $\mu$ s |
|             |             | Single Word Program Operation (Note 2)                           | Typ | 60            |     |     |         |
|             |             | Accelerated Single Word Program Operation (Note 2)               | Typ | 54            |     |     |         |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2)                                  | Typ | 0.5           |     |     | sec     |
|             | $t_{VHH}$   | $V_{HH}$ Rise and Fall Time (Note 1)                             | Min | 250           |     |     | ns      |
|             | $t_{VCS}$   | $V_{CC}$ Setup Time (Note 1)                                     | Min | 50            |     |     | $\mu$ s |
|             | $t_{BUSY}$  | WE# High to RY/BY# Low   | Min | 90            | 100 | 110 | ns      |
|             | $t_{POLL}$  | Program Valid before Status Polling                              | Max | 4             |     |     | $\mu$ s |

**Notes**

1. Not 100% tested.
2. See the [Erase And Programming Performance on page 87](#) for more information.
3. For 1–16 words/1–32 bytes programmed.
4. If a program suspend command is issued within  $t_{POLL}$ , the device requires  $t_{POLL}$  before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after  $t_{POLL}$ , status data is available immediately after programming resumes. See [Figure 16.5 on page 79](#).

Table 16.6 Erase and Program Operations-S29GL032A Only

| Parameter   |             | Description  |     | Speed Options |     |     | Unit    |
|-------------|-------------|--|-----|---------------|-----|-----|---------|
| JEDEC       | Std.        |  |     | 90            | 10  | 11  |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)  | Min | 90            | 100 | 110 | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time   | Min | 0             |     |     | ns      |
|             | $t_{ASO}$   | Address Setup Time to OE# low during toggle bit polling          | Min | 15            |     |     | ns      |
| $t_{WLAX}$  | $t_{AH}$    | Address Hold Time  | Min | 45            |     |     | ns      |
|             | $t_{AHT}$   | Address Hold Time From CE# or OE# high during toggle bit polling | Min | 0             |     |     | ns      |
| $t_{DVWH}$  | $t_{DS}$    | Data Setup Time  | Min | 35            |     |     | ns      |
| $t_{WHDX}$  | $t_{DH}$    | Data Hold Time   | Min | 0             |     |     | ns      |
|             | $t_{CEPH}$  | CE# High during toggle bit polling                               | Min | 20            |     |     | ns      |
|             | $t_{OEPH}$  | OE# High during toggle bit polling                               | Min | 20            |     |     | ns      |
| $t_{GHWL}$  | $t_{GHWL}$  | Read Recovery Time Before Write (OE# High to WE# Low)            | Min | 0             |     |     | ns      |
| $t_{ELWL}$  | $t_{CS}$    | CE# Setup Time   | Min | 0             |     |     | ns      |
| $t_{WHEH}$  | $t_{CH}$    | CE# Hold Time  | Min | 0             |     |     | ns      |
| $t_{WLWH}$  | $t_{WP}$    | Write Pulse Width  | Min | 35            |     |     | ns      |
| $t_{WHDL}$  | $t_{WPH}$   | Write Pulse Width High   | Min | 30            |     |     | ns      |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Note 2, 3)                       | Typ | 240           |     |     | $\mu$ s |
|             |             | Single Word Program Operation (Note 2)                           | Typ | 60            |     |     |         |
|             |             | Accelerated Single Word Program Operation (Note 2)               | Typ | 54            |     |     |         |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2)                                  | Typ | 0.5           |     |     | sec     |
|             | $t_{VHH}$   | $V_{HH}$ Rise and Fall Time (Note 1)                             | Min | 250           |     |     | ns      |
|             | $t_{VCS}$   | $V_{CC}$ Setup Time (Note 1)                                     | Min | 50            |     |     | $\mu$ s |
|             | $t_{BUSY}$  | WE# High to RY/BY# Low   | Min | 90            | 100 | 110 | ns      |
|             | $t_{POLL}$  | Program Valid before Status Polling                              | Max | 4             |     |     | $\mu$ s |

**Notes**

1. Not 100% tested.
2. See [Erase And Programming Performance on page 87](#) for more information
3. For 1–16 words/1–32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. If a program suspend command is issued within  $t_{POLL}$ , the device requires  $t_{POLL}$  before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after  $t_{POLL}$ , status data is available immediately after programming resumes. See [Figure 16.5 on page 79](#).

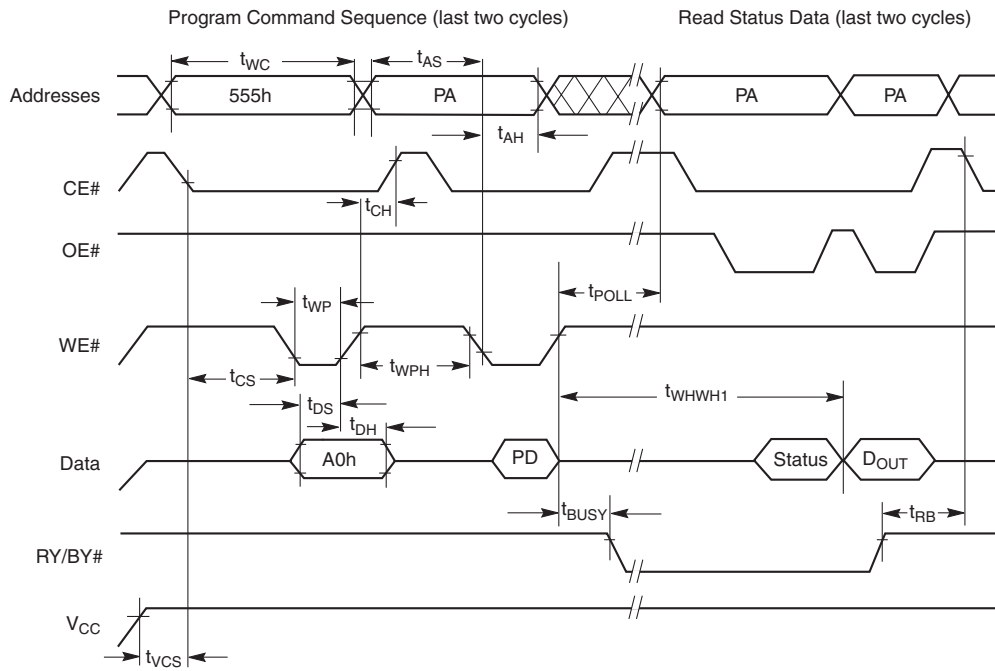
**Table 16.7** Erase and Program Operations-S29GL016A Only

| Parameter   |             | Description  |     | Speed Options |     | Unit    |
|-------------|-------------|--|-----|---------------|-----|---------|
| JEDEC       | Std.        |  |     | 90            | 10  |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)  | Min | 90            | 100 | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time   | Min | 0             |     | ns      |
|             | $t_{ASO}$   | Address Setup Time to OE# low during toggle bit polling          | Min | 15            |     | ns      |
| $t_{WLAX}$  | $t_{AH}$    | Address Hold Time  | Min | 45            |     | ns      |
|             | $t_{AHT}$   | Address Hold Time From CE# or OE# high during toggle bit polling | Min | 0             |     | ns      |
| $t_{DVWH}$  | $t_{DS}$    | Data Setup Time  | Min | 35            |     | ns      |
| $t_{WHDX}$  | $t_{DH}$    | Data Hold Time   | Min | 0             |     | ns      |
|             | $t_{CEPH}$  | CE# High during toggle bit polling                               | Min | 20            |     | ns      |
|             | $t_{OEPH}$  | OE# High during toggle bit polling                               | Min | 20            |     | ns      |
| $t_{GHWL}$  | $t_{GHWL}$  | Read Recovery Time Before Write (OE# High to WE# Low)            | Min | 0             |     | ns      |
| $t_{ELWL}$  | $t_{CS}$    | CE# Setup Time   | Min | 0             |     | ns      |
| $t_{WHEH}$  | $t_{CH}$    | CE# Hold Time  | Min | 0             |     | ns      |
| $t_{WLWH}$  | $t_{WP}$    | Write Pulse Width  | Min | 35            |     | ns      |
| $t_{WHDL}$  | $t_{WPH}$   | Write Pulse Width High   | Min | 30            |     | ns      |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Note 2, 3)                       | Typ | 240           |     | $\mu$ s |
|             |             | Single Word Program Operation (Note 2)                           | Typ | 60            |     |         |
|             |             | Accelerated Single Word Program Operation (Note 2)               | Typ | 54            |     |         |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2)                                  | Typ | 0.5           |     | sec     |
|             | $t_{VHH}$   | $V_{HH}$ Rise and Fall Time (Note 1)                             | Min | 250           |     | ns      |
|             | $t_{VCS}$   | $V_{CC}$ Setup Time (Note 1)                                     | Min | 50            |     | $\mu$ s |
|             | $t_{BUSY}$  | WE# High to RY/BY# Low   | Max | 90            | 100 | ns      |
|             | $t_{POLL}$  | Program Valid before Status Polling                              | Max | 4             |     | $\mu$ s |

**Notes**

1. Not 100% tested.
2. See [Erase And Programming Performance on page 87](#) for more information
3. For 1–16 words/1–32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. If a program suspend command is issued within  $t_{POLL}$ , the device requires  $t_{POLL}$  before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after  $t_{POLL}$ , status data is available immediately after programming resumes. See [Figure 16.5 on page 79](#)

Figure 16.5 Program Operation Timings



Notes

1. PA = program address, PD = program data,  $D_{OUT}$  is the true data at the program address.
2. Illustration shows device in word mode.

Figure 16.6 Accelerated Program Timing Diagram

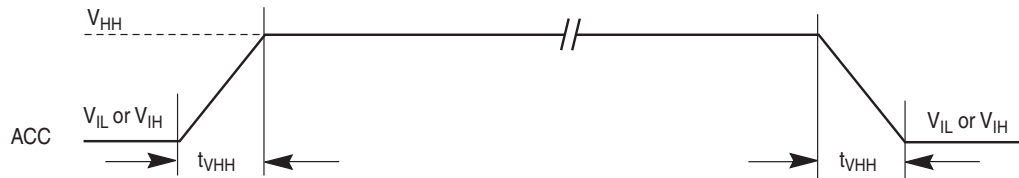
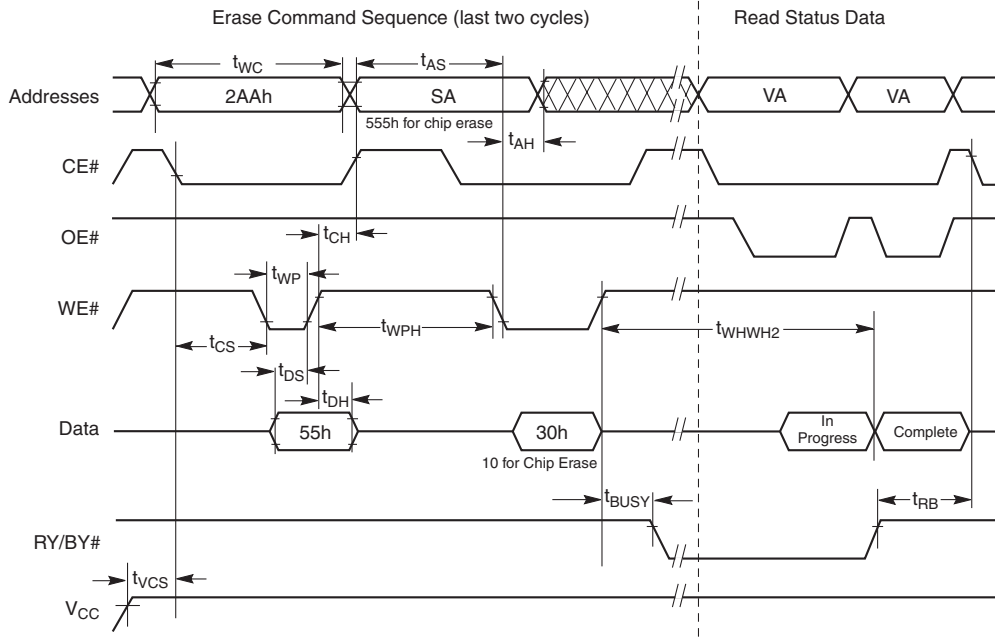


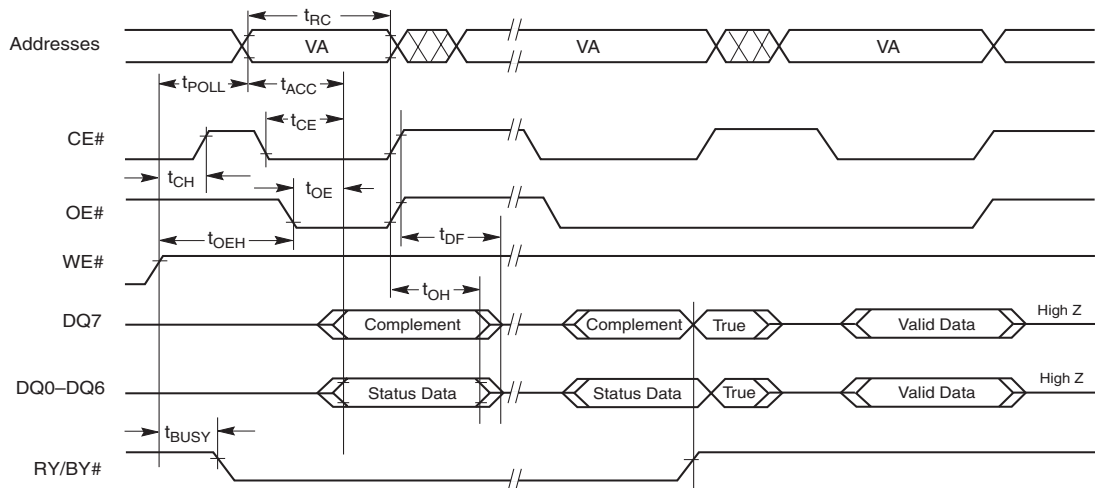
Figure 16.7 Chip/Sector Erase Operation Timings



**Notes**

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see [Write Operation Status on page 63.](#))
2. Illustration shows device in word mode.

Figure 16.8 Data# Polling Timings (During Embedded Algorithms)

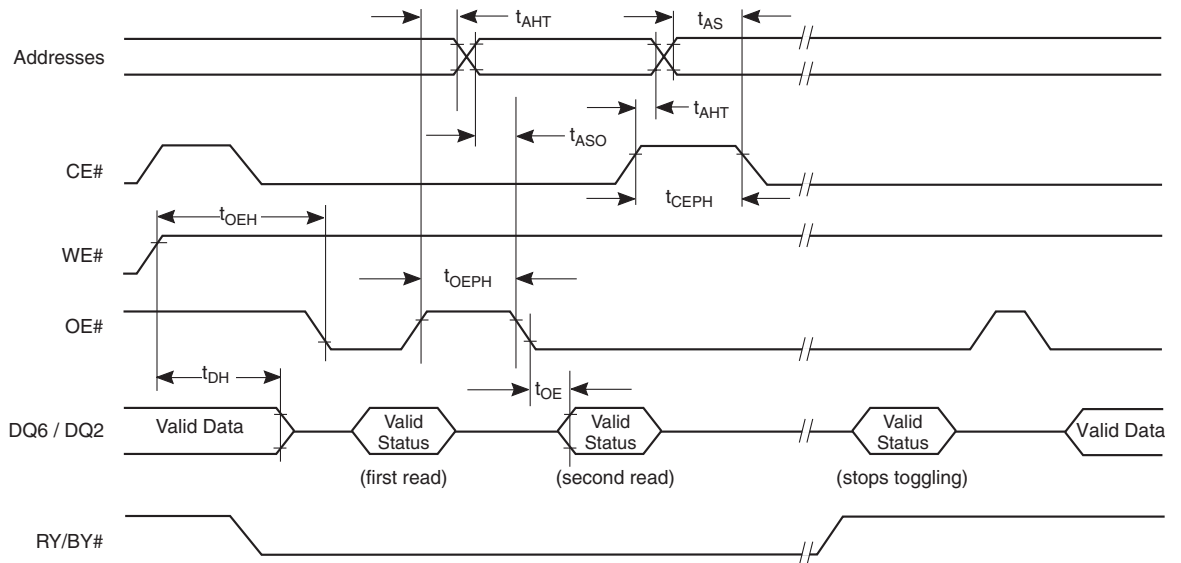


**Note**

VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.



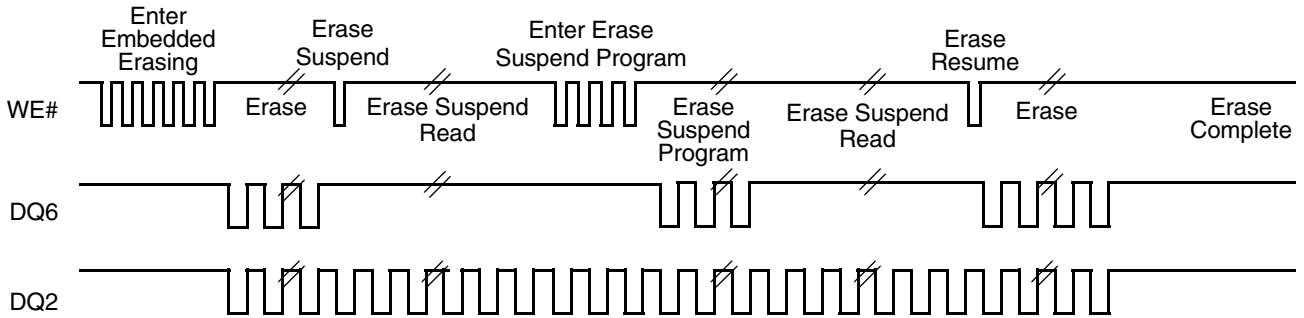
Figure 16.9 Toggle Bit Timings (During Embedded Algorithms)



**Note**

VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 16.10 DQ2 vs. DQ6



**Note**

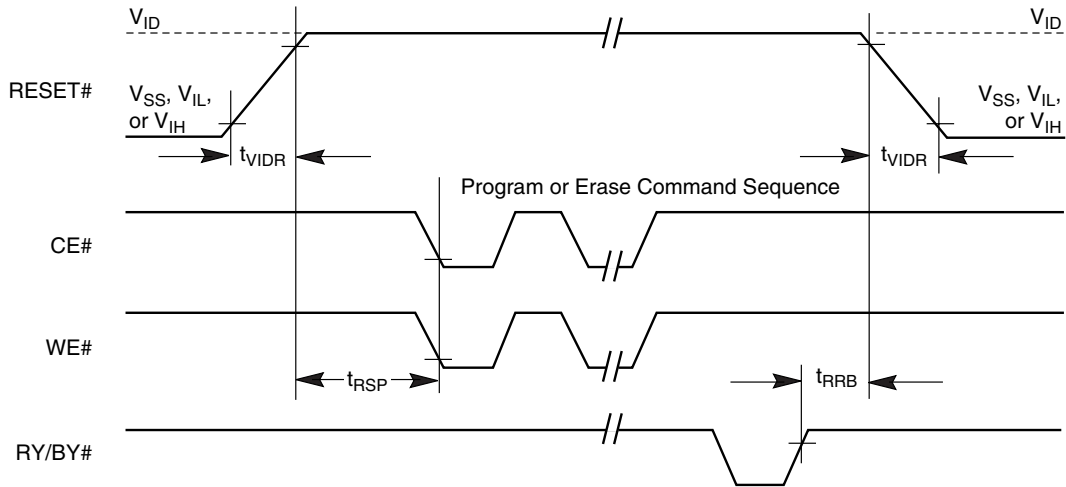
DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

**Table 16.8** Temporary Sector Unprotect

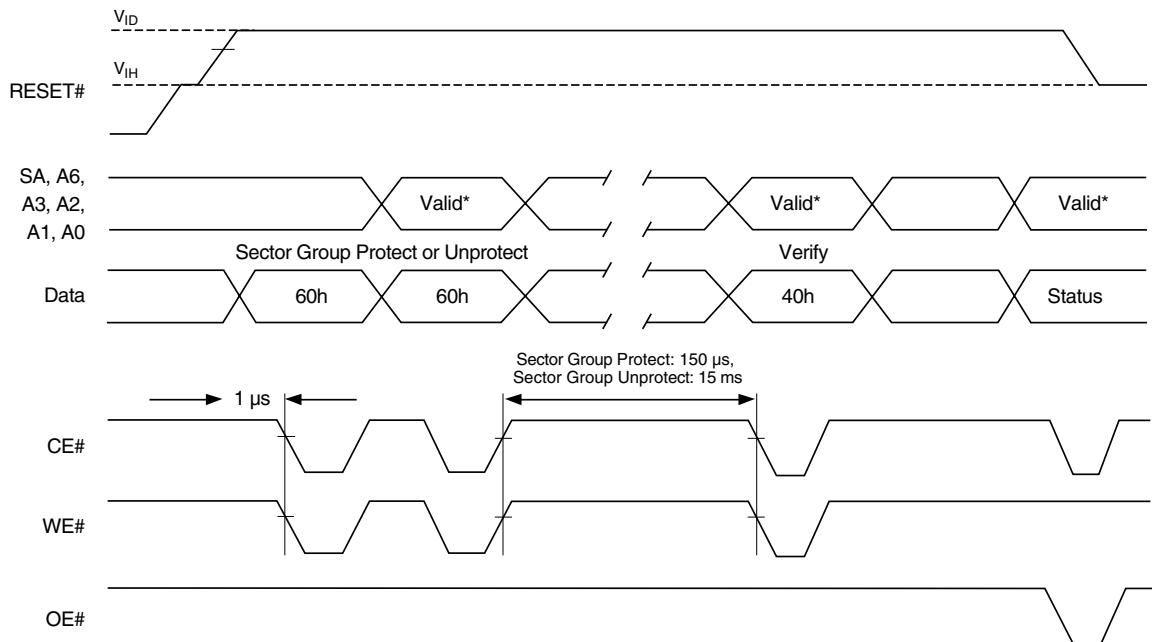
| Parameter |            | Description                                      |     | All Speed Options | Unit    |
|-----------|------------|--|-----|-------------------|---------|
| JEDEC     | Std        |  |     |                   |         |
|           | $t_{VIDR}$ | $V_{ID}$ Rise and Fall Time (See Note)           | Min | 500               | ns      |
|           | $t_{RSP}$  | RESET# Setup Time for Temporary Sector Unprotect | Min | 4                 | $\mu$ s |

**Note**  
Not 100% tested.

**Figure 16.11** Temporary Sector Group Unprotect Timing Diagram



**Figure 16.12** Sector Group Protect and Unprotect Timing Diagram



**Note**  
For sector group protect, A6:A0 = 0xx0010. For sector group unprotect, A6:A0 = 1xx0010.

Table 16.9 Alternate CE# Controlled Erase and Program Operations-S29GL064A

| Parameter   |             | Description   | Speed Options |     |     | Unit |         |
|-------------|-------------|---|---------------|-----|-----|------|---------|
| JEDEC       | Std.        |   | 90            | 10  | 11  |      |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)                             | Min           | 90  | 100 | 110  | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time                                    | Min           | 0   |     |      | ns      |
| $t_{ELAX}$  | $t_{AH}$    | Address Hold Time                                     | Min           | 45  |     |      | ns      |
| $t_{DVEH}$  | $t_{DS}$    | Data Setup Time                                       | Min           | 35  |     |      | ns      |
| $t_{EHDX}$  | $t_{DH}$    | Data Hold Time  | Min           | 0   |     |      | ns      |
| $t_{GHLE}$  | $t_{GHLE}$  | Read Recovery Time Before Write (OE# High to WE# Low) | Min           | 0   |     |      | ns      |
| $t_{WLEL}$  | $t_{WS}$    | WE# Setup Time  | Min           | 0   |     |      | ns      |
| $t_{EHWL}$  | $t_{WH}$    | WE# Hold Time   | Min           | 0   |     |      | ns      |
| $t_{ELEH}$  | $t_{CP}$    | CE# Pulse Width                                       | Min           | 35  |     |      | ns      |
| $t_{EHEL}$  | $t_{CPH}$   | CE# Pulse Width High                                  | Min           | 25  |     |      | ns      |
| $t_{WVWH1}$ | $t_{WVWH1}$ | Write Buffer Program Operation (Notes 2, 3)           | Typ           | 240 |     |      | $\mu$ s |
|             |             | Single Word Program Operation (Note 2)                | Typ           | 60  |     |      |         |
|             |             | Accelerated Single Word Program Operation (Note 2)    | Typ           | 54  |     |      |         |
| $t_{WVWH2}$ | $t_{WVWH2}$ | Sector Erase Operation (Note 2)                       | Typ           | 0.5 |     |      | sec     |
|             | $t_{RH}$    | RESET# High Time Before Write                         | Min           | 50  |     |      | ns      |
|             | $t_{POLL}$  | Program Valid before Status Polling (Note 4)          | Max           | 4   |     |      | $\mu$ s |

**Notes**

1. Not 100% tested.
2. See [Erase And Programming Performance on page 87](#) for more information.
3. For 1–16 words/1–32 bytes programmed.
4. If a program suspend command is issued within  $t_{POLL}$ , the device requires  $t_{POLL}$  before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after  $t_{POLL}$ , status data is available immediately after programming resumes. See [Figure 16.13 on page 86](#).

**Table 16.10** Alternate CE# Controlled Erase and Program Operations-S29GL032A

| Parameter   |             | Description   |     | Speed Options |     |     | Unit    |
|-------------|-------------|---|-----|---------------|-----|-----|---------|
| JEDEC       | Std.        |   |     | 90            | 10  | 11  |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)                             | Min | 90            | 100 | 110 | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time                                    | Min | 0             |     |     | ns      |
| $t_{ELAX}$  | $t_{AH}$    | Address Hold Time                                     | Min | 45            |     |     | ns      |
| $t_{DVEH}$  | $t_{DS}$    | Data Setup Time                                       | Min | 35            |     |     | ns      |
| $t_{EHDX}$  | $t_{DH}$    | Data Hold Time  | Min | 0             |     |     | ns      |
| $t_{GHLEL}$ | $t_{GHLEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0             |     |     | ns      |
| $t_{WLEL}$  | $t_{WS}$    | WE# Setup Time  | Min | 0             |     |     | ns      |
| $t_{EHWH}$  | $t_{WH}$    | WE# Hold Time   | Min | 0             |     |     | ns      |
| $t_{ELEH}$  | $t_{CP}$    | CE# Pulse Width                                       | Min | 35            |     |     | ns      |
| $t_{EHLEL}$ | $t_{CPH}$   | CE# Pulse Width High                                  | Min | 25            |     |     | ns      |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3)           | Typ | 240           |     |     | $\mu$ s |
|             |             | Single Word Program Operation (Note 2)                | Typ | 60            |     |     |         |
|             |             | Accelerated Single Word Program Operation (Note 2)    | Typ | 54            |     |     |         |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2)                       | Typ | 0.5           |     |     | sec     |
|             | $t_{RH}$    | RESET# High Time Before Write                         | Min | 50            |     |     | ns      |
|             | $t_{POLL}$  | Program Valid before Status Polling (Note 4)          | Max | 4             |     |     | $\mu$ s |

**Notes**

1. Not 100% tested.
2. See [Erase And Programming Performance on page 87](#) for more information
3. For 1–16 words/1–32 bytes programmed.
4. If a program suspend command is issued within  $t_{POLL}$ , the device requires  $t_{POLL}$  before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after  $t_{POLL}$ , status data is available immediately after programming resumes. See [Figure 16.13 on page 86](#).

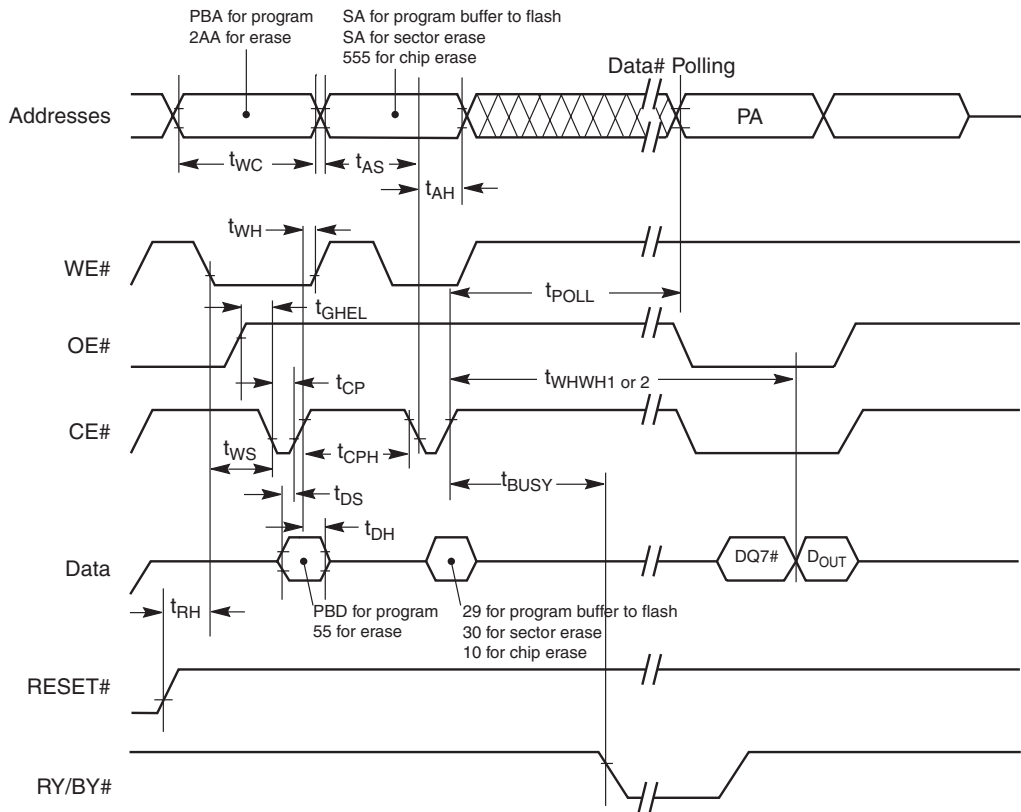
Table 16.11 Alternate CE# Controlled Erase and Program Operations-S29GL016A

| Parameter   |             | Description   |     | Speed Options |     | Unit    |
|-------------|-------------|---|-----|---------------|-----|---------|
| JEDEC       | Std.        |   |     | 90            | 10  |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)                             | Min | 90            | 100 | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time                                    | Min | 0             |     | ns      |
| $t_{ELAX}$  | $t_{AH}$    | Address Hold Time                                     | Min | 45            |     | ns      |
| $t_{DVEH}$  | $t_{DS}$    | Data Setup Time                                       | Min | 35            |     | ns      |
| $t_{EHDX}$  | $t_{DH}$    | Data Hold Time  | Min | 0             |     | ns      |
| $t_{GHLEL}$ | $t_{GHLEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0             |     | ns      |
| $t_{WLEL}$  | $t_{WS}$    | WE# Setup Time  | Min | 0             |     | ns      |
| $t_{EHWH}$  | $t_{WH}$    | WE# Hold Time   | Min | 0             |     | ns      |
| $t_{ELEH}$  | $t_{CP}$    | CE# Pulse Width                                       | Min | 35            |     | ns      |
| $t_{EHLEL}$ | $t_{CPH}$   | CE# Pulse Width High                                  | Min | 25            |     | ns      |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3)           | Typ | 240           |     | $\mu$ s |
|             |             | Single Word Program Operation (Note 2)                | Typ | 60            |     |         |
|             |             | Accelerated Single Word Program Operation (Note 2)    | Typ | 54            |     |         |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2)                       | Typ | 0.5           |     | sec     |
|             | $t_{RH}$    | RESET# High Time Before Write                         | Min | 50            |     | ns      |
|             | $t_{POLL}$  | Program Valid before Status Polling (Note 4)          | Max | 4             |     | $\mu$ s |

**Notes**

1. Not 100% tested.
2. See [Erase And Programming Performance on page 87](#) for more information
3. For 1–16 words/1–32 bytes programmed.
4. If a program suspend command is issued within  $t_{POLL}$ , the device requires  $t_{POLL}$  before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after  $t_{POLL}$ , status data is available immediately after programming resumes. See [Figure 16.13 on page 86](#)

**Figure 16.13** Alternate CE# Controlled Write (Erase/Program) Operation Timings



**Notes**

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3.  $DQ7\#$  is the complement of the data written to the device.  $D_{OUT}$  is the data written to the device.
4. Illustration shows device in word mode

## 17. Erase And Programming Performance

| Parameter  |           | Typ (Note 1) | Max (Note 2) | Unit    | Comments   |
|--|-----------|--------------|--------------|---------|--|
| Sector Erase Time  |           | 0.5          | 3.5          | sec     | Excludes 00h programming prior to erasure (Note 6) |
| Chip Erase Time  | S29GL016A | 17.5         | 35           |         |  |
|  | S29GL032A | 32           | 64           |         |  |
|  | S29GL064A | 64           | 128          |         |  |
| Total Write Buffer Program Time (Notes 3, 5)                       |           | 240          |              | $\mu$ s | Excludes system level overhead (Note 7)            |
| Total Accelerated Effective Write Buffer Program Time (Notes 4, 5) |           | 200          |              |         |  |
| Chip Program Time  | S29GL016A | 16           |              | sec     |  |
|  | S29GL032A | 31.5         |              |         |  |
|  | S29GL064A | 63           |              |         |  |

### Notes

1. Typical program and erase times assume the following conditions: 25°C,  $V_{CC} = 3.0V$ , 10,000 cycles; checkerboard data pattern.
2. Under worst case conditions of 90°C; Worst case  $V_{CC}$ , 100,000 cycles.
3. Effective programming time (typ) is 15  $\mu$ s (per word), 7.5  $\mu$ s (per byte).
4. Effective accelerated programming time (typ) is 12.5  $\mu$ s (per word), 6.3  $\mu$ s (per byte).
5. Effective write buffer specification is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.
6. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
7. System-level overhead is the time required to execute the command sequence(s) for the program command. See [Table 10.2 on page 61](#) and [Table 10.1 on page 62](#) for further information on command definitions.

**Table 17.1** TSOP Pin and BGA Package Capacitance

| Parameter Symbol | Parameter Description   | Test Setup    |      | Typ | Max | Unit |
|------------------|-------------------------|---------------|------|-----|-----|------|
| $C_{IN}$         | Input Capacitance       | $V_{IN} = 0$  | TSOP | 6   | 7.5 | pF   |
|                  |                         |               | BGA  | 4.2 | 5.0 | pF   |
| $C_{OUT}$        | Output Capacitance      | $V_{OUT} = 0$ | TSOP | 8.5 | 12  | pF   |
|                  |                         |               | BGA  | 5.4 | 6.5 | pF   |
| $C_{IN2}$        | Control Pin Capacitance | $V_{IN} = 0$  | TSOP | 7.5 | 9   | pF   |
|                  |                         |               | BGA  | 3.9 | 4.7 | pF   |

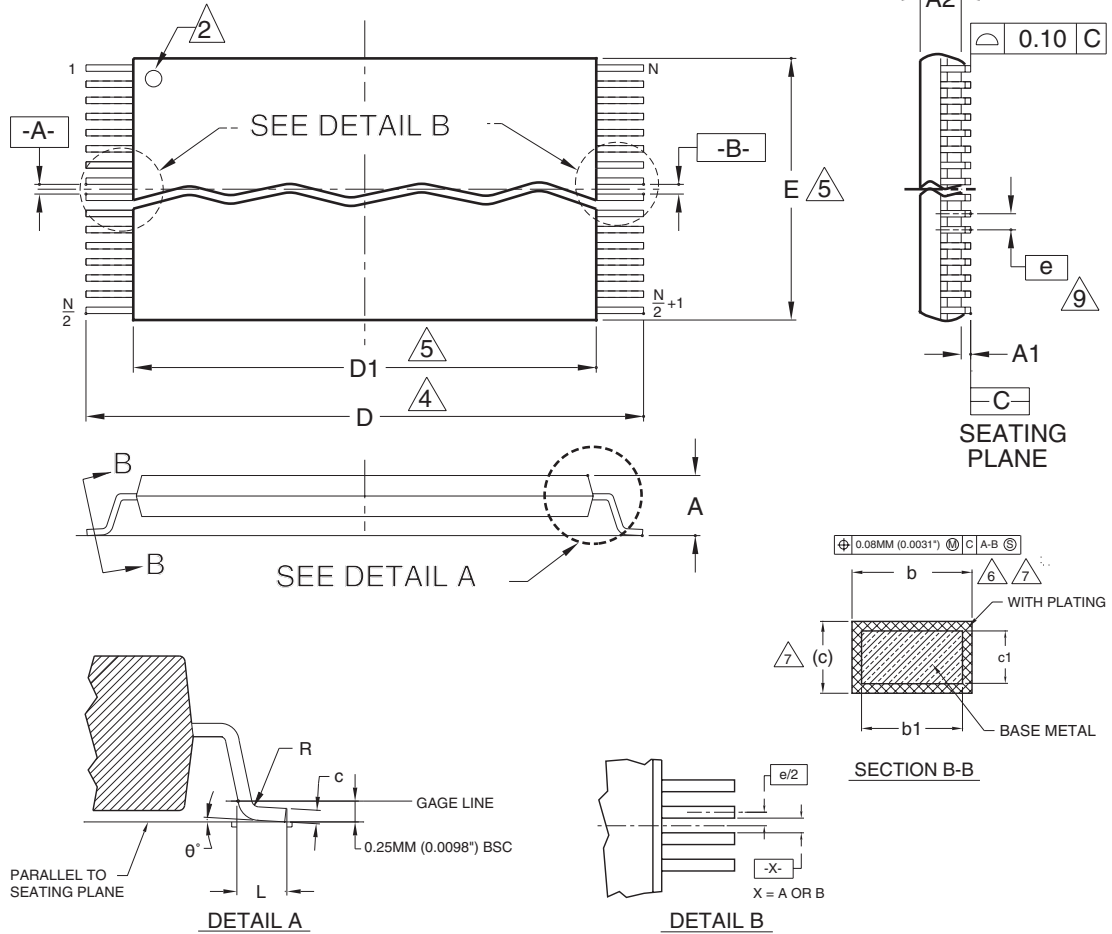
### Notes

1. Sampled, not 100% tested.
2. Test conditions  $T_A = 25^\circ C$ ,  $f = 1.0$  MHz.

## 18. Physical Dimensions

### 18.1 TS048—48-Pin Standard Thin Small Outline Package (TSOP)

STANDARD PIN OUT (TOP VIEW)



| Package | TS 048        |       |       |
|---------|---------------|-------|-------|
| Jedec   | MO-142 (B) EC |       |       |
| Symbol  | MIN           | NOM   | MAX   |
| A       | —             | —     | 1.20  |
| A1      | 0.05          | —     | 0.15  |
| A2      | 0.95          | 1.00  | 1.05  |
| b1      | 0.17          | 0.20  | 0.23  |
| b       | 0.17          | 0.22  | 0.27  |
| c1      | 0.10          | —     | 0.16  |
| c       | 0.10          | —     | 0.21  |
| D       | 19.80         | 20.00 | 20.20 |
| D1      | 18.30         | 18.40 | 18.50 |
| E       | 11.90         | 12.00 | 12.10 |
| e       | 0.50 BASIC    |       |       |
| L       | 0.50          | 0.60  | 0.70  |
| 0       | 0°            | 3°    | 5°    |
| R       | 0.08          | —     | 0.20  |
| N       | 48            |       |       |

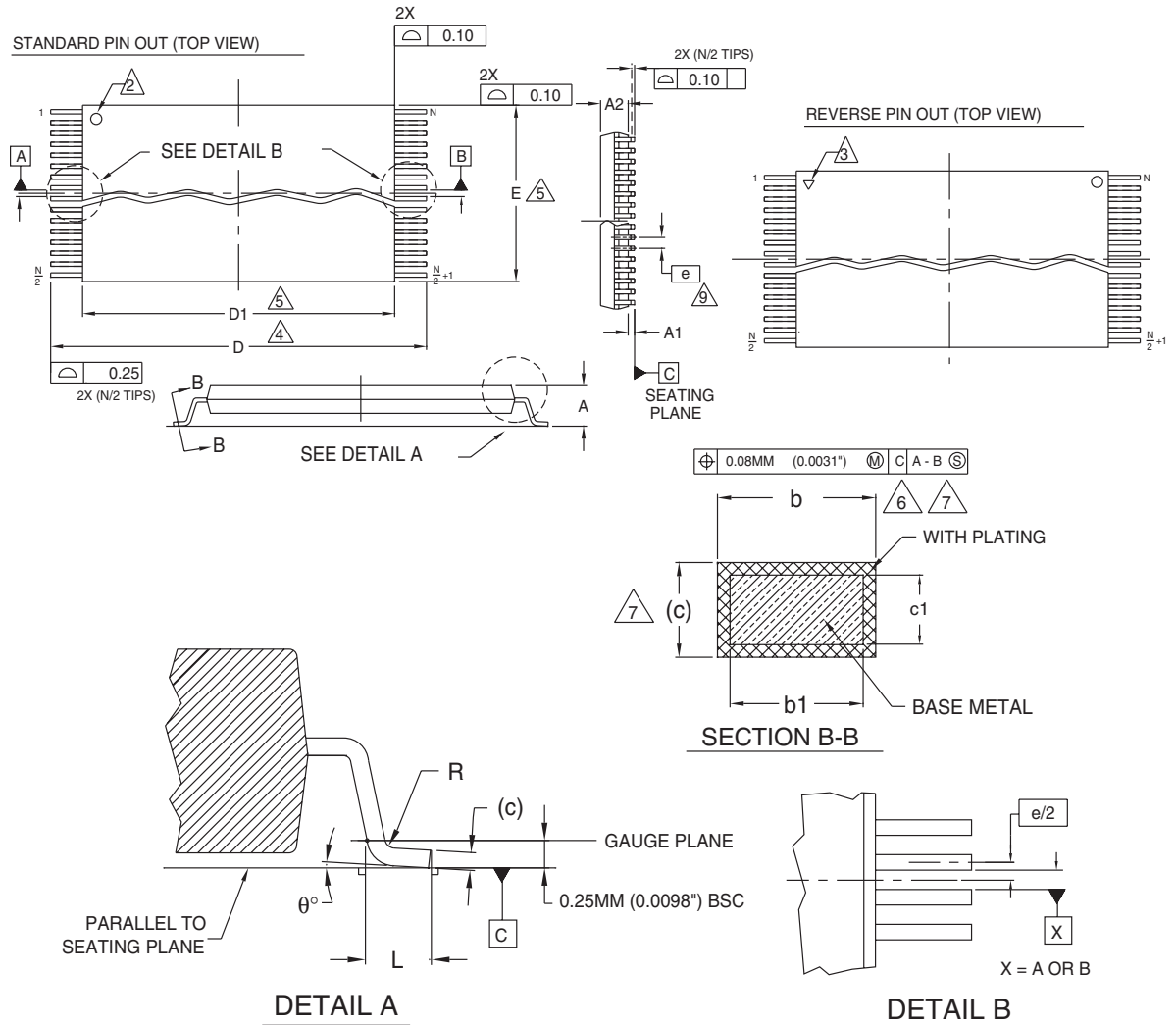
NOTES:

- ① CONTROLLING DIMENSIONS ARE IN MILLIMETERS (MM). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
- ② PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
- ③ NOT APPLICABLE.
- ④ TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
- ⑤ DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15MM (.0059") PER SIDE.
- ⑥ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
- ⑦ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
- ⑧ LEAD COPLANARITY SHALL BE WITHIN 0.10MM (0.004") AS MEASURED FROM THE SEATING PLANE.
- ⑨ DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

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## 18.2 TS056—56-Pin Standard Thin Small Outline Package (TSOP)



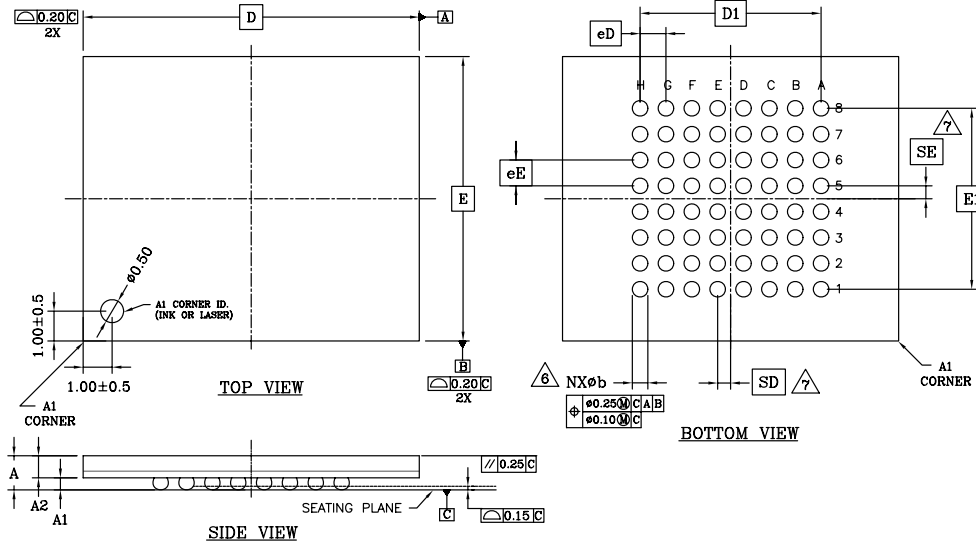
| Package  | TS 056        |       |       |
|----------|---------------|-------|-------|
| Jedec    | MO-142 (D) EC |       |       |
| Symbol   | MIN           | NOM   | MAX   |
| A        | —             | —     | 1.20  |
| A1       | 0.05          | —     | 0.15  |
| A2       | 0.95          | 1.00  | 1.05  |
| b1       | 0.17          | 0.20  | 0.23  |
| b        | 0.17          | 0.22  | 0.27  |
| c1       | 0.10          | —     | 0.16  |
| c        | 0.10          | —     | 0.21  |
| D        | 19.80         | 20.00 | 20.20 |
| D1       | 18.30         | 18.40 | 18.50 |
| E        | 13.90         | 14.00 | 14.10 |
| e        | 0.50 BASIC    |       |       |
| L        | 0.50          | 0.60  | 0.70  |
| $\theta$ | 0°            | —     | 8°    |
| R        | 0.08          | —     | 0.20  |
| N        | 56            |       |       |

NOTES:

- 1 CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
- 2 PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
- 3 PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
- 4 TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
- 5 DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15mm (.0059") PER SIDE.
- 6 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
- 7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
- 8 LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
- 9 DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

3356 \ 16-038.10c

### 18.3 LAA064—64-Ball Fortified Ball Grid Array (BGA)

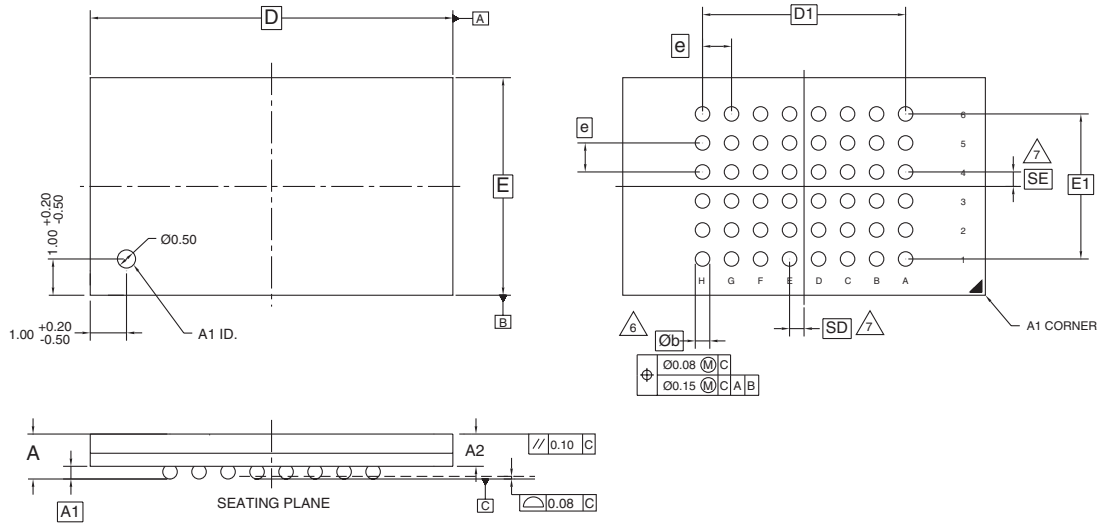


| PACKAGE | LAA 064                |      |      |                          |
|---------|------------------------|------|------|--------------------------|
| JEDEC   | N/A                    |      |      |                          |
|         | 13.00x11.00 mm PACKAGE |      |      |                          |
| SYMBOL  | MIN.                   | NOM. | MAX. | NOTE                     |
| A       | —                      | —    | 1.40 | PROFILE HEIGHT           |
| A1      | 0.40                   | —    | —    | STANDOFF                 |
| A2      | 0.60                   | —    | —    | BODY THICKNESS           |
| D       | 13.00 BSC.             |      |      | BODY SIZE                |
| E       | 11.00 BSC.             |      |      | BODY SIZE                |
| D1      | 7.00 BSC.              |      |      | MATRIX FOOTPRINT         |
| E1      | 7.00 BSC.              |      |      | MATRIX FOOTPRINT         |
| MD      | 8                      |      |      | MATRIX SIZE D DIRECTION  |
| ME      | 8                      |      |      | MATRIX SIZE E DIRECTION  |
| N       | 64                     |      |      | BALL COUNT               |
| φb      | 0.50                   | 0.60 | 0.70 | BALL DIAMETER            |
| φD      | 1.00 BSC.              |      |      | BALL PITCH - D DIRECTION |
| φE      | 1.00 BSC.              |      |      | BALL PITCH - E DIRECTION |
| SD/SE   | 0.50 BSC.              |      |      | SOLDER BALL PLACEMENT    |
|         | A1-AB, K1-K8           |      |      | DEPOPULATED SOLDER BALLS |

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994 .
- ALL DIMENSIONS ARE IN MILLIMETERS .
- BALL POSITION DESIGNATION PER JEDEC 95-1, SPP-010 (EXCEPT AS NOTED).
- [C] REPRESENTS THE SOLDER BALL GRID PITCH .
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- △b DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM "C".
- △SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

### 18.4 VBN048—48-Ball Fine-pitch Ball Grid Array (BGA) 10x 6 mm Package



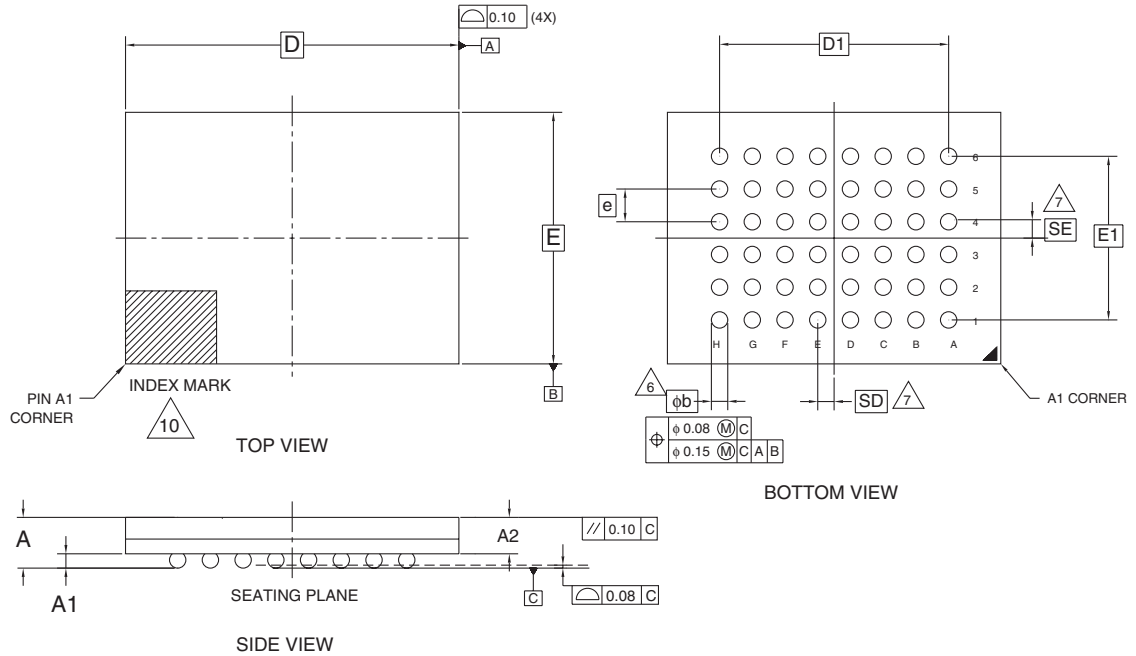
|         |                                |     |      |                             |
|---------|--------------------------------|-----|------|-----------------------------|
| PACKAGE | VBN 048                        |     |      |                             |
| JEDEC   | N/A                            |     |      |                             |
|         | 10.00 mm x 6.00 mm NOM PACKAGE |     |      |                             |
| SYMBOL  | MIN                            | NOM | MAX  | NOTE                        |
| A       | ---                            | --- | 1.00 | OVERALL THICKNESS           |
| A1      | 0.17                           | --- | ---  | BALL HEIGHT                 |
| A2      | 0.62                           | --- | 0.73 | BODY THICKNESS              |
| D       | 10.00 BSC.                     |     |      | BODY SIZE                   |
| E       | 6.00 BSC.                      |     |      | BODY SIZE                   |
| D1      | 5.60 BSC.                      |     |      | BALL FOOTPRINT              |
| E1      | 4.00 BSC.                      |     |      | BALL FOOTPRINT              |
| MD      | 8                              |     |      | ROW MATRIX SIZE D DIRECTION |
| ME      | 6                              |     |      | ROW MATRIX SIZE E DIRECTION |
| N       | 48                             |     |      | TOTAL BALL COUNT            |
| phi b   | 0.35                           | --- | 0.45 | BALL DIAMETER               |
| e       | 0.80 BSC.                      |     |      | BALL PITCH                  |
| SD / SE | 0.40 BSC.                      |     |      | SOLDER BALL PLACEMENT       |
|         | NONE                           |     |      | DEPOPULATED SOLDER BALLS    |

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE TOTAL NUMBER OF SOLDER BALLS.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- NOT USED.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3425/16-038.25

### 18.5 VBK048—Ball Fine-pitch Ball Grid Array (BGA) 8.15x 6.15 mm Package



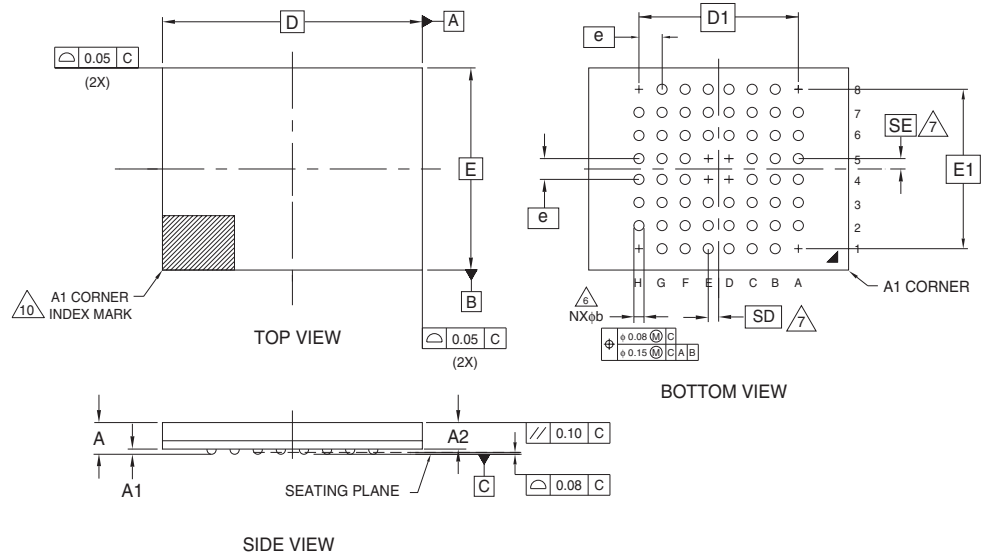
| PACKAGE | VBK 048                       |     |      | NOTE                        |
|---------|-------------------------------|-----|------|-----------------------------|
| JEDEC   | N/A                           |     |      |                             |
|         | 8.15 mm x 6.15 mm NOM PACKAGE |     |      |                             |
| SYMBOL  | MIN                           | NOM | MAX  |                             |
| A       | ---                           | --- | 1.00 | OVERALL THICKNESS           |
| A1      | 0.18                          | --- | ---  | BALL HEIGHT                 |
| A2      | 0.62                          | --- | 0.76 | BODY THICKNESS              |
| D       | 8.15 BSC.                     |     |      | BODY SIZE                   |
| E       | 6.15 BSC.                     |     |      | BODY SIZE                   |
| D1      | 5.60 BSC.                     |     |      | BALL FOOTPRINT              |
| E1      | 4.00 BSC.                     |     |      | BALL FOOTPRINT              |
| MD      | 8                             |     |      | ROW MATRIX SIZE D DIRECTION |
| ME      | 6                             |     |      | ROW MATRIX SIZE E DIRECTION |
| N       | 48                            |     |      | TOTAL BALL COUNT            |
| φb      | 0.35                          | --- | 0.43 | BALL DIAMETER               |
| e       | 0.80 BSC.                     |     |      | BALL PITCH                  |
| SD / SE | 0.40 BSC.                     |     |      | SOLDER BALL PLACEMENT       |
|         | ---                           |     |      | DEPOPULATED SOLDER BALLS    |

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
- e REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE TOTAL NUMBER OF SOLDER BALLS.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\frac{e}{2}$
- NOT USED.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3338 \ 16-038.25 \ 10.05.04

### 18.6 VBU056—Ball Fine-pitch Ball Grid Array (BGA) 9 x 7 mm Package



| PACKAGE | VBU 056                       |      |      |                             |
|---------|-------------------------------|------|------|-----------------------------|
| JEDEC   | N/A                           |      |      |                             |
|         | 9.00 mm x 7.00 mm NOM PACKAGE |      |      |                             |
| SYMBOL  | MIN                           | NOM  | MAX  | NOTE                        |
| A       | ---                           | ---  | 1.00 | OVERALL THICKNESS           |
| A1      | 0.17                          | ---  | ---  | BALL HEIGHT                 |
| A2      | 0.62                          | ---  | 0.76 | BODY THICKNESS              |
| D       | 9.00 BSC.                     |      |      | BODY SIZE                   |
| E       | 7.00 BSC.                     |      |      | BODY SIZE                   |
| D1      | 5.60 BSC.                     |      |      | BALL FOOTPRINT              |
| E1      | 5.60 BSC.                     |      |      | BALL FOOTPRINT              |
| MD      | 8                             |      |      | ROW MATRIX SIZE D DIRECTION |
| ME      | 8                             |      |      | ROW MATRIX SIZE E DIRECTION |
| N       | 56                            |      |      | TOTAL BALL COUNT            |
| φb      | 0.35                          | 0.40 | 0.45 | BALL DIAMETER               |
| e       | 0.80 BSC.                     |      |      | BALL PITCH                  |
| SD / SE | 0.40 BSC.                     |      |      | SOLDER BALL PLACEMENT       |
|         | A1,A8,D4,D5,E4,E5,H1,H8       |      |      | DEPOPULATED SOLDER BALLS    |

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
- e REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE TOTAL NUMBER OF SOLDER BALLS.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE =  $\lfloor \frac{e}{2} \rfloor$ .  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\lfloor \frac{e}{2} \rfloor$ .
- NOT USED.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3440: 16-038.25 \ 01.13.05

## 19. Revision History

| Section                                    | Description  |
|--|--|
| <b>Revision A (October 13, 2004)</b>       |  |
| Global                                     | Initial Release.   |
| <b>Revision A1 (December 17, 2004)</b>     |  |
| Secured Silicon Sector Flash Memory Region | Updated Secured Silicon Sector address table with addresses in x8-mode.  |
| DC Characteristics (CMOS Compatible)       | Re-specified $I_{LIT}$ over temperature. Corrected WP#/ACC input load current footnote.  |
| <b>Revision A2 (January 28, 2005)</b>      |  |
| Global                                     | Added S29GL032A information.   |
| <b>Revision A3 (April 22, 2005)</b>        |  |
| Global                                     | Added S29GL016A information.   |
| Table 7.12                                 | Corrected Secured Silicon Sector Indicator Bit.  |
| <b>Revision A4 (July 29, 2005)</b>         |  |
| Global                                     | Corrected S29GL032A fine-pitch BGA package description from VBN048 to VBK048.<br>Corrected S29GL016A information in Tables 15 and 17.<br>Updated Ordering Information and Valid Combinations for S29GL016A, S29GL032A, and S29GL064A. Added requirements for MCP Cellular Handsets.<br>Added VBU056 Connection Diagram and VBU056 Package Dimension drawings |
| <b>Revision A5 (January 11, 2006)</b>      |  |
| Global                                     | Added model numbers 01 and 02 to ordering information section and autoselect codes table.<br>Corrected sector address bit range in S29GL064A table for models R3, W3 and table for models R4 and W4.<br>Replaced model numbers W1, W2 with W3, W4 in DQ7 to DQ0 section of sector address table.   |
| <b>Revision A6 (June 5, 2006)</b>          |  |
| Global                                     | Removed the 64 Mb MCP-compatible devices.<br>Removed the 32 Mb single-bank products in the MCP-compatible package.   |
| <b>Revision A7 (January 22, 2007)</b>      |  |
| AC Characteristics                         | <i>Erase and Program Operations table</i> : Changed $t_{BUSY}$ to a maximum specification.   |
| <b>Revision A8 (January 29, 2007)</b>      |  |
| Global                                     | Deleted Preliminary designation from document.   |
| <b>Revision A9 (March 23, 2007)</b>        |  |
| Connection Diagrams                        | Clarified notes for LAA064 package.  |
| Sector Address Tables                      | Corrected page breaks in tables.   |
| <b>Revision A10 (August 6, 2007)</b>       |  |
| Device Geometry Definition Table           | Corrected CFI values in Erase Block Region 1 & 2   |
| <b>Revision A11 (September 10, 2007)</b>   |  |
| Cover page and first page                  | GL032A is now included as EOD, in addition to GL064A.  |
| Device Geometry Definition Table           | Corrected CFI values in Erase Block Region 2   |
| <b>Revision A12 (May 21, 2008)</b>         |  |
| Cover page and Features page               | Updated product status to retired  |

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