THIS SPEC IS OBSOLETE

Spec No: 002-02760

Spec Title: S4041-1B1 8 GB / 16 GB, 3.0 V E.MMC FLASH

Replaced by: None

S4041-1B1

8 GB / 16 GB, 3.0 V e.MMC Flash

Features

- e.MMC 4.51 Specification compatible
  - Backward compatible with previous e.MMC specifications
- Storage temperature
  - –40 °C to +85 °C
- Operating voltage
  - V_{CCQ}: 1.7 V - 1.95 V or 2.7 V - 3.6 V
  - V_{CC}: 2.7 V - 3.6 V
- Density: 8/16 GB of data storage
- Data bus width:
  - SDR mode: 1 bit, 4 bit, 8 bit
  - DDR mode: 4 bit, 8 bit
  - HS200 mode: 4 bit, 8 bit
- Clock frequency: 52 MHz, 200 MHz (e.MMC 4.51)
  - SDR mode: up to 52 MHz
  - DDR mode: up to 52 MHz
  - HS200 mode: up to 200 MHz
- BGA packages
  - 153-ball VFBGA: 13 mm × 11.5 mm × 1.0 mm
  - 100-ball LBGA: 18 mm × 14 mm × 1.4 mm
- Operating temperature range
  - Embedded: –25 °C to +85 °C
  - Industrial: –40 °C to +85 °C

Key Supported Features

- Boot Operation
- Partition Management
- Boot Area Partition
- Replay Protected Memory Block (RPMB)
- Sleep (CMD5)
- Sanitize
- Trim
- High Priority Interrupt
- Background Operations
- Auto Background Operations
- Hardware Reset
- HS200
- Health Monitoring

Performance

- Sequential Read (MB/s): 120
- Sequential Write (MB/s): 20
  - Based on 16-GB device
  - Bus in x8 I/O and HS200 modes
- Random Read (IOPS): 5000
- Random Write (IOPS): 1400

General Description

Cypress® e.MMC is a managed NAND memory solution designed for embedded applications. Cypress e.MMC includes a flash controller and a standard MLC NAND flash memory, and is compatible with the JEDEC JESD84-B451 with backwards compatibility to previous e.MMC specifications.

Designed for faster throughput and large data transfer, Cypress e.MMC offers high performance, great reliability, and minimal latency. In addition to higher performance, Cypress's e.MMC offers optimum power management features resulting in reduced power consumption, making it an ideal solution for mobile applications.

In addition, highly optimized Cypress firmware fully utilizes the MLC NAND capabilities leveraging wear-leveling, defect management, garbage collection, and ECC to enhance product life.

The Cypress e.MMC product family offers a vast array of the JEDEC e.MMC features including HS200, high priority interrupt (HPI), boot partitions, RPMB partitions, background operations, hardware reset, and power off notification.

Combined with an advanced e.MMC feature set and Cypress's commitment to quality, Cypress e.MMC is ideal for industrial applications as well as set top boxes, gaming consoles, and consumer electronic devices.

Cypress Product Offering

The Cypress e.MMC product offering includes: 8/16 GB in 153-FBGA (13 mm × 11.5 mm) and 100-BGA (18 mm × 14 mm) packages.

- 8 GB: S40410081
  - 153 VFBGA (13 × 11.5 × 1.0, 0.5 mm ball pitch)
  - 100 LBGA (18 × 14 × 1.4, 1.0 mm ball pitch)
- 16 GB: S40410161
  - 153 VFBGA (13 × 11.5 × 1.0, 0.5 mm ball pitch)
  - 100 LBGA (18 × 14 × 1.4, 1.0 mm ball pitch)

Contents

Package Configurations

Figure 1. FBGA 153 (Top View, Balls Down)

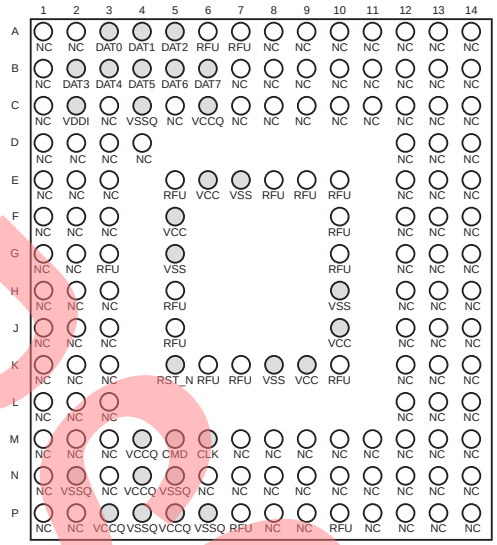


Figure 2. BGA 100 (Top View, Balls Down)

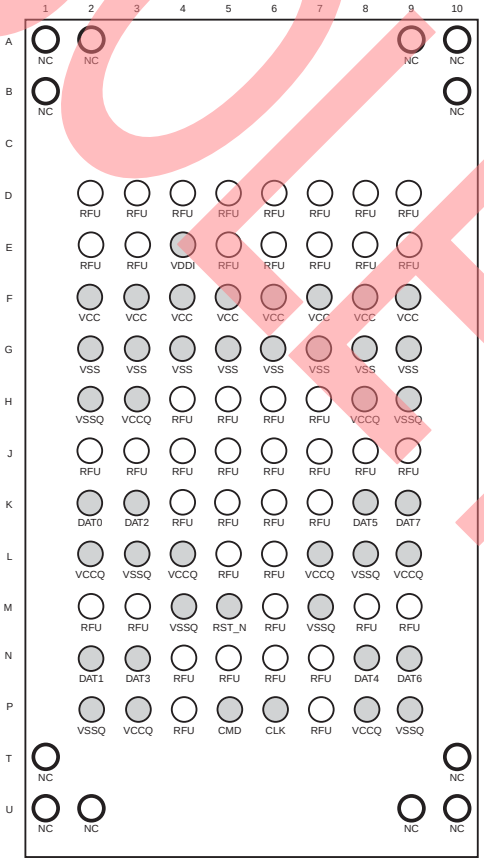


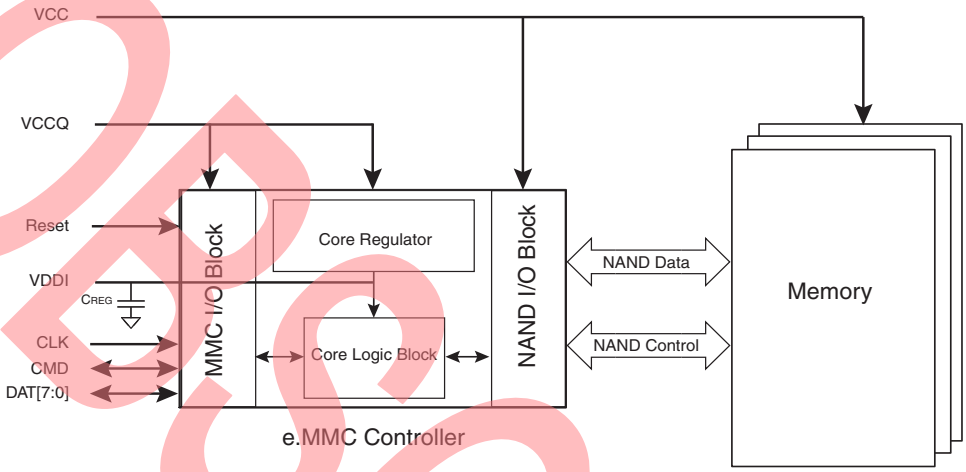
Table 1. Pin Description

Pin Name	Type	Description
DAT0 - DAT7	I/O	Bidirectional data channels used for data transfers
CMD	I/O	Bidirectional command channel used for device initialization and command transfers
CLK	Input	Clock input
RST_N	Input	Hardware reset
VCC	Power	Supply voltage for the flash memory
VCCQ	Power	Supply voltage for the memory controller and MMC interface
VDDI	Power	Internal power node. Connect capacitor to ground.
VSS	Power	Ground pin for the flash memory
VSSQ	Power	Ground pin for the memory controller and MMC interface
NC	—	Not connected
RFU	—	Reserved for future use. Do not connect.

Architecture

Cypress e.MMC is an embedded non-volatile storage solution with a MultiMediaCard (MMC) interface, a high performance memory controller, and state of the art flash memory all supported by Cypress optimized flash management software. Based on the JEDEC industry-standard MMC System Specification v4.51, the Cypress e.MMC product family is offered in standard JEDEC BGA packages. Figure 3 represents the basic block diagram of the Cypress e.MMC.

Figure 3. Cypress e.MMC Architecture



Key Supported e.MMC Features

Cypress e.MMC supports the JEDEC JESD84-B451 specification.

Boot Operation

Cypress e.MMC supports boot mode as well as alternate boot mode. Boot operations can be performed at high speed and dual data rate timings.

Figure 4. MultiMediaCard State Diagram (Boot Mode)

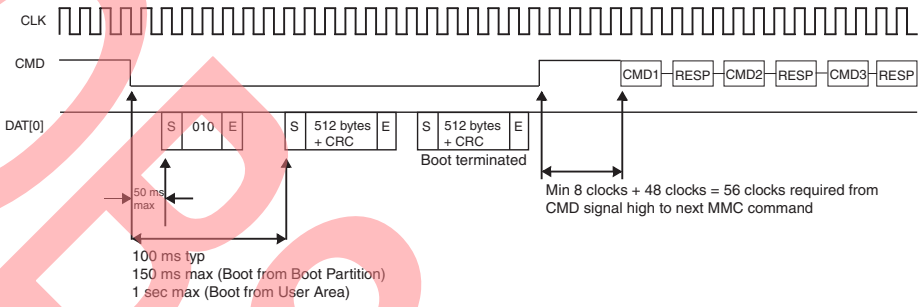
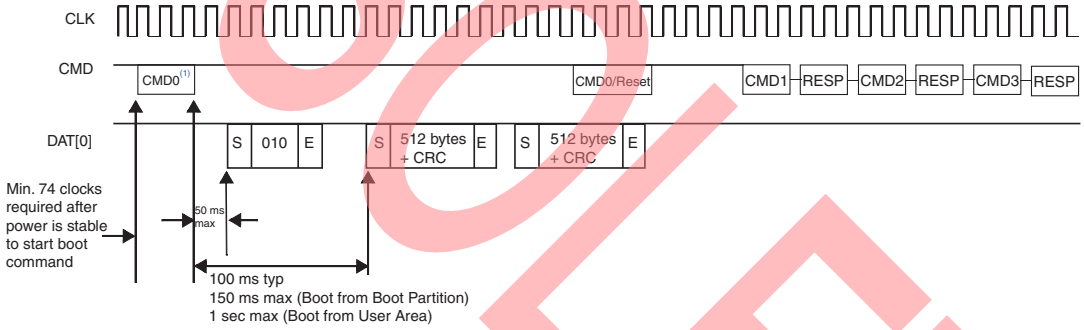


Figure 5. MultiMediaCard State Diagram (Alternative Boot Mode)[1]



Partition Management

e.MMC specifications allow for the device to have the following partitions: a User Data Area for general purpose storage, two boot partitions for storing boot images, and the Replay Protected Memory Block (RPMB) for data management in a replay protected and authenticated manner.

The Cypress e.MMC device can be configured as below:

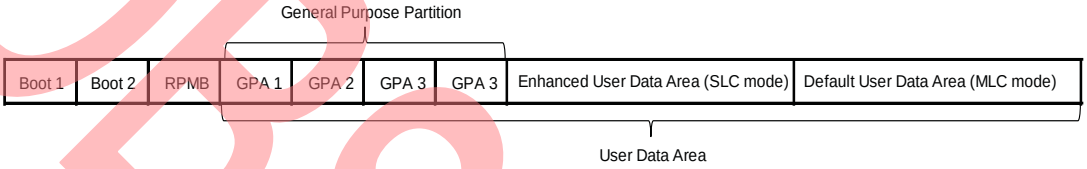
- Factory configuration supplies two boot partitions size of 4 MB each and one RPMB partition size of 4 MB. These partitions are configured in Enhanced (SLC) mode for higher reliability.
- The host can create up to four General Purpose Partitions within the User Data Area. These partitions can be configured in Enhanced (SLC) mode or Default (MLC) mode. The host will also need to configure the size of each partition. These attributes can be programmed by the host only once in the device life-cycle (one-time programmable).
- In addition to the General Purpose Partitions the host can also configure a segment of the User Data Area to be accessed in Enhanced (SLC) mode. The host will need to specify the starting location and size. These attributes can be programmed by the host only once in the device life-cycle (one-time programmable).

Note
1. CMD0 with argument 0xFFFFFFFA.

Table 2. Partition Type

Partition		NAND Mode
Boot Area 1		SLC Mode
Boot Area 2		SLC Mode
RPMB Area		SLC Mode
User Data Area	General Purpose Partition	MLC or SLC Mode
	Enhanced	SLC Mode
	Default	MLC Mode

Figure 6. Partitions



Sleep (CMD5)

Sleep/Awake (CMD5) is used to switch the device between Sleep and Standby mode. During the Sleep state, V_{CC} can be switched off for maximum power savings. While a device is in Sleep mode it can only respond to the Reset (CMD0) and Sleep/Awake (CMD5) commands.

High Priority Interrupt (HPI)

High Priority Interrupt (HPI) is intended to suspend an ongoing operation while allowing for a high priority read operation to be performed.

Background Operations

e.MMC devices are equipped with a Background Operations feature (see Table 7 on page 12). When enabled, Background Operations allow the e.MMC device to perform a number of routine data maintenance operations such as wear leveling, garbage collection, erase, and compaction while the host CPU is not being serviced.

Auto Background Operations

Auto Background Operations is a feature that allows the e.MMC device to fully manage background operations without any requirements from the Host. The e.MMC device will check if background operations are required at specified intervals and initiate background operations if needed. This frees the host from having to develop software to manage these maintenance tasks and ensure that the e.MMC device is operating at the optimum performance levels. Issuing any command while auto background operations are occurring will stop the current background operation activities. There will be a maximum latency of 40 ms if auto background operations are interrupted by any read or write command from the host.

This feature is enabled on default and can be configured through the CMD56 command. A separate application note is available with the full details of the CMD56 command. A non-disclosure agreement (NDA) is required to view this application note. Contact your nearest Cypress sales office for more information.

Trim

Similar to the Erase operation, the Trim function (Table 7 on page 12) performs a targeted erase on specific write blocks. Data that is no longer needed, designated by the host, will be erased during background erase events.

Sanitize

Sanitize (Table 7 on page 12) is intended for applications with high security requirements that can afford the performance impact. This command is used in conjunction with standard Erase or Trim operations and requires the device to physically remove data from the unmapped user address space. The busy line will be asserted once the Sanitize operations begin and will remain busy until the operation has been completed or interrupted.

Hardware Reset

Used by the host to reset the device, hardware reset moves the device into a pre-idle state and disables the power-on period write protection on blocks that were set at power-on as write protected.

Health Monitoring

Health Monitoring is a proprietary feature of the Cypress e.MMC product that provides useful information about the life span of the NAND flash component. The host can query for the device's health by using the CMD56 command to get information such as the number of bad blocks and the number of erase cycles for each block. EXT_CSD registers [269:254] also contain valuable device health information. A separate application note is available with the full details of the CMD56 command and EXT_CSD registers [269:254]. A non-disclosure agreement (NDA) is required to view this application note. Contact your nearest Cypress sales office for more information.

Field Firmware Update

Field Firmware Update is a feature that allows the host to upload a new version of the firmware to the e.MMC. This can be done by setting the device into FFU mode and performing writes with the arguments defined in the FFU_ARG register. A separate application note is available with the full details of this feature. A non-disclosure agreement (NDA) is required to view this application note. Contact your nearest Cypress sales office for more information.

Register Values

Operating Conditions Register

Operation Conditions Register (OCR) stores the e.MMC voltage profile. In addition, it contains the status bit (31) which is set when the device power up has been completed.

Table 3. OCR Register

Field Description	OCR Slice	Value
Reserved	[6:0]	00 00000b
V_{CCQ}: 1.7 - 1.95 range	[7]	Dual Voltage: 1b
V_{CCQ}: 2.0 - 2.6 range	[14:8]	000 0000b
V_{CCQ}: 2.7 - 3.6 range	[23:15]	1 1111 1111b
Reserved	[28:24]	0 0000b
Access Mode	[30:29]	Sector Mode: 10b
e.MMC power up status bit (busy)[2]	[31]	–

Card Identification Register

The Card Identification Register (CID) contains the card identification information used during the card identification phase.

Table 4. CID Register

Field Name	Field ID	Width	CID Slice	CID Value
Manufacturer ID	MID	8	[127:120]	01h
Card BGA	CBX	2	[113:112]	01b
OEM/Application ID	OID	8	[111:104]	00h
Product Name	PNM	48	[103:56]	See Product Table.
Product Revision[5]	PRV	8	[55:48]	–
Product Serial Number	PSN	32	[47:16]	32-bit unsigned binary integer assigned at random
Manufacturing Date[4]	MDT	8	[15:8]	–
CRC7 Checksum[4]	CRC	7	[7:1]	–
Not Used	—	1	[0]	Always 1

Product Table

Table 5. Product Table

Cypress Part Number	Density	Product Name in CID Register (PNM)
S40410081	8 GB	“S40408” – 533430343038h
S40410161	16 GB	“S40416” – 533430343136h

Notes
2. Reserved bits should be read at ‘0’.
3. R = Read only. R/W = One time programmable and readable. R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
4. V_{DD} represents the total consumed current for V_{CC} and V_{CCQ}.

Card Specific Data Register

Card Specific Data (CSD) Register contains the e.MMC access information. It includes data format, error correction, transfer speeds, and access times. It also includes information as to whether the DSR register can be accessed.

Table 6. CSD Register

Field Name	Field ID	Size (Bits)	Cell Type	CSD Slice	CSD Value
CSD Structure	CSD_STRUCTURE	2	R	[127:126]	3h
System Specification Version	SPEC_VERS	4	R	[125:122]	4h
Reserved[5]	—	2	R	[121:120]	—
Data Read Access Time 1	TAAC	8	R	[119:112]	4Fh
Data Read Access Time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	01h
Maximum Bus Clock Frequency	TRAN_SPEED	8	R	[103:96]	32h
Card Command Classes	CCC	12	R	[95:84]	0F5h
Maximum Read Block Length	READ_BL_LEN	4	R	[83:80]	9h
Partial Blocks For Read Allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write Block Misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read Block Misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
Dsr Implemented	DSR_IMP	1	R	[76:76]	0h
Reserved[5]	—	2	R	[75:74]	—
Device Size	*C_SIZE	12	R	[73:62]	FFFh
Maximum Read Current at V_{DD} min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Maximum Read Current at V_{DD} max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Maximum Write Current at V_{DD} min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Maximum Write Current at V_{DD} max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device Size Multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase Group Size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase Group Size Multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write Protect Group Size	WP_GRP_SIZE	5	R	[36:32]	8 GB: 0Fh 16 GB: 1Fh
Write Protect Group Enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer Default	DEFAULT_ECC	2	R	[30:29]	0h
Write Speed Factor	R2W_FACTOR	3	R	[28:26]	2h
Maximum Write Data Block Length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial Blocks For Write Allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved[5]	—	4	R	[20:17]	—
Content Protection Application	CONTENT_PROT_APP	1	R	[16:16]	0h
File Format Group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy Flag (OTP)	COPY	1	R/W	[14:14]	0h
Permanent Write Protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h

Notes
5. Reserved bits should be read at '0'.
6. R = Read only. R/W = One time programmable and readable. R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
7. V_{DD} represents the total consumed current for V_{CC} and V_{CCQ}.

Table 6. CSD Register (Continued)

Field Name	Field ID	Size (Bits)	Cell Type	CSD Slice	CSD Value
Temporary Write Protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File Format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC Code	ECC	2	R/W/E	[9:8]	0h
Calculated CRC	CRC	7	R/W/E	[7:1]	—
Not Used	—	1	—	[0]	Always 1

Notes
5. Reserved bits should be read at '0'.
6. R = Read only. R/W = One time programmable and readable. R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
7. V_{DD} represents the total consumed current for V_{CC} and V_{CCQ}.

Extended CSD Register (EXT_CSD)

The Extended CSD Register defines the e.MMC selected modes and properties. It is 512 bytes long. The most significant 320 bytes, also know as Properties segment, define the e.MMC capabilities and cannot be modified by the host. The remaining 192 bytes define e.MMC operating modes and can be modified by the host via a Switch command.

Table 7. Extended CSD Register (EXT_CSD)

Field Name	Field ID	Size (Bytes)	Cell Type	EXT_CSD Slice	Value
Reserved[8]	—	6	—	[511:506]	—
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	00h
Supported Command Sets	S_CMD_SET	1	R	[504]	01h
HPI Features	HPI_FEATURES	1	R	[503]	01h
Background Operations Support	BKOPS_SUPPORT	1	R	[502]	01h
Max Packed Read Commands	MAX_PACKED_READS	1	R	[501]	3Ch
Max Packed Write Commands	MAX_PACKED_WRITES	1	R	[500]	3Ch
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	01h
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	03h
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	00h
Context Management Capabilities	CONTEXT_CAPABILITIES	1	R	[496]	05h
Large Unit Size	LARGE_UNIT_SIZE_M1	1	R	[495]	8 Gb: 03h 16 Gb: 07h
Extended Partitions Attribute Support	EXT_SUPPORT	1	R	[494]	03h
Supported Modes	SUPPORTED_MODES	1	R	[493]	01h
FFU Features	FFU_FEATURES	1	R	[492]	00h
Operation Codes Timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	00h

Notes
8. Reserved bits should be read at 0, unless otherwise specified.
9. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
10. Set to 0 after power up and can be changed via a Switch command.
11. R = Read only.
    R/W = One time programmable and readable.
    R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
    R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
    R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
    W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
12. Value depends on state of the device.
13. Value depends on the firmware that the device is loaded with.

Table 7. Extended CSD Register (EXT_CSD) (Continued)

Field Name	Field ID	Size (Bytes)	Cell Type	EXT_CSD Slice	Value
FFU Argument	FFU_ARG	4	R	[490:487]	Normal mode: 00000000h FFU mode: 0000FFFFh
Reserved[8]		181	—	[486:306]	—
Number of FW Sectors Correctly Programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	00000000h
Reserved[8]	—	32	—	[301:270]	—
Device Life Time Estimation Type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	01h
Device Life Time Estimation Type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	01h
Pre-EOL Information	PRE_EOL_INFO	1	R	[267]	01h[12]
Optimal Read Size	OPTIMAL_READ_SIZE	1	R	[266]	01h
Optimal Write Size	OPTIMAL_WRITE_SIZE	1	R	[265]	04h
Optimal Trim Unit Size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	01h
Device Version	DEVICE_VERSION	2	R	[263:262]	B101h
Firmware Version[13]	FIRMWARE_VERSION	8	R	[261:254]	—
Reserved[8]	—	1	—	[253]	—
Cache Size	CACHE_SIZE	4	R	[252:249]	00000000h
Generic CMD6 Timeout	GENERIC_CMD6_TIME	1	R	[248]	19h
Power Off Notification (Long) Timeout	POWER_OFF_LONG_TIME	1	R	[247]	FFh
Background Operations Status	BKOPS_STATUS	1	R	[246]	00h
Number Of Correctly Programmed Sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	00000000h
1st Initialization Time after Partitioning	INI_TIMEOUT_PA	1	R	[241]	32h
Reserved[8]	—	1	—	[240]	—
Power Class for 52 MHz, DDR at 3.6 V	PWR_CL_DDR_52_360	1	R	[239]	44h
Power Class for 52 MHz, DDR at 1.95 V	PWR_CL_DDR_52_195	1	R	[238]	99h
Power Class for 200 MHz at 1.95 V	PWR_CL_200_195	1	R	[237]	AAh
Power Class for 200 MHz at 1.30 V	PWR_CL_200_130	1	R	[236]	00h
Minimum Write Performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	08h
Minimum Read Performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	08h
Reserved[8]	—	1	—	[233]	—

Notes
8. Reserved bits should be read at 0, unless otherwise specified.
9. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
10. Set to 0 after power up and can be changed via a Switch command.
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12. Value depends on state of the device.
13. Value depends on the firmware that the device is loaded with.

Table 7. Extended CSD Register (EXT_CSD) (Continued)

Field Name	Field ID	Size (Bytes)	Cell Type	EXT_CSD Slice	Value
Trim Multiplier	TRIM_MULT	1	R	[232]	0Fh
Secure Feature Support	SEC_FEATURE_SUPPORT	1	R	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	06h
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	09h
Boot Information	BOOT_INFO	1	R	[228]	07h
Reserved[8]	—	1	—	[227]	—
Boot Partition Size	BOOT_SIZE_MULTI	1	R	[226]	20h
Access Size	ACC_SIZE	1	R	[225]	8 GB: 06h 16 GB: 07h
High Capacity Erase Unit Size	HC_ERASE_GRP_SIZE	1	R	[224]	8 GB: 08h 16 GB: 10h
High Capacity Erase Time Out	ERASE_TIMEOUT_MULT	1	R	[223]	01h
Reliable Write Sector Count	REL_WR_SEC_C	1	R	[222]	01h
High Capacity Write Protect Group Size	HC_WP_GRP_SIZE	1	R	[221]	02h
Sleep Current [V_{CC}]	S_C_VCC	1	R	[220]	08h
Sleep Current [V_{CCQ}]	S_C_VCCQ	1	R	[219]	08h
Production State Awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	14h
Sleep/awake Time Out	S_A_TIMEOUT	1	R	[217]	10h
Reserved[8]	—	1	—	[216]	0Fh
Sector Count	SEC_COUNT	4	R	[215:212]	8 GB: 00E90000h 16 GB: 01D20000h
Reserved[8]	—	1	—	[211]	—
Minimum Write Performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	08h
Minimum Read Performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	08h
Minimum Write Performance for 4-bit at 52 MHz or 8-bit at 26 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	08h
Minimum Read Performance for 4-bit at 52 MHz or 8-bit at 26 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	08h
Minimum Write Performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	08h

Notes

8. Reserved bits should be read at 0, unless otherwise specified.
9. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
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    R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
    W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
12. Value depends on state of the device.
13. Value depends on the firmware that the device is loaded with.

Table 7. Extended CSD Register (EXT_CSD) (Continued)

Field Name	Field ID	Size (Bytes)	Cell Type	EXT_CSD Slice	Value
Minimum Read Performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	08h
Reserved[8]	—	1	—	[204]	—
Power Class for 26 MHz at 3.6 V	PWR_CL_26_360	1	R	[203]	22h
Power Class for 52 MHz at 3.6 V	PWR_CL_52_360	1	R	[202]	22h
Power Class for 26 MHz at 1.95 V	PWR_CL_26_195	1	R	[201]	77h
Power Class for 52 MHz at 1.95 V	PWR_CL_52_195	1	R	[200]	77h
Partition Switching Timing	PARTITION_SWITCH_TIME	1	R	[199]	03h
Out-of-Interrupt Busy Timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	04h
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0Fh
Card Type	CARD_TYPE	1	R	[196]	17h
Reserved[8]	—	1	—	[195]	—
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	02h
Reserved[8]	—	1	—	[193]	—
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	06h
Command Set	CMD_SET	1	R/W/E_P	[191]	00h
Reserved[8]	—	1	—	[190]	—
Command Set Revision	CMD_SET_REV	1	R	[189]	00h
Reserved[8]	—	1	—	[188]	—
Power Class	POWER_CLASS	1	R/W/E_P	[187]	00h
Reserved[8]	—	1	—	[186]	—
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0h[9]
Reserved[8]	—	1	—	[184]	—
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0h[10]
Reserved[8]	—	1	—	[182]	—
Content of Explicit Erased Memory Range	ERASED_MEM_CONT	1	R	[181]	00h
Reserved[8]	—	1	—	[180]	—
Partition Configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	00h
Boot Config Protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	00h
Boot Bus Width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	00h
Reserved[8]	—	1	—	[176]	—
High-Density Erase Group Definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	00h

Notes

8. Reserved bits should be read at 0, unless otherwise specified.
9. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
10. Set to 0 after power up and can be changed via a Switch command.
11. R = Read only.
    R/W = One time programmable and readable.
    R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
    R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
    R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
    W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
12. Value depends on state of the device.
13. Value depends on the firmware that the device is loaded with.

Table 7. Extended CSD Register (EXT_CSD) (Continued)

Field Name	Field ID	Size (Bytes)	Cell Type	EXT_CSD Slice	Value
Boot Write Protection Status Register	BOOT_WP_STATUS	1	R	[174]	00h
Boot Area Write Protect Register	BOOT_WP	1	R/W, R/W/C_P	[173]	00h
Reserved[8]	—	1	—	[172]	—
User Area Write Protect Register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	00h
Reserved[8]	—	1	—	[170]	—
FW Configuration	FW_CONFIG	1	R/W	[169]	00h
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	20h
Write Reliability Setting Register	WR_REL_SET	1	R/W	[167]	00h
Write Reliability Parameter Register	WR_REL_PARAM	1	R	[166]	05h
Start Sanitize Operation	SANITIZE_START	1	W/E_P	[165]	00h
Manually Start Background Operations	BKOPS_START	1	W/E_P	[164]	00h
Enable Background Operations Handshake	BKOPS_EN	1	R/W	[163]	00h
Hardware Reset Function	RST_n_FUNCTION	1	R/W	[162]	00h
HPI Management	HPI_MGMT	1	R/W/E_P	[161]	00h
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	07h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0001D2h
Partitions Attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	00h
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	00h
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	00...00h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	000000h
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	00000000h
Reserved[8]	—	1	—	[135]	—
Bad Block Management Mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	00h
Production State Awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	00h
Package Case Temperature is Controlled	TCASE_SUPPORT	1	W/E_P	[132]	00h
Periodic Wakeup	PERIODIC_WAKEUP	1	R/W/E	[131]	00h
Program CID/CSD in DDR Mode Support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	01h
Reserved[8]	—	2	—	[129:128]	—

Notes
8. Reserved bits should be read at 0, unless otherwise specified.
9. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
10. Set to 0 after power up and can be changed via a Switch command.
11. R = Read only.
    R/W = One time programmable and readable.
    R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
    R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
    R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
    W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
12. Value depends on state of the device.
13. Value depends on the firmware that the device is loaded with.

Table 7. Extended CSD Register (EXT_CSD) (Continued)

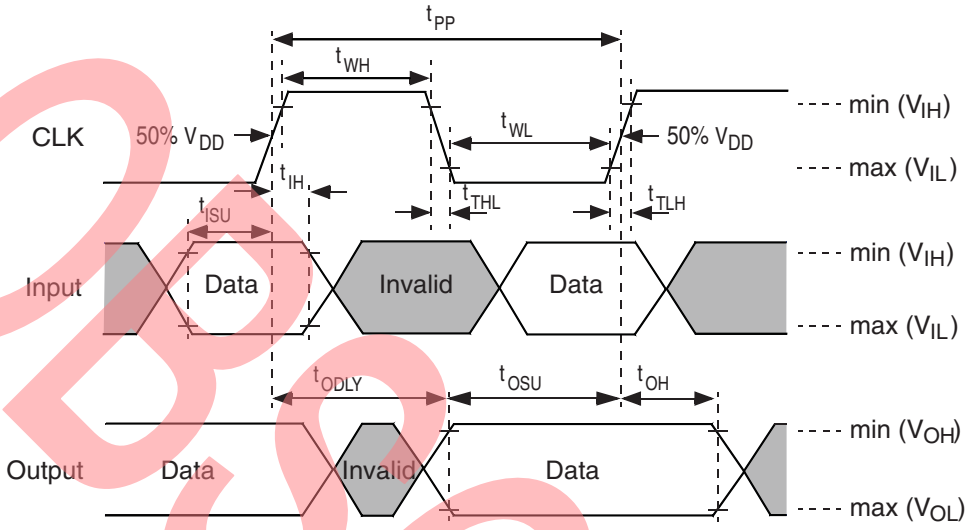
Field Name	Field ID	Size (Bytes)	Cell Type	EXT_CSD Slice	Value
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	00...00h
Native Sector Size	NATIVE_SECTOR_SIZE	1	R	[63]	00h
Sector Size Emulation	USE_NATIVE_SECTOR	1	R/W	[62]	00h
Sector Size	DATA_SECTOR_SIZE	1	R	[61]	00h
1st Initialization After Disabling Sector Size Emulation	INI_TIMEOUT_EMU	1	R	[60]	0Ah
Class 6 Command Control	CLASS_6_CTRL	1	R/W/E_P	[59]	00h
Number Of Address Group To Be Released	DYNCAP_NEEDED	1	R	[58]	00h
Exception Events Control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0000h
Exception Events Status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0000h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0000h
Context Configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	00...00h
Packed Command Status	PACKED_COMMAND_STATUS	1	R	[36]	00h
Packed Command Failure Index	PACKED_FAILURE_INDEX	1	R	[35]	00h
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	00h
Control to Turn the Cache On/Off	CACHE_CTRL	1	R/W/E_P	[33]	00h
Flushing of the Cache	FLUSH_CACHE	1	W/E_P	[32]	00h
Reserved[8]		1	—	[31]	—
Mode Config	MODE_CONFIG	1	R/W/E_P	[30]	00h
Mode Operation Codes	MODE_OPERATION_CODES	1	W/E_P	[29]	00h
Reserved[8]		2	—	[28:27]	—
FFU Status	FFU_STATUS	1	R	[26]	00h
Pre Loading Data Size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	00000000h
Max Pre Loading Data Size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	8 GB: 00748000h 16 GB: 00E90000h
Enable Production State Awareness	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E and R	[17]	01h
Reserved[8]		17	—	[16:0]	—

Notes
8. Reserved bits should be read at 0, unless otherwise specified.
9. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
10. Set to 0 after power up and can be changed via a Switch command.
11. R = Read only.
    R/W = One time programmable and readable.
    R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
    R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable.
    R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
    W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
12. Value depends on state of the device.
13. Value depends on the firmware that the device is loaded with.

AC Parameter

Bus Timing

Figure 7. Bus Timing Diagram[14]



High Speed Timing

Table 8. High Speed Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK					
Clock Frequency Data Transfer Mode	f_{PP}	0	52	MHz	CL ≤ 30 pF Tolerance: +100 kHz
Clock Frequency Identification Mode	f_{OD}	0	400	kHz	Tolerance: +20 kHz
Clock Low Time	t_{WL}	6.5	—	ns	CL ≤ 30 pF
Clock High Time	t_{WH}	6.5	—	ns	CL ≤ 30 pF
Clock Rise Time	t_{TLH}	—	3	ns	CL ≤ 30 pF
Clock Fall Time	t_{THL}	—	3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input Set-up Time	t_{ISU}	3	—	ns	CL ≤ 30 pF
Input Hold Time	t_{IH}	3	—	ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output Delay Time During Data Transfer Mode	t_{ODLY}	—	13.7	ns	CL ≤ 30 pF
Output Hold Time	t_{OH}	2.5	—	ns	CL ≤ 30 pF
Signal Rise Time	t_{RISE}	—	3	ns	CL ≤ 30 pF
Signal Fall Time	t_{FALL}	—	3	ns	CL ≤ 30 pF

Note
14. Data must always be sampled on the rising edge of the clock.

Backward Compatible Timing

Table 9. Backward Compatible Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK					
Clock Frequency Data Transfer Mode	f_{PP}	0	26	MHz	CL ≤ 30 pF
Clock Frequency Identification Mode	f_{OD}	0	400	kHz	
Clock Low Time	t_{WL}	10	—	ns	CL ≤ 30 pF
Clock High Time	t_{WH}	10	—	ns	—
Clock Rise Time	t_{TLH}	—	10	ns	CL ≤ 30 pF
Clock Fall Time	t_{THL}	—	10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input Set-Up Time	t_{ISU}	3	—	ns	CL ≤ 30 pF
Input Hold Time	t_{IH}	3	—	ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output Hold Time	t_{OH}	8.3	—	ns	CL ≤ 30 pF
Output Set-up Time	t_{OSU}	11.7	—	ns	CL ≤ 30 pF

DDR Interface Timing

Figure 8. DDR Interface Timing

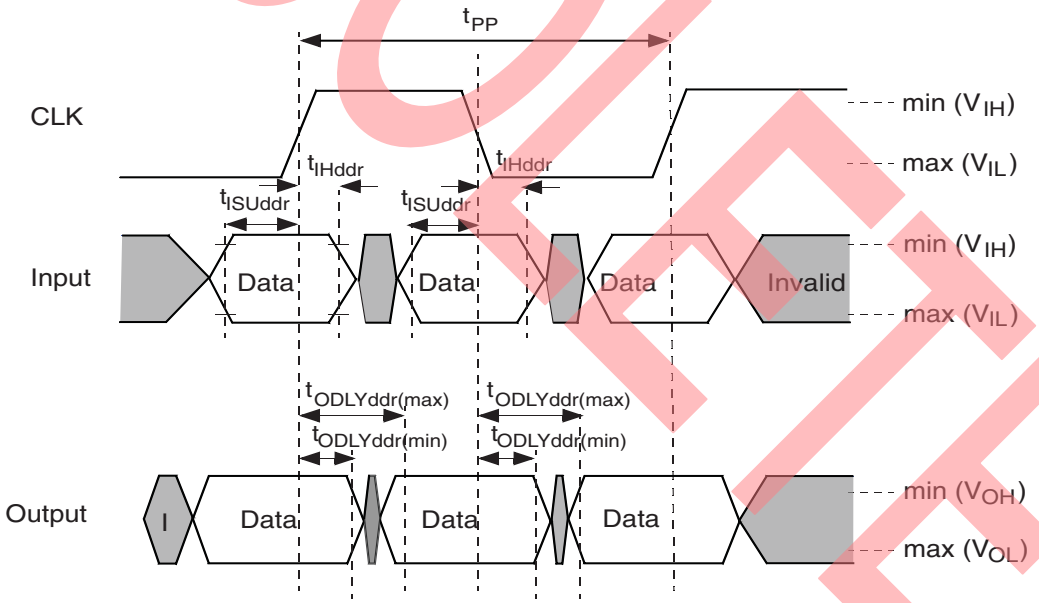


Table 10. DDR Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK1					
Clock Duty Cycle	—	45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input Set-up Time	t_{ISUddr}	2.5	—	ns	CL ≤ 20 pF
Input Hold Time	t_{IHddr}	2.5	—	ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output Delay Time During Data Transfer	$t_{ODLYddr}$	1.5	7	ns	CL ≤ 20 pF
Signal Rise Time (All Signals)	t_{RISE}	—	2	ns	CL ≤ 20 pF
Signal Fall Time (All Signals)	t_{FALL}	—	2	ns	CL ≤ 20 pF

Timing Specifications for HS200 Mode

HS200 Clock Timing

HS200 mode is available when V_{CCQ} is 1.7V to 1.95V, and the clock timing should conform with the timing diagram shown in Figure 9. CLK input timings need to meet the clock timing across the entire range of operating environment. CLK timings must be measured while CMD and DAT signals are either high or low. HS200 supports clock frequencies of up to 200 MHz.

Figure 9. HS200 Clock Signal Timing

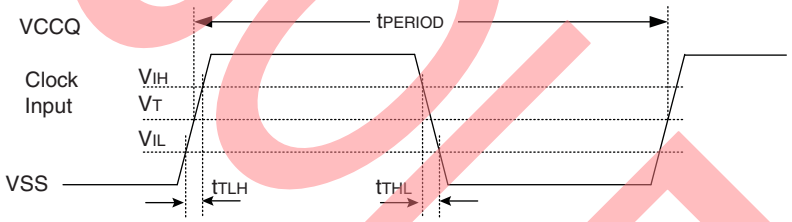


Table 11. HS200 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{PERIOD}	5	—	ns	200 MHz (max.) between rising edges.
t_{TLH}, t_{THL}	—	0.2 t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1 ns (max.) at 200 MHz, CBGA = 12 pF. The absolute max. value of t_{TLH}, t_{TLH} is 10 ns regardless of clock frequency.
Duty Cycle	30	70	%	—

Note
15. V_{IH} denotes $V_{IH(min.)}$, and V_{IL} denotes $V_{IL(max.)}$.
16. V_T = 0.975 V, Clock Threshold (V_{CCQ} = 1.8 V); indicates reference points for timing measurements.

HS200 Input Timing

Figure 10. HS200 Device Input Timing[17, 18]

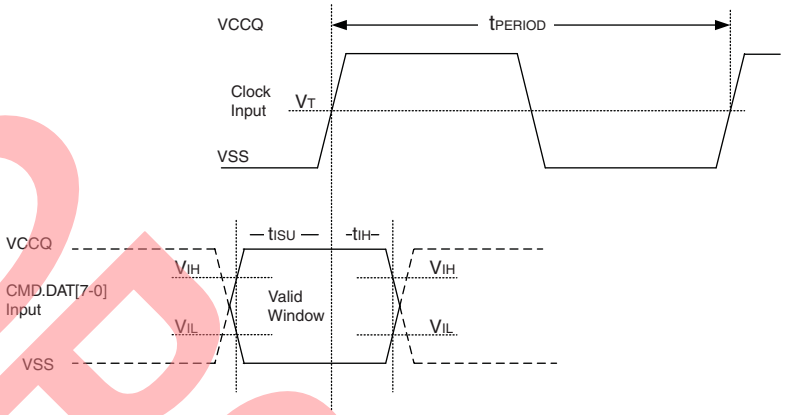


Table 12. HS200 Device Input Timing

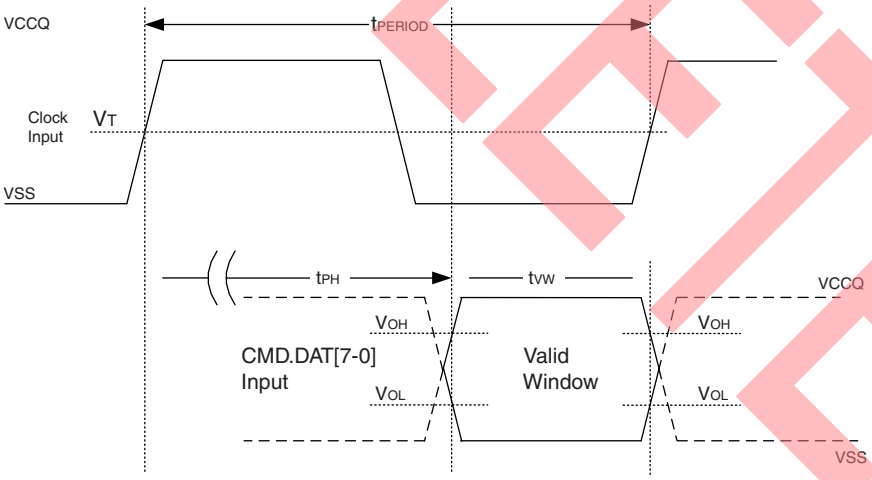
Symbol	Min	Max	Unit	Remark
t_{ISU}	1.40	—	ns	5 pF ≤ CBGA ≤ 12 pF
t_{IH}	0.8	—	ns	5 pF ≤ CBGA ≤ 12 pF

HS200 Output Timing

The t_{PH} parameter is defined to allow device output delay to be longer than t_{PERIOD}. t_{PH} may have random phase relation to the clock upon initialization. The Host is ultimately responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

The impact of a temperature drift (Δ_{TPH}) has to be taken into account when setting the sampling point. Output valid data window (t_{VW}) is available regardless of the drift (Δ_{TPH}) while the position of data window varies by the drift.

Figure 11. HS200 Device Output Timing[19]

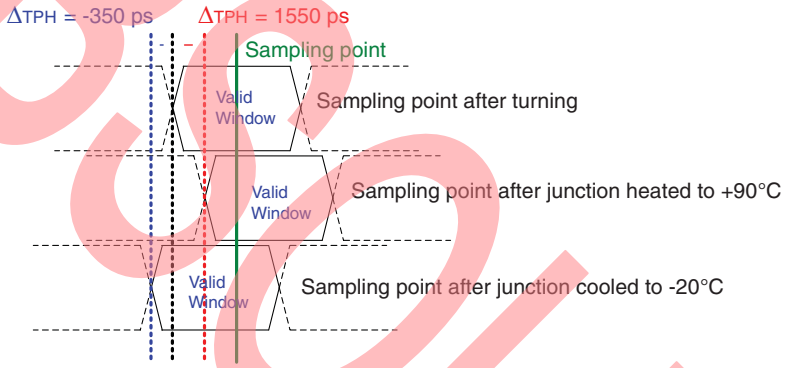


Note
17. t_{ISU} and t_{IH} are measured at $V_{IL(max.)}$ and $V_{IH(min.)}$.
18. V_{IH} denotes $V_{IH(min.)}$, and V_{IL} denotes $V_{IL(max.)}$.
19. V_{OH} denotes $V_{OH(min.)}$, and V_{OL} denotes $V_{OL(max.)}$.

Table 13. HS200 Device Output Timing[20]

Symbol	Min	Max	Unit	Notes
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
Δ_{TPH}	−350 (ΔT = −20 °C)	+1550 (ΔT = 90 °C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (t_{VW}) from last system Tuning procedure. Δ_{TPH} is 2600 ps for ΔT from −25 °C to 125 °C during operation.
t_{VW}	0.575	—	UI	t_{VW} = 2.88 ns at 200 MHz. Host path may add Signal Integrity induced noise, skews, and so on. Expected t_{VW} at Host input is larger than 0.475 UI.

Figure 12. Δ_{TPH} Consideration



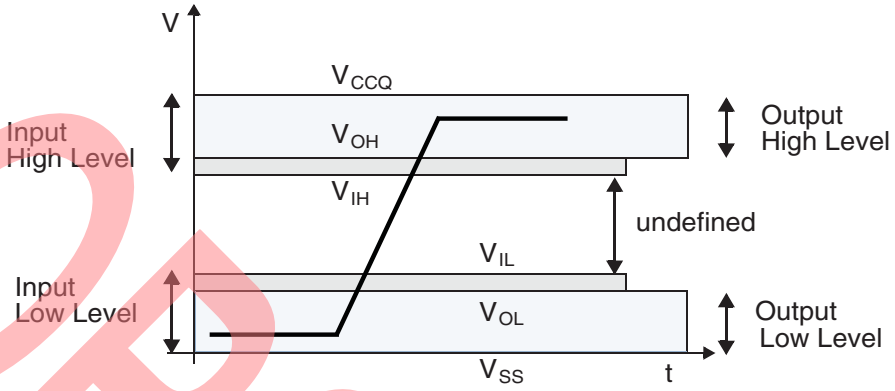
Implementation Guide:

- The host should avoid sampling errors that are caused by the Δ_{TPH} drift.
- Tuning should be performed while the device wakes up after sleep.
- Reducing operating frequency can help overcome the Δ_{TPH} drift.

Note
20. Unit Interval (UI) is one-bit nominal time (i.e., UI = 5 ns at 200 MHz).

Signal Levels

Figure 13. Signal Levels



Open-Drain Mode Bus Signal Level

Table 14. Open-Drain Mode Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output High Voltage	V_{OH}	V_{CCQ} - 0.2	—	V	I_{OH} = –100 µA
Output Low Voltage	V_{OL}	—	0.3	V	I_{OLL} = 2 mA

Push-Pull Mode Bus Signal Level — High Voltage e.MMC

Table 15. Push-Pull Mode Bus Signal Level — High Voltage e.MMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output High Voltage	V_{OH}	0.75 * V_{CCQ}	—	V	I_{OH} = –100 µA at V_{CCQ} min
Output Low Voltage	V_{OL}	—	0.125 * V_{CCQ}	V	I_{OL} = 100 µA at V_{CCQ} min
Input High Voltage	V_{IH}	0.625 * V_{CCQ}	V_{CCQ} + 0.3	V	—
Input Low Voltage	V_{IL}	V_{SS} - 0.3	0.25 * V_{CCQ}	V	—

Push-Pull Bus Signal Level — Dual Voltage e.MMC

Table 16. Push-Pull Bus Signal Level — Dual Voltage e.MMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output High Voltage	V_{OH}	V_{CCQ} - 0.45V	—	V	I_{OH} = –2 mA
Output Low Voltage	V_{OL}	—	0.45V	V	I_{OL} = 2 mA
Input High Voltage	V_{IH}	0.65 * V_{CCQ}	V_{CCQ} + 0.3	V	—
Input Low Voltage	V_{IL}	V_{SS} - 0.3	0.35 * V_{CCQ}	V	—

DC Parameter

Supply Voltage

Table 17. Supply Voltage

Symbol	Min	Max	Unit
V_{CC}	2.7	3.6	V
V_{CCQ}	2.7	3.6	V
	1.7	1.95	V
V_{SS}	−0.5	0.5	V

Bus Operating Condition

Table 18. Bus Operating Condition

Parameter	Min	Max	Unit
Peak Voltage on all lines	−0.5	V_{CCQ} + 0.5	V
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	−2	2	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	−2	2	µA

Power Consumption (Temperature = 25 °C)

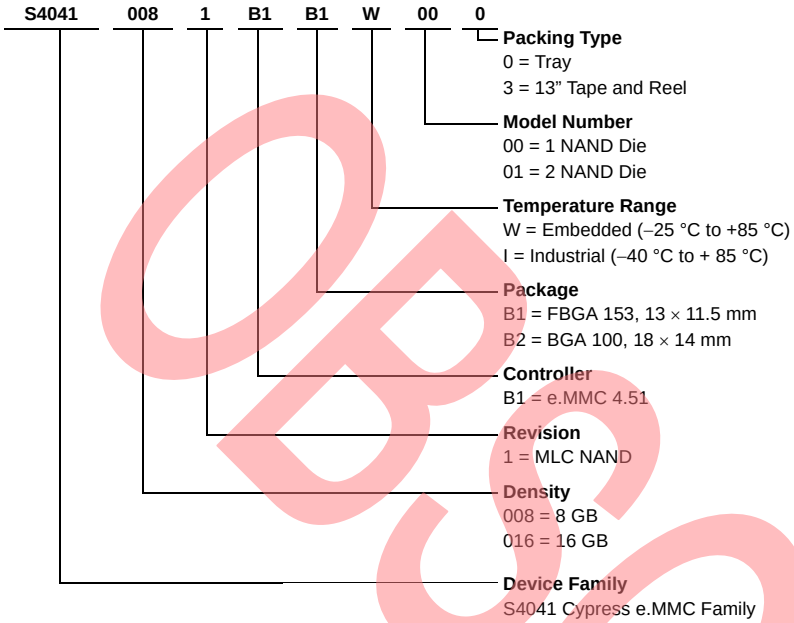
Table 19. Power Consumption (Temperature = 25 °C)[21, 22, 23]

Density	Mode	V_{CCQ}			V_{CC}		
		3.6V	1.95V		3.6V		
		SDR52	DDR52	HS200	SDR52	DDR52	HS200
8 GB	Write [mA]	50	50	100	100	100	100
	Read [mA]	50	50	100	100	100	100
	Standby	650 µA					
	Sleep (CMD5)	500 µA					
16 GB	Write [mA]	50	50	100	100	150	150
	Read [mA]	50	50	100	100	150	150
	Standby	700 µA					
	Sleep (CMD5)	500 µA					

Note
21. Measurements averaged over periods of 100 ms.
22. In Standby mode, CLK is set low.
23. In Sleep mode, VCC power supply is off.

Ordering Information

The ordering part number is formed by a valid combination of the following:



Valid Combinations

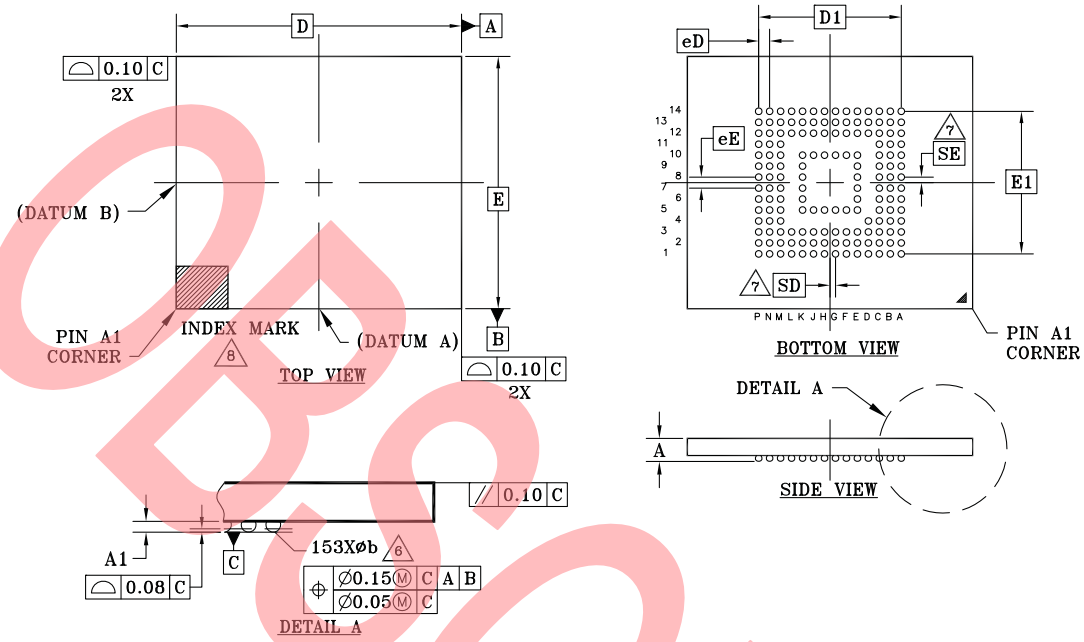
Valid Combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 20. Valid Combinations

Device Family	Density	Revision	Controller	Package Type	Tempera-ture Range	Model Number	Packing Type	Package Description
S4041	008	1	B1	B1, B2	W, I	00	0, 3	BGA
	016					01		

Package Diagrams

Figure 14. VFBGA 153 (13 × 11.5 × 1.0 mm)



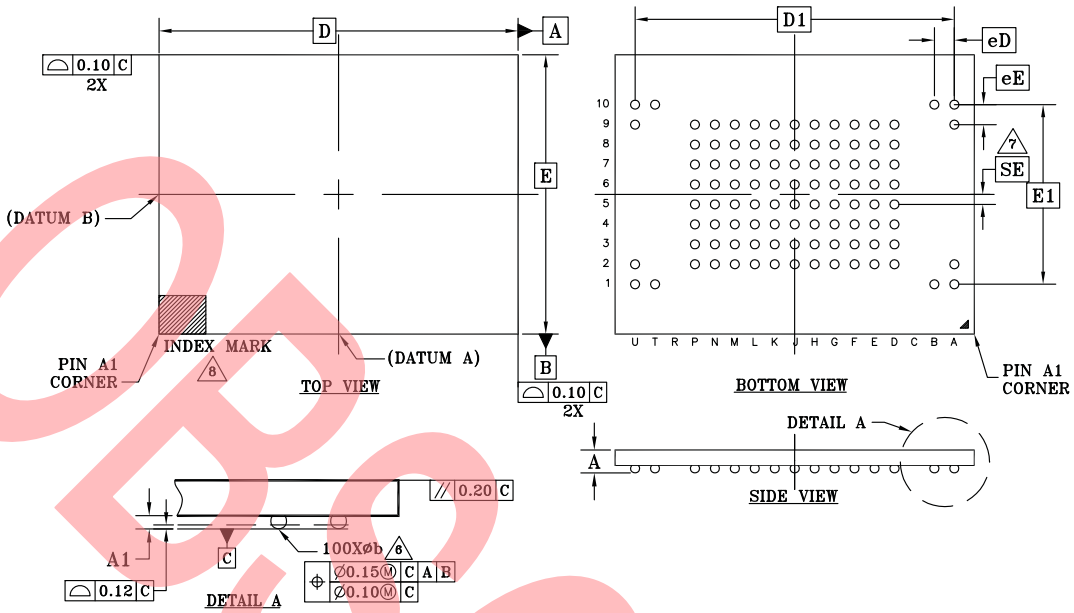
PACKAGE	RLH/RMA 153			NOTE
JEDEC	MO-276			
D X E	13.00 mm x 11.50 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.00	PROFILE
A1	0.17	---	---	BALL HEIGHT
D	13.00 BSC			BODY SIZE
E	11.50 BSC			BODY SIZE
D1	6.50 BSC			MATRIX FOOTPRINT
E1	6.50 BSC			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	153			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC			SOLDER BALL PLACEMENT
	D5-D11,E11-K11,L4-L11,E4-K4 F6-F9,G6-G9,H6-H9,J6-J9			DEPOPULATED SOLDER BALL LOCATIONS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.6.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
9. TEST PADS MAY BE PRESENT BUT ARE NOT SHOWN. THEY ARE FOR INTERNAL USE ONLY AND ARE NOT SOLDER BALLS.

g5028 \ f16-038.63 \ 3-21-2014

Figure 15. LBGA 100 (18 × 14 × 1.4 mm)



PACKAGE	L2B/L3B 100			NOTE
JEDEC	MO-304			
D X E	18.00mm X 14.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	---	---	1.40	PROFILE
A1	0.25	---	---	BALL HEIGHT
D	18.00 BSC			BODY SIZE
E	14.00 BSC			BODY SIZE
D1	16.00 BSC			MATRIX FOOTPRINT
E1	9.00 BSC			MATRIX FOOTPRINT
MD	17			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	100			BALL COUNT
Ø b	0.40	0.45	0.50	BALL DIAMETER
eE	1.00 BSC			BALL PITCH
eD	1.00 BSC			BALL PITCH
SE	0.50 BSC			SOLDER BALL PLACEMENT
	A3-A8,B2-B9,C1-C10,U3-U8, T2-T9,R1-R10,D10-P10,D1-P1			DEPOPULATED SOLDER BALL LOCATIONS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP 95, SECTION 4.6.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP 95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = e/2
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
9. TEST PADS MAY BE PRESENT BUT ARE NOT SHOWN. THEY ARE FOR INTERNAL USE ONLY AND ARE NOT SOLDER BALLS.

gs5027-l2b/l3b 100-3/21/2014

Document History Page

Document Title: S4041-1B1, 8 GB / 16 GB, 3.0 V e.MMC Flash Document Number: 002-02760				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	BWHA	04/17/2014	Global: Changed S4041-1 to S4041-1B1 Features: Operating Temperature Range: changed ‘Extended Commercial’ to ‘Super Commercial’ Physical Diagram: Updated figures: VFBGA 153 — Package Dimensions 13 mm x 11.5 mm x 1.0 mm LBGA 100 — Package Dimensions 18 mm x 14 mm x 1.4 mm Extended CSD Register (EXT_CSD)Updated Extended CSD Register (EXT_CSD) table Ordering Information: Updated Model Number and Controller descriptions Temperature Range: changed ‘Extended Commercial’ to ‘Super Commercial’
*A	—	BWHA	08/05/2014	Key Supported Features: Changed ‘Secure Erase’ to Sanitize Removed Secure Trim Key Supported e.MMC Features: Changed ‘Secure Erase’ to Sanitize. Updated section Removed Secure Trim section Register Values: Updated Extended CSD Register (EXT_CSD) table DC Parameter: Power Consumption (Temperature = 25°C) table: corrected Standby and Sleep (CMD5) values, corrected Note 2 Ordering Information: Valid Combinations table: corrected Model Numbers
*B	—	BWHA	10/06/2014	Features: Added Storage Temperature Performance: Corrected Random Read and Random Write General Description: Updated section Recommended System Configuration: Removed section
*C	—	BWHA	10/16/2014	Global: Data Sheet designation updated from Advance Information to Preliminary Features: Operating Temperature Range: changed ‘Super Commercial’ to ‘Embedded’ Auto Background Operations: Added Auto Background Operations section Ordering Information: Temperature Range: changed ‘Super Commercial’ to ‘Embedded’
*D	—	BWHA	11/14/2014	Ordering InformationUpdated Revision description.
*E	—	BWHA	01/12/2015	PerformanceChanged ‘Random Read (IOPS) to 5000. Changed ‘Sequential Read (MB/s)’ to 120.
*F	—	BWHA	02/26/2015	Package Configurations: FBGA 153 (Top View, Balls Down) figure: corrected ball C5 to NC.
*G	4963172	BWHA	11/16/2015	Updated to new template.
*H	5160239	XILA	03/03/2016	Obsolete datasheet.

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