



## S6E2G Series

# 32-bit ARM<sup>®</sup> Cortex<sup>®</sup>-M4F FM4 Microcontroller

S6E2G Series are FM4 devices with up to 180 MHz CPU, 1MB flash, 192KB SRAM, 20x communication peripherals, 33x digital peripherals and 3x analog peripherals. They are designed for industrial automation and metering applications.

Devices in the S6E2G Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the ARM Cortex-M4F processor with on-chip flash memory and SRAM. The series has peripherals such as motor control timers, A/D converters, and communications interfaces (USB, CAN, UART, CSIO (SPI), I2C, LIN). The products that are described in this data sheet are placed into TYPE5-M4 product categories in the "FM4 Family Peripheral Manual Main Part (002-04856)".

- 32-bit ARM Cortex-M4F Core
  - Up to 180 MHz frequency operation
- On-chip Memories
  - Flash memory: Up to 1024 Kbytes
  - SRAM memory:
    - SRAM0: up to 128 Kbytes
    - SRAM1: 32 Kbytes
    - SRAM2: 32 Kbytes
- Direct Memory Access (DMA) Controller (Eight Channels)
- Descriptor System Data Transfer Controller (DSTC); 256 channels
- External Bus Interface
- USB Interface (Max two channels): Host and Device
- CAN Interface (Max one channel) Available on S6E2GM and S6E2GH Devices Only
- Multi-function Serial Interface (Max 10 Channels)
  - UART (Universal Asynchronous Receiver/Transmitter)
  - Clock Synchronous Serial Interface (CSIO (SPI))
  - Local Interconnect Network (LIN)
  - Inter-Integrated Circuit (I<sup>2</sup>C)
  - Inter-IC Sound (I<sup>2</sup>S)
- Base Timer (Max 16 channels)
- General Purpose I/O Port
  - Up to 121 high-speed general-purpose I/O ports in 144-pin package
  - Up to 153 high-speed general-purpose I/O ports in 176-pin package
- Multi-function Timer (Max two units)
- Real-Time Clock (RTC)
- Analog to Digital Converter (ADC) (Max 32 Channels)
- Dual Timer (32-/16-bit Down Counter)
- Quadrature Position/Revolution Counter (QPRC; Max four channels)
- Watch Counter
- External Interrupt Controller Unit
- Watchdog Timer (Two channels)
- Cyclic Redundancy Check (CRC) Accelerator
- SD Card Interface Available on S6E2GM, S6E2GH, and S6E2GK Devices Only
- Ethernet-MAC Available on S6E2GM, S6E2GK, and S6E2G2 Devices only
- Smartcard Interface (Max 2 channels)
- Five Clock Sources
- Six Reset Sources
- Clock Supervisor (CSV)
- Low-Voltage Detector (LVD)
- Six Low-power Consumption Modes
  - Sleep
  - Timer
  - RTC
  - Stop
  - Deep standby RTC
  - Deep standby stop
- Peripheral Clock Gating System
- Crypto Assist Function
- Debug
  - Serial wire JTAG debug port (SWJ-DP)
  - Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
  - AHB trace macrocells (HTM)
- 41-bit Unique ID
- Wide range voltage: VCC = 2.7 to 5.5 V

## Ecosystem for Cypress FM4 MCUs

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right MCU for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for FM4 MCUs:

- Overview: [Product Portfolio](#), [Product Roadmap](#)
- Product Selectors: [FM4 MCUs](#)
- Application notes: Cypress offers a large number of FM4 application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FM4 family of MCUs are:
  - [AN204468 - FM4 I2S USB MP3 Player Application 32-Bit Microcontroller FM4 Family](#): This application note describes the general structure of the I2S USB MP3Player software example, its single modules in detail and how it is used.
  - [AN204471 - FM4 S6E2CC Series External Memory Programmer](#): This document describes use of the MCU Universal Programmer as an off-line programmer for Quad SPI flash memory programming on the S6E2CC Series SK.
  - [AN203277 - FM 32-Bit Microcontroller Family Hardware Design Considerations](#): This application note reviews several topics for designing a hardware system around FM0+, FM3, and FM4 family MCUs. Subjects include power system, reset, crystal, and other pin connections, and programming and debugging interfaces.
  - [AN202488 - FM4 MB9BF56x and S6E2HG Series MCU - Servo Motor Speed Control](#): This document covers servo motor speed control solution on FM4 MCU - MB9BF56x and S6E2HG.
  - [AN99235 - FM4 S6E2HG Series MCU - 16-Bit PWM Using a Base Timer](#): Cypress FM4 Family of 32-bit ARM® Cortex®-M4 Microcontrollers FM4 S6E2H Series Motor Control ARM® Cortex®-M4 MCU
  - [AN202487 - Differences Among FM0+, FM3, and FM4 32-Bit Microcontrollers](#): Highlights the peripheral differences in Cypress's FM family MCUs. It provides dedicated sections for each peripheral and contains lists, tables, and descriptions of peripheral feature and register differences.
  - [AN204438 - How to Setup Flash Security for FM0+, FM3 and FM4 Families](#): This application note describes how to setup the Flash Security for FM0+, FM3, and FM4 devices
- Development kits:
  - [FM4-U120-9B560 - ARM® Cortex®-M4 MCU Starter Kit with USB and CMSIS-DAP](#)
  - [FM4-216-ETHERNET ARM® Cortex®-M4 MCU Development Kit with Ethernet, CAN and USB Host](#)
  - [FM4-176L-S6E2CC-ETH - ARM® Cortex®-M4 MCU Starter Kit with Ethernet and USB Host](#)
  - [FM4-176L-S6E2GM - ARM® Cortex®-M4 MCU Pioneer Kit with Ethernet and USB Host](#)
- Peripheral Manuals

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## 2. Product Lineup

### Memory Size

Memory Type		Product Name	
		<b>S6E2GM6</b> <b>S6E2GK6</b> <b>S6E2GH6</b> <b>S6E2G36</b> <b>S6E2G26</b>	<b>S6E2GM8</b> <b>S6E2GK8</b> <b>S6E2GH8</b> <b>S6E2G38</b> <b>S6E2G28</b>
On-chip flash memory		512 Kbytes	1024 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes
	SRAM0	64 Kbytes	128 Kbytes
	SRAM1	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes

### Function Availability by Part

Description		Product Name				
		<b>S6E2GM6</b> <b>S6E2GM8</b>	<b>S6E2GK6</b> <b>S6E2GK8</b>	<b>S6E2GH6</b> <b>S6E2GH8</b>	<b>S6E2G36</b> <b>S6E2G38</b>	<b>S6E2G26</b> <b>S6E2G28</b>
CPU		Cortex-M4F, MPU, NVIC 128 ch				
	Freq.	180 MHz				
Power supply voltage range		2.7 V to 5.5 V				
USB2.0 (Device/Host)		2 ch				
Ethernet-MAC		1 ch. (Max) MII: 1 ch / RMII: 1 ch (Max)	N/A		1ch. (Max) MII: 1 ch / RMII: 1 ch (Max)	
CAN		1 ch (Max)	N/A	1 ch (Max)	N/A	
SD card interface		1 unit			N/A	
DMAC		8 ch				
DSTC		256 ch				
External bus interface		Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash SDRAM				
Multi-function serial interface (UART/CSIO(SPI)/LIN/I <sup>2</sup> C/I <sup>2</sup> S)		10ch (Max) ch 1, ch 4 to ch 7: FIFO, ch 0, ch 2, ch3, ch 8 to ch 15: No FIFO ch 1: I <sup>2</sup> S				

Description	Product Name				
	S6E2GM6 S6E2GM8	S6E2GK6 S6E2GK8	S6E2GH6 S6E2GH8	S6E2G36 S6E2G38	S6E2G26 S6E2G28
Base timer (PWC/Reload timer/PWM/PPG)	16 ch (Max)				
MF timer	A/D activation compare	6 ch	2 units (Max)		
	Input capture	4 ch			
	Free-run timer	3 ch			
	Output compare	6 ch			
	Waveform generator	3 ch			
	PPG	3 ch			
Smartcard (ISO7816)	2 ch (Max)				
QPRC	4 ch (Max)				
Dual timer	1 unit				
Real-time clock	1 unit				
Watch counter	1 unit				
CRC accelerator	Yes (fixed)				
Watchdog timer	1 ch (SW) + 1 ch (HW)				
External interrupts	32 pins (Max)+ NMI × 1				
CSV (clock supervisor)	Yes				
LVD (low-voltage detector)	2 ch				
Built-in CR	High-s peed	4 MHz (±2%)			
	Low-s peed	100 kHz (Typ)			
Debug function	SWJ-DP/ETM/HTM				
Unique ID	Yes				

\*1: Crypto Assist Function is built in following products.  
S6E2GM6HHA, S6E2GM8HHA, S6E2GM6JHA, S6E2GM8JHA

**Notes:**

- Because of package pin limitations, not all functions within the device can be brought out to external pins. You must carefully work out the pin allocation needed for your design.  
You must use the port relocate function of the I/O port according to your function use.
- See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.

### 3. Package-Dependent Features

All S6E2G Series of parts are available in both 144-pin LQFP and 176-pin LQFP.

Description	Base Part Number S6E2G			
	Package Suffix			
	H0A	HHA*	J0A	JHA*
LQFP: (0.5 mm pitch)	144 pins		176 pins	
I/O Ports	121 pins (Max)		153 pins (Max)	
12-bit ADC converter	24 (3 units)		32 ch (3 units)	
Crypto Assist Function	—	Yes	—	Yes

\*HHA and JHA parts have the Crypto Assist Function built in. HHA and JHA options are not available for the S6E2GH or S6E2G3 parts. The HHA and JHA options are available on the S6E2GM, S6E2GK, and S6E2G2 parts.

**Notes:**

- For an explicit list of part numbers and the feature differences among them, see 13. Ordering Information
- See 14. Package Dimensions for detailed information on each package.

## 4. Product Features in Detail

### 32-bit ARM Cortex-M4F Core

- Up to 180 MHz frequency operation
- FPU built-in
- Support DSP instructions
- Memory protection unit (MPU): improves the reliability of an embedded system
- Integrated nested vectored interrupt controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): system timer for OS task management

### On-chip Memories

#### ■ Flash memory

This series is on-chip flash memories.

- Up to 1024 Kbytes
- Built-in flash accelerator for zero wait state
- Security function for code protection

#### ■ SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to the I-code bus and D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to system bus of Cortex-M4F core.

- SRAM0: up to 128 Kbytes
- SRAM1: 32 Kbytes
- SRAM2: 32 Kbytes

### External Bus Interface

- Supports SRAM, NOR, NAND flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-/32-bit data width
- Up to 25-bit address bus
- Supports address/data multiplexing
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000\_0000 to 0xDFFF\_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note:** It is necessary to use the Cypress provided software library to use the scramble function.

### USB Interface (Max two channels)

The USB interface is composed of a Device and a Host.

- USB Device
  - USB 2.0 Full-speed supported
  - Max 6 EndPoint supported

- EndPoint 0 is control transfer
- EndPoint 1,2 can be selected bulk-transfer, interrupt-transfer or isochronous-transfer
- EndPoint 3 to 5 can select bulk-transfer or interrupt-transfer
  - EndPoint 1 to 5 comprise double buffer
  - The size of each endpoint is as follows.
    - Endpoint 0, 2 to 5: 64 byte
    - EndPoint 1: 256 byte

#### ■ USB Host

- USB2.0 Full-Speed/Low-Speed supported
- Bulk-transfer, interrupt-transfer, and isochronous-transfer support
- USB Device connected/dis-connected automatically detect
- IN/OUT token handshake packet automatically
- Max 256-byte packet length supported
- Wake-up function supported

### CAN Interface (Max one channel) Available on S6E2GM and S6E2GH Devices Only

- Compatible with CAN specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32-message buffer

### Multi-function Serial Interface (Max 10 Channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 1 and channels 4 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I2C
  - I2S
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)



- LIN break delimiter generation (can change to 1- to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)
- I<sup>2</sup>C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported
- I<sup>2</sup>S
  - Using CSIO (SPI) (ch 1 only) and I2S clock generator
  - Supports two transfer protocol: I2S and MSB-justified
  - Master mode only

### DMA Controller (Eight Channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

### DSTC (Descriptor System Data Transfer Controller; 256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

### A/D Converter (Max 32 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5  $\mu$ s at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

### Base Timer (Max 16 channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer

- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer
- Event counter mode (External clock mode)

### General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 121 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.  
See 6. Pin Descriptions and 7. I/O Circuit Type for the corresponding pins.

### Multi-function Timer (Max two units)

The multi-function timer is composed of the following blocks:  
Minimum resolution: 5.56 ns

- 16-bit free-run timer  $\times$  3 ch/unit
- Input capture  $\times$  4 ch/unit
- Output compare  $\times$  6 ch/unit
- A/D activation compare  $\times$  6 ch/unit
- Waveform generator  $\times$  3 ch/unit
- 16-bit PPG timer  $\times$  3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

### Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute/second/day of the week) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

### Quadrature Position/Revolution Counter (QPRC; Max four channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

### Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

### Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

### External Interrupt Controller Unit

- External interrupt input pin: Max 32 pins
  - Both edges(Rise edge and Fall edge) detect
- Include one non-maskable interrupt (NMI)

### Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

### Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

### SD Card Interface Available on S6E2GM, S6E2GH, and S6E2GK Devices Only

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

### Ethernet-MAC Available on S6E2GM, S6E2GK, and S6E2G2 Devices only

- Compliant with IEEE802.3 specification
- 10 Mbps/100 Mbps data transfer rates supported
- MII/RMII for external PHY device supported.
- MII: Max one channel
- RMII: Max one channel
- Full-duplex and half-duplex mode supported.
- Wake-ON-LAN supported
- Built-in dedicated descriptor-system DMAC
- Built-in 2 Kbytes transmit FIFO and 2 Kbytes receive FIFO.
- Compliant IEEE1558-2008 (PTP)

### Smartcard Interface (Max 2 channels)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

### Clock and Reset

- Clocks
 

Five clock sources (two external oscillators, two internal CR oscillators, and Main PLL) that are dynamically selectable.

  - Main clock: 4 MHz to 48 MHz
  - Sub clock: 30 kHz to 100 kHz
  - High-speed internal CR clock: 4 MHz
  - Low-speed internal CR clock: 100 kHz
  - Main PLL Clock

### ■ Resets

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timer reset
- Low-voltage detector reset
- Clock supervisor reset

### Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

### Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

### Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

### Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

### Crypto Assist Function

These features are enabled for the crypto assist function.

The dedicated middleware is necessary for this calculator operation.

- PKA (Public Key Accelerator)
  - PKA (Public Key Accelerator) is modular exponentiation calculation accelerator used of RSA Public Key crypto and so on.
  - Available bit length: Up to 2048-bit
- AES calculator
  - AES (Advanced Encryption Standard) calculator is a AES common key crypto accelerator which is compliant with FIPS (Federal Information Processing Standard Publication)197.
  - Available key length: 128/192/256-bit
  - CBC mode and ECB mode support
- External Bus Data Scramble
  - It enables to scramble input/output data of External Bus Interface.

### Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

### Unique ID

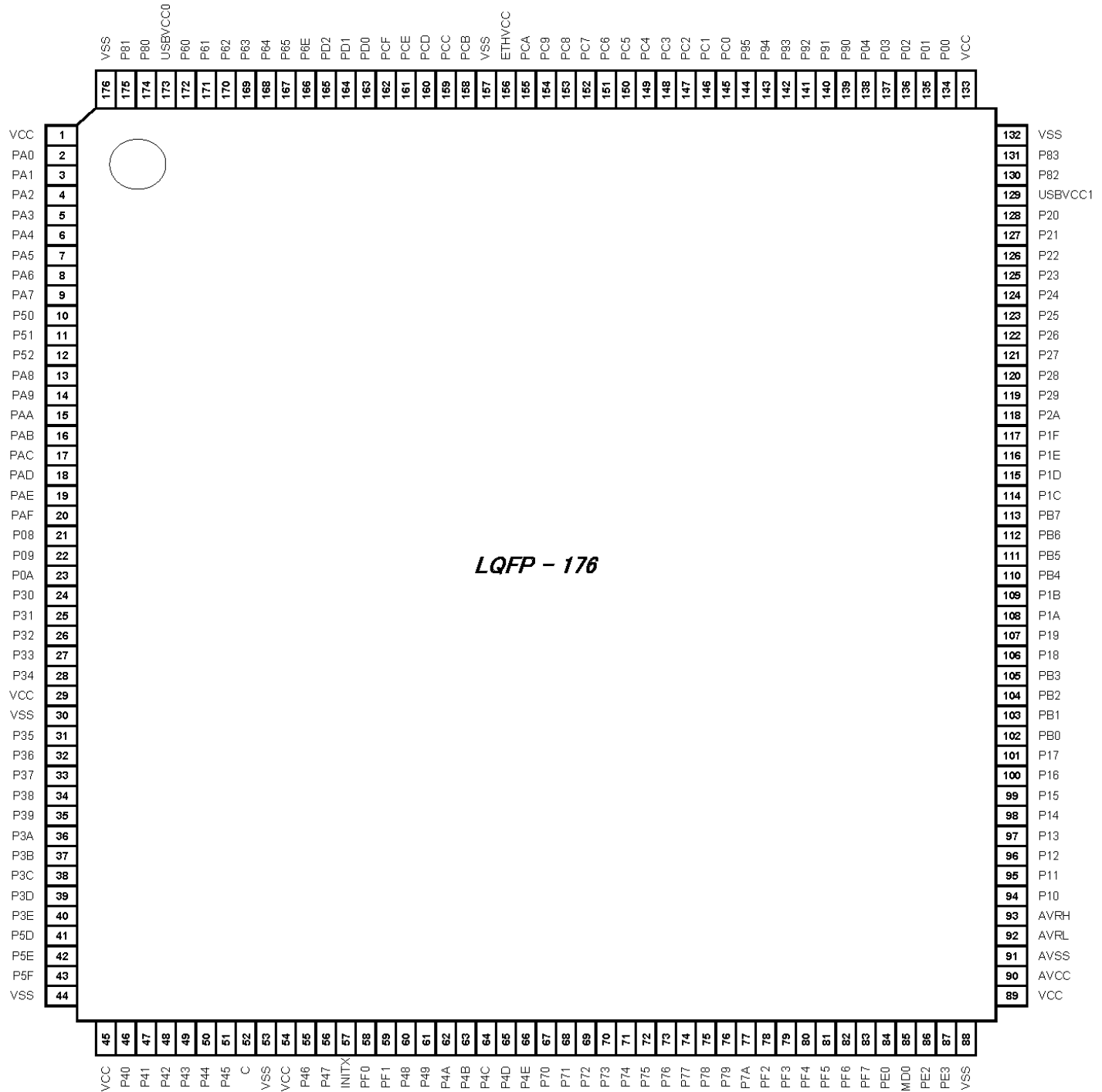
Unique value of the device (41-bit) is set.

### Power Supply

- Five power supplies
  - Wide range voltage: VCC = 2.7 V to 5.5 V
  - Power supply for USB ch 0 I/O: USBVCC0 = 3.0 V to 3.6 V (when USB is used) = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for USB ch 1 I/O: USBVCC1 = 3.0 V to 3.6 V (when USB is used) = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for Ethernet-MAC I/O: ETHVCC = 3.0 V to 5.5 V (when Ethernet is used.)



## LQP176



**Note:**

– Only the GPIO function is shown on GPIO pins. See the table in [Pin Descriptions](#) for the full, multiplexed signal name.

## 6. Pin Descriptions

### List of Pin Functions

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
1	1	VCC	-	-
2	2	PA0	E	K
		RTO00_1 (PPG00_1)		
		TIOA8_0		
		INT00_0		
		MADATA00_0		
IC0_CIN_0				
3	3	PA1	E	I
		RTO01_1 (PPG01_1)		
		TIOA9_0		
		MADATA01_0		
IC0_DATA_0				
4	4	PA2	E	I
		RTO02_1 (PPG02_1)		
		TIOA10_0		
		MADATA02_0		
IC0_RST_0				
5	5	PA3	E	I
		RTO03_1 (PPG03_1)		
		TIOA11_0		
		MADATA03_0		
IC0_VPEN_0				
6	6	PA4	E	I
		RTO04_1 (PPG04_1)		
		TIOA12_0		
		MADATA04_0		
IC0_VCC_0				
7	7	PA5	E	K
		RTO05_1 (PPG05_1)		
		TIOA13_0		
		INT01_0		
		MADATA05_0		
IC0_CLK_0				

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
8	8	PA6	E	K
		DTTIOX_1		
		INT00_2		
		MADATA06_0		
9	9	PA7	E	K
		IC00_1		
		INT02_2		
		MADATA07_0		
		RTCCO_1		
		SUBOUT_1		
10	-	P50	E	I
		SCS72_0		
		IC01_1		
		TIOA8_2		
11	-	P51	E	I
		SCS73_0		
		IC02_1		
		TIOB8_2		
12	-	P52	E	I
		IC03_1		
		TIOA9_2		
13	10	PA8	I	Q
		SIN7_0		
		FRCK0_1		
		INT02_0		
		WKUP1		
		MADATA08_0		
14	11	PA9	N	I
		SOT7_0 (SDA7_0)		
		AIN1_1		
		MADATA09_0		
15	12	PAA	N	I
		SCK7_0 (SCL7_0)		
		BIN1_1		
		MADATA10_0		
16	13	PAB	E	K
		SCS70_0		
		ZIN1_1		
		INT03_0		
		MADATA11_0		
17	14	PAC	E	I
		SCS71_0		
		TIOB8_0		
		MADATA12_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
18	15	PAD	N	I
		SCK3_0 (SCL3_0)		
		TIOB9_0		
		MADATA13_0		
19	16	PAE	N	I
		ADTG_0		
		SOT3_0 (SDA3_0)		
		TIOB10_0		
		MADATA14_0		
20	17	PAF	I	K
		SIN3_0		
		TIOB11_0		
		INT16_0		
		MADATA15_0		
21	18	P08	E	K
		TIOB12_0		
		INT17_0		
		MDQM0_0		
22	19	P09	E	K
		TIOB13_0		
		INT18_0		
		MDQM1_0		
23	20	P0A	L	I
		ADTG_1		
		MCLKOUT_0		
24	-	P30	E	K
		MI2SWS1_1		
		RX0_1		
		TIOB11_2		
		INT01_2		
25	-	P31	E	I
		MI2SMCK1_1		
		TX0_1		
		TIOA12_2		
26	21	P32	L	K
		INT19_0		
		S_DATA1_0		
27	22	P33	L	I
		FRCK0_0		
		S_DATA0_0		



Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
28	23	P34	L	K
		IC03_0		
		INT00_1		
		S_CLK_0		
29	24	VCC	-	-
30	25	VSS	-	-
31	26	P35	L	K
		IC02_0		
		INT01_1		
		S_CMD_0		
32	27	P36	L	K
		IC01_0		
		INT02_1		
		S_DATA3_0		
33	28	P37	L	K
		IC00_0		
		INT03_1		
		S_DATA2_0		
34	29	P38	E	I
		ADTG_2		
		DTTIOX_0		
		S_WP_0		
35	30	P39	G	K
		RTO00_0 (PPG00_0)		
		TIOA0_1		
		AIN1_0		
		INT16_1		
		S_CD_0		
MAD24_0				
36	31	P3A	G	K
		RTO01_0 (PPG01_0)		
		TIOA1_1		
		BIN1_0		
		INT17_1		
		MAD23_0		
37	32	P3B	G	K
		RTO02_0 (PPG02_0)		
		TIOA2_1		
		ZIN1_0		
		INT18_1		
		MAD22_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
38	33	P3C	G	K
		SIN2_1		
		RTO03_0 (PPG03_0)		
		TIOA3_1		
		INT19_1		
		MAD21_0		
39	34	P3D	G	I
		SOT2_1 (SDA2_1)		
		RTO04_0 (PPG04_0)		
		TIOA4_1		
		MAD20_0		
40	35	P3E	G	I
		SCK2_1 (SCL2_1)		
		RTO05_0 (PPG05_0)		
		TIOA5_1		
		MAD19_0		
41	-	P5D	E	K
		SIN1_1		
		MI2SDI1_1		
		TIOB12_2		
		INT03_2		
42	-	P5E	E	I
		SOT1_1 (SDA1_1)		
		MI2SDO1_1		
		TIOA13_2		
43	-	P5F	E	I
		SCK1_1 (SCL1_1)		
		MI2SCK1_1		
		TIOB13_2		
44	36	VSS	-	-
45	37	VCC	-	-
46	38	P40	G	K
		SIN7_1		
		RTO10_0 (PPG10_0)		
		TIOA0_0		
		AIN0_0		
		INT23_0		
		MCSX7_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
47	39	P41	G	I
		SOT7_1 (SDA7_1)		
		RTO11_0 (PPG11_0)		
		TIOA1_0		
		BIN0_0		
		MCSX6_0		
48	40	P42	G	I
		SCK7_1 (SCL7_1)		
		RTO12_0 (PPG12_0)		
		TIOA2_0		
		ZIN0_0		
		MCSX5_0		
49	41	P43	G	K
		SCS70_1		
		RTO13_0 (PPG13_0)		
		TIOA3_0		
		INT04_0		
		MCSX4_0		
50	42	P44	G	I
		SCS71_1		
		RTO14_0 (PPG14_0)		
		TIOA4_0		
		MCSX3_0		
51	43	P45	G	I
		SCS72_1		
		RTO15_0 (PPG15_0)		
		TIOA5_0		
		MCSX2_0		
52	44	C	-	-
53	45	VSS	-	-
54	46	VCC	-	-
55	47	P46	D	S
		X0A		
56	48	P47	D	T
		X1A		
57	49	INITX	B	C

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
58	-	PF0	E	K
		SCS73_1		
		RX0_2		
		TIOA15_1		
		INT22_1		
59	-	PF1	E	K
		TX0_2		
		TIOB15_1		
		INT23_1		
60	50	P48	L	K
		SIN1_0		
		MI2SDI1_0		
		DTT11X_0		
		INT06_0		
		MRASX_0		
61	51	P49	L	I
		SOT1_0 (SDA1_0)		
		MI2SDO1_0		
		IC10_0		
		MCASX_0		
62	52	P4A	L	I
		SCK1_0 (SCL1_0)		
		MI2SCK1_0		
		IC11_0		
		MSDWEX_0		
63	53	P4B	L	K
		MI2SWS1_0		
		IC12_0		
		INT04_2		
		MCSX8_0		
64	54	P4C	L	K
		MI2SMCK1_0		
		IC13_0		
		INT05_2		
65	55	MSDCKE_0	L	K
		P4D		
		FRCK1_0		
		INT07_0		
		MSDCLK_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
66	56	P4E	L	Q
		SCK9_0 (SCL9_0)		
		INT05_0		
		WKUP2		
		MCSX1_0		
67	57	P70	L	I
		ADTG_7		
		SOT9_0 (SDA9_0)		
		MCSX0_0		
68	58	P71	I	K
		ADTG_8		
		SIN9_0		
		INT04_1		
		MRDY_0		
69	59	P72	E	I
		TIOB0_0		
		INT06_2		
		MAD00_0		
70	60	P73	E	K
		SIN8_0		
		TIOB1_0		
		INT20_0		
		MAD01_0		
71	61	P74	E	I
		SOT8_0 (SDA8_0)		
		TIOB2_0		
		MAD02_0		
72	62	P75	E	I
		SCK8_0 (SCL8_0)		
		TIOB3_0		
		MAD03_0		
73	63	P76	E	K
		SIN6_0		
		TIOB4_0		
		INT21_0		
		MAD04_0		
74	64	P77	L	I
		SOT6_0 (SDA6_0)		
		TIOB5_0		
		MAD05_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
75	65	P78	L	I
		SCK6_0 (SCL6_0)		
		AIN0_1		
		MAD06_0		
76	66	P79	E	K
		SCS60_0		
		BIN0_1		
		INT22_0		
		MAD07_0		
77	67	P7A	E	K
		SCS61_0		
		ZIN0_1		
		INT07_2		
		MAD08_0		
78	-	PF2	E	I
		SCS62_0		
		DTT11X_1		
		TIOA6_1		
		IC1_CLK_1		
79	-	PF3	E	K
		SCS63_0		
		FRCK1_1		
		TIOB6_1		
		INT05_1		
		IC1_VCC_1		
80	-	PF4	E	K
		IC10_1		
		TIOA7_1		
		INT06_1		
		IC1_VPEN_1		
81	-	PF5	E	K
		SIN3_1		
		IC11_1		
		TIOB7_1		
		INT07_1		
		IC1_RST_1		
82	-	PF6	E	K
		SOT3_1 (SDA3_1)		
		IC12_1		
		TIOA14_1		
		INT20_1		
		IC1_DATA_1		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
83	-	PF7	E	K
		SCK3_1 (SCL3_1)		
		IC13_1		
		TIOB14_1		
		INT21_1		
		IC1_CIN_1		
84	68	PE0	C	E
		MD1		
85	69	MD0	J	D
86	70	PE2	A	A
		X0		
87	71	PE3	A	B
		X1		
88	72	VSS	-	-
89	73	VCC	-	-
90	74	AVCC	-	-
91	75	AVSS	-	-
92	76	AVRL	-	-
93	77	AVRH	-	-
94	78	P10	F	M
		AN00		
		TIOA0_2		
		INT08_0		
		MNREX_0		
		IC1_CLK_0		
95	79	P11	F	L
		AN01		
		TIOB0_2		
		MNWEX_0		
		IC1_VCC_0		
96	80	P12	F	L
		AN02		
		TIOA1_2		
		MNCLE_0		
		IC1_VPEN_0		
97	81	P13	F	M
		AN03		
		SIN9_1		
		TIOB1_2		
		INT25_1		
		MNALE_0		
		IC1_RST_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
98	82	P14	F	N
		AN04		
		SOT9_1 (SDA9_1)		
		TIOA2_2		
		IC1_DATA_0		
		TRACED0		
99	83	P15	F	N
		AN05		
		SCK9_1 (SCL9_1)		
		TIOB2_2		
		IC1_CIN_0		
		TRACED1		
100	84	P16	F	O
		AN06		
		SIN6_1		
		RX0_0		
		INT09_0		
		TRACED2		
101	85	P17	F	N
		AN07		
		SOT6_1 (SDA6_1)		
		TX0_0		
		TRACED3		
102	-	PB0	F	N
		AN16		
		SCK6_1 (SCL6_1)		
		TIOA9_1		
		TRACED8		
103	-	PB1	F	O
		AN17		
		SCS60_1		
		TIOB9_1		
		AIN0_2		
		INT08_1		
		TRACED9		
104	-	PB2	F	O
		AN18		
		SCS61_1		
		TIOA10_1		
		BIN0_2		
		INT09_1		
		TRACED10		



Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
105	-	PB3	F	N
		AN19		
		SCS62_1		
		TIOB10_1		
		ZIN0_2		
		TRACED11		
106	86	P18	F	O
		AN08		
		SIN2_0		
		TIOA3_2		
		INT10_0		
		TRACED4		
107	87	P19	F	O
		AN09		
		SOT2_0 (SDA2_0)		
		TIOB3_2		
		INT24_1		
		TRACED5		
108	88	P1A	F	N
		AN10		
		SCK2_0 (SCL2_0)		
		TIOA4_2		
		TRACED6		
109	89	P1B	F	O
		AN11		
		TIOB4_2		
		INT11_0		
		TRACED7		
110	-	PB4	F	O
		AN20		
		SCS63_1		
		TIOA11_1		
		INT10_1		
		TRACED12		
111	-	PB5	F	O
		AN21		
		SIN8_1		
		TIOB11_1		
		AIN1_2		
		INT11_1		
		TRACED13		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
112	-	PB6	F	N
		AN22		
		SOT8_1 (SDA8_1)		
		TIOA12_1		
		BIN1_2		
		TRACED14		
113	-	PB7	F	N
		AN23		
		SCK8_1 (SCL8_1)		
		TIOB12_1		
		ZIN1_2		
		TRACED15		
114	90	P1C	F	N
		AN12		
		SCK0_1 (SCL0_1)		
		TIOA5_2		
		TRACECLK		
115	91	P1D	F	L
		AN13		
		SOT0_1 (SDA0_1)		
		TIOB5_2		
		MAD09_0		
116	92	P1E	F	M
		AN14		
		SIN0_1		
		TIOA8_1		
		INT26_1		
		MAD10_0		
117	93	P1F	F	M
		AN15		
		RTS5_0		
		TIOB8_1		
		INT27_1		
		MAD11_0		
118	94	P2A	F	M
		AN24		
		CTS5_0		
		INT08_2		
		MAD12_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
119	95	P29	F	M
		AN25		
		SCK5_0 (SCL5_0)		
		INT09_2		
		MAD13_0		
120	96	P28	F	M
		AN26		
		SOT5_0 (SDA5_0)		
		INT10_2		
		MAD14_0		
121	97	P27	F	M
		AN27		
		SIN5_0		
		INT24_0		
		MAD15_0		
122	98	P26	E	M
		ADTG_6		
		TIOA6_2		
		INT11_2		
		MAD16_0		
123	99	P25	F	M
		AN28		
		TIOB6_2		
		INT25_0		
		MAD17_0		
124	100	P24	F	L
		AN29		
		TIOA13_1		
		MAD18_0		
125	101	P23	F	L
		UHCONX1		
		AN30		
		SCK0_0 (SCL0_0)		
		TIOB13_1		
126	102	P22	E	M
		AN31		
		SOT0_0 (SDA0_0)		
		INT26_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
127	103	P21	I	K
		ADTG_4		
		SIN0_0		
		INT27_0		
		CROUT_0		
128	104	P20	I	F
		NMIX		
		WKUP0		
129	105	USBVCC1	-	-
130	106	P82	H	R
		UDM1		
131	107	P83	H	R
		UDP1		
132	108	VSS	-	-
133	109	VCC	-	-
134	110	P00	E	G
		TRSTX		
135	111	P01	E	G
		TCK		
		SWCLK		
136	112	P02	E	G
		TDI		
137	113	P03	E	G
		TMS		
		SWDIO		
138	114	P04	E	G
		TDO		
		SWO		
139	-	P90	E	K
		RTO10_1 (PPG10_1)		
		TIOB0_1		
		INT12_1		
		IC0_CLK_1		
140	-	P91	E	K
		SIN5_1		
		RTO11_1 (PPG11_1)		
		TIOB1_1		
		INT13_1		
		IC0_VCC_1		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
141	-	P92	E	K
		SOT5_1 (SDA5_1)		
		RTO12_1 (PPG12_1)		
		TIOB2_1		
		INT14_1		
		IC0_VPEN_1		
142	-	P93	E	K
		SCK5_1 (SCL5_1)		
		RTO13_1 (PPG13_1)		
		TIOB3_1		
		INT15_1		
		IC0_RST_1		
143	-	P94	E	I
		CTS5_1		
		RTO14_1 (PPG14_1)		
		TIOB4_1		
		IC0_DATA_1		
144	-	P95	E	I
		RTS5_1		
		RTO15_1 (PPG15_1)		
		TIOB5_1		
		IC0_CIN_1		
145	115	PC0	K	V
		E_RXER		
146	116	PC1	K	V
		TIOB6_0		
		E_RX03		
147	117	PC2	K	V
		TIOA6_0		
		E_RX02		
148	118	PC3	K	V
		TIOB7_0		
		E_RX01		
149	119	PC4	K	V
		TIOA7_0		
		E_RX00		
150	120	PC5	K	V
		TIOB14_0		
		E_RXDV		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
151	121	PC6	K	V
		TIOA14_0		
		E_MDIO		
152	122	PC7	E	W
		INT13_0		
		E_MDC		
		CROUT_1		
153	123	PC8	K	V
		E_RXCK_REFCK		
154	124	PC9	K	V
		TIOB15_0		
		E_COL		
155	125	PCA	K	V
		TIOA15_0		
		E_CRS		
156	126	ETHVCC	-	-
157	127	VSS	-	-
158	128	PCB	L	W
		INT28_0		
		E_COUT		
159	129	PCC	K	V
		E_TCK		
160	130	PCD	L	W
		SOT4_1 (SDA4_1)		
		INT14_0		
		E_TXER		
161	131	PCE	L	W
		SIN4_1		
		INT15_0		
		E_TX03		
162	132	PCF	L	W
		RTS4_1		
		INT12_0		
		E_TX02		
163	133	PD0	L	W
		INT30_1		
		E_TX01		
164	134	PD1	L	W
		INT31_1		
		E_TX00		
165	135	PD2	L	V
		CTS4_1		
		E_TXEN		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
166	136	P6E	E	W
		ADTG_5		
		SCK4_1 (SCL4_1)		
		INT29_0		
		E_PPS		
167	-	P65	E	K
		INT28_1		
168	-	P64	I	K
		CTS4_0		
		INT29_1		
169	137	P63	L	K
		ADTG_3		
		RTS4_0		
		INT30_0		
		MOEX_0		
170	138	P62	L	I
		SCK4_0 (SCL4_0)		
		TIOB7_2		
		MWEX_0		
171	139	P61	L	I
		UHCONX0		
		SOT4_0 (SDA4_0)		
		TIOA7_2		
		MALE_0		
		RTCCO_0		
		SUBOUT_0		
172	140	P60	I	Q
		SIN4_0		
		INT31_0		
		WKUP3		
173	141	USBVCC0	-	-
174	142	P80	H	R
		UDM0		
175	143	P81	H	R
		UDP0		
176	144	VSS	-	-

**Signal Descriptions**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
A/D converter	ADTG_0	A/D converter external trigger input pin	19	16
	ADTG_1		23	20
	ADTG_2		34	29
	ADTG_3		169	137
	ADTG_4		127	103
	ADTG_5		166	136
	ADTG_6		122	98
	ADTG_7		67	57
	ADTG_8		68	58
	AN00	A/D converter analog input pin. ANxx describes A/D converter ch xx.	94	78
	AN01		95	79
	AN02		96	80
	AN03		97	81
	AN04		98	82
	AN05		99	83
	AN06		100	84
	AN07		101	85
	AN08		106	86
	AN09		107	87
	AN10		108	88
	AN11		109	89
	AN12		114	90
	AN13		115	91
	AN14		116	92
	AN15		117	93
	AN16		102	-
	AN17		103	-
	AN18		104	-
	AN19		105	-
	AN20		110	-
	AN21		111	-
	AN22		112	-
	AN23		113	-
AN24	118		94	
AN25	119		95	
AN26	120		96	
AN27	121		97	
AN28	123		99	
AN29	124		100	
AN30	125		101	
AN31	126	102		



Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Base Timer 0	TIOA0_0	Base Timer ch 0 TIOA pin	46	38
	TIOA0_1		35	30
	TIOA0_2		94	78
	TIOB0_0	Base Timer ch 0 TIOB pin	69	59
	TIOB0_1		139	-
	TIOB0_2		95	79
Base Timer 1	TIOA1_0	Base Timer ch 1 TIOA pin	47	39
	TIOA1_1		36	31
	TIOA1_2		96	80
	TIOB1_0	Base Timer ch 1 TIOB pin	70	60
	TIOB1_1		140	-
	TIOB1_2		97	81
Base Timer 2	TIOA2_0	Base Timer ch 2 TIOA pin	48	40
	TIOA2_1		37	32
	TIOA2_2		98	82
	TIOB2_0	Base Timer ch 2 TIOB pin	71	61
	TIOB2_1		141	-
	TIOB2_2		99	83
Base Timer 3	TIOA3_0	Base Timer ch 3 TIOA pin	49	41
	TIOA3_1		38	33
	TIOA3_2		106	86
	TIOB3_0	Base Timer ch 3 TIOB pin	72	62
	TIOB3_1		142	-
	TIOB3_2		107	87
Base Timer 4	TIOA4_0	Base Timer ch 4 TIOA pin	50	42
	TIOA4_1		39	34
	TIOA4_2		108	88
	TIOB4_0	Base Timer ch 4 TIOB pin	73	63
	TIOB4_1		143	-
	TIOB4_2		109	89
Base Timer 5	TIOA5_0	Base Timer ch 5 TIOA pin	51	43
	TIOA5_1		40	35
	TIOA5_2		114	90
	TIOB5_0	Base Timer ch 5 TIOB pin	74	64
	TIOB5_1		144	-
	TIOB5_2		115	91
Base Timer 6	TIOA6_0	Base Timer ch 6 TIOA pin	147	117
	TIOA6_1		78	-
	TIOA6_2		122	98
	TIOB6_0	Base Timer ch 6 TIOB pin	146	116
	TIOB6_1		79	-
	TIOB6_2		123	99

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	149	119
	TIOA7_1		80	-
	TIOA7_2		171	139
	TIOB7_0	Base Timer ch 7 TIOB pin	148	118
	TIOB7_1		81	-
	TIOB7_2		170	138
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2
	TIOA8_1		116	92
	TIOA8_2		10	-
	TIOB8_0	Base Timer ch 8 TIOB pin	17	14
	TIOB8_1		117	93
	TIOB8_2		11	-
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3
	TIOA9_1		102	-
	TIOA9_2		12	-
	TIOB9_0	Base Timer ch 9 TIOB pin	18	15
	TIOB9_1		103	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4
	TIOA10_1		104	-
	TIOB10_0	Base Timer ch 10 TIOB pin	19	16
	TIOB10_1		105	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5
	TIOA11_1		110	-
	TIOB11_0	Base Timer ch 11 TIOB pin	20	17
	TIOB11_1		111	-
	TIOB11_2		24	-
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6
	TIOA12_1		112	-
	TIOA12_2		25	-
	TIOB12_0	Base Timer ch 12 TIOB pin	21	18
	TIOB12_1		113	-
	TIOB12_2		41	-
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7
	TIOA13_1		124	100
	TIOA13_2		42	-
	TIOB13_0	Base Timer ch 13 TIOB pin	22	19
	TIOB13_1		125	101
	TIOB13_2		43	-
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	151	121
	TIOA14_1		82	-
	TIOB14_0	Base Timer ch 14 TIOB pin	150	120
	TIOB14_1		83	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	155	125
	TIOA15_1		58	-
	TIOB15_0	Base timer ch 15 TIOB pin	154	124
	TIOB15_1		59	-
CAN 0	TX0_0	CAN interface ch 0 TX output pin	101	85
	TX0_1		25	-
	TX0_2		59	-
	RX0_0	CAN interface ch 0 RX input pin	100	84
	RX0_1		24	-
	RX0_2		58	-
Debugger	SWCLK	Serial wire debug interface clock input pin	135	111
	SWDIO	Serial wire debug interface data input/output pin	137	113
	SWO	Serial wire viewer output pin	138	114
	TCK	JTAG test clock input pin	135	111
	TDI	JTAG test data input pin	136	112
	TDO	JTAG debug data output pin	138	114
	TMS	JTAG test mode state input/output pin	137	113
	TRACECLK	Trace CLK output pin of ETM/HTM	114	90
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	98	82
	TRACED1		99	83
	TRACED2	Trace data output pin of HTM	100	84
	TRACED3		101	85
	TRACED4		106	86
	TRACED5		107	87
	TRACED6		108	88
	TRACED7		109	89
	TRACED8		102	-
	TRACED9		103	-
	TRACED10		104	-
	TRACED11		105	-
	TRACED12		110	-
	TRACED13		111	-
	TRACED14		112	-
	TRACED15		113	-
	TRSTX		JTAG test reset Input pin	134

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MAD00_0	External bus interface address bus	69	59
	MAD01_0		70	60
	MAD02_0		71	61
	MAD03_0		72	62
	MAD04_0		73	63
	MAD05_0		74	64
	MAD06_0		75	65
	MAD07_0		76	66
	MAD08_0		77	67
	MAD09_0		115	91
	MAD10_0		116	92
	MAD11_0		117	93
	MAD12_0		118	94
	MAD13_0		119	95
	MAD14_0		120	96
	MAD15_0		121	97
	MAD16_0		122	98
	MAD17_0		123	99
	MAD18_0		124	100
	MAD19_0		40	35
	MAD20_0		39	34
	MAD21_0		38	33
	MAD22_0		37	32
	MAD23_0		36	31
	MAD24_0	35	30	
	MCSX0_0	External bus interface chip select output pin	67	57
	MCSX1_0		66	56
	MCSX2_0		51	43
MCSX3_0	50		42	
MCSX4_0	49		41	
MCSX5_0	48		40	
MCSX6_0	47		39	
MCSX7_0	46		38	
MCSX8_0	63	53		

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2
	MADATA01_0		3	3
	MADATA02_0		4	4
	MADATA03_0		5	5
	MADATA04_0		6	6
	MADATA05_0		7	7
	MADATA06_0		8	8
	MADATA07_0		9	9
	MADATA08_0		13	10
	MADATA09_0		14	11
	MADATA10_0		15	12
	MADATA11_0		16	13
	MADATA12_0		17	14
	MADATA13_0		18	15
	MADATA14_0		19	16
	MADATA15_0		20	17
	MDQM0_0	External bus interface byte mask signal output pin	21	18
	MDQM1_0		22	19
	MALE_0	External bus interface address latch enable output signal for multiplex	171	139
	MRDY_0	External bus interface external RDY input signal	68	58
	MCLKOUT_0	External bus interface external clock output pin	23	20
	MNALE_0	External bus interface ALE signal to control NAND flash output pin	97	81
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	96	80
	MNREX_0	External bus interface read enable signal to control NAND flash	94	78
	MNWEX_0	External bus interface write enable signal to control NAND flash	95	79
	MOEX_0	External bus interface read enable signal for SRAM	169	137
	MWEX_0	External bus interface write enable signal for SRAM	170	138
	MSDCLK_0	SDRAM interface SDRAM clock output pin	65	55
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	64	54
	MRASX_0	SDRAM interface SDRAM row active strobe pin	60	50
	MCASX_0	SDRAM interface SDRAM column active strobe pin	61	51
	MSDWEX_0	SDRAM interface SDRAM write enable pin	62	52

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External interrupt	INT00_0	External interrupt request 00 input pin	2	2
	INT00_1		28	23
	INT00_2		8	8
	INT01_0	External interrupt request 01 input pin	7	7
	INT01_1		31	26
	INT01_2		24	-
	INT02_0	External interrupt request 02 input pin	13	10
	INT02_1		32	27
	INT02_2		9	9
	INT03_0	External interrupt request 03 input pin	16	13
	INT03_1		33	28
	INT03_2		41	-
	INT04_0	External interrupt request 04 input pin	49	41
	INT04_1		68	58
	INT04_2		63	53
	INT05_0	External interrupt request 05 input pin	66	56
	INT05_1		79	-
	INT05_2		64	54
	INT06_0	External interrupt request 06 input pin	60	50
	INT06_1		80	-
	INT06_2		69	59
	INT07_0	External interrupt request 07 input pin	65	55
	INT07_1		81	-
	INT07_2		77	67
	INT08_0	External interrupt request 08 input pin	94	78
	INT08_1		103	-
	INT08_2		118	94
	INT09_0	External interrupt request 09 input pin	100	84
	INT09_1		104	-
	INT09_2		119	95
	INT10_0	External interrupt request 10 input pin	106	86
	INT10_1		110	-
	INT10_2		120	96
	INT11_0	External interrupt request 11 input pin	109	89
	INT11_1		111	-
	INT11_2		122	98
	INT12_0	External interrupt request 12 input pin	162	132
	INT12_1		139	-
	INT13_0	External interrupt request 13 input pin	152	122
	INT13_1		140	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External interrupt	INT14_0	External interrupt request 14 input pin	160	130
	INT14_1		141	-
	INT15_0	External interrupt request 15 input pin	161	131
	INT15_1		142	-
	INT16_0	External interrupt request 16 input pin	20	17
	INT16_1		35	30
	INT17_0	External interrupt request 17 input pin	21	18
	INT17_1		36	31
	INT18_0	External interrupt request 18 input pin	22	19
	INT18_1		37	32
	INT19_0	External interrupt request 19 input pin	26	21
	INT19_1		38	33
	INT20_0	External interrupt request 20 input pin	70	60
	INT20_1		82	-
	INT21_0	External interrupt request 21 input pin	73	63
	INT21_1		83	-
	INT22_0	External interrupt request 22 input pin	76	66
	INT22_1		58	-
	INT23_0	External interrupt request 23 input pin	46	38
	INT23_1		59	-
	INT24_0	External interrupt request 24 input pin	121	97
	INT24_1		107	87
	INT25_0	External interrupt request 25 input pin	123	99
	INT25_1		97	81
	INT26_0	External interrupt request 26 input pin	126	102
	INT26_1		116	92
	INT27_0	External interrupt request 27 input pin	127	103
	INT27_1		117	93
	INT28_0	External interrupt request 28 input pin	158	128
	INT28_1		167	-
	INT29_0	External interrupt request 29 input pin	166	136
	INT29_1		168	-
	INT30_0	External interrupt request 30 input pin	169	137
INT30_1	163		133	
INT31_0	External interrupt request 31 input pin	172	140	
INT31_1		164	134	
NMIX	Non-maskable interrupt input pin	128	104	

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P00	General-purpose I/O port 0	134	110
	P01		135	111
	P02		136	112
	P03		137	113
	P04		138	114
	P08		21	18
	P09		22	19
	P0A		23	20
	P10	General-purpose I/O port 1	94	78
	P11		95	79
	P12		96	80
	P13		97	81
	P14		98	82
	P15		99	83
	P16		100	84
	P17		101	85
	P18		106	86
	P19		107	87
	P1A		108	88
	P1B		109	89
	P1C	114	90	
	P1D	115	91	
	P1E	116	92	
	P1F	117	93	
	P20	General-purpose I/O port 2	128	104
	P21		127	103
	P22		126	102
	P23		125	101
	P24		124	100
	P25		123	99
P26	122		98	
P27	121		97	
P28	120		96	
P29	119		95	
P2A	118	94		



Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P30	General-purpose I/O port 3	24	-
	P31		25	-
	P32		26	21
	P33		27	22
	P34		28	23
	P35		31	26
	P36		32	27
	P37		33	28
	P38		34	29
	P39		35	30
	P3A		36	31
	P3B		37	32
	P3C		38	33
	P3D		39	34
	P3E		40	35
	P40	General-purpose I/O port 4	46	38
	P41		47	39
	P42		48	40
	P43		49	41
	P44		50	42
	P45		51	43
	P46		55	47
	P47		56	48
	P48		60	50
	P49		61	51
	P4A		62	52
	P4B		63	53
	P4C		64	54
	P4D		65	55
	P4E		66	56
	P50	General-purpose I/O port 5	10	-
	P51		11	-
	P52		12	-
P5D	41		-	
P5E	42		-	
P5F	43		-	
P60	General-purpose I/O port 6	172	140	
P61		171	139	
P62		170	138	
P63		169	137	
P64		168	-	
P65		167	-	
P6E		166	136	

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P70	General-purpose I/O port 7	67	57
	P71		68	58
	P72		69	59
	P73		70	60
	P74		71	61
	P75		72	62
	P76		73	63
	P77		74	64
	P78		75	65
	P79		76	66
	P7A		77	67
	P80	General-purpose I/O port 8	174	142
	P81		175	143
	P82		130	106
	P83		131	107
	P90	General-purpose I/O port 9	139	-
	P91		140	-
	P92		141	-
	P93		142	-
	P94		143	-
	P95		144	-
	PA0	General-purpose I/O port A	2	2
	PA1		3	3
	PA2		4	4
	PA3		5	5
	PA4		6	6
	PA5		7	7
	PA6		8	8
	PA7		9	9
	PA8		13	10
	PA9		14	11
	PAA		15	12
PAB	16		13	
PAC	17		14	
PAD	18		15	
PAE	19	16		
PAF	20	17		

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	PB0	General-purpose I/O port B	102	-
	PB1		103	-
	PB2		104	-
	PB3		105	-
	PB4		110	-
	PB5		111	-
	PB6		112	-
	PB7		113	-
GPIO	PC0	General-purpose I/O port C	145	115
	PC1		146	116
	PC2		147	117
	PC3		148	118
	PC4		149	119
	PC5		150	120
	PC6		151	121
	PC7		152	122
	PC8		153	123
	PC9		154	124
	PCA		155	125
	PCB		158	128
	PCC		159	129
	PCD		160	130
	PCE		161	131
	PCF		162	132
	PD0	General-purpose I/O port D	163	133
	PD1		164	134
	PD2		165	135
	PE0	General-purpose I/O port E	84	68
	PE2		86	70
	PE3		87	71
	PF0	General-purpose I/O port F	58	-
	PF1		59	-
	PF2		78	-
	PF3		79	-
	PF4		80	-
	PF5		81	-
PF6	82		-	
PF7	83		-	

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 0	SIN0_0	Multi-function serial interface ch 0 input pin	127	103
	SIN0_1		116	92
	SOT0_0 (SDA0_0)	Multi-function serial interface ch 0 output pin This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I <sup>2</sup> C (operation mode 4).	126	102
	SOT0_1 (SDA0_1)		115	91
	SCK0_0 (SCL0_0)	Multi-function serial interface ch 0 clock I/O pin This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I <sup>2</sup> C (operation mode 4)	125	101
	SCK0_1 (SCL0_1)		114	90
Multi-Function Serial 1	SIN1_0 (MI2SDI1_0)	Multi-function serial interface ch 1 input pin.	60	50
	SIN1_1 (MI2SDI1_1)	SIN1 pin operates as MI2SDI1 when used as an I <sup>2</sup> S pin (operation mode 2).	41	-
	SOT1_0 (SDA1_0) (MI2SDO1_0)	Multi-function serial interface ch 1 output pin This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I <sup>2</sup> C (operation mode 4).	61	51
	SOT1_1 (SDA1_1) (MI2SDO1_1)		SOT1 pin operates as MI2SDO1 when used as an I <sup>2</sup> S pin (operation mode 2).	42
	SCK1_0 (SCL1_0) (MI2SCK1_0)	Multi-function serial interface ch 1 clock I/O pin This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I <sup>2</sup> C (operation mode 4).	62	52
	SCK1_1 (SCL1_1) (MI2SCK1_1)		SCK1 pin operates as MI2SCK1 when used as an I <sup>2</sup> S pin (operation mode 2).	43
	MI2SWS1_0	I <sup>2</sup> S word select (WS) output pin	63	53
	MI2SWS1_1		24	-
	MI2SMCK1_0	I <sup>2</sup> S master clock I/O pin	64	54
	MI2SMCK1_1		25	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 2	SIN2_0	Multi-function serial interface ch 2 input pin	106	86
	SIN2_1		38	33
	SOT2_0 (SDA2_0)	Multi-function serial interface ch 2 output pin	107	87
	SOT2_1 (SDA2_1)	This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I <sup>2</sup> C (operation mode 4).	39	34
	SCK2_0 (SCL2_0)	Multi-function serial interface ch 2 clock I/O pin	108	88
	SCK2_1 (SCL2_1)	This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I <sup>2</sup> C (operation mode 4).	40	35
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	20	17
	SIN3_1		81	-
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin	19	16
	SOT3_1 (SDA3_1)	This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I <sup>2</sup> C (operation mode 4).	82	-
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin	18	15
	SCK3_1 (SCL3_1)	This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I <sup>2</sup> C (operation mode 4).	83	-
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	172	140
	SIN4_1		161	131
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin	171	139
	SOT4_1 (SDA4_1)	This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I <sup>2</sup> C (operation mode 4).	160	130
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin	170	138
	SCK4_1 (SCL4_1)	This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I <sup>2</sup> C (operation mode 4).	166	136
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	168	-
	CTS4_1		165	135
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	169	137
	RTS4_1		162	132

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	121	97
	SIN5_1		140	-
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin	120	96
	SOT5_1 (SDA5_1)	This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I <sup>2</sup> C (operation mode 4).	141	-
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin	119	95
	SCK5_1 (SCL5_1)	This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I <sup>2</sup> C (operation mode 4).	142	-
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	118	94
	CTS5_1		143	-
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	117	93
	RTS5_1		144	-
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	73	63
	SIN6_1		100	84
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin	74	64
	SOT6_1 (SDA6_1)	This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I <sup>2</sup> C (operation mode 4).	101	85
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin	75	65
	SCK6_1 (SCL6_1)	This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I <sup>2</sup> C (operation mode 4).	102	-
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	76	66
	SCS60_1		103	-
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	77	67
	SCS61_1		104	-
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	78	-
	SCS62_1		105	-
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	79	-
	SCS63_1		110	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Multi-Function Serial 7	SIN7_0	Multi-function serial interface ch 7 input pin	13	10
	SIN7_1		46	38
	SOT7_0 (SDA7_0)	Multi-function serial interface ch 7 output pin	14	11
	SOT7_1 (SDA7_1)	This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I <sup>2</sup> C (operation mode 4).	47	39
	SCK7_0 (SCL7_0)	Multi-function serial interface ch 7 clock I/O pin	15	12
	SCK7_1 (SCL7_1)	This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I <sup>2</sup> C (operation mode 4).	48	40
	SCS70_0	Multi-function serial interface ch 7 chip select 0 input/output pin	16	13
	SCS70_1		49	41
	SCS71_0	Multi-function serial interface ch 7 chip select 1 input/output pin	17	14
	SCS71_1		50	42
	SCS72_0	Multi-function serial interface ch 7 chip select 2 input/output pin	10	-
	SCS72_1		51	43
	SCS73_0	Multi-function serial interface ch 7 chip select 3 input/output pin	11	-
	SCS73_1		58	-
Multi-Function Serial 8	SIN8_0	Multi-function serial interface ch 8 input pin	70	60
	SIN8_1		111	-
	SOT8_0 (SDA8_0)	Multi-function serial interface ch 8 output pin	71	61
	SOT8_1 (SDA8_1)	This pin operates as SOT8 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA8 when it is used in an I <sup>2</sup> C (operation mode 4).	112	-
	SCK8_0 (SCL8_0)	Multi-function serial interface ch 8 clock I/O pin	72	62
	SCK8_1 (SCL8_1)	This pin operates as SCK8 when it is used in a CSIO (operation mode 2) and as SCL8 when it is used in an I <sup>2</sup> C (operation mode 4).	113	-
Multi-Function Serial 9	SIN9_0	Multi-function serial interface ch 9 input pin	68	58
	SIN9_1		97	81
	SOT9_0 (SDA9_0)	Multi-function serial interface ch 9 output pin	67	57
	SOT9_1 (SDA9_1)	This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I <sup>2</sup> C (operation mode 4).	98	82
	SCK9_0 (SCL9_0)	Multi-function serial interface ch 9 clock I/O pin	66	56
	SCK9_1 (SCL9_1)	This pin operates as SCK9 when it is used in a CSIO (operation mode 2) and as SCL9 when it is used in an I <sup>2</sup> C (operation mode 4).	99	83

Module	Pin Name	Function	Pin Number		
			LQFP 176	LQFP 144	
Multi-Function Timer 0	DTTI0X_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	34	29	
	DTTI0X_1		8	8	
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	27	22	
	FRCK0_1		13	10	
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	33	28	
	IC00_1		9	9	
	IC01_0		32	27	
	IC01_1		10	-	
	IC02_0		31	26	
	IC02_1		11	-	
	IC03_0		28	23	
	IC03_1		12	-	
	RTO00_0 (PPG00_0)		Waveform generator output pin of Multi-Function Timer 0.	35	30
	RTO00_1 (PPG00_1)		This pin operates as PPG00 when it is used in PPG0 output modes.	2	2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0.	36	31	
	RTO01_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output modes.	3	3	
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	37	32	
	RTO02_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	4	4	
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	38	33	
	RTO03_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	5	5	
RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	39	34		
RTO04_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	6	6		
RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	40	35		
RTO05_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	7	7		



Module	Pin Name	Function	Pin Number		
			LQFP 176	LQFP 144	
Multi-Function Timer 1	DTTI1X_0	Input signal controlling waveform generator outputs RTO10 to RTO15 of Multi-Function Timer 1.	60	50	
	DTTI1X_1		78	-	
	FRCK1_0	16-bit free-run timer ch 1 external clock input pin	65	55	
	FRCK1_1		79	-	
	IC10_0	16-bit input capture input pin of Multi-Function Timer 1. ICxx describes channel number.	61	51	
	IC10_1		80	-	
	IC11_0		62	52	
	IC11_1		81	-	
	IC12_0		63	53	
	IC12_1		82	-	
	IC13_0		64	54	
	IC13_1		83	-	
	RTO10_0 (PPG10_0)		Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	46	38
	RTO10_1 (PPG10_1)			139	-
	RTO11_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	47	39	
	RTO11_1 (PPG10_1)		140	-	
	RTO12_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	48	40	
	RTO12_1 (PPG12_1)		141	-	
	RTO13_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	49	41	
	RTO13_1 (PPG12_1)		142	-	
RTO14_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	50	42		
RTO14_1 (PPG14_1)		143	-		
RTO15_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	51	43		
RTO15_1 (PPG14_1)		144	-		

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch 0 AIN input pin	46	38
	AIN0_1		75	65
	AIN0_2		103	-
	BIN0_0	QPRC ch 0 BIN input pin	47	39
	BIN0_1		76	66
	BIN0_2		104	-
	ZIN0_0	QPRC ch 0 ZIN input pin	48	40
	ZIN0_1		77	67
	ZIN0_2		105	-
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch 1 AIN input pin	35	30
	AIN1_1		14	11
	AIN1_2		111	-
	BIN1_0	QPRC ch 1 BIN input pin	36	31
	BIN1_1		15	12
	BIN1_2		112	-
	ZIN1_0	QPRC ch 1 ZIN input pin	37	32
	ZIN1_1		16	13
	ZIN1_2		113	-
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	171	139
	RTCCO_1		9	9
	SUBOUT_0	Sub-clock output pin	171	139
	SUBOUT_1		9	9
USB0	UDM0	USB ch 0 function/host D – pin	174	142
	UDP0	USB ch 0 function/host D + pin	175	143
	UHCONX0	USB ch 0 external pull-up control pin	171	139
USB1	UDM1	USB ch 1 function/host D – pin	130	106
	UDP1	USB ch 1 function/host D + pin	131	107
	UHCONX1	USB ch 1 external pull-up control pin	125	101
Low power consumption mode	WKUP0	Deep standby mode return signal input pin 0	128	104
	WKUP1	Deep standby mode return signal input pin 1	13	10
	WKUP2	Deep standby mode return signal input pin 2	66	56
	WKUP3	Deep standby mode return signal input pin 3	172	140

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	28	23
	S_CMD_0	SD memory card interface SD memory card command output	31	26
	S_DATA1_0	SD memory card interface SD memory card data bus	26	21
	S_DATA0_0		27	22
	S_DATA3_0		32	27
	S_DATA2_0		33	28
	S_CD_0	SD memory card interface SD memory card detection pin	35	30
S_WP_0	SD memory card interface SD memory card write protection	34	29	
Ethernet	E_COL	Collision detection	154	124
	E_COUT	Clock output for Ethernet PHY	158	128
	E_CRS	Carrier detection	155	125
	E_MDC	Management clock	152	122
	E_MDIO	Management data I/O	151	121
	E_PPS	PTP counter monitor	166	136
	E_RX00	Received data0	149	119
	E_RX01	Received data1	148	118
	E_RX02	Received data2	147	117
	E_RX03	Received data3	146	116
	E_RXCK_RE FCK	Received clock input/ Reference clock	153	123
	E_RXDV	Received data enable	150	120
	E_RXER	Received data error detection	145	115
	E_TCK	Transition clock input	159	129
	E_TX00	Transition data0	164	134
	E_TX01	Transition data1	163	133
	E_TX02	Transition data2	162	132
	E_TX03	Transition data3	161	131
E_TXEN	Transition data enable	165	135	
E_TXER	Transition data error detection	160	130	

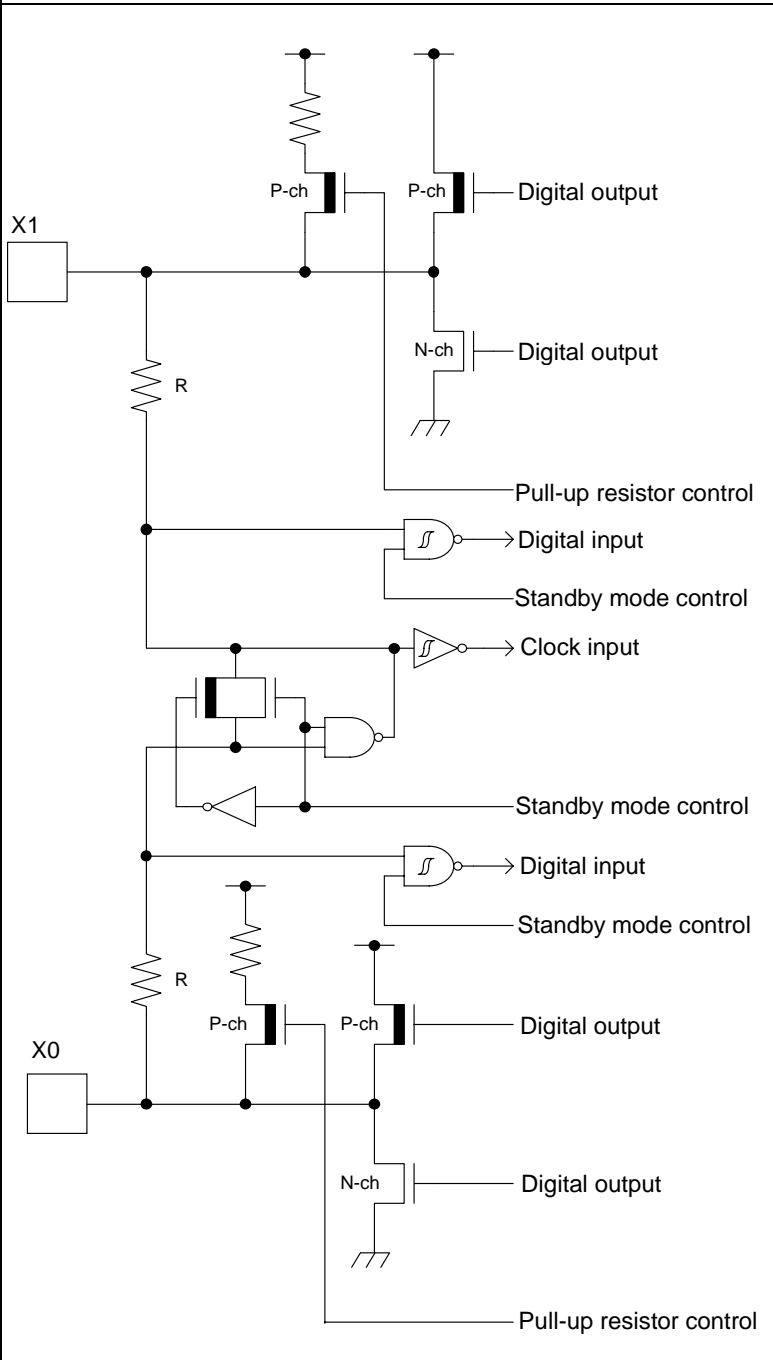
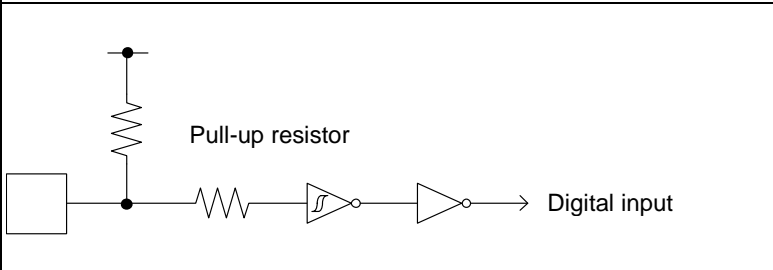
Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Smartcard0	IC0_VCC_0	Smartcard ch 0 power enable output pin	6	6
	IC0_VCC_1		140	-
	IC0_VPEN_0	Smartcard ch 0 programming output pin	5	5
	IC0_VPEN_1		141	-
	IC0_RST_0	Smartcard ch 0 reset output pin	4	4
	IC0_RST_1		142	-
	IC0_CIN_0	Smartcard ch 0 insert detection input pin	2	2
	IC0_CIN_1		144	-
	IC0_CLK_0	Smartcard ch 0 serial interface clock output pin	7	7
	IC0_CLK_1		139	-
	IC0_DATA_0	Smartcard ch 0 serial interface data I/O pin	3	3
	IC0_DATA_1		143	-
Smartcard1	IC1_VCC_0	Smartcard ch 1 power enable output pin	95	79
	IC1_VCC_1		79	-
	IC1_VPEN_0	Smartcard ch 1 programming output pin	96	80
	IC1_VPEN_1		80	-
	IC1_RST_0	Smartcard ch 1 reset output pin	97	81
	IC1_RST_1		81	-
	IC1_CIN_0	Smartcard ch 1 insert detection input pin	99	83
	IC1_CIN_1		83	-
	IC1_CLK_0	Smartcard ch 1 serial interface clock output pin	94	78
	IC1_CLK_1		78	-
	IC1_DATA_0	Smartcard ch 1 serial interface data I/O pin	98	82
	IC1_DATA_1		82	-

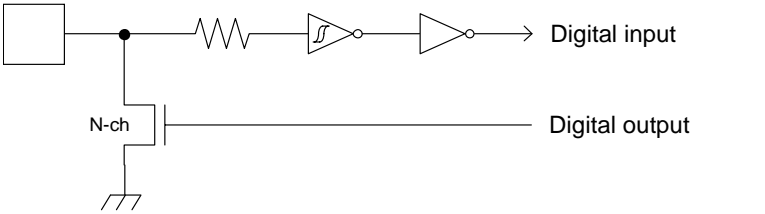
Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Reset	INITX	External reset Input pin A reset is valid when INITX = L.	57	49
Mode	MD1	Mode 1 pin During serial programming to flash memory, MD1 = L must be input.	84	68
	MD0	Mode 0 pin During normal operation, MD0 = L must be input. During serial programming to flash memory, MD0 = H must be input.	85	69
Power	VCC	Power supply pin	1	1
			29	24
			45	37
			54	46
			89	73
			133	109
	USBVCC0	3.3V power supply port for USB I/O	173	141
USBVCC1		129	105	
ETHVCC	Power supply pin for Ethernet I/O	156	126	
GND	VSS	GND pin	30	25
			44	36
			53	45
			88	72
			132	108
			157	127
			176	144
Clock	X0	Main clock (oscillation) input pin	86	70
	X1	Main clock (oscillation) I/O pin	87	71
	X0A	Sub clock (oscillation) input pin	55	47
	X1A	Sub clock (oscillation) I/O pin	56	48
	CROUT_0	Built-in high-speed CR-oscillation clock output port	127	103
	CROUT_1		152	122
Analog power	AVCC	A/D converter and D/A converter analog power-supply pin	90	74
	AVRL	A/D converter analog reference voltage input pin	92	76
	AVRH	A/D converter analog reference voltage input pin	93	77
Analog GND	AVSS	A/D converter and D/A converter GND pin	91	75
C pin	C	Power supply stabilization capacity pin	52	44

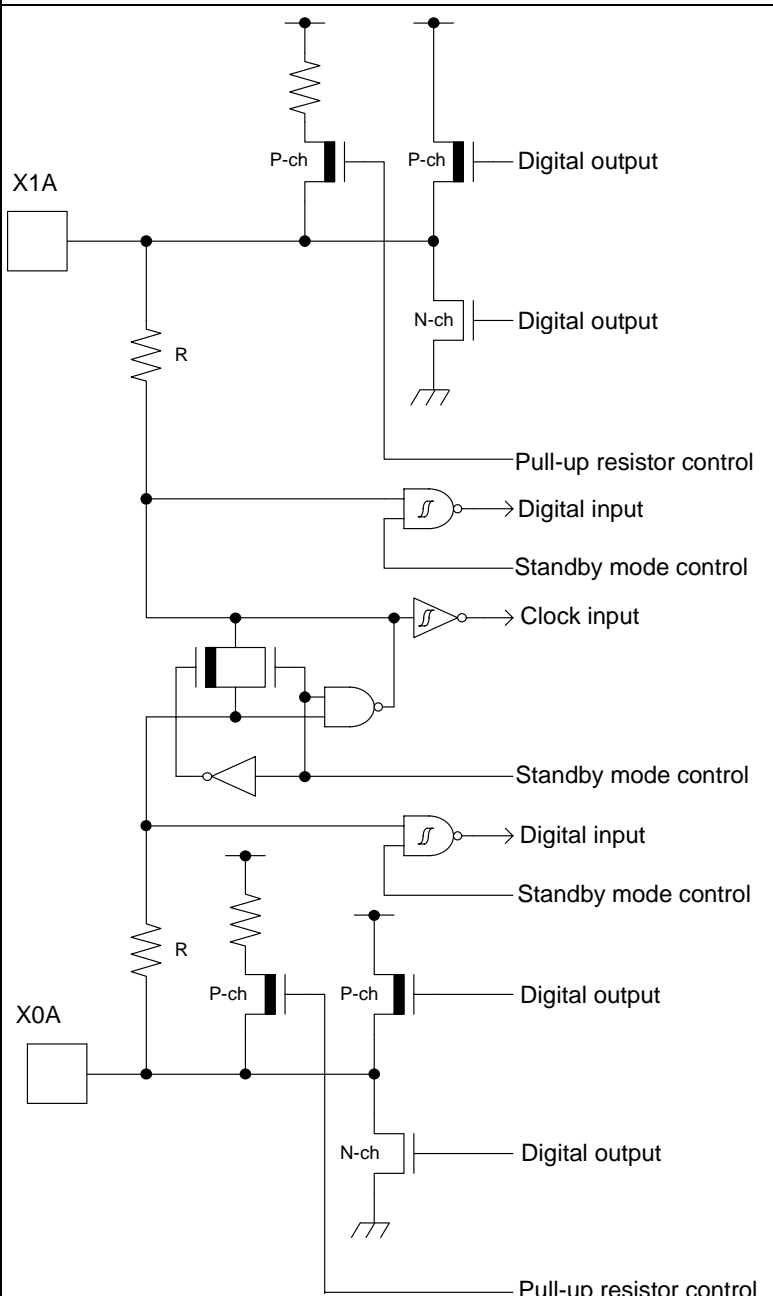
**Notes:**

- While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.

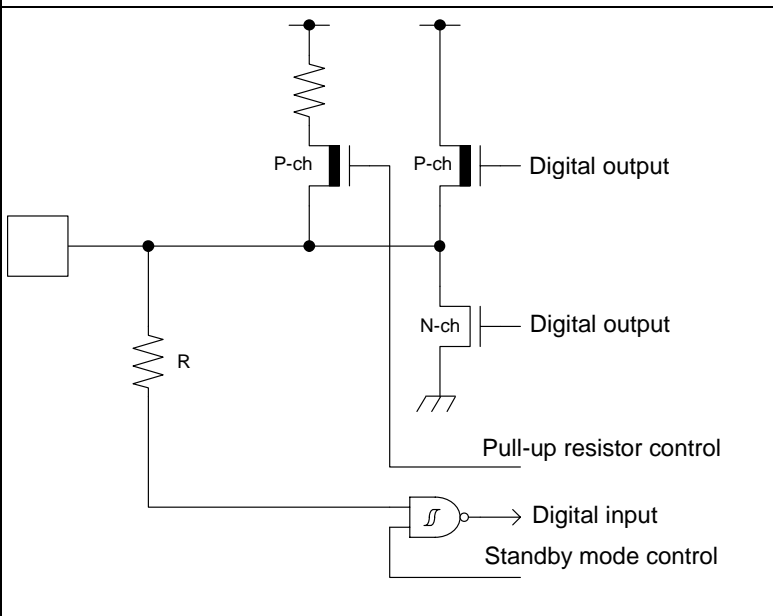
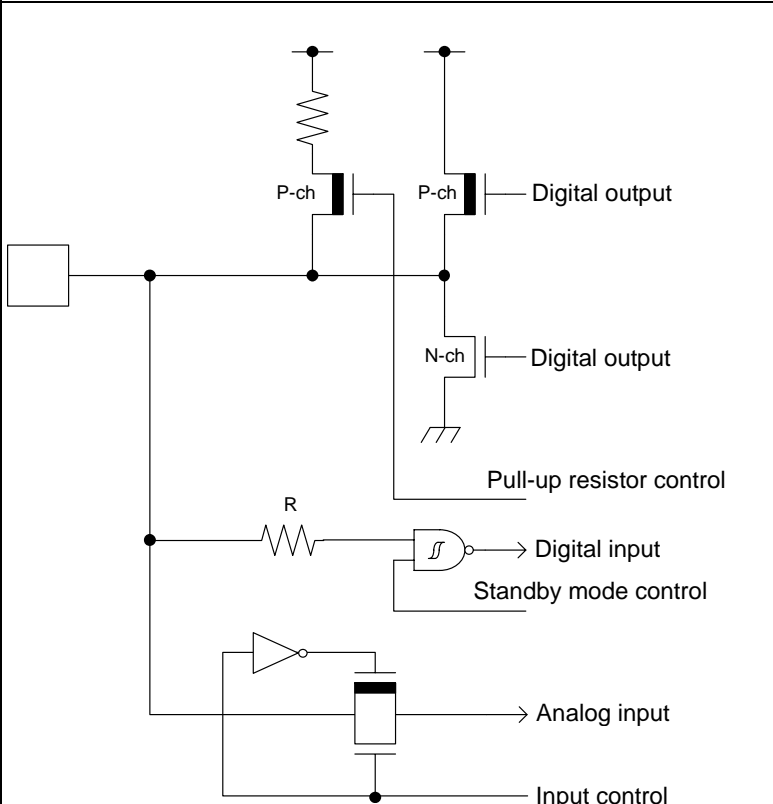
### 7. I/O Circuit Type

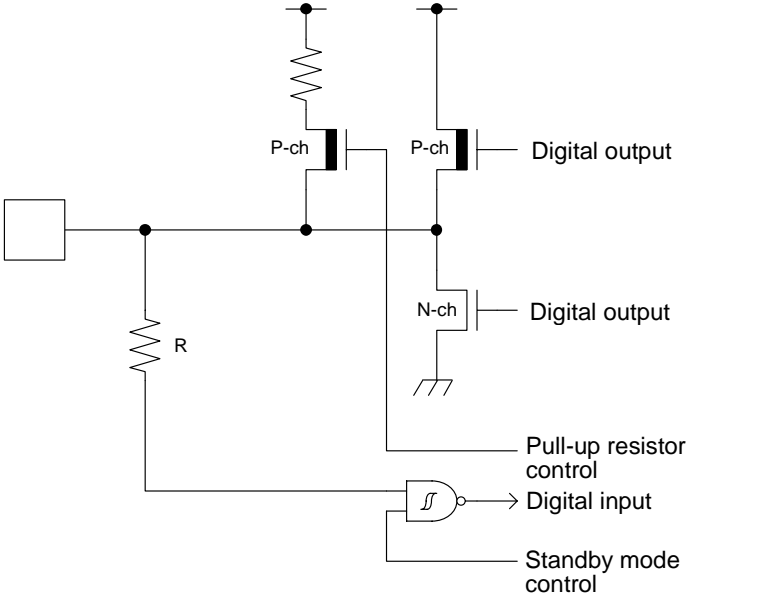
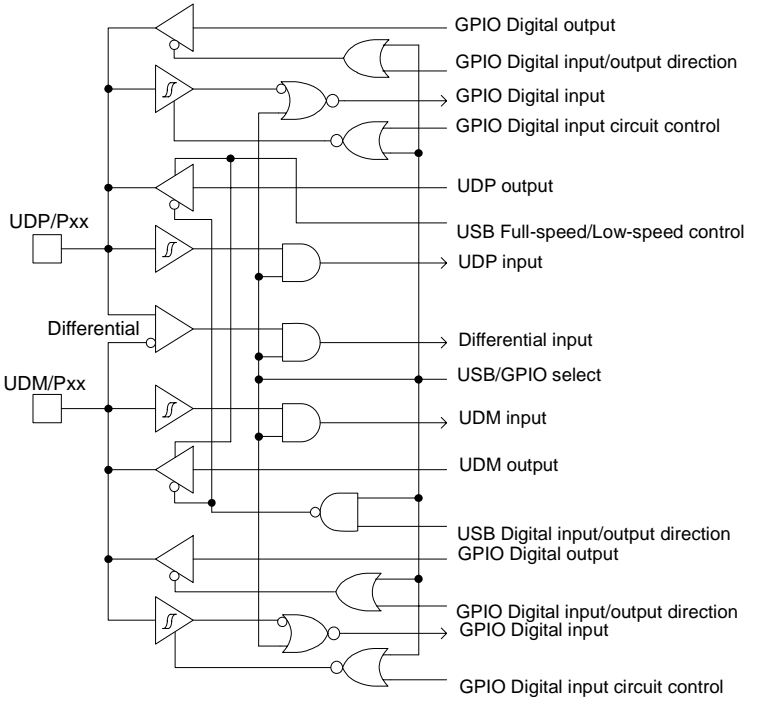
Type	Circuit	Remarks
A		<p>It is possible to select the main Oscillation/GPIO function.</p> <p>When the main oscillation is selected:</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor: approximately 1 MΩ</li> <li>• Standby mode control</li> </ul> <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
B		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor: approximately 50 kΩ</li> </ul>

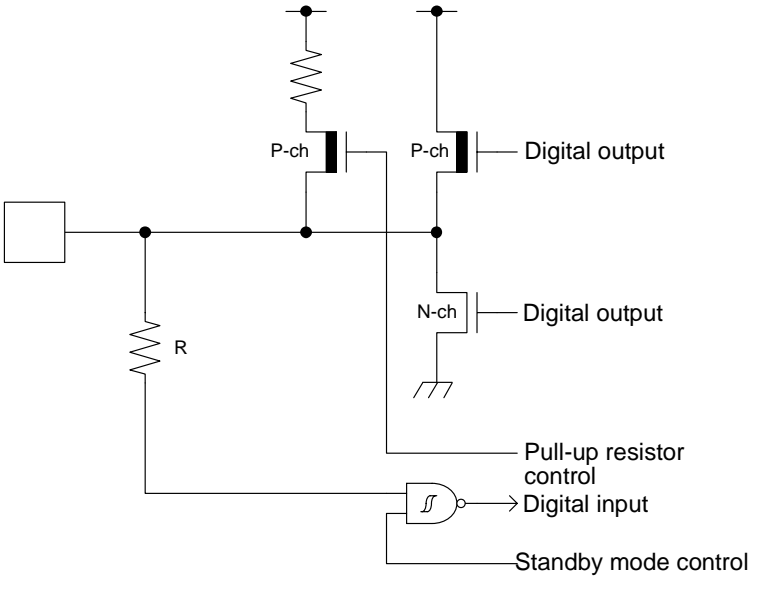
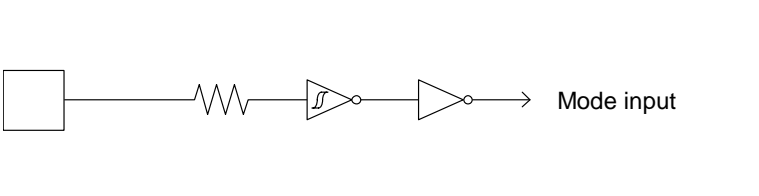
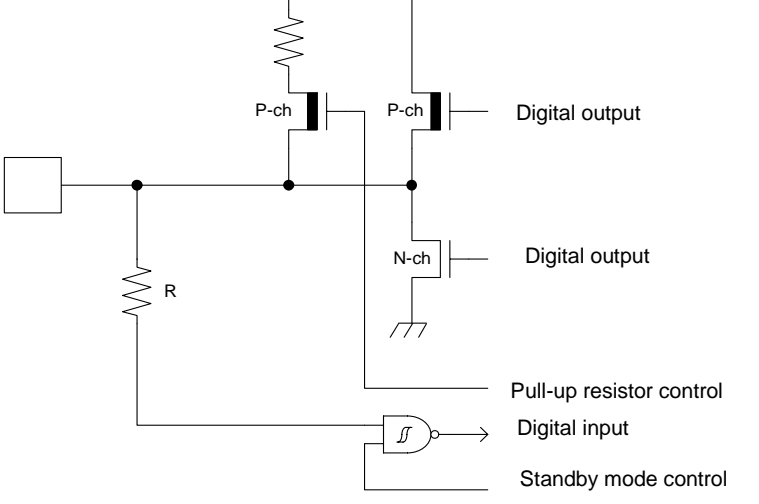
Type	Circuit	Remarks
C		<ul style="list-style-type: none"> <li>• Open drain output</li> <li>• CMOS level hysteresis input</li> </ul>

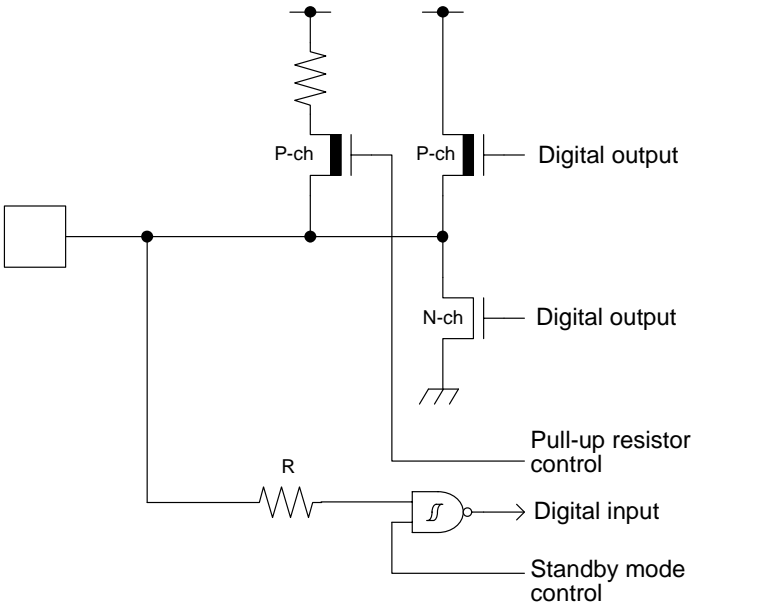
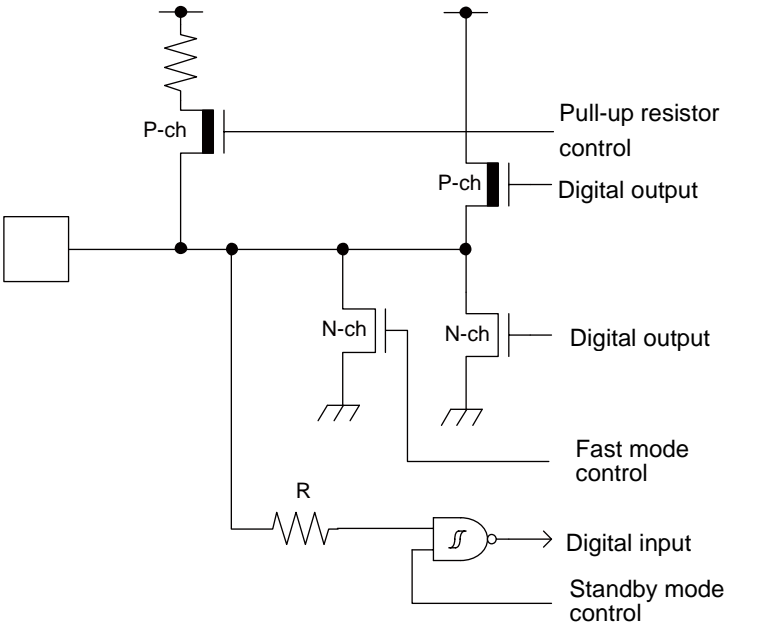
Type	Circuit	Remarks
D	 <p>The circuit diagram shows two oscillators, X1A and X0A, each with a pull-up resistor R. X1A is connected to a P-ch MOSFET and an N-ch MOSFET, both labeled as Digital output. X0A is also connected to P-ch and N-ch MOSFETs, both labeled as Digital output. The circuit includes several digital inputs and standby mode controls, along with pull-up resistor control signals. The diagram illustrates the internal structure of the device, including transistors, resistors, and logic gates.</p>	<p>It is possible to select the sub oscillation/GPIO function.</p> <p>When the main oscillation is selected:</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor: approximately 5 MΩ</li> <li>• Standby mode control</li> </ul> <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

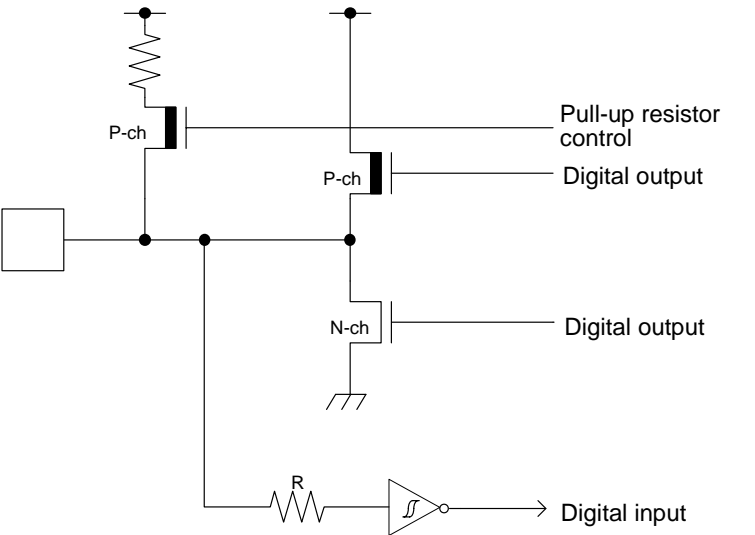
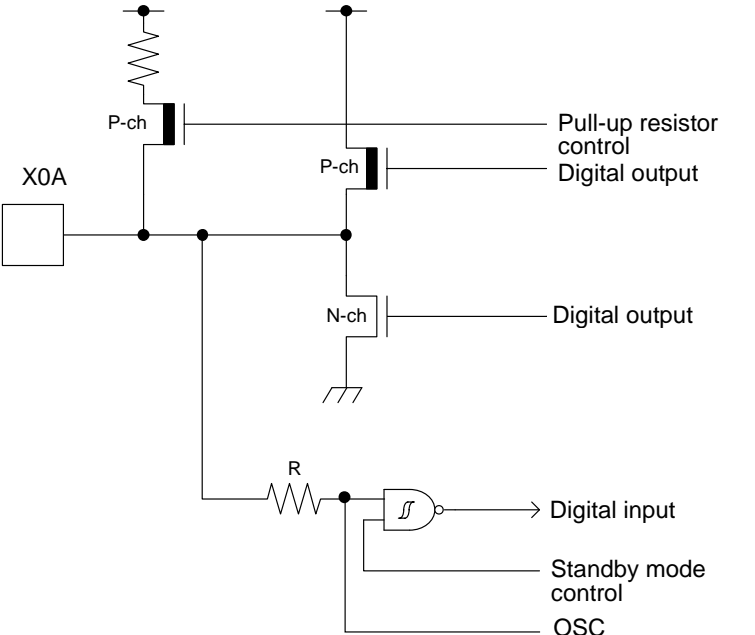


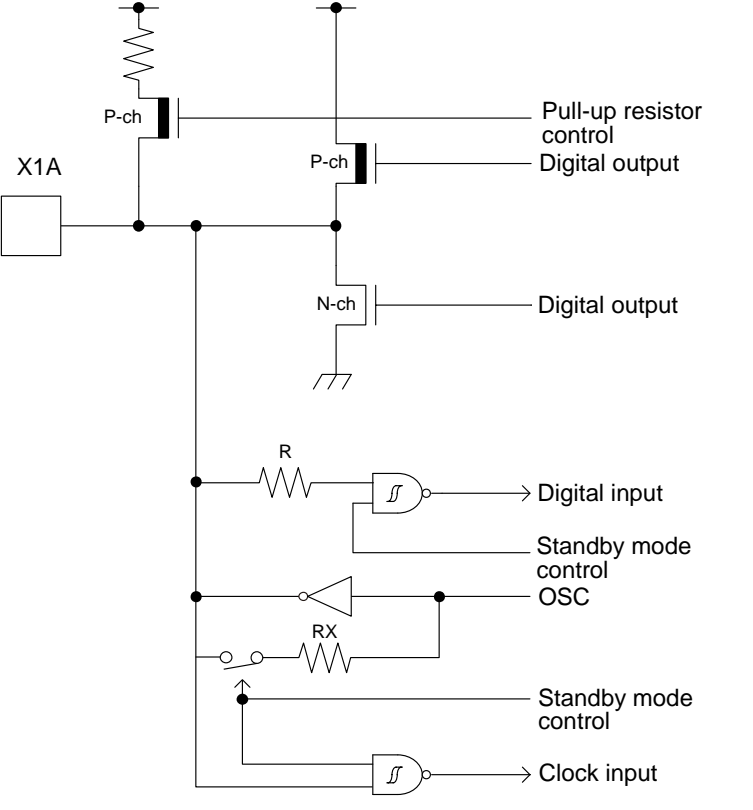
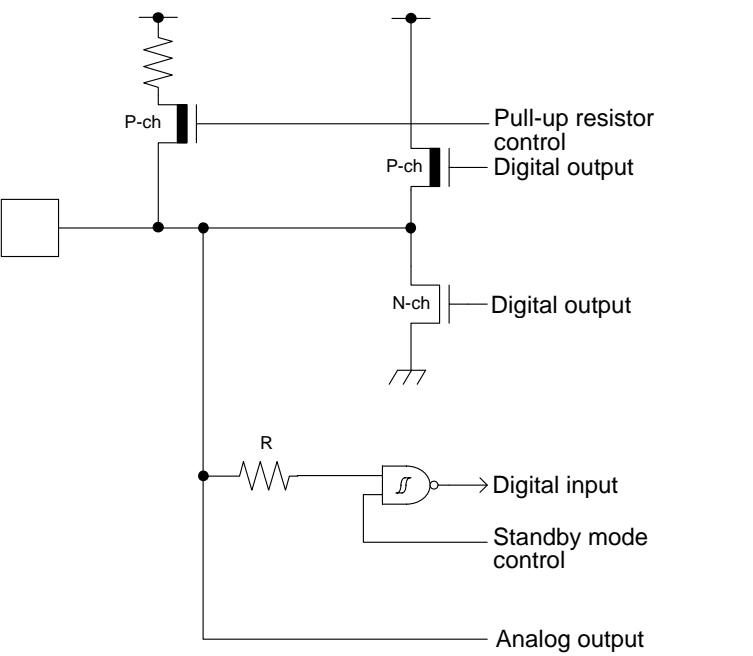
Type	Circuit	Remarks
E		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>
F		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Input control</li> <li>• Analog input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>

Type	Circuit	Remarks
G	 <p>The diagram shows a pull-up resistor R connected to a digital input/output pin. The pin is connected to the gates of two transistors: a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch transistor's source is connected to VDD, and its drain is connected to the pin. The N-ch transistor's source is connected to ground, and its drain is connected to the pin. A digital input signal is connected to the gates of both transistors through an AND gate. A standby mode control signal is connected to the gates of both transistors through an AND gate. The output of the P-ch transistor is labeled 'Digital output', and the output of the N-ch transistor is also labeled 'Digital output'.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -12 \text{ mA}</math>, <math>I_{OL} = 12 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>
H	 <p>The diagram shows a complex digital logic circuit. It includes several multiplexers (MUX) and logic gates (AND, OR, NOT). The inputs to the MUXes are labeled 'UDP/Pxx' and 'UDM/Pxx'. The outputs of the MUXes are connected to various digital signals: 'GPIO Digital output', 'GPIO Digital input/output direction', 'GPIO Digital input', 'GPIO Digital input circuit control', 'UDP output', 'USB Full-speed/Low-speed control', 'UDP input', 'Differential input', 'USB/GPIO select', 'UDM input', 'UDM output', 'USB Digital input/output direction', 'GPIO Digital output', 'GPIO Digital input/output direction', 'GPIO Digital input', and 'GPIO Digital input circuit control'.</p>	<p>It is possible to select either USB I/O or GPIO function.</p> <p>When the USB I/O is selected:</p> <ul style="list-style-type: none"> <li>• Full-speed, low-speed control</li> </ul> <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Standby mode control</li> <li>• <math>I_{OH} = -20.5 \text{ mA}</math>, <math>I_{OL} = 18.5 \text{ mA}</math></li> </ul>

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5 V tolerant</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control of PZR registers (pseudo-open drain control)</li> <li>• For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).</li> </ul>
J		<p>CMOS level hysteresis input</p>
K		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• TTL level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

Type	Circuit	Remarks
L		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -8 \text{ mA}</math>, <math>I_{OL} = 8 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>
N		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5V tolerant</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math> (GPIO)</li> <li>• <math>I_{OL} = 20 \text{ mA}</math> (Fast mode Plus)</li> <li>• Available to control of PZR register (pseudo-open drain control)</li> <li>• For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>

Type	Circuit	Remarks
O		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5 V tolerant</li> <li>• Pull-up resistor control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4\text{ mA}</math>, <math>I_{OL} = 4\text{ mA}</math></li> <li>• Available to control of PZR register (pseudo-open drain control)</li> <li>• For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).</li> </ul>
P		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4\text{ mA}</math>, <math>I_{OL} = 4\text{ mA}</math></li> </ul>

Type	Circuit	Remarks
Q	 <p>The circuit diagram for Type Q shows a pull-up resistor connected to a P-ch transistor. The output of this P-ch transistor is labeled 'Pull-up resistor control'. The node between the pull-up resistor and the P-ch transistor is connected to another P-ch transistor (labeled 'Digital output') and an N-ch transistor (labeled 'Digital output'). The N-ch transistor is connected to ground. Below this, there is a resistor 'R' connected to a digital input. Further down, there is a standby mode control input connected to an oscillator symbol 'OSC'. Below that, there is a resistor 'RX' connected to another standby mode control input. At the bottom, there is a clock input connected to an oscillator symbol.</p>	<p>It is possible to select the sub oscillation/GPIO function.</p> <p>When the sub oscillation is selected:</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor: approximately 10 MΩ</li> </ul> <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
R	 <p>The circuit diagram for Type R shows a pull-up resistor connected to a P-ch transistor. The output of this P-ch transistor is labeled 'Pull-up resistor control'. The node between the pull-up resistor and the P-ch transistor is connected to another P-ch transistor (labeled 'Digital output') and an N-ch transistor (labeled 'Digital output'). The N-ch transistor is connected to ground. Below this, there is a resistor 'R' connected to a digital input. Further down, there is a standby mode control input connected to an oscillator symbol.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Analog output</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math> (4.5V to 5.5V)</li> <li>• <math>I_{OH} = -2 \text{ mA}</math>, <math>I_{OL} = 2 \text{ mA}</math> (2.7V to 4.5V)</li> </ul>

## 8. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

### 8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

### **Latch-Up**

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

### **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

### **Fail-Safe Design**

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

### **Precautions Related to Usage of Devices**

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## **8.2 Precautions for Package Mounting**

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

### **Lead Insertion Type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.



You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

### **Lead-Free Packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

### **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

### **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

### **Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

### 8.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

**CAUTION:** Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 9. Handling Devices

### Power-Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. All of these pins should be connected externally to the power supply or ground lines, however, in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Be sure to connect the current-supply source with the power pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between VCC and VSS near this device.

A malfunction may occur when the power-supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1V/ $\mu\text{s}$  at a momentary fluctuation such as switching the power supply.

### Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane, as this is expected to produce stable operation.

Evaluate the oscillation introduced by the use of the crystal oscillator by your mount board.

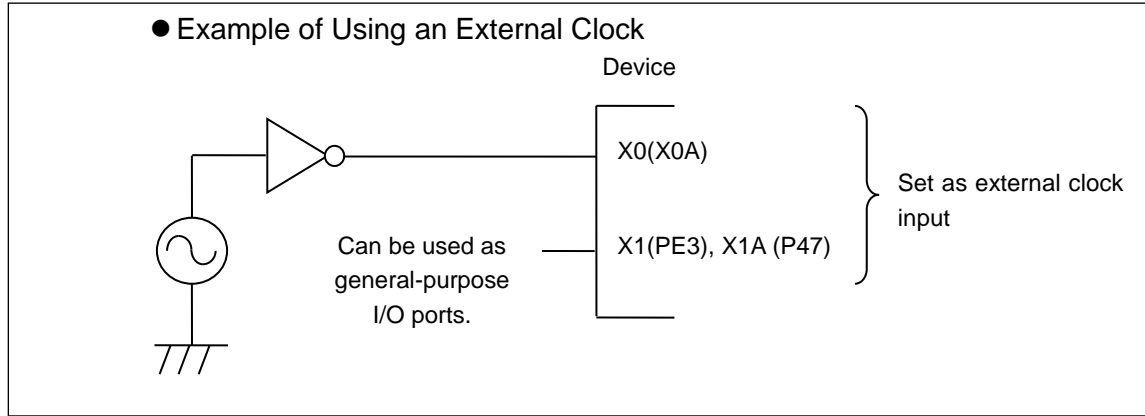
### Sub Crystal Oscillator

The sub-oscillator circuit for devices in this family is low gain to keep current consumption low. To stabilize the oscillation, Cypress recommends a crystal oscillator that meets the following conditions:

- Surface mount type
  - Size: More than 3.2 mm  $\times$  1.5 mm
  - Load capacitance: approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: approximately 6 pF to 7 pF

**Using an External Clock**

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

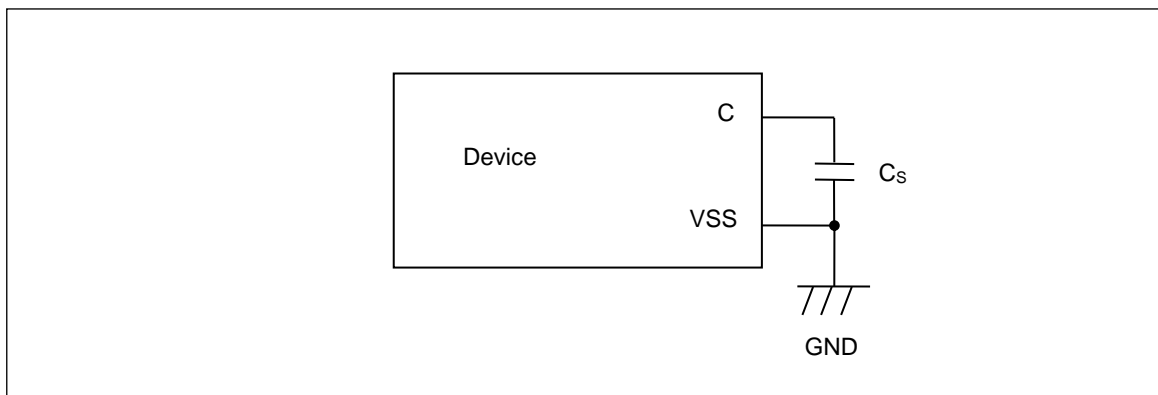


**Handling When Using Multi-Function Serial Pin as I<sup>2</sup>C Pin**

If the application uses the multi-function serial pin as an I<sup>2</sup>C pin, the P-channel transistor of the digital output must be disabled. I<sup>2</sup>C pins need to conform to electrical limitations like other pins, however, and avoid connecting to live external systems with the MCU power off.

**C Pin**

Devices in this series contain a regulator. Be sure to connect a smoothing capacitor (C<sub>S</sub>) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. Some laminated ceramic capacitors have a large capacitance variation due to thermal fluctuation. Please select a capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of the device. A smoothing capacitor of about 4.7 μF would be recommended for this series.



**Mode Pins (MD0)**

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, the distance between the mode pins and VCC pins or VSS pins is as short as possible, and the connection impedance is low when the pins are pulled up/down such as for switching the pin level and rewriting the flash memory data. This is important to prevent the device from erroneously switching to test mode as a result of noise.

### Notes on Power-On

Turn power on/off in the sequence shown below or at the same time. If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VCC → USBVCC0  
VCC → USBVCC1  
VCC → ETHVCC  
VCC → AVCC → AVRH  
Turning off: USBVCC0 → VCC  
USBVCC1 → VCC  
ETHVCC → VCC  
AVRH → AVCC → VCC

### Serial Communication

There is a possibility of receiving incorrect data as a result of noise or other issues introduced by the serial communication. Take care to design the printed circuit board to minimize noise.

Consider the case of introducing error as a result of noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

### Differences in Characteristics within the Product Line

The electric characteristics including power consumption, ESD, latch-up, noise, and oscillation differ among members of the product line because chip layout and memory structures are not the same; for example, different sizes, flash versus ROM, etc. If you are switching to a different product of the same series, please make sure to evaluate the electric characteristics.

### Pull-Up Function of 5 V Tolerant I/O

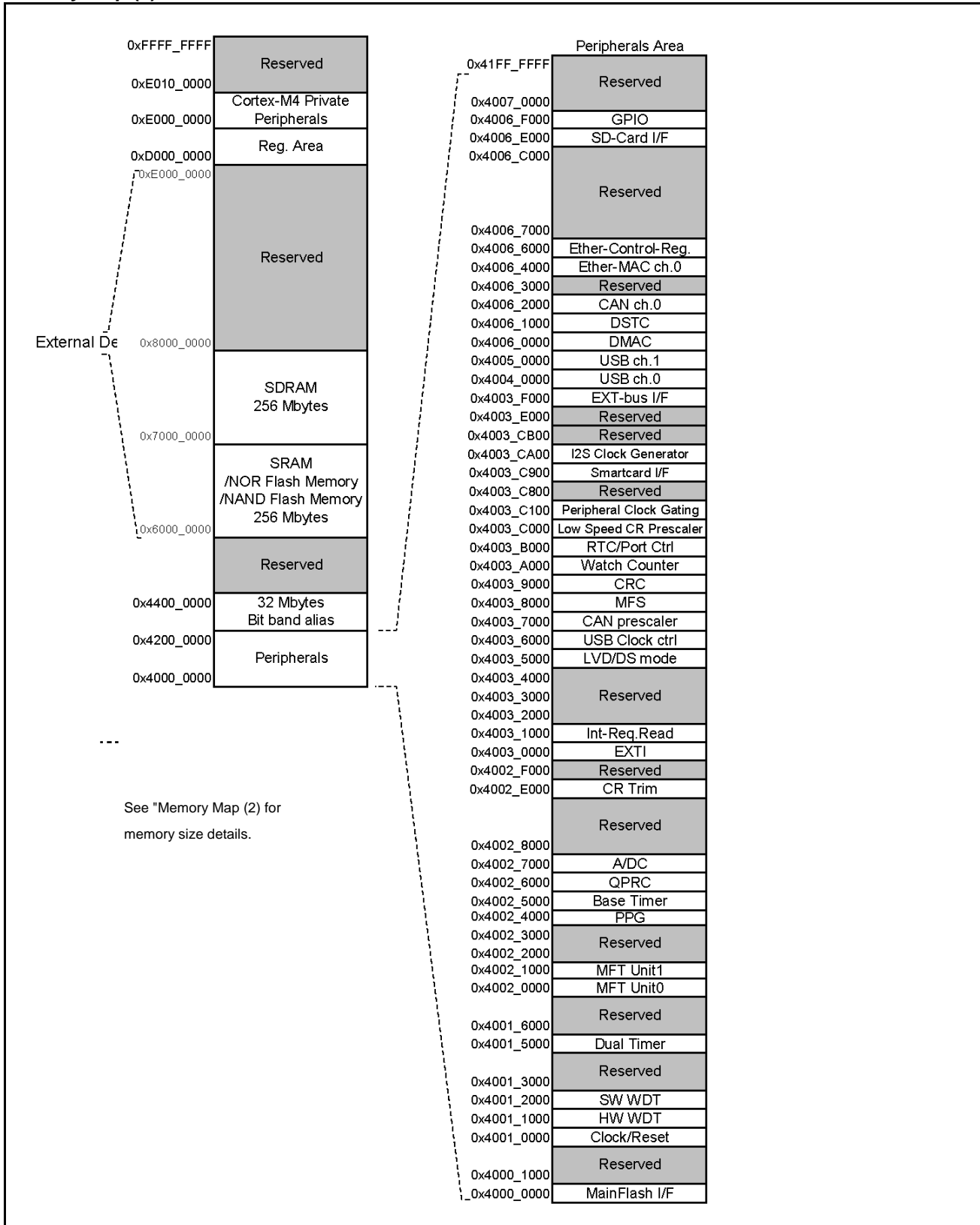
Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

### Pin Doubled as Debug Function

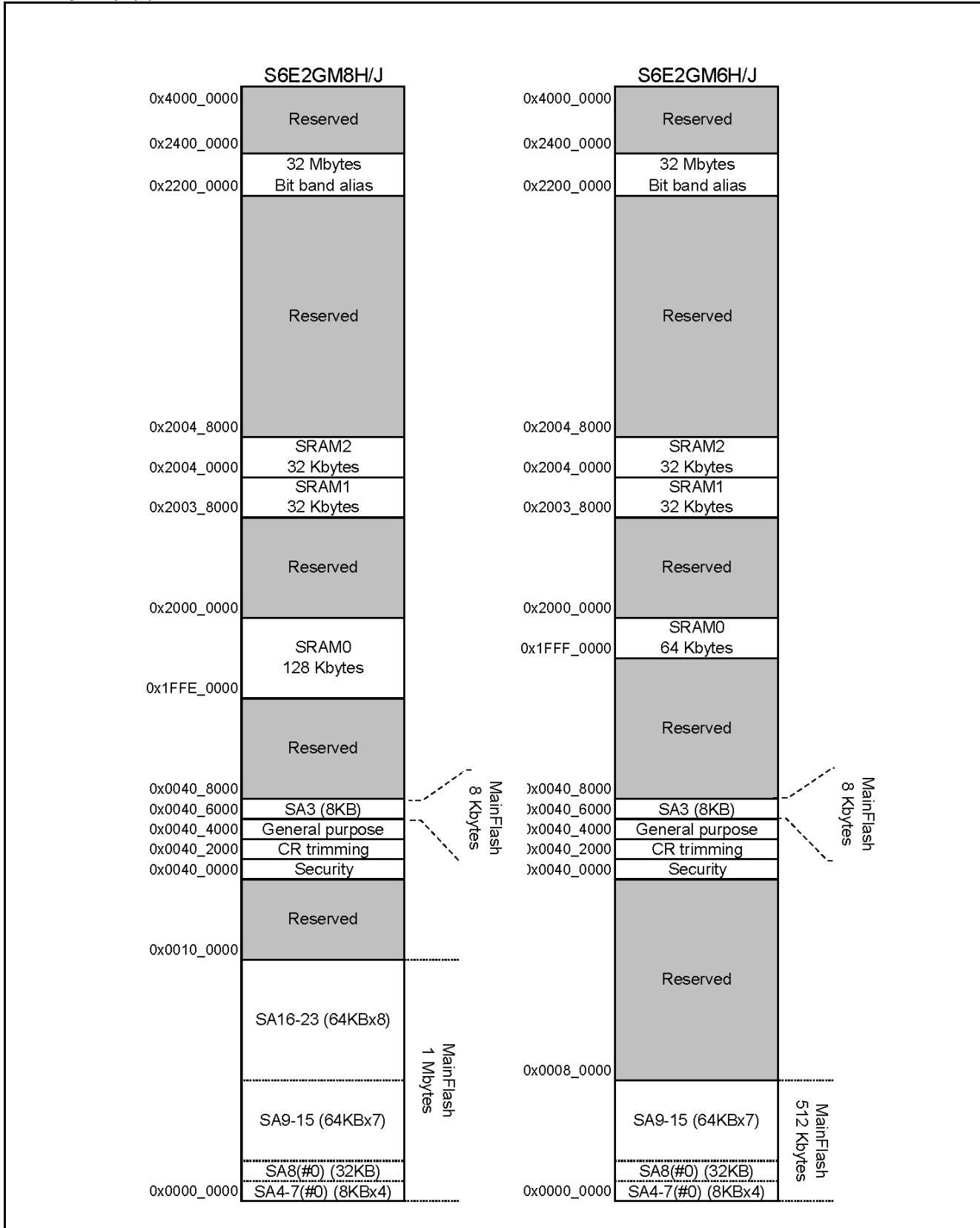
The pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK should be used as output only. Do not use as input.

## 10. Memory Map

### Memory Map (1)



**Memory Map (2)**



\*: See S6E2GM/GK/GH/G3/G2 Series Flash Programming Manual to confirm the detail of flash Memory.

**Peripheral Address Map**

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF		APB1
0x4002_1000	0x4002_1FFF	Multi-Function Timer unit 1	
0x4002_2000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	PPG	
0x4002_5000	0x4002_5FFF	Base timer	
0x4002_6000	0x4002_6FFF	Quadrature position/revolution counter	
0x4002_7000	0x4002_7FFF	A/D converter	
0x4002_8000	0x4002_DFFF	Reserved	
0x4002_E000	0x4002_EFFF	Internal CR trimming	
0x4002_F000	0x4002_FFFF	Reserved	
0x4003_0000	0x4003_0FFF	APB2	
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_C8FF		Reserved
0x4003_C900	0x4003_C9FF		I2S clock generator
0x4003_CA00	0x4003_CAFF		Smartcard Interface
0x4003_CB00	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface



Start Address	End Address	Bus	Peripherals
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x4006_5FFF		Ethernet-MAC ch 0
0x4006_6000	0x4006_6FFF		Ethernet-MAC setting register
0x4006_7000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x41FF_FFFF		Reserved

## 11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- **INITX = 0**  
This is the period when the INITX pin is at the L level.
- **INITX = 1**  
This is the period when the INITX pin is at the H level.
- **SPL = 0**  
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 0.
- **SPL = 1**  
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 1.
- **Input enabled**  
Indicates that the input function can be used.
- **Internal input fixed at 0**  
This is the status that the input function cannot be used. Internal input is fixed at L.
- **Hi-Z**  
Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.
- **Setting disabled**  
Indicates that the setting is disabled.
- **Maintain previous state**  
Maintains the state that was immediately prior to entering the current mode.  
If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.
- **Analog input is enabled**  
Indicates that the analog input is enabled.
- **Trace output**  
Indicates that the trace function can be used.
- **GPIO selected**  
In Deep standby mode, pins switch to the general-purpose I/O port.
- **Setting prohibition**  
Prohibition of a setting by specification limitation

**List of Pin Behavior by Mode State**

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enabled	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops* <sup>1</sup> , it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/ internal input fixed at 0			GPIO selected
	GPIO selected									
G	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/Internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/Internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State			
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable			
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1			
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-			
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected			
	External interrupt enable selected					Maintain previous state	Maintain previous state				GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0						
	GPIO selected												
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected			
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0						
	GPIO selected												
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled			
	Resource other than above selected		Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected		
	GPIO selected												

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected						Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled
S	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Sub crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled



Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
T	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enabled	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*5, it will be Hi-Z/ Internal input fixed at 0					
V	Ethernet I/O selected *4	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at "0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
W	Ethernet input/output selected <sup>*4</sup>	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected									
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									

S	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Sub crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
T	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enabled	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops <sup>*5</sup> , it will be Hi-Z/ Internal input fixed at 0					

- 1: Oscillation is stopped at Sub Timer mode, sub CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.
- 2: Maintain previous state at Timer mode. GPIO selected internal input fixed at 0 at RTC mode, Stop mode.
- 3: Maintain previous state at Timer mode. Hi-Z/internal input fixed at 0 at RTC mode, Stop mode.
- 4: It shows the case selected by EPFR14.E\_SPLC register.

## 12. Electrical Characteristics

### 12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage <sup>*1,*2</sup>	$V_{CC}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Power supply voltage (for USB) <sup>*1,*3</sup>	$USBV_{CC0}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Power supply voltage (for USB) <sup>*1,*3</sup>	$USBV_{CC1}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Power supply voltage (for Ethernet-MAC) <sup>*1,*4</sup>	$ETHV_{CC}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Analog power supply voltage <sup>*1,*5</sup>	$AV_{CC}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Analog reference voltage <sup>*1,*5</sup>	$AVRH$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Input voltage <sup>*1</sup>	$V_I$	$V_{SS} - 0.5$	$V_{CC} + 0.5 (\leq 6.5 \text{ V})$	V	Except for USB and Ethernet-MAC pin
		$V_{SS} - 0.5$	$USBV_{CC0} + 0.5 (\leq 6.5 \text{ V})$	V	USB ch 0 pin
		$V_{SS} - 0.5$	$USBV_{CC1} + 0.5 (\leq 6.5 \text{ V})$	V	USB ch 1 pin
		$V_{SS} - 0.5$	$ETHV_{CC} + 0.5 (\leq 6.5 \text{ V})$	V	Ethernet-MAC Pin
		$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	5 V tolerant
Analog pin input voltage <sup>*1</sup>	$V_{IA}$	$V_{SS} - 0.5$	$AV_{CC} + 0.5 (\leq 6.5 \text{ V})$	V	
Output voltage <sup>*1</sup>	$V_O$	$V_{SS} - 0.5$	$V_{CC} + 0.5 (\leq 6.5 \text{ V})$	V	
L level maximum output current <sup>*6</sup>	$I_{OL}$	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			22.4	mA	I <sup>2</sup> C Fm+
L level average output current <sup>*7</sup>	$I_{OLAV}$	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			20	mA	I <sup>2</sup> C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current <sup>*8</sup>	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current <sup>*6</sup>	$I_{OH}$	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	12 mA type
H level average output current <sup>*7</sup>	$I_{OHAV}$	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current <sup>*8</sup>	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	$T_{STG}$	- 55	+ 150	°C	

1: These parameters are based on the condition that  $V_{SS} = AV_{SS} = 0.0 \text{ V}$ .

- 2:  $V_{CC}$  must not drop below  $V_{SS} - 0.5$  V.
- 3:  $USBV_{CC0}$ ,  $USBV_{CC1}$  must not drop below  $V_{SS} - 0.5$  V.
- 4:  $ETHV_{CC}$  must not drop below  $V_{SS} - 0.5$  V.
- 5: Ensure that the voltage does not exceed  $V_{CC} + 0.5$ V, for example, when the power is turned on.
- 6: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
- 7: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.
- 8: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

**WARNING:**

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

## 12.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Value		Unit	Remarks	
			Min	Max			
Power supply voltage	$V_{CC}$	-	2.7*10	5.5	V		
Power supply voltage (for USB ch 0)	USBV <sub>CC0</sub>	-	3.0	3.6 ( $\leq V_{CC}$ )	V	*1	
			2.7	5.5 ( $\leq V_{CC}$ )		*2	
Power supply voltage (for USB ch 1)	USBV <sub>CC1</sub>	-	3.0	3.6 ( $\leq V_{CC}$ )	V	*3	
			2.7	5.5 ( $\leq V_{CC}$ )		*4	
Power supply voltage (for Ethernet-MAC)	ETHV <sub>CC</sub>	-	3.0	3.6 ( $\leq V_{CC}$ )	V	*5	
			4.5	5.5 ( $\leq V_{CC}$ )		*5	
			2.7	5.5 ( $\leq V_{CC}$ )		*6	
Analog power supply voltage	AV <sub>CC</sub>	-	2.7	5.5	V	AV <sub>CC</sub> = V <sub>CC</sub>	
Analog reference voltage	AVRH	-	*9	AV <sub>CC</sub>	V		
	AVRL	-	AV <sub>SS</sub>	AV <sub>SS</sub>	V		
Smoothing capacitor	C <sub>S</sub>	-	1	10	μF	for built-in regulator *7	
Operating temperature	Junction temperature	T <sub>J</sub>	-	- 40	+ 125	°C	
	Ambient temperature	T <sub>A</sub>	-	-40	*8	°C	

- 1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)
- 2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)
- 3: When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)
- 4: When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)
- 5: When the pins in Ethernet-MAC Timing, except P6E/ADTG\_5/SCK4\_1/IC23\_1/INT29\_0/E\_PPS pin, are used as Ethernet-MAC pin
- 6: When the pins in [Ethernet-MAC Timing](#), except P6E/ADTG\_5/SCK4\_1/IC23\_1/INT29\_0/E\_PPS pin, are used as function pins
- 7: See "C pin" in [9 Handling Devices](#) for the connection of the smoothing capacitor.
- 8: The maximum temperature of the ambient temperature (T<sub>A</sub>) can guarantee a range that does not exceed the junction temperature (T<sub>J</sub>).  
The calculation formula of the ambient temperature (T<sub>A</sub>) is:  

$$T_A (\text{Max}) = T_J (\text{Max}) - P_d (\text{Max}) \times \theta_{JA}$$

P<sub>d</sub>: Power dissipation (W)  
 $\theta_{JA}$ : Package thermal resistance (°C/W)

$$P_d (\text{Max}) = V_{CC} \times I_{CC} (\text{Max}) + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I<sub>OL</sub>: L level output current  
I<sub>OH</sub>: H level output current  
V<sub>OL</sub>: L level output voltage  
V<sub>OH</sub>: H level output voltage
- 9: The minimum value of analog reference voltage depends on the value of compare clock cycle (T<sub>CK</sub>). See 12.5. 12-bit A/D Converter for the details.
- 10: For the voltage range between V<sub>CC</sub>(min) and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR.

Package thermal resistance and maximum permissible power for each package are shown below. The operation is guaranteed maximum permissible power or less for semiconductor devices.

**Table for Package Thermal Resistance and Maximum Permissible Power**

Package	Printed Circuit Board	Thermal Resistance $\theta_{ja}$ ( $^{\circ}\text{C}/\text{W}$ )	Maximum Permissible Power (mW)	
			$T_A = +85\text{ }^{\circ}\text{C}$	$T_A = +105\text{ }^{\circ}\text{C}$
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645

**WARNING:**

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
- *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

**Ethernet-MAC Pins**

Pin Name	Ethernet-MAC Function	Except For Ethernet-MAC Function	Power Supply Type
P6E/ADTG_5/SCK4_1/INT29_0/E_PPS	E_PPS *	P6E/ADTG_5/SCK4_1/INT29_0	V <sub>CC</sub>
PC0/E_RXER	E_RXER	PC0	ETHV <sub>CC</sub>
PC1/TIOB6_0/E_RX03	E_RX03	PC1/TIOB6_0	
PC2/TIOA6_0/E_RX02	E_RX02	PC2/TIOA6_0	
PC3/TIOB7_0/E_RX01	E_RX01	PC3/TIOB7_0	
PC4/TIOA7_0/E_RX00	E_RX00	PC4/TIOA7_0	
PC5/TIOB14_0/E_RXDV	E_RXDV	PC5/TIOB14_0	
PC6/TIOA14_0/E_MDIO	E_MDIO	PC6/TIOA14_0	
PC7/INT13_0/E_MDC/CROUT_1	E_MDC	PC7/INT13_0/CROUT_1	
PC8/E_RXCK_REFCK	E_RXCK_REFCK	PC8	
PC9/TIOB15_0/E_COL	E_COL	PC9/TIOB15_0	
PCA/TIOA15_0/E_CRX	E_CRX	PCA/TIOA15_0	
PCB/INT28_0/E_COUT	E_COUT	PCB/INT28_0	
PCC/E_TCK	E_TCK	PCC	
PCD/SOT4_1/INT14_0/E_TXER	E_TXER	PCD/SOT4_1/INT14_0	
PCE/SIN4_1/INT15_0/E_TX03	E_TX03	PCE/SIN4_1/INT15_0	
PCF/RTS4_1/INT12_0/E_TX02	E_TX02	PCF/RTS4_1/INT12_0	
PD0/INT30_1/E_TX01	E_TX01	PD0/INT30_1	
PD1/INT31_1/E_TX00	E_TX00	PD1/INT31_1	
PD2/CTS4_1/E_TXEN	E_TXEN	PD2/CTS4_1	

\*: It is used to confirm the PTP counter cycle in Ethernet-MAC by waveforms.



### Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$P_d = V_{CC} \times I_{CC} + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

$I_{OL}$ : L level output current  
 $I_{OH}$ : H level output current  
 $V_{OL}$ : L level output voltage  
 $V_{OH}$ : H level output voltage

$I_{CC}$  is the current drawn by the device.

It can be analyzed as follows.

$$I_{CC} = I_{CC}(\text{INT}) + \sum I_{CC}(\text{IO})$$

$I_{CC}(\text{INT})$ : Current drawn by internal logic and memory, etc. through the regulator

$\sum I_{CC}(\text{IO})$ : Sum of current (I/O switching current) drawn by the output pin

For  $I_{CC}(\text{INT})$ , it can be anticipated by "(1) Current Rating" in "12.3. DC Characteristics" (This rating value does not include  $I_{CC}(\text{IO})$  for a value at pin fixed).

For  $I_{CC}(\text{IO})$ , it depends on system used by customers.

The calculation formula is shown below.

$$I_{CC}(\text{IO}) = (C_{\text{INT}} + C_{\text{EXT}}) \times V_{CC} \times f_{\text{SW}}$$

$C_{\text{INT}}$ : Pin internal load capacitance  
 $C_{\text{EXT}}$ : External load capacitance of output pin  
 $f_{\text{SW}}$ : Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	$C_{\text{INT}}$	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate  $I_{CC}(\text{Max})$  as follows when the power dissipation can be evaluated by yourself:

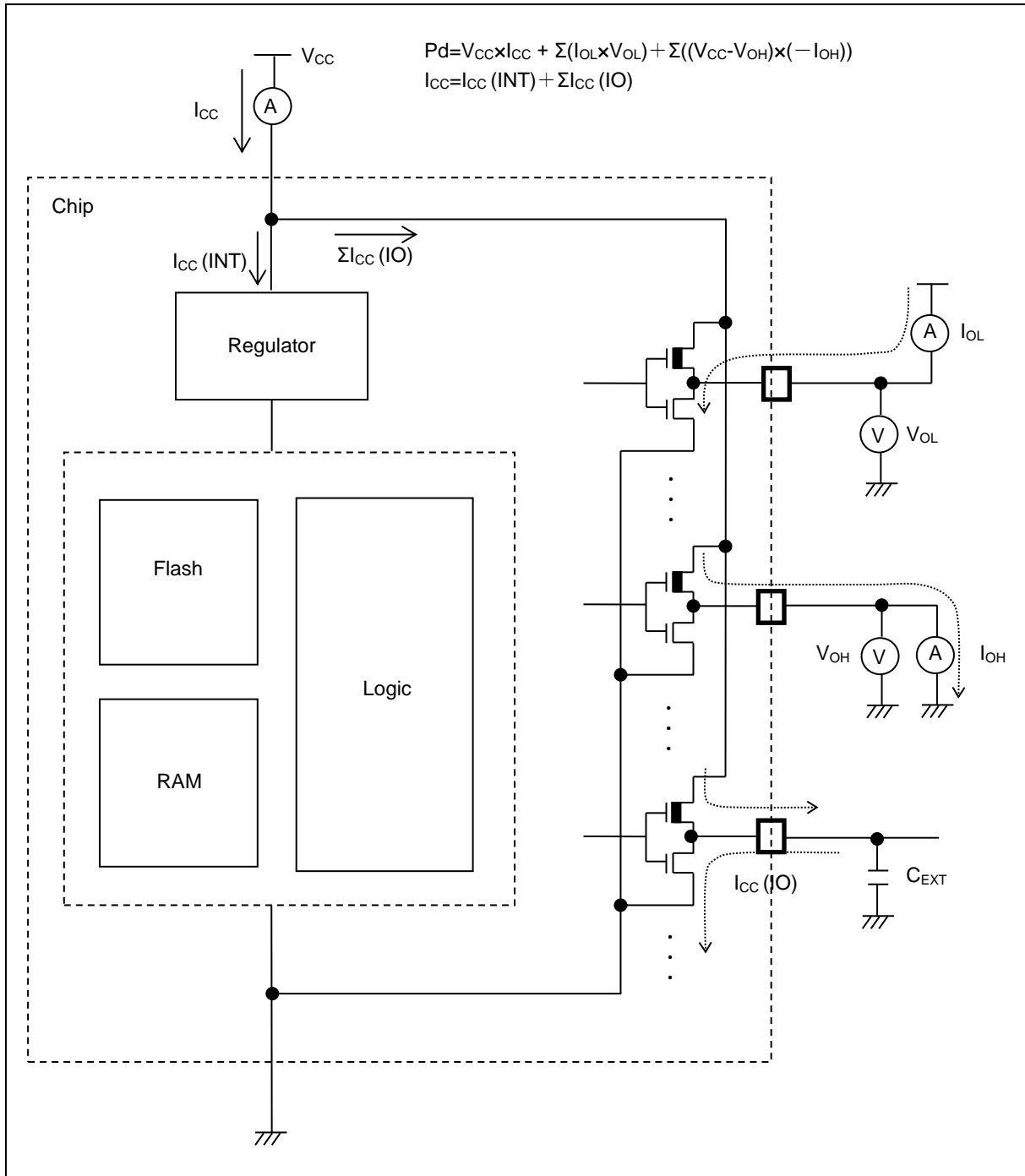
Measure current value  $I_{CC}(\text{Typ})$  at normal temperature (+25°C).

Add maximum leakage current value  $I_{CC}(\text{leak\_max})$  at operating on a value in (1).

$$I_{CC}(\text{Max}) = I_{CC}(\text{Typ}) + I_{CC}(\text{leak\_max})$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	$I_{CC}(\text{leak\_max})$	$T_J = +125^\circ\text{C}$	53.6 mA
		$T_J = +105^\circ\text{C}$	26.6 mA
		$T_J = +85^\circ\text{C}$	17.5 mA

Current Explanation Diagram



12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks	
					Typ*1	Max*2			
Power supply current	I <sub>CC</sub>	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	73	131	mA	*3 When all peripheral clocks are on
				*6	160 MHz	65	123	mA	
					144 MHz	59	117	mA	
					120 MHz	50	108	mA	
					100 MHz	43	101	mA	
					80 MHz	35	93	mA	
					60 MHz	27	85	mA	
					40 MHz	19	77	mA	
					20 MHz	11	69	mA	
					8 MHz	6.9	64	mA	
				4 MHz	5.3	63	mA		
				*5	180 MHz	44	102	mA	*3 When all peripheral clocks are off
				*6	160 MHz	40	98	mA	
					144 MHz	36	94	mA	
					120 MHz	31	89	mA	
					100 MHz	27	85	mA	
					80 MHz	22	80	mA	
					60 MHz	17	75	mA	
					40 MHz	13	71	mA	
					20 MHz	7.9	65	mA	
8 MHz	5.2	63	mA						
4 MHz	4.3	62	mA						

1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

6: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory.”

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)**

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>4</sup>	Value		Unit	Remarks	
					Typ* <sup>1</sup>	Max* <sup>2</sup>			
Power supply current	I <sub>CC</sub>	VCC	Normal operation * <sup>7</sup> ,* <sup>8</sup> (PLL)	* <sup>5</sup>	180 MHz	82	140	mA	* <sup>3</sup> When all peripheral clocks are on
				* <sup>6</sup>	160 MHz	74	132	mA	
					144 MHz	68	126	mA	
					120 MHz	58	116	mA	
					100 MHz	49	107	mA	
					80 MHz	40	98	mA	
					60 MHz	31	89	mA	
					40 MHz	22	80	mA	
					20 MHz	13	71	mA	
					8 MHz	7.5	65	mA	
					4 MHz	5.6	63	mA	
				* <sup>5</sup>	180 MHz	48	106	mA	* <sup>3</sup> When all peripheral clocks are off
				* <sup>6</sup>	160 MHz	44	102	mA	
					144 MHz	41	99	mA	
					120 MHz	35	93	mA	
					100 MHz	30	88	mA	
					80 MHz	25	83	mA	
					60 MHz	20	78	mA	
					40 MHz	14	72	mA	
					20 MHz	8.7	66	mA	
8 MHz	5.6	63	mA						
4 MHz	4.5	62	mA						

1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

7: With data access to a MainFlash memory.

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)**

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>4</sup>	Value		Unit	Remarks	
					Typ* <sup>1</sup>	Max* <sup>2</sup>			
Power supply current	I <sub>CC</sub>	VCC	Normal operation * <sup>6</sup> ,* <sup>7</sup> (PLL)	* <sup>5</sup>	72 MHz	54	112	mA	* <sup>3</sup> When all peripheral clocks are on
					60 MHz	47	105	mA	
					48 MHz	39	97	mA	
					36 MHz	31	89	mA	
					24 MHz	23	81	mA	
					12 MHz	14	72	mA	
					8 MHz	11	69	mA	
					4 MHz	7.2	65	mA	
				* <sup>5</sup>	72 MHz	37	95	mA	* <sup>3</sup> When all peripheral clocks are off
					60 MHz	33	91	mA	
					48 MHz	28	86	mA	
					36 MHz	23	81	mA	
					24 MHz	17	75	mA	
					12 MHz	11	69	mA	
				8 MHz	8.3	66	mA		
				4 MHz	5.9	63	mA		

1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFDR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)**

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>4</sup>	Value		Unit	Remarks
					Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CC</sub>	VCC	Normal operation * <sup>6</sup> , * <sup>7</sup> (main oscillation)	* <sup>5</sup> 4 MHz	4.3	62	mA	* <sup>3</sup> When all peripheral clocks are on
					3.7	61	mA	* <sup>3</sup> When all peripheral clocks are off
			Normal operation * <sup>6</sup> (built-in High-speed CR)	* <sup>5</sup> 4 MHz	3.5	61	mA	* <sup>3</sup> When all peripheral clocks are on
					2.9	60	mA	* <sup>3</sup> When all peripheral clocks are off
			Normal operation * <sup>6</sup> , * <sup>8</sup> (sub oscillation)	* <sup>5</sup> 32 kHz	0.47	58	mA	* <sup>3</sup> When all peripheral clocks are on
					0.46	58	mA	* <sup>3</sup> When all peripheral clocks are off
			Normal operation * <sup>6</sup> (built-in low-speed CR)	* <sup>5</sup> 100 kHz	0.51	58	mA	* <sup>3</sup> When all peripheral clocks are on
					0.50	58	mA	* <sup>3</sup> When all peripheral clocks are off

1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

8: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

**Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2**

Parameter	Symbol	Pin Name	Conditions	Frequency <sup>*4</sup>	Value		Unit	Remarks
					Typ <sup>*1</sup>	Max <sup>*2</sup>		
Power supply current	I <sub>CCS</sub>	VCC	Sleep operation <sup>*5</sup> (PLL)	180 MHz	58	116	mA	*3 When all peripheral clocks are on
				160 MHz	52	110	mA	
				144 MHz	48	106	mA	
				120 MHz	40	98	mA	
				100 MHz	35	93	mA	
				80 MHz	28	86	mA	
				60 MHz	22	80	mA	
				40 MHz	16	74	mA	
				20 MHz	9.7	67	mA	
				8 MHz	6.2	64	mA	
				4 MHz	5.0	63	mA	*3 When all peripheral clocks are off
				180 MHz	30	88	mA	
				160 MHz	27	85	mA	
				144 MHz	25	83	mA	
				120 MHz	21	79	mA	
				100 MHz	18	76	mA	
				80 MHz	15	73	mA	
				60 MHz	12	70	mA	
				40 MHz	9.3	67	mA	
				20 MHz	6.2	64	mA	
8 MHz	4.5	62	mA					
4 MHz	4.0	62	mA					

 1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

 2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-6 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK**

Parameter	Symbol	Pin Name	Conditions	Frequency <sup>*4</sup>	Value		Unit	Remarks
					Typ <sup>*1</sup>	Max <sup>*2</sup>		
Power supply current	I <sub>CCS</sub>	VCC	Sleep operation <sup>*5</sup> (PLL)	72 MHz	32	90	mA	*3 When all peripheral clocks are on
				60 MHz	27	85	mA	
				48 MHz	23	81	mA	
				36 MHz	18	76	mA	
				24 MHz	13	71	mA	
				12 MHz	8.5	66	mA	
				8 MHz	6.9	64	mA	
				4 MHz	5.3	63	mA	
				72 MHz	15	73	mA	*3 When all peripheral clocks are off
				60 MHz	13	71	mA	
				48 MHz	11	69	mA	
				36 MHz	9.3	67	mA	
				24 MHz	7.3	65	mA	
				12 MHz	5.4	63	mA	
				8 MHz	4.7	62	mA	
				4 MHz	4.1	62	mA	

1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)



**Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (Other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2**

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>4</sup>	Value		Unit	Remarks
					Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CCS</sub>	VCC	Sleep operation * <sup>5</sup> (main oscillation)	4 MHz	2.6	60	mA	* <sup>3</sup> When all peripheral clocks are on
					2.0	60	mA	* <sup>3</sup> When all peripheral clocks are off
			Sleep operation (built-in High-speed CR)	4 MHz	2.0	60	mA	* <sup>3</sup> When all peripheral clocks are on
					1.3	59	mA	* <sup>3</sup> When all peripheral clocks are off
			Sleep operation * <sup>6</sup> (sub oscillation)	32 kHz	0.46	58	mA	* <sup>3</sup> When all peripheral clocks are on
					0.45	58	mA	* <sup>3</sup> When all peripheral clocks are off
			Sleep operation (built-in low-speed CR)	100 kHz	0.47	58	mA	* <sup>3</sup> When all peripheral clocks are on
					0.46	58	mA	* <sup>3</sup> When all peripheral clocks are off

1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

3: When all ports are fixed.

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

**Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode**

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks	
					Typ* <sup>1</sup>	Max* <sup>2</sup>			
Power supply current	I <sub>CCH</sub>	VCC	Stop mode	-	0.41	1.9	mA	*3, *4 T <sub>A</sub> = +25°C	
					-	18	mA	*3, *4 T <sub>A</sub> = +85°C	
					-	26	mA	*3, *4 T <sub>A</sub> = +105°C	
	I <sub>CCT</sub>		Timer mode* <sup>5</sup> (main oscillation)	4 MHz	1.4	2.9	mA	*3, *4 T <sub>A</sub> = +25°C	
					-	19	mA	*3, *4 T <sub>A</sub> = +85°C	
					-	27	mA	*3, *4 T <sub>A</sub> = +105°C	
			Timer mode (built-in High-speed CR)	4 MHz	0.71	2.2	mA	*3, *4 T <sub>A</sub> = +25°C	
					-	19	mA	*3, *4 T <sub>A</sub> = +85°C	
					-	27	mA	*3, *4 T <sub>A</sub> = +105°C	
			Timer mode* <sup>6</sup> (sub oscillation)	32 kHz	0.41	1.9	mA	*3, *4 T <sub>A</sub> = +25°C	
					-	18	mA	*3, *4 T <sub>A</sub> = +85°C	
					-	27	mA	*3, *4 T <sub>A</sub> = +105°C	
					0.42	1.9	mA	*3, *4 T <sub>A</sub> = +25°C	
					-	18	mA	*3, *4 T <sub>A</sub> = +85°C	
					-	27	mA	*3, *4 T <sub>A</sub> = +105°C	
			I <sub>CCR</sub>	RTC mode* <sup>6</sup> (sub oscillation)	32 kHz	0.42	1.9	mA	*3, *4 T <sub>A</sub> = +25°C
						-	18	mA	*3, *4 T <sub>A</sub> = +85°C
						-	27	mA	*3, *4 T <sub>A</sub> = +105°C

1: V<sub>CC</sub> = 3.3 V

2: V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: When LVD is off

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

**Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode**

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CCHD</sub>	VCC	Deep standby Stop mode (When RAM is off)	-	89	162	μA	*3, *4 T <sub>A</sub> = +25°C
					-	1689	μA	*3, *4 T <sub>A</sub> = +85°C
					-	2189	μA	*3, *4 T <sub>A</sub> = +105°C
			Deep standby Stop mode (When RAM is on)		101	245	μA	*3, *4 T <sub>A</sub> = +25°C
					-	2401	μA	*3, *4 T <sub>A</sub> = +85°C
					-	3223	μA	*3, *4 T <sub>A</sub> = +105°C
	I <sub>CCRD</sub>		Deep standby RTC mode <sup>*6</sup> (When RAM is off)	32 kHz	93	166	μA	*3, *4 T <sub>A</sub> = +25°C
					-	1693	μA	*3, *4 T <sub>A</sub> = +85°C
					-	2193	μA	*3, *4 T <sub>A</sub> = +105°C
			Deep standby RTC mode <sup>*6</sup> (When RAM is on)		105	249	μA	*3, *4 T <sub>A</sub> = +25°C
					-	2405	μA	*3, *4 T <sub>A</sub> = +85°C
					-	3227	μA	*3, *4 T <sub>A</sub> = +105°C

1: V<sub>CC</sub> = 3.3 V

2: V<sub>CC</sub> = 5.5 V

3: When all ports are fixed

4: When LVD is off

5: When sub oscillation is off

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

**Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/Erase**

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	$I_{CC\text{LVD}}$	VCC	At operation	-	4	7	$\mu\text{A}$	For occurrence of interrupt
MainFlash memory write/erase current	$I_{CC\text{FLASH}}$		At write/erase	-	13.4	15.9	mA	*1

1: When programming or erase in flash memory, Flash Memory Write/Erase current ( $I_{CC\text{FLASH}}$ ) is added to the Power supply current ( $I_{CC}$ ).

**Table 12-11 Peripheral Current Dissipation**

Clock System	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			45	90	180		
HCLK	GPIO	All ports	0.69	1.39	2.76	mA	$T_A=+25^\circ\text{C}$ , $V_{CC}=3.3\text{ V}$
	DMAC	-	0.74	1.46	2.83		
	DSTC	-	0.58	1.13	2.12		
	External bus I/F	-	0.23	0.44	0.87		
	SD card I/F	-	0.56	1.10	2.18		
	CAN	1 ch	0.09	0.10	0.12		
	USB	1 ch	0.41	0.83	1.64		
	Ethernet-MAC	-	1.52	2.97	5.84		
PCLK1	Base timer	4 ch	0.38	0.76	1.50	mA	$T_A=+25^\circ\text{C}$ , $V_{CC}=3.3\text{ V}$
	Multi-functional timer/PPG	1 unit/4 ch	0.72	1.43	2.83		
	Quadrature position/revolution counter	1 unit	0.06	0.12	0.22		
	A/D converter	1 unit	0.31	0.61	1.22		
PCLK2	Multi-function serial	1 ch	0.36	0.72	-	mA	$T_A=+25^\circ\text{C}$ , $V_{CC}=3.3\text{ V}$
	IC Card Interface	1 ch	0.27	0.54	-		
	I2S clock generator	1 ch	0.26	0.53	-		

## 12.3.2 Pin Characteristics

( $V_{CC} = \text{USB}_{V_{CC}0} = \text{USB}_{V_{CC}1} = \text{ETH}_{V_{CC}} = \text{AV}_{CC} = 2.7\text{V to } 5.5\text{V}$ ,  $V_{SS} = \text{AV}_{SS} = 0\text{V}$ )

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	$V_{IHS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
			-	$\text{ETH}_{V_{CC}} \times 0.8$	-	$\text{ETH}_{V_{CC}} + 0.3$	V	
		MADATAxx	$V_{CC} > 3.0\text{ V}$ , $V_{CC} \leq 3.6\text{ V}$ ,	2.4	-	$V_{CC} + 0.3$	V	At External Bus
		5V tolerant input pin	-	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
		Input pin doubled as I <sup>2</sup> C Fm+	-	$V_{CC} \times 0.7$	-	$V_{SS} + 5.5$	V	
		TTL Schmitt input pin	-	2.0	-	$\text{ETH}_{V_{CC}} + 0.3$	V	
L level input voltage (hysteresis input)	$V_{ILS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
			-	$V_{SS} - 0.3$	-	$\text{ETH}_{V_{CC}} \times 0.2$	V	
		5V tolerant input pin	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		Input pin doubled as I <sup>2</sup> C Fm+	-	$V_{SS}$	-	$V_{CC} \times 0.3$	V	
		TTL Schmitt input pin	-	$V_{SS} - 0.3$	-	0.8	V	
H level output voltage	$V_{OH}$	4 mA type	$V_{CC} \geq 4.5\text{ V}$ , $I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5\text{ V}$ , $I_{OH} = -2\text{ mA}$					
			$\text{ETH}_{V_{CC}} \geq 4.5\text{ V}$ , $I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	-	$\text{ETH}_{V_{CC}}$	V	
			$\text{ETH}_{V_{CC}} < 4.5\text{ V}$ , $I_{OH} = -2\text{ mA}$					
		8 mA type	$V_{CC} \geq 4.5\text{ V}$ , $I_{OH} = -8\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5\text{ V}$ , $I_{OH} = -4\text{ mA}$					
			$\text{ETH}_{V_{CC}} \geq 4.5\text{ V}$ , $I_{OH} = -8\text{ mA}$	$\text{ETH}_{V_{CC}} - 0.5$	-	$\text{ETH}_{V_{CC}}$	V	
			$\text{ETH}_{V_{CC}} < 4.5\text{ V}$ , $I_{OH} = -4\text{ mA}$					
		12 mA type	$V_{CC} \geq 4.5\text{ V}$ , $I_{OH} = -12\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5\text{ V}$ , $I_{OH} = -8\text{ mA}$					
The pin doubled as USB I/O	$\text{USB}_{V_{CC}} \geq 4.5\text{ V}$ , $I_{OH} = -20.5\text{ mA}$	$\text{USB}_{V_{CC}} - 0.4$	-	$\text{USB}_{V_{CC}}$	V	*1		
	$\text{USB}_{V_{CC}} < 4.5\text{ V}$ , $I_{OH} = -13.0\text{ mA}$							
The pin doubled as I <sup>2</sup> C Fm+	$V_{CC} \geq 4.5\text{ V}$ , $I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	At GPIO		
	$V_{CC} < 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$							

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks		
				Min	Typ	Max				
L level output voltage	$V_{OL}$	4 mA type	$V_{CC} \geq 4.5 V$ , $I_{OL} = 4 mA$	$V_{SS}$	-	0.4	V			
			$V_{CC} < 4.5 V$ , $I_{OL} = 2 mA$							
			$ETHV_{CC} \geq 4.5 V$ , $I_{OL} = 4 mA$	$V_{SS}$	-	0.4			V	
			$RTHV_{CC} < 4.5 V$ , $I_{OL} = 2 mA$							
		8 mA type	$V_{CC} \geq 4.5 V$ , $I_{OL} = 8 mA$	$V_{SS}$	-	0.4	V			
			$V_{CC} < 4.5 V$ , $I_{OL} = 4 mA$							
			$ETHV_{CC} \geq 4.5 V$ , $I_{OL} = 8 mA$	$V_{SS}$	-	0.4			V	
			$RTHV_{CC} < 4.5 V$ , $I_{OL} = 4 mA$							
		12 mA type	$V_{CC} \geq 4.5 V$ , $I_{OL} = 12 mA$	$V_{SS}$	-	0.4	V			
			$V_{CC} < 4.5 V$ , $I_{OL} = 8 mA$							
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5 V$ , $I_{OL} = 18.5 mA$	$V_{SS}$	-	0.4			V	*1
			$USBV_{CC} < 4.5 V$ , $I_{OL} = 10.5 mA$							
		The pin doubled as I <sup>2</sup> C Fm+	$V_{CC} \geq 4.5 V$ , $I_{OL} = 4 mA$	$V_{SS}$	-	0.4	V	At GPIO		
			$V_{CC} < 4.5 V$ , $I_{OL} = 3 mA$							
$V_{CC} \leq 4.5 V$ , $I_{OL} = 20 mA$	At I <sup>2</sup> C Fm+									
Input leak current	$I_{IL}$	-	-	- 5	-	+ 5	$\mu A$			
Pull-up resistor value	$R_{PU}$	Pull-up pin	$V_{CC} \geq 4.5 V$	25	50	100	k $\Omega$			
			$V_{CC} < 4.5 V$	30	80	200				
Input capacitance	$C_{IN}$	Other than VCC, USBVCC0, USBVCC1, ETHVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF			

1: USBV<sub>CC0</sub> and USBV<sub>CC1</sub> are described as USBV<sub>CC</sub>.

**12.4 AC Characteristics**

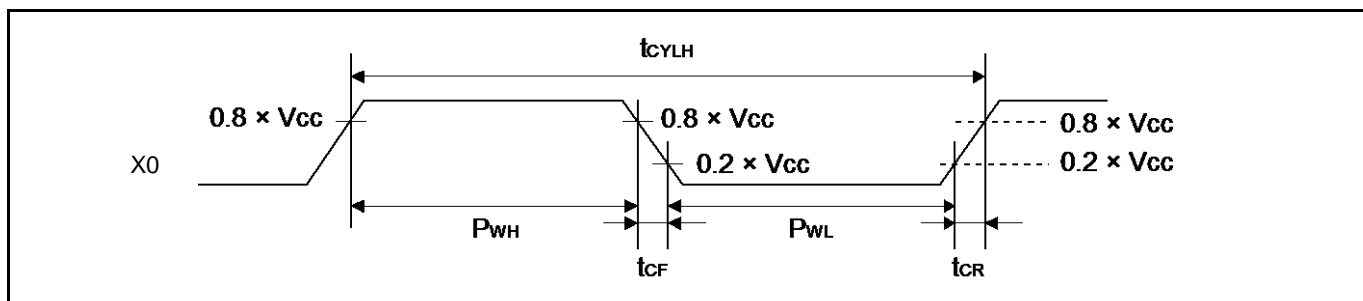
**12.4.1 Main Clock Input Characteristics**

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$f_{CH}$	X0, X1	$V_{CC} \geq 4.5 V$	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5 V$	4	20		
			$V_{CC} \geq 4.5 V$	4	48	MHz	When using external clock
			$V_{CC} < 4.5 V$	4	20		
Input clock cycle	$t_{CYLH}$		$V_{CC} \geq 4.5 V$	20.83	250	ns	When using external clock
			$V_{CC} < 4.5 V$	50	250		
Input clock pulse width	-		$P_{WH}/t_{CYLH}$ , $P_{WL}/t_{CYLH}$	45	55	%	When using external clock
Input clock rise time and fall time	$t_{CF}$ , $t_{CR}$		-	-	5	ns	When using external clock
Internal operating clock <sup>*1</sup> frequency	$f_{CC}$	-	-	-	180	MHz	Base clock (HCLK/FCLK)
	$f_{CP0}$	-	-	-	90	MHz	APB0bus clock <sup>**2</sup>
	$f_{CP1}$	-	-	-	180	MHz	APB1bus clock <sup>**2</sup>
	$f_{CP2}$	-	-	-	90	MHz	APB2bus clock <sup>**2</sup>
Internal operating clock <sup>*1</sup> cycle time	$t_{CYCC}$	-	-	5.56	-	ns	Base clock (HCLK/FCLK)
	$t_{CYCP0}$	-	-	11.1	-	ns	APB0bus clock <sup>**2</sup>
	$t_{CYCP1}$	-	-	5.56	-	ns	APB1bus clock <sup>**2</sup>
	$t_{CYCP2}$	-	-	11.1	-	ns	APB2bus clock <sup>**2</sup>

1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

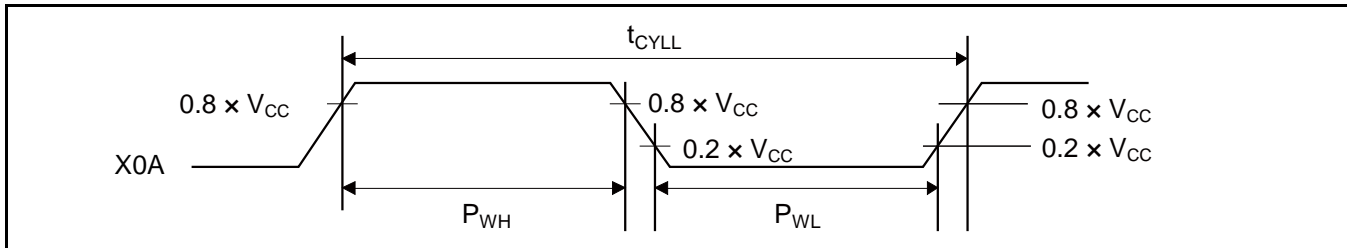
2: For more about each APB bus to which each peripheral is connected, see 1. S6E2G Series Block Diagram in this data sheet.



**12.4.2 Sub Clock Input Characteristics**
 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	$t_{CYLL}$		-	10	-	31.25	$\mu s$	When using external clock
Input clock pulse width	-		$P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}$	45	-	55	%	When using external clock

\*: For more information about crystal oscillator, see Sub crystal oscillator in 9. Handling Devices.


**12.4.3 Built-In CR Oscillation Characteristics**
**Built-In High-speed CR**
 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRH}$	$T_J = -20^\circ C \text{ to } +105^\circ C$	3.92	4	4.08	MHz	When trimmed *1
		$T_J = -40^\circ C \text{ to } +125^\circ C$	3.88	4	4.12		
		$T_J = -40^\circ C \text{ to } +125^\circ C$	2.9	4	5		When not trimmed
Frequency stabilization time	$t_{CRWT}$	-	-	-	30	$\mu s$	*2

1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

**Built-In Low-speed CR**
 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRL}$	-	50	100	150	kHz	



**12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)**
*(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)*

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* <sup>1</sup> (lock up time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f <sub>PLLO</sub>	200	-	400	MHz	
Main PLL clock frequency* <sup>2</sup>	f <sub>CLKPLL</sub>	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

**12.4.5 Operating Conditions of USB/Ethernet PLL (in the Case of Using Main Clock for Input Clock of PLL)**
*(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)*

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time <sup>1</sup> (lock up time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f <sub>PLLO</sub>	200	-	400	MHz	USB/Ethernet
USB/Ethernet clock frequency <sup>2</sup>	f <sub>CLKPLL</sub>	-	-	50	MHz	After the M frequency division

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

## 12.4.6 Operating Conditions of Main PLL (in the Case of Using Built-in High-Speed CR Clock for Input Clock of Main PLL)

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time <sup>*1</sup> (lock up time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	95	multiplier	
PLL macro oscillation clock frequency	f <sub>PLLO</sub>	190	-	400	MHz	
Main PLL clock frequency <sup>*2</sup>	f <sub>CLKPLL</sub>	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

**Note:**

- The High-speed CR clock (CLKHC) should be set with frequency/temperature trimming to act as the source clock of the Main PLL.

## 12.4.7 Reset Input Characteristics

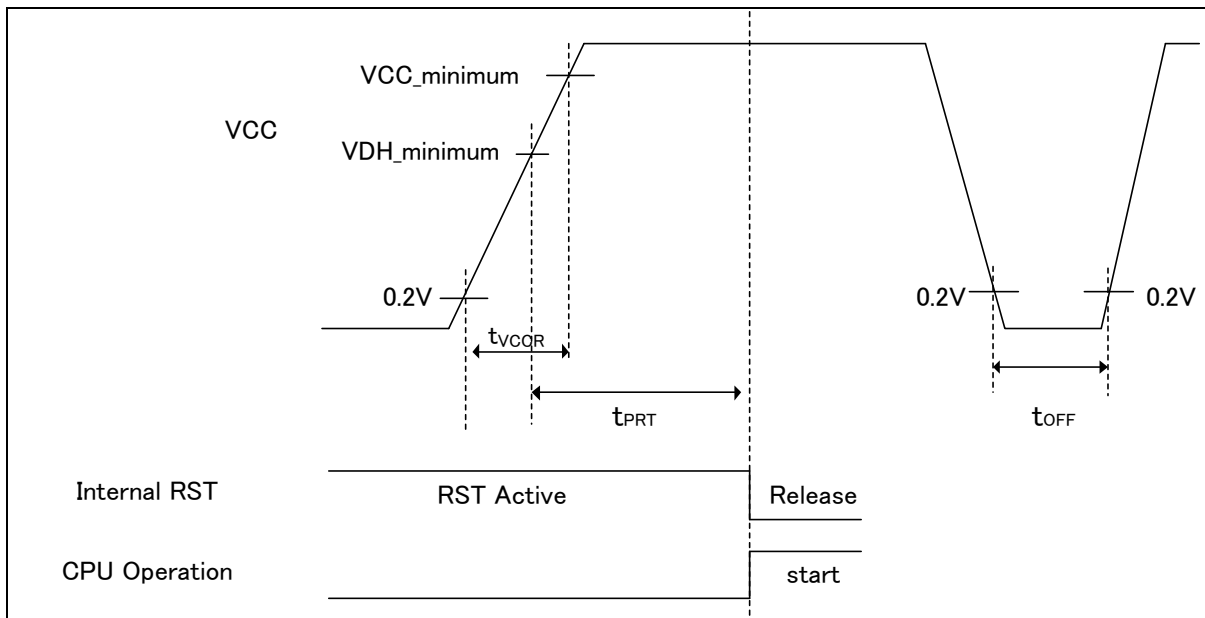
(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Reset input time	t <sub>INITX</sub>	INITX	-	500	-	ns	

## 12.4.8 Power-On Reset Timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Typ		
Power supply rise time	$t_{VCCR}$	VCC	0	-	ms	
Power supply shut down time	$t_{OFF}$		1	-	ms	
Time until releasing Power-on reset	$t_{PRT}$		0.33	0.60	ms	



### Glossary

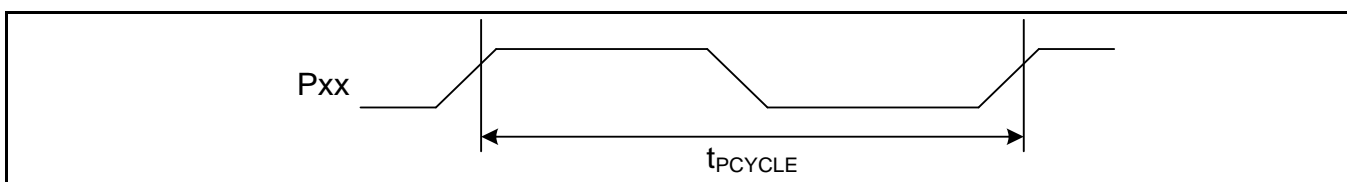
- $V_{CC\_minimum}$ : minimum  $V_{CC}$  of recommended operating conditions
- $V_{DH\_minimum}$ : minimum release voltage of low-voltage detection reset  
See 12.7. Low-Voltage Detection Characteristics.

## 12.4.9 GPIO Output Characteristics

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Output frequency	$t_{PCYCLE}$	Pxx*	$V_{CC} \geq 4.5V$	-	50	MHz	
			$V_{CC} < 4.5V$	-	32	MHz	

\*: GPIO is a target.



12.4.10 External Bus Timing

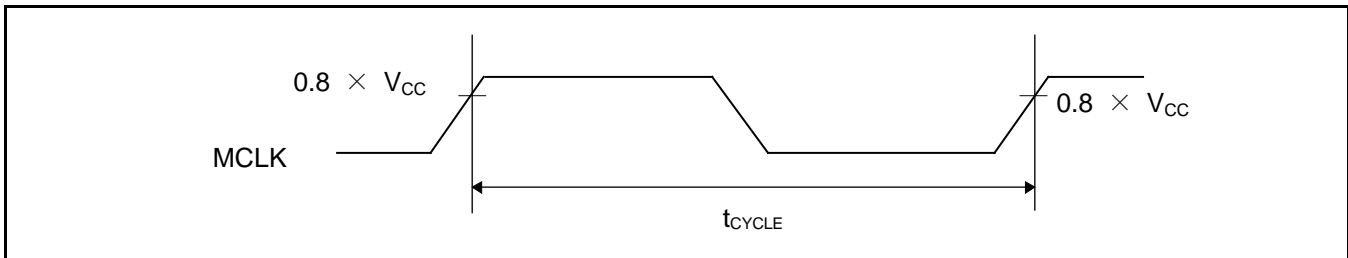
External Bus Clock Output Characteristics

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Output frequency	$t_{CYCLE}$	MCLKOUT <sup>*1</sup>		-	50 <sup>*2</sup>	MHz	

1: The external bus clock (MCLKOUT) is a divided clock of HCLK.

For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main Part (002-04856).

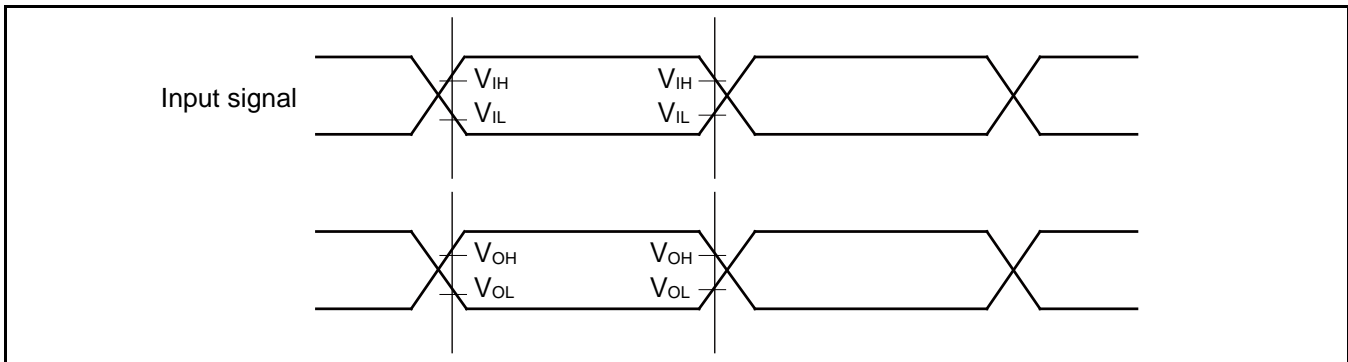
2: Generate MCLKOUT at setting more than four divisions when the AHB bus clock exceeds 100 MHz.



External Bus Signal I/O Characteristics

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	$V_{IH}$	-	$0.8 \times V_{CC}$	V	
	$V_{IL}$		$0.2 \times V_{CC}$	V	
Signal output characteristics	$V_{OH}$		$0.8 \times V_{CC}$	V	
	$V_{OL}$		$0.2 \times V_{CC}$	V	

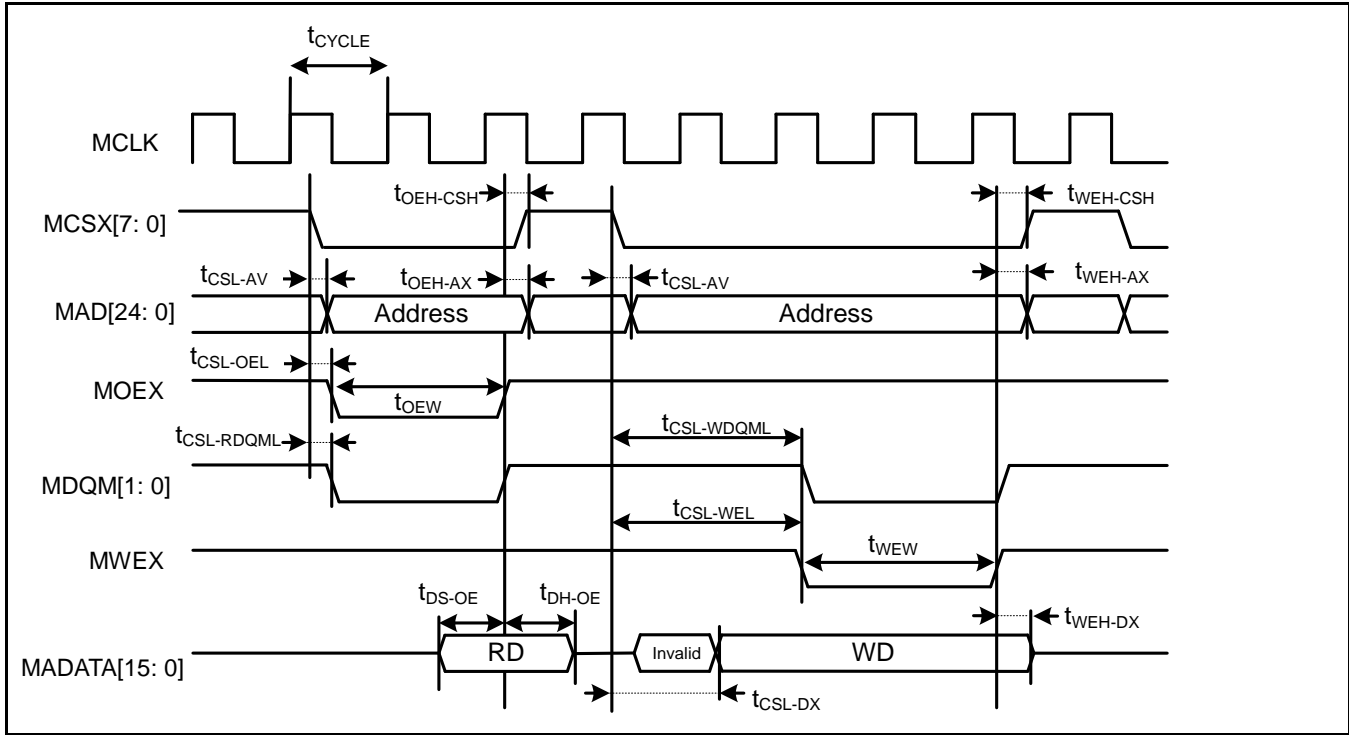


**Separate Bus Access Asynchronous SRAM Mode**
 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Minimum pulse width	$t_{OE\overline{W}}$	MOEX	-	$MCLK \times n - 3$	-	ns	
MCSX $\downarrow \rightarrow$ Address output delay time	$t_{CSL - AV}$	MCSX[7: 0], MAD[24: 0]	-	-9	+9	ns	
MOEX $\uparrow \rightarrow$ Address hold time	$t_{OE\overline{H} - AX}$	MOEX, MAD[24: 0]	-	0	$MCLK \times m + 9$	ns	
MCSX $\downarrow \rightarrow$ MOEX $\downarrow$ delay time	$t_{CSL - OEL}$	MOEX, MCSX[7: 0]	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MOEX $\uparrow \rightarrow$ MCSX $\uparrow$ time	$t_{OE\overline{H} - CSH}$		-	0	$MCLK \times m + 9$	ns	
MCSX $\downarrow \rightarrow$ MDQM $\downarrow$ delay time	$t_{CSL - RDQML}$	MCSX, MDQM[3: 0]	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
Data set up $\rightarrow$ MOEX $\uparrow$ time	$t_{DS - OE}$	MOEX, MADATA[31: 0]	-	20	-	ns	
MOEX $\uparrow \rightarrow$ Data hold time	$t_{DH - OE}$	MOEX, MADATA[31: 0]	-	0	-	ns	
MWEX Minimum pulse width	$t_{WE\overline{W}}$	MWEX	-	$MCLK \times n - 3$	-	ns	
MWEX $\uparrow \rightarrow$ Address output delay time	$t_{WE\overline{H} - AX}$	MWEX, MAD[24: 0]	-	0	$MCLK \times m + 9$	ns	
MCSX $\downarrow \rightarrow$ MWEX $\downarrow$ delay time	$t_{CSL - WEL}$	MWEX, MCSX[7: 0]	-	$MCLK \times n - 9$	$MCLK \times n + 9$	ns	
MWEX $\uparrow \rightarrow$ MCSX $\uparrow$ delay time	$t_{WE\overline{H} - CSH}$		-	0	$MCLK \times m + 9$	ns	
MCSX $\downarrow \rightarrow$ MDQM $\downarrow$ delay time	$t_{CSL - WDQML}$	MCSX, MDQM[3: 0]	-	$MCLK \times n - 9$	$MCLK \times n + 9$	ns	
MCSX $\downarrow \rightarrow$ Data output time	$t_{CSL - DX}$	MCSX, MADATA[31: 0]	-	$MCLK - 9$	$MCLK + 9$	ns	
MWEX $\uparrow \rightarrow$ Data hold time	$t_{WE\overline{H} - DX}$	MWEX, MADATA[31: 0]	-	0	$MCLK \times m + 9$	ns	

**Note:**

- When the external load capacitance  $C_L = 30 \text{ pF}$  ( $m = 0 \text{ to } 15, n = 1 \text{ to } 16$ )



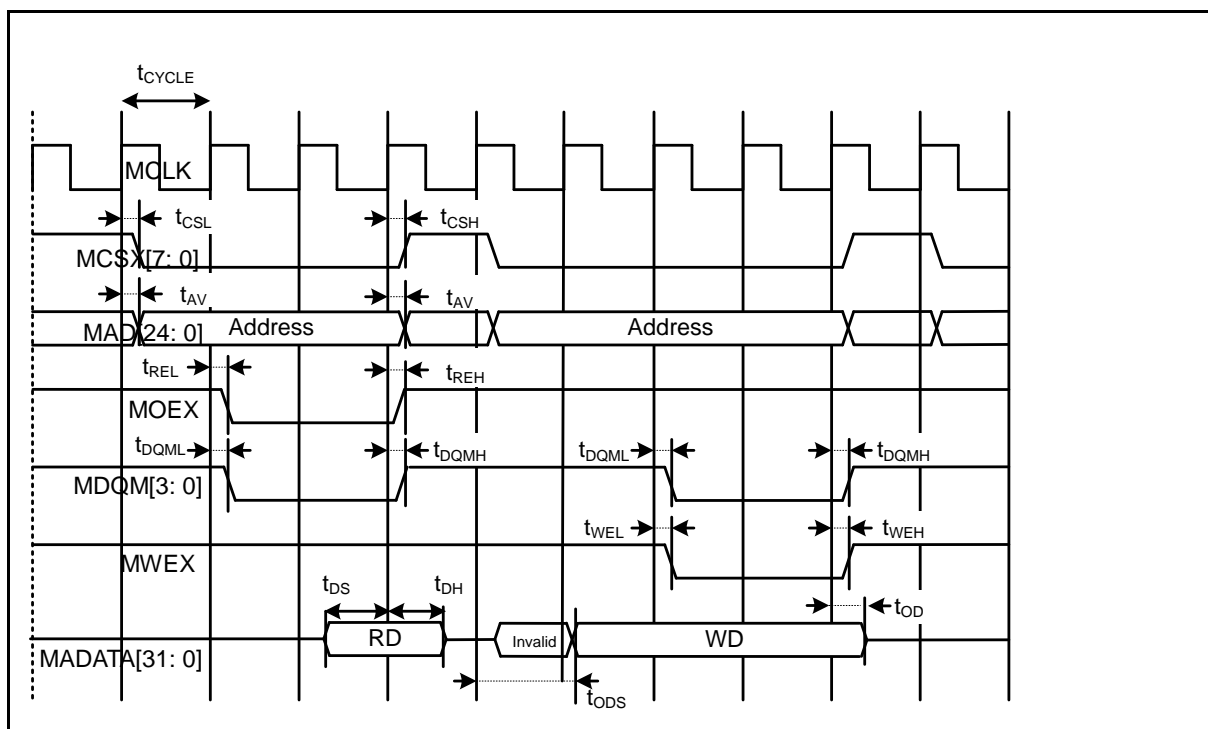
## Separate Bus Access Synchronous SRAM Mode

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	$t_{AV}$	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	$t_{CSL}$	MCLK, MCSX[7: 0]	-	1	9	ns	
	$t_{CSH}$		-	1	9	ns	
MOEX delay time	$t_{REL}$	MCLK, MOEX	-	1	9	ns	
	$t_{REH}$		-	1	9	ns	
Data set up →MCLK ↑ time	$t_{DS}$	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	$t_{DH}$	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	$t_{WEL}$	MCLK, MWEX	-	1	9	ns	
	$t_{WEH}$		-	1	9	ns	
MDQM[1: 0] delay time	$t_{DQML}$	MCLK, MDQM[3: 0]	-	1	9	ns	
	$t_{DQMH}$		-	1	9	ns	
MCLK ↑ → Data output time	$t_{ODS}$	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	$t_{OD}$	MCLK, MADATA[31: 0]	-	1	18	ns	

**Note:**

- When the external load capacitance  $CL = 30$  pF



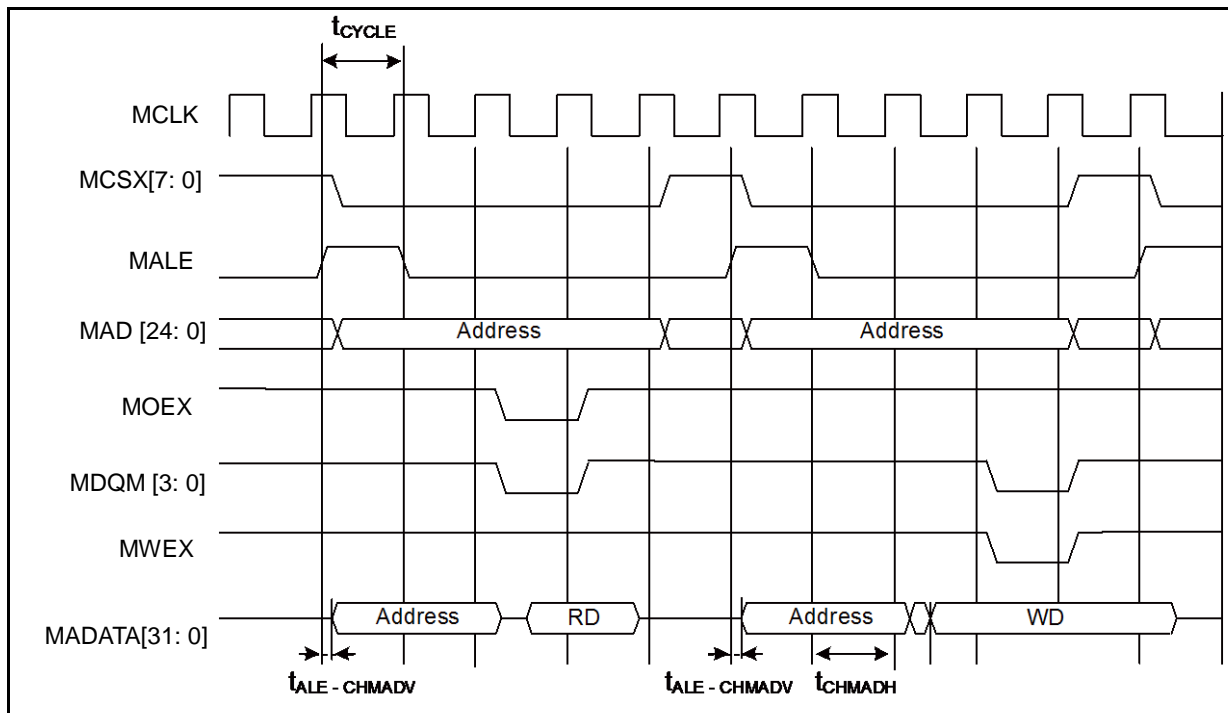
**Multiplexed Bus Access Asynchronous SRAM Mode**

 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	$t_{CHMADH}$		-	$MCLK \times n + 0$	$MCLK \times n + 10$	ns	

**Note:**

- When the external load capacitance  $C_L = 30$  pF ( $m = 0$  to  $15$ ,  $n = 1$  to  $16$ )





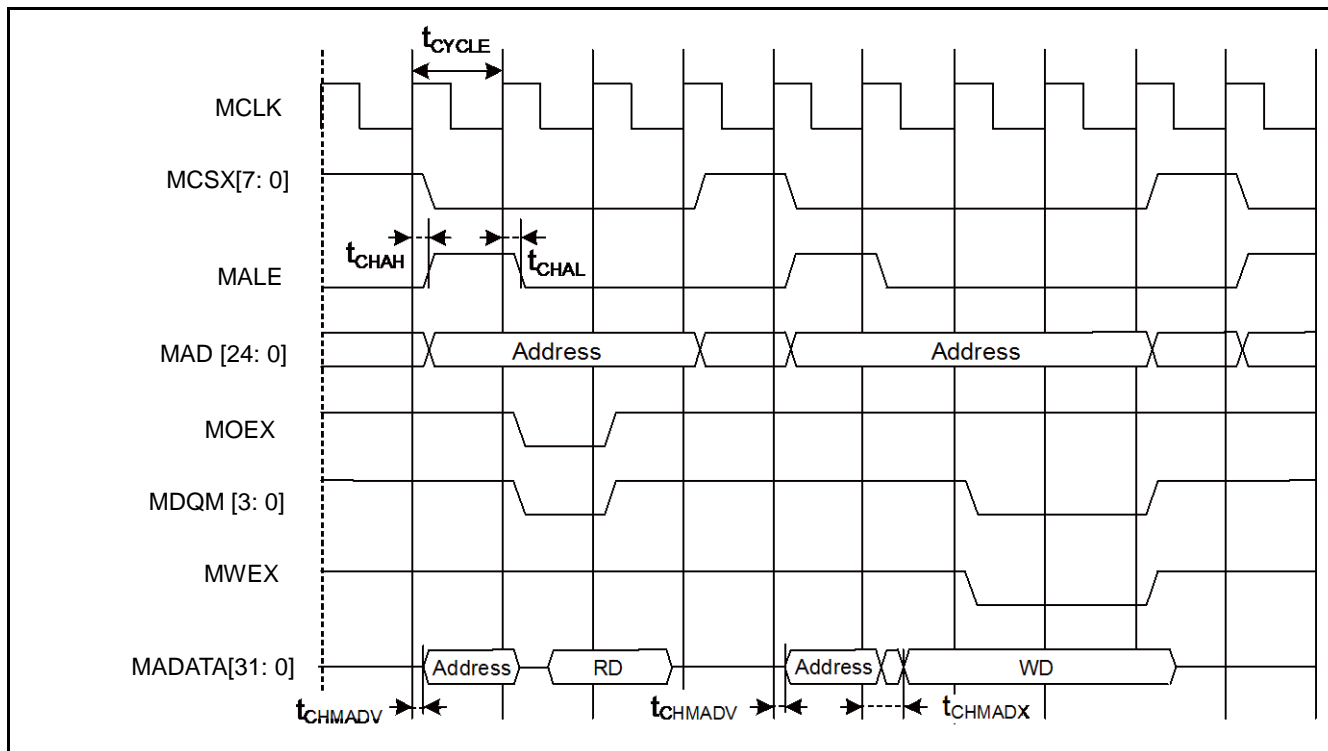
**Multiplexed Bus Access Synchronous SRAM Mode**

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	$t_{CHAL}$	MCLK, MALE	-	1	9		
	$t_{CHAH}$		-	1	9		
MCLK $\uparrow$ $\rightarrow$ Multiplexed address delay time	$t_{CHMADV}$	MCLK, MADATA[31: 0]	-	1	$t_{OD}$	ns	
MCLK $\uparrow$ $\rightarrow$ Multiplexed data output time	$t_{CHMADX}$		-	1	$t_{OD}$	ns	

**Note:**

- When the external load capacitance  $C_L = 30$  pF



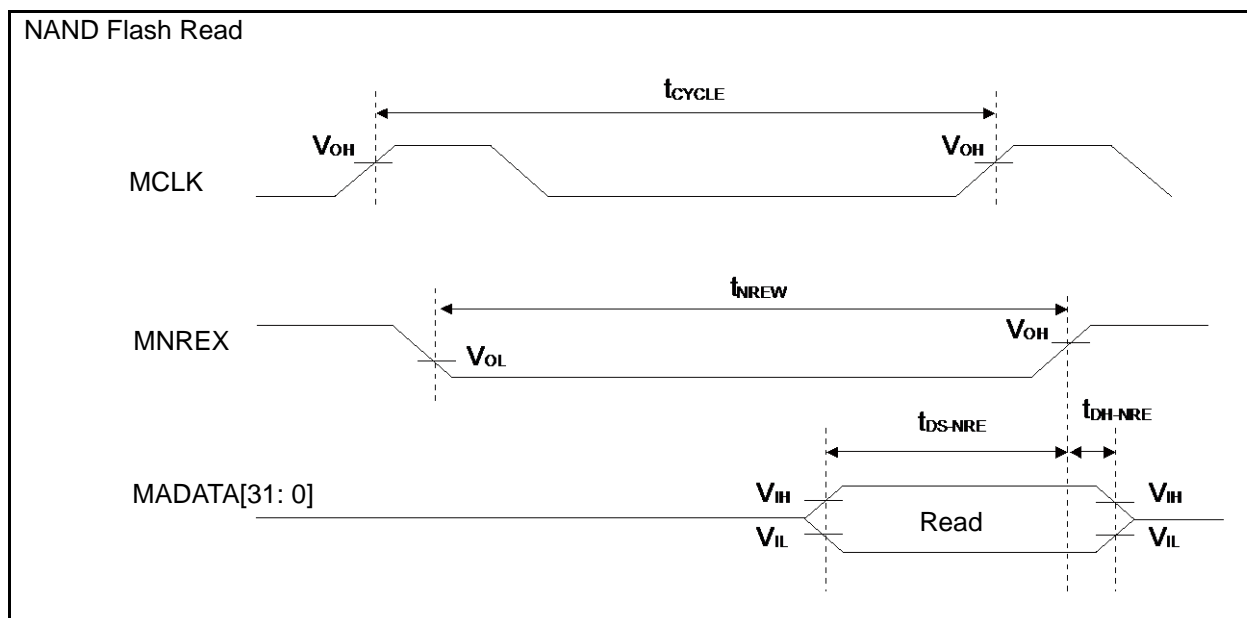
## NAND Flash Mode

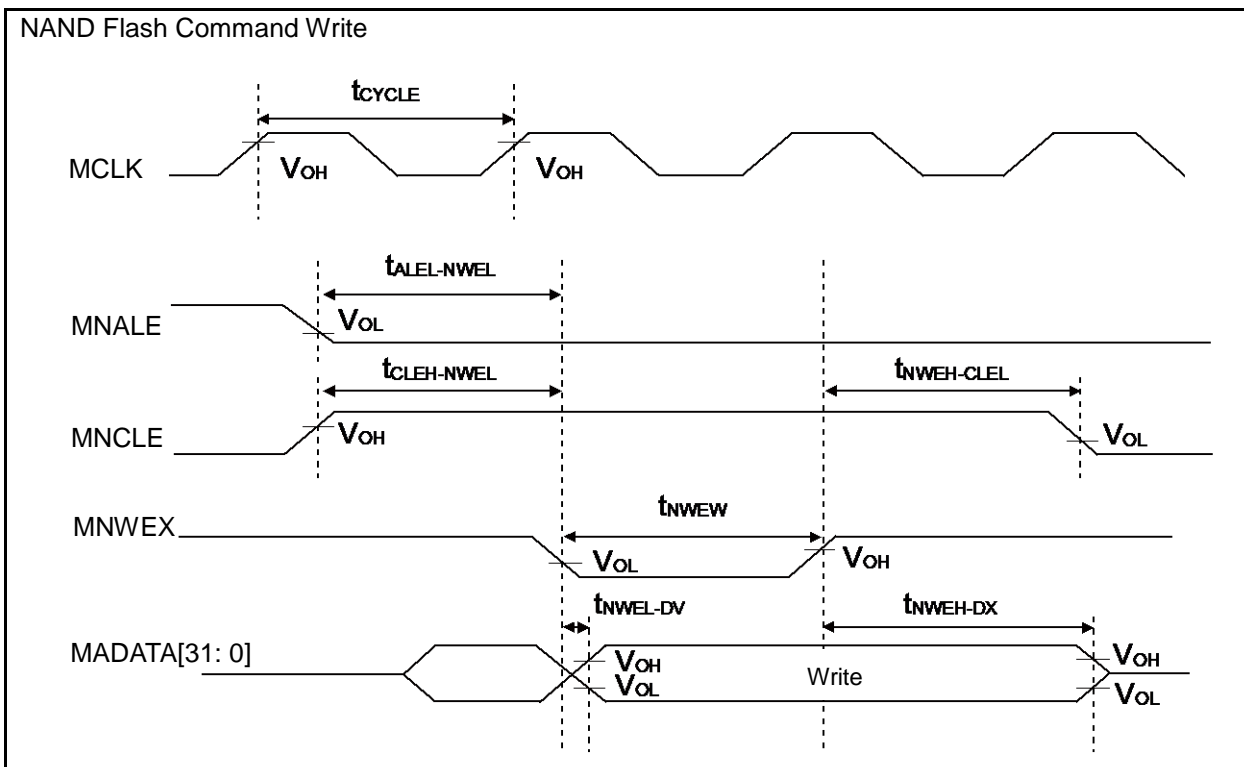
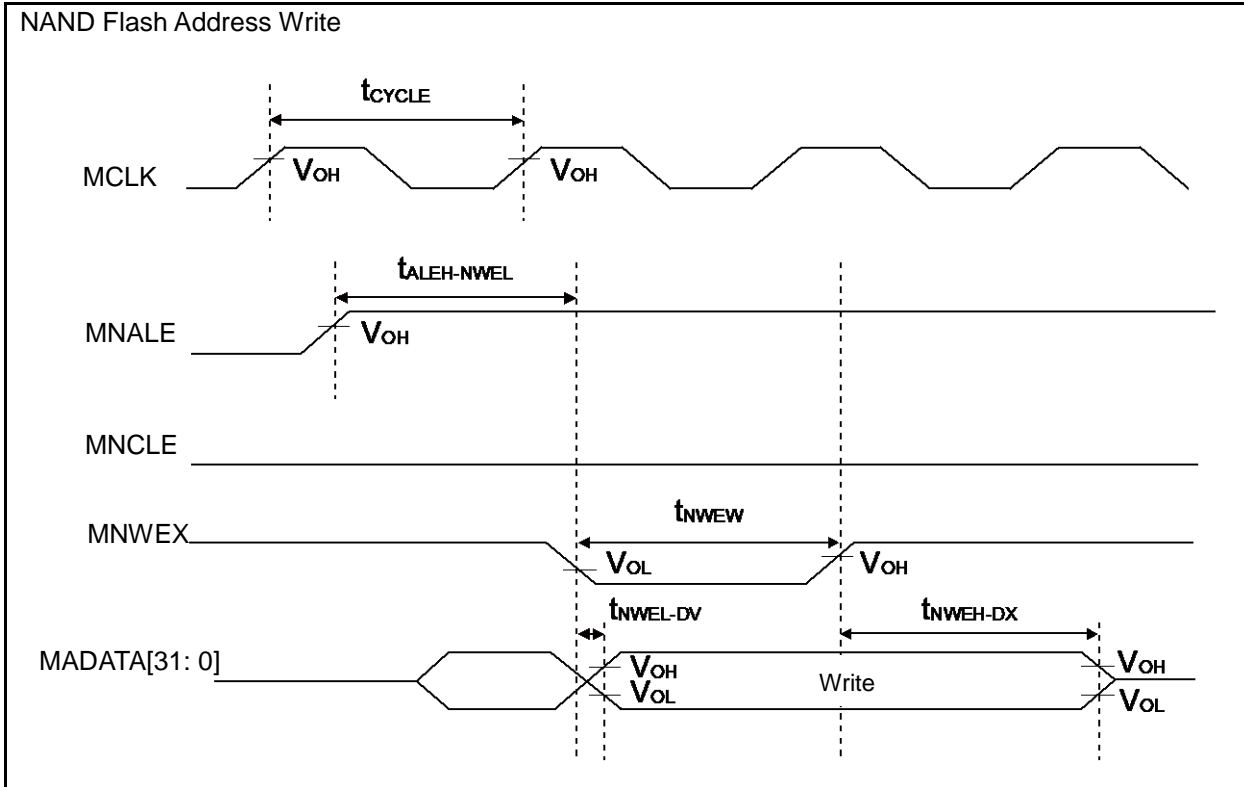
( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	$t_{NREW}$	MNREX	-	$MCLK \times n - 3$	-	ns	
Data set up → MNREX ↑ time	$t_{DS-NRE}$	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX ↑ → Data hold time	$t_{DH-NRE}$	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	$MCLK \times m + 9$	ns	
MNWEX Min pulse width	$t_{NWEW}$	MNWEX	-	$MCLK \times n - 3$	-	ns	
MNWEX ↓ → Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[31: 0]	-	-9	9	ns	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[31: 0]	-	0	$MCLK \times m + 9$	ns	

**Note:**

- When the external load capacitance  $C_L = 30$  pF ( $m = 0$  to  $15$ ,  $n = 1$  to  $16$ )



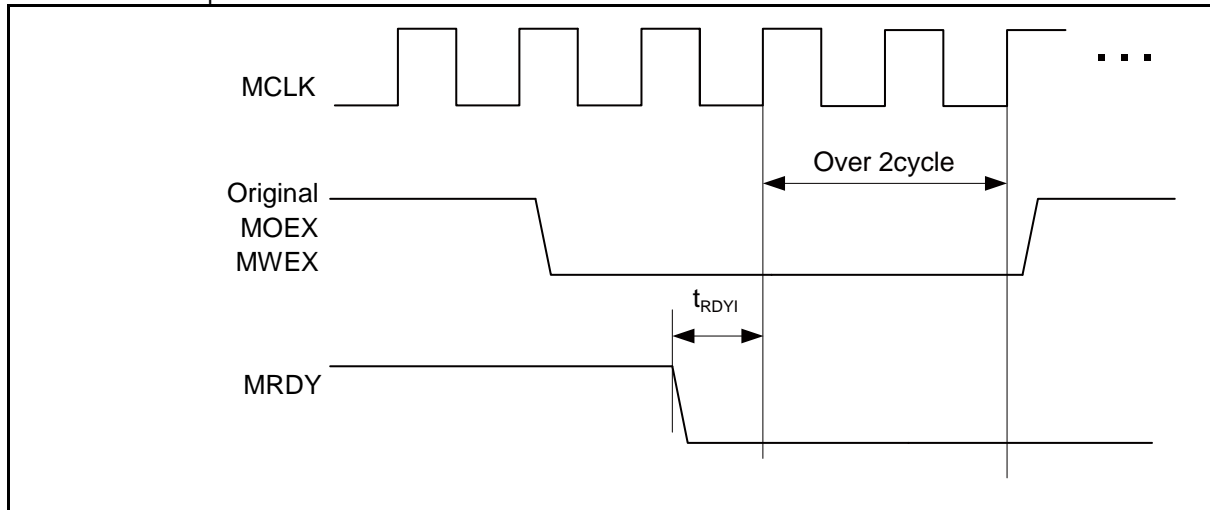


**External Ready Input Timing**

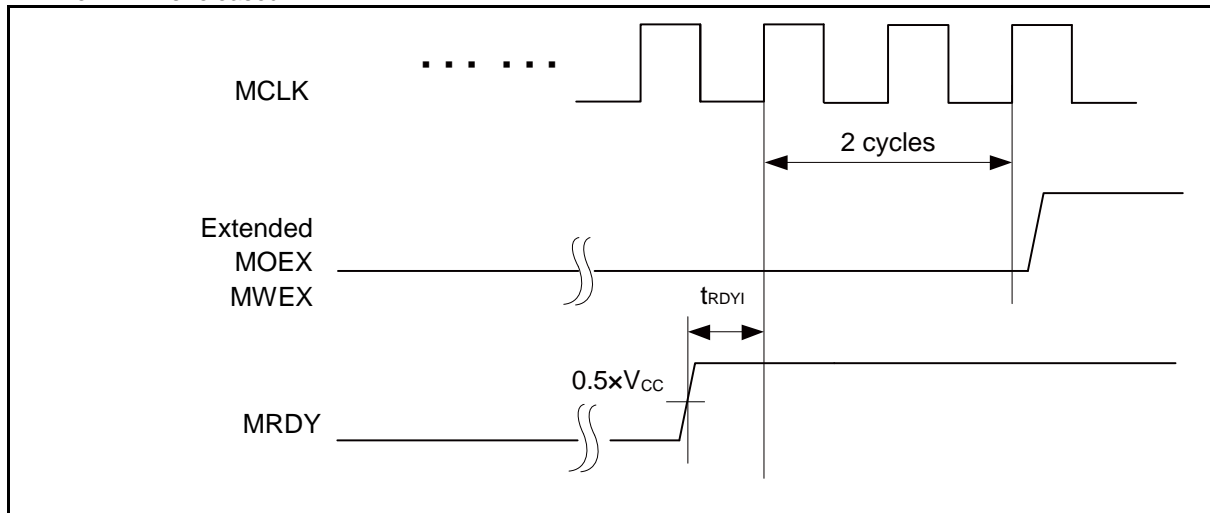
 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	$t_{RDYI}$	MCLK, MRDY	-	19	-	ns	

## ■ When RDY is input



## ■ When RDY is released



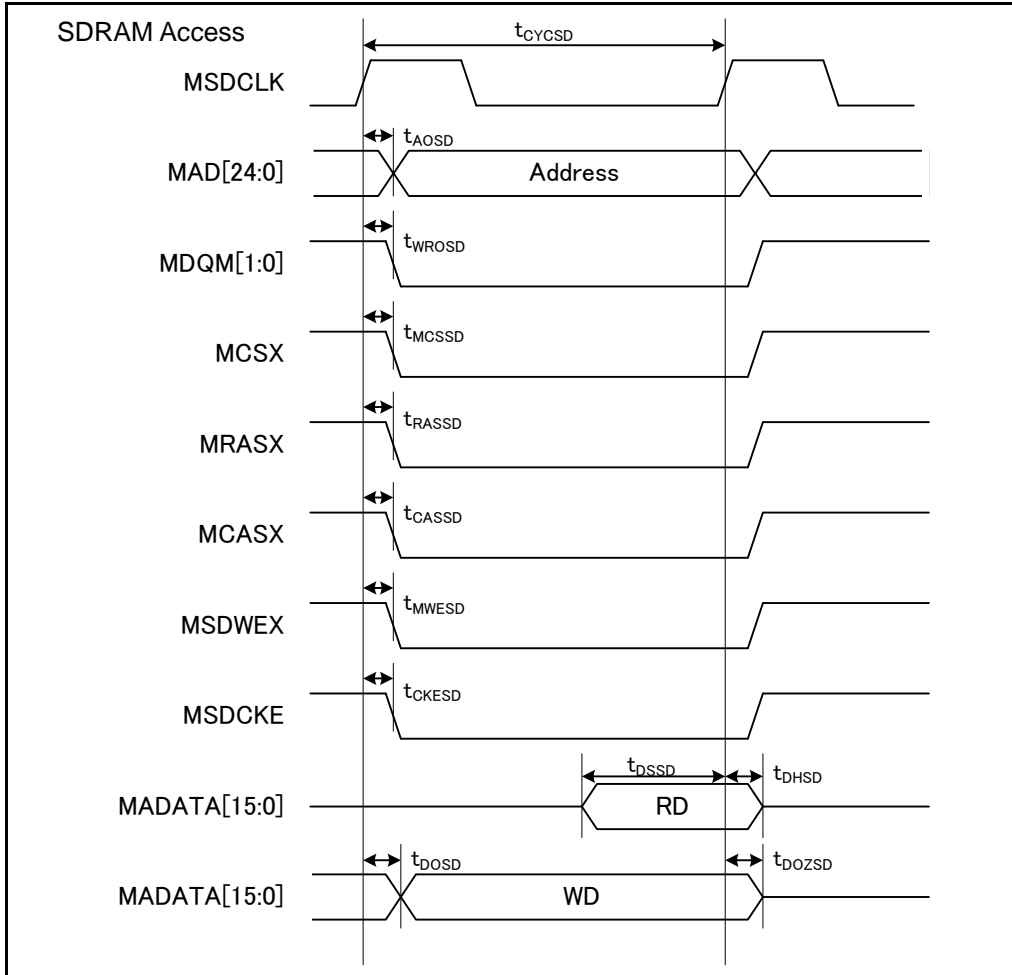
**SDRAM Mode**

 (V<sub>CC</sub> = 2.7V to 3.6V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Value	Unit		Unit	Remarks
				Min	Max		
Output frequency	t <sub>CYCS</sub> D	MSDCLK	-	-	50	MHz	
Address delay time	t <sub>AO</sub> SD	MSDCLK, MAD[15: 0]	-	2	12	ns	
MSDCLK ↑ → Data output delay time	t <sub>DO</sub> SD	MSDCLK, MADATA[31: 0]	-	2	12	ns	
MSDCLK ↑ → Data output Hi-Z time	t <sub>DOZ</sub> SD	MSDCLK, MADATA[31: 0]	-	2	19.5	ns	
MDQM[3: 0] delay time	t <sub>WRO</sub> SD	MSDCLK, MDQM[1: 0]	-	1	12	ns	
MCSX delay time	t <sub>MC</sub> SSD	MSDCLK, MCSX8	-	2	12	ns	
MRASX delay time	t <sub>RA</sub> SSD	MSDCLK, MRASX	-	2	12	ns	
MCASX delay time	t <sub>CA</sub> SSD	MSDCLK, MCASX	-	2	12	ns	
MSDWEX delay time	t <sub>MW</sub> ESD	MSDCLK, MSDWEX	-	2	12	ns	
MSDCKE delay time	t <sub>CK</sub> ESD	MSDCLK, MSDCKE	-	2	12	ns	
Data set up time	t <sub>DS</sub> SD	MSDCLK, MADATA[31: 0]	-	19	-	ns	
Data hold time	t <sub>DH</sub> SD	MSDCLK, MADATA[31: 0]	-	0	-	ns	

**Note:**

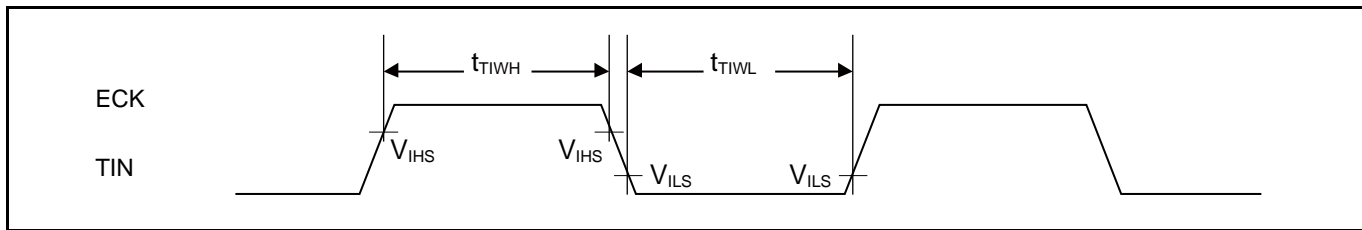
- When the external load capacitance C<sub>L</sub> = 30 pF



**12.4.11 Base Timer Input Timing**
**Timer Input Timing**

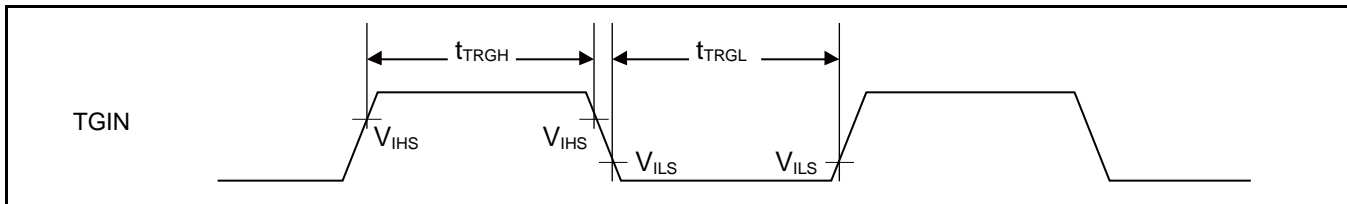
 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Condi tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	


**Trigger Input Timing**

 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Condi tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ , $t_{TRGL}$	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	


**Note:**

- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the base timer is connected, see 1. S6E2G Series Block Diagram in this data sheet.

## 12.4.12 CSIO (SPI) Timing

### Synchronous Serial (SPI = 0, SCINV = 0)

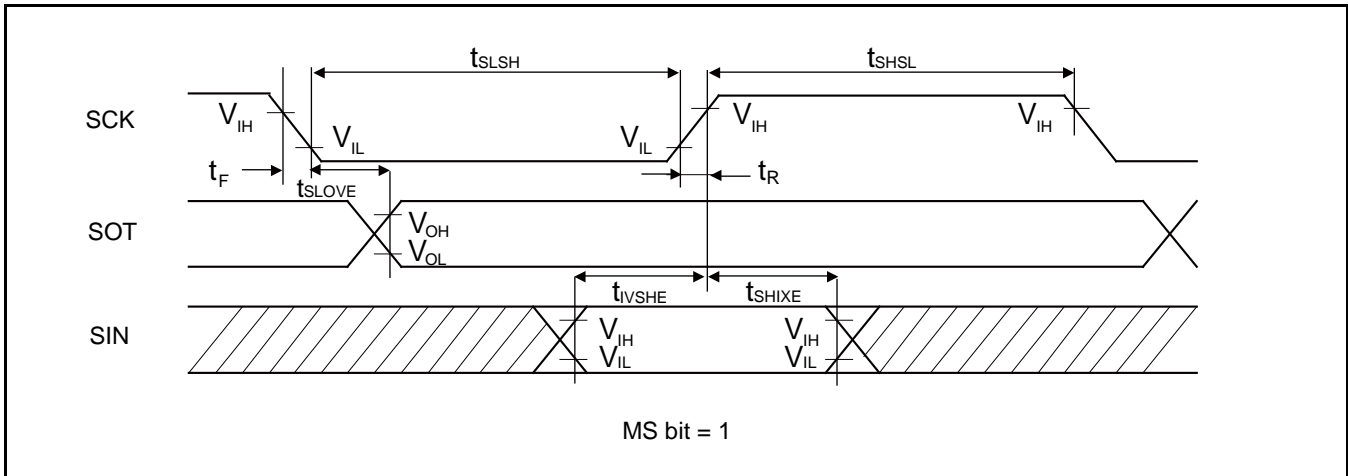
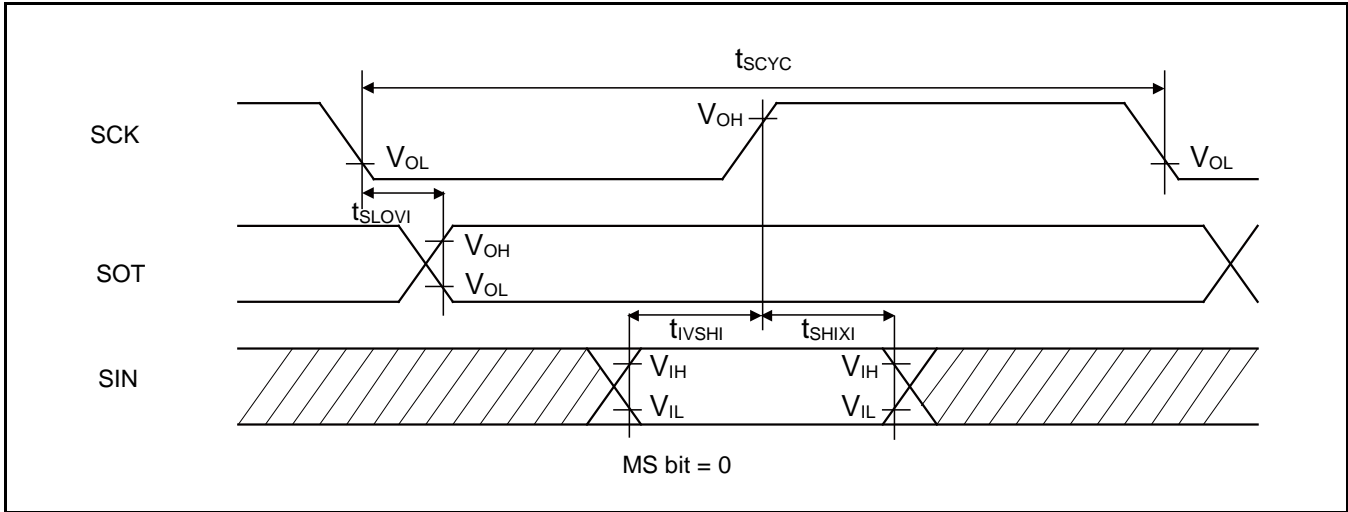
(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK <sub>↓</sub> →SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK <sub>↑</sub> setup time	t <sub>IVSHI</sub>	SCKx, SINx		50	-	30	-	ns
SCK <sub>↑</sub> →SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns	
SCK <sub>↓</sub> →SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK <sub>↑</sub> setup time	t <sub>IVSHE</sub>	SCKx, SINx		10	-	10	-	ns
SCK <sub>↑</sub> →SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

#### Notes:

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.





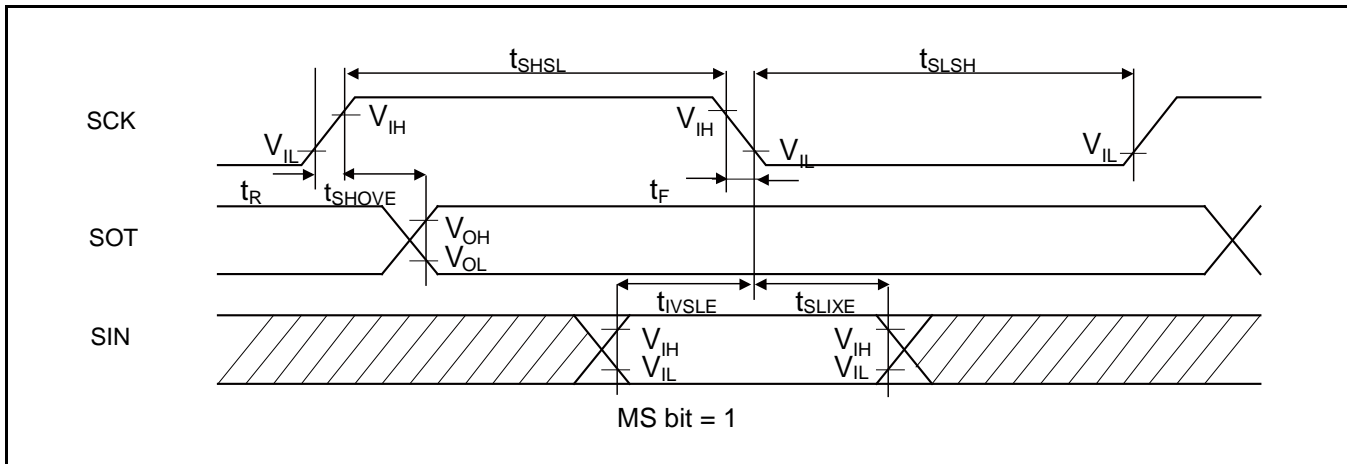
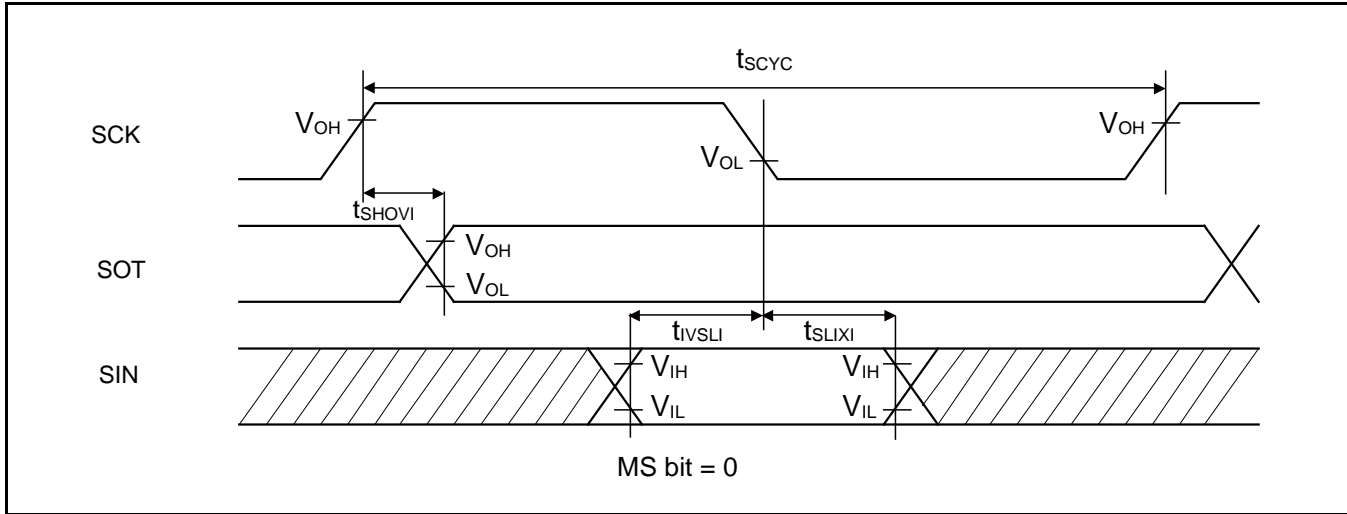
**Synchronous Serial (SPI = 0, SCINV = 1)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↑→SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns	
SCK↑→SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.



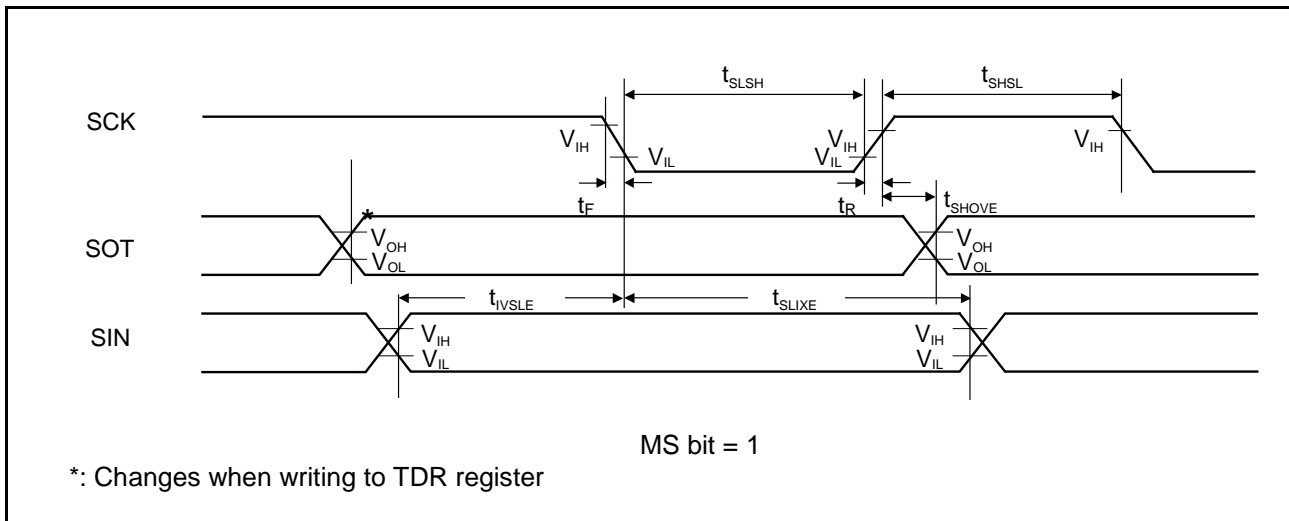
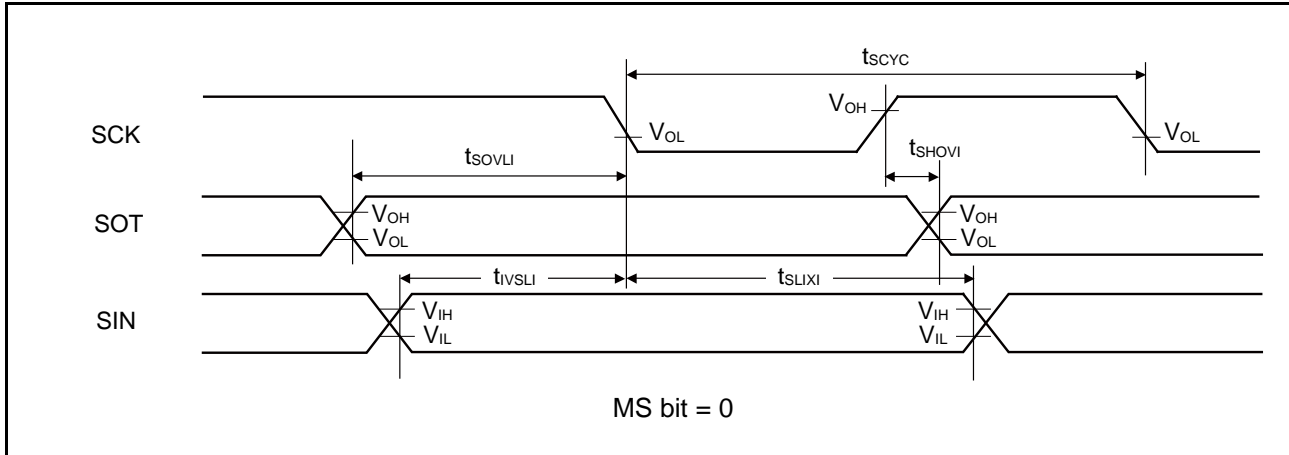
**Synchronous Serial (SPI = 1, SCINV = 0)**

 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK $\uparrow$ →SOT delay time	$t_{SHOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKx, SINx		50	-	30	-	ns
SCK $\downarrow$ →SIN hold time	$t_{SLIXI}$	SCKx, SINx		0	-	0	-	ns
SOT→SCK $\downarrow$ delay time	$t_{SOVLI}$	SCKx, SOTx		$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx		$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns	
SCK $\uparrow$ →SOT delay time	$t_{SHOVE}$	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKx, SINx		10	-	10	-	ns
SCK $\downarrow$ →SIN hold time	$t_{SLIXE}$	SCKx, SINx		20	-	20	-	ns
SCK fall time	$t_F$	SCKx		-	5	-	5	ns
SCK rise time	$t_R$	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 30$  pF.



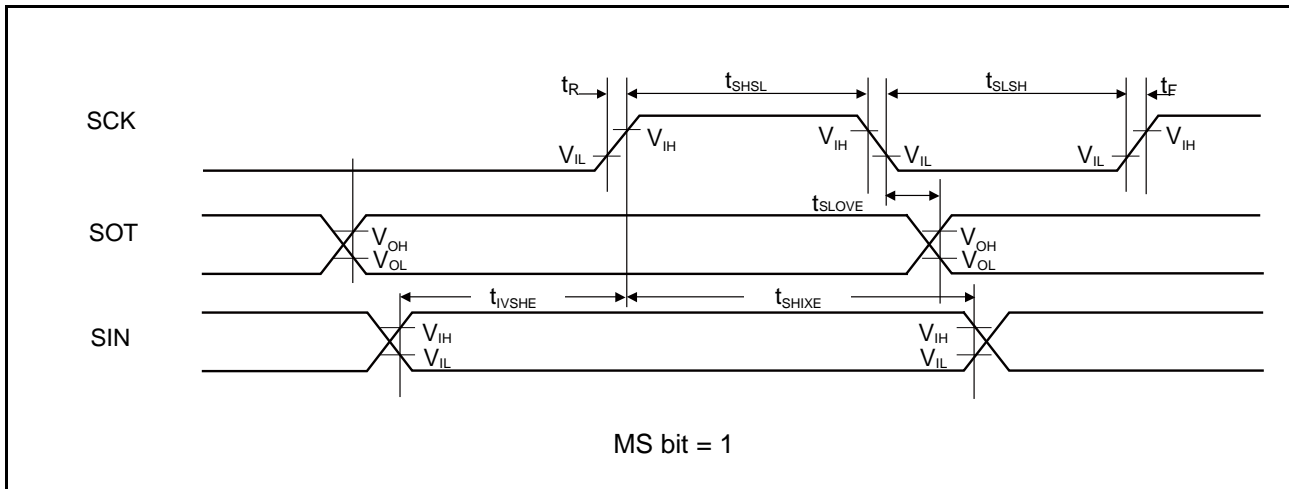
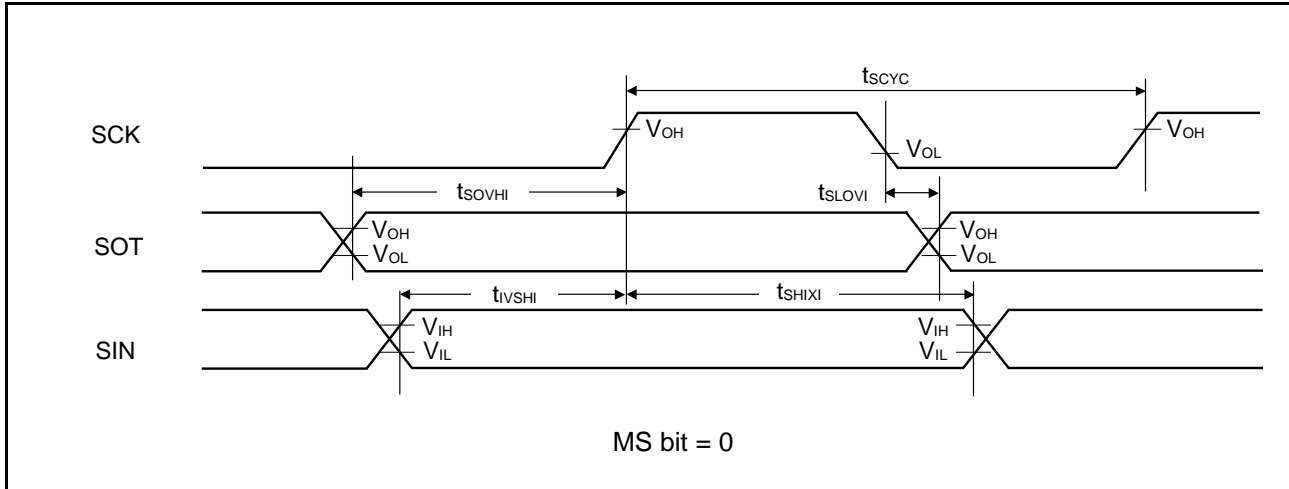
## Synchronous Serial (SPI = 1, SCINV = 1)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK $\downarrow$ →SOT delay time	$t_{SLOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK $\uparrow$ setup time	$t_{IVSHI}$	SCKx, SINx		50	-	30	-	ns
SCK $\uparrow$ →SIN hold time	$t_{SHIXI}$	SCKx, SINx		0	-	0	-	ns
SOT→SCK $\uparrow$ delay time	$t_{SOVHI}$	SCKx, SOTx		$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx		$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns	
SCK $\downarrow$ →SOT delay time	$t_{SLOVE}$	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK $\uparrow$ setup time	$t_{IVSHE}$	SCKx, SINx		10	-	10	-	ns
SCK $\uparrow$ →SIN hold time	$t_{SHIXE}$	SCKx, SINx		20	-	20	-	ns
SCK fall time	$t_F$	SCKx		-	5	-	5	ns
SCK rise time	$t_R$	SCKx		-	5	-	5	ns

### Notes:

- The above characteristics apply to CLK synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCLKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 30 pF$ .



**When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS = 0, CSLVL = 1)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t <sub>CShI</sub>		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-50 +5t <sub>CYCP</sub>	(*3)+50 +5t <sub>CYCP</sub>	(*3)-50 +5t <sub>CYCP</sub>	(*3)+50 +5t <sub>CYCP</sub>	ns
SCS↓→SCK↓ setup time	t <sub>CSSe</sub>	External shift clock operation	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCK↑→SCS↑ hold time	t <sub>CShE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDe</sub>		3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS ↓ →SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS ↑ →SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

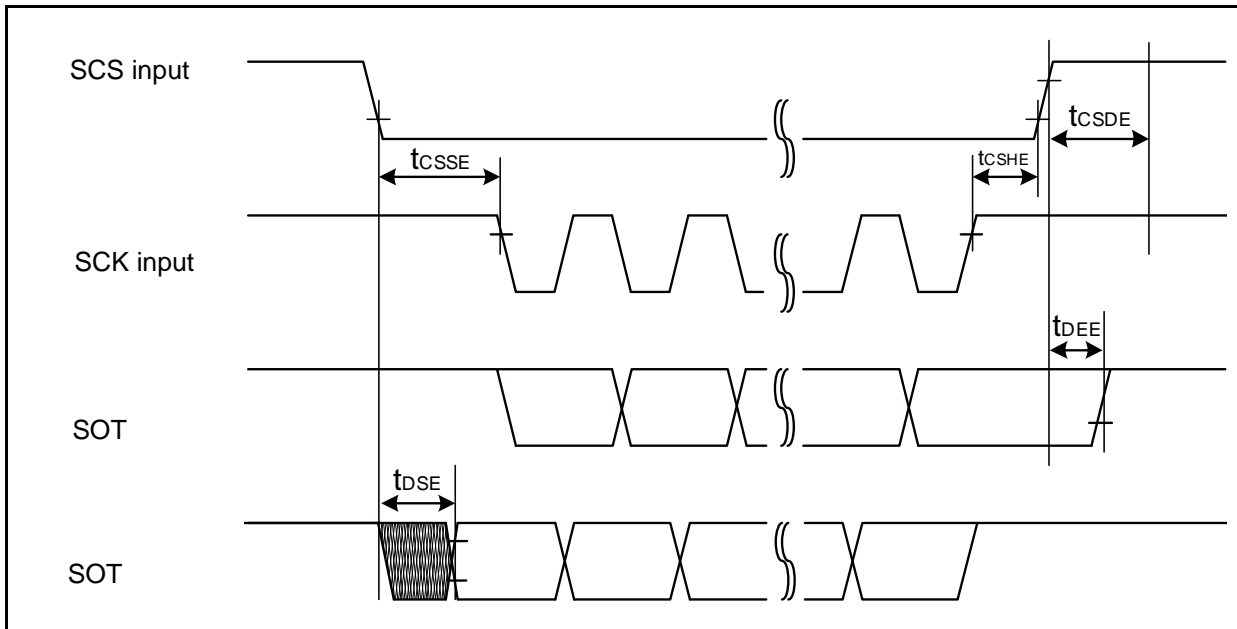
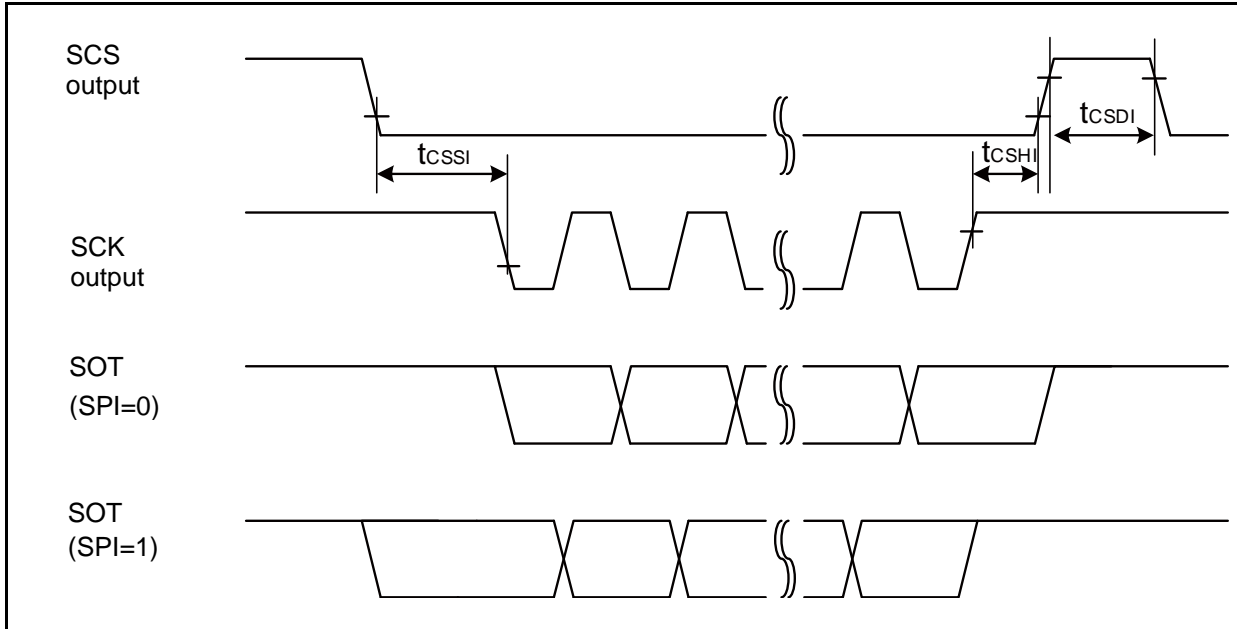
(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.





## When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS = 0, CSLVL = 1)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
			Min	Max	Min	Max	
SCS $\downarrow$ →SCK $\downarrow$ setup time	$t_{CSSI}$	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK $\uparrow$ →SCS $\uparrow$ hold time	$t_{CSHI}$		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	$t_{CSDI}$		(*3)-50 +5 $t_{CYCP}$	(*3)+50 +5 $t_{CYCP}$	(*3)-50 +5 $t_{CYCP}$	(*3)+50 +5 $t_{CYCP}$	ns
SCS $\downarrow$ →SCK $\downarrow$ setup time	$t_{CSSE}$	External shift clock operation	3 $t_{CYCP}$ +30	-	3 $t_{CYCP}$ +30	-	ns
SCK $\uparrow$ →SCS $\uparrow$ hold time	$t_{CSHE}$		0	-	0	-	ns
SCS deselect time	$t_{CSDE}$		3 $t_{CYCP}$ +30	-	3 $t_{CYCP}$ +30	-	ns
SCS $\downarrow$ →SOT delay time	$t_{DSE}$		-	40	-	40	ns
SCS $\uparrow$ →SOT delay time	$t_{DEE}$		0	-	0	-	ns

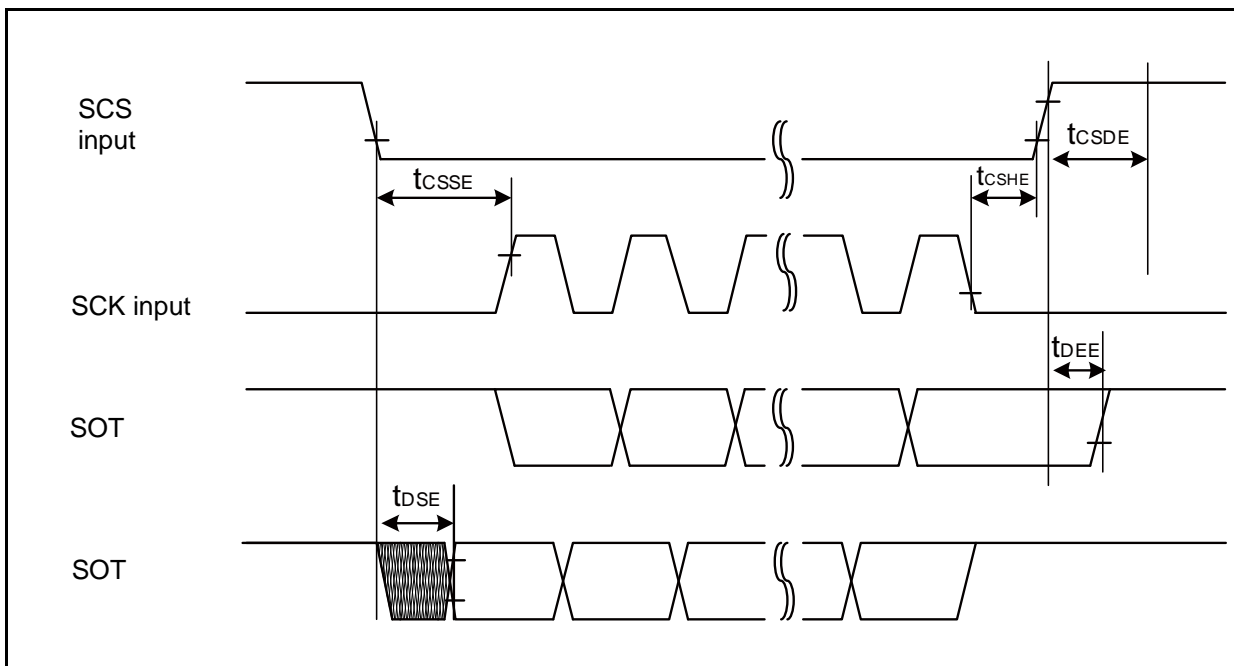
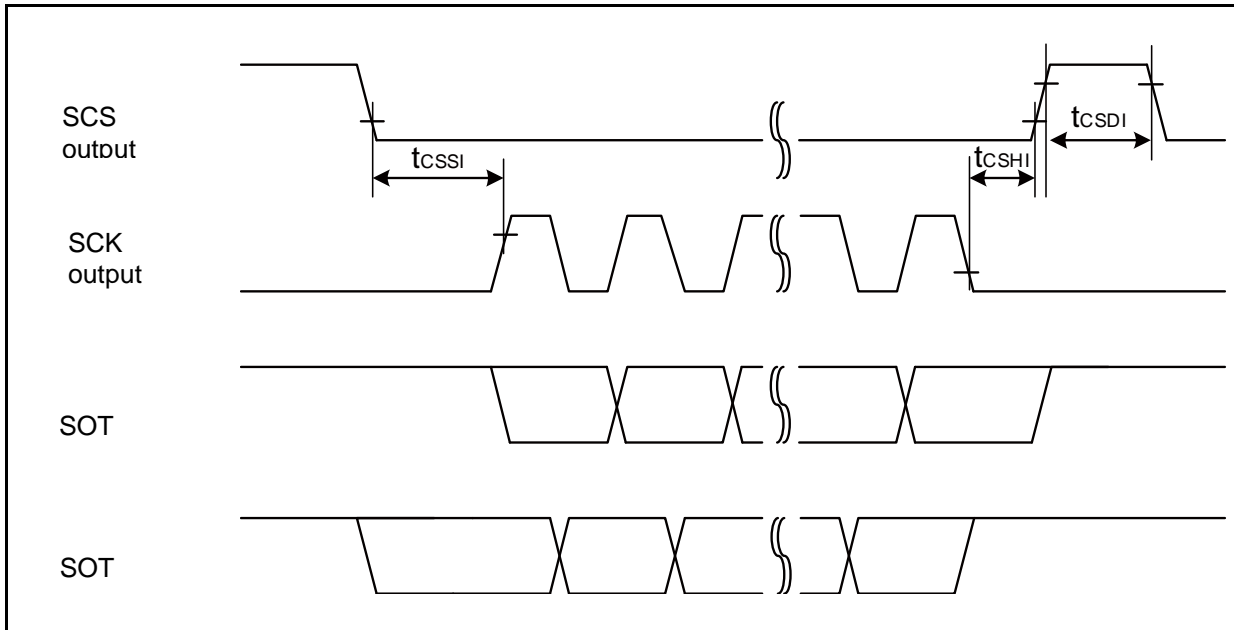
(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

### Notes:

- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance  $C_L = 30 pF$ .



## When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS = 0, CSLVL = 0)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
			Min	Max	Min	Max	
SCS $\uparrow$ →SCK $\downarrow$ setup time	$t_{CSSI}$	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK $\uparrow$ →SCS $\downarrow$ hold time	$t_{CSHI}$		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	$t_{CSDI}$		(*3)-50 +5 $t_{CYCP}$	(*3)+50 +5 $t_{CYCP}$	(*3)-50 +5 $t_{CYCP}$	(*3)+50 +5 $t_{CYCP}$	ns
SCS $\uparrow$ →SCK $\downarrow$ setup time	$t_{CSSE}$	External shift clock operation	3 $t_{CYCP}$ +30	-	3 $t_{CYCP}$ +30	-	ns
SCK $\uparrow$ →SCS $\downarrow$ hold time	$t_{CSHE}$		0	-	0	-	ns
SCS deselect time	$t_{CSDE}$		3 $t_{CYCP}$ +30	-	3 $t_{CYCP}$ +30	-	ns
SCS $\uparrow$ →SOT delay time	$t_{DSE}$		-	40	-	40	ns
SCS $\downarrow$ →SOT delay time	$t_{DEE}$		0	-	0	-	ns

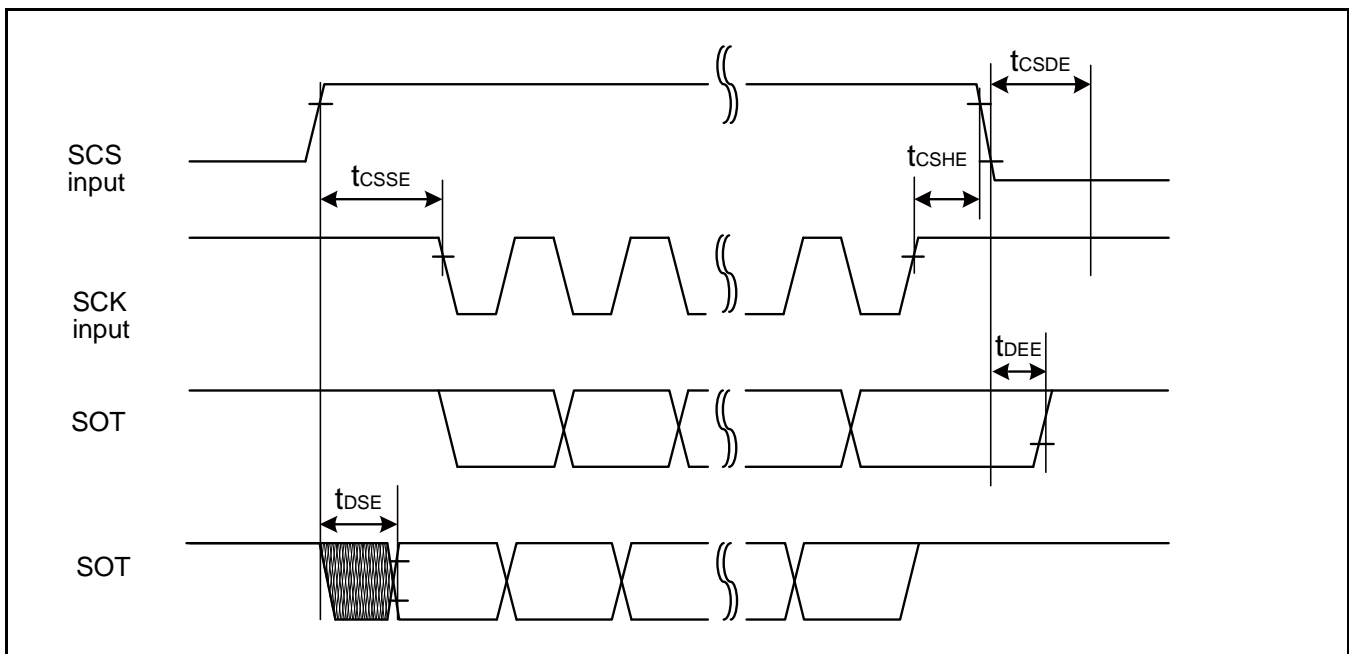
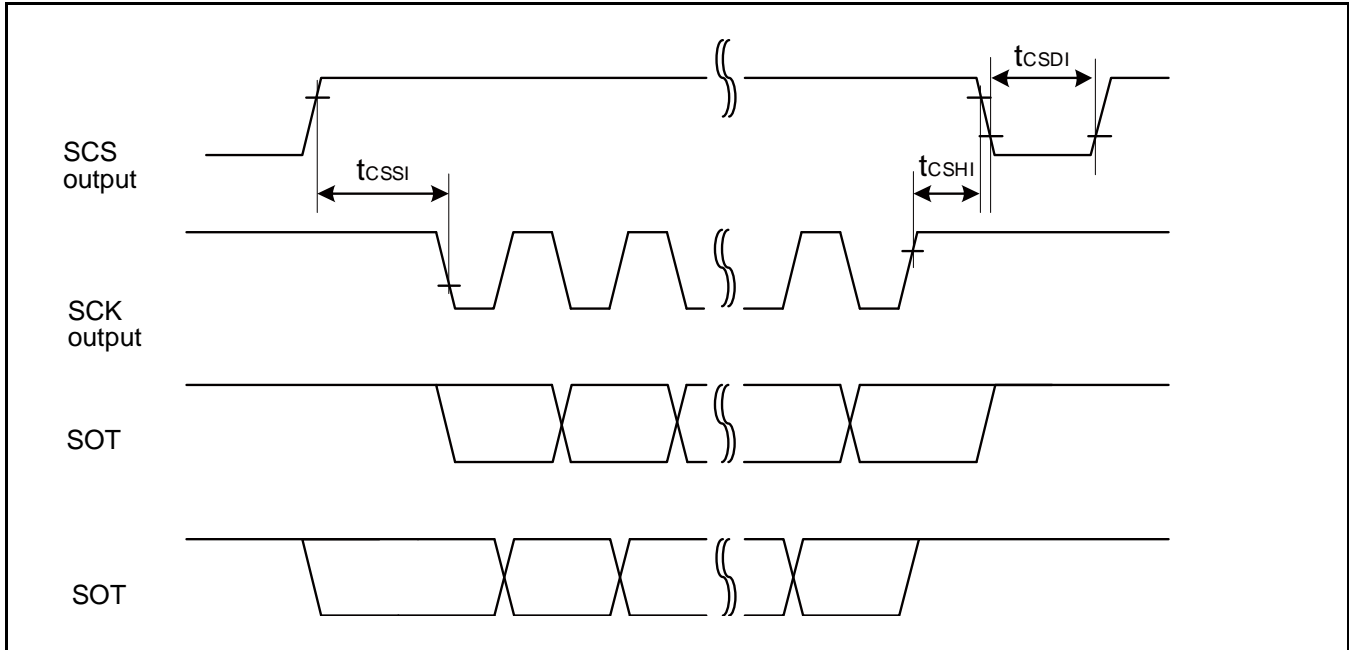
(\*1): CSSU bit value $\times$ serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value $\times$ serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value $\times$ serial chip select timing operating clock cycle [ns]

### Notes:

- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance  $C_L = 30 pF$ .



## When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS = 0, CSLVL = 0)

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	VCC < 4.5 V		VCC ≥ 4.5 V		Units
			Min	Max	Min	Max	
SCS ↑ → SCK ↑ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK ↓ → SCS ↓ hold time	t <sub>CShI</sub>		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-50 +5t <sub>CYCP</sub>	(*3)+50 +5t <sub>CYCP</sub>	(*3)-50 +5t <sub>CYCP</sub>	(*3)+50 +5t <sub>CYCP</sub>	ns
SCS ↑ → SCK ↑ setup time	t <sub>CSSe</sub>	External shift clock operation	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCK ↓ → SCS ↓ hold time	t <sub>CShE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDe</sub>		3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS ↑ → SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS ↓ → SOT delay time	t <sub>DSE</sub>		0	-	0	-	ns

(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

### Notes:

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



## High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

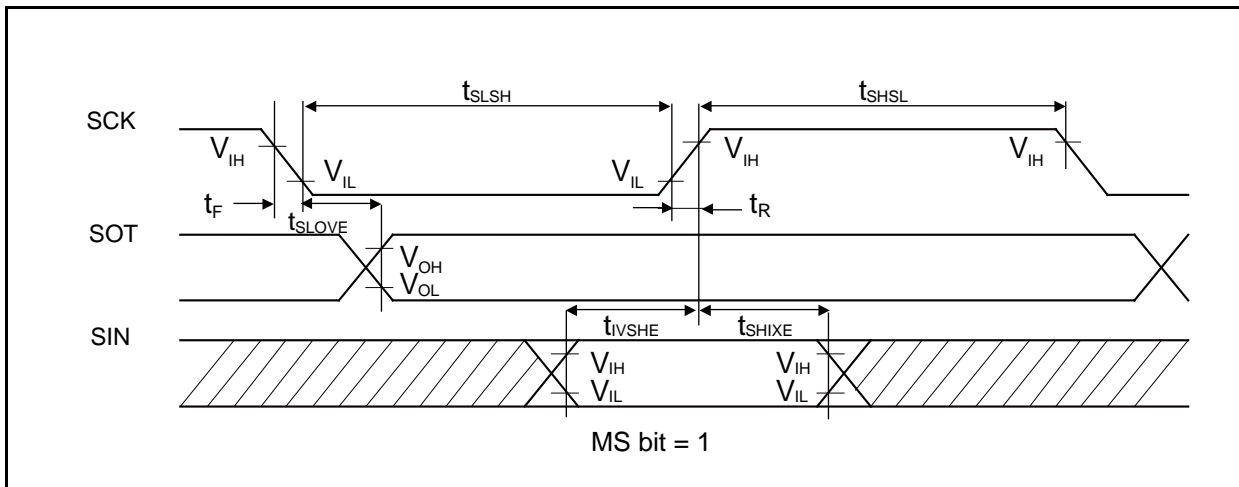
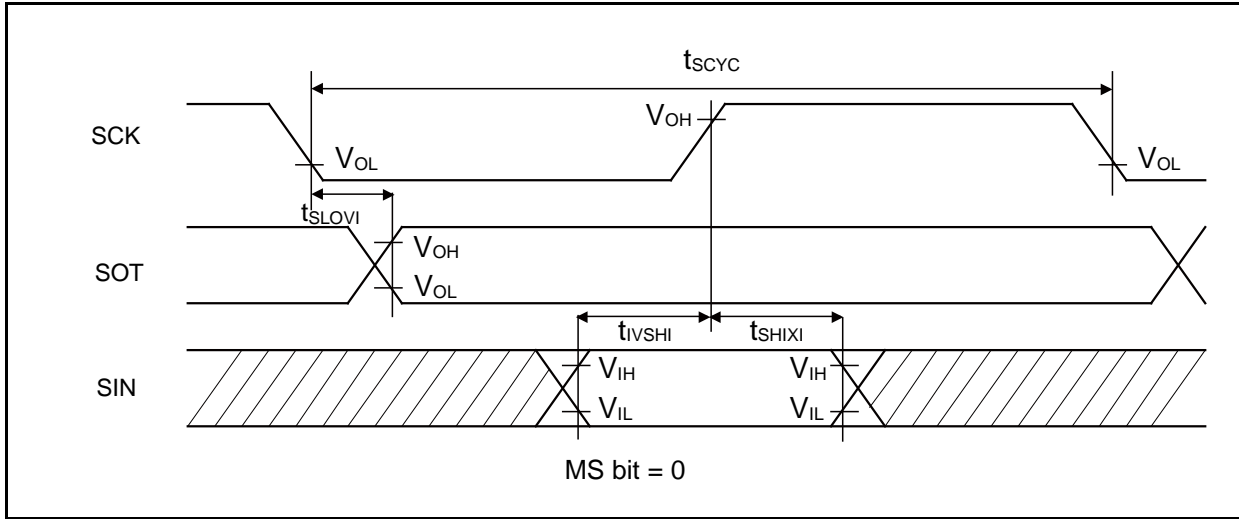
(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	22.5	-	22.5	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↓→SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t <sub>IVSHI</sub>	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↑→SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx	External shift clock operation	2t <sub>CYCP</sub> - 5	-	2t <sub>CYCP</sub> - 5	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK↓→SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t <sub>IVSHE</sub>	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		5	-	5	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

### Notes:

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
  - No chip select: SIN4\_0, SOT4\_0, SCK4\_0
  - Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance C<sub>L</sub> = 30 pF. (For \*, when C<sub>L</sub> = 10 pF)





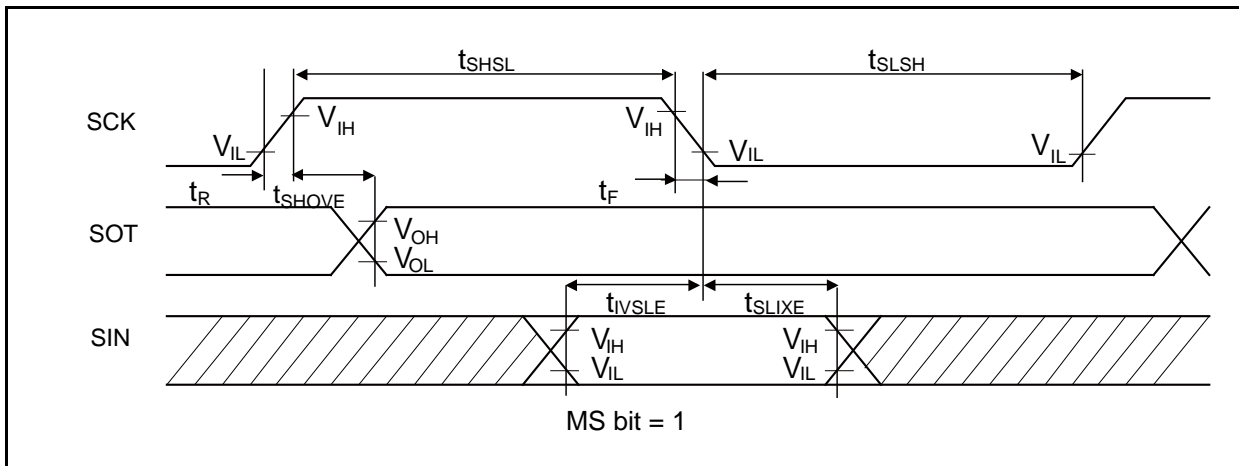
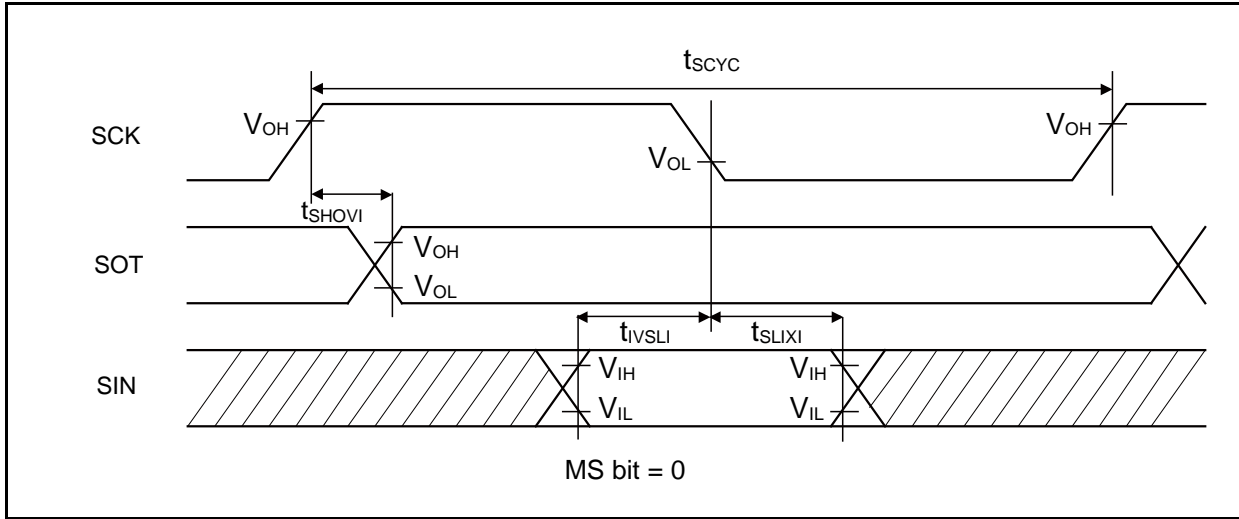
## High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	22.5	-	22.5	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK $\uparrow$ →SOT delay time	$t_{SHOVI}$	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK $\downarrow$ →SIN hold time	$t_{SLIXI}$	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx	External shift clock operation	$2t_{CYCP} - 5$	-	$2t_{CYCP} - 5$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK $\uparrow$ →SOT delay time	$t_{SHOVE}$	SCKx, SOTx		-	15	-	15	ns
SIN→SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKx, SINx		5	-	5	-	ns
SCK $\downarrow$ →SIN hold time	$t_{SLIXE}$	SCKx, SINx		5	-	5	-	ns
SCK fall time	$t_F$	SCKx		-	5	-	5	ns
SCK rise time	$t_R$	SCKx		-	5	-	5	ns

### Notes:

- The above characteristics apply to CLK synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
  - No chip select: SIN4\_0, SOT4\_0, SCK4\_0
  - Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance  $C_L = 30$  pF. (For \*, when  $C_L = 10$  pF)



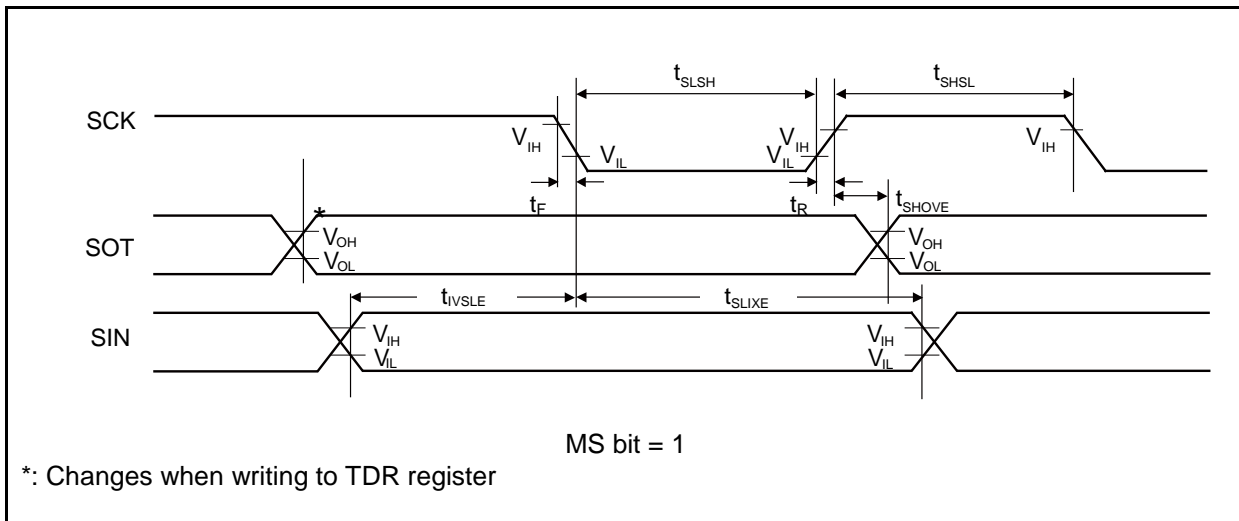
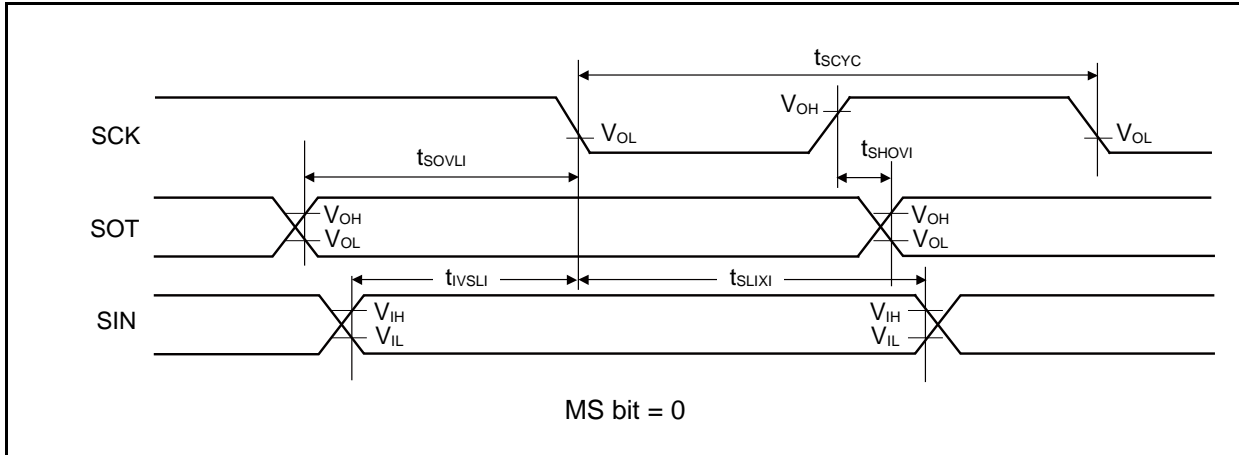
## High-Speed Synchronous Serial (SPI = 1, SCINV = 0)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	22.5	-	22.5	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK $\uparrow$ →SOT delay time	$t_{SHOVI}$	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK $\downarrow$ →SIN hold time	$t_{SLIXI}$	SCKx, SINx		5	-	5	-	ns
SOT→SCK $\downarrow$ delay time	$t_{SOVLI}$	SCKx, SOTx		$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock L pulse width	$t_{LSLH}$	SCKx	External shift clock operation	$2t_{CYCP} - 5$	-	$2t_{CYCP} - 5$	-	ns
Serial clock H pulse width	$t_{HSHL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK $\uparrow$ →SOT delay time	$t_{SHOVE}$	SCKx, SOTx		-	15	-	15	ns
SIN→SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKx, SINx		5	-	5	-	ns
SCK $\downarrow$ →SIN hold time	$t_{SLIXE}$	SCKx, SINx		5	-	5	-	ns
SCK fall time	$t_F$	SCKx		-	5	-	5	ns
SCK rise time	$t_R$	SCKx		-	5	-	5	ns

### Notes:

- The above characteristics apply to CLK synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
  - No chip select: SIN4\_0, SOT4\_0, SCK4\_0
  - Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance  $C_L = 30$  pF. (for \*, when  $C_L = 10$  pF)



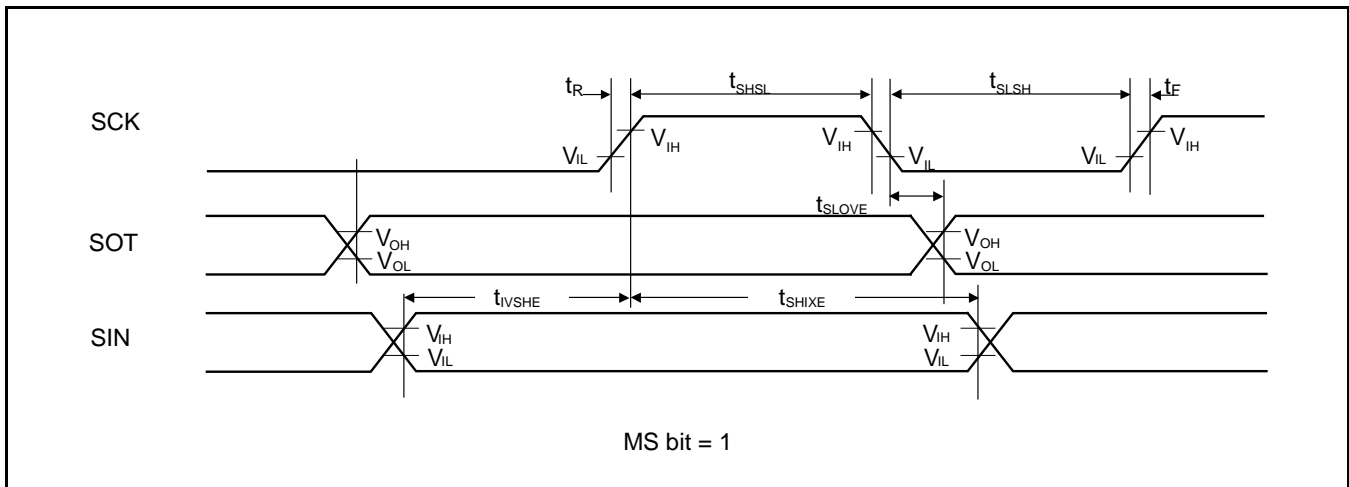
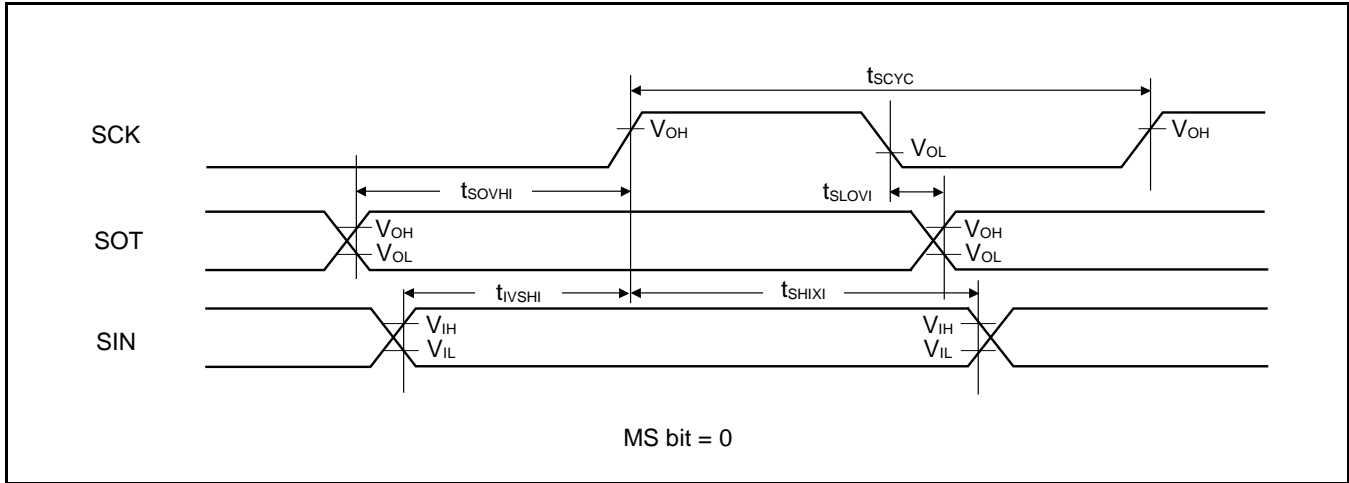
## High-Speed Synchronous Serial (SPI = 1, SCINV = 1)

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	22.5	-	22.5	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↓→SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t <sub>IVSHI</sub>	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↑→SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		5	-	5	-	ns
SOT→SCK↑ delay time	t <sub>SOVHI</sub>	SCKx, SOTx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx		2t <sub>CYCP</sub> - 5	-	2t <sub>CYCP</sub> - 5	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns	
SCK↓→SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx	External shift clock operation	-	15	-	15	ns
SIN→SCK↑ setup time	t <sub>IVSHE</sub>	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		5	-	5	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

### Notes:

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
  - No chip select: SIN4\_0, SOT4\_0, SCK4\_0
  - Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance C<sub>L</sub> = 30 pF. (for \*, when C<sub>L</sub> = 10 pF)



**When Using High-Speed Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS = 0, CSLVL = 1)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t <sub>CShI</sub>		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	ns
SCS↓→SCK↓ setup time	t <sub>CSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCK↑→SCS↑ hold time	t <sub>CSHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>		3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCS↓→SOT delay time	t <sub>DSE</sub>		-	25	-	25	ns
SCS↑→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

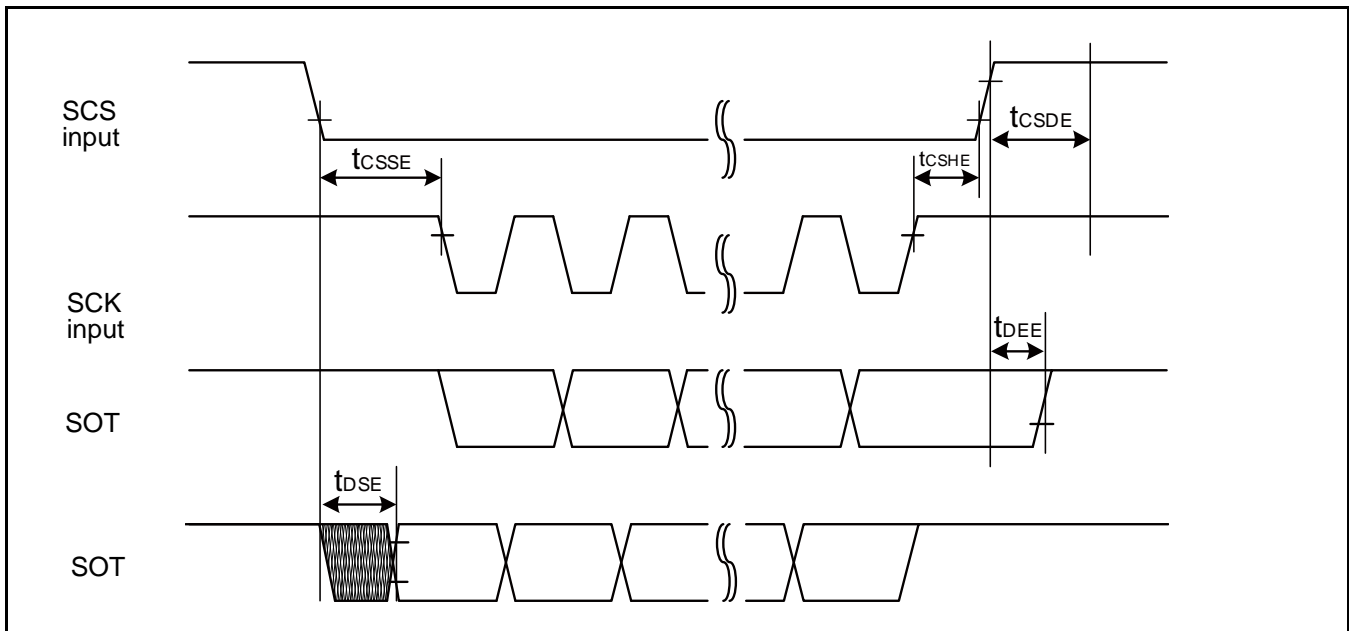
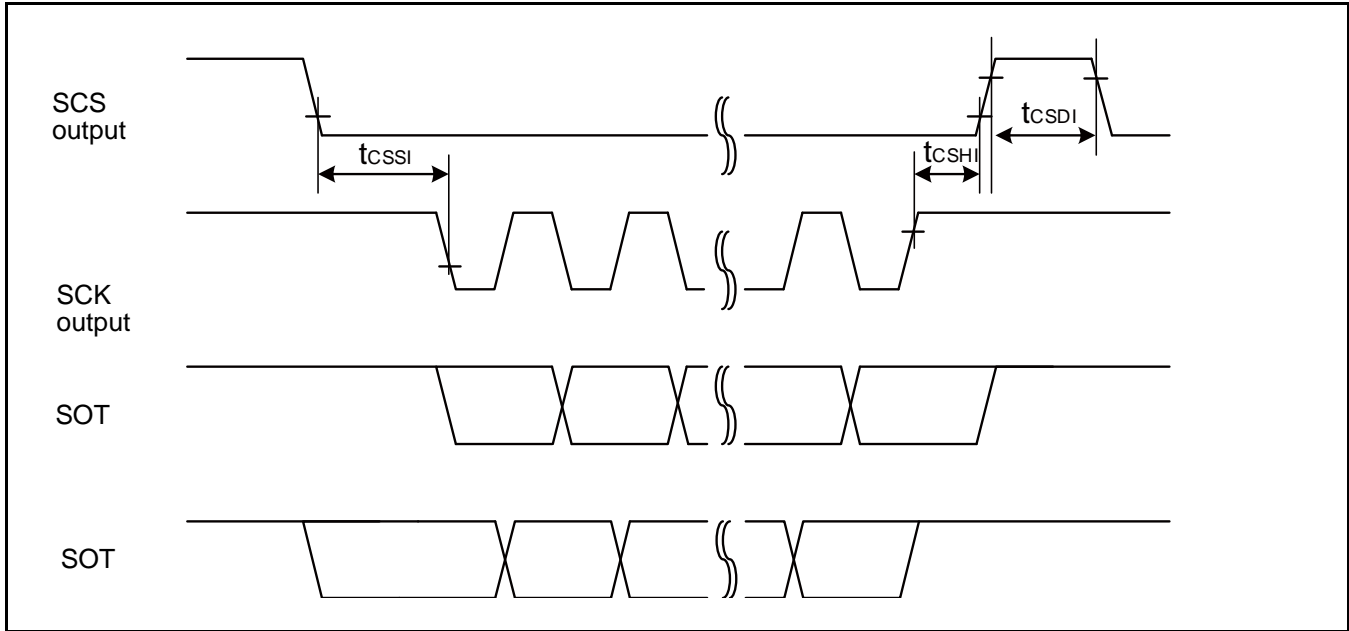
(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.





## When Using High-Speed Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS = 0, CSLVL = 1)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
			Min	Min	Min	Max	
SCS $\downarrow$ →SCK $\downarrow$ setup time	$t_{CSSI}$	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK $\uparrow$ →SCS $\uparrow$ hold time	$t_{CSHI}$		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	$t_{CSDI}$		(*3)-20 +5 $t_{CYCP}$	(*3)+20 +5 $t_{CYCP}$	(*3)-20 +5 $t_{CYCP}$	(*3)+20 +5 $t_{CYCP}$	ns
SCS $\downarrow$ →SCK $\uparrow$ setup time	$t_{CSSE}$	External shift clock operation	3 $t_{CYCP}$ +15	-	3 $t_{CYCP}$ +15	-	ns
SCK $\uparrow$ →SCS $\uparrow$ hold time	$t_{CSHE}$		0	-	0	-	ns
SCS deselect time	$t_{CSDE}$		3 $t_{CYCP}$ +15	-	3 $t_{CYCP}$ +15	-	ns
SCS $\downarrow$ →SOT delay time	$t_{DSE}$		-	25	-	25	ns
SCS $\uparrow$ →SOT delay time	$t_{DEE}$		0	-	0	-	ns

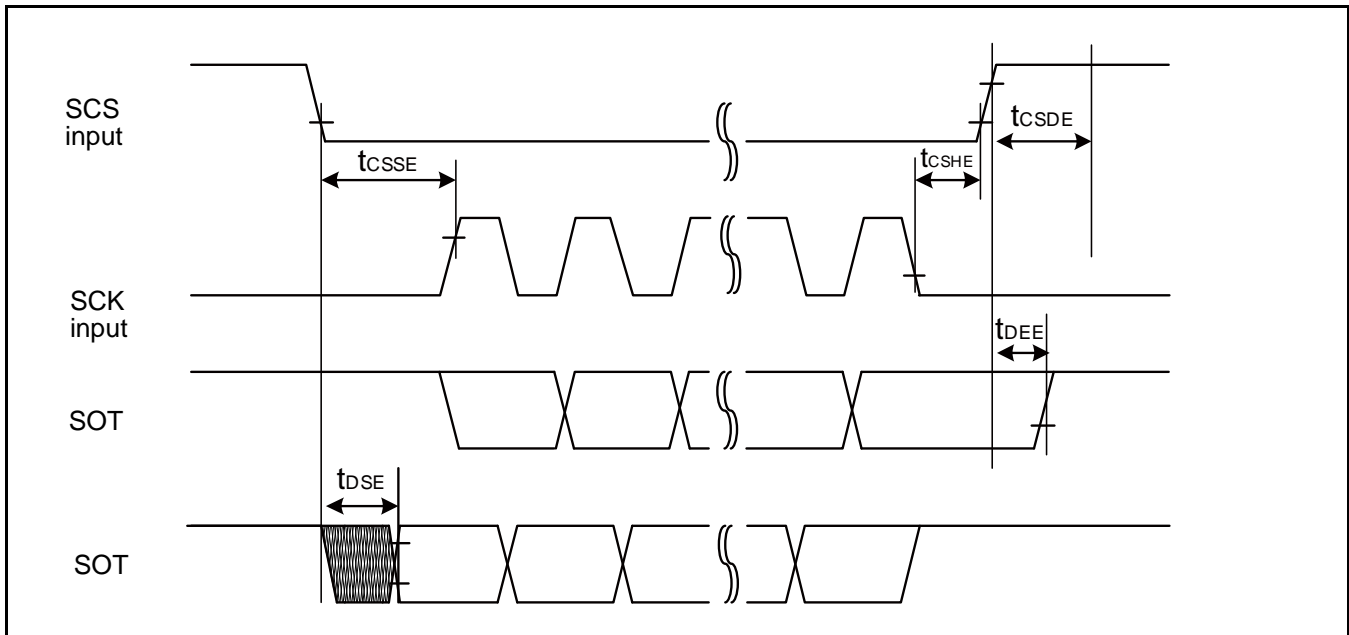
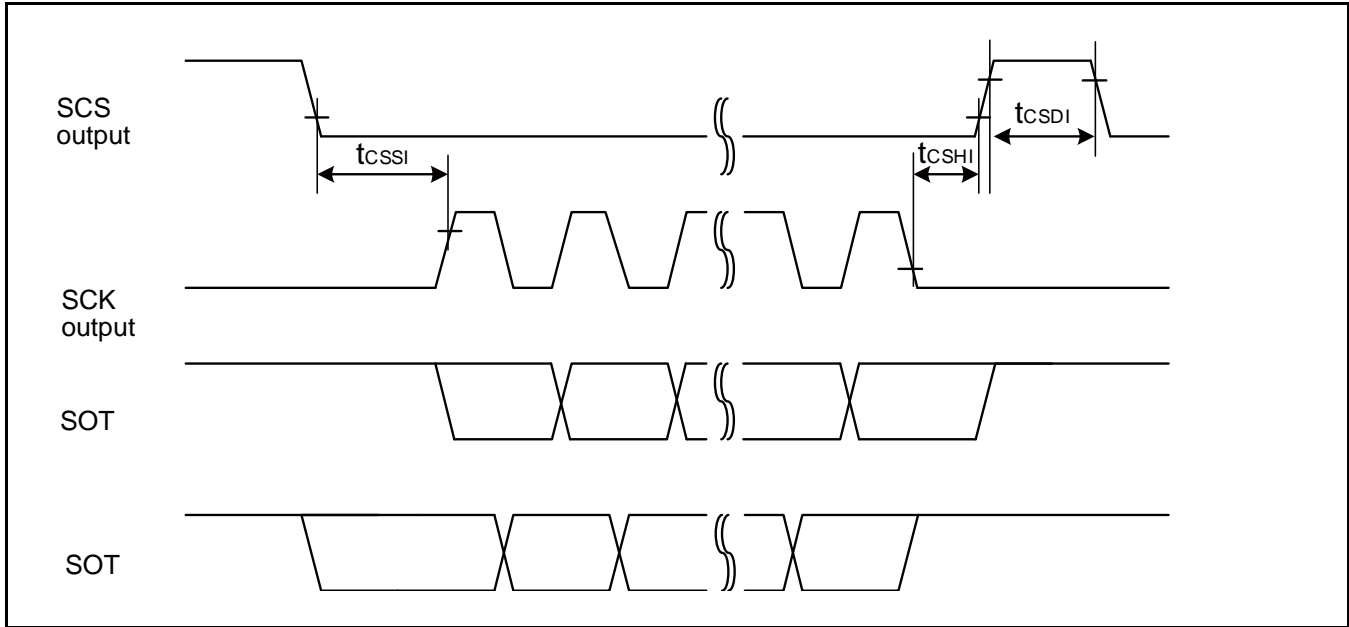
(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

### Notes:

- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance  $C_L = 30 pF$ .



**When Using High-Speed Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS = 0, CSLVL = 0)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t <sub>CSHI</sub>		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	ns
SCS↑→SCK↓ setup time	t <sub>CSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCK↑→SCS↓ hold time	t <sub>CSHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>		3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCS↑→SOT delay time	t <sub>DSE</sub>		-	25	-	25	ns
SCS↓→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

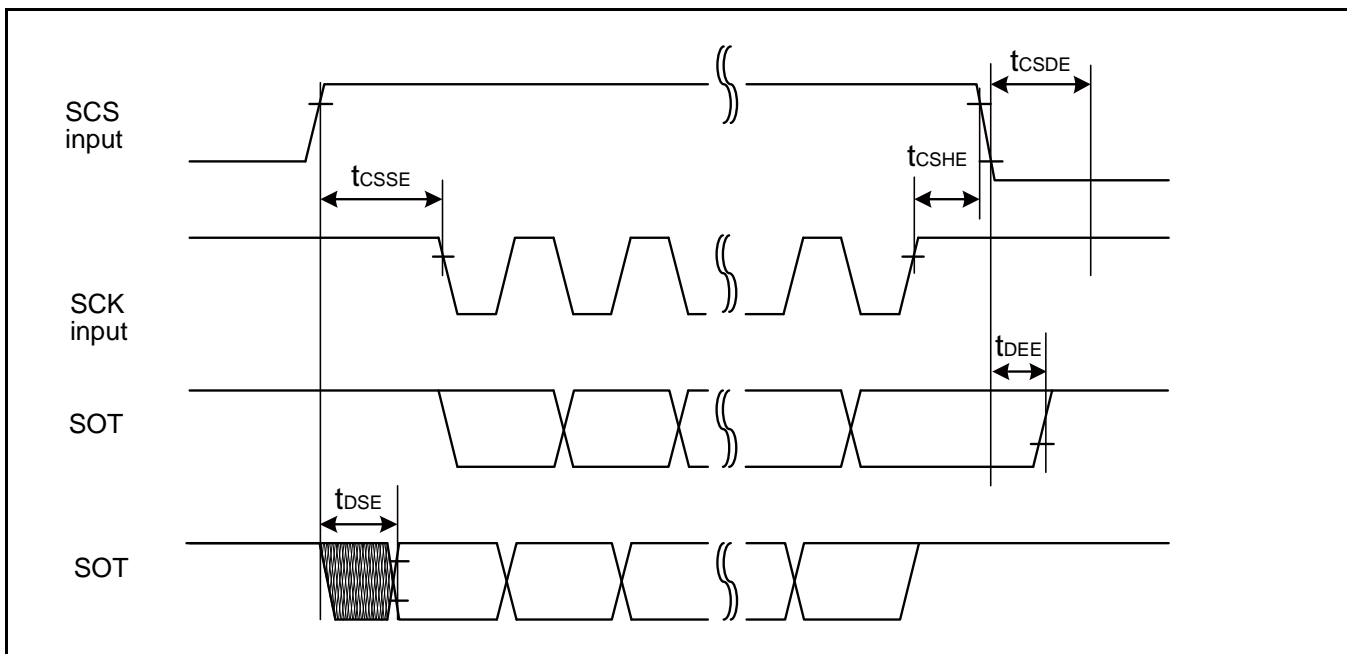
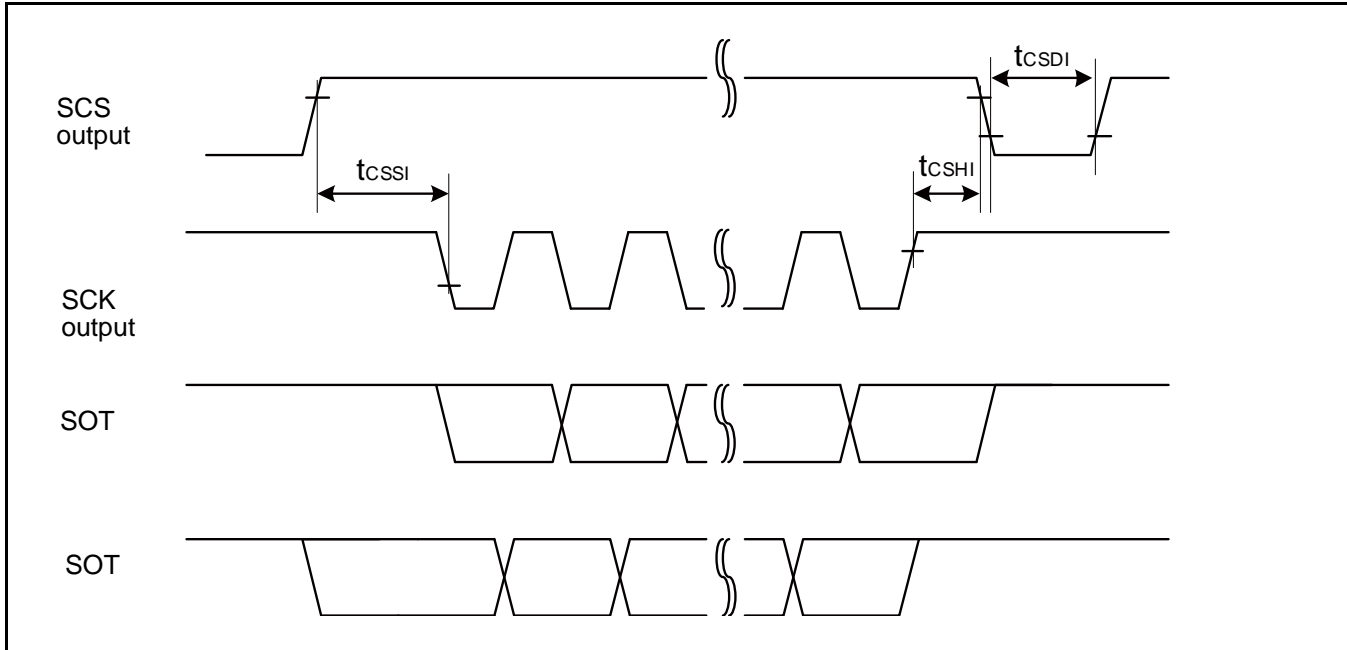
(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



**When Using High-Speed Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS = 0, CSLVL = 0)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t <sub>CSDI</sub>		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	ns
SCS↑→SCK↑ setup time	t <sub>CSSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCK↓→SCS↓ hold time	t <sub>CSDHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDDE</sub>		3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCS↑→SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS↓→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

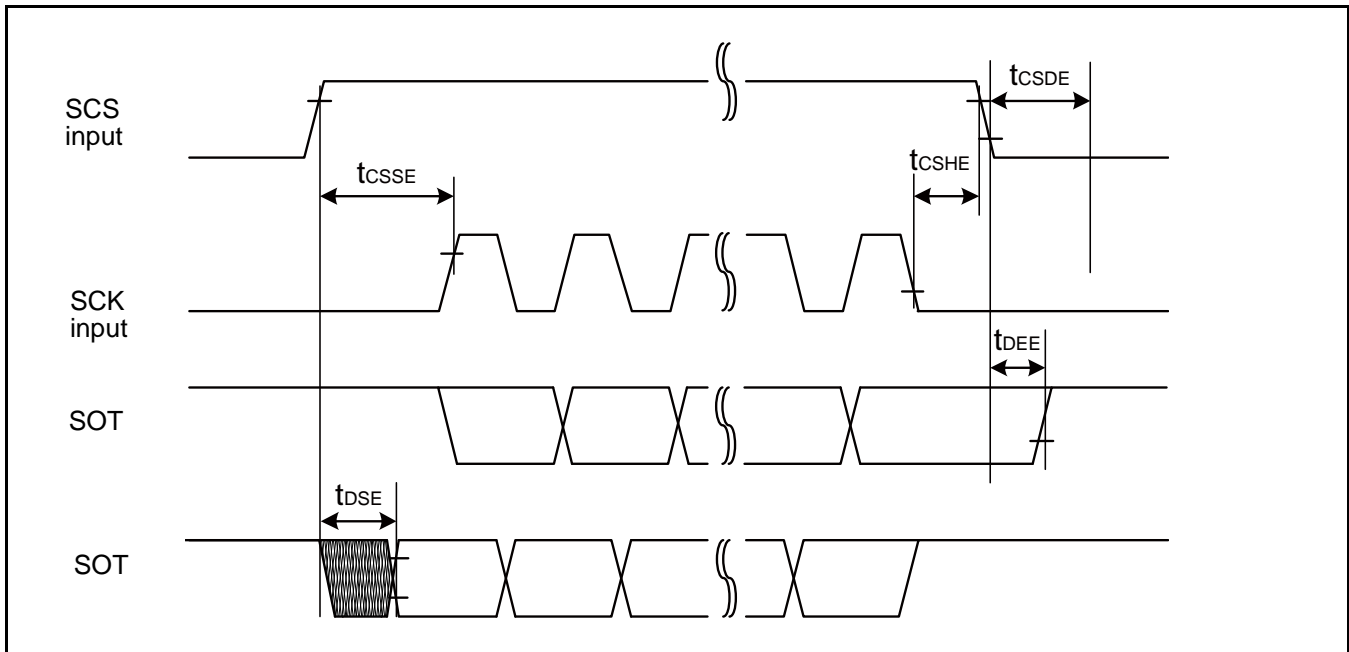
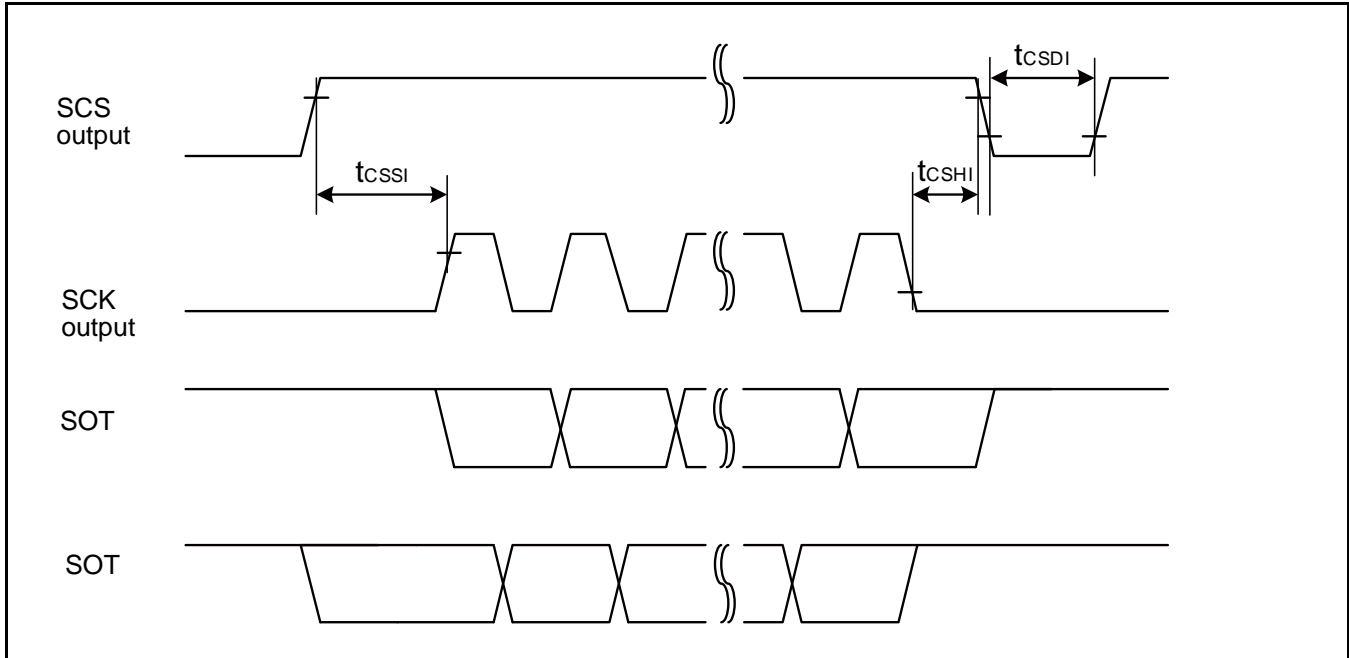
(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

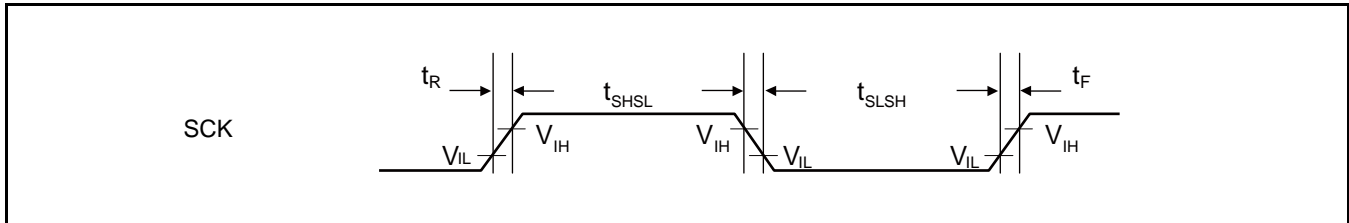
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



**External Clock (EXT = 1): When in Asynchronous Mode Only**

 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	$t_{SLSH}$	$C_L = 30\text{ pF}$	$t_{CYCP} + 10$	-	ns	
Serial clock H pulse width	$t_{SHSL}$		$t_{CYCP} + 10$	-	ns	
SCK fall time	$t_F$		-	5	ns	
SCK rise time	$t_R$		-	5	ns	





**12.4.13 External Input Timing**

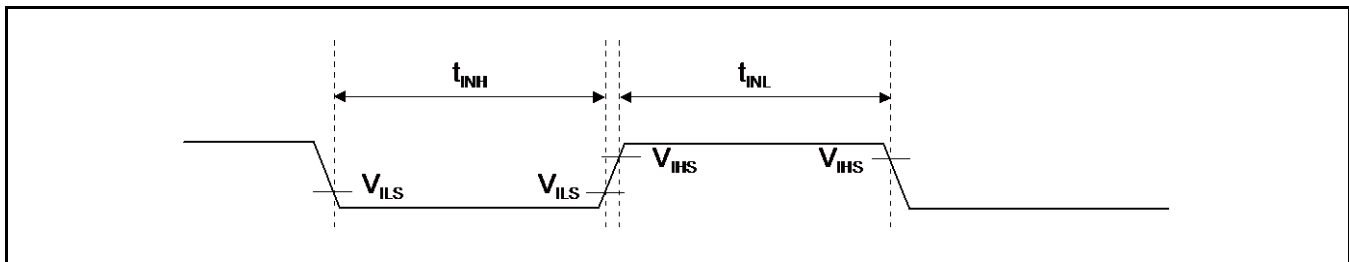
 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{INH}$ , $t_{INL}$	ADTGx	-	$2t_{CYCP}^{*1}$	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTlxX	-	$2t_{CYCP}^{*1}$	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP} + 100^{*1}$	-	ns	External interrupt, NMI
				$500^{*2}$	-	ns	
WKUPx	-	$500^{*3}$	-	ns	Deep standby wake up		

1:  $t_{CYCP}$  indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 1. S6E2G Series Block Diagram in this data sheet.

2: When in Stop mode, in Timer mode

3: When in Deep Standby RTC mode, in Deep Standby Stop mode

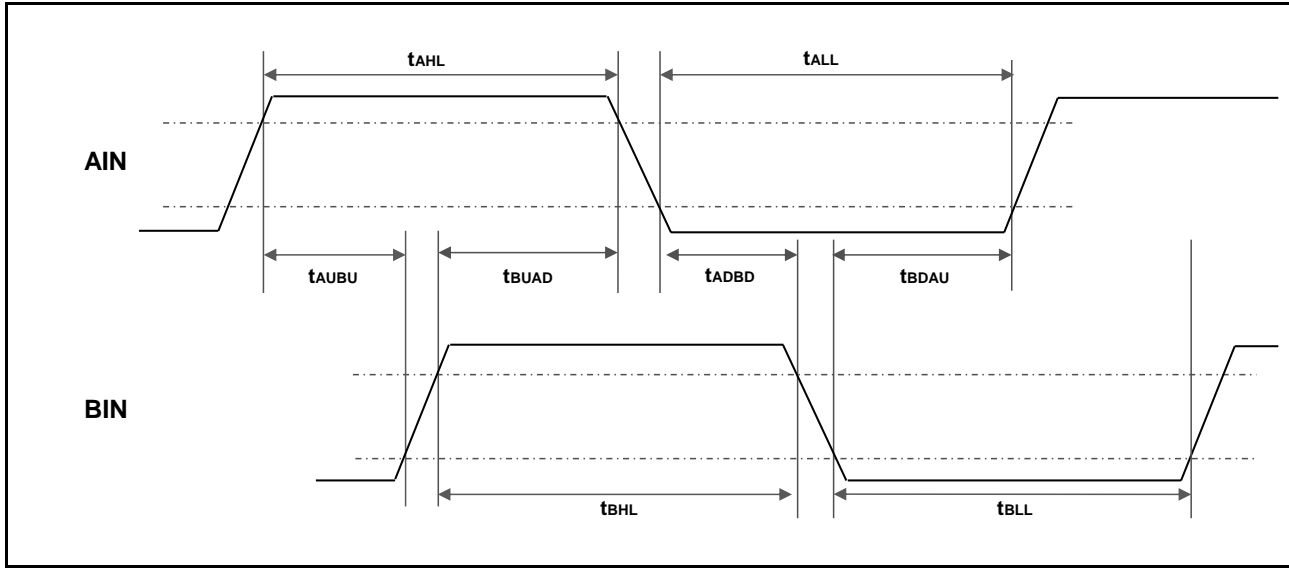


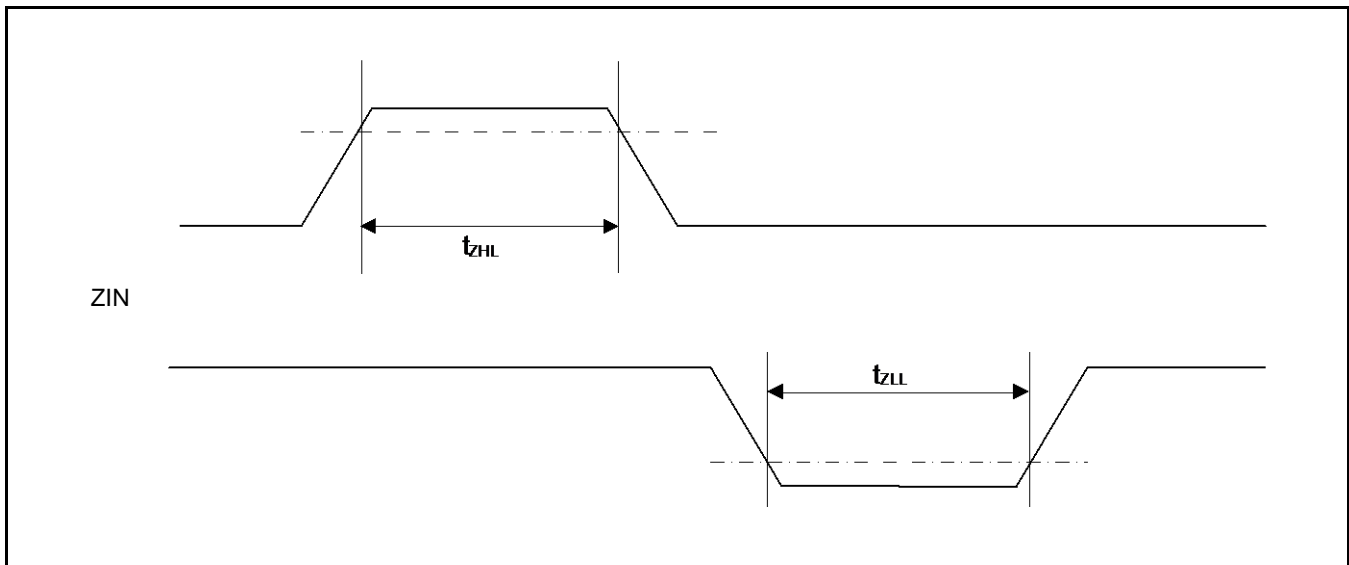
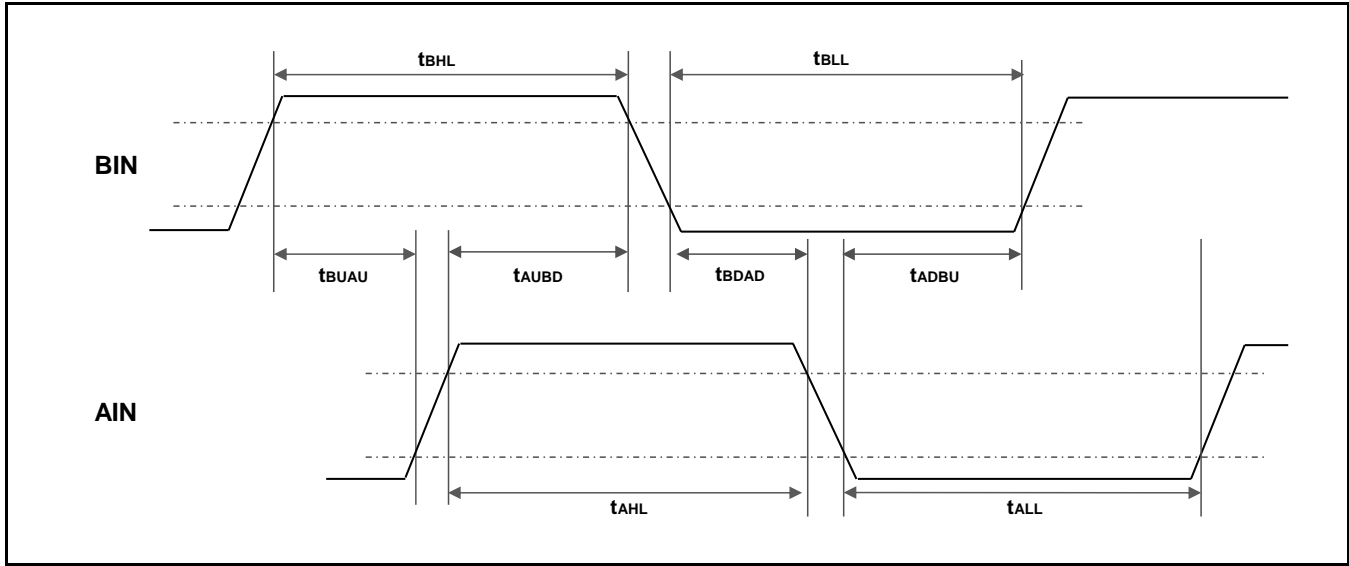
**12.4.14 Quadrature Position/Revolution Counter Timing**

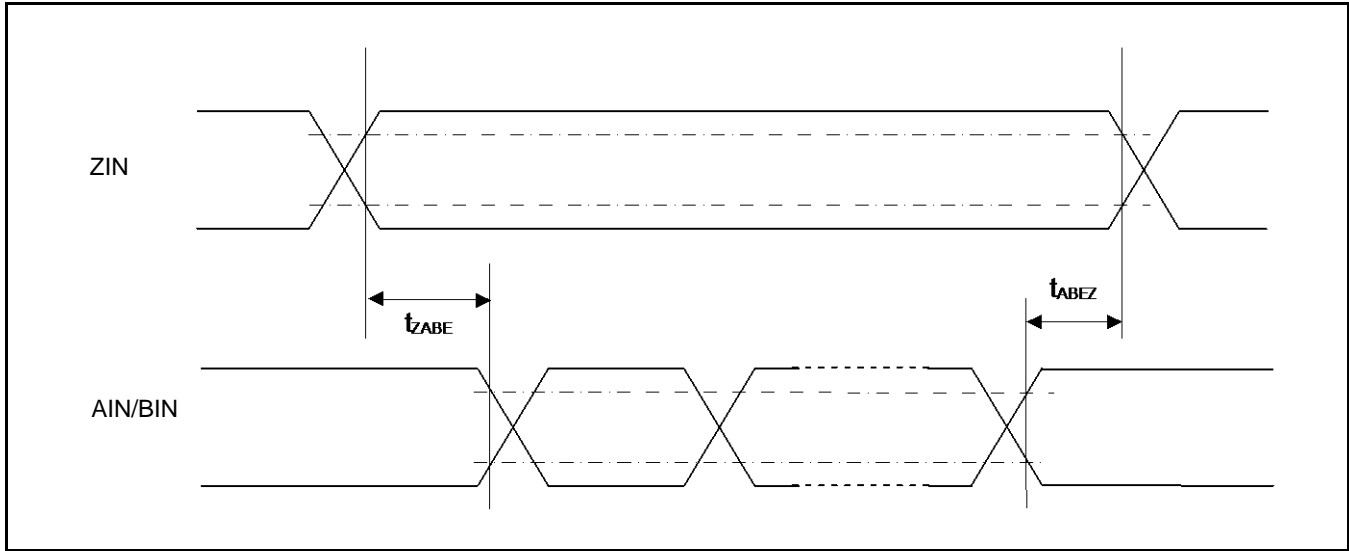
 (V<sub>CC</sub> = AV<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t <sub>AHL</sub>	-	2t <sub>CYCP</sub> *	-	ns
AIN pin L width	t <sub>ALL</sub>	-			
BIN pin H width	t <sub>BHL</sub>	-			
BIN pin L width	t <sub>BLL</sub>	-			
BIN rise time from AIN pin H level	t <sub>AUBU</sub>	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin H level	t <sub>BUAD</sub>	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin L level	t <sub>ADBD</sub>	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin L level	t <sub>BDAU</sub>	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin H level	t <sub>BUAU</sub>	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin H level	t <sub>AUBD</sub>	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin L level	t <sub>BDAD</sub>	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin L level	t <sub>ADBU</sub>	PC_Mode2 or PC_Mode3			
ZIN pin H width	t <sub>ZHL</sub>	QCR: CGSC = 0			
ZIN pin L width	t <sub>ZLL</sub>	QCR: CGSC = 0			
AIN/BIN rise and fall time from determined ZIN level	t <sub>ZABE</sub>	QCR: CGSC = 1			
Determined ZIN level from AIN/BIN rise and fall time	t <sub>ABEZ</sub>	QCR: CGSC = 1			

\*: t<sub>CYCP</sub> indicates the APB bus clock cycle time except when in Stop mode, in Timer mode. For more information about the APB bus number to which the quadrature position/revolution counter is connected, see 1. S6E2G Series Block Diagram in this data sheet.







## 12.4.15 I<sup>2</sup>C Timing

### Standard-Mode, Fast-Mode

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f <sub>SCL</sub>	C <sub>L</sub> = 30 pF <sub>1</sub> R = (V <sub>p</sub> /I <sub>OL</sub> ) <sup>1</sup>	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>		4.0	-	0.6	-	μs	
SCL clock L width	t <sub>LOW</sub>		4.7	-	1.3	-	μs	
SCL clock H width	t <sub>HIGH</sub>		4.0	-	0.6	-	μs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45 <sup>*2</sup>	0	0.9 <sup>*3</sup>	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	-	0.6	-	μs	
Bus free time between Stop condition and START condition	t <sub>BUF</sub>		4.7	-	1.3	-	μs	
Noise filter	t <sub>SP</sub>	2 MHz ≤ t <sub>CYCP</sub> < 40 MHz	2 t <sub>CYCP</sub> <sup>*4</sup>	-	2 t <sub>CYCP</sub> <sup>*4</sup>	-	ns	*5
		40 MHz ≤ t <sub>CYCP</sub> < 60 MHz	4 t <sub>CYCP</sub> <sup>*4</sup>	-	4 t <sub>CYCP</sub> <sup>*4</sup>	-	ns	
		60 MHz ≤ t <sub>CYCP</sub> < 80 MHz	6 t <sub>CYCP</sub> <sup>*4</sup>	-	6 t <sub>CYCP</sub> <sup>*4</sup>	-	ns	
		80 MHz ≤ t <sub>CYCP</sub> ≤ 100 MHz	8 t <sub>CYCP</sub> <sup>*4</sup>	-	8 t <sub>CYCP</sub> <sup>*4</sup>	-	ns	

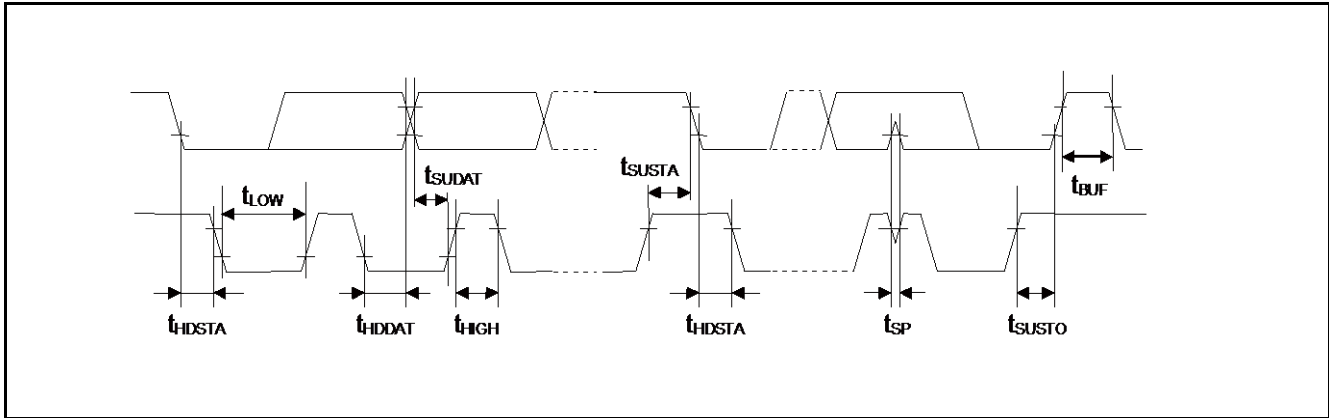
- 1: R and C<sub>L</sub> represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V<sub>p</sub> indicates the power supply voltage of the pull-up resistance and I<sub>OL</sub> indicates V<sub>OL</sub> guaranteed current.
- 2: The maximum t<sub>HDDAT</sub> must not extend beyond the low period (t<sub>LOW</sub>) of the device's SCL signal.
- 3: Fast-mode I<sup>2</sup>C bus device can be used on a Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of "t<sub>SUDAT</sub> ≥ 250 ns.
- 4: t<sub>CYCP</sub> is the APB bus clock cycle time. For more information about the APB bus number to which the I<sup>2</sup>C is connected, see 1.S6E2G Series Block Diagram in this data sheet.  
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.  
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.
- 5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

## Fast mode Plus (Fm+)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Conditions	Fast mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	$f_{SCL}$	$C_L = 30\text{ pF}$ , $R = (V_p/I_{OL})$ <sup>1</sup>	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HDSTA}$		0.26	-	μs	
SCL clock L width	$t_{LOW}$		0.5	-	μs	
SCL clock H width	$t_{HIGH}$		0.26	-	μs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SUSTA}$		0.26	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HDDAT}$		0	0.45 <sup>*2, *3</sup>	μs	
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SUDAT}$		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	$t_{SUSTO}$		0.26	-	μs	
Bus free time between Stop condition and START condition	$t_{BUF}$		0.5	-	μs	
Noise filter	$t_{SP}$	60 MHz ≤ $t_{CYCP} < 80\text{ MHz}$	6 $t_{CYCP}$ <sup>*4</sup>	-	ns	*5
		80 MHz ≤ $t_{CYCP} \leq 100\text{ MHz}$	8 $t_{CYCP}$ <sup>*4</sup>	-	ns	

- 1: R and  $C_L$  represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.  $V_p$  indicates the power supply voltage of the pull-up resistance and  $I_{OL}$  indicates  $V_{OL}$  guaranteed current.
- 2: The maximum  $t_{HDDAT}$  must not extend beyond the low period ( $t_{LOW}$ ) of the device's SCL signal.
- 3: The Fast mode I<sup>2</sup>C bus device can be used on a Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of " $t_{SUDAT} \geq 250\text{ ns}$ ."
- 4:  $t_{CYCP}$  is the APB bus clock cycle time. For more information about the APB bus number to which the I<sup>2</sup>C is connected, see 1.S6E2G Series Block Diagram in this data sheet.  
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.
- 5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.
- 6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I<sup>2</sup>C Fm+ in the EPFR register.  
See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.





**12.4.16 SD Card Interface Timing**

**Default-Speed Mode**

■ Clock CLK (All values are referenced to  $V_{IH}$  and  $V_{IL}$  transition points)

( $V_{CC} = 2.7V$  to  $3.6V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	$f_{PP}$	S_CLK	$C_{CARD} \leq 10$ pF (1card)	0	25	MHz
Clock frequency Identification mode	$f_{OD}$	S_CLK		0/100	400	kHz
Clock low time	$t_{WL}$	S_CLK		10	-	ns
Clock high time	$t_{WH}$	S_CLK		10	-	ns
Clock rise time	$t_{TLH}$	S_CLK		-	10	ns
Clock fall time	$t_{THL}$	S_CLK		-	10	ns

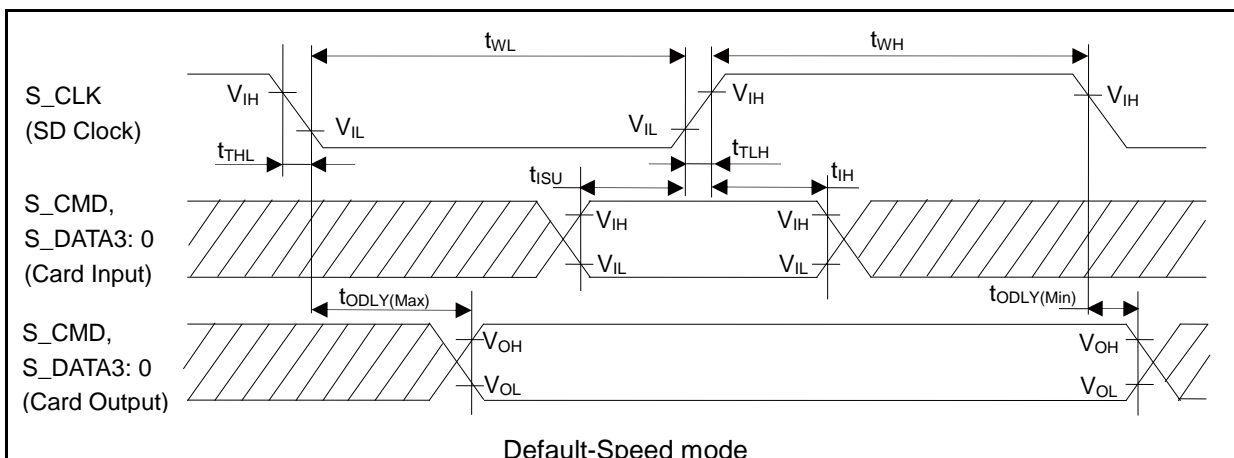
\*: 0 Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	$t_{ISU}$	S_CMD, S_DATA3: 0	$C_{CARD} \leq 10$ pF (1card)	5	-	ns
Input hold time	$t_{IH}$	S_CMD, S_DATA3: 0		5	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer mode	$t_{ODLY}$	S_CMD, S_DATA3: 0	$C_{CARD} \leq 40$ pF (1card)	0	14	ns
Output Delay time during Identification mode	$t_{ODLY}$	S_CMD, S_DATA3: 0		0	50	ns



**Notes:**

- The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.
- For more information about clock frequency ( $f_{PP}$ ), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).

**High-speed Mode**

- Clock CLK (All values are referred to  $V_{IH}$  and  $V_{IL}$ )

( $V_{CC} = 2.7V$  to  $3.6V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	$f_{PP}$	S_CLK	$C_{CARD} \leq 10$ pF (1 card)	0	45	MHz
Clock low time	$t_{WL}$	S_CLK		7	-	ns
Clock high time	$t_{WH}$	S_CLK		7	-	ns
Clock rise time	$t_{TLH}$	S_CLK		-	3	ns
Clock fall time	$t_{THL}$	S_CLK		-	3	ns

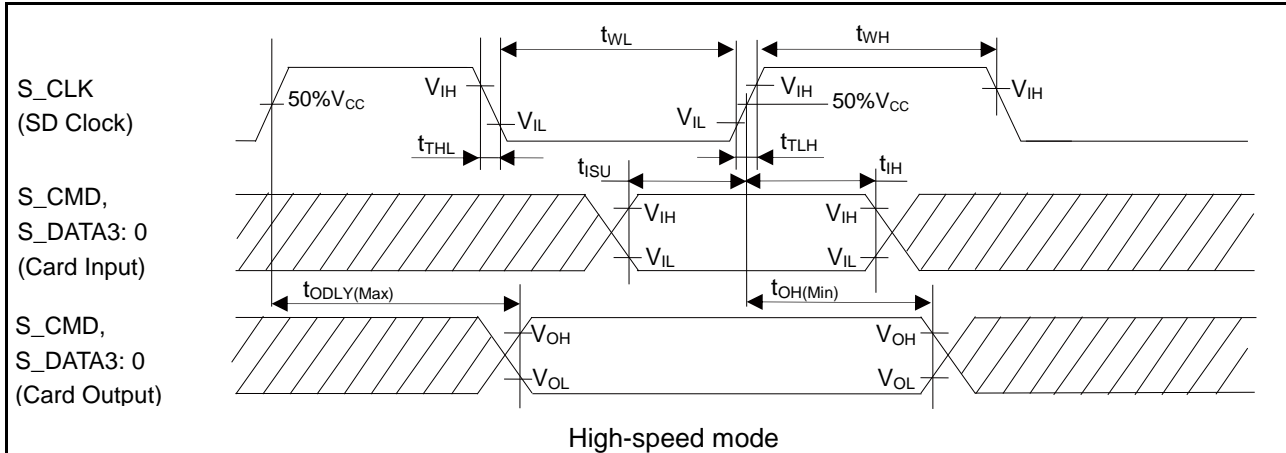
- Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	$t_{ISU}$	S_CMD, S_DATA3: 0	$C_{CARD} \leq 10$ pF (1 card)	6	-	ns
Input hold time	$t_{IH}$	S_CMD, S_DATA3: 0		2	-	ns

- Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	$t_{ODLY}$	S_CMD, S_DATA3: 0	$C_L \leq 40$ pF (1 card)	0	14	ns
Output hold time	$t_{OH}$	S_CMD, S_DATA3: 0	$C_L \geq 15$ pF (1 card)	2.5	-	ns
Total system capacitance for each line*	$C_L$	-	1 card	-	40	pF

\*: In order to satisfy severe timing, host shall drive only one card.


**Notes:**

- The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.
- For more information about clock frequency ( $f_{PP}$ ), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).

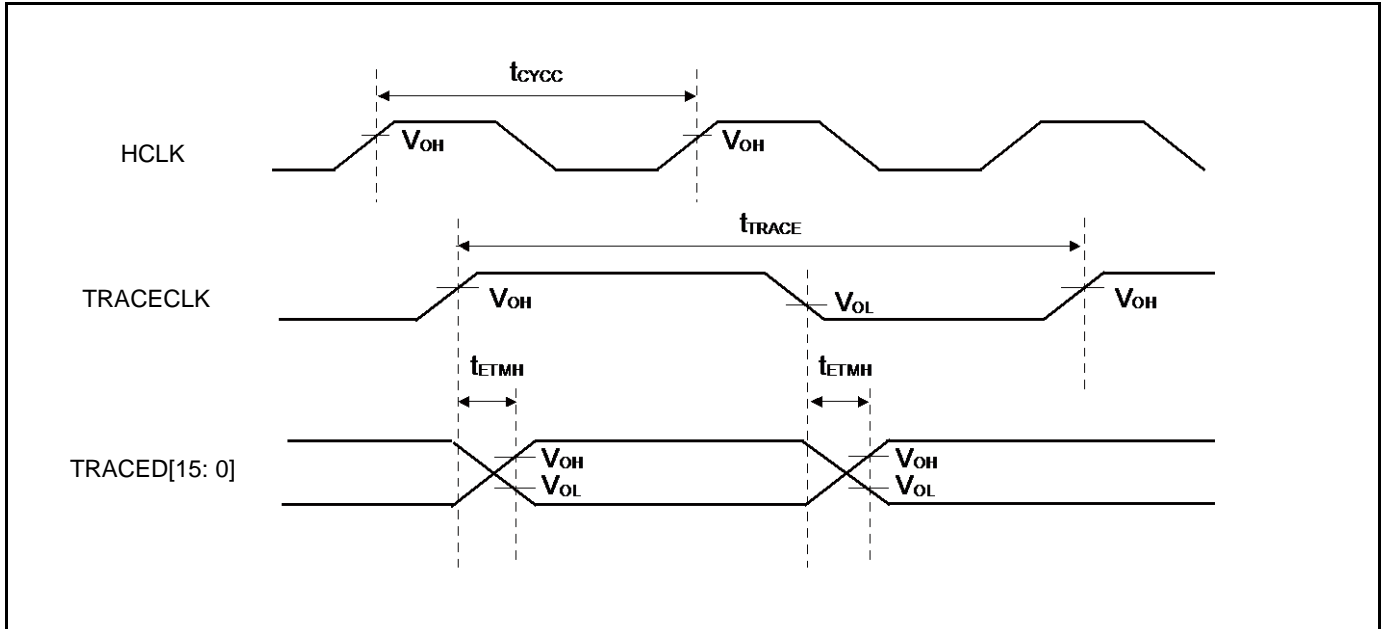
**12.4.17 ETM/HTM Timing**

- ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	$t_{ETMH}$	TRACECLK, TRACED[15: 0]	$V_{CC} \geq 4.5 V$	2	9	ns	
			$V_{CC} < 4.5 V$	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5 V$		50	MHz	
			$V_{CC} < 4.5 V$		32	MHz	
TRACECLK clock cycle	$t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5 V$	20	-	ns	
			$V_{CC} < 4.5 V$	31.25	-	ns	

**Note:**

- When the external load capacitance  $C_L = 30 pF$ .

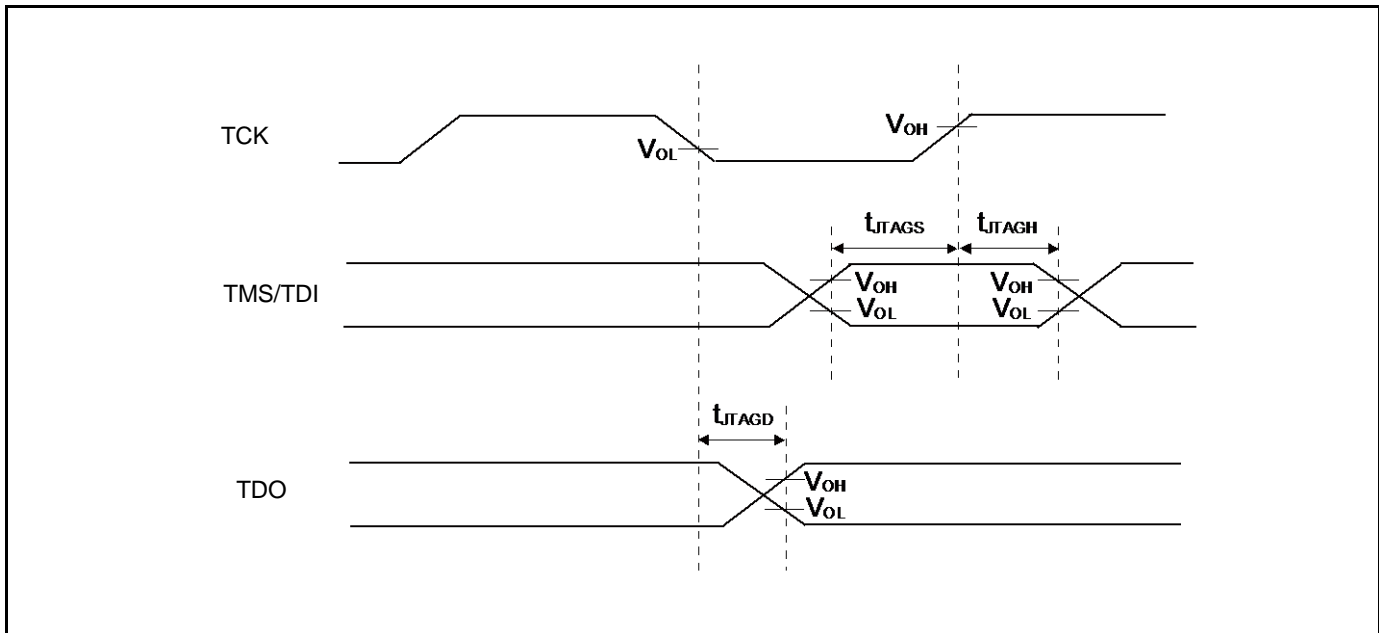


**12.4.18 JTAG Timing**

 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	$t_{JTAGS}$	TCK, TMS, TDI	$V_{CC} \geq 4.5 V$	15	-	ns	
			$V_{CC} < 4.5 V$				
TMS, TDI hold time	$t_{JTAGH}$	TCK, TMS, TDI	$V_{CC} \geq 4.5 V$	15	-	ns	
			$V_{CC} < 4.5 V$				
TDO delay time	$t_{JTAGD}$	TCK, TDO	$V_{CC} \geq 4.5 V$	-	25	ns	
			$V_{CC} < 4.5 V$	-	45		

**Note:**

 - When the external load capacitance  $C_L = 30 pF$ .


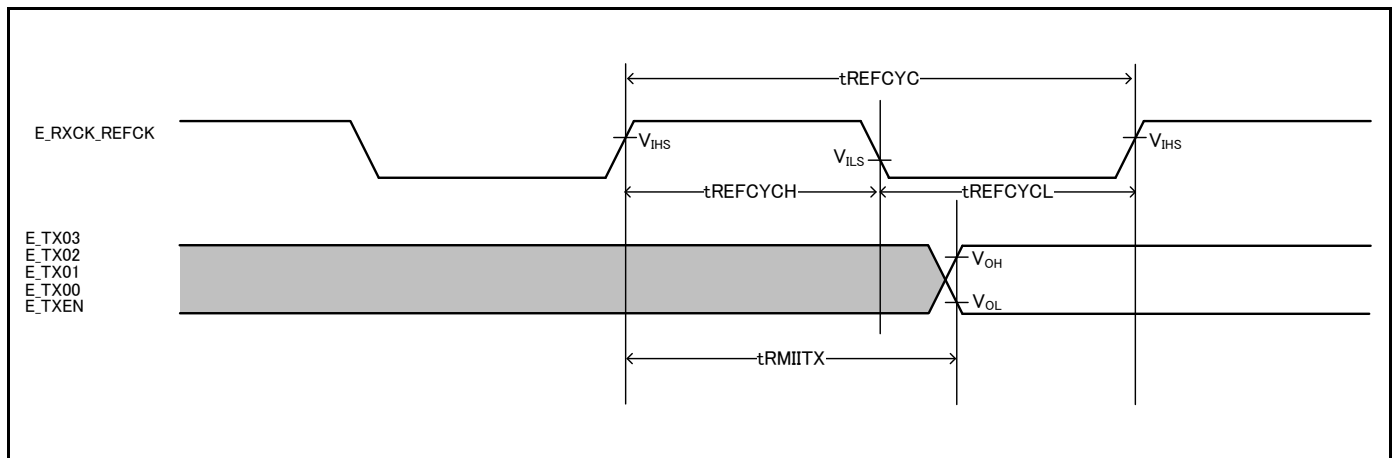
**12.4.19 Ethernet-MAC Timing**

**RMII Transmission (100 Mbps/10 Mbps)**

(ETHV<sub>CC</sub> = 3.0V to 3.6V, 4.5V to 5.5V<sup>\*1</sup>, V<sub>SS</sub> = 0V, C<sub>L</sub> = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time <sup>*2</sup>	t <sub>REFCYC</sub>	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	t <sub>REFCYCH</sub>	E_RXCK_REFCK	t <sub>REFCYCH</sub> /t <sub>REFCYC</sub>	35	65	%
Reference clock Low-pulse-width duty cycle	t <sub>REFCYCL</sub>	E_RXCK_REFCK	t <sub>REFCYCL</sub> /t <sub>REFCYC</sub>	35	65	%
REFCK ↑ → Transmitted data delay time	t <sub>RMIITX</sub>	E_TX03, E_RX02, E_TX01, E_TX00, E_TXEN	-	-	12	ns

- 1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.
- 2: The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.

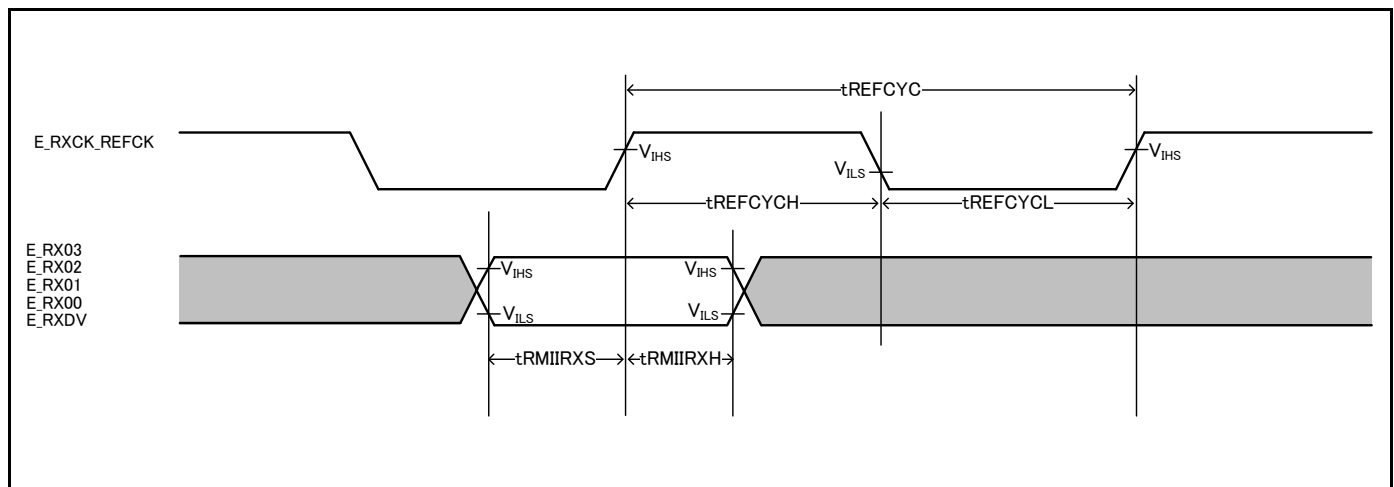


**RMII Receiving (100 Mbps/10 Mbps)**

 (ETHV<sub>CC</sub> = 3.0V to 3.6V, 4.5V to 5.5V, V<sub>SS</sub> = 0V, C<sub>L</sub> = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time*	t <sub>REFCYC</sub>	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	t <sub>REFCYCH</sub>	E_RXCK_REFCK	t <sub>REFCYCH</sub> /t <sub>REFCYC</sub>	35	65	%
Reference clock Low-pulse-width duty cycle	t <sub>REFCYCL</sub>	E_RXCK_REFCK	t <sub>REFCYCL</sub> /t <sub>REFCYC</sub>	35	65	%
Received data → REFCK ↑ Setup time	t <sub>RMIRXS</sub>	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	4	-	ns
REFCK ↑ → Received data Hold time	t <sub>RMIRXH</sub>	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

\*: The reference clock is fixed to 50 MHz in the RMII specifications.  
 The clock accuracy should meet the PHY-device specifications.

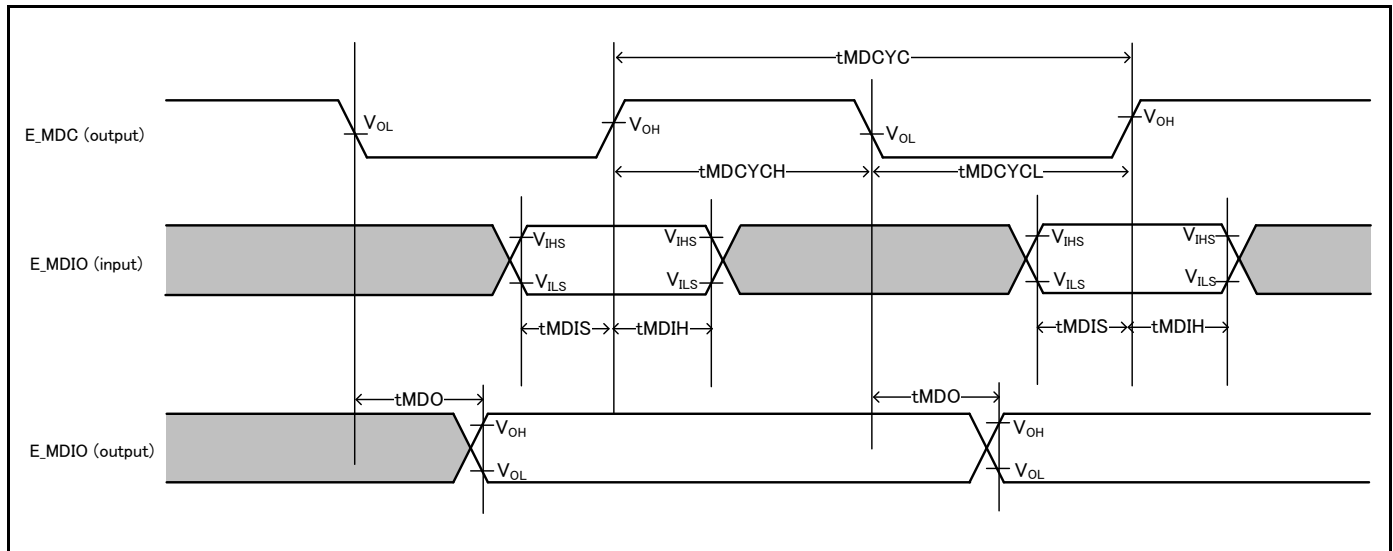


**Management Interface**

 (ETHV<sub>CC</sub> = 3.0V to 3.6V, 4.5V to 5.5V, V<sub>SS</sub> = 0V, C<sub>L</sub> = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Management clock cycle time*	t <sub>MDCYC</sub>	E_MDC	-	400	-	ns
Management clock High pulse width duty cycle	t <sub>MDCYCH</sub>	E_MDC	t <sub>MDCYCH</sub> /t <sub>MDCYC</sub>	35	65	%
Management clock Low pulse width duty cycle	t <sub>MDCYCL</sub>	E_MDC	t <sub>MDCYCL</sub> /t <sub>MDCYC</sub>	35	65	%
MDC ↓ → MDIO Delay time	t <sub>MDO</sub>	E_MDIO	-	-	60	ns
MDIO → MDC ↑ Setup time	t <sub>MDIS</sub>	E_MDIO	-	20	-	ns
MDC ↑ → MDIO Hold time	t <sub>MDIH</sub>	E_MDIO	-	0	-	ns

\*: The clock time should be set to a value greater than the minimum value by setting the Ethernet-MAC setting register.



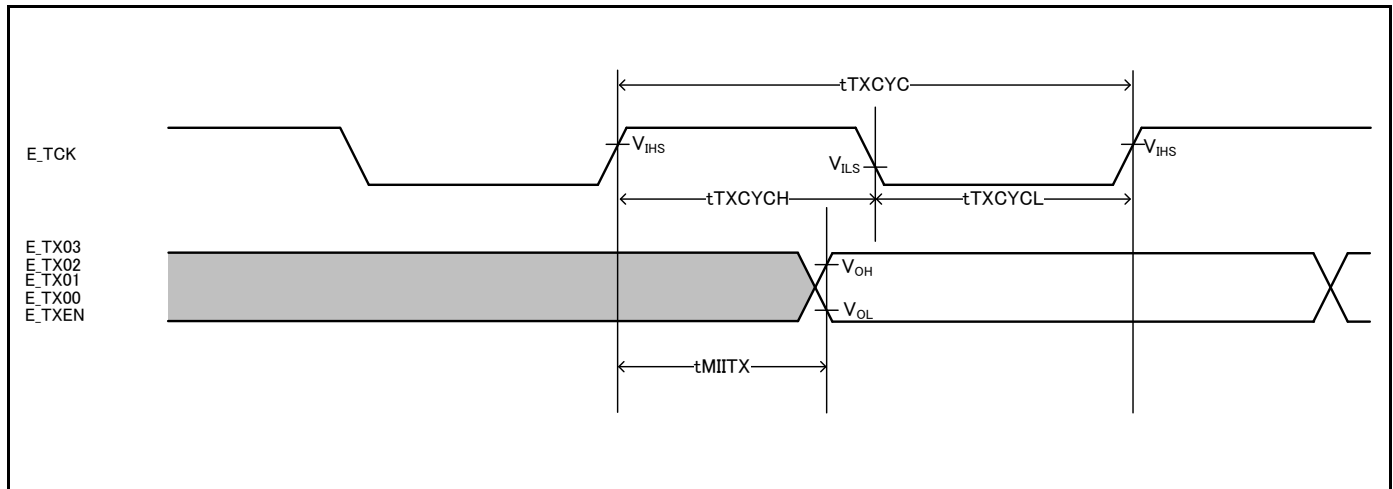


**MII Transmission (100 Mbps/10 Mbps)**

 (ETHV<sub>CC</sub> = 3.0V to 3.6V, 4.5V to 5.5V<sup>\*1</sup>; V<sub>SS</sub> = 0V, C<sub>L</sub> = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Transmission clock Cycle time*2	t <sub>TXCYC</sub>	E_TCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Transmission clock High-pulse-width duty cycle	t <sub>TXCYCH</sub>	E_TCK	t <sub>TXCYCH</sub> /t <sub>TXCYC</sub>	35	65	%
Transmission clock Low-pulse-width duty cycle	t <sub>TXCYCL</sub>	E_TCK	t <sub>TXCYCL</sub> /t <sub>TXCYC</sub>	35	65	%
TXCK ↑ → Transmitted data delay time	t <sub>MIITX</sub>	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	24	ns

- 1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.
- 2: The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications. The clock accuracy should meet the PHY-device specifications.



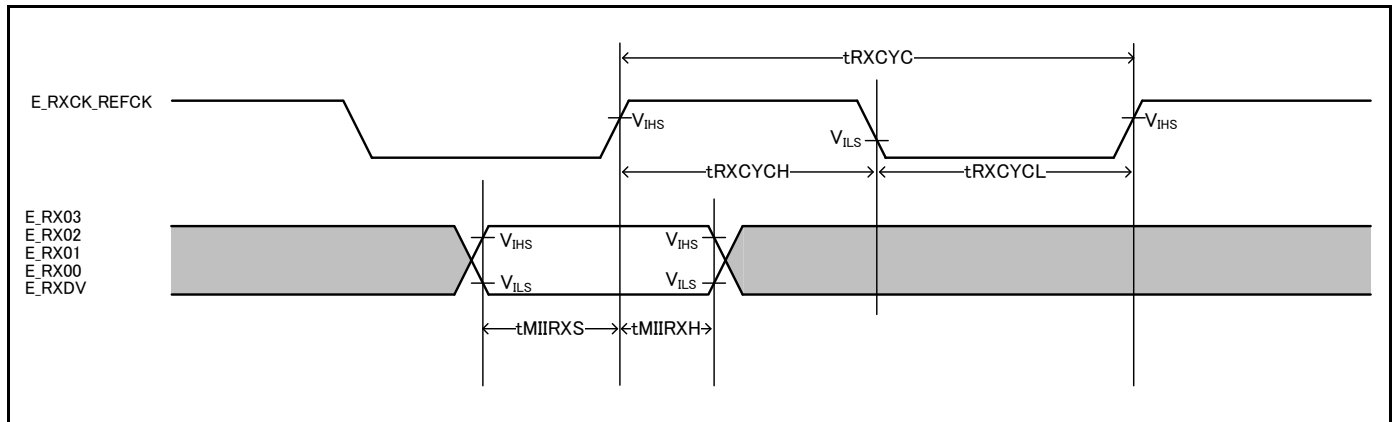
**MII Receiving (100 Mbps/10 Mbps)**

 (ETHV<sub>CC</sub> = 3.0V to 3.6V, 4.5V to 5.5V, V<sub>SS</sub> = 0V, C<sub>L</sub> = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Receiving clock cycle time*	t <sub>RXCYC</sub>	E_RXCK_REFCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Receiving clock High pulse width duty cycle	t <sub>RXCYCH</sub>	E_RXCK_REFCK	t <sub>RXCYCH</sub> /t <sub>RXCYC</sub>	35	65	%
Receiving clock Low pulse width duty cycle	t <sub>RXCYCL</sub>	E_RXCK_REFCK	t <sub>RXCYCL</sub> /t <sub>RXCYC</sub>	35	65	%
Received data → REFCK ↑ Setup time	t <sub>MIIRXS</sub>	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	5	-	ns
REFCK ↑ → Received data Hold time	t <sub>MIIRXH</sub>	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

\*: The receiving clock 100Mbps is fixed to 25MHz or 2.5MHz in the MII specifications.

The clock accuracy should meet the PHY-device specifications.



**12.4.20 I<sup>2</sup>S Timing (Multi-function Serial Interface)**

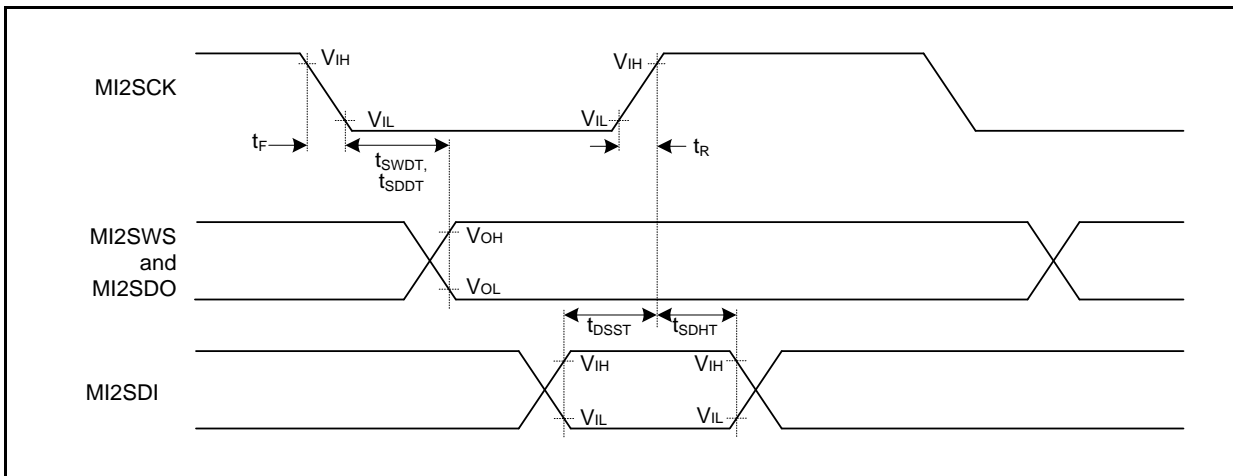
(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
I2SCK max frequency (*1)	f <sub>I2SCK</sub>	MI2SCKx	-	-	6.144	MHz	
I2S clock cycle time (*1)	t <sub>ICYC</sub>	MI2SCKx	-	4 t <sub>CYCP2</sub>	-	%	
I2S clock Duty cycle	Δ	MI2SCKx		45	55	%	
I2SCK ↓ → I2SWS delay time	t <sub>SWDT</sub>	MI2SCKx, MI2SWSx	-	-20	+20	ns	
I2SCK ↓ → I2SDO delay time	t <sub>SDDT</sub>	MI2SCKx, MI2SDOx	-	-20	+20	ns	
I2SDI → I2SCK ↑ setup time	t <sub>DSST</sub>	MI2SCKx, MI2SDIx	-	36	-	ns	
I2SCK ↑ → I2SDI hold time	t <sub>SDHT</sub>		-	0	-	ns	
I2SCK falling time	t <sub>F</sub>	MI2SCKx	-	-	5	ns	
I2SCK rising time	t <sub>R</sub>		-	-	5	ns	

\*1: I2S clock should meet the multiple of PCLK(t<sub>ICYC</sub>) and the frequency less than f<sub>I2SCK</sub> meantime.

**Notes:**

- See Chapter 1-6: I<sup>2</sup>S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04856) for the details.



**12.5 12-bit A/D Converter**
**Electrical Characteristics for the A/D Converter**
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = AV_{RL} = 0V)$ 

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	-	-	$\pm 4.5$	LSB	AVRH = 2.7 V to 5.5 V Offset calibration when used
Differential nonlinearity	-	-	-	-	$\pm 2.5$	LSB	
Zero transition voltage	$V_{ZT}$	ANxx	-	$\pm 2$	$\pm 7$	LSB	
Full-scale transition voltage	$V_{FST}$	ANxx	-	$AVRH \pm 2$	$AVRH \pm 7$	LSB	
Total error	-	-	-	$\pm 3$	$\pm 8$	LSB	
Conversion time	-	-	$0.5^{*1}$	-	-	$\mu s$	$AV_{CC} \geq 4.5 V$
Sampling time *2	$t_s$	-	0.15	-	10	$\mu s$	$AV_{CC} \geq 4.5 V$
			0.3	-			$AV_{CC} < 4.5 V$
Compare clock cycle *3	$t_{CCK}$	-	25	-	1000	ns	$AV_{CC} \geq 4.5 V$
			50	-	1000		$AV_{CC} < 4.5 V$
State transition time to operation permission	$t_{STT}$	-	-	-	1.0	$\mu s$	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22		$\mu A$
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3		$\mu A$
Analog input capacity	$C_{AIN}$	-	-	-	12.05	pF	
Analog input resistance	$R_{AIN}$	-	-	-	1.2	k $\Omega$	$AV_{CC} \geq 4.5 V$
					1.8		$AV_{CC} < 4.5 V$
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	$\mu A$	
Analog input voltage	-	ANxx	$AV_{SS}$	-	AVRH	V	
			$AV_{SS}$	-	$AV_{CC}$		
Reference voltage	-	AVRH	4.5	-	$AV_{CC}$	V	$T_{cck} < 50 \text{ ns}$
			2.7	-	$AV_{CC}$		$T_{cck} \geq 50 \text{ ns}$
	-	AVRL	$AV_{SS}$	-	$AV_{SS}$	V	

1: The conversion time is the value of sampling time ( $t_s$ ) + compare time ( $t_c$ ).

The condition of the minimum conversion time is when the value of  $T_s = 150 \text{ ns}$  and  $T_c = 350 \text{ ns}$  ( $AV_{CC} \geq 4.5V$ ). Ensure that it satisfies the value of sampling time ( $t_s$ ) and compare clock cycle ( $t_{CCK}$ ).

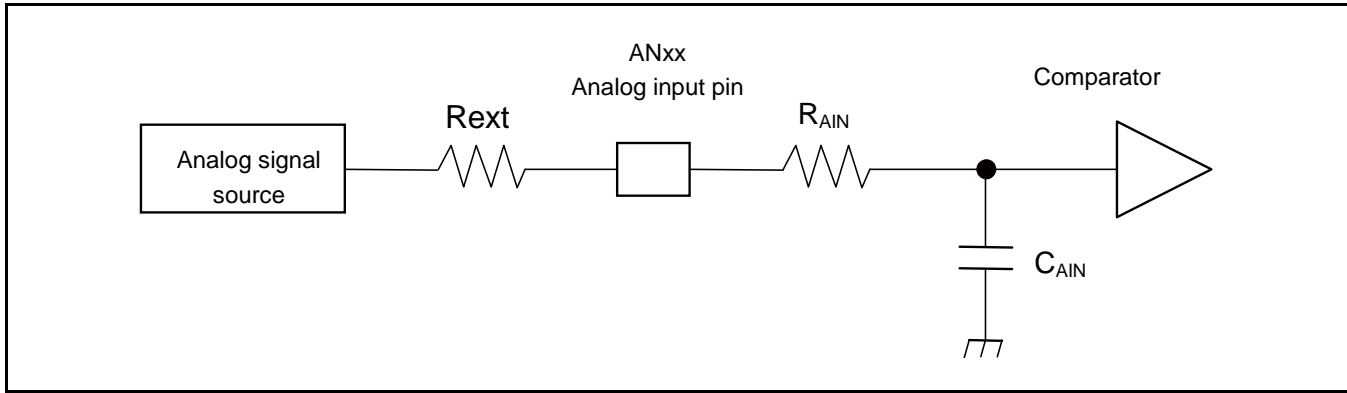
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more

information about the APB bus number to which the A/D converter is connected, see 1. S6E2G Series Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

3: The compare time ( $t_c$ ) is the value of (Equation 2).



$$(Equation 1) t_s \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$$

$t_s$ : Sampling time

$R_{AIN}$ : Input resistance of A/D = 1.2 k $\Omega$  at 4.5 V  $\leq$  AVCC  $\leq$  5.5 V

Input resistance of A/D = 1.8 k $\Omega$  at 2.7 V  $\leq$  AVCC < 4.5 V

$C_{AIN}$ : Input capacity of A/D = 12.05 pF at 2.7 V  $\leq$  AVCC  $\leq$  5.5 V

$R_{ext}$ : Output impedance of external circuit

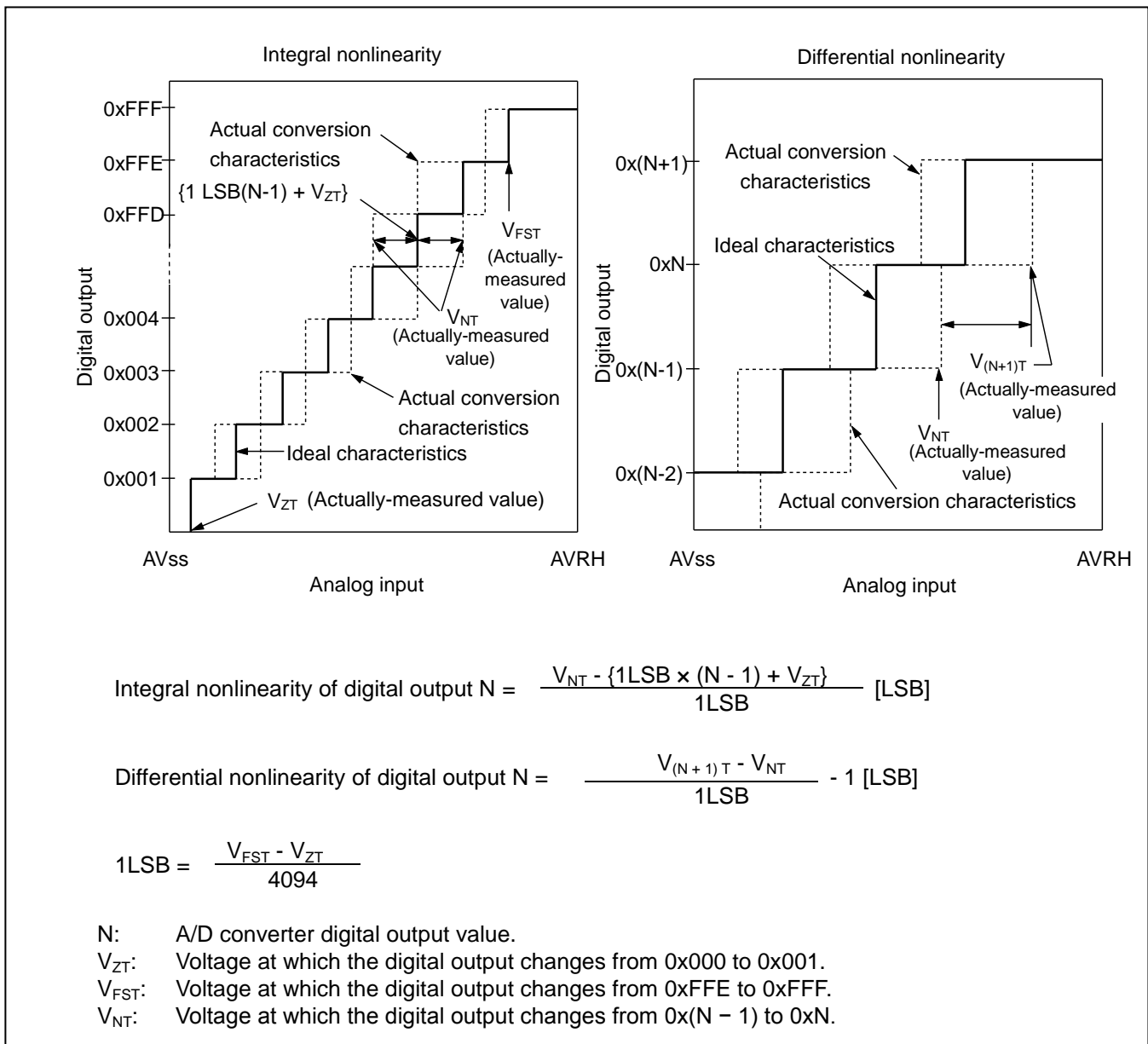
$$(Equation 2) t_c = t_{CCK} \times 14$$

$t_c$ : Compare time

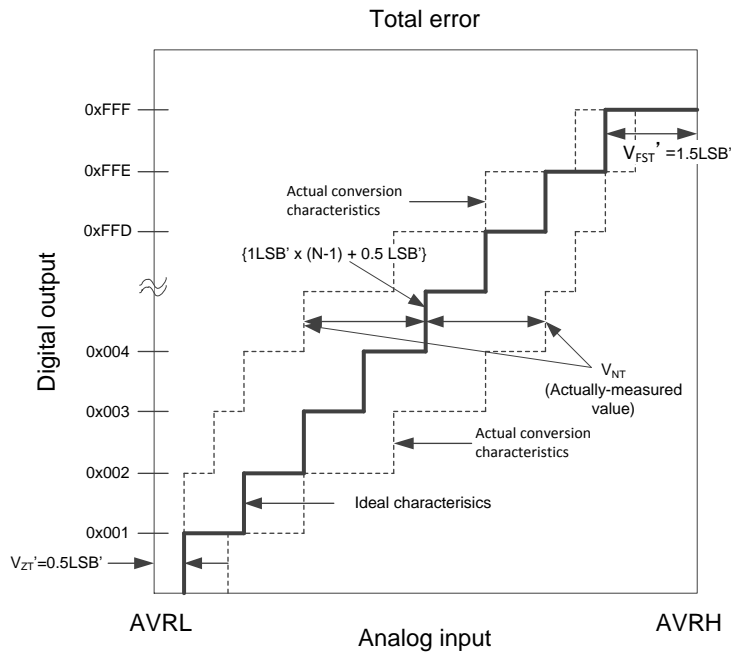
$t_{CCK}$ : Compare clock cycle

**Definition of 12-bit A/D Converter Terms**

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ↔ 0b000000000001) and the full-scale transition point (0b111111111110 ↔ 0b111111111111) from the actual conversion characteristics.
- Differential nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



- Total error:** A difference between actual value and theoretical value.  
 The overall error includes zero-transition voltage, full-scale transition voltage and linearity error.



$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N-1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'} \quad [\text{LSB}]$$

$$1 \text{ LSB}' \text{ (ideal value)} = \frac{AVRH - AVRL}{4096} \quad [\text{V}]$$

$$V_{ZT}' \text{ (ideal value)} = AVRL + 0.5 \text{ LSB}' \quad [\text{V}]$$

$$V_{FST}' \text{ (ideal value)} = AVRH - 1.5 \text{ LSB}' \quad [\text{V}]$$

$V_{NT}'$  : A voltage for causing transition of digital output from (N-1) to N

**12.6 USB Characteristics**

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $USBV_{CC0} = USBV_{CC1} = 3.0V$  to  $3.6V$ ,  $V_{SS} = AV_{SS} = 0V$ )

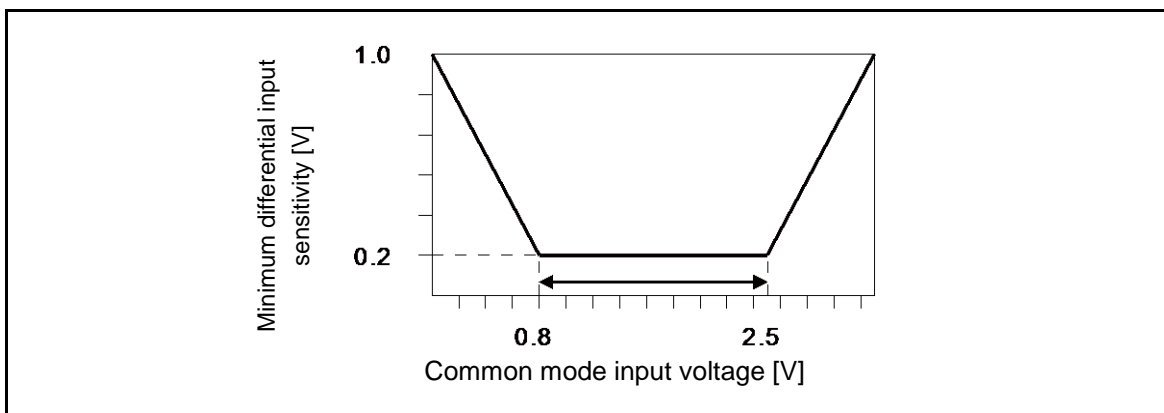
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input characteristics	Input H level voltage	$V_{IH}$	-	2.0	$USBV_{CC} + 0.3$	V	*1
	Input L level voltage	$V_{IL}$	-	$V_{SS} - 0.3$	0.8	V	*1
	Differential input sensitivity	$V_{DI}$	-	0.2	-	V	*2
	Different common mode range	$V_{CM}$	-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	$V_{OH}$	External pull-down resistance = 15 k $\Omega$	2.8	3.6	V	*3
	Output L level voltage	$V_{OL}$	External pull-up resistance = 1.5 k $\Omega$	0.0	0.3	V	*3
	Crossover voltage	$V_{CRS}$	-	1.3	2.0	V	*4
	Rise time	$t_{FR}$	Full-Speed	4	20	ns	*5
	Fall time	$t_{FF}$	Full-Speed	4	20	ns	*5
	Rise/fall time matching	$t_{FRFM}$	Full-Speed	90	111.11	%	*5
	Output impedance	$Z_{DRV}$	Full-Speed	28	44	$\Omega$	*6
	Rise time	$t_{LR}$	Low-Speed	75	300	ns	*7
	Fall time	$t_{LF}$	Low-Speed	75	300	ns	*7
	Rise/fall time matching	$t_{LRFM}$	Low-Speed	80	125	%	*7

1: The switching threshold voltage of the single-end-receiver of USB I/O buffer is set as within  $V_{IL}$  (Max) = 0.8 V,  $V_{IH}$  (Min) = 2.0 V (TTL input standard).

There is some hysteresis applied to lower noise sensitivity.

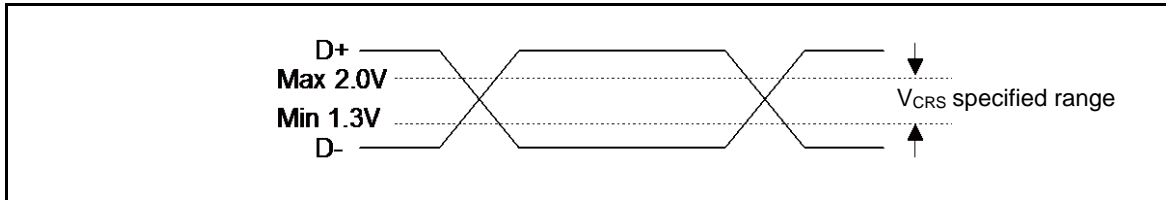
2: Use differential-receiver to receive USB differential data signal. Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

Above voltage range is the common mode input voltage range.

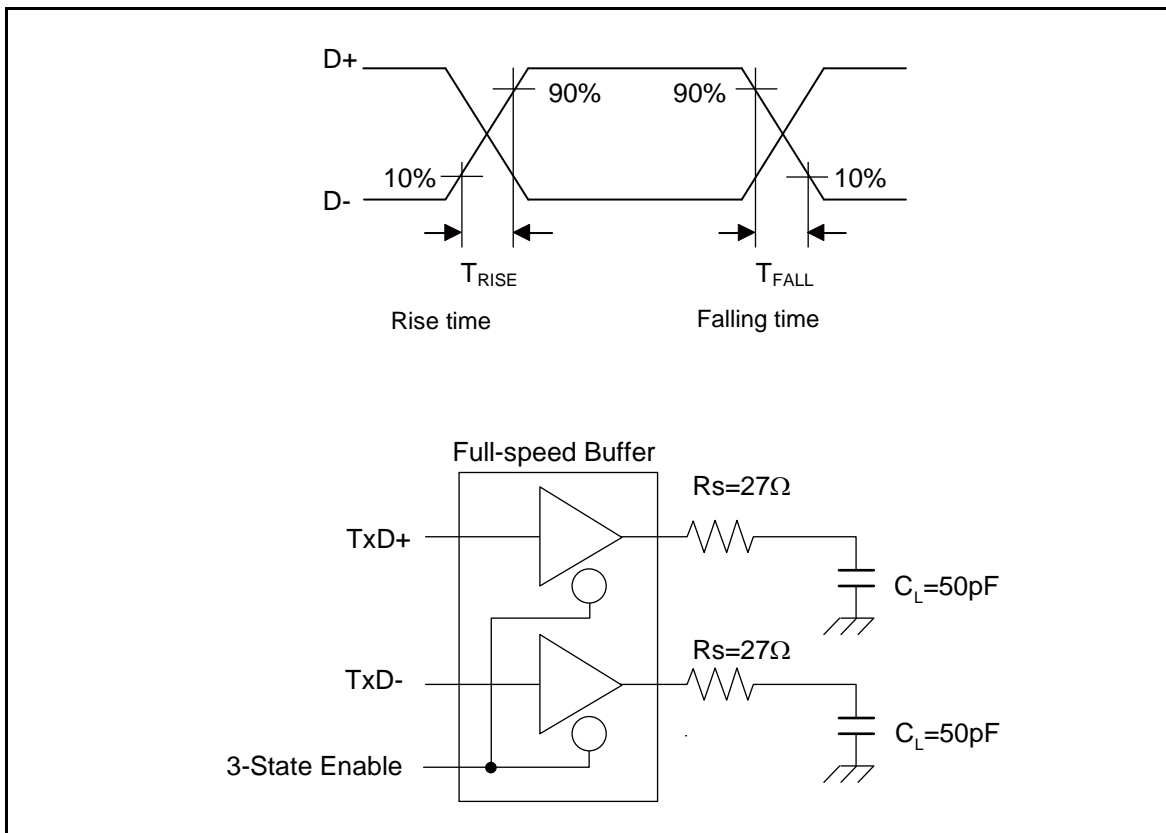




- 3: The output drive capability of the driver is below 0.3 V at low state ( $V_{OL}$ ) (to 3.6 V and 1.5 k $\Omega$  load), and 2.8 V or above (to the VSS and 1.5 k $\Omega$  load) at high state ( $V_{OH}$ ).
- 4: The cross voltage of the external differential output signal (D +/D -) of USB I/O buffer is within 1.3 V to 2.0 V.

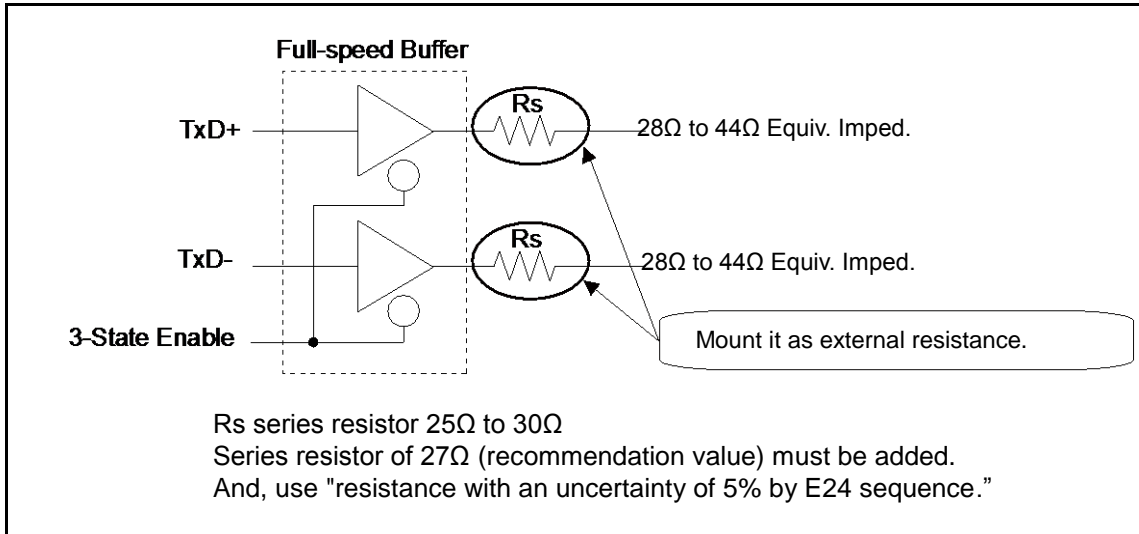


- 5: They indicate rise time ( $t_{RISE}$ ) and fall time ( $t_{FALL}$ ) of the full-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage. For full-speed buffer,  $t_R/t_F$  ratio is regulated as within  $\pm 10\%$  to minimize RFI emission.

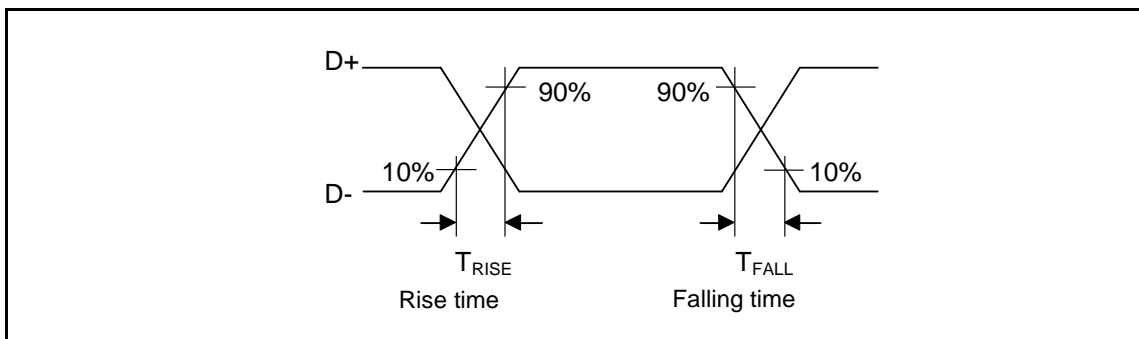


6: USB Full-speed connection is performed via twisted-pair cable shield with  $90\Omega \pm 15\%$  characteristic impedance (differential mode).

USB standard defines that the output impedance of the USB driver must be in the range from  $28\Omega$  to  $44\Omega$ . So, a discrete series resistor ( $R_s$ ) addition is defined in order to satisfy the above definition and keep balance. When using this USB I/O, use it with  $25\Omega$  to  $30\Omega$  (recommended value  $27\Omega$ ) series resistor  $R_s$ .



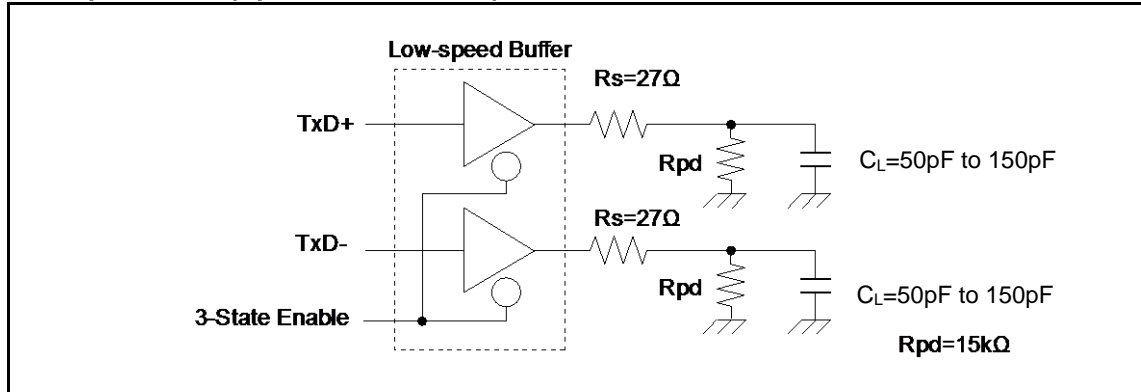
7: They indicate rise time ( $t_{RISE}$ ) and fall time ( $t_{FALL}$ ) of the low-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage.



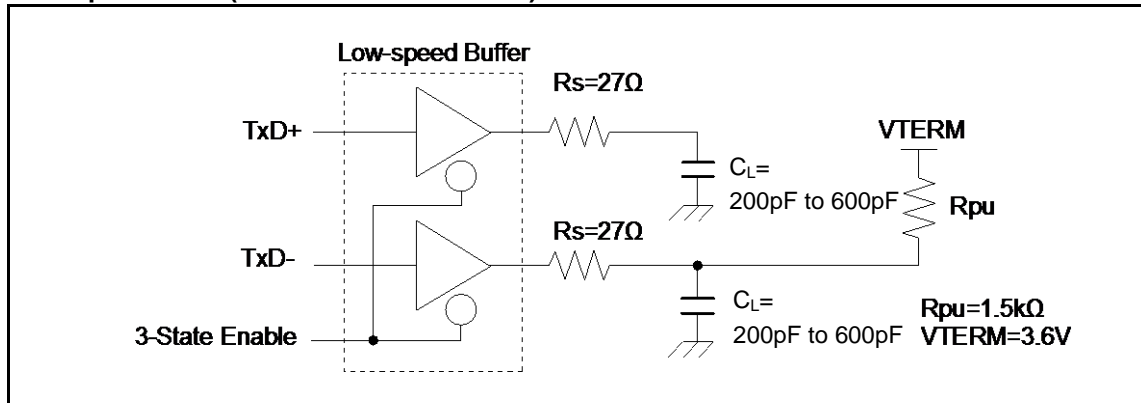
**Note:**

- See Low-Speed Load (Compliance Load) for conditions of external load.

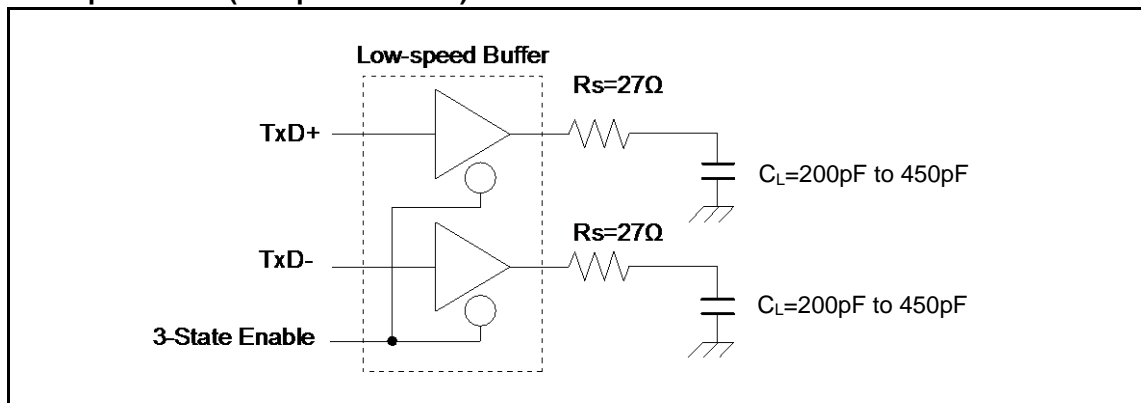
**Low-Speed Load (Upstream Port Load) - Reference 1**



**Low-Speed Load (Downstream Port Load) - Reference 2**



**Low-Speed Load (Compliance Load)**



## 12.7 Low-Voltage Detection Characteristics

### 12.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

### 12.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t <sub>LVDW</sub>	-	-	-	6000xt <sub>CYCP</sub> *	μs	

\*: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.

**12.8 MainFlash Memory Write/Erase Characteristics**

(V<sub>CC</sub> = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	μs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time*		-	13.6	68	s	Includes write time prior to internal erase

\*: It indicates the chip erase time of 1MB MainFlash memory

For devices with 1.5 MB or 2 MB of MainFlash memory, two erase cycles are required.

See 3.2.2 Command Operating Explanations and 3.3.3 Flash Erase Operation in this product's Flash Programming Manual for the detail.

**Write Cycles and Data Retention Time**

Erase/Write Cycles (Cycle)	Data Retention Time (Year)
1,000	20*
10,000	10*
100,000	5*

\*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

**12.9 Standby Recovery Time**

**12.9.1 Recovery Cause: Interrupt/WKUP**

The time from the interrupt occurring to the time of program operation start is shown.

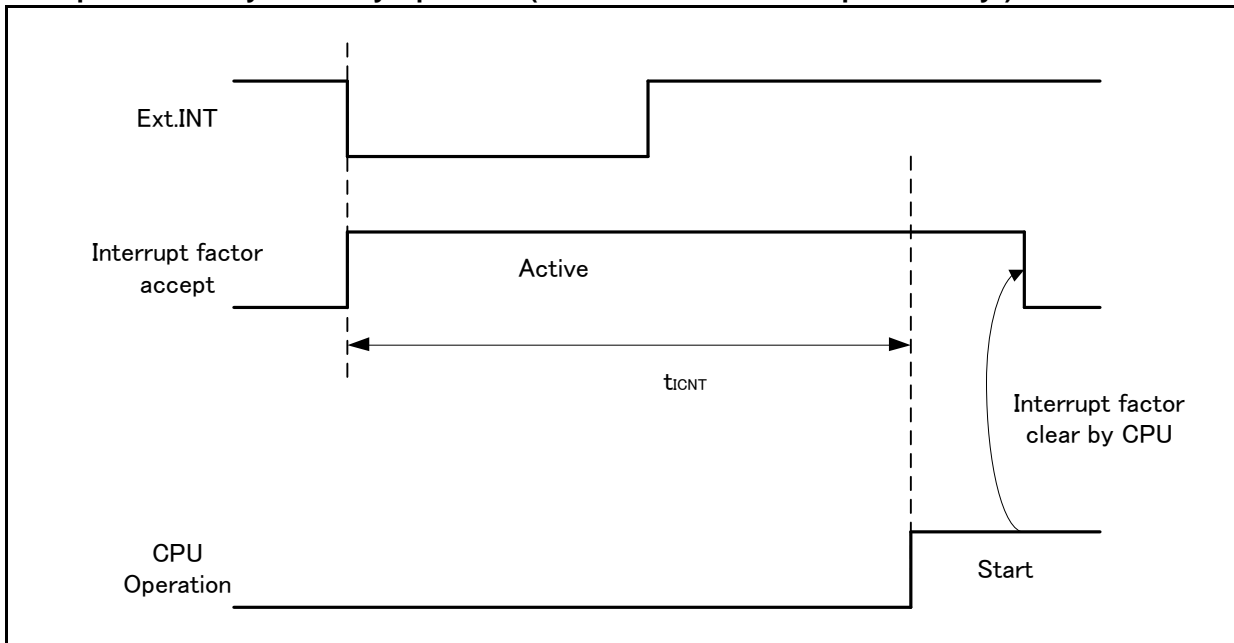
**Recovery Count Time**

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t <sub>ICNT</sub>	HCLKx1		μs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	μs	
Low-speed CR Timer mode		450	900	μs	
Sub Timer mode		896	1136	μs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	μs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	μs	
Deep Standby RTC mode with RAM retention Deep Standby Stop mode with RAM retention		365	667	μs	without RAM retention
		365	667	μs	with RAM retention

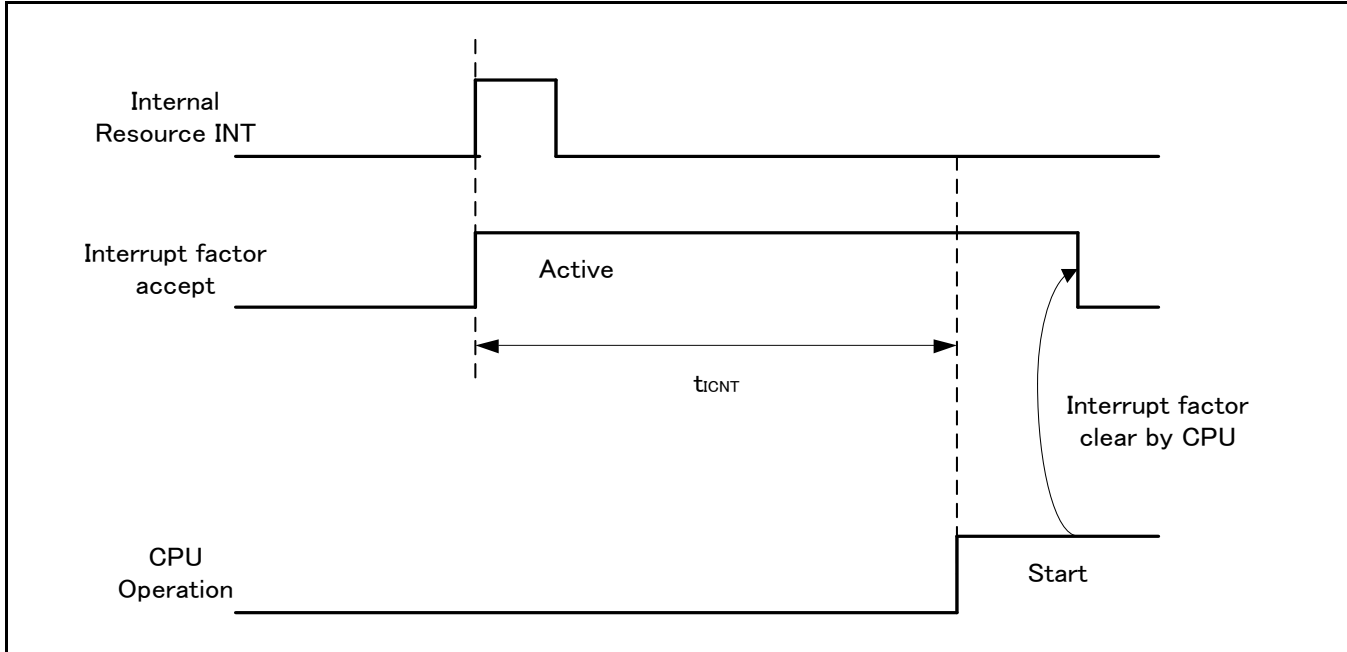
\*: The maximum value depends on the built-in CR accuracy.

**Example of Standby Recovery Operation (when in External Interrupt Recovery\*)**



\*: External interrupt is set to detecting fall edge.

**Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery\*)**



\*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

**Notes:**

- The return factor is different in each low-power consumption mode. See Chapter 6: Low Power Consumption mode and Operations of Standby modes in FM4 Family Peripheral Manual Main Part (002-04856).
- The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).

**12.9.2 Recovery Cause: Reset**

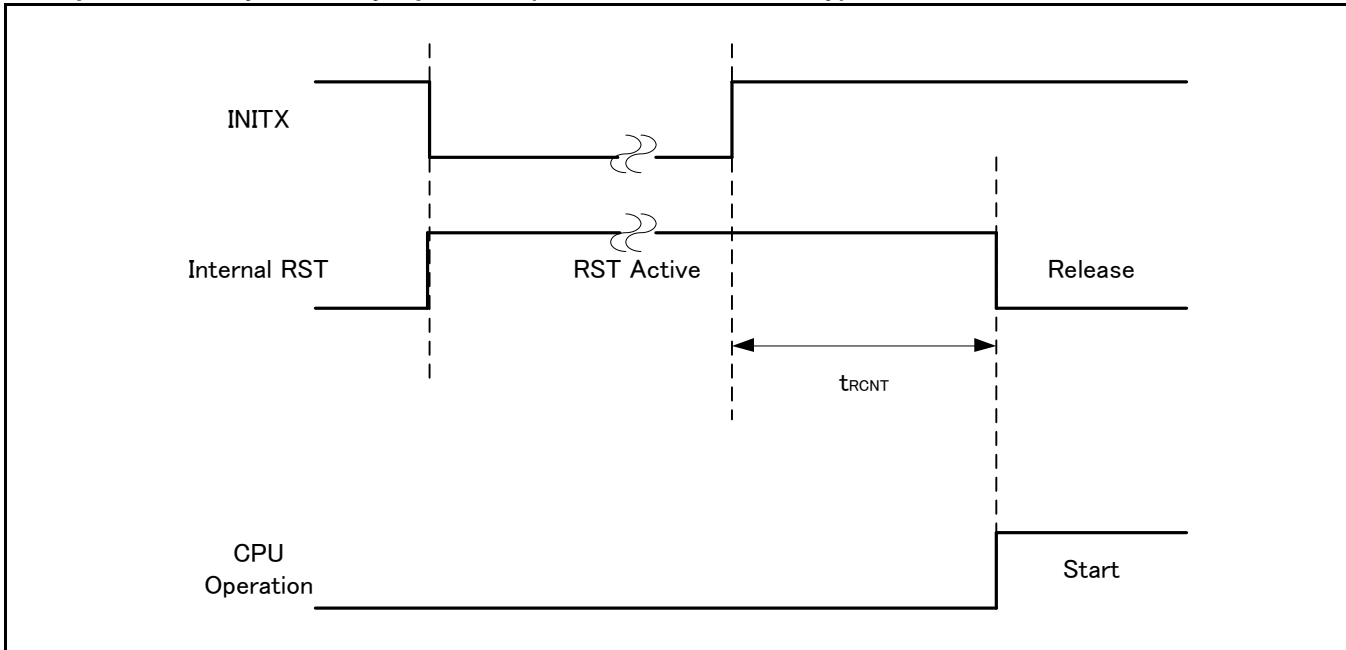
The time from reset release to the program operation start is shown.

**Recovery Count Time**

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ )

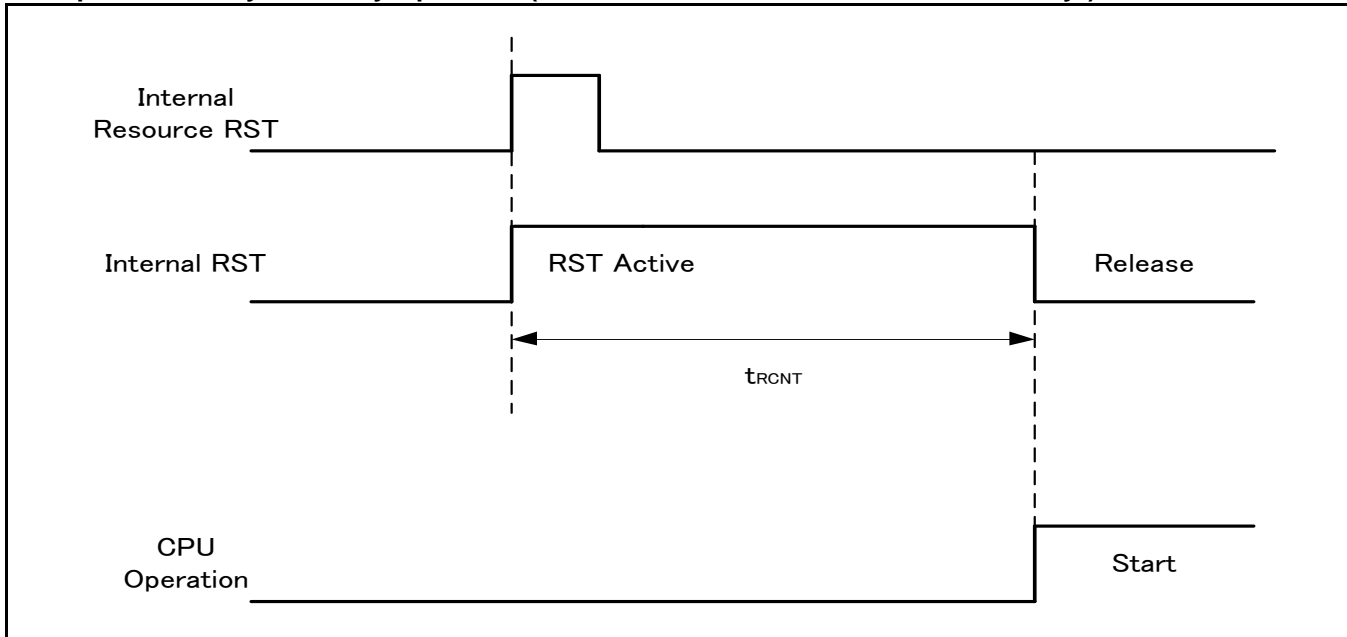
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t <sub>RCNT</sub>	155	266	μs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	μs	
Low-speed CR Timer mode		315	567	μs	
Sub Timer mode		315	567	μs	
RTC mode Stop mode		315	567	μs	
Deep Standby RTC mode with RAM retention		336	667	μs	without RAM retention
Deep Standby Stop mode with RAM retention		336	667	μs	with RAM retention

\*: The maximum value depends on the built-in CR accuracy.

**Example of Standby Recovery Operation (when in INITX Recovery)**




**Example of Standby Recovery Operation (when in Internal Resource Reset Recovery\*)**



\*: Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

**Notes:**

- The return factor is different in each low power consumption mode. See Chapter 6: Low Power Consumption mode and Operations of Standby modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).
- When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.
- In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.
- Internal resource reset indicates Watchdog reset and CSV reset.

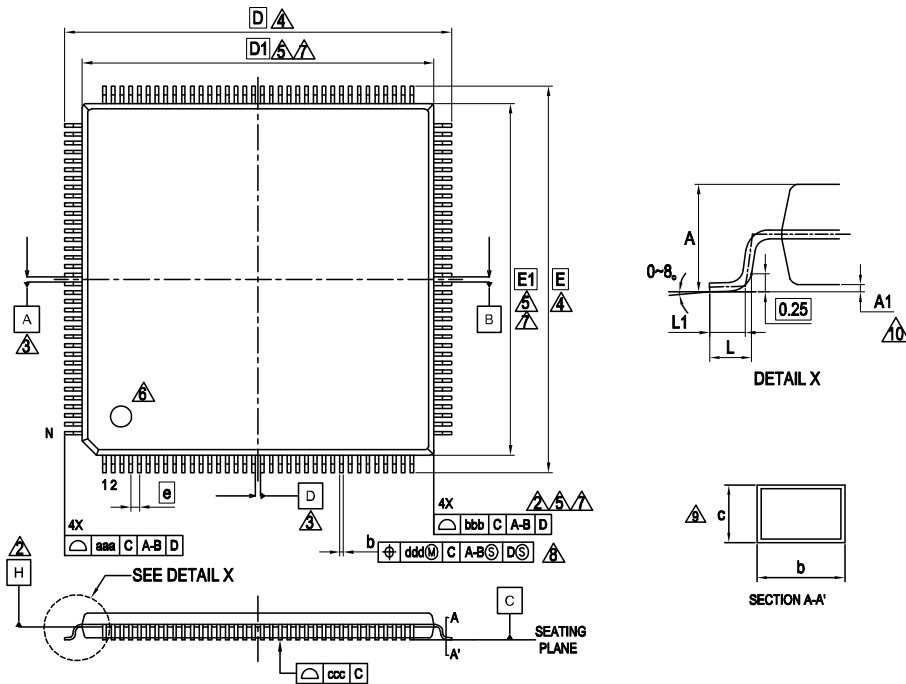
## 13. Ordering Information

Part Number	Flash	RAM	CAN	Ethernet	SD Card	Crypto	Package
S6E2GM6H0AGV20000	512 KB	128 KB	✓	✓	✓		Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2GM8H0AGV20000	1 MB	192 KB	✓	✓	✓		
S6E2GM6HHAGV20000	512 KB	128 KB	✓	✓	✓	✓	
S6E2GM8HHAGV20000	1 MB	192 KB	✓	✓	✓	✓	
S6E2GM6J0AGV20000	512 KB	128 KB	✓	✓	✓		Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2GM8J0AGV20000	1 MB	192 KB	✓	✓	✓		
S6E2GM6JHAGV20000	512 KB	128 KB	✓	✓	✓	✓	
S6E2GM8JHAGV20000	1 MB	192 KB	✓	✓	✓	✓	
S6E2GK6H0AGV20000	512 KB	128 KB		✓	✓		Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2GK8H0AGV20000	1 MB	192 KB		✓	✓		
S6E2GK6HHAGV20000	512 KB	128 KB		✓	✓	✓	
S6E2GK8HHAGV20000	1 MB	192 KB		✓	✓	✓	
S6E2GK6J0AGV20000	512 KB	128 KB		✓	✓		Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2GK8J0AGV20000	1 MB	192 KB		✓	✓		
S6E2GK6JHAGV20000	512 KB	128 KB		✓	✓	✓	
S6E2GK8JHAGV20000	1 MB	192 KB		✓	✓	✓	
S6E2GH6H0AGV20000	512 KB	128 KB	✓		✓		Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2GH8H0AGV20000	1 MB	192 KB	✓		✓		
S6E2GH6J0AGV20000	512 KB	128 KB	✓		✓		Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2GH8J0AGV20000	1 MB	192 KB	✓		✓		
S6E2G36H0AGV20000	512 KB	128 KB					Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2G38H0AGV20000	1 MB	192 KB					
S6E2G36J0AGV20000	512 KB	128 KB					Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2G38J0AGV20000	1 MB	192 KB					
S6E2G26H0AGV20000	512 KB	128 KB		✓			Plastic LQFP (0.5 mm pitch), 144 pin (LQS144)
S6E2G28H0AGV20000	1 MB	192 KB		✓			
S6E2G26HHAGV20000	512 KB	128 KB		✓		✓	
S6E2G28HHAGV20000	1 MB	192 KB		✓		✓	
S6E2G26J0AGV20000	512 KB	128 KB		✓			Plastic LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2G28J0AGV20000	1 MB	192 KB		✓			
S6E2G26JHAGV20000	512 KB	128 KB		✓		✓	
S6E2G28JHAGV20000	1 MB	192 KB		✓		✓	

### 14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS144

#### LQS144 , 144 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQS144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.08	—	0.28
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC.		
D1	20.00 BSC.		
e	0.50 BSC		
E	22.00 BSC.		
E1	20.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	144		

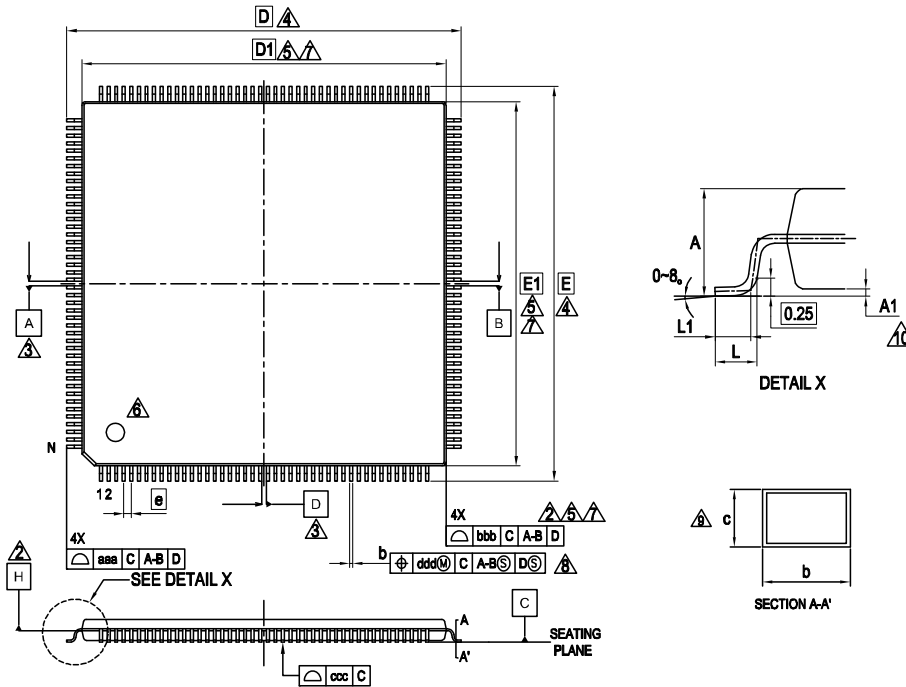
**NOTES**

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- A1 TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
- DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Package Type	Package Code
LQFP 176	LQP176

LQP176 , 176 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQP176		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.50 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	176		

NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

## Document History

Document Title: S6E2G Series 32-bit ARM® Cortex® -M4F, FM4 Microcontroller

Document Number: 001-98708

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4861788	YOHO	07/27/2015	New Spec.
*A	4945035	HITK	11/20/2015	<p>Changed status from Preliminary to Final.</p> <p>Updated <a href="#">4 Pin Description</a>:</p> <p>Added "Note" about TAP pins.</p> <p>Updated <a href="#">12.2 Recommended Operating Conditions</a>:</p> <p>Added the "Smoothing capacitor (C<sub>s</sub>)".</p> <p>Added the "Current Value" in "Maximum leak current at operating".</p> <p>Updated <a href="#">12.3.1 Current Rating</a>:</p> <p>Updated Table 12-1 to Table 12-9:</p> <p>Added the "MAX" value.</p> <p>Updated Table 12-11:</p> <p>Updated <a href="#">12.5 12-bit A/D Converter</a>:</p> <p>Updated "Zero transition" and "Full-scale transition" value.</p> <p>Added "Total error".</p>
*B	5122844	BOO	3/29/2016	<p>Removed full multiplexed signal names from the <a href="#">Pin Assignments</a> drawing.</p> <p>Consolidated the G Series of Cypress MCUs into one data sheet. Added tables to differentiate parts in <a href="#">2 Product Lineup</a> and <a href="#">3 Package-Dependent Features</a>. Expanded <a href="#">13 Ordering Information</a>. Added hyperlinks to <a href="#">6 Pin Descriptions</a>. Added circuit type <b>D</b> to <a href="#">7 I/O Circuit Type</a> and pin state types <b>S</b> and <b>T</b> to <a href="#">11 Pin Status in Each CPU State</a>. Consolidated <a href="#">10 Memory Map</a> to two pages.</p>

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