S6J32E, S6J32F, S6J32G Series

32-bit Microcontroller Traveo™ Datasheet

The S6J32E, S6J32F, and S6J32G series is an extension of the existing S6J3200 series with 4-MB Flash, 512-KB RAM, and Ethernet RMII support.

The S6J3200 series microcontrollers are members of the 55-nm Traveo™ family targeting Cluster and Head-Up Display (HUD). They are built as a single-chip solution to drive a complete mid-range instrument cluster. They can control up to six gauges and drive up to two Thin Film Transistor (TFT) displays with WVGA resolution (854 × 480 pixels each). For connecting a HUD, one display output can be warped on-the-fly for the necessary correction of the windshield bulge. A powerful 2.5D graphics engine enables the device to be used for many mid-range graphics applications.

Features

Key Features

- 240-MHz Arm® Cortex® R5F CPU
- 4-MB internal high-speed Flash memory, 512-KB RAM
- Supports 2.7 V to 5.5 V and 2.7 V to 3.6 V I/O supply voltage
- 1.2-V core power supply
- 50-channel 12-bit SAR A/D converter with 1-Msps conversion rate
- Embedded 4-channel CAN FD controller
- 12-channel Multi-Function Serial (MFS) communication block
- Optional Ethernet AVB with MII and RMII interface
- Two-channel DDR HSSPI
- Optional HyperBus™ interface
- Optional Media-LB (MOST25) interface
- Six-channel Stepper Motor Controller
- Enhanced sound function for high quality
- 2D/2.5D graphics subsystem with video capture, 2-MB VRAM, dual-display support, on-the-fly-warping
- Optional embedded Secure Hardware Extension (SHE) with AES-128 encryption and decryption
- Flash memory retention time up to 20 years
- ASIL-B support on ISO26262 specification
- 216-pin and 208-pin TEQFP packages
- Power domain control

Applications

- Automotive cluster application
- Classic Cluster Control
- Head-Up Display

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1. Overview

1.1 Microcontroller Support Information

http://www.cypress.com/products/cypress-traveo-family-32-bit-arm-cortex-r5-core-based-microcontrollers

1.2 Related Documents

The following table lists the related documents for the S6J32E, S6J32F, and S6J32G series.

Table 1-1 Related Documents

Document Type	Definition	Primary User	Document #
S6J3200 Series, Datasheet	Specifies the function and its characteristics quantitatively.	Investigator and hardware engineer	002-05682
S6J32E, S6J32F, S6J32G Series Hardware Manual	Describes the function and operation of the S6J3200 series.	Software engineer	002-12500
Traveo™ Platform Hardware Manual	Describes the function and operation of the CPU core platform.	Software engineer	002-04854
Supplementary Datasheet	Supplementary information for document, such as differences with the previous revision.	Datasheet user	NA
Supplementary Hardware manual	Supplementary information for document, such as differences with the previous revision.	Hardware manual user.	NA
Application notes	Explanation of the reference software, sample application, the reference board design, and so on.	Software and hardware engineer	AN209861 Getting Started with the Traveo Family S6J3200 Series For more application notes, visit http://www.cypress.com

Notes:

- *Refer to all the documents for system development.*
- *The "primary user" is most likely the engineer who will find the document useful.*
- *The description of the datasheet and the S6J3200 hardware manual should precede the duplicated description of Traveo platform hardware manual.*
- *The Traveo platform hardware manual is expected to be used as a dictionary of platform specification.*
- *Document code usually includes its revision.*
- *Information from the previous revision can be seen in the supplementary documents.*

2. Function List

2.1 Function List Table

The following table shows the functions implemented in the S6J32E, S6J32F, and S6J32G series.

Table 2-1 Function List

Function	Description	Remark
CPU core	Arm Cortex R5F	
FPU	Available (Double precision and Single precision)	
PPU	Available	
MPU	Available	
TPU	Available	
Endian	Little endian	
Core clock frequency	Option	See 2.2.1 and AC Characteristics.
HPM bus frequency	Option	See AC Characteristics
Resource clock frequency	Option	See AC Characteristics
Embedded CR oscillation	Slow clock:100 kHz, Fast clock: 4 MHz (Center frequency)	See AC Characteristics
PLL	PLL0, 1, 2, 3	
SSCG PLL	SSCG0, 1, 2, 3	
Clock supervisor	Available	
DMA	16 ch	
Boot-ROM	16 KB	
JTAG	Available	
Data cache	16 KB	
Instruction cache	16 KB	
Program FLASH	4160 KB	
Work FLASH	112 KB	
TC-RAM	128 KB	
System-RAM	384 KB	
Backup-RAM	16 KB	
Security (SHE)	Option	See 2.2.1
Low latency interrupt	Available	
Power domain	5 domains	
Power supply	5 V ± 0.5 V, 3.3 V ± 0.3 V, 1.2 V ± 0.1 V	
Embedded LDO power supply for 5.0 V	Available	
Low-voltage detection of external power supply	Available	
Low-voltage detection of internal LDO output	Available	
Hardware watchdog timer	Available	
Software watchdog timer	Available	
Package	Option	See 2.2.1
AUTOSAR	AUTOSAR 4.0.3	
GPIO	Option	See 2.2.3
Quad Position and Revolution Counter	2 ch	
I/O timer	3 units x 8 ch	
32-bit Reload timer	14 ch	
Real time clock	Available	Automatic calibration
Sound generator	4 ch	
Sound waveform generator	Option 1 unit x 5 outputs	See 2.2.1
Sound mixer	Option 1 unit x 10 inputs	See 2.2.1
Stereo audio DAC	Option 1 unit (L and R)	See 2.2.1
PCM-PWM	Option 1 unit (L and R)	See 2.2.1
Base timer	12 units (24ch)	

Function	Description	Remark
Free-run timer	12 ch	
Input Capture Unit	12 units (24 channels of capture)	
Output Compare Unit	12units (24 channels of compare match)	
Stepping motor controller (SMC)	For 6 gauges	
12-bit A/D converter	1 unit x 50 input ports (Max)	See 2.2.3
CRC	4 units	
Programmable CRC	1 unit	
Source clock timer	4 ch	
NMI	Available	
External interrupt	16 ch	
Internal interrupt	512 vectors	
I2S	2 ch	One only supports an output as a function of the sound system.
DDR HSSPI	2 ch	A type of Quad SPI
HyperBus (RPC2)	Option	See 2.2.1
Multi-function serial interface	12 ch	
CAN-FD	4 ch	
CAN-FD RAM (ECC supported)	16 KB/ch Equivalent to 128 message buffers per CAN-FD channel	
Ethernet AVB	1 ch	MII-Interface and RMII Interface
Media-LB (MOST25)	1 ch	
Indicator PWM	1 ch	
MPU for AHB	1 unit	
MPU for AXI	1 unit	
Internal VRAM	2 MB	
Graphic engine clock	200 MHz	
Graphic AXI clock	200 MHz	
Display clock	64 MHz (ch.0), 50 MHz(ch.1)	
Display clock source	Graphic display controller clock or external clock	
Target frame rate	60 fps	
Number of display outputs	Maximum 2 outputs simultaneously	See 2.2.1
TTL output (RGB888)	2 ch	Display channel ch.0 Display channel ch.1
RSDS/TCON support	1 output	Display channel ch.0
FPD-Link (LVDS)	1 output, 350 Mbps (Max)	Display channel ch.0 Display channel ch.1
Video capture unit	1 ch	
Video capture format	ITU656, YCbCr4:4:4, YCbCr4:2:2, RGB888, RGB666	
2D Graphic engine	1 unit	
2.5D support	Available	
Vector drawing on 2D engine	Available	
Warping	Available	
Scale/Rotate/Blend	Available	
2D Driver API	Cypress proprietary	

Notes:

- *The options are described in Section 2.2.*
- *The specifications related to the electric characteristics in the table only show the typical values. They do not necessarily include the width of characteristics, errors, and so on. For details, refer to the electrical characteristics sections in this document.*
- *Target resolution of graphics is WVGA 800 × 480, WQVGA 480 × 272.*
- *Target capture resolution of graphics is WVGA 800 × 480.*

2.2 Optional Function

2.2.1 Basic Option

The following figure shows the optional function and the part number relations of the combined S6J3200 and S6J32E, S6J32F, S6J32G Series.

Figure 2-1: Option and Part Number

S 6 J 3 2 0 0 H A A x x x x x x x x

Ordering options 7 digit

Revision

Digit	Description
M	2nd revision, fixed FL0023 [1]
P	3rd revision, fixed FL0023, fixed PEN-182201 [1]
N	4th revision, added alternative location for RXDV on P5_27, fixed FL0027, fixed PEN-182201 [1]

Option

Digit	SHE	Flash Chip erase
S	ON	Enabled
U	OFF	
T	ON	controlled by MK_CEER [2]
V	OFF	

Pin count

Digit	Pin count
K	208 pin
L	216 pin

Memory size

Digit	Program FLASH	Work FLASH	TC-RAM	VRAM
E	4160KB	112KB	128KB	2048KB

Function
See the function digit table.

Product series

Digit	Product type
2	Graphic SoC

Identifier: Automotive MCU

1) Please contact your Cypress sales representative to receive the customer information CI708-00001 and Product Errata documents
2) controlled by Chip erase enable marker MK_CEER

Table 2-2: Function Digit Table for revision N

Part Number	S6J32X (X = function digit)			
Function Digit	E	F	G	H
CPU Clock Maximum (MHz)	240	240	240	240
Graphics Clock Maximum (MHz)	200	200	200	200
Display Output Support (ch. no.)	0, 1	0, 1	0, 1	0, 1
Video Capture Support (units)	1	1	1	1
Graphic Engine Type	2D	2D	2D	2D
Hyper Bus Interface (ch. no.)	0, 1	0, 1	0, 1, 2	0, 1, 2
Sound System	OFF	ON	ON	ON
Ethernet RMII	ON	ON	ON	OFF

Table 2-3: Function Digit Table for revision M and revision P

Part Number	S6J32X (X = function digit)		
Function Digit	E	F	G
CPU Clock Maximum (MHz)	240	240	240
Graphics Clock Maximum (MHz)	200	200	200
Display Output Support (ch. no.)	0, 1	0, 1	0, 1
Video Capture Support (units)	1	1	1
Graphic Engine Type	2D	2D	2D
Hyper Bus Interface (ch. no.)	0, 1	0, 1	0, 1, 2
Sound System	OFF	ON	ON
Ethernet RMII	ON	ON	ON

Notes:

- *This table only shows the relations between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet and confirm actual availability of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The CLK_CPU is assigned to the CPU clock. The CLK_CD3A0 is assigned to the graphic clock. They are defined in the Clock Configuration chapter.*

2.2.2 ID

Each function digit has an ID and revision, which is defined in Figure 2-1.
Chip ID can be read from SYSC0_SYSIDR. For SYSC0_SYSIDR (see the Traveo™ Platform hardware manual).

Function Digit	Memory	Pin Count	Option	Revision	Chip ID	JTAG ID
E	E	K	S	M / P	0x10150001	0x101035CF
			T			0x1010B5CF
			U			0x101135CF
			V			0x1011B5CF
		L	S			0x101015CF
			T			0x101095CF
			U			0x101115CF
			V			0x101195CF
F		K	S			0x101055CF
			T			0x1010D5CF
			U			0x101155CF
			V			0x1011D5CF
		L	S			0x101045CF
			T			0x1010C5CF
			U			0x101145CF
			V			0x1011C5CF
G		K	S			0x101025CF
			T			0x1010A5CF
			U			0x101125CF
			V			0x1011A5CF
		L	S			0x101005CF
			T			0x101085CF
			U			0x101105CF
			V			0x101185CF

Function Digit	Memory	Pin Count	Option	Revision	Chip ID	JTAG ID
E	E	K	S	N	0x10150002	0x201035CF
			T			0x2010B5CF
			U			0x201135CF
			V			0x2011B5CF
		L	S			0x201015CF
			T			0x201095CF
			U			0x201115CF
			V			0x201195CF
F		K	S			0x201055CF
			T			0x2010D5CF
			U			0x201155CF
			V			0x2011D5CF
		L	S			0x201045CF
			T			0x2010C5CF
			U			0x201145CF
			V			0x2011C5CF
G		K	S			0x201025CF
			T			0x2010A5CF
			U			0x201125CF
			V			0x2011A5CF
		L	S			0x201005CF
			T			0x201085CF
			U			0x201105CF
			V			0x201185CF
H		K	S			0x201075CF
			T			0x2010F5CF
			U			0x201175CF
			V			0x2011F5CF
		L	S			0x201065CF
			T			0x2010E5CF
			U			0x201165CF
			V			0x2011E5CF

Note:

- *The JTAG-ID is stored in a memory in the PD2. It can only be read after device startup (VCC12 must be supplied and RSTX must be released).*

2.2.3 Restriction

Some functions have restrictions depending on package pin counts.

Table 2-4: Pin Function Restrictions

Function	TEQFP-216	TEQFP-208
Analog input port (12-bit ADC)	AN0 to AN49 (50 ports available)	AN1 to AN3, AN5 to AN17, AN20, to AN49 (46 ports)
GPIO	P0_00, P0_01, P0_02, P0_03, P0_04, P0_05, P0_06, P0_07, P0_08, P0_09, P0_10, P0_11, P0_12, P0_13, P0_14, P0_15, P0_16, P0_17, P0_18, P0_19, P0_26, P0_27, P0_28, P0_30, P0_31, P1_00, P1_01, P1_02, P1_03, P1_04, P1_05, P1_06, P1_07, P1_08, P1_09, P2_16, P2_17, P2_19, P2_22, P2_24, P2_25, P2_26, P2_27, P2_28, P2_29, P2_30, P2_31, P3_00, P3_01, P3_02, P3_03, P3_04, P3_05, P3_06, P3_07, P3_08, P3_09, P3_10, P3_11, P3_12, P3_13, P3_14, P3_15, P3_16, P3_17, P3_18, P3_19, P3_20, P3_21, P3_22, P3_23, P3_24, P3_25, P3_26, P3_27, P3_28, P3_29, P3_30, P3_31, P4_00, P4_01, P4_02, P4_03, P4_04, P4_05, P4_06, P4_07, P4_08, P4_09, P4_10, P4_11, P4_12, P4_25, P4_26, P4_27, P4_28, P4_29, P4_30, P4_31, P5_00, P5_01, P5_02, P5_03, P5_04, P5_05, P5_06, P5_07, P5_08, P5_09, P5_10, P5_11, P5_12, P5_13, P5_14, P5_15, P5_16, P5_17, P5_18, P5_19, P5_20, P5_21, P5_22, P5_27, P5_28, P5_29, P5_30, P5_31, P6_00 (128 ports)	P0_00, P0_01, P0_04, P0_05, P0_06, P0_07, P0_08, P0_09, P0_10, P0_11, P0_12, P0_13, P0_14, P0_15, P0_16, P0_17, P0_18, P0_19, P0_26, P0_27, P0_28, P0_30, P0_31, P1_00, P1_01, P1_02, P1_03, P1_04, P1_05, P1_06, P1_07, P1_08, P1_09, P2_16, P2_17, P2_19, P2_22, P2_25, P2_26, P2_27, P2_29, P2_30, P2_31, P3_00, P3_01, P3_02, P3_03, P3_04, P3_05, P3_06, P3_07, P3_08, P3_09, P3_12, P3_13, P3_14, P3_15, P3_16, P3_17, P3_18, P3_21, P3_22, P3_23, P3_24, P3_25, P3_26, P3_27, P3_28, P3_29, P3_30, P3_31, P4_00, P4_01, P4_02, P4_03, P4_04, P4_05, P4_06, P4_07, P4_08, P4_09, P4_10, P4_11, P4_12, P4_25, P4_26, P4_27, P4_28, P4_29, P4_30, P4_31, P5_00, P5_01, P5_02, P5_03, P5_04, P5_05, P5_06, P5_07, P5_08, P5_09, P5_10, P5_11, P5_12, P5_13, P5_14, P5_15, P5_16, P5_17, P5_18, P5_19, P5_20, P5_21, P5_22, P5_27, P5_28, P5_29, P5_30, P5_31, P6_00 (120 ports)
PPG triggered input	PPG0/1/2/3/4/5_TIN1, PPG6/7/8/9/10/11_TIN	PPG6/7/8/9/10/11_TIN

Notes:

- *See multiplexed functions on the pin assignment sheet.*
- *The optional restriction will be added without notification.*

3. Product Description

3.1 Overview

This section explains the product features of the S6J3200 series. The description of this section should precede the duplicated description on the platform manual.

3.2 Product Description

The following table describes the product features.

Table 3-1: Feature Description

Feature	Description
Technology	55-nm CMOS technology with embedded FLASH Fully automotive-qualified according to ISO/TS 16949 and AEC-Q100
Functional Safety	The product series has some functional safety features suited for ASIL-B application.
Peripherals	See function list.
Power Domain (PD)	Refer to the platform manual and the *State Transition* section for details. The product series supports the power-off control of PD1, PD2 (including PD3 and 5), and PD6. The power domain resets of PD3 and PD5 included in PD2 are not supported in the product series, and "0" is always read from the reset factor flags of them. This series does not support partial wakeup for PD6.
Debug and Trace	Refer to the platform manual for details. − Standard 5-pin JTAG interface − 4k Word Embedded Trace Buffer 4-bit trace support for TEQFP package.
System Control	Refer to the platform manual for details. Main and sub oscillator is available. − A wide range of 3.6 - 16MHz is available for main oscillator − 32 kHz is available for sub oscillator Sub clock is enabled/disabled by register settings
Clock	Refer to the platform manual for details. CLK_CLKO (Clock Output Function) is not supported. Main Oscillation Stabilization Wait Time (at 4 MHz):8.19 ms (Initial value)
Embedded CR oscillation	Refer to the platform manual for details. Stabilization time is as follows: − 5 µs for 4 MHz (Fast clock) − 20 µs for 100 kHz (Slow clock)
Clock Supervisor	Refer to the platform manual for details. This product series does not support the clock supervisor output port. (Related register and internal circuit is implemented.)
Reset	Refer to the platform manual for details. The following resets are not mounted on this device. − INITX − SRSTX (and nSRST pin) This product series does not support EX5VRST and writing EX5VRSTCNT bits in SYSC0_SPECFGR has no effect.
Hardware Watchdog	Refer to the platform manual for details. The hardware watchdog function stops during the PSS mode. In the related register of HWDG_CFG, the bit ALLOWSTOPCLK is always read as 1 (HWDG_CFG.ALLOWSTOPCLK=1). The product series does not support the Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.)

Feature	Description
Software Watchdog	Refer to the platform manual for details. The product series does not support the Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.)
Standby Mode	Refer to the platform manual for details. Standby mode with 5-V single power supply is available. Turning off the 3.3-V supply and the external 1.2-V supply in standby mode is available. The long-term pulse of the indicator PWM can be outputted during RTC Standby mode.
PLL / SSCG PLL	Refer to the platform manual for details. Use case assumption follows. – PLL ➢ Sound system clock ➢ Sound frequency master clock ➢ Peripherals ➢ Display clock ➢ Trace clock – SSCG ➢ CPU core ➢ GDC core ➢ HyperBus ➢ DDR-HSSPI This product supports down spread and center spread modes with the conditions defined in the Internal Clock Timing section.
External Interrupts	Refer to the platform manual for details.
NMI	Refer to the platform manual for details. 1 NMI pin.
Memory Protection	MPU16 AHB: Refer to the platform manual for details. MPU for AXI: ch.0 (Supervise Ethernet) MPU for AHB: ch.1 (Supervise Media LB) Additional MPU for graphic subsystem, MediaLB, and Ethernet AVB. These are described in the MPU for AHB and MPU for AXI chapters in the hardware manual. To configure Lock or Unlock for both MPUXn_UNLOCK and MPUHn_UNLOCK, – Lock: 0x112ABB56 – Unlock: 0xACCABB56
Peripheral Protection	Refer to the platform manual for details. Protected peripherals are described in the base address map.
Internal Memories System RAM	Refer to the platform manual for details. 1 wait cycle is necessary for RAM read at over 160 MHz. Do not insert wait cycles for RAM write.
Internal Memories TCRAM	Refer to the platform manual for details.
Internal Memories Backup RAM	16 KB Backup RAM can only be operated in RUN mode (normal operation mode). In other modes, the memory content should be retained, but it cannot be operated. SLEEP control for Backup RAM is not supported and cannot be used.
Internal Memories VRAM	ECC region is shared with the user region. Memory size available for the user program is less when ECC is enabled. User can define ECC enabled area and ECC disabled area. Single error correction, double error detection (SECDED) ECC support per 32-bit word.

Feature	Description
Embedded Program/Work Flash Memory	Embedded Program Flash can be accessed with 0-wait-cycle if CPU frequency is 80 MHz or less. 0-wait cycle: 80 MHz or less. 1-wait cycle: 160 MHz or less. 2-wait cycle: more than 160 MHz. Erase suspend is supported. Reading and writing to the other sectors are possible when Flash Erase is suspended. Serial Flash programming and Parallel Flash programming are supported. Margin mode is not supported.
Internal Power Domains	PD1: Always ON PD2: Cortex R5F platform/ GDC/ additional peripherals PD4: Backup RAM PD6: Peripherals * The block diagram section of the TRM explains this in detail.
Power Supply	External 5 V, 3 V, 1.2 V is required. Built-in LDO provides internal 1.2 V for Always On region (PD1). External 1.2-V power supply control pin is supported. External 3.3-V power supply should be controlled by GPIO. There are constraints of power on/off sequence.
Low-voltage Detection	LVD for external voltage is supported. LVD for internal voltage is supported. See the specification of the detected level on the datasheet.
Low-voltage Detection for RAM Retention (RVD)	RVD for RAM retention is effective only during the standby mode. That is, the function is available only for the Backup RAM of 16 KB.
Resource inter-connect	The output signal of some resources can be inputted to the other resource.
I/O Ports	5-V GPIO 3-V GPIO Multi input level and multi output drivability Pull-up, pull-down function is available. Resource input and output is multiplexed. +B input is allowed many pins of the 3.3 V, 5 V, and 3.3 V/5 V I/O domains.
A/D Converter	12-bit resolution, 1 unit 50 channels of analog input for TEQFP-216 46 channels of analog input for TEQFP-208 24 channels of them are shared with the SMC for TEQFP-216/208 External trigger and timer trigger are available. The description of the A/D converter function should be referred in the S6J3200 hardware manual. Do not refer to the description of another A/D converter function in the I/O port chapter of the Traveo PF V3 hardware manual
CRC	Refer to the platform manual for details.
Programmable CRC	DMA support
Sound Generator	Produces sound/melody with varying frequency and amplitude for convenient duration Square wave sound output Automatic linear amplitude increment or decrement Interrupt request generated when specified sound length ends
Sound Waveform Generator	Sine waveform, saw-tooth waveform, and square waveform are generated with easy configuration of the parameters, which specifies sound sources. Fade-in and fade-out control for reverberation.

Feature	Description
Sound Mixer	The input channels of 0 - 4 are reserved for the waveform generator. Mixing different sampling frequency sounds. Mixing internal sounds and external I2S input sounds. Saturating addition function for keeping sound quality. Cut a specific frequency data by digital filter. LPF is supported by FIR filter. Fade-in and Fade-out control.
PCM-PWM	Conversion of PCM audio streaming to pulse-width modulated signals. Supports two output channels for stereo and mono data Up to 16-bit output sample resolution Support for half and full H-bridges
Audio DAC	The sound source of the fixed 48-kHz sampling frequency can be outputted. 1 unit, L/R channels support. BTL connection is available.
I2S	2ch. − I2S0 can output sound sources which are processed by Sound System. − I2S1 can input sound sources which are processed by Sound System. See the "Sound System Configuration" of the S6J3200 hardware manual in detail.
Base Timer	Refer to the platform manual for details. A unit consists of a pair of 16-bit base timers. 12 units, that is, 24 channels of base timers are available.
Reload Timer	Refer to the platform manual for details.
I/O Timer	Refer to the platform manual for details.
Quad Position & Revolution Counter (Up/Down Counter)	Refer to the platform manual for details.
Multi-functional Serial (MFS)	Refer to the platform manual for details. 5 ports of MFS only support I^2C. Note − Not all pins support I^2C. Only pins which have the I^2C I/O characteristics support it. See the datasheet in detail. The I^2C is not designed to be hot swappable. The availability of chip select function can be seen at the Function Digit Table. Chip Select Input is not supported. CTS/RTS is not mounted (hardware flow control is not supported for this series.) WUCR function is not supported for this product.
CAN-FD	Flexible data rate is supported. 16 KB/ch of message RAM is available. The clock output from CAN pre-scaler is supplied to every CAN. ECC error generation function of the message RAM is not supported for this device. Therefore, CAN FD ECC Error Insertion Control Register (FDFECR) is not writeable. CAN-FD rev 3.2 is used. Refer to the platform manual for details
Real Time Clock (RTC) with Auto-calibration	Refer to the platform manual for details.
DDR High Speed SPI	ch.0: HSSPI as a MCU peripheral ch.1: HSSPI on graphic subsystem Refer to the platform manual for details

Feature	Description
HyperBus I/F	ch.0: HyperBus as a MCU peripheral ch.1: HyperBus on graphic subsystem ch.2: HyperBus on graphic subsystem The following registers are not supported. − Controller Status Register (HYPERBUSIn_CSR) − Interrupt Enable Register (HYPERBUSIn_IEN) − Interrupt Status Register (HYPERBUSIn_ISR) − Write Protection Register (HYPERBUSIn_WPR) − Test Register (HYPERBUSIn_TEST) GPO signal can only be used for "Internal Control example by GPO" in this product, that is, it can select using HyperBus of PF or using HyperBus of Graphic sub system. See the "HyperBus Interface Port Configuration" of the S6J32E, S6J32F, S6J32G series hardware manual in detail.
Stepper Motor Control (SMC)	Each channel has 4 motor drivers with high output capability
External Interrupt Capture Unit (EICU)	Refer to the platform manual for details.
Ethernet AVB	10/100 Mbps MII-Interface and RMII-Interface Supports audio-video bridging (AVB) See Section 3.2.1 for details.
MediaLB	MOST25 (512FS) 3 wires Maximum 15 ch is available.
SHE	Refer to the platform manual for details.
Source Clock Timer	Refer to the platform manual for details.
Graphics Subsystem	Variable setting of the GDC clock. (Asynchronous with CPU clock) CPU can directly access VRAM. Programmable panel timing controller with RGB888 and RSDS support.

Note:

− *The description of the preliminary documentation will be changed without any notification.*

3.2.1 Ethernet

The following functions are not supported.

Functions	Remark
External FIFO Interface	
Additional Low Latency TX FIFO Interface for DMA configurations	
MAC Transmit Block - half-duplex - collision - back_pressure	
MAC Filtering Block - external address match - Wakeup On Lan	
Energy Efficient Ethernet support	
LPI Operation in Cadence IP	
PHY Interface - GMII - SGMII - TBI	
10/100/1000 Operation - 1000 M	
SGMII Operation	
Jumbo Frames	
Physical Control Sub-Layer	

The following pin functions are required for MII-Interface and RMII-Interface:

Pin Function	MII-Interface	RMII Interface
RMII_RXERR	Not used	Used
RMII_REFCLK	Not used	Used
RMII_RX0	Not used	Used
RMII_RX1	Not used	Used
RMII_TXD0	Not used	Used
RMII_TXD1	Not used	Used
RXD0	Used	Not used
RXD1	Used	Not used
RXD2	Used	Not used
RXD3	Used	Not used
TXD0	Used	Not used
TXD1	Used	Not used
TXD2	Used	Not used
TXD3	Used	Not used
RXER	Used	Not used
RXDV	Used	Used (CRS_DV function)
RXCLK	Used	Not used
TXER	Used	Not used
TXEN	Used	Used
TXCLK	Used	Not used
MDC	Used	Used
MDIO	Used	Used

3.2.2 RAM Guarantee

For the following reset factors, RAM Guarantee is not supported

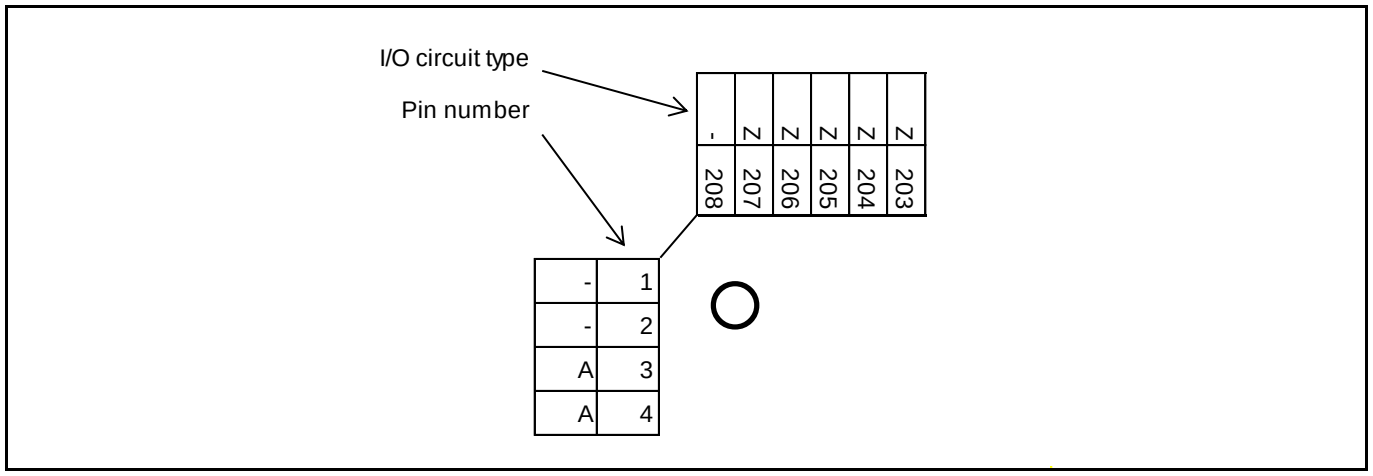
Reset Category	Reset Factor	Operation after Reset is Released				
		Waiting for Stabilization	Mode Evaluation	Security Evaluation	Operation Clock	RAM Guarantee
Hardware Reset	Extended internal power supply low-voltage detection reset	Flash 1.2-V external power supply control	Yes	Yes	Fast CR	No
	RSTX pin input reset External power supply low-voltage detection reset	N/A	Yes	Yes	Fast CR	No

4. Package and Pin Assignment

4.1 Pin Assignment

The characters next to the pin number in the pin assignment drawing specify the I/O circuit type described in Section 5.

Figure 4-1: Pin Number and I/O Circuit Type

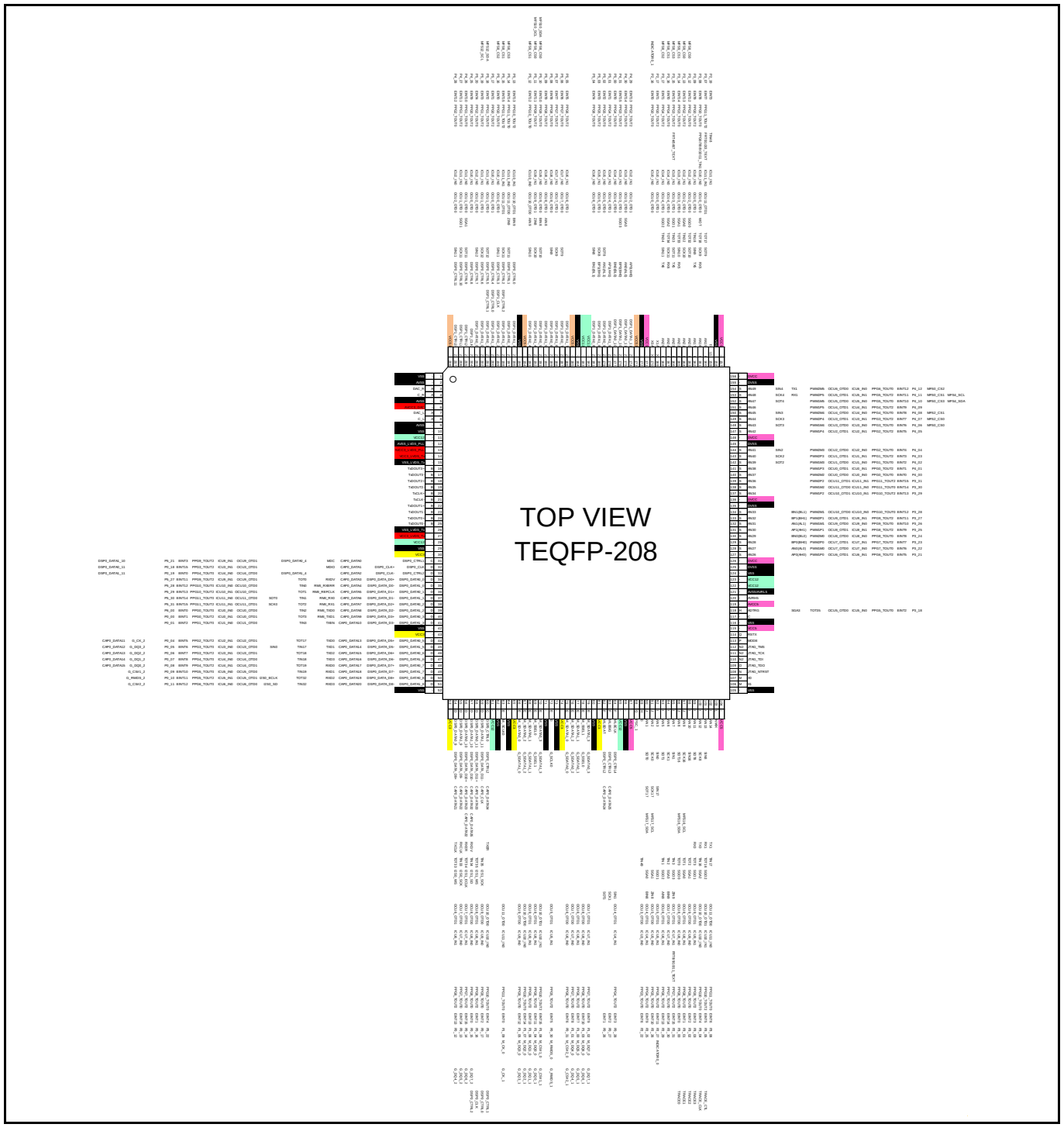


The following port functions are only supported in certain revisions

Port Name	Description	Package Pin Number		Available at revision
		TEQFP-208	TEQFP-216	
RXDV	Ethernet pin	34	34	N

4.1.1 TEQFP-208

Figure 4-2: TEQFP-208 (S6J32EEK, S6J32FEK, S6J32GEK)



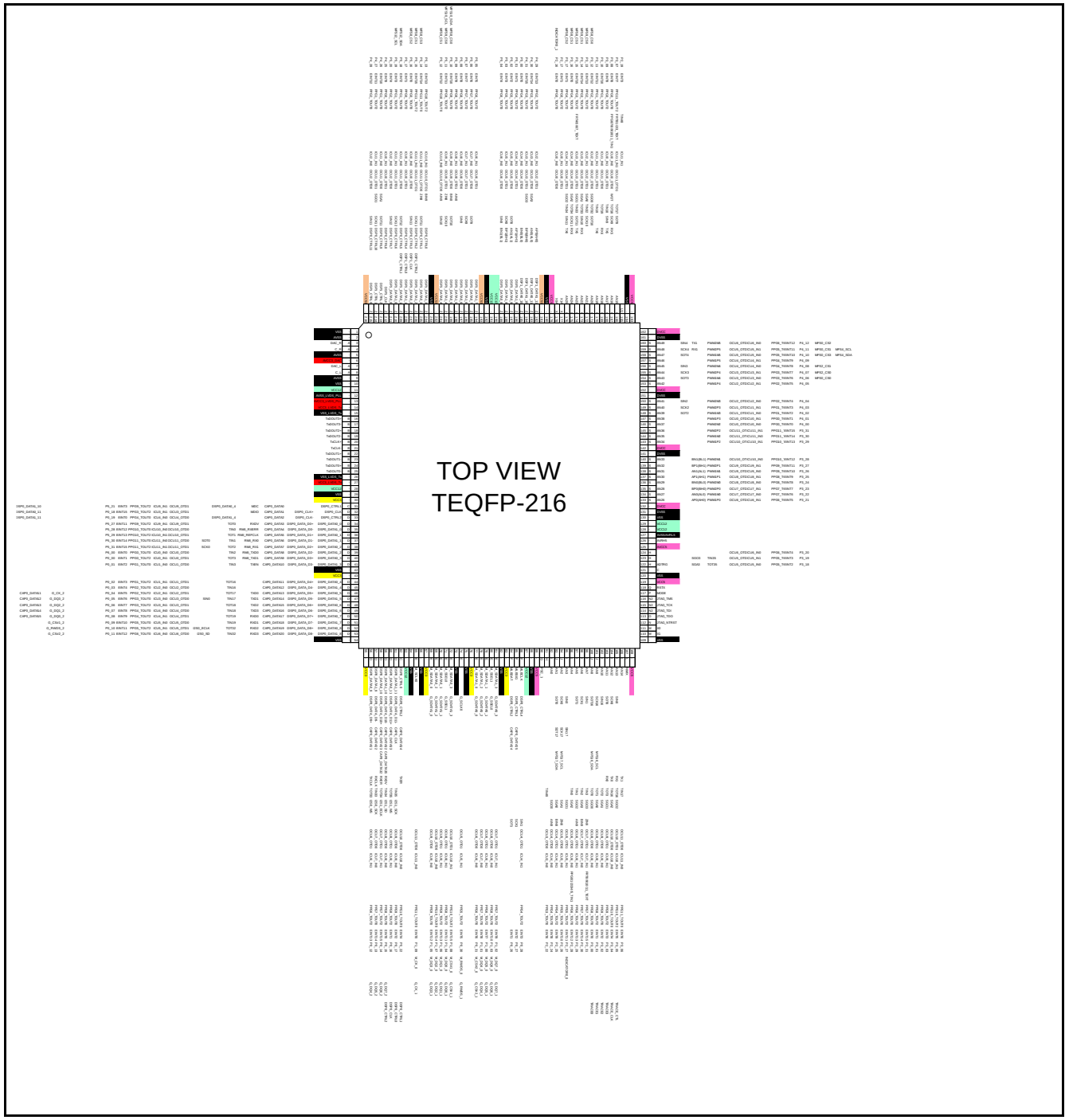
Notes:

Any function at the following pins is not supported by S6J32EEK.

Package Pin Number	Condition on PCB
2, 5, 6, 9	Set to ground
3, 4, 7, 8	Open

4.1.2 TEQFP-216

Figure 4-3: TEQFP-216 (S6J32EEL, S6J32FEL, S6J32GEL)



Notes:

Any function at the following pins is not supported by S6J32EEL.

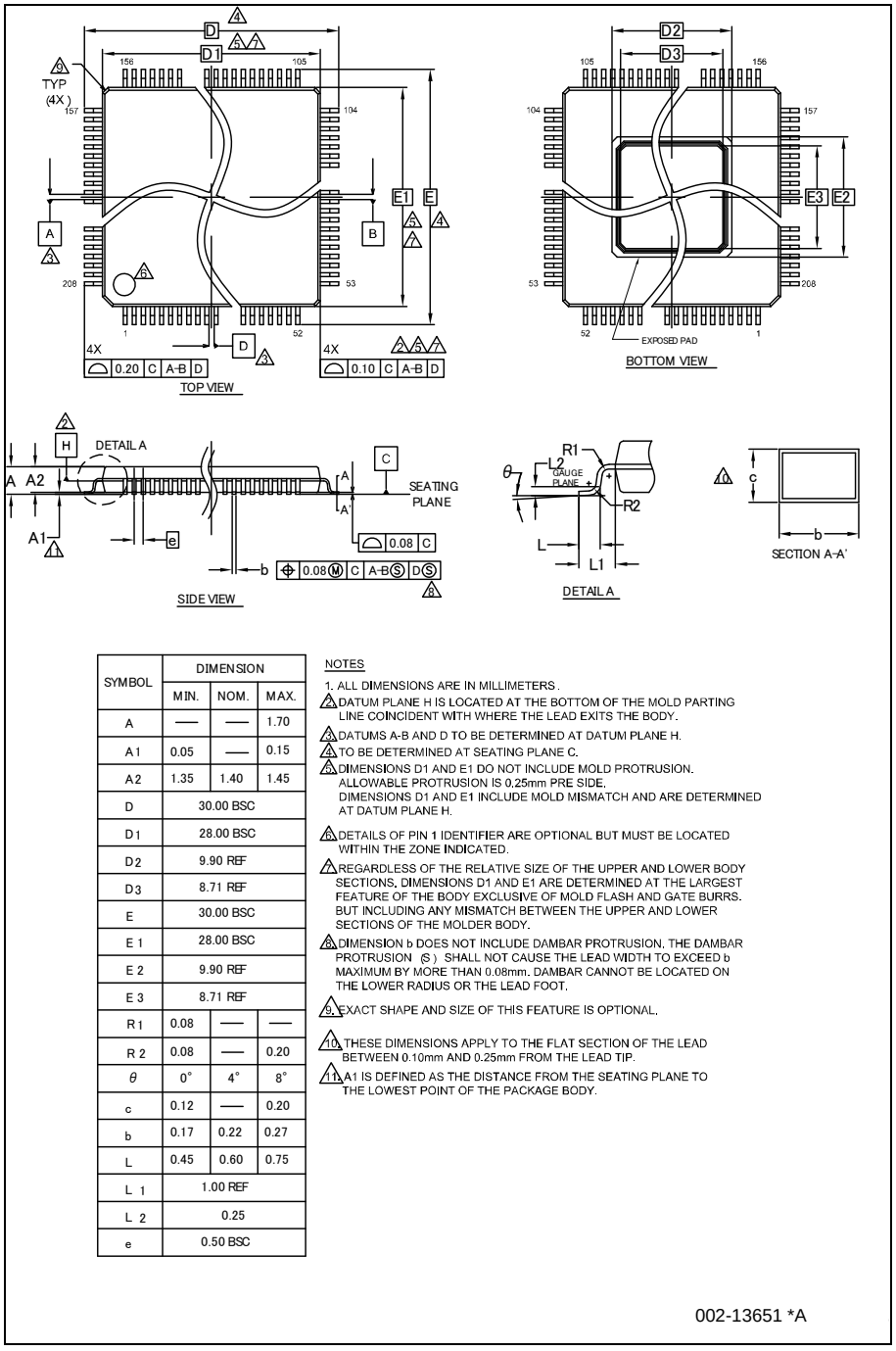
Package Pin Number	Condition on PCB
2, 5, 6, 9	Set to ground
3, 4, 7, 8	Open

4.2 Package Dimensions

Note:
If the same size is specified for min, nom, and max, then it should be regarded as maximum size.

4.2.1 TEQFP-208

Figure 4-4: LET-208



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D		30.00 BSC	
D1		28.00 BSC	
D2		9.90 REF	
D3		8.71 REF	
E		30.00 BSC	
E1		28.00 BSC	
E2		9.90 REF	
E3		8.71 REF	
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	4°	8°
c	0.12	—	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25	
e		0.50 BSC	

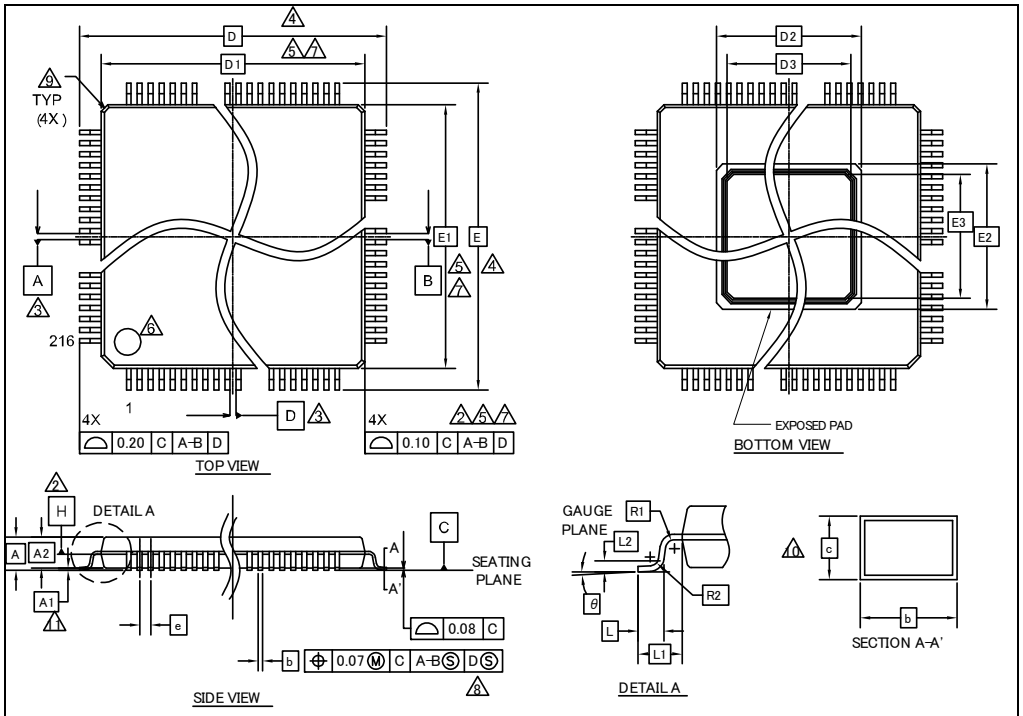
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13651 *A

4.2.2 TEQFP-216

Figure 4-5 LEQ-216



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.70
A 1	0.05	——	0.15
A 2	1.35	1.40	1.45
D		26.00 BSC	
D 1		24.00 BSC	
D 2		9.90 REF	
D 3		8.70 REF	
E		26.00 BSC	
E 1		24.00 BSC	
E 2		9.90 REF	
E 3		8.70 REF	
R 1	0.08	——	——
R 2	0.08	——	0.20
θ	0°	4°	8°
c	0.09	——	0.20
b	0.13	0.18	0.23
L	0.45	0.60	0.75
L 1		1.00 REF	
L 2		0.25	
e		0.40 BSC	

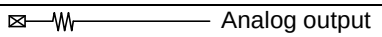
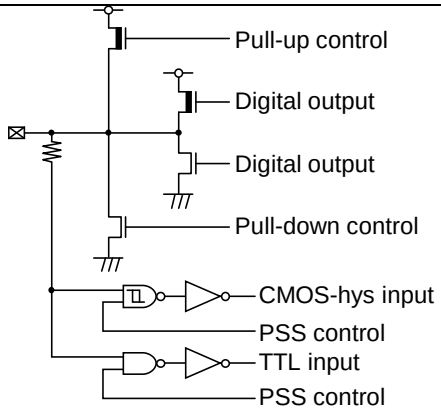
NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

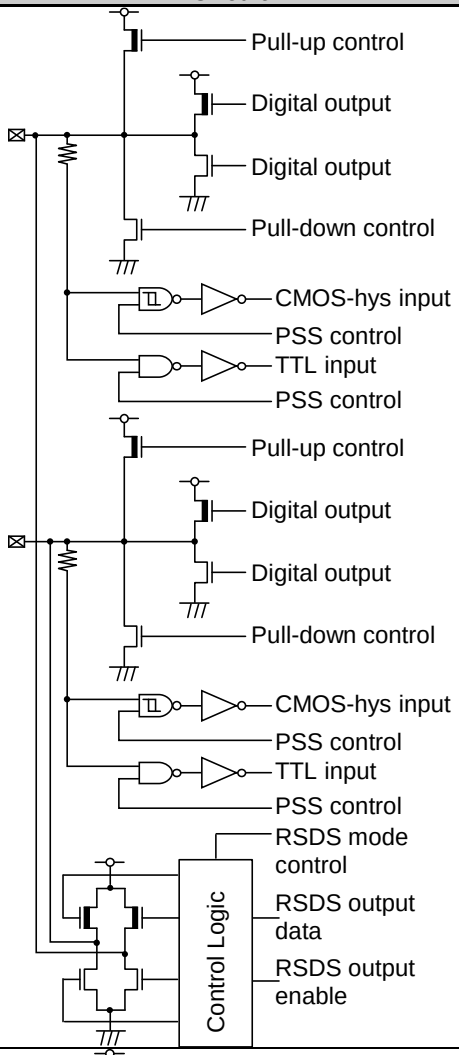
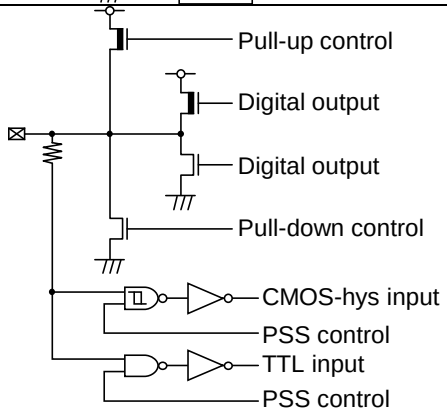
002-10860 *B

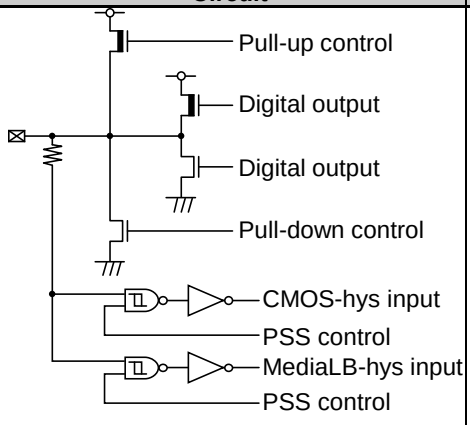
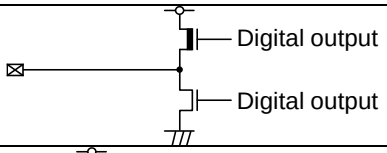
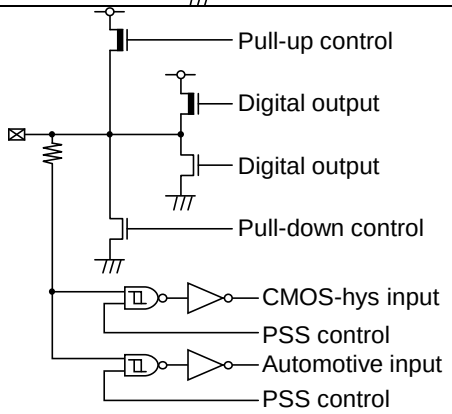
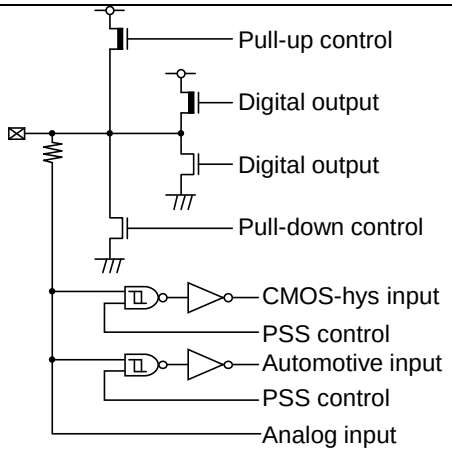
5. I/O Circuit Type

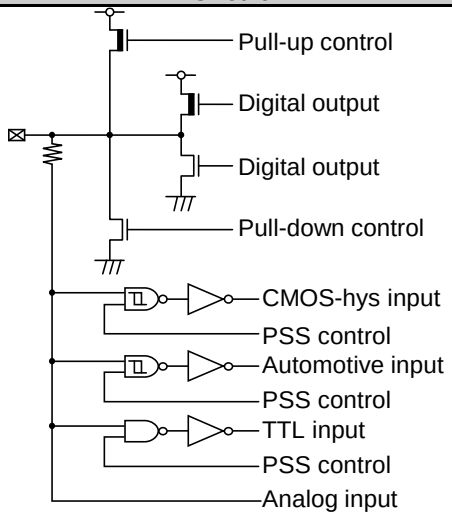
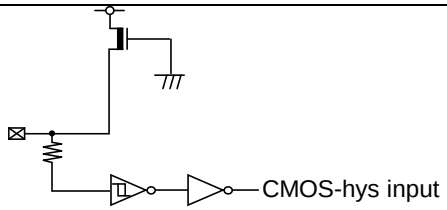
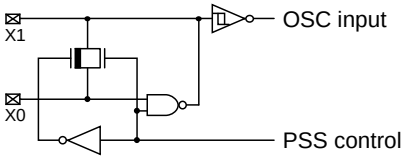
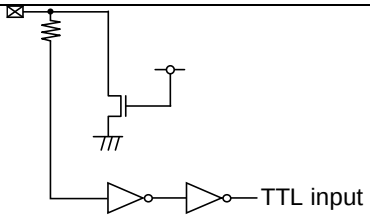
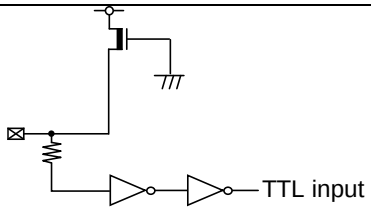
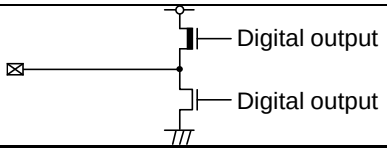
5.1 I/O Circuit Type

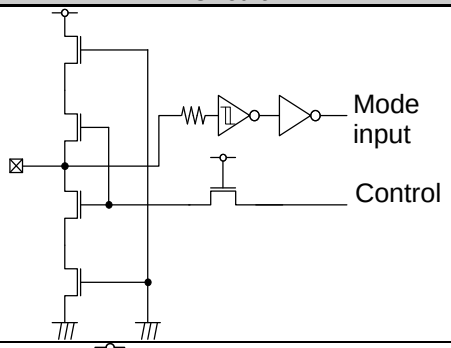
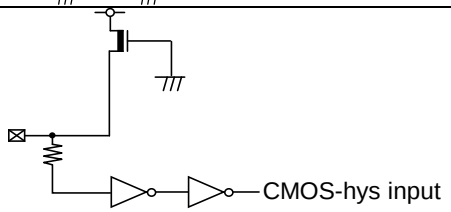
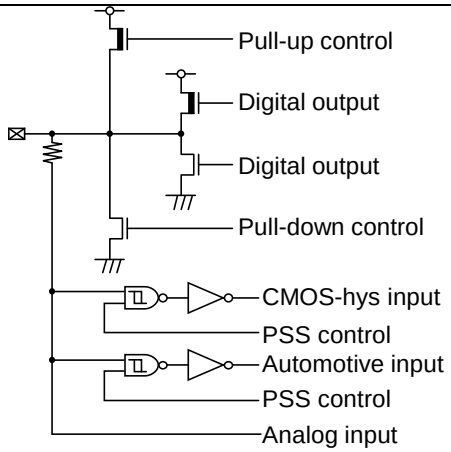
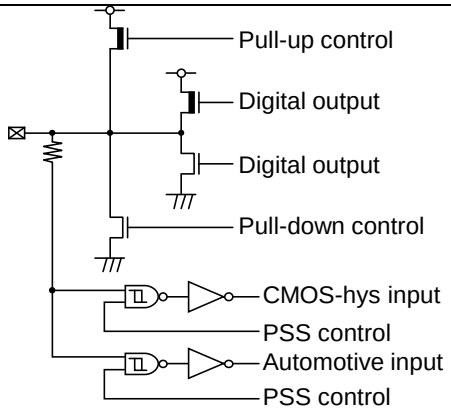
This section explains I/O circuit types. The character denoting the I/O circuit type corresponds to the character for the I/O circuit type in section 4.1.

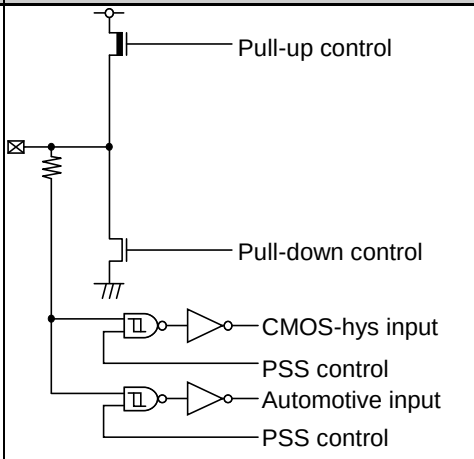
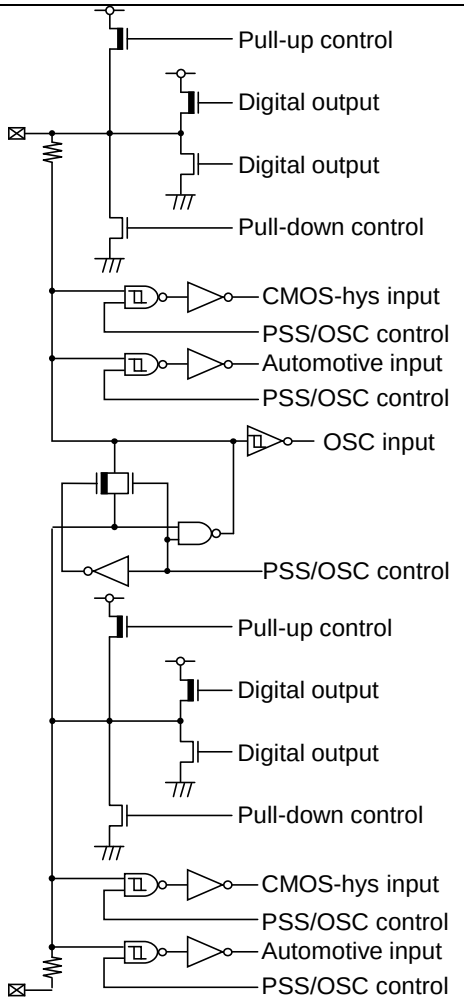
Type	Circuit	Remark
A		Analog output (3 V) Audio DAC output
B		Analog output (3 V) LVDS output
C		General-purpose I/O port Output 2 mA, 5 mA, 10 mA, or 20 mA selectable 33 kΩ with pull-up resistor control 33 kΩ with pull-down resistor control CMOS hysteresis input TTL input

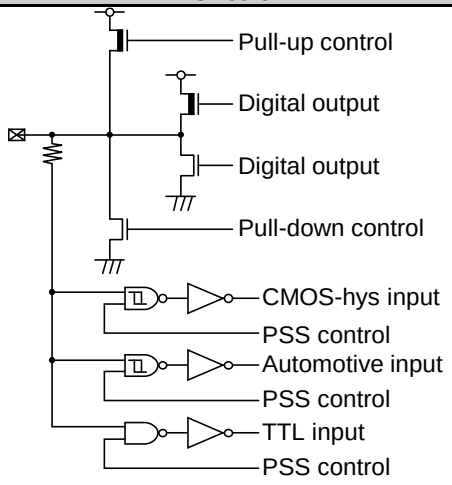
Type	Circuit	Remark
D		General-purpose I/O port Output 2 mA, 5 mA, 10 mA, or 20 mA selectable 33 kΩ with pull-up resistor control 33 kΩ with pull-down resistor control CMOS hysteresis input TTL input RSDS differential output data
E		General-purpose I/O port Output 2 mA, 5 mA, or 10 mA selectable 33 kΩ with pull-up resistor control 33 kΩ with pull-down resistor control CMOS hysteresis input TTL input

Type	Circuit	Remark
F		GPIO port Output 2 mA, 5 mA, 6 mA, or 10 mA selectable 33 kΩ with pull-up resistor control 33 kΩ with pull-down resistor control CMOS hysteresis input MediaLB level hysteresis input
G		External 1.2-V regulator control Output 2 mA
H		GPIO port Output 1 mA, 2 mA, or 5 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input Automotive hysteresis input
I		GPIO port with analog input Output 1 mA, 2 mA, or 5 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input Automotive hysteresis input

Type	Circuit	Remark
J		GPIO port with analog input Output 1 mA, 2 mA, 3 mA (I^2C), or 5 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input Automotive hysteresis input TTL input
L		50 kΩ with pull-up CMOS hysteresis input
M		Main oscillation I/O
N		JTAG_NTRST 50 kΩ with pull-down TTL input
N2		JTAG_TDI/TMS/TCK 50 kΩ with pull-up TTL input
O		JTAG_TDO Output 5 mA

Type	Circuit	Remark
P		Mode input CMOS hysteresis input
Q		CMOS hysteresis input 50 kΩ with pull-up
S		GPIO port with analog input Output 1 mA, 2 mA, 5 mA, or 30 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input Automotive hysteresis input
T		GPIO port Output 1 mA, 2 mA, 5 mA, or 30 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input Automotive hysteresis input

Type	Circuit	Remark
U1		– General-purpose input port – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input Automotive hysteresis input
X		Sub oscillation I/O shared GPIO port Output 1 mA, 2 mA, or 5 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input Automotive hysteresis input

Type	Circuit	Remark
Z		GPIO port Output 1 mA, 2 mA, or 5 mA selectable 50 kΩ with pull-up resistor control 50 kΩ with pull-down resistor control CMOS hysteresis input Automotive hysteresis input TTL input

6. Port Description

6.1 Port Description List

The following table shows the port functions of descriptions that are supported. The port function, which is not described in the table, is not supported for the product.

Port Name	Description	TEQFP-208	TEQFP-216	Remark
VCC12	+1.2-V power supply pin	11, 28, 61, 85, 122, 123, 182, 183	11, 28, 63, 87, 128, 129, 190, 191	
VCC5	+5.0-V power supply pin	87, 104, 115, 157, 171	89, 108, 119, 163, 179	
VCC3	+3.3-V power supply pin	30, 43, 53, 65, 74, 81	30, 43, 55, 67, 76, 83	
VCC53	+3.3 V/+5.0 V selection power supply pin	173, 185, 194, 208	181, 193, 202, 216	
VCC3_LVDS_Tx	LVDS Tx power supply pin	14, 27	14, 27	
VSS	GND	1, 10, 29, 42, 52, 62, 64, 71, 73, 80, 86, 105, 116, 124, 158, 172, 184, 195	1, 10, 29, 42, 54, 64, 66, 73, 75, 82, 88, 109, 120, 130, 164, 180, 192, 203	
VSS_LVDS_Tx	LVDS Tx GND	15, 26	15, 26	
AVCC3_DAC	Audio DAC power supply pin	6	6	Not available on S6J32EE, connect to GND
AVCC3_LVDS_PLL	LVDS PLL power supply pin	13	13	
AVSS_LVDS_PLL	LVDS PLL GND	12	12	
AVCC5	A/D converter analog power supply pin	119	125	
AVRH5	A/D converter upper limit reference voltage pin	120	126	
AVSS	Audio DAC GND	2, 5, 9	2, 5, 9	Not available on S6J32EE, connect to GND
AVSS/AVRL5	A/D converter GND, A/D converter lower limit reference voltage	121	127	
DVCC	SMC large current port power supply pin	126, 136, 146, 156	132, 142, 152, 162	
DVSS	SMC large current port GND	125, 135, 145, 155	131, 141, 151, 161	
X1	Main clock oscillator output pin	106	110	
X0	Main clock oscillator input pin	107	111	
X1A	Sub-clock oscillator output	169	177	
X0A	Sub-clock oscillator input	170	178	
NMIX	Non-maskable interrupt input pin	103	107	
RSTX	External reset input pin	114	118	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
PSC_1	External power supply control pin	88	90	
MODE	Mode pin	113	117	
C	External capacity connection output pin	117	121	
JTAG_NTRST	JTAG test reset input pin	108	112	
JTAG_TDO	JTAG test data output pin	109	113	
JTAG_TDI	JTAG test data input pin	110	114	
JTAG_TCK	JTAG test clock input pin	111	115	
JTAG_TMS	JTAG test mode state input pin	112	116	
TRACE0	Trace data 0 output pin	96	100	
TRACE1	Trace data 1 output pin	97	101	
TRACE2	Trace data 2 output pin	98	102	
TRACE3	Trace data 3 output pin	99	103	
TRACE4	Trace data 4 output pin	-	-	
TRACE5	Trace data 5 output pin	-	-	
TRACE6	Trace data 6 output pin	-	-	
TRACE7	Trace data 7 output pin	-	-	
TRACE8	Trace data 8 output pin	-	-	
TRACE9	Trace data 9 output pin	-	-	
TRACE10	Trace data 10 output pin	-	-	
TRACE11	Trace data 11 output pin	-	-	
TRACE12	Trace data 12 output pin	-	-	
TRACE13	Trace data 13 output pin	-	-	
TRACE14	Trace data 14 output pin	-	-	
TRACE15	Trace data 15 output pin	-	-	
TRACE_CLK	Trace clock	100	104	
TRACE_CTL	Trace control	101	105	
ADTRG	A/D converter external trigger input pin	118	122	
AN0	ADC Analog 0 input pin	-	92	
AN1	ADC Analog 1 input pin	90	93	
AN2	ADC Analog 2 input pin	91	94	
AN3	ADC Analog 3 input pin	92	95	
AN4	ADC Analog 4 input pin	-	96	
AN5	ADC Analog 5 input pin	93	97	
AN6	ADC Analog 6 input pin	94	98	
AN7	ADC Analog 7 input pin	95	99	
AN8	ADC Analog 8 input pin	96	100	
AN9	ADC Analog 9 input pin	97	101	
AN10	ADC Analog 10 input pin	98	102	
AN11	ADC Analog 11 input pin	99	103	
AN12	ADC Analog 12 input pin	100	104	
AN13	ADC Analog 13 input pin	101	105	
AN14	ADC Analog 14 input pin	102	106	
AN15	ADC Analog 15 input pin	160	166	
AN16	ADC Analog 16 input pin	161	167	
AN17	ADC Analog 17 input pin	162	168	
AN18	ADC Analog 18 input pin	-	169	
AN19	ADC Analog 19 input pin	-	170	
AN20	ADC Analog 20 input pin	163	171	
AN21	ADC Analog 21 input pin	164	172	
AN22	ADC Analog 22 input pin	165	173	
AN23	ADC Analog 23 input pin	166	174	
AN24	ADC Analog 24 input pin	167	175	
AN25	ADC Analog 25 input pin	168	176	
AN26	ADC Analog 26 input pin	127	133	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
AN27	ADC Analog 27 input pin	128	134	
AN28	ADC Analog 28 input pin	129	135	
AN29	ADC Analog 29 input pin	130	136	
AN30	ADC Analog 30 input pin	131	137	
AN31	ADC Analog 31 input pin	132	138	
AN32	ADC Analog 32 input pin	133	139	
AN33	ADC Analog 33 input pin	134	140	
AN34	ADC Analog 34 input pin	137	143	
AN35	ADC Analog 35 input pin	138	144	
AN36	ADC Analog 36 input pin	139	145	
AN37	ADC Analog 37 input pin	140	146	
AN38	ADC Analog 38 input pin	141	147	
AN39	ADC Analog 39 input pin	142	148	
AN40	ADC Analog 40 input pin	143	149	
AN41	ADC Analog 41 input pin	144	150	
AN42	ADC Analog 42 input pin	147	153	
AN43	ADC Analog 43 input pin	148	154	
AN44	ADC Analog 44 input pin	149	155	
AN45	ADC Analog 45 input pin	150	156	
AN46	ADC Analog 46 input pin	151	157	
AN47	ADC Analog 47 input pin	152	158	
AN48	ADC Analog 48 input pin	153	159	
AN49	ADC Analog 49 input pin	154	160	
TX0	CAN transmission data 0 output pin	100	104	
TX1	CAN transmission data 1 output pin	102, 154	106, 160	
TX5	CAN transmission data 5 output pin	162, 166	168, 174	
TX6	CAN transmission data 6 output pin	168	170, 176	
RX0	CAN reception data 0 input pin	99	103	
RX1	CAN reception data 1 input pin	101, 153	105, 159	
RX5	CAN reception data 5 input pin	161, 165	167, 173	
RX6	CAN reception data 6 input pin	167	169, 175	
EINT0	External interrupt input pin	33, 39, 57, 63, 96, 140, 167, 170, 177, 199	33, 39, 59, 65, 100, 146, 175, 178, 185, 207	
EINT1	External interrupt input pin	40, 58, 82, 97, 141, 168, 169, 178, 200	40, 60, 84, 101, 147, 176, 177, 186, 208	
EINT2	External interrupt input pin	41, 59, 83, 98, 118, 142, 179, 201	41, 61, 85, 102, 122, 148, 187, 209	
EINT3	External interrupt input pin	31, 84, 99, 143, 159, 180, 202	31, 44, 86, 103, 123, 149, 165, 188, 210	
EINT4	External interrupt input pin	60, 100, 144, 181, 203	45, 62, 104, 124, 150, 189, 211	
EINT5	External interrupt input pin	44, 72, 101, 127, 147, 186	46, 74, 105, 133, 153, 194	
EINT6	External interrupt input pin	45, 75, 89, 102, 128, 148, 187	47, 77, 91, 106, 134, 154, 195	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
EINT7	External interrupt input pin	46, 77, 129, 149, 160, 188	48, 79, 135, 155, 166, 196	
EINT8	External interrupt input pin	47, 76, 130, 150, 161, 189	49, 78, 92, 136, 156, 167, 197	
EINT9	External interrupt input pin	48, 79, 90, 131, 151, 162, 190, 204	50, 81, 93, 137, 157, 168, 198, 212	
EINT10	External interrupt input pin	49, 78, 91, 132, 152, 191, 205	51, 80, 94, 138, 158, 169, 199, 213	
EINT11	External interrupt input pin	34, 50, 69, 92, 133, 153, 192, 206	34, 52, 71, 95, 139, 159, 170, 200, 214	
EINT12	External interrupt input pin	35, 51, 66, 134, 154, 163, 193, 207	35, 53, 68, 96, 140, 160, 171, 201, 215	
EINT13	External interrupt input pin	36, 54, 68, 93, 137, 164, 174, 196	36, 56, 70, 97, 143, 172, 182, 204	
EINT14	External interrupt input pin	37, 55, 67, 94, 138, 165, 175, 197	37, 57, 69, 98, 144, 173, 183, 205	
EINT15	External interrupt input pin	32, 38, 56, 70, 95, 139, 166, 176, 198	32, 38, 58, 72, 99, 145, 174, 184, 206	
MFS0_CS0	Multi-function serial ch.0 chip select 0 pin	148	154	
MFS0_CS1	Multi-function serial ch.0 chip select 1 pin	153	159	
MFS0_CS2	Multi-function serial ch.0 chip select 2 pin	154	160	
MFS0_CS3	Multi-function serial ch.0 chip select 3 pin	152	158	
MFS2_CS0	Multi-function serial ch.2 chip select 0 pin	149	155	
MFS2_CS1	Multi-function serial ch.2 chip select 1 pin	150	156	
MFS8_CS0	Multi-function serial ch.8 chip select 0 pin	163, 191	171, 199	
MFS8_CS1	Multi-function serial ch.8 chip select 1 pin	167, 198	175, 206	
MFS8_CS2	Multi-function serial ch.8 chip select 2 pin	168, 199	176, 207	
MFS8_CS3	Multi-function serial ch.8 chip select 3 pin	166, 197	174, 205	
MFS9_CS0	Multi-function serial ch.9 chip select 0 pin	164, 192	172, 200	
MFS9_CS1	Multi-function serial ch.9 chip select 1 pin	165, 193	173, 201	
SCK0	Multi-function serial ch.0 clock I/O pin	38, 91	38, 94	
SCK1	Multi-function serial ch.1 clock I/O pin	83, 94	85, 98	
SCK2	Multi-function serial ch.2 clock I/O pin	143	149	
SCK3	Multi-function serial ch.3 clock I/O pin	149	155	
SCK4	Multi-function serial ch.4 clock I/O pin	153	159	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
SCK8	Multi-function serial ch.8 clock I/O pin	100, 180	104, 188	
SCK9	Multi-function serial ch.9 clock I/O pin	161, 188	167, 196	
SCK10	Multi-function serial ch.10 clock I/O pin	164, 192	172, 200	
SCK11	Multi-function serial ch.11 clock I/O pin	167, 198, 206	175, 206, 214	
SCK12	Multi-function serial ch.12 clock I/O pin	202	210	
SCK16	Multi-function serial ch.16 clock I/O pin	97	101	
SCK17	Multi-function serial ch.17 clock I/O pin	91	94	
SIN0	Multi-function serial ch.0 serial data input pin	45, 92	47, 95	
SIN1	Multi-function serial ch.1 serial data input pin	84, 95	86, 99	
SIN2	Multi-function serial ch.2 serial data input pin	144	150	
SIN3	Multi-function serial ch.3 serial data input pin	150	156	
SIN4	Multi-function serial ch.4 serial data input pin	154	160	
SIN8	Multi-function serial ch.8 serial data input pin	101, 181	105, 189	
SIN9	Multi-function serial ch.9 serial data input pin	162, 189	168, 197	
SIN10	Multi-function serial ch.10 serial data input pin	165, 193	173, 201	
SIN11	Multi-function serial ch.11 serial data input pin	168, 199, 207	176, 207, 215	
SIN12	Multi-function serial ch.12 serial data input pin	203	211	
SIN16	Multi-function serial ch.16 serial data input pin	98	102	
SIN17	Multi-function serial ch.17 serial data input pin	92	95	
SOT0	Multi-function serial ch.0 serial data output pin	37, 90	37, 93	
SOT1	Multi-function serial ch.1 serial data output pin	82, 93	84, 97	
SOT2	Multi-function serial ch.2 serial data output pin	142	148	
SOT3	Multi-function serial ch.3 serial data output pin	148	154	
SOT4	Multi-function serial ch.4 serial data output pin	152	158	
SOT8	Multi-function serial ch.8 serial data output pin	99, 179	103, 187	
SOT9	Multi-function serial ch.9 serial data output pin	160, 187	166, 195	
SOT10	Multi-function serial ch.10 serial data output pin	163, 191	171, 199	
SOT11	Multi-function serial ch.11 serial data output pin	166, 197, 205	174, 205, 213	
SOT12	Multi-function serial ch.12 serial data output pin	201	209	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
SOT16	Multi-function serial ch.16 serial data output pin	96	100	
SOT17	Multi-function serial ch.17 serial data output pin	90	93	
MFS4_SCL	I^2C ch.4 clock I/O pin	153	159	
MFS10_SCL	I^2C ch.10 clock I/O pin	192	200	
MFS12_SCL	I^2C ch.12 clock I/O pin	202	210	
MFS16_SCL	I^2C ch.16 clock I/O pin	97	101	
MFS17_SCL	I^2C ch.17 clock I/O pin	91	94	
MFS4_SDA	I^2C ch.4 serial data I/O pin	152	158	
MFS10_SDA	I^2C ch.10 serial data I/O pin	191	199	
MFS12_SDA	I^2C ch.12 serial data I/O pin	201	209	
MFS16_SDA	I^2C ch.16 serial data I/O pin	96	100	
MFS17_SDA	I^2C ch.17 serial data I/O pin	90	93	
PPG0_TOUT0	Base timer 0 output pin	39, 140, 161, 170, 199	39, 146, 167, 178, 207	
PPG0_TOUT2	Base timer 1 output pin	40, 141, 162, 169, 200, 204	40, 147, 168, 177, 208, 212	
PPG1_TOUT0	Base timer 2 output pin	41, 142, 201, 205	41, 148, 169, 209, 213	
PPG1_TOUT2	Base timer 3 output pin	143, 202, 206	44, 149, 170, 210, 214	
PPG2_TOUT0	Base timer 4 output pin	144, 163, 203, 207	45, 150, 171, 211, 215	
PPG2_TOUT2	Base timer 5 output pin	44, 147, 164, 174	46, 153, 172, 182	
PPG3_TOUT0	Base timer 6 output pin	45, 89, 148, 165, 175	47, 91, 154, 173, 183	
PPG3_TOUT2	Base timer 7 output pin	32, 46, 149, 166, 176	32, 48, 155, 174, 184	
PPG4_TOUT0	Base timer 8 output pin	33, 47, 150, 167, 177	33, 49, 92, 156, 175, 185	
PPG4_TOUT2	Base timer 9 output pin	48, 84, 90, 151, 168, 178	50, 86, 93, 157, 176, 186	
PPG5_TOUT0	Base timer 10 output pin	49, 91, 118, 152, 179	51, 94, 122, 158, 187	
PPG5_TOUT2	Base timer 11 output pin	50, 72, 92, 153, 180	52, 74, 95, 123, 159, 188	
PPG6_TOUT0	Base timer 12 output pin	51, 75, 154, 181	53, 77, 96, 124, 160, 189	
PPG6_TOUT2	Base timer 13 output pin	54, 77, 93, 127, 186	56, 79, 97, 133, 194	
PPG7_TOUT0	Base timer 14 output pin	55, 76, 94, 128, 187	57, 78, 98, 134, 195	
PPG7_TOUT2	Base timer 15 output pin	56, 79, 95, 129, 188	58, 81, 99, 135, 196	
PPG8_TOUT0	Base timer 16 output pin	57, 78, 96, 130, 189	59, 80, 100, 136, 197	
PPG8_TOUT2	Base timer 17 output pin	58, 69, 97, 131, 190	60, 71, 101, 137, 198	
PPG9_TOUT0	Base timer 18 output pin	59, 66, 98, 132, 191	61, 68, 102, 138, 199	
PPG9_TOUT2	Base timer 19 output pin	31, 34, 68, 99, 133, 192	31, 34, 70, 103, 139, 200	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
PPG10_TOUT0	Base timer 20 output pin	35, 60, 67, 100, 134, 193	35, 62, 69, 104, 140, 201	
PPG10_TOUT2	Base timer 21 output pin	36, 70, 101, 137, 196	36, 72, 105, 143, 204	
PPG11_TOUT0	Base timer 22 output pin	37, 63, 102, 138, 197	37, 65, 106, 144, 205	
PPG11_TOUT2	Base timer 23 output pin	38, 139, 160, 198	38, 145, 166, 206	
PPG0/1/2/3/4/5_TIN1	Base timer 0/2/4/6/8/10 input pin	-	96	
PPG6/7/8/9/10/11_TIN1	Base timer 12/14/16/18/20/22 input pin	161	167	
WOT	RTC overflow output pin	161	167	
PWM1M0	SMC ch.0 output pin	128	134	
PWM1M1	SMC ch.1 output pin	132	138	
PWM1M2	SMC ch.2 output pin	138	144	
PWM1M3	SMC ch.3 output pin	142	148	
PWM1M4	SMC ch.4 output pin	148	154	
PWM1M5	SMC ch.5 output pin	152	158	
PWM1P0	SMC ch.0 output pin	127	133	
PWM1P1	SMC ch.1 output pin	131	137	
PWM1P2	SMC ch.2 output pin	137	143	
PWM1P3	SMC ch.3 output pin	141	147	
PWM1P4	SMC ch.4 output pin	147	153	
PWM1P5	SMC ch.5 output pin	151	157	
PWM2M0	SMC ch.0 output pin	130	136	
PWM2M1	SMC ch.1 output pin	134	140	
PWM2M2	SMC ch.2 output pin	140	146	
PWM2M3	SMC ch.3 output pin	144	150	
PWM2M4	SMC ch.4 output pin	150	156	
PWM2M5	SMC ch.5 output pin	154	160	
PWM2P0	SMC ch.0 output pin	129	135	
PWM2P1	SMC ch.1 output pin	133	139	
PWM2P2	SMC ch.2 output pin	139	145	
PWM2P3	SMC ch.3 output pin	143	149	
PWM2P4	SMC ch.4 output pin	149	155	
PWM2P5	SMC ch.5 output pin	153	159	
OCU0_OTD0	Output compare 0 ch.0 output pin	39, 140, 161, 170, 199	39, 146, 167, 178, 207	
OCU0_OTD1	Output compare 0 ch.1 output pin	40, 141, 162, 169, 200, 204	40, 147, 168, 177, 208, 212	
OCU1_OTD0	Output compare 1 ch.0 output pin	41, 142, 201, 205	41, 148, 169, 209, 213	
OCU1_OTD1	Output compare 1 ch.1 output pin	143, 202, 206	44, 149, 170, 210, 214	
OCU2_OTD0	Output compare 2 ch.0 output pin	144, 163, 203, 207	45, 150, 171, 211, 215	
OCU2_OTD1	Output compare 2 ch.1 output pin	44, 147, 164, 174	46, 153, 172, 182	
OCU3_OTD0	Output compare 3 ch.0 output pin	45, 89, 148, 165, 175	47, 91, 154, 173, 183	
OCU3_OTD1	Output compare 3 ch.1 output pin	32, 46, 149, 166, 176	32, 48, 155, 174, 184	
OCU4_OTD0	Output compare 4 ch.0 output pin	33, 47, 150, 167, 177	33, 49, 92, 156, 175, 185	
OCU4_OTD1	Output compare 4 ch.1 output pin	48, 84, 90, 151, 168, 178	50, 86, 93, 157, 176, 186	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
OCU5_OTD0	Output compare 5 ch.0 output pin	49, 91, 118, 152, 179	51, 94, 122, 158, 187	
OCU5_OTD1	Output compare 5 ch.1 output pin	50, 72, 92, 153, 180	52, 74, 95, 123, 159, 188	
OCU6_OTD0	Output compare 6 ch.0 output pin	51, 75, 154, 181	53, 77, 96, 124, 160, 189	
OCU6_OTD1	Output compare 6 ch.1 output pin	54, 77, 93, 127, 186	56, 79, 97, 133, 194	
OCU7_OTD0	Output compare 7 ch.0 output pin	55, 76, 94, 128, 187	57, 78, 98, 134, 195	
OCU7_OTD1	Output compare 7 ch.1 output pin	56, 79, 95, 129, 188	58, 81, 99, 135, 196	
OCU8_OTD0	Output compare 8 ch.0 output pin	57, 78, 96, 130, 189	59, 80, 100, 136, 197	
OCU8_OTD1	Output compare 8 ch.1 output pin	58, 69, 97, 131, 190	60, 71, 101, 137, 198	
OCU9_OTD0	Output compare 9 ch.0 output pin	59, 66, 98, 132, 191	61, 68, 102, 138, 199	
OCU9_OTD1	Output compare 9 ch.1 output pin	31, 34, 68, 99, 133, 192	31, 34, 70, 103, 139, 200	
OCU10_OTD0	Output compare 10 ch.0 output pin	35, 60, 67, 100, 134, 193	35, 62, 69, 104, 140, 201	
OCU10_OTD1	Output compare 10 ch.1 output pin	36, 70, 101, 137, 196	36, 72, 105, 143, 204	
OCU11_OTD0	Output compare 11 ch.0 output pin	37, 63, 102, 138, 197	37, 65, 106, 144, 205	
OCU11_OTD1	Output compare 11 ch.1 output pin	38, 139, 160, 198	38, 145, 166, 206	
ICU0_IN0	Input Capture 0 ch.0 input pin	39, 140, 161, 170, 199	39, 146, 167, 178, 207	
ICU0_IN1	Input Capture 0 ch.1 input pin	40, 141, 162, 169, 200, 204	40, 147, 168, 177, 208, 212	
ICU1_IN0	Input Capture 1 ch.0 input pin	41, 142, 201, 205	41, 148, 169, 209, 213	
ICU1_IN1	Input Capture 1 ch.1 input pin	143, 159, 202, 206	44, 149, 165, 170, 210, 214	
ICU2_IN0	Input Capture 2 ch.0 input pin	144, 163, 203, 207	45, 150, 171, 211, 215	
ICU2_IN1	Input Capture 2 ch.1 input pin	44, 147, 164, 174	46, 153, 172, 182	
ICU3_IN0	Input Capture 3 ch.0 input pin	45, 89, 148, 165, 175	47, 91, 154, 173, 183	
ICU3_IN1	Input Capture 3 ch.1 input pin	32, 46, 149, 166, 176	32, 48, 155, 174, 184	
ICU4_IN0	Input Capture 4 ch.0 input pin	33, 47, 150, 167, 177	33, 49, 92, 156, 175, 185	
ICU4_IN1	Input Capture 4 ch.1 input pin	48, 84, 90, 151, 168, 178	50, 86, 93, 157, 176, 186	
ICU5_IN0	Input Capture 5 ch.0 input pin	49, 91, 118, 152, 179	51, 94, 122, 158, 187	
ICU5_IN1	Input Capture 5 ch.1 input pin	50, 72, 92, 153, 180	52, 74, 95, 123, 159, 188	
ICU6_IN0	Input Capture 6 ch.0 input pin	51, 75, 154, 181	53, 77, 96, 124, 160, 189	
ICU6_IN1	Input Capture 6 ch.1 input pin	54, 77, 93, 127, 186	56, 79, 97, 133, 194	
ICU7_IN0	Input Capture 7 ch.0 input pin	55, 76, 94, 128, 187	57, 78, 98, 134, 195	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
ICU7_IN1	Input Capture 7 ch.1 input pin	56, 79, 95, 129, 188	58, 81, 99, 135, 196	
ICU8_IN0	Input Capture 8 ch.0 input pin	57, 78, 96, 130, 189	59, 80, 100, 136, 197	
ICU8_IN1	Input Capture 8 ch.1 input pin	58, 69, 97, 131, 190	60, 71, 101, 137, 198	
ICU9_IN0	Input Capture 9 ch.0 input pin	59, 66, 98, 132, 191	61, 68, 102, 138, 199	
ICU9_IN1	Input Capture 9 ch.1 input pin	31, 34, 68, 99, 133, 192	31, 34, 70, 103, 139, 200	
ICU10_IN0	Input Capture 10 ch.0 input pin	35, 60, 67, 100, 134, 193	35, 62, 69, 104, 140, 201	
ICU10_IN1	Input Capture 10 ch.1 input pin	36, 70, 101, 137, 196	36, 72, 105, 143, 204	
ICU11_IN0	Input Capture 11 ch.0 input pin	37, 63, 102, 138, 197	37, 65, 106, 144, 205	
ICU11_IN1	Input Capture 11 ch.1 input pin	38, 139, 160, 198	38, 145, 166, 206	
SGA0	Sound generator ch.0 SGA output pin	90, 97, 164	93, 101, 172	
SGA1	Sound generator ch.1 SGA output pin	91, 98, 165, 205	94, 102, 173, 213	
SGA2	Sound generator ch.2 SGA output pin	100, 167	96, 104, 175	
SGA3	Sound generator ch.3 SGA output pin	94, 118, 175	98, 122, 183	
SGO0	Sound generator ch.0 SGO output pin	96, 163	92, 100, 171	
SGO1	Sound generator ch.1 SGO output pin	92, 99, 166, 206	95, 103, 174, 214	
SGO2	Sound generator ch.2 SGO output pin	93, 101, 168	97, 105, 176	
SGO3	Sound generator ch.3 SGO output pin	95, 176	99, 123, 184	
AN0(AL0)	PCM PWM ch.0 output pin	128, 175	134, 183	
AN1(AL1)	PCM PWM ch.1 output pin	132, 179	138, 187	
AP0(AH0)	PCM PWM ch.0 output pin	127, 174	133, 182	
AP1(AH1)	PCM PWM ch.1 output pin	131, 178	137, 186	
BN0(BL0)	PCM PWM ch.0 output pin	130, 177	136, 185	
BN1(BL1)	PCM PWM ch.1 output pin	134, 181	140, 189	
BP0(BH0)	PCM PWM ch.0 output pin	129, 176	135, 184	
BP1(BH1)	PCM PWM ch.1 output pin	133, 180	139, 188	
I2S0_ECLK	I2S external clock ch.0 input pin	50	52	
I2S1_ECLK	I2S external clock ch.1 input pin	56	58	
I2S0_SCK	I2S continuous serial clock ch.0 pin	55	57	
I2S1_SCK	I2S continuous serial clock ch.1 pin	59	61	
I2S0_SD	I2S serial data ch.0 pin	51	53	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
I2S1_SD	I2S serial data ch.1 pin	57	59	
I2S0_WS	I2S word select ch.0 pin	54	56	
I2S1_WS	I2S word select ch.1 pin	58	60	
C_L	Audio DAC external capacity connection output pin (L)	8	8	Not available on S6J32EEx, leave open
C_R	Audio DAC external capacity connection output pin (R)	4	4	
DAC_L	Audio DAC output pin (L)	7	7	
DAC_R	Audio DAC output pin (R)	3	3	
FRT0/1/2/3_TEXT	Free-run timer ch.0/1/2/3 clock input pin	160	166	
FRT4/5/6/7_TEXT	Free-run timer ch.4/5/6/7 clock input pin	166	174	
FRT8/9/10/11_TEXT	Free-run timer ch.4/5/6/7 clock input pin	95	99	
TIN0	Reload timer ch.0 event input pin	35	35, 96	
TIN1	Reload timer ch.1 event input pin	37, 93	37, 97	
TIN2	Reload timer ch.2 event input pin	39, 94	39, 98	
TIN3	Reload timer ch.3 event input pin	41, 95	41, 99	
TIN16	Reload timer ch.16 event input pin	100	45, 104	
TIN17	Reload timer ch.17 event input pin	45, 102	47, 106	
TIN18	Reload timer ch.18 event input pin	47, 162	49, 168	
TIN19	Reload timer ch.19 event input pin	49	51, 170	
TIN32	Reload timer ch.32 event input pin	51, 164	53, 172	
TIN33	Reload timer ch.33 event input pin	55, 166	57, 174	
TIN34	Reload timer ch.34 event input pin	57, 168	59, 176	
TIN35	Reload timer ch.35 event input pin	59	61, 123	
TIN48	Reload timer ch.48 event input pin	159	165	
TIN49	Reload timer ch.49 event input pin	89	91	
TOT0	Reload timer ch.0 output pin	34, 96	34, 100	
TOT1	Reload timer ch.1 output pin	36, 97	36, 101	
TOT2	Reload timer ch.2 output pin	38, 98	38, 102	
TOT3	Reload timer ch.3 output pin	40, 99	40, 103	
TOT16	Reload timer ch.16 output pin	101	44, 105	
TOT17	Reload timer ch.17 output pin	44, 160	46, 166	
TOT18	Reload timer ch.18 output pin	46, 161	48, 167	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
TOT19	Reload timer ch.19 output pin	48	50, 169	
TOT32	Reload timer ch.32 output pin	50, 163	52, 171	
TOT33	Reload timer ch.33 output pin	54, 165	56, 173	
TOT34	Reload timer ch.34 output pin	56, 167	58, 175	
TOT35	Reload timer ch.35 output pin	58, 118	60, 122	
AIN8	Up/Down counter AIN input pin ch.8	190	92, 198	
AIN9	Up/Down counter AIN input pin ch.9	93, 193	97, 201	
BIN8	Up/Down counter BIN input pin ch.8	90, 191	93, 199	
BIN9	Up/Down counter BIN input pin ch.9	94, 196	98, 204	
ZIN8	Up/Down counter ZIN input pin ch.8	91, 192	94, 200	
ZIN9	Up/Down counter ZIN input pin ch.9	95, 197	99, 205	
RMII_RXERR	Ethernet pin	35	35	
RMII_REFCLK	Ethernet pin	36	36	
RMII_RX0	Ethernet pin	37	37	
RMII_RX1	Ethernet pin	38	38	
RMII_TXD0	Ethernet pin	39	39	
RMII_TXD1	Ethernet pin	40	40	
RXD0	Ethernet pin	48	50	
RXD1	Ethernet pin	49	51	
RXD2	Ethernet pin	50	52	
RXD3	Ethernet pin	51	53	
TXD0	Ethernet pin	44	46	
TXD1	Ethernet pin	45	47	
TXD2	Ethernet pin	46	48	
TXD3	Ethernet pin	47	49	
RXER	Ethernet pin	56	58	
RXDV	Ethernet pin	34, 57	34, 59	Pin 34 is not supported on revision M
RXCLK	Ethernet pin	55	57	
TXER	Ethernet pin	60	62	
TXEN	Ethernet pin	41	41	
TXCLK	Ethernet pin	54	56	
MDC	Ethernet pin	31	31	
MDIO	Ethernet pin	32	32	
MLBCLK	MediaLB pin	84	86	
MLBDAT	MediaLB pin	82	84	
MLBSIG	MediaLB pin	83	85	
TxCLK-	LVDS clock output pin	21	21	Described as TXOUT4M in FPD-Link Converter
TxCLK+	LVDS clock output pin	20	20	Described as TXOUT4P in FPD-Link Converter

Port Name	Description	TEQFP-208	TEQFP-216	Remark
TxDOUT0-	LVDS data output pin	25	25	Described as TXOUT0M in FPD-Link Converter
TxDOUT0+	LVDS data output pin	24	24	Described as TXOUT0P in FPD-Link Converter
TxDOUT1-	LVDS data output pin	23	23	Described as TXOUT1M in FPD-Link Converter
TxDOUT1+	LVDS data output pin	22	22	Described as TXOUT1P in FPD-Link Converter
TxDOUT2-	LVDS data output pin	19	19	Described as TXOUT2M in FPD-Link Converter
TxDOUT2+	LVDS data output pin	18	18	Described as TXOUT2P in FPD-Link Converter
TxDOUT3-	LVDS data output pin	17	17	Described as TXOUT3M in FPD-Link Converter
TxDOUT3+	LVDS data output pin	16	16	Described as TXOUT3P in FPD-Link Converter
G_SCLK0	Graphic HS-SPI clock output pin	72	74	
G_SDATA0_0	Graphic HS-SPI0 data 0 pin	75	77	
G_SDATA0_1	Graphic HS-SPI0 data 1 pin	77	79	
G_SDATA0_2	Graphic HS-SPI0 data 2 pin	76	78	
G_SDATA0_3	Graphic HS-SPI0 data 3 pin	79	81	
G_SDATA1_0	Graphic HS-SPI1 data 0 pin	66	68	
G_SDATA1_1	Graphic HS-SPI1 data 1 pin	68	70	
G_SDATA1_2	Graphic HS-SPI1 data 2 pin	67	69	
G_SDATA1_3	Graphic HS-SPI1 data 3 pin	70	72	
G_SSEL0	Graphic HS-SPI select 0 output pin	78	80	
G_SSEL1	Graphic HS-SPI select 1 output pin	69	71	
G_CK_1	Hyper Bus 1 clock output pin	63	65	
G_CS#1_1	Hyper Bus 1 select 1 output pin	70	72	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
G_CS#2_1	Hyper Bus 1 select 2 output pin	75	77	
G_DQ0_1	Hyper Bus 1 Data 0 pin	69	71	
G_DQ1_1	Hyper Bus 1 Data 1 pin	68	70	
G_DQ2_1	Hyper Bus 1 Data 2 pin	67	69	
G_DQ3_1	Hyper Bus 1 Data 3 pin	66	68	
G_DQ4_1	Hyper Bus 1 Data 4 pin	76	78	
G_DQ5_1	Hyper Bus 1 Data 5 pin	77	79	
G_DQ6_1	Hyper Bus 1 Data 6 pin	78	80	
G_DQ7_1	Hyper Bus 1 Data 7 pin	79	81	
G_RWDS_1	Hyper Bus 1 RWDS pin #699	72	74	
G_CK_2	Hyper Bus 2 clock output pin	44	46	Not available on S6J32EE, S6J32FE
G_CS#1_2	Hyper Bus 2 select 1 output pin	49	51	
G_CS#2_2	Hyper Bus 2 select 2 output pin	51	53	
G_DQ0_2	Hyper Bus 2 Data 0 pin	48	50	
G_DQ1_2	Hyper Bus 2 Data 1 pin	47	49	
G_DQ2_2	Hyper Bus 2 Data 2 pin	46	48	
G_DQ3_2	Hyper Bus 2 Data 3 pin	45	47	
G_DQ4_2	Hyper Bus 2 Data 4 pin	54	56	
G_DQ5_2	Hyper Bus 2 Data 5 pin	55	57	
G_DQ6_2	Hyper Bus 2 Data 6 pin	56	58	
G_DQ7_2	Hyper Bus 2 Data 7 pin	57	59	
G_RWDS_2	Hyper Bus 2 RWDS pin	50	52	
M_SCLK0	MCU HS-SPI clock output pin	63	65	
M_SDATA0_0	MCU HS-SPI0 data 0 pin	66	68	
M_SDATA0_1	MCU HS-SPI0 data 1 pin	68	70	
M_SDATA0_2	MCU HS-SPI0 data 2 pin	67	69	
M_SDATA0_3	MCU HS-SPI0 data 3 pin	70	72	
M_SDATA1_0	MCU HS-SPI1 data 0 pin	75	77	
M_SDATA1_1	MCU HS-SPI1 data 1 pin	77	79	
M_SDATA1_2	MCU HS-SPI1 data 2 pin	76	78	
M_SDATA1_3	MCU HS-SPI1 data 3 pin	79	81	
M_SSEL0	MCU HS-SPI select 0 output pin	69	71	
M_SSEL1	MCU HS-SPI select 1 output pin	78	80	
M_CK_0	MCU Hyper Bus clock output pin	63	65	
M_CS#1_0	MCU Hyper Bus select 1 output pin	70	72	
M_CS#2_0	MCU Hyper Bus select 2 output pin	75	77	
M_DQ0_0	MCU Hyper Bus Data 0 pin	69	71	
M_DQ1_0	MCU Hyper Bus Data 1 pin	68	70	
M_DQ2_0	MCU Hyper Bus Data 2 pin	67	69	
M_DQ3_0	MCU Hyper Bus Data 3 pin	66	68	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
M_DQ4_0	MCU Hyper Bus Data 4 pin	76	78	
M_DQ5_0	MCU Hyper Bus Data 5 pin	77	79	
M_DQ6_0	MCU Hyper Bus Data 6 pin	78	80	
M_DQ7_0	MCU Hyper Bus Data 7 pin	79	81	
M_RWDS_0	MCU Hyper Bus RWDS pin #699	72	74	
DSP0_CLK	Display 0 Clock output pin	32, 58	32, 60	
DSP0_CLK-	Display 0 RSDS Clock output pin	33	33	
DSP0_CLK+	Display 0 RSDS Clock output pin	32	32	
DSP0_CTRL0	Display 0 Control output pin	59, 60, 196	61, 62, 204	
DSP0_CTRL1	Display 0 Control output pin	31, 60, 197	31, 62, 205	
DSP0_CTRL2	Display 0 Control output pin	33, 57, 60, 82, 198	33, 59, 62, 84, 206	
DSP0_CTRL3	Display 0 Control output pin	83, 199	85, 207	
DSP0_CTRL4	Display 0 Control output pin	84, 200	86, 208	
DSP0_CTRL5	Display 0 Control output pin	201	209	
DSP0_CTRL6	Display 0 Control output pin	202	210	
DSP0_CTRL7	Display 0 Control output pin	203	211	
DSP0_CTRL8	Display 0 Control output pin	204	212	
DSP0_CTRL9	Display 0 Control output pin	205	213	
DSP0_CTRL10	Display 0 Control output pin	206	214	
DSP0_CTRL11	Display 0 Control output pin	207	215	
DSP0_DATA0_0	Display 0 Data output pin	34	34	
DSP0_DATA0_1	Display 0 Data output pin	36	36	
DSP0_DATA0_2	Display 0 Data output pin	38	38	
DSP0_DATA0_3	Display 0 Data output pin	40	40	
DSP0_DATA0_4	Display 0 Data output pin	31	31, 44	
DSP0_DATA0_5	Display 0 Data output pin	44	46	
DSP0_DATA0_6	Display 0 Data output pin	46	48	
DSP0_DATA0_7	Display 0 Data output pin	48	50	
DSP0_DATA0_8	Display 0 Data output pin	50	52	
DSP0_DATA0_9	Display 0 Data output pin	54	56	
DSP0_DATA0_10	Display 0 Data output pin	56	58	
DSP0_DATA0_11	Display 0 Data output pin	32, 58	32, 60	
DSP0_DATA1_0	Display 0 Data output pin	35	35	
DSP0_DATA1_1	Display 0 Data output pin	37	37	
DSP0_DATA1_2	Display 0 Data output pin	39	39	
DSP0_DATA1_3	Display 0 Data output pin	41	41	
DSP0_DATA1_4	Display 0 Data output pin	33	33, 45	
DSP0_DATA1_5	Display 0 Data output pin	45	47	
DSP0_DATA1_6	Display 0 Data output pin	47	49	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
DSP0_DATA1_7	Display 0 Data output pin	49	51	
DSP0_DATA1_8	Display 0 Data output pin	51	53	
DSP0_DATA1_9	Display 0 Data output pin	55	57	
DSP0_DATA1_10	Display 0 Data output pin	31, 57	31, 59	
DSP0_DATA1_11	Display 0 Data output pin	33, 59	33, 61	
DSP0_DATA_D0-	Display 0 RSDS Data output pin	35	35	
DSP0_DATA_D0+	Display 0 RSDS Data output pin	34	34	
DSP0_DATA_D1-	Display 0 RSDS Data output pin	37	37	
DSP0_DATA_D1+	Display 0 RSDS Data output pin	36	36	
DSP0_DATA_D2-	Display 0 RSDS Data output pin	39	39	
DSP0_DATA_D2+	Display 0 RSDS Data output pin	38	38	
DSP0_DATA_D3-	Display 0 RSDS Data output pin	41	41	
DSP0_DATA_D3+	Display 0 RSDS Data output pin	40	40	
DSP0_DATA_D4-	Display 0 RSDS Data output pin	-	45	
DSP0_DATA_D4+	Display 0 RSDS Data output pin	-	44	
DSP0_DATA_D5-	Display 0 RSDS Data output pin	45	47	
DSP0_DATA_D5+	Display 0 RSDS Data output pin	44	46	
DSP0_DATA_D6-	Display 0 RSDS Data output pin	47	49	
DSP0_DATA_D6+	Display 0 RSDS Data output pin	46	48	
DSP0_DATA_D7-	Display 0 RSDS Data output pin	49	51	
DSP0_DATA_D7+	Display 0 RSDS Data output pin	48	50	
DSP0_DATA_D8-	Display 0 RSDS Data output pin	51	53	
DSP0_DATA_D8+	Display 0 RSDS Data output pin	50	52	
DSP0_DATA_D9-	Display 0 RSDS Data output pin	55	57	
DSP0_DATA_D9+	Display 0 RSDS Data output pin	54	56	
DSP0_DATA_D10-	Display 0 RSDS Data output pin	57	59	
DSP0_DATA_D10+	Display 0 RSDS Data output pin	56	58	
DSP0_DATA_D11-	Display 0 RSDS Data output pin	59	61	
DSP0_DATA_D11+	Display 0 RSDS Data output pin	58	60	
DSP1_CLK	Display 1 Clock output pin	199, 204	207, 212	
DSP1_CTRL0	Display 1 Control output pin	200, 207	208, 215	
DSP1_CTRL1	Display 1 Control output pin	201, 206	209, 214	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
DSP1_CTRL2	Display 1 Control output pin	198, 205	206, 213	
DSP1_DATA0_0	Display 1 Data output pin	203	211	
DSP1_DATA0_1	Display 1 Data output pin	201	209	
DSP1_DATA0_2	Display 1 Data output pin	199	207	
DSP1_DATA0_3	Display 1 Data output pin	197	205	
DSP1_DATA0_4	Display 1 Data output pin	193	201	
DSP1_DATA0_5	Display 1 Data output pin	191	199	
DSP1_DATA0_6	Display 1 Data output pin	189	197	
DSP1_DATA0_7	Display 1 Data output pin	187	195	
DSP1_DATA0_8	Display 1 Data output pin	181	189	
DSP1_DATA0_9	Display 1 Data output pin	179	187	
DSP1_DATA0_10	Display 1 Data output pin	177	185	
DSP1_DATA0_11	Display 1 Data output pin	175	183	
DSP1_DATA1_0	Display 1 Data output pin	202	210	
DSP1_DATA1_1	Display 1 Data output pin	200	208	
DSP1_DATA1_2	Display 1 Data output pin	198	206	
DSP1_DATA1_3	Display 1 Data output pin	196	204	
DSP1_DATA1_4	Display 1 Data output pin	192	200	
DSP1_DATA1_5	Display 1 Data output pin	190	198	
DSP1_DATA1_6	Display 1 Data output pin	188	196	
DSP1_DATA1_7	Display 1 Data output pin	186	194	
DSP1_DATA1_8	Display 1 Data output pin	180	188	
DSP1_DATA1_9	Display 1 Data output pin	178	186	
DSP1_DATA1_10	Display 1 Data output pin	176	184	
DSP1_DATA1_11	Display 1 Data output pin	174	182	
CAP0_CLK	Video Capture 0 Clock input pin	59	61	
CAP0_DATA0	Video Capture 0 Data input pin	31	31	
CAP0_DATA1	Video Capture 0 Data input pin	32	32	
CAP0_DATA2	Video Capture 0 Data input pin	33	33	
CAP0_DATA3	Video Capture 0 Data input pin	34	34	
CAP0_DATA4	Video Capture 0 Data input pin	35	35	
CAP0_DATA5	Video Capture 0 Data input pin	36	36	
CAP0_DATA6	Video Capture 0 Data input pin	37	37	
CAP0_DATA7	Video Capture 0 Data input pin	38	38	
CAP0_DATA8	Video Capture 0 Data input pin	39	39	
CAP0_DATA9	Video Capture 0 Data input pin	40	40	
CAP0_DATA10	Video Capture 0 Data input pin	41	41	
CAP0_DATA11	Video Capture 0 Data input pin	44	44, 46	
CAP0_DATA12	Video Capture 0 Data input pin	45	45, 47	
CAP0_DATA13	Video Capture 0 Data input pin	44, 46	46, 48	
CAP0_DATA14	Video Capture 0 Data input pin	45, 47	47, 49	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
CAP0_DATA15	Video Capture 0 Data input pin	46, 48	48, 50	
CAP0_DATA16	Video Capture 0 Data input pin	47	49	
CAP0_DATA17	Video Capture 0 Data input pin	48	50	
CAP0_DATA18	Video Capture 0 Data input pin	49	51	
CAP0_DATA19	Video Capture 0 Data input pin	50	52	
CAP0_DATA20	Video Capture 0 Data input pin	51	53	
CAP0_DATA21	Video Capture 0 Data input pin	54	56	
CAP0_DATA22	Video Capture 0 Data input pin	55	57	
CAP0_DATA23	Video Capture 0 Data input pin	56	58	
CAP0_DATA24	Video Capture 0 Data input pin	82	84	
CAP0_DATA25	Video Capture 0 Data input pin	83	85	
CAP0_DATA32	Video Capture 0 Data input pin	56, 57	58, 59	
CAP0_DATA33	Video Capture 0 Data input pin	58	60	
CAP0_DATA34	Video Capture 0 Data input pin	60	62	
CAP0_DATA35	Video Capture 0 Data input pin	57	59	
INDICATOR0_0	Indicator PWM output pin 0 (It can also be obtained from INDICATOR0_1)	92	95	
INDICATOR0_1	Indicator PWM output pin 1 (It can also be obtained from INDICATOR0_0)	170	178	
P0_00	GPIO port	40	40	
P0_01	GPIO port	41	41	
P0_02	GPIO port	-	44	
P0_03	GPIO port	-	45	
P0_04	GPIO port	44	46	
P0_05	GPIO port	45	47	
P0_06	GPIO port	46	48	
P0_07	GPIO port	47	49	
P0_08	GPIO port	48	50	
P0_09	GPIO port	49	51	
P0_10	GPIO port	50	52	
P0_11	GPIO port	51	53	
P0_12	GPIO port	54	56	
P0_13	GPIO port	55	57	
P0_14	GPIO port	56	58	
P0_15	GPIO port	57	59	
P0_16	GPIO port	58	60	
P0_17	GPIO port	59	61	
P0_18	GPIO port	32	32	
P0_19	GPIO port	33	33	
P0_26	GPIO port	82	84	
P0_27	GPIO port	83	85	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
P0_28	GPIO port	84	86	
P0_30	GPIO port	72	74	
P0_31	GPIO port	75	77	
P1_00	GPIO port	77	79	
P1_01	GPIO port	76	78	
P1_02	GPIO port	79	81	
P1_03	GPIO port	78	80	
P1_04	GPIO port	69	71	
P1_05	GPIO port	66	68	
P1_06	GPIO port	68	70	
P1_07	GPIO port	67	69	
P1_08	GPIO port	70	72	
P1_09	GPIO port	63	65	
P2_16	GPIO port	170	178	
P2_17	GPIO port	169	177	
P2_19	GPIO port	159	165	
P2_22	GPIO port	89	91	
P2_24	GPIO port	-	92	
P2_25	GPIO port	90	93	
P2_26	GPIO port	91	94	
P2_27	GPIO port	92	95	
P2_28	GPIO port	-	96	
P2_29	GPIO port	93	97	
P2_30	GPIO port	94	98	
P2_31	GPIO port	95	99	
P3_00	GPIO port	96	100	
P3_01	GPIO port	97	101	
P3_02	GPIO port	98	102	
P3_03	GPIO port	99	103	
P3_04	GPIO port	100	104	
P3_05	GPIO port	101	105	
P3_06	GPIO port	102	106	
P3_07	GPIO port	160	166	
P3_08	GPIO port	161	167	
P3_09	GPIO port	162	168	
P3_10	GPIO port	-	169	
P3_11	GPIO port	-	170	
P3_12	GPIO port	163	171	
P3_13	GPIO port	164	172	
P3_14	GPIO port	165	173	
P3_15	GPIO port	166	174	
P3_16	GPIO port	167	175	
P3_17	GPIO port	168	176	
P3_18	GPIO port	118	122	
P3_19	GPIO port	-	123	
P3_20	GPIO port	-	124	
P3_21	GPIO port	127	133	
P3_22	GPIO port	128	134	
P3_23	GPIO port	129	135	
P3_24	GPIO port	130	136	
P3_25	GPIO port	131	137	
P3_26	GPIO port	132	138	
P3_27	GPIO port	133	139	
P3_28	GPIO port	134	140	
P3_29	GPIO port	137	143	
P3_30	GPIO port	138	144	
P3_31	GPIO port	139	145	
P4_00	GPIO port	140	146	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
P4_01	GPIO port	141	147	
P4_02	GPIO port	142	148	
P4_03	GPIO port	143	149	
P4_04	GPIO port	144	150	
P4_05	GPIO port	147	153	
P4_06	GPIO port	148	154	
P4_07	GPIO port	149	155	
P4_08	GPIO port	150	156	
P4_09	GPIO port	151	157	
P4_10	GPIO port	152	158	
P4_11	GPIO port	153	159	
P4_12	GPIO port	154	160	
P4_25	GPIO port	204	212	
P4_26	GPIO port	205	213	
P4_27	GPIO port	206	214	
P4_28	GPIO port	207	215	
P4_29	GPIO port	174	182	
P4_30	GPIO port	175	183	
P4_31	GPIO port	176	184	
P5_00	GPIO port	177	185	
P5_01	GPIO port	178	186	
P5_02	GPIO port	179	187	
P5_03	GPIO port	180	188	
P5_04	GPIO port	181	189	
P5_05	GPIO port	186	194	
P5_06	GPIO port	187	195	
P5_07	GPIO port	188	196	
P5_08	GPIO port	189	197	
P5_09	GPIO port	190	198	
P5_10	GPIO port	191	199	
P5_11	GPIO port	192	200	
P5_12	GPIO port	193	201	
P5_13	GPIO port	196	204	
P5_14	GPIO port	197	205	
P5_15	GPIO port	198	206	
P5_16	GPIO port	199	207	
P5_17	GPIO port	200	208	
P5_18	GPIO port	201	209	
P5_19	GPIO port	202	210	
P5_20	GPIO port	203	211	
P5_21	GPIO port	31	31	
P5_22	GPIO port	60	62	
P5_27	GPIO port	34	34	
P5_28	GPIO port	35	35	
P5_29	GPIO port	36	36	
P5_30	GPIO port	37	37	
P5_31	GPIO port	38	38	
P6_00	GPIO port	39	39	
P6_01	GPIO port	-	-	
P6_02	GPIO port	-	-	
P6_03	GPIO port	-	-	
P6_04	GPIO port	-	-	
P6_05	GPIO port	-	-	
P6_06	GPIO port	-	-	
P6_07	GPIO port	-	-	
P6_08	GPIO port	-	-	
P6_09	GPIO port	-	-	
P6_10	GPIO port	-	-	

Port Name	Description	TEQFP-208	TEQFP-216	Remark
P6_11	GPIO port	-	-	
P6_12	GPIO port	-	-	
P6_13	GPIO port	-	-	
P6_14	GPIO port	-	-	
P6_15	GPIO port	-	-	
P6_16	GPIO port	-	-	
P6_17	GPIO port	-	-	
P6_18	GPIO port	-	-	
P6_19	GPIO port	-	-	
P6_20	GPIO port	-	-	
P6_21	GPIO port	-	-	
P6_22	GPIO port	-	-	
P6_23	GPIO port	-	-	
P6_24	GPIO port	-	-	
P6_25	GPIO port	-	-	
P6_26	GPIO port	-	-	

6.2 Remarks

Notes:

- *The port description list shows the port function of the description, which is mounted and supported on the product. The function, which is not described in this table, is not supported and assured.*
- *Only the specified GPIOs can be used as inputs. Otherwise, undesired chip behavior can occur.*
- *See the function list of the product as well.*

7. Precautions and Handling Devices

7.1 Handling Precautions

All semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, and so on.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

7.1.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, and so on.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering applications outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

Follow these precautions when handling the pins, which connect semiconductor devices to power supply and input/output functions.

1. Preventing overvoltage and overcurrent conditions
   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases, leads to permanent damage of the device. Try to prevent such overvoltage or overcurrent conditions at the design stage.

2. Protection of Output Pins
   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present, for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins
   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

7.1.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

You can mount lead-insertion type packages on printed circuit boards by two methods: direct soldering on the board or mounting by using a socket.

Direct mounting on boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress-recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason, it is recommended that you verify the surface treatment of socket contacts and IC leads before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

Use appropriate mounting techniques. Cypress recommends the solder reflow method and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Pb-free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C. For dry packages, the recommended relative humidity range is 40% to 70%.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 ˚C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%.
   You may need to use an apparatus for ion generation to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by using rings or bracelets connected to the ground through high resistance (on the level of 1 MΩ). Wearing conductive clothing and shoes, use of conductive floor mats, and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.1.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity
   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity
   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil
   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation
   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame
   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Check the latest handling precautions at the following URL:
http://www.cypress.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf

7.2 Handling Devices

For Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC or lower than VSS; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Take care that analog power supplies (AVCC, AVRH) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.
The power-on sequence is as follows. Simultaneously, turn on the digital supply voltage (VCC) and analog supply voltages (AVCC, AVRH).

Handling Unused Pins

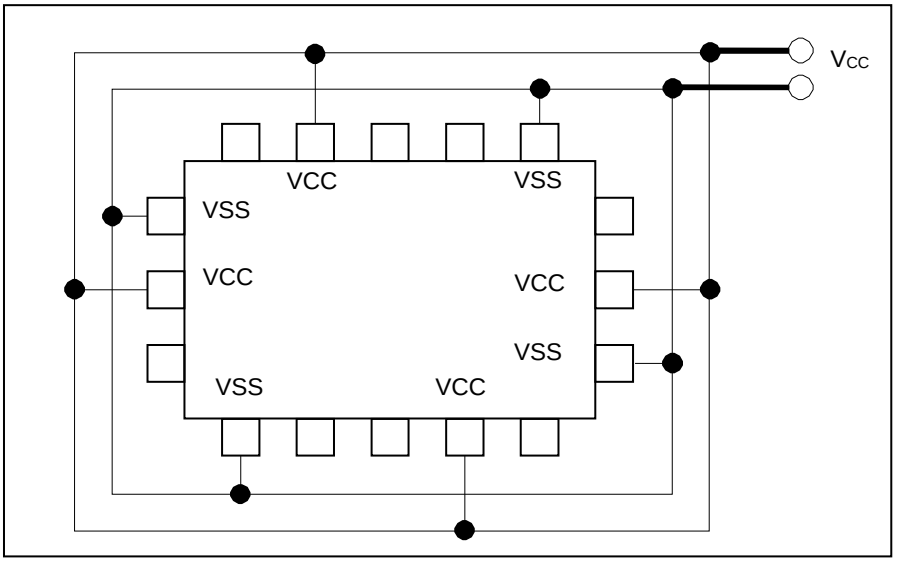
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kilo ohms or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current. Be sure to connect all the VCC and VSS pins to the power source and ground externally. Also, handle all the VSS power supply pins as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 7-1 Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

We recommend connecting a ceramic capacitor as a bypass capacitor between VCC and VSS, near this device.

Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

Mode Pin (MD)

Use mode pin MD by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that AVCC = AVRH = VCC and AVSS/AVRL5 = VSS.

Using External Clocks

External clocks are not supported.

External direct clock input cannot be used.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC) before the application of the power supplies (AVCC, AVRH, and AVRL5) and analog inputs (AN0 to AN63) of an A/D converter.
At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC). Perform these power-on and power-off operations without AVRH exceeding AVCC. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AVCC. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

Method to Switch off VCC12 during Power-off Sequence

During power-off sequence, it is necessary to switch off VCC12 by driving the PSC1 pin low by entering PSS mode (power domain 2 off). If VCC12 needs to be switched off by other means, RSTX needs to be asserted before switching off VCC12 to deactivate the operation of the VCC12 supplied domain below the operation assurance range.

C Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest datasheet.

Precautions on Designing a Mounting Substrate

Take measures against heat generation from the package for the mounting substrate to observe the absolute maximum rating (operating temperature). Design a mounting substrate with 4 or more layers. Connect the back of the package stage and the substrate pad with solder paste. Arrange thermal via holes on the substrate pad.

Writing to a Register Containing a Status Flag

In writing to a register containing a status flag (particularly an interrupt request flag) to control a function, it is important to take care not to accidentally clear the status flag.
Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value.
Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions have only 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

Note: Bit instructions take this point into account for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

8. Electrical Characteristics

8.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC5}	V_{SS}-0.3	V_{SS}+6.0	V	
	V_{CC53}	V_{SS}-0.3	V_{SS}+6.0	V	$V_{CC53} \leq V_{CC5}$
	V_{CC3}	V_{SS}-0.3	V_{SS}+4.0	V	$V_{CC3} \leq V_{CC5}$
	DV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	$DV_{CC} \leq V_{CC5}$
	V_{CC12}	V_{SS}-0.3	V_{SS}+1.8	V	$V_{CC12} \leq V_{CC53}$ $V_{CC12} \leq V_{CC3}$ $V_{CC12} \leq DV_{CC}$ $V_{CC12} \leq AV_{CC5}$
Analog supply voltage*1, *2	AV_{CC5}	V_{SS}-0.3	V_{SS}+6.0	V	$AV_{CC5} \leq V_{CC5}$
	AV_{CC3}_DAC	V_{SS}-0.3	V_{SS}+4.0	V	for DAC
	V_{CC3}_LVDS_Tx	V_{SS}-0.3	V_{SS}+4.0	V	for LVDS
	AV_{CC3}_LVDS_PLL	V_{SS}-0.3	V_{SS}+4.0	V	for LVDS PLL
Analog reference voltage*1	AVRH5	V_{SS}-0.3	V_{SS}+6.0	V	AVRH5 ≤ AV_{CC5}
Input voltage*1	V_{I1}	V_{SS}-0.3	V_{CC5}+0.3	V	5-V pins not shared SMC
	V_{I2}	V_{SS}-0.3	DV_{CC}+0.3	V	5-V pins shared SMC
	V_{I3}	V_{SS}-0.3	V_{CC3}+0.3	V	3-V pins
	V_{IE}	V_{SS}-0.3	V_{CC53}+0.3	V	5-V/3-V pins
Analog pin input voltage (Input voltage for pins shared with ADC) *1	V_{IA1}	V_{SS}-0.3	V_{CC5}+0.3, AV_{CC5}+0.3	V	5-V pins not shared SMC
	V_{IA2}	V_{SS}-0.3	DV_{CC5}+0.3, AV_{CC5}+0.3	V	5-V pins shared SMC
Output voltage*1	V_{O1}	V_{SS}-0.3	V_{CC5}+0.3	V	5-V pins not shared SMC*13
	V_{O2}	V_{SS}-0.3	DV_{CC}+0.3	V	5-V pins shared SMC*13
	V_{O3}	V_{SS}-0.3	V_{CC3}+0.3	V	3-V pins
	V_{O4}	V_{SS}-0.3	V_{CC53}+0.3	V	5-V/3-V pins
Maximum clamp current	$\|I_{CLAMP}\|$	-	4	mA	*12, *A
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	*12, *A
"L"-level maximum output current*3	I_{OL1}	-	3.5	mA	When setting is 1 mA*6, *7, *8
	I_{OL2}	-	7	mA	When setting is 2 mA*6, *7, *8, *9
	I_{OL3}	-	10	mA	When setting is 5 mA*6, *7, *8, *9
	I_{OL4}	-	16	mA	When setting is 10 mA*9
	I_{OL5}	-	30	mA	When setting is 20 mA*9
	I_{OL6}	-	40	mA	When setting is 30 mA*7
	I_{OL7}	-	8	mA	When setting is 3 mA *10
	I_{OL8}	-	11	mA	When setting is 6 mA *11

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"L"-level average output current[*4]	I_{OLAV1}	-	1	mA	When setting is 1 mA[*6, *7, *8]
	I_{OLAV2}	-	2	mA	When setting is 2 mA[*6, *7, *8, *9]
	I_{OLAV3}	-	5	mA	When setting is 5 mA[*6, *7, *8, *9]
	I_{OLAV4}	-	10	mA	When setting is 10 mA[*9]
	I_{OLAV5}	-	20	mA	When setting is 20 mA[*9]
	I_{OLAV6}	-	30	mA	When setting is 30 mA[*7]
	I_{OLAV7}	-	3	mA	When setting is 3 mA [*10]
	I_{OLAV8}	-	6	mA	When setting is 6 mA [*11]
"L"-level total output current[*5]	ΣI_{OL1}	-	50	mA	*6, *10
	ΣI_{OL2}	-	250	mA	*7
	ΣI_{OL3}	-	50	mA	*8
	ΣI_{OL4}	-	50	mA	*9, *11
"H"-level maximum output current[*3]	I_{OH1}	-	-3.5	mA	When setting is 1 mA[*6, *7, *8]
	I_{OH2}	-	-7	mA	When setting is 2 mA[*6, *7, *8, *9]
	I_{OH3}	-	-10	mA	When setting is 5 mA[*6, *7, *8, *9]
	I_{OH4}	-	-16	mA	When setting is 10 mA[*9]
	I_{OH5}	-	-30	mA	When setting is 20 mA[*9]
	I_{OH6}	-	-40	mA	When setting is 30mA[*7]
	I_{OH8}	-	-11	mA	When setting is 6 mA [*11]
"H"-level average output current[*4]	I_{OHAV1}	-	-1	mA	When setting is 1 mA[*6, *7, *8]
	I_{OHAV2}	-	-2	mA	When setting is 2 mA[*6, *7, *8, *9]
	I_{OHAV3}	-	-5	mA	When setting is 5 mA[*6, *7, *8, *9]
	I_{OHAV4}	-	-10	mA	When setting is 10 mA[*9]
	I_{OHAV5}	-	-20	mA	When setting is 20 mA[*9]
	I_{OHAV6}	-	-30	mA	When setting is 30 mA[*7]
	I_{OHAV8}	-	-6	mA	When setting is 6 mA [*11]
"H"-level total output current[*5]	ΣI_{OH1}	-	-50	mA	*6, *10
	ΣI_{OH2}	-	-250	mA	*7
	ΣI_{OH3}	-	-50	mA	*8
	ΣI_{OH4}	-	-50	mA	*9, *11
Power dissipation and operation temperature Case 1	P_D	-	3300	mW	-
	T_A	-40	+97	°C	Both should be satisfied.
	T_C	-40	+144	°C	
Power dissipation and operation temperature Case 2	P_D	-	3150	mW	-
	T_A	-40	+100	°C	Both should be satisfied.
	T_C	-40	+144	°C	
Power dissipation and operation temperature Case 3	P_D	-	3000	mW	-
	T_A	-40	+102	°C	Both should be satisfied.
	T_C	-40	+144	°C	
Power dissipation and operation temperature Case 4	P_D	-	2900	mW	-
	T_A	-40	+105	°C	Both should be satisfied.
	T_C	-40	+144	°C	
System Thermal Resistance	T_{JA}	-	16	°C/W	The minimum value depends on the system specification of heat radiation. The described value is estimated under the condition which is specified at Operation Assurance Condition.
Package Thermal Resistance	T_{JC}	-	7.5	°C/W	-
Storage temperature	Tstg	-55	+150	°C	-

*1: These parameters are based on the condition that VSS = AVSS = DVSS = 0.0 V.

*2: Take care that DVCC and AVCC5 do not exceed VCC5 at, for example, the power-on time. It is strongly recommended to set VCC5, DVCC, and AVCC5 to the same voltage during operation (see *13).

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Output of 5-V pins.

*7: Output of SMC pins.

*8: Output of 5-V/3-V pins.

*9: Output of 3-V pins.

*10: Output of I^2C.

*11: Output of Media LB pins

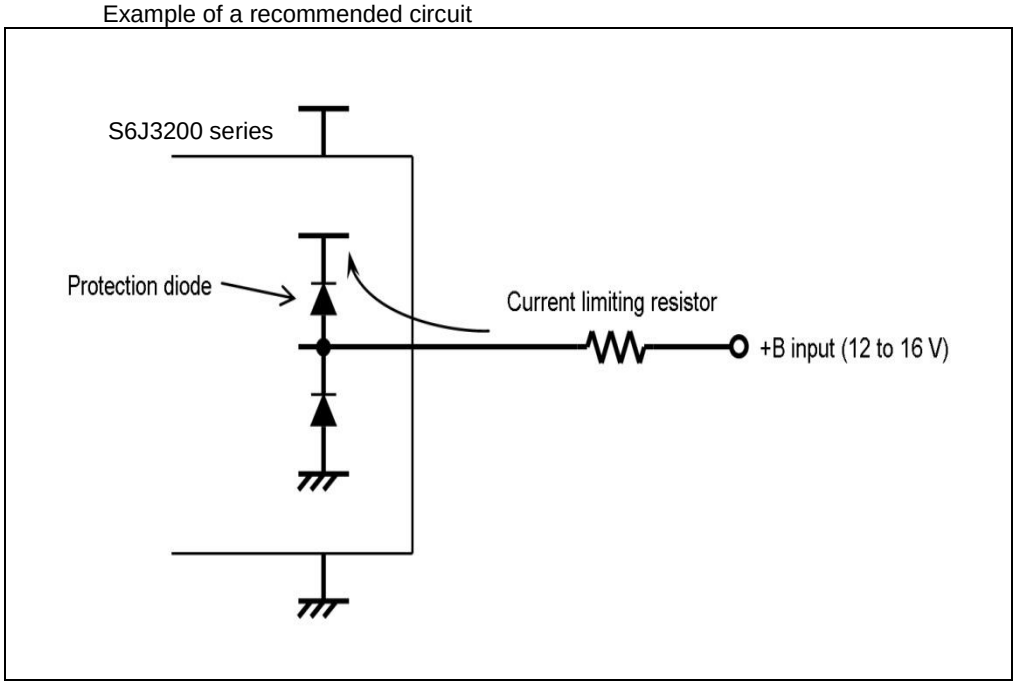
*12: VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.

*13: Take care that the output voltage of ADC shared pins does not exceed AVCC5+0.3 V because ADC Analog input pins (AN0-49) are internally connected to the analog elements. It is strongly recommended to set VCC5, DVCC, and AVCC5 to the same voltage.

*A: Relevant pins: All general-purpose ports and analog input pins

- Corresponding pins: all general-purpose ports
- Use within the operation assurance condition (See 8.2. Operation Assurance).
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- It is recommended to confirm that the maximum ratings at the pins is not exceeded using simulation based on the IBIS model. Variation of the resistance and voltages shall be included for this simulation.

Example of a recommended circuit



WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

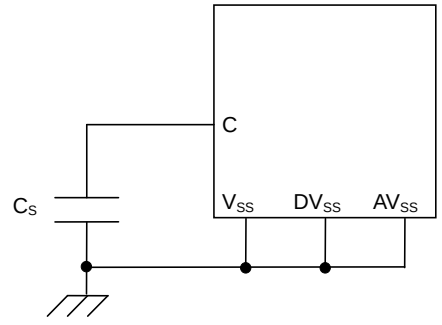
8.2 Operation Assurance Condition

Parameter	Symbol		Value		Unit	Remarks
	Power Supply	Corresponding Ground	Min	Max		
Supply voltage	V_{CC5}	V_{SS}	4.5	5.5	V	Specified electric characteristics are assured in this range.
	V_{CC53}	V_{SS}	4.5	5.5	V	
			3.0	3.6	V	
	DV_{CC}	DV_{SS}	4.5	5.5	V	
	AV_{CC5}	AV_{SS}	4.5	5.5	V	
	V_{CC3}	V_{SS}	3.0	3.6	V	
	V_{CC12}	V_{SS}	1.1	1.3	V	
	AV_{CC3}_DAC	AV_{SS3}_DAC	3.0	3.6	V	
	V_{CC3}_LVDS_Tx	V_{SS3}_LVDS_Tx	3.0	3.6	V	
	AV_{CC3}_LVDS_PLL	AV_{SS3}_LVDS_PLL	3.0	3.6	V	
	V_{CC5}	V_{SS}	3.5	5.5	V	Specified electric characteristics are NOT assured in this range.
	V_{CC53}	V_{SS}	2.7	5.5	V	
	DV_{CC}	DV_{SS}	3.5	5.5	V	
	AV_{CC5}	AV_{SS}	3.5	5.5	V	
	V_{CC3}	V_{SS}	2.7	3.6	V	
	AV_{CC3}_DAC	AV_{SS3}_DAC	2.7	3.6	V	
Ripple on FPD-Link PLL supply	Vpp	-	-	7	mV	AV_{CC3}_LVDS_PLL peak-peak supply noise
Smoothing capacitor*1	C_S	-	4.7		µF	Tolerance of up to ±40%
Operating temperature	T_A	-	-40	+105	°C	See the notes below.
	T_C	-	-40	+144	°C	

Notes:

- **1. For the connections of smoothing capacitor C_S, see the following diagram.*
- *Power supply sequence is recommended as*
  VCC5 ➔ [DVCC or AVCC5 or VCC3 or AVCC3] ➔ VCC12 ➔ [AVCC3_LVDS_PLL or VCC3_LVDS_TX]
  VCC5 ➔ [AVCC5 or DVCC] ➔ [VCC12 or VCC3 or AVCC3_DAC] ➔ [AVCC3_LVDS_PLL or VCC3_LVDS_TX]
  VCC5 ➔ AVCC5 ➔ [DVCC or VCC12 or VCC3 or AVCC3_DAC] ➔ [AVCC3_LVDS_PLL or VCC3_LVDS_TX]
- *Note that power supplies inside "[ ]" can be turned on in arbitrary order.*
- *It is recommended to set AVCC5 and VCC5 to the same voltage.*
- *If you are connecting V_{CC3}_LVDS_Tx and AV_{CC3}_LVDS_PLL to the same supply source, it is recommended to use a R/C noise filter to ensure the Ripple on the FPD-Link PLL supply.*

C Pin Connection Diagram



WARNING:

1. *The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this datasheet. If you are considering application under any conditions other than listed herein, contact a sales representative before you implement the settings.*

Notes:

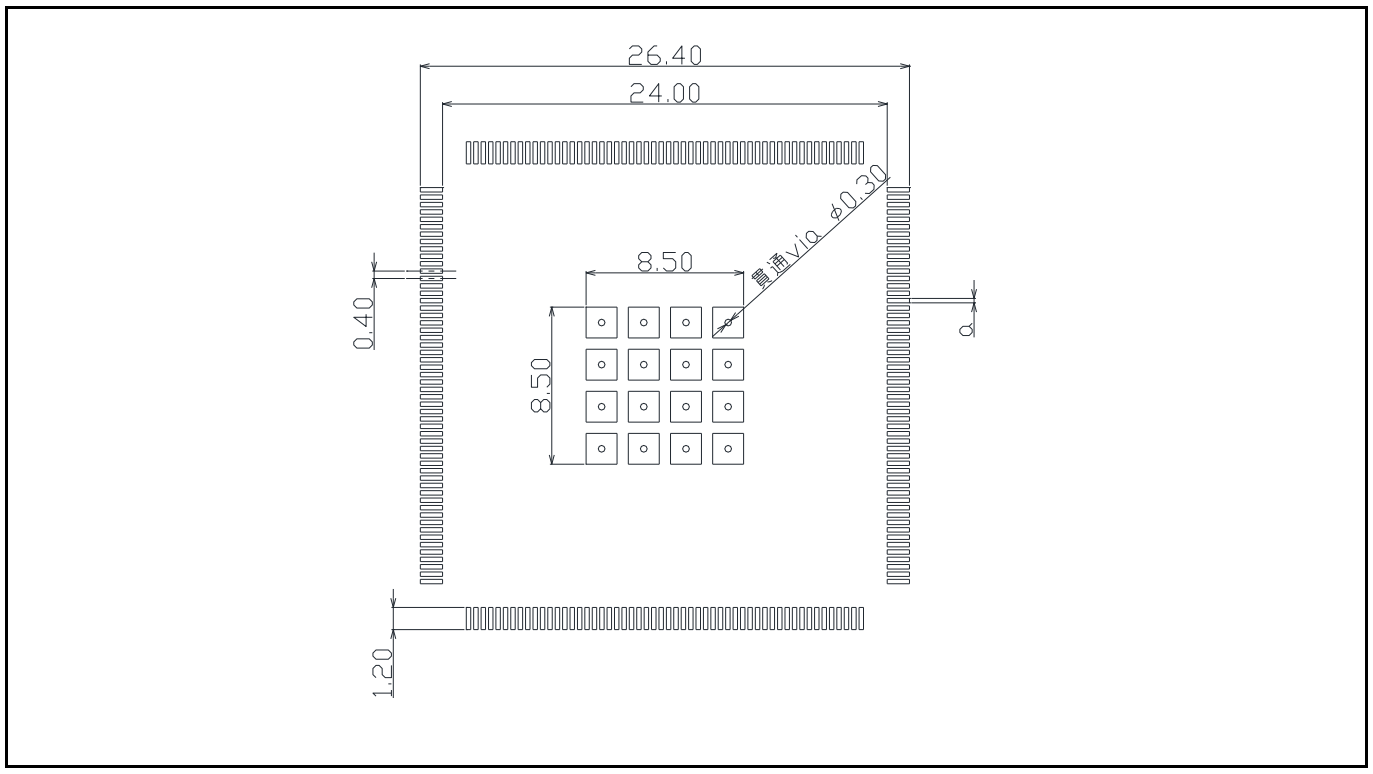
- *T_A: Ambient temperature (JEDEC)*
- *T_C: Case temperature (JEDEC), the maximum measured temperature of package case top.*
- *Both rating of T_A and T_C should simultaneously be satisfied as maximum operation temperature.*
- *The following conditions should be satisfied to facilitate heat dissipation.*
    1. *Four or more layers PCB should be used.*
    2. *The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)*
    3. *One layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.*
    4. *35% or more of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.*
    5. *The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.*

Figure 8-1: Example Thermal via Holes on PCB.

Notes:

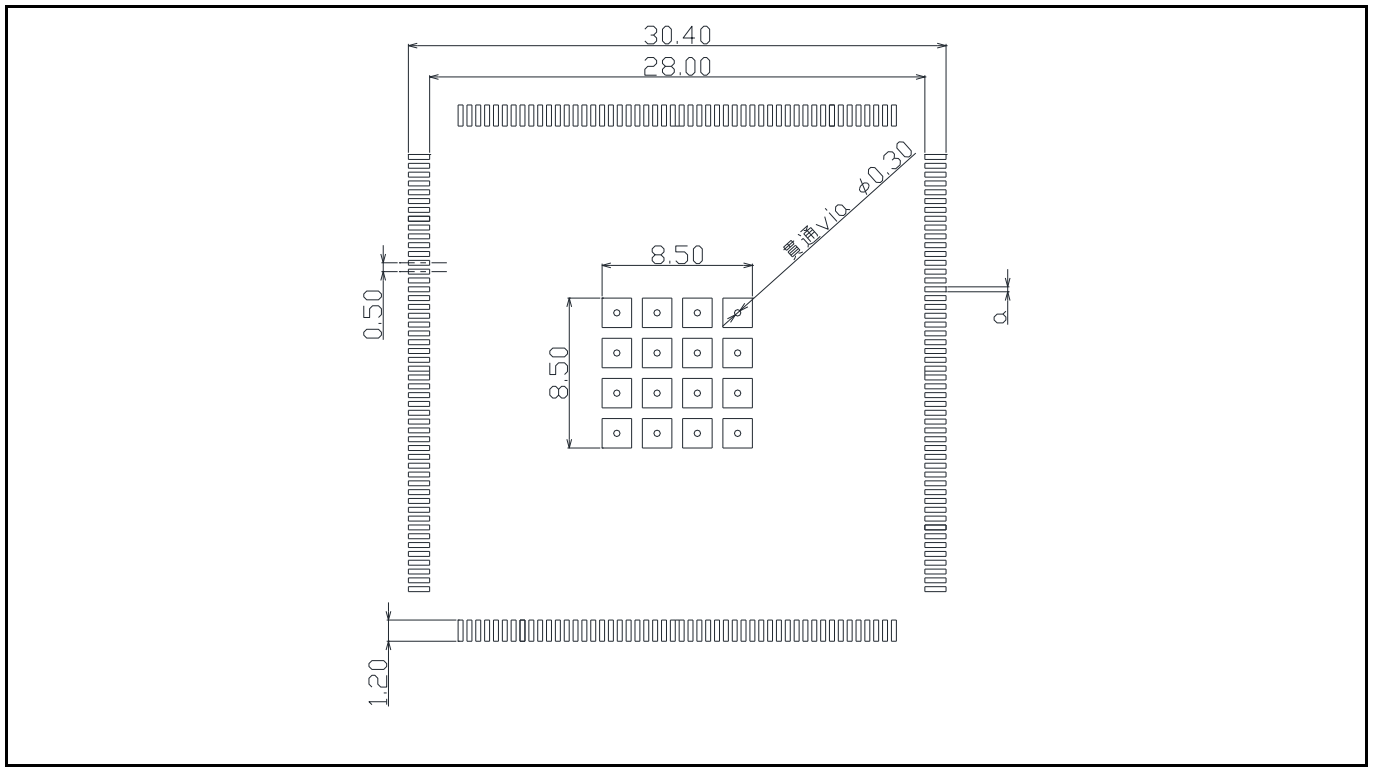
- *Figure 8-1 is a schematic diagram showing PCB in section.*
- *Figure 8-2, Figure 8-3, and Figure 8-4 in the following pages are recommended land patterns for each package series. Thermal via holes should be placed closely and aligned with lands.*
- *When thermal via holes cannot be with lands, the following are recommended as represented by Figure 8-4 which is an example for LEQ-216.*
- *(1). Increase pattern area size as much as possible inside the package outline.*
- *(2). Place thermal via holes to be with lands as close as possible.*
- *0.25 mm ≤ a ≤ 0.30 mm in Figure 8-2, Figure 8-3, and Figure 8-4.*

Figure 8-2: Land Pattern and Thermal via LEQ-216



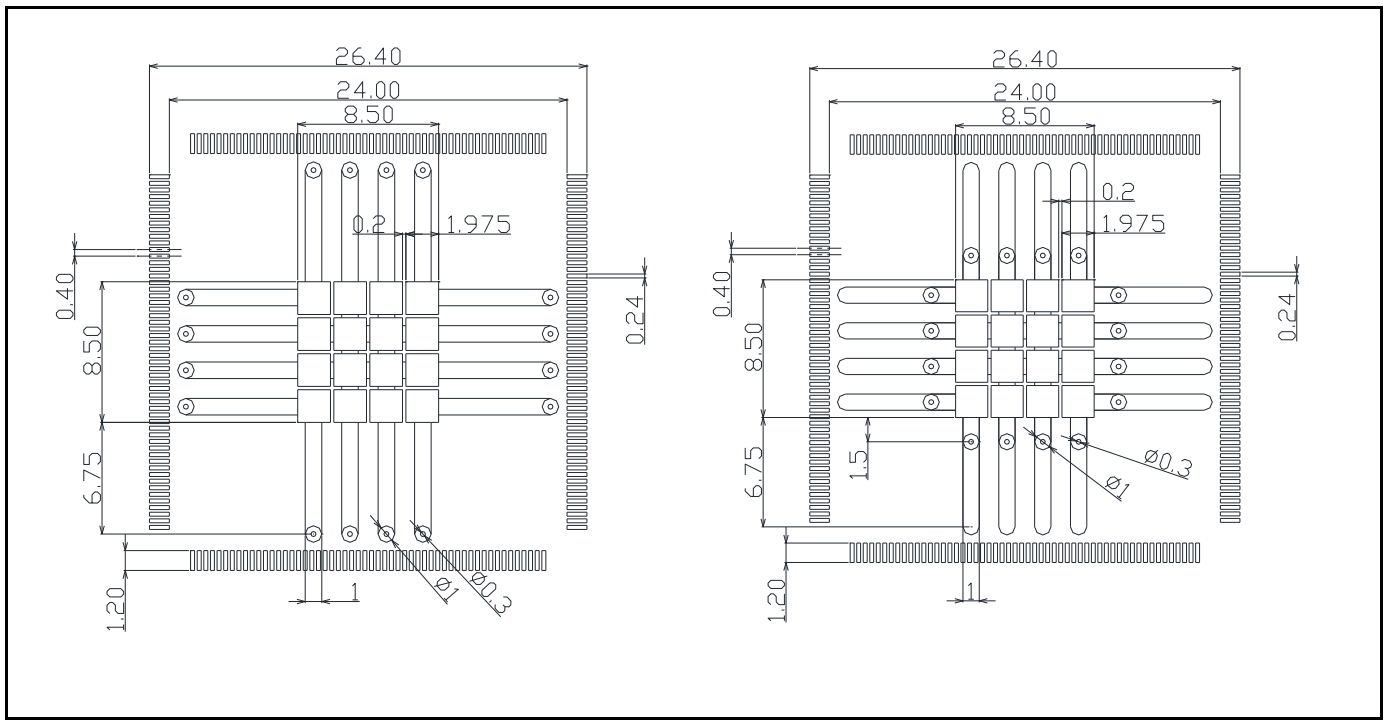
0.25 mm ≤ a ≤ 0.30 mm

Figure 8-3: Land Pattern and Thermal via LET-208



0.25 mm ≤ a ≤ 0.30 mm

Figure 8-4: Optional Land Pattern



0.25 mm ≤ a ≤ 0.30 mm

8.3 DC Characteristics

8.3.1 Port Function Characteristics

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level Input voltage	V_{IH1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	CMOS hysteresis input level is selected	$0.7\times V_{CC53}$	-	$V_{CC53}+0.3$	V	
	V_{IH2}		Automotive input level is selected	$0.8\times V_{CC53}$	-	$V_{CC53}+0.3$	V	
	V_{IH3}		TTL input level is selected	2.0	-	$V_{CC53}+0.3$	V	
	V_{IH4}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P6_02 to 08, 17 to 19	CMOS hysteresis input level is selected	$0.7\times V_{CC5}$	-	$V_{CC5}+0.3$	V	
	V_{IH5}		Automotive input level is selected	$0.8\times V_{CC5}$	-	$V_{CC5}+0.3$	V	
	V_{IH6}	P2_25, 26, P3_00, 01	TTL input level is selected	2.0	-	$V_{CC5}+0.3$	V	
	V_{IH7}	RSTX NMIX	-	$0.7\times V_{CC5}$	-	$V_{CC5}+0.3$	V	
	V_{IH8}	MD	-	$0.7\times V_{CC5}$	-	$V_{CC5}+0.3$	V	
	V_{IH9}	JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS	-	2.3	-	$V_{CC5}+0.3$	V	
	V_{IH10}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	CMOS hysteresis input level is selected	$0.7\times V_{CC3}$	-	$V_{CC3}+0.3$	V	
	V_{IH11}	P0_00 to 19, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	TTL input level is selected	2.0	-	$V_{CC3}+0.3$	V	
	V_{IH12}	P0_26 to 28	-	1.8	-	$V_{CC3}+0.3$	V	MediaLB
	V_{IH13}	P3_21 to 31, P4_00 to 12, P6_09 to 16	CMOS hysteresis input level is selected	$0.7\times DV_{CC}$	-	$DV_{CC}+0.3$	V	
	V_{IH14}		Automotive input level is selected	$0.8\times DV_{CC}$	-	$DV_{CC}+0.3$	V	

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level Input voltage	V_{IL1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	CMOS hysteresis input level is selected	V_{SS}-0.3	-	0.3×V_{CC53}	V	
	V_{IL2}		Automotive input level is selected	V_{SS}-0.3	-	0.5×V_{CC53}	V	
	V_{IL3}		TTL input level is selected	V_{SS}-0.3	-	0.8	V	
	V_{IL4}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P6_02 to 08, 17 to 19	CMOS hysteresis input level is selected	V_{SS}-0.3	-	0.3×V_{CC5}	V	
	V_{IL5}		Automotive input level is selected	V_{SS}-0.3	-	0.5×V_{CC5}	V	
	V_{IL6}	P2_25, 26, P3_00, 01	TTL input level is selected	V_{SS}-0.3	-	0.8	V	
	V_{IL7}	RSTX NMIX	-	V_{SS}-0.3	-	0.3×V_{CC5}	V	
	V_{IL8}	MD	-	V_{SS}-0.3	-	0.3×V_{CC5}	V	
	V_{IL9}	JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS	-	V_{SS}-0.3	-	0.8	V	
	V_{IL10}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	CMOS hysteresis input level is selected	V_{SS}-0.3	-	0.3×V_{CC3}	V	
	V_{IL11}	P0_00 to 19, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	TTL input level is selected	V_{SS}-0.3	-	0.8	V	
	V_{IL12}	P0_26 to 28	-	V_{SS}-0.3	-	0.7	V	MediaLB
	V_{IL13}	P3_21 to 31, P4_00 to 12, P6_09 to 16	CMOS hysteresis input level is selected	DV_{SS}-0.3	-	0.3×DV_{CC}	V	
	V_{IL14}		Automotive input level is selected	DV_{SS}-0.3	-	0.5×DV_{CC}	V	

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	V_{CC53} = 3.0 V I_{OH} = -1.0 mA	V_{CC53}-0.5	-	V_{CC53}	V	
	V_{OH2}		V_{CC53} = 3.0 V I_{OH} = -2.0 mA	V_{CC53}-0.5	-	V_{CC53}	V	
	V_{OH3}		V_{CC53} = 3.0 V I_{OH} = -5.0 mA	V_{CC53}-0.5	-	V_{CC53}	V	
	V_{OH4}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P6_02 to 08, 17 to 19	V_{CC5} = 4.5 V I_{OH} = -1.0 mA	V_{CC5}-0.5	-	V_{CC5}	V	
	V_{OH5}		V_{CC5} = 4.5 V I_{OH} = -2.0 mA	V_{CC5}-0.5	-	V_{CC5}	V	
	V_{OH6}		V_{CC5} = 4.5 V I_{OH} = -5.0 mA	V_{CC5}-0.5	-	V_{CC5}	V	
	V_{OH7}	PSC_1	V_{CC5} = 4.5 V I_{OH} = -2.0 mA	V_{CC5}-0.5	-	V_{CC5}	V	
	V_{OH8}	JTAG_TDO	$V_{CC}5$ = 4.5 V I_{OH} = -5.0 mA	V_{CC5}-0.5	-	V_{CC5}	V	
	V_{OH12}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	V_{CC3} = 3.0 V I_{OH} = -2.0 mA	V_{CC3}-0.5	-	V_{CC3}	V	
	V_{OH13}		V_{CC3} = 3.0 V I_{OH} = -5.0 mA	V_{CC3}-0.5	-	V_{CC3}	V	
	V_{OH14}		V_{CC3} = 3.0 V I_{OH} = -10.0 mA	V_{CC3}-0.5	-	V_{CC3}	V	
	V_{OH15}	P0_00 to 19, P5_21, 22, 27 to 31, P6_00, 01	V_{CC3} = 3.0 V I_{OH} = -20.0 mA	V_{CC3}-0.5	-	V_{CC3}	V	
	V_{OH16}	P0_26 to 28	V_{CC3} = 3.0 V I_{OH} = -6.0 mA	2.0	-	V_{CC3}	V	MediaLB
	V_{OH20}	P3_21 to 31, P4_00 to 12, P6_09 to 16	DV_{CC5} = 4.5 V I_{OH} = -1.0 mA	DV_{CC}-0.5	-	DV_{CC}	V	SMC
	V_{OH21}		DV_{CC5} = 4.5 V I_{OH} = -2.0 mA	DV_{CC}-0.5	-	DV_{CC}	V	SMC
	V_{OH22}		DV_{CC5} = 4.5 V I_{OH} = -5.0 mA	DV_{CC}-0.5	-	DV_{CC}	V	SMC
	V_{OH23}		DV_{CC} = 4.5 V I_{OH} = -30.0 mA	DV_{CC}-0.5	-	DV_{CC}	V	SMC
	V_{OH24}		DV_{CC} = 4.5 V I_{OH} = -40.0 mA	DV_{CC}-0.55	-	DV_{CC}	V	SMC T_J=-40°C

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	V_{CC53}=3.0 V I_{OL}=1.0 mA	0	-	0.4	V	
	V_{OL2}		V_{CC53}=3.0 V I_{OL}=2.0 mA	0	-	0.4	V	
	V_{OL3}		V_{CC53}=3.0 V I_{OL}=5.0 mA	0	-	0.4	V	
	V_{OL4}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P6_02 to 08, 17 to 19	V_{CC5}=4.5 V I_{OL}=1.0 mA	0	-	0.4	V	
	V_{OL5}		V_{CC5}=4.5 V I_{OL}=2.0 mA	0	-	0.4	V	
	V_{OL6}		V_{CC5}=4.5 V I_{OL}=5.0 mA	0	-	0.4	V	
	V_{OL7}	PSC_1	V_{CC5}=4.5 V I_{OL}=2.0 mA	0	-	0.4	V	
	V_{OL8}	JTAG_TDO	V_{CC5}=4.5 V I_{OL}=5.0 mA	0	-	0.4	V	
	V_{OL9}	P2_25, 26, P3_00, 01	V_{CC5}=4.5 V I_{OL}=3.0 mA	0	-	0.4	V	I^2C
	V_{OL12}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	V_{CC3}=3.0 V I_{OL}=2.0 mA	0	-	0.4	V	
	V_{OL13}		V_{CC3}=3.0 V I_{OL}=5.0 mA	0	-	0.4	V	
	V_{OL14}		V_{CC3}=3.0 V I_{OL}=10.0 mA	0	-	0.4	V	
	V_{OL15}	P0_00 to 19, P5_21, 22, 27 to 31, P6_00, 01	V_{CC3}=3.0 V I_{OL}=20.0 mA	0	-	0.4	V	
	V_{OL16}	P0_26 to 28	V_{CC3}=3.0 V I_{OL}=6.0 mA	0	-	0.4	V	MediaLB
	V_{OL20}	P3_21 to 31, P4_00 to 12, P6_09 to 16	DV_{CC5}=4.5 V I_{OL}=1.0 mA	0	-	0.4	V	SMC
	V_{OL21}		DV_{CC5}=4.5 V I_{OL}=2.0 mA	0	-	0.4	V	SMC
	V_{OL22}		DV_{CC5}=4.5 V I_{OL}=5.0 mA	0	-	0.4	V	SMC
	V_{OL23}		DV_{CC}=4.5 V I_{OL}=30.0 mA	0	-	0.55	V	SMC
	V_{OL24}		DV_{CC}=4.5 V I_{OL}=40.0 mA	0	-	0.55	V	SMC T_J=-40°C

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 26	$V_{CC5} = V_{CC53} = DV_{CC} = AV_{CC} = 5.5$ V $V_{SS} < VI < V_{CC}$	-5	-	+5	µA	5-V pins 5-V/3-V pins
		P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	$V_{CC3} = 3.6$ V $V_{SS} < VI < V_{CC3}$	-10	-	+10	µA	3-V pins
Pull-up resistor	R_{UP1}	RSTX, NMIX	-	25	50	100	kΩ	
	R_{UP2}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 26	Pull-up resistor Selected V_{CC53} = 4.5 V to 5.5 V	25	50	100	kΩ	5-V pins 5-V/3-V pins
		P4_25 to 31, P5_00 to 20, P6_20 to 26	Pull-up resistor Selected V_{CC53} = 3.0 V to 3.6 V	40	100	200	kΩ	5-V/3-V pins
	R_{UP3}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	Pull-up resistor selected	17	33	66	kΩ	3-V pins
	R_{UP4}	JTAG_TDI, JTAG_TMS, JTAG_TCK	-	25	50	100	kΩ	
Pull-down resistor	R_{down1}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31,P5_00 to 20, P6_02 to 26	Pull-down resistor Selected V_{CC53} = 4.5 V to 5.5 V	25	50	100	kΩ	5-V pins 5-V/3-V pins
		P4_25 to 31, P5_00 to 20, P6_20 to 26	Pull-down resistor Selected V_{CC53} = 3.0 V to 3.6 V	40	100	200	kΩ	5-V/3-V pins
	R_{down2}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	Pull-down resistor selected	17	33	66	kΩ	3-V pins
	R_{down3}	JTAG_NTRST	-	25	50	100	kΩ	
Input capacitance	C_{IN1}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P4_25 to 31, P5_00 to 22, 27 to 31, P6_00 to 08, 17 to 26	-	-	5	15	pF	
	C_{IN2}	P3_21 to 31, P4_00 to 12, P6_09 to 16	-	-	15	45	pF	

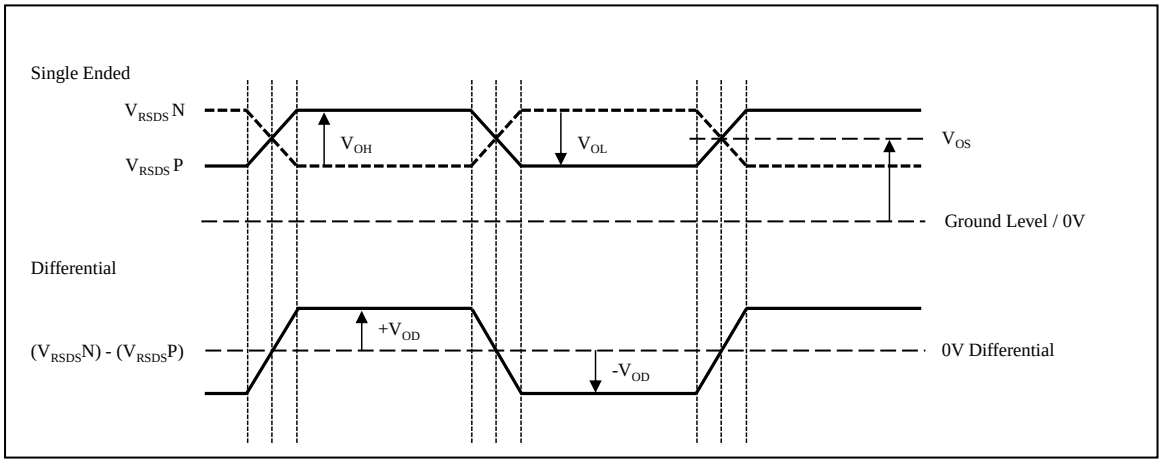
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
High current output drive capacity Phase-to-phase deviation1	Delta-V_{OH23}	P3_21 to 31, P4_00 to 12, P6_09 to 16	DV_{CC} = 4.5 V I_{OH} = -30.0 mA Maximum deviation of V_{OH23}	-	-	90	mV	*
High current output drive capacity Phase-to-phase deviation2	Delta-V_{OL23}		DV_{CC} = 4.5 V I_{OL} = 30.0 mA Maximum deviation of V_{OL23}	-	-	90	mV	*

*: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of V_{OH4} / V_{OL4} for each pin is defined. Same for other channels.

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output Differential Voltage	| V_{OD} |	DSP0_DATAn+, DSP0_DATAn- n=0 to 11	BOOST = 0 (Drivability 2 mA) R_L = 100 Ω	100	200	600	| mV |	
			BOOST = 1 (Drivability 4 mA) R_L = 50 Ω					
Output Offset Voltage	V_{OS}		BOOST=0 (Drivability 2 mA) R_L = 100 Ω	0.5	1.2	1.5	V	
			BOOST = 1 (Drivability 4 mA) R_L = 50 Ω					



8.3.2 Power Supply Current

8.3.2.1 Run Mode

(Condition: See 8.2. Operation Assurance)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CC5}	VCC5	Normal Operation	45	-	mA	25	-
			-	70	mA	105	
		Adder for Work Flash Programming or Erasing	-	20	mA	105	-
I_{CC12}	VCC12	CPU: 240 MHz, HPM: 120 MHz, GDC: 200 MHz (Worst case use case)	700	-	mA	25	*2
			-	1250	mA	105	*2
		CPU: 120 MHz, HPM: 60 MHz, GDC: 0 MHz For TC Flash Programming or Erasing (Worst case use case)	-	900	mA	105	*2
		CPU: 80 MHz, HPM: 40 MHz, GDC: 0 MHz For TC Flash Programming or Erasing Worst case use case	-	800	mA	105	*2
		Example use case *3	-	635	mA	105	*3
		Adder for Work Flash Programming or Erasing	-	20	mA	105	-
ILVDS	VCC3_LVDS_Tx	50 MHz	-	75	mA	105	*1
	AVCC3_LVDS_PLL	50 MHz	-	9	mA	105	-

Notes:

- *The output port current is not included in the specified value*
- **1. A few mA, which depend on usage for FPD-Link data transfer, should be estimated for each port in an actual application, and then it should be added to the current consumption at VCC3_LVDS_Tx.*
- *The current consumption at VCC3_LVDS_Tx is specified under RL= 100 ohm, CL= 5 pF, f = 50 MHz, and 0/1 alternation pattern output.*
- **2 This current consumption assumes extremely high activity, which is unlikely to achieved in real application. Actual current consumption is dependent on actual application.*
- **3 Example use case at following conditions*
  CPU: 240 MHz, HPM: 120 MHz, GDC: 200 MHz
  *(Clock settings according to ch 8.4.3 Internal Clock Timing Max*1)*
  Active peripherals: Ethernet, 1ch HyperBus (Flash+RAM), PWMs, ADC, 6ch SMCs, I^2C, 2ch CAN, 2ch LIN and 2ch SPI
  DMAC active (WorkFlash > SystemRAM), All timers active
  CPU: Arm Cortex R5_max_power function
  GFX-Sub system:
  Blit Engine with 3 (= all) source buffers active (ROP3, noise RGBA, 32 bpp)
  Both Display Controllers with 7 display buffers active (noise RGBA, 32 bpp)
  Drawing Engine and Command Sequencer active, Capture controller idle
  Display Controller #1 : 10 MHz RGB interface
  Display Controller #2 : 22 MHz FPD link
  I/Os do no toggle

8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF)

(Condition: See 8.2. Operation Assurance)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCT5}	VCC5	4-MHz Crystal for Main Oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON	350	600	µA	25	C_L=10 pF MCGAIN = 0b00 (4 MHz)
		4-MHz Crystal for Main Oscillator PD1 = ON, PD4_0 or PD4_1 = ON	345	575	µA	25	C_L=10 pF MCGAIN = 0b00 (4 MHz)
		4-MHz Crystal for Main Oscillator PD1 = ON, PD4_0 = OFF, PD4_1 = OFF	340	550	µA	25	C_L= 10 pF MCGAIN = 0b00 (4 MHz)
		8-MHz Crystal for Main Oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON	450	730	µA	25	C_L= 10 pF MCGAIN = 0b01(8 MHz)
		8-MHz Crystal for Main Oscillator PD1 = ON, PD4_0 or PD4_1 = ON	445	705	µA	25	C_L=10 pF MCGAIN = 0b01(8 MHz)
		8-MHz Crystal for Main Oscillator PD1 = ON, PD4_0 = OFF, PD4_1 = OFF	440	680	µA	25	C_L=10 pF MCGAIN = 0b01(8 MHz)
		4-MHz External Clock PD1 = ON, PD4_0 = ON, PD4_1 = ON	180	280	µA	25	-
		4-MHz External Clock PD1 = ON, PD4_0 or PD4_1 = ON	175	275	µA	25	-
		4-MHz External Clock PD1 = ON, PD4_0 = OFF, PD4_1 = OFF	170	270	µA	25	-
		8-MHz External Clock PD1 = ON, PD4_0 = ON, PD4_1 = ON	190	300	µA	25	-
		8-MHz External Clock PD1 = ON, PD4_0 or PD4_1 = ON	185	295	µA	25	-
		8-MHz External Clock PD1 = ON, PD4_0 = OFF, PD4_1 = OFF	180	290	µA	25	-
		32-kHz Crystal for Sub Oscillator PD1 = ON, PD4_0 = ON, PD4_1 = ON	85	300	µA	25	-
		32-kHz Crystal for Sub Oscillator PD1 = ON, PD4_0 or PD4_1 = ON	80	275	µA	25	-
		32-kHz Crystal for Sub Oscillator PD1 = ON, PD4_0 = OFF, PD4_1 = OFF	75	250	µA	25	-

Note:

- *The values have been standardized with regulator standby mode (RMSEL=1) and CR-oscillators disabled.*

8.3.2.3 PSS Stop Mode Shutdown

(Condition: See 8.2. Operation Assurance)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCH5}	VCC5	PD1 = ON, PD4_0 = ON, PD4_1 = ON	54	81	µA	25	Revision M and P only
		PD1 = ON, PD4_0 or PD4_1 = ON	52	78	µA	25	
		PD1 = ON, PD4_0 = OFF, PD4_1 = OFF	49	70	µA	25	
		PD1 = ON, PD4_0 = ON, PD4_1 = ON	65	150	µA	25	Except revision M and P
		PD1 = ON, PD4_0 or PD4_1 = ON	60	145	µA	25	
		PD1 = ON, PD4_0 = OFF, PD4_1 = OFF	55	140	µA	25	

Note:

- *The values have been standardized with regulator standby mode (RMSEL=1) and CR-oscillators disabled.*

8.3.2.4 Internal CR oscillator current consumption

(Condition: See 8.2. Operation Assurance)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
	VCC5	Slow CR oscillator (100 kHz) – operation mode	1	3	µA	105	-
		Fast CR oscillator (4 MHz) – operation mode	22	52	µA	105	Before trimming
		Fast CR oscillator (4 MHz) – operation mode	17	40	µA	105	After trimming

8.4 AC Characteristics

8.4.1 Source Clock Timing

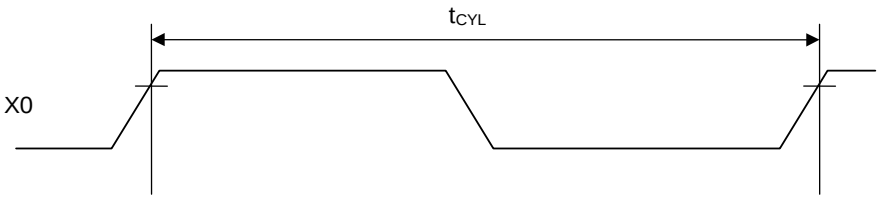
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	FC	X0, X1	-	3.6	-	16	MHz	
Source oscillation clock cycle time	tCYL	X0, X1	-	62.5	-	277.8	ns	
CAN PLL jitter (when locked)	tPJ	-	-	-10	-	10	ns	
Internal Slow CR oscillation frequency	FCRS	-	-	50	100	150	kHz	
Internal Fast CR oscillation frequency	FCRF	-	-	2.40	4.00	5.61	MHz	Before trim
				3.20	4.00	4.81	MHz	After trim

Notes:

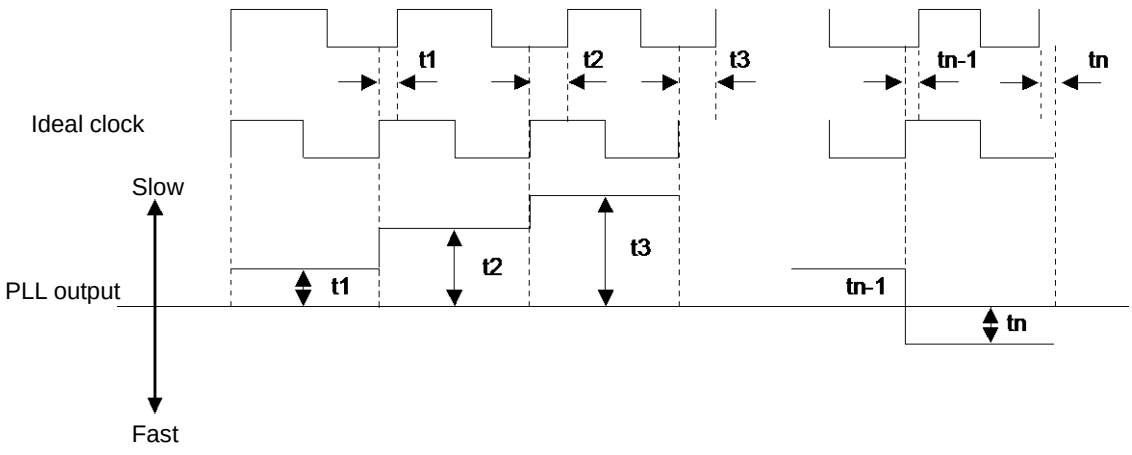
- *The maximum/minimum values have been standardized with the main clock and PLL clock in use.*
- *The error of source oscillator frequency must be smaller than 3000 ppm.*
- *Enough evaluation and adjustment are recommended using oscillator on your system board.*

- X0 and X1 clock timing



CAN PLL jitter

A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.

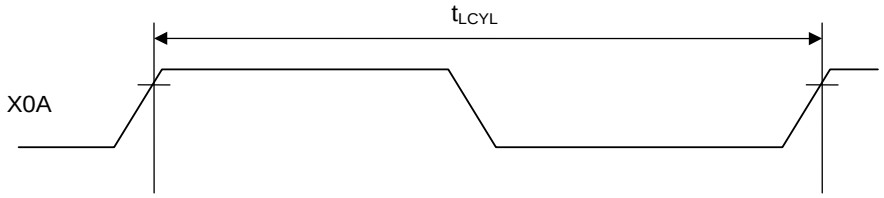


8.4.2 Sub Clock Timing

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	-	-	30.52	-	µs	

- X0A and X1A clock timing



8.4.3 Internal Clock Timing

- This section shows the characteristics for internal clock timing at the current stage.
- In the column symbol, the same clock names as described in 'Chapter 5: Clock System' of the Platform hardware manual are used.
- Corresponding functions for these clocks are described in 'Chapter 5: Clock Configuration' of the S6J3200 series hardware manual.

(Condition: See 8.2. Operation Assurance)

Table 8-1: Assured Combination of Clock Frequency

Symbol	Max Value Combination			Unit	Remarks
	Max *1	Max *2	Max *3		
F_{SSCG0}	232 (464)	200 (800)	160 (640)	MHz	SSCG0 output clock
F_{SSCG1}	200 (800)	200 (800)	200 (800)	MHz	SSCG1 output clock
F_{SSCG2}	200 (800)	200 (800)	200 (800)	MHz	SSCG2 output clock
F_{SSCG3}	400 (800)	400 (800)	400 (800)	MHz	SSCG3 output clock
F_{PLL0}	240 (480)	200 (800)	200 (800)	MHz	PLL0 output clock
F_{PLL1}	400 (800)	400 (800)	400 (800)	MHz	PLL1 output clock
F_{PLL2}	200 (800)	200 (800)	200 (800)	MHz	PLL2 output clock
F_{PLL3}	240 (480)	240 (480)	240 (480)	MHz	PLL3 output clock
F_{CLK_CPU0}	240	200	160	MHz	
F_{CLK_SHE}	240	200	160	MHz	
F_{CLK_FCLK}	80	66.7	80	MHz	
F_{CLK_ATB}	120	100	80	MHz	
F_{CLK_DBG}	120	100	80	MHz	
F_{CLK_HPM}	120	200	160	MHz	

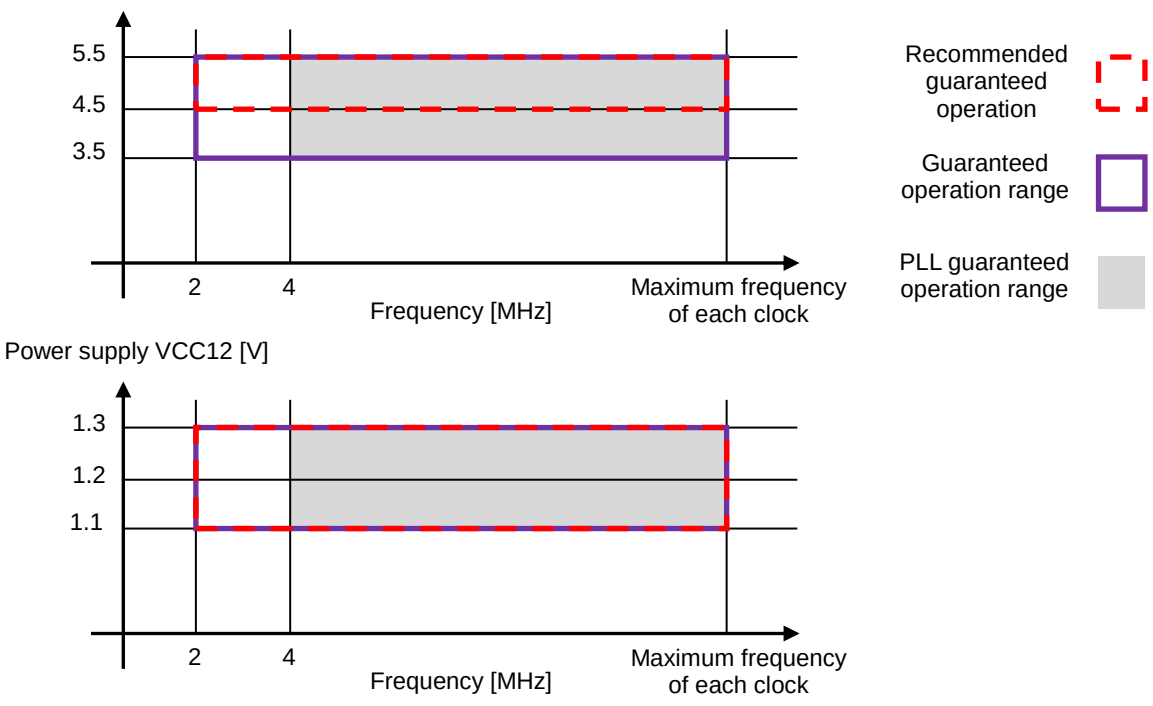
Symbol	Max Value Combination			Unit	Remarks
	Max *1	Max *2	Max *3		
F_{CLK_HPM2}	60	100	80	MHz	
F_{CLK_DMA}	120	200	160	MHz	
F_{CLK_MEMC}	120	200	160	MHz	
F_{CLK_EXTBUS}	40	40	40	MHz	Unused
F_{CLK_SYSC1}	40	40	40	MHz	
$F_{CLK_HAPP0A0}$	40	40	40	MHz	Unused
$F_{CLK_HAPP0A1}$	40	40	40	MHz	Unused
$F_{CLK_HAPP1B0}$	60	50	80	MHz	
$F_{CLK_HAPP1B1}$	40	40	40	MHz	Unused
F_{CLK_LLPBM}	240	200	160	MHz	
F_{CLK_LLPBM2}	120	100	80	MHz	
F_{CLK_LCP}	60	50	80	MHz	
F_{CLK_LCP0}	40	40	40	MHz	
F_{CLK_LCP0A}	60	66.7	80	MHz	
F_{CLK_LCP1}	40	40	40	MHz	Unused
F_{CLK_LCP1A}	60	66.7	80	MHz	
F_{CLK_LAPP0}	40	40	40	MHz	Unused
F_{CLK_LAPP0A}	40	40	40	MHz	Unused
F_{CLK_LAPP1}	40	40	40	MHz	Unused
F_{CLK_LAPP1A}	40	40	40	MHz	Unused
F_{CLK_TRC}	100	100	100	MHz	
F_{CLK_CD1}	400	400	400	MHz	
F_{CLK_CD1A0}	100	100	100	MHz	Unused
F_{CLK_CD1A1}	100	100	100	MHz	Unused
F_{CLK_CD1B0}	100	100	100	MHz	Unused
F_{CLK_CD1B1}	100	100	100	MHz	Unused
F_{CLK_CD2}	400	400	400	MHz	Unused
F_{CLK_CD2A0}	400	400	400	MHz	
F_{CLK_CD2A1}	400	400	400	MHz	Unused
F_{CLK_CD2B0}	400	400	400	MHz	Unused
F_{CLK_CD2B1}	400	400	400	MHz	Unused
F_{CLK_CD3}	200	200	200	MHz	Unused
F_{CLK_CD3A0}	200	200	200	MHz	
F_{CLK_CD3A1}	200	200	200	MHz	Unused
F_{CLK_CD3B0}	200	200	200	MHz	Unused
F_{CLK_CD3B1}	200	200	200	MHz	Unused
F_{CLK_CD4}	200	200	200	MHz	
F_{CLK_CD4A0}	200	200	200	MHz	Unused
F_{CLK_CD4A1}	200	200	200	MHz	Unused
F_{CLK_CD4B0}	200	200	200	MHz	Unused
F_{CLK_CD4B1}	200	200	200	MHz	Unused
F_{CLK_CD5}	240	240	240	MHz	
F_{CLK_CD5A0}	120	120	120	MHz	
F_{CLK_CD5A1}	120	120	120	MHz	Unused
F_{CLK_CD5B0}	60	60	60	MHz	
F_{CLK_CD5B1}	60	60	60	MHz	Unused
F_{CLK_HSSPI}	200	200	200	MHz	
F_{CLK_SYSC0H}	60	66.7	80	MHz	
F_{CLK_COMH}	60	66.7	80	MHz	
F_{CLK_RAM0H}	60	66.7	80	MHz	
F_{CLK_RAM1H}	60	66.7	80	MHz	
F_{CLK_SYSC0P}	60	66.7	80	MHz	
F_{CLK_COMP}	60	66.7	80	MHz	
F_{CLK_CAN}	40	40	40	MHz	

Notes:

- **1: Maximum clock frequencies when CPU clock = 240 MHz.*
- *For SSCG, down spread and center spread modes are supported with following conditions:*
  - *For down spread mode, clock frequency setting can be up to max SSCG frequency defined in above table.*
  - *For center spread mode, an appropriate clock frequency setting has to be chosen so that the modulated clock does not exceed the max SSCG frequency defined in above table.*
- *240 MHz or less is available for PLL.*
- **2: Maximum clock frequencies when CPU clock = 200 MHz.*
- **3: Maximum clock frequencies when CPU clock = 160 MHz. This is also a combination of maximum clock frequencies for TC FLASH Programming or Erasing.*
- *Even if a combination of clock frequency is able to be configured by software, the frequency should be configured under maximum frequency described in Table 8-1. For example, 80 MHz of CLK_LCP0A seems to be configurable from both divided 240 MHz and 160 MHz of CLK_CPU. But each duty ratio of configured 80 MHz as an internal signal is different from one another. In this series, the 80 MHz from the 160 MHz divided by 2 can only be assured, but the 240 MHz divided by 3 cannot be assured from the internal timing design point of view.*
- *F_{CLK_TRC}/2 (half frequency of F_{CLK_TRC}) comes out of the trace clock port of package external pin.*
- *The frequency described in () is maximum output frequency of SSCG PLL / PLL multiplier circuit.*
- *The configurable minimum frequency of PLLn and SSCGn output is 400 MHz.*
- *"Unused" means a clock source, which does not have any supply destinations. Configure these clocks to a lower clock frequency than the described maximum.*

- Operation assurance range

Relationship between the internal clock frequency and supply voltage

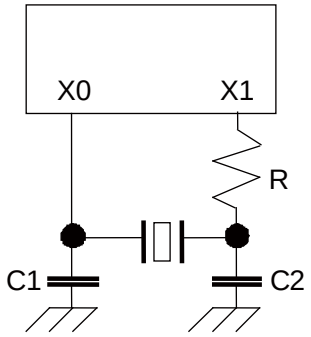


Note: CPU will be reset, when the power supply voltage is equal to or less than LVD setting voltage.

- Relationship between the oscillation clock frequency and internal clock frequency (example)

		Internal Operation Clock Frequency							
		Main Clock	PLL Clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4		Multiplied by 40	Multiplied by 60
Oscillation clock frequency [MHz]	4	2	4	8	12	16	…	160	240

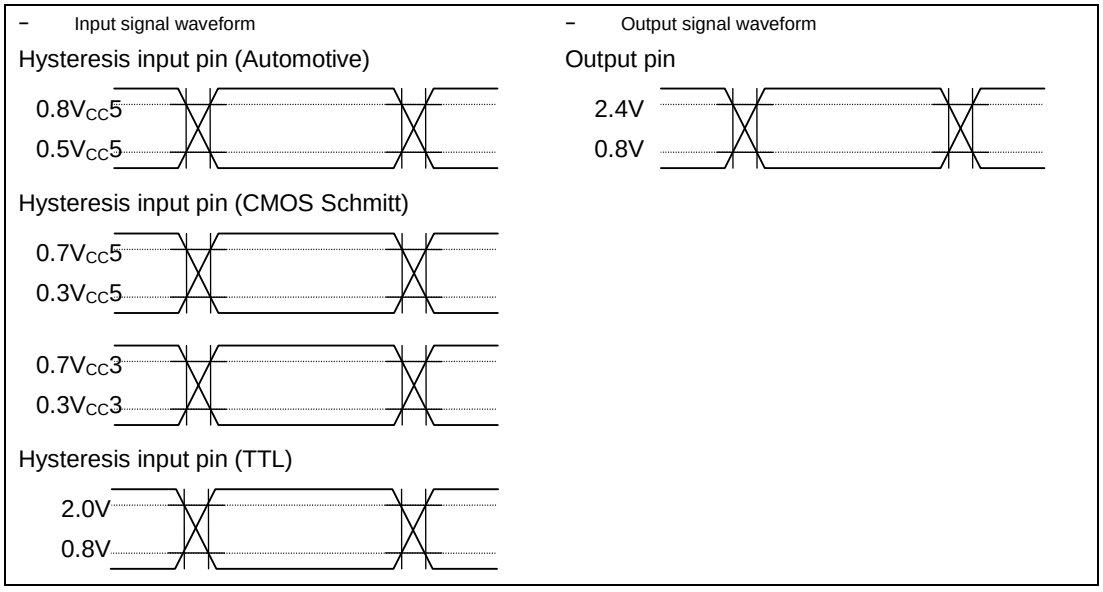
- Oscillation circuit example



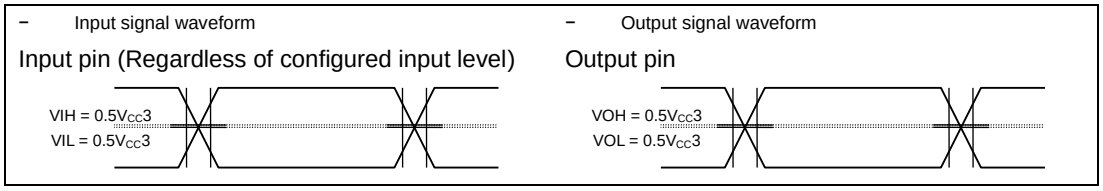
Note:
For the configuration of an oscillation circuit, request the oscillator manufacturer to perform a circuit matching evaluation before designing.

8.4.4 Reference Voltages for AC Characteristics of I/O Cells

AC characteristics are specified by the following measurement reference voltage values.



DDR-HSSPI and HyperBus AC characteristics are specified with the following reference voltages regardless of the automotive input-level configuration, CMOS Schmitt, and TTL.

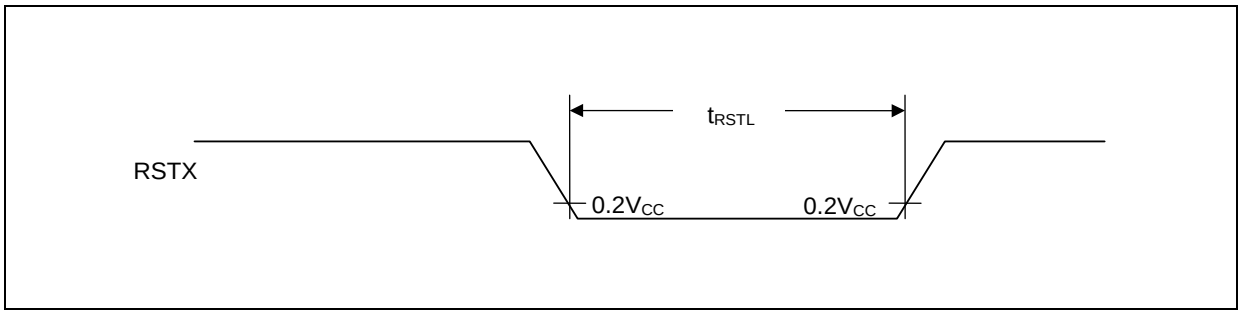


8.4.5 Reset

8.4.5.1 Reset Input

(Condition: See 8.2. Operation Assurance)

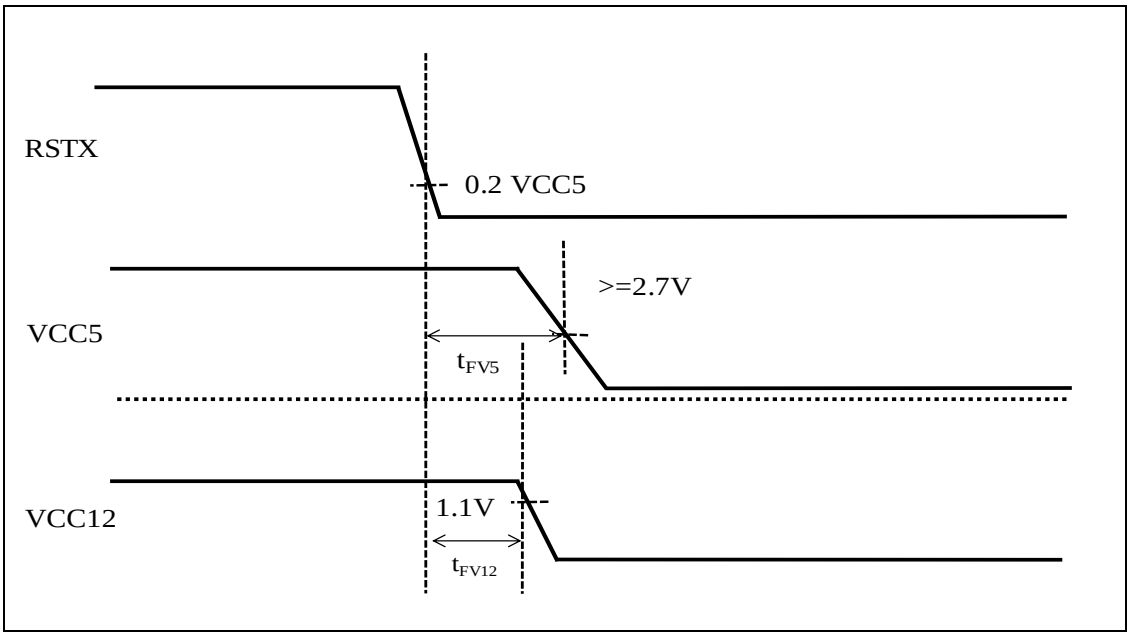
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	
Reset input pulse filter time				-	1	µs	



8.4.5.2 Power Supply Voltage Stability Conditions

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
VCC5 stability time after RSTX assertion	t_{FV5}	VCC5	-	35	-	µs	VCC5 ≥ 2.7 V
VCC12 stability time after RSTX assertion	t_{FV12}	VCC12		35	-	µs	VCC12 ≥ 1.1 V



8.4.6 Power-On Conditions

8.4.6.1 Power-On Conditions

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC5	-	2.15	2.35	2.55	V	
Reset release voltage	-	VCC5	-	2.25	2.45	2.65	V	
Level detection time	-	-	-	-	-	540	µs	*1
Power off time	t_{OFF}	VCC5	VCC5 < 0.2 V	1	-	-	ms	*2
Power ramp rate	dV/dt	VCC5	VCC5: Between 0.2 V to 2.65 V	-	-	6	mV/µs	*3
Power ramp rate	dV/dt	VCC5	VCC5: Between 0.2 V to 2.65 V	-	-	100	mV/µs	*4
Maximum ramp rate guaranteed to not generate power-on reset	|dV/dt|	VCC5	VCC5: Between 2.65 V and 4.5 V	-	-	50	mV/µs	*5

Notes:

*1: If a power fluctuation precedes the low-voltage detection time, the detection may occur or be canceled after the supply voltage passes the detection voltage range.

*2: If Vcc is held below 0.2 V for a minimum period of t_{OFF}, power-on reset will occur. If t_{OFF} is not satisfied, power-on reset will still occur if the power ramp rate is kept below 6 mV/µs.

*3: This is the power ramp rate with which power-on reset will always occur regardless of power-off time, as mentioned in *2.

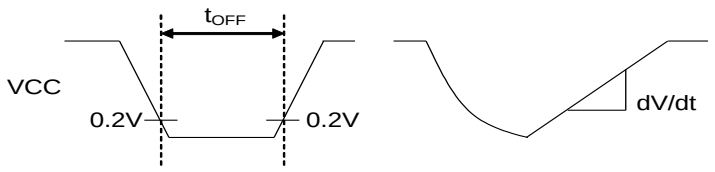
*4 If power ramp rate is below this value power on reset is guaranteed.

*5: When VCC5 is within the 2.65 V to 4.5 V range, and VCC5 fluctuation is below 50 mV/µs, the power-on reset is suppressed. Between 4.5 V to 5.5 V, the power-on reset does not occur with any VCC5 fluctuation.

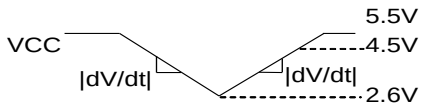
Note:

When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

Power off time, Power ramp rate at Power-on



Maximum ramp rate guaranteed to not generate power-on reset



8.4.6.2 VCC12 Stabilization Time during Power-On / PSS to RUN Transition

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
VCC12 stabilization time during power-on	tV12STPO	VCC12	-		-	-	14.2	ms	*1
VCC12 stabilization time during PSS (PD2 off) to RUN transition (Fast-CR untrimmed)	tV12STP1	VCC12	SYSC0_ SPECFGR: EX12VRSTCNT	0000	-	-	0.7	ms	*1
				0001	-	-	1.4		
				0010	-	-	2.1		
				0011	-	-	2.8		
				0100	-	-	3.5		
				0101	-	-	4.2		
				0110	-	-	4.9		
				0111	-	-	5.7		
				1000	-	-	6.4		
				1001	-	-	7.1		
				1010	-	-	8.5		
				1011	-	-	9.9		
				1100	-	-	11.4		
				1101	-	-	12.8		
				1110 (default)	-	-	14.2		
				1111	-	-	21.3		
VCC12 stabilization time during PSS (PD2 off) to RUN transition (Fast-CR trimmed)	tV12STP2	VCC12	SYSC0_ SPECFGR: EX12VRSTCNT	0000	-	-	0.8	ms	*1
				0001	-	-	1.6		
				0010	-	-	2.4		
				0011	-	-	3.3		
				0100	-	-	4.1		
				0101	-	-	4.9		
				0110	-	-	5.8		
				0111	-	-	6.6		
				1000	-	-	7.4		
				1001	-	-	8.3		
				1010	-	-	9.9		
				1011	-	-	11.6		
				1100	-	-	13.3		
				1101	-	-	14.9		
				1110 (default)	-	-	16.6		
				1111	-	-	24.9		

*1: After LVDL2 reset release during power-on sequence and PSS (PD2 off) to RUN transition, VCC12 has to rise above operation assurance range within this time.

8.4.7 Multi-Function Serial

8.4.7.1 Asynchronous Serial Interface (UART) Timing (SMR:MD2-0=0b000, 0b001)

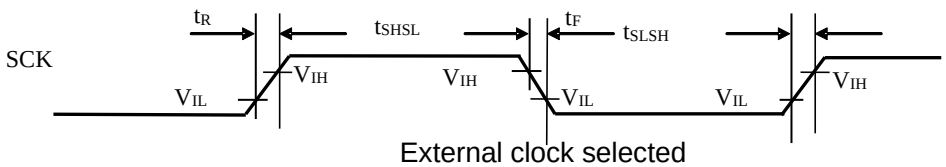
(1) External Clock Selected (BGR:EXT=1)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12	(CL = 50 pF, I_{OL}=-2 mA, I_{OH}=2 mA), (CL=20 pF, I_{OL}=-1 mA, I_{OH}=1 mA)	t_{CLK_LCPnA}*1 +10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12		t_{CLK_LCPnA}*1 +10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	
SCK rising time	t_R			-	5	ns	

Note:

*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12



External clock selected

External clock selected

8.4.7.2 CSIO Timing (SMR:MD2-0=0b010)

(1) Normal Synchronous Transfer (SCR:SPI=0) and Mark Level "H" of Serial Clock Output (SMR:SCINV=0)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Master Mode (CL = 20 pF, I_{OL}= -5 mA, I_{OH} = 5 mA)	$3t_{CLK_LCPnA}$*1	-	ns	
		SCK2		$3t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$3t_{CLK_COMP}$	-		
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12, SOT0, SOT1, SOT3, SOT4, SOT8 to SOT12		-2	30	ns	
				-2	20*2		
		SCK2, SOT2		-2	20		
		SCK16 to SCK17, SOT16, SOT17		-2	15		
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12 SIN0, SIN1, SIN3, SIN4, SIN8 to SIN12		26.5	-	ns	
				20*2	-		
		SCK2, SCK16, SCK17 SIN2, SIN16, SIN17		20	-		
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		0	-	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Slave Mode (CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$			
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
SCK ↓→ SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		0	28.5	ns	
					25 *2		
		SCK16, SCK17 SOT16, SOT17		0	25		
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		10.0	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			1	-	ns	
tSCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	

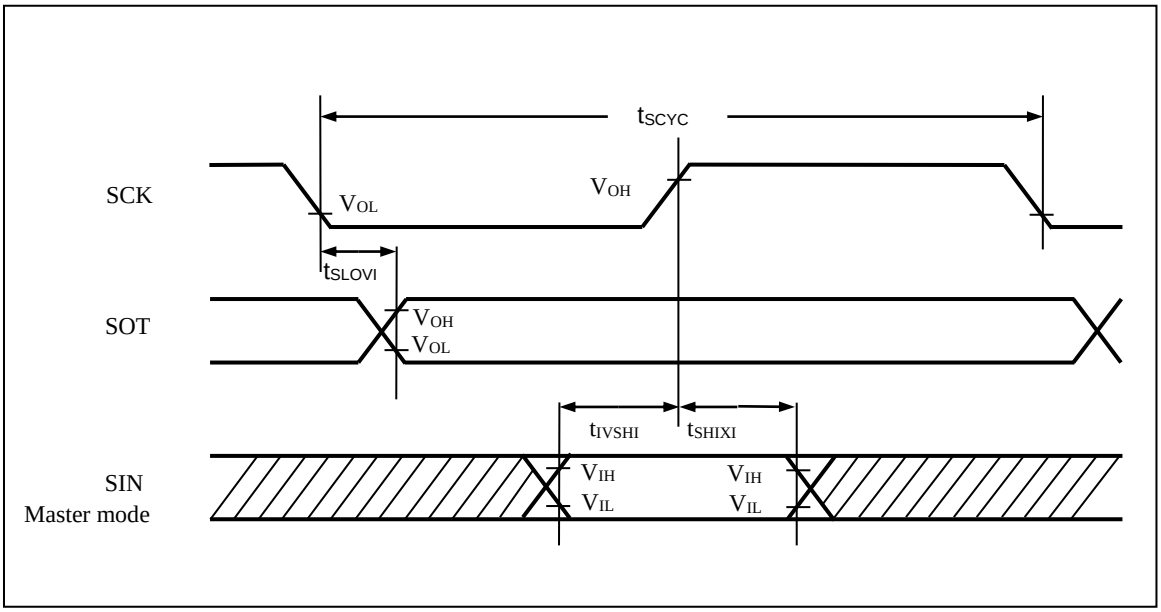
Notes:

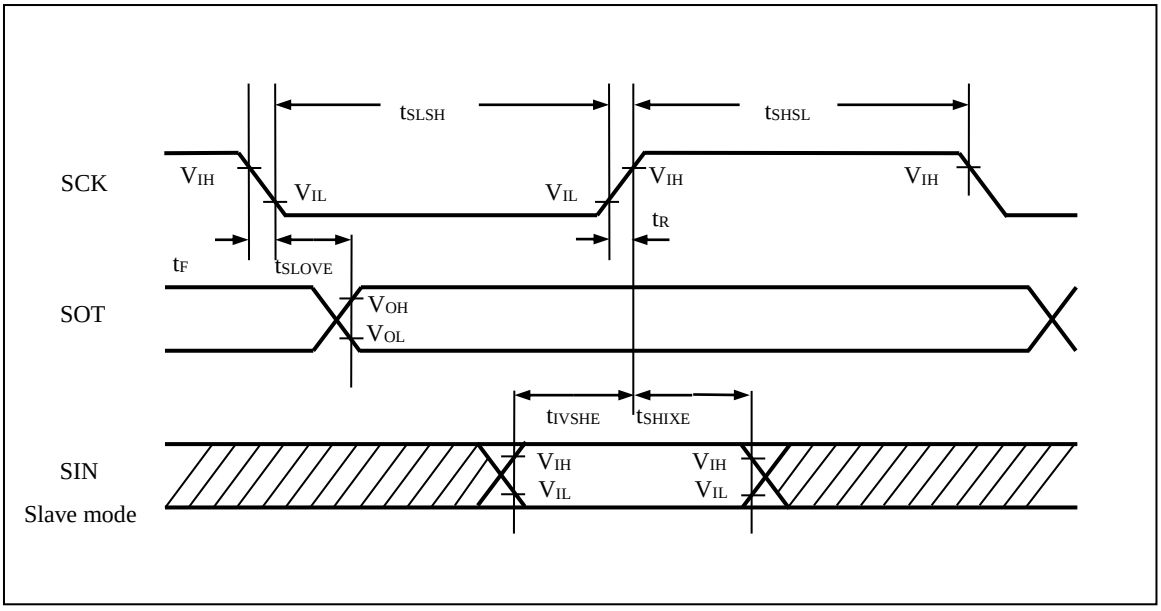
*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12

*2: Group2 of ch.0, ch1, Group1 of ch.8 (refer to Chapter 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*


tSCYC
SCK
VOL
VOH
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
Master mode
VIH
VIL
VIH
VIL


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tR
tF
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
Slave mode
VIH
VIL
VIH
VIL

(2) Normal Synchronous Transfer (SCR:SPI=0) and Mark Level "L" of Serial Clock Output (SMR:SCINV=1)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Master Mode (CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	$3t_{CLK_LCPnA}$*1	-	ns	
		SCK2		$3t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$3t_{CLK_COMP}$	-		
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12, SOT0, SOT1, SOT3, SOT4, SOT8 to SOT12		-2	30	ns	
				-2	20*2		
		SCK2, SOT2		-2	20		
		SCK16 to SCK17, SOT16, SOT17		-2	15		
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12 SIN0, SIN1, SIN3, SIN4, SIN8 to SIN12		26.5	-	ns	
				20*2	-		
		SCK2, SCK16, SCK17 SIN2, SIN16, SIN17		20	-		
SCK ↓→ Valid SIN hold time	t_{SLIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		0	-	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Slave Mode (CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
SCK ↑→ SOT delay time	t_{SHOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		0	28.5	ns	
					25 *2		
		SCK16, SCK17 SOT16, SOT17		0	25		
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		10.0	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			1	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	

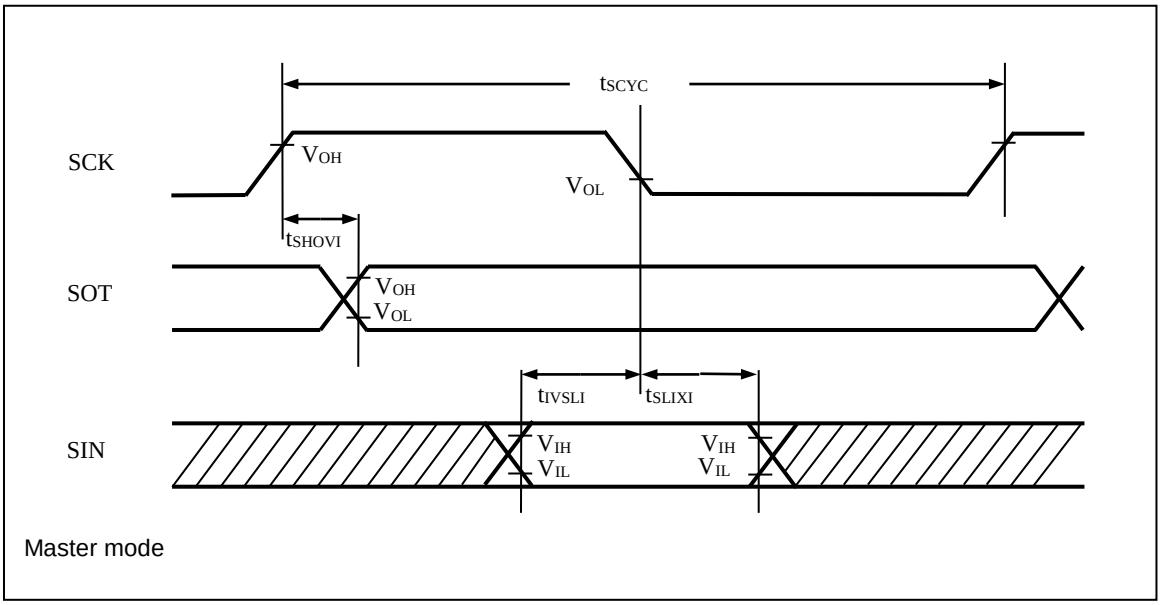
Notes:

*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12

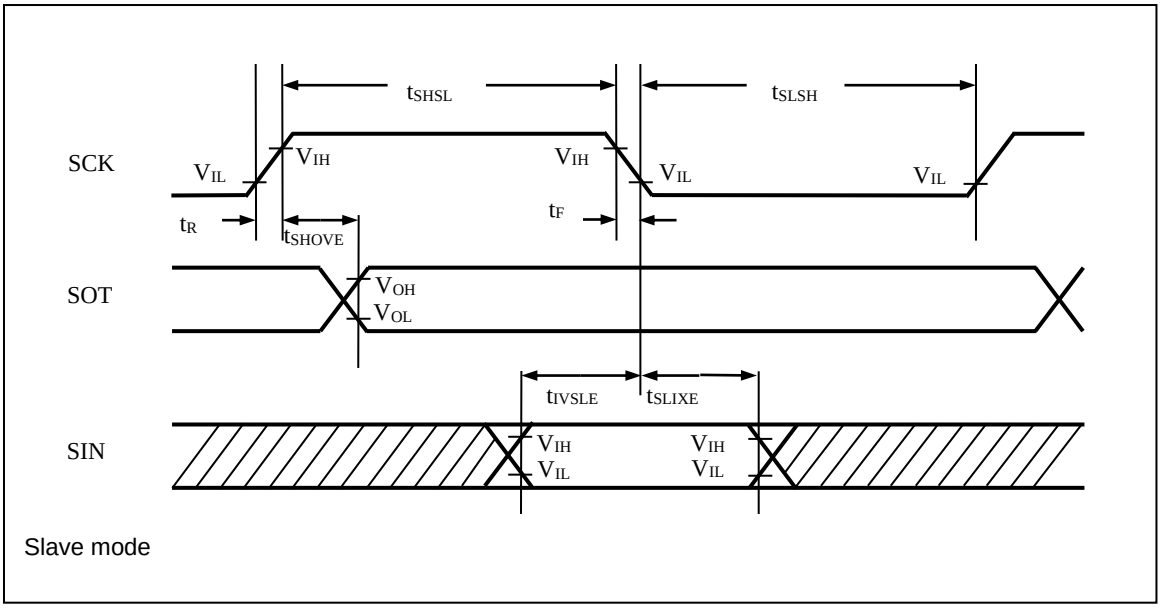
*2: Group2 of ch.0, ch1, Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*



Master mode



Slave mode

(3) SPI Supported (SCR:SPI=1), and Mark Level "H" of Serial Clock Output (SMR:SCINV=0)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Master Mode (CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	$3t_{CLK_LCPnA}$*1	-	ns	
		SCK2		$3t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$3t_{CLK_COMP}$	-		
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12, SOT0, SOT1, SOT3, SOT4, SOT8 to SOT12		-2	30	ns	
				-2	20*2		
		SCK2, SOT2		-2	20		
		SCK16 to SCK17, SOT16, SOT17		-2	15		
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12 SIN0, SIN1, SIN3, SIN4, SIN8 to SIN12		26.5	-	ns	
				20*2	-		
		SCK2, SCK16, SCK17 SIN2, SIN16, SIN17		20	-		
SCK ↓→ Valid SIN hold time	t_{SLIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		0	-	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12, SOT0, SOT1, SOT3, SOT4, SOT8 to SOT12		$2t_{CLK_LCPnA}$*1 -30	-	ns	
				$2t_{CLK_LCPnA}$ -20*2,3	-		
		SCK2, SOT2		$2t_{CLK_LCP0A}$ -20	-		
		SCK16, SCK17 SOT16, SOT17		$2t_{CLK_COMP}$*1 -15	-		

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Slave Mode (CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$			
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
SCK ↑→ SOT delay time	t_{SHOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		0	28.5	ns	
					25 *2		
		SCK16, SCK17 SOT16, SOT17		0	25		
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			1	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	

Notes:

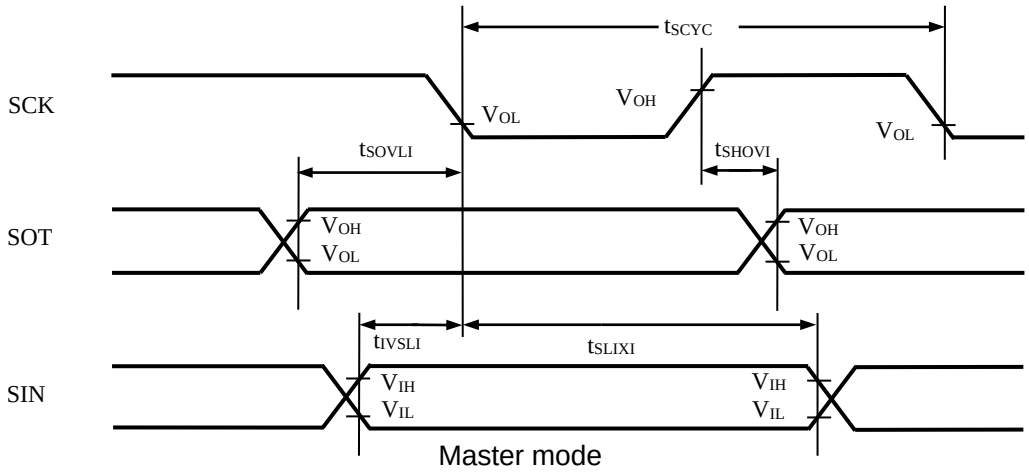
*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12

*2: Group2 of ch.0, ch1, Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

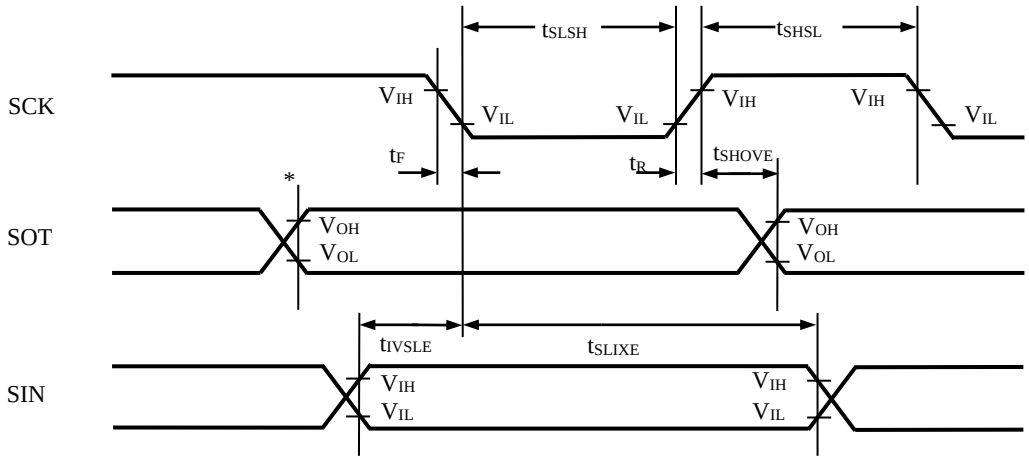
*3: n=0:Group2 of ch.0 /ch1,n=1:Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*



Master mode



* Changes when writing to the TDR register

Slave mode

(4) SPI Supported (SCR:SPI=1), and Mark Level "L" of Serial Clock Output (SMR:SCINV=1)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Master Mode (CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	$3t_{CLK_LCPnA}$*1	-	ns	
		SCK2		$3t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$3t_{CLK_COMP}$	-		
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12, SOT0, SOT1, SOT3, SOT4, SOT8 to SOT12		-2	30	ns	
				2	20*2		
		SCK2, SOT2		-2	20		
		SCK16 to SCK17, SOT16, SOT17		-2	15		
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12 SIN0, SIN1, SIN3, SIN4, SIN8 to SIN12		26.5	-	ns	
				20*2	-		
		SCK2, SCK16, SCK17 SIN2, SIN16, SIN17		20	-		
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		0	-	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12, SOT0, SOT1, SOT3, SOT4, SOT8 to SOT12		$2t_{CLK_LCPnA}$*1 -30	-	ns	
				$2t_{CLK_LCPnA}$ -20*2,3	-		
		SCK2, SOT2		$2t_{CLK_LCP0A}$ -20	-		
		SCK16, SCK17 SOT16, SOT17		$2t_{CLK_COMP}$*1 -15	-		

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12	Slave Mode (CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$			
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0, SCK1, SCK3, SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$ *1	-	ns	
		SCK2		$2t_{CLK_LCP0A}$	-		
		SCK16, SCK17		$2t_{CLK_COMP}$	-		
SCK ↓→ SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		0	28.5	ns	
					25 *2		
		SCK16, SCK17 SOT16, SOT17		0	25		
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16, SIN17		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			1	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12, SCK16, SCK17		-	5	ns	

Notes:

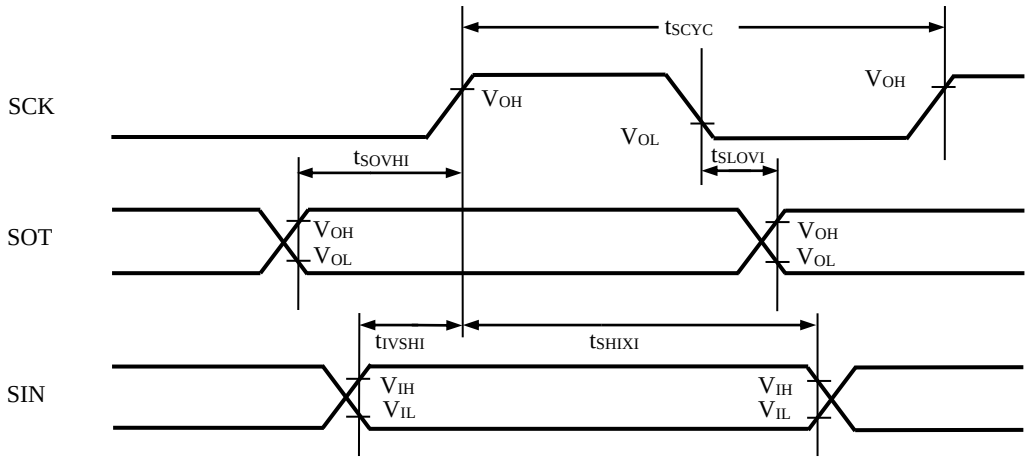
*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12

*2: Group2 of ch.0, ch1, Group1 of ch.8 (refer to Chapter 11: Port Configuration in the hardware manual)

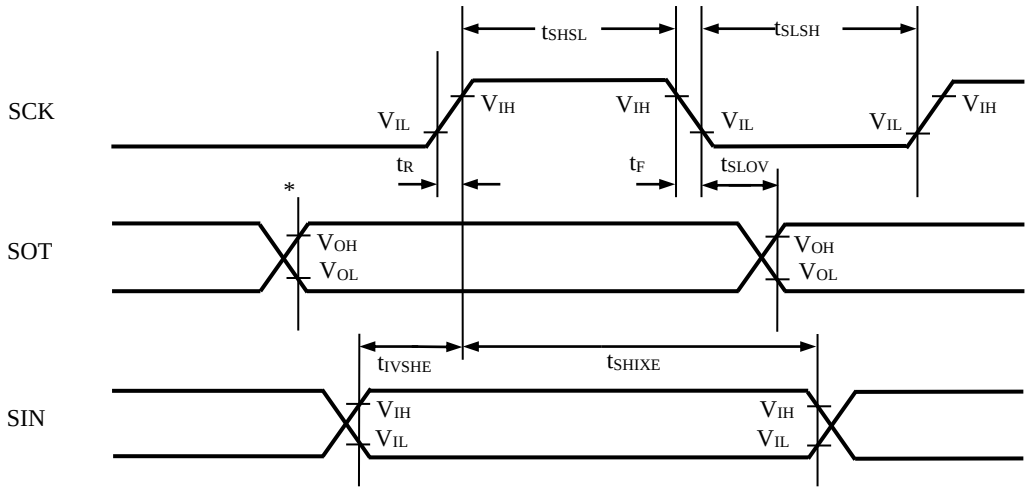
*3: n=0:Group2 of ch.0 /ch1,n=1:Group1 of ch.8 (refer to Chapter 11: Port Configuration in the hardware manual)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*



Master mode



* Changes when writing to the TDR register

Slave mode

(5) Mark Level "H" of Serial Clock Output (SMR:SCINV=0) and Mark Level "H" of Serial Chip Select (SCSCR:CSLVL=1)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↓ →SCK ↓ setup time	t_{CSSI}	Master mode (CL = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	-20*1	-	ns	
SCK ↑ →SCS ↑ hold time	t_{CSHI}		-3*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↓ →SCS ↓ clock change time	t_{SCC}	Round Function Master mode (CL = 20 pF I_{OL} =-5 mA, I_{OH} = 5 mA)	3tcp+0	3tcp+20	ns	

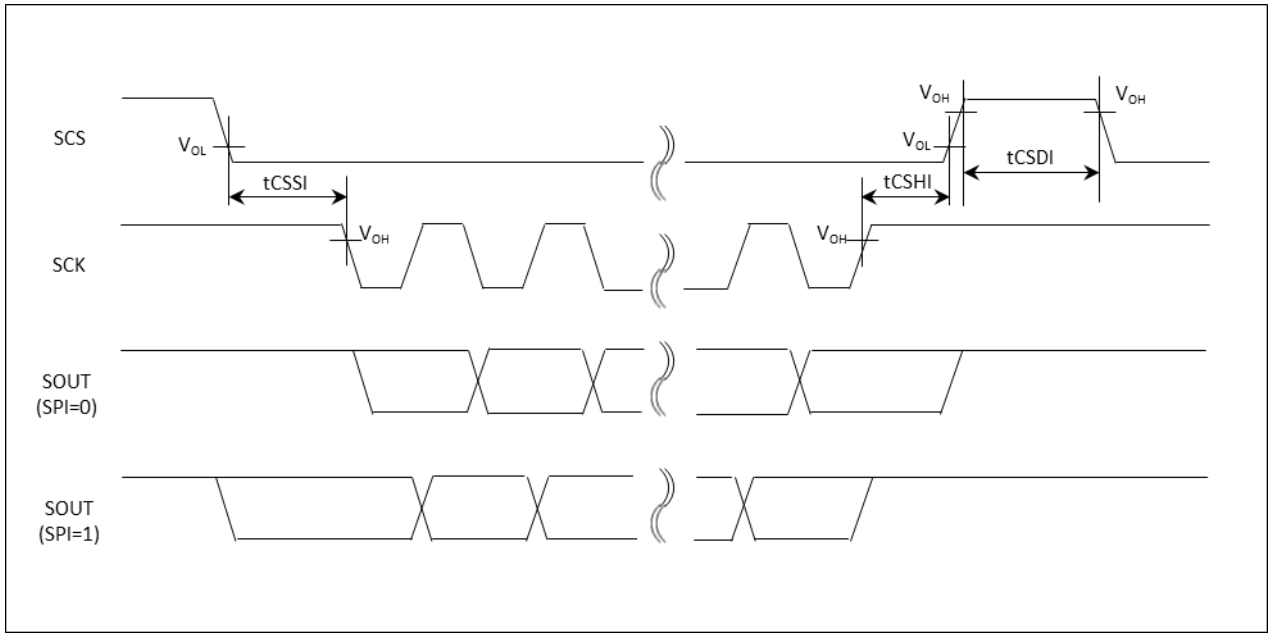
Notes:

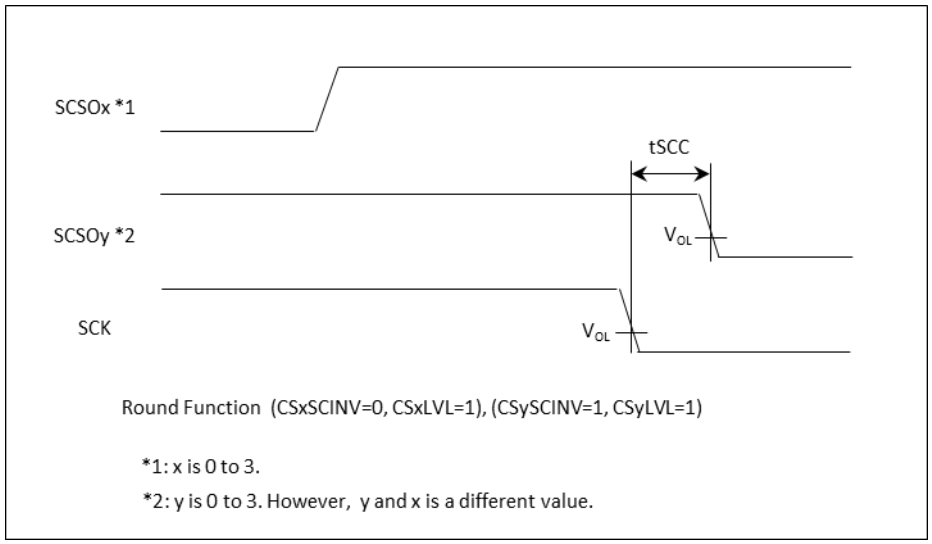
*1)SCSTR1.CSSU=0. tCSSI can be configured.

*2)SCSTR0.CSHD=0. tCSHI can be configured.

*3)SCSTR3/2.CSDS=0. tCSDI can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





(6) Mark Level "L" of Serial Clock Output (SMR:SCINV=1) and Mark Level "H" of Serial Chip Select (SCSCR:CSLVL=1)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↓ →SCK ↑ setup time	t_{CSSI}	Master mode (CL = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	-20*1	-	ns	
SCK ↓ →SCS ↑ hold time	t_{CSHI}		-3*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↑ →SCS ↓ clock change time	t_{SCC}	Round Function Master mode (CL = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	3tcp+0	3tcp+20	ns	

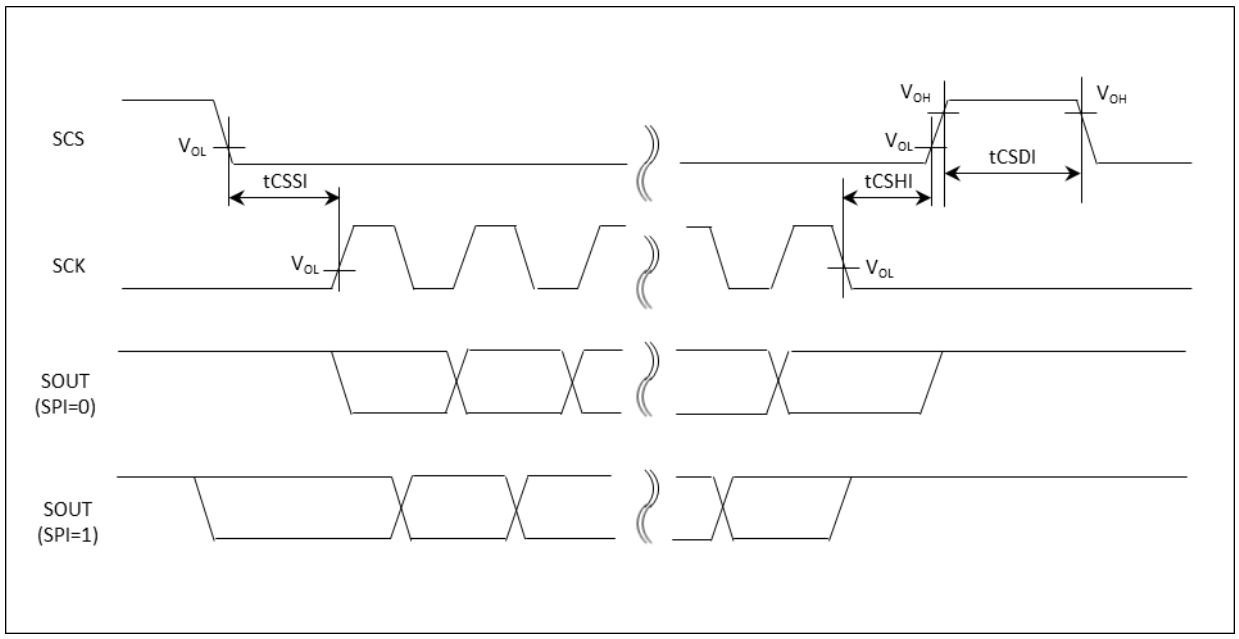
Notes

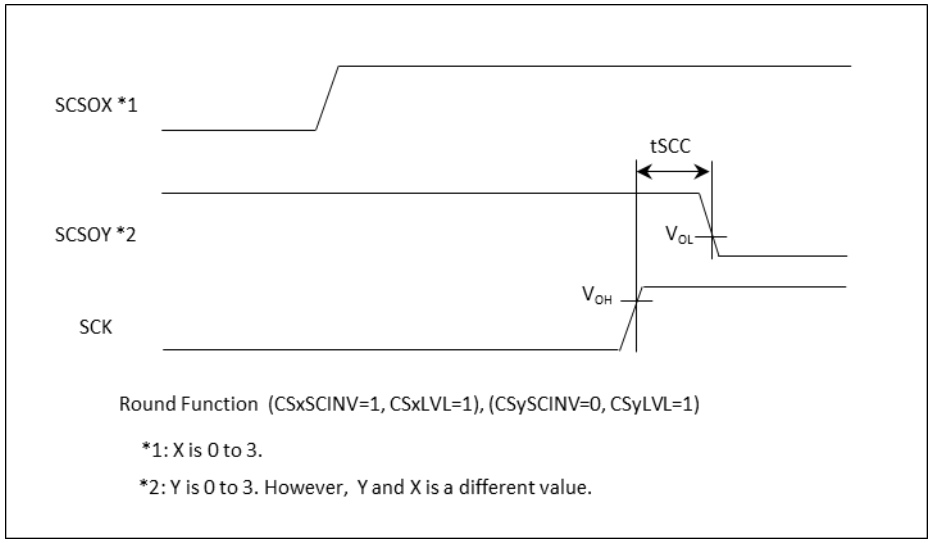
*1)SCSTR1.CSSU=0. tCSSI can be configured.

*2)SCSTR0.CSHD=0. tCSHI can be configured.

*3)SCSTR3/2.CSDS=0. tCSDI can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





Round Function (CSxSCINV=1, CSxLVL=1), (CSySCINV=0, CSyLVL=1)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.

(7) Mark Level "H" of Serial Clock Output (SMR:SCINV=0) and Mark Level "L" of Serial Chip Select (SCSCR:CSLVL=0)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↑ →SCK ↓ setup time	t_{CSSI}	Master mode (CL = 20 pF I_{OL} = -5 mA, I_{OH} = 5 mA)	-20*1	-	ns	
SCK ↑ →SCS ↓ hold time	t_{CSHI}		-3*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↓ →SCS ↑ clock change time	t_{SCC}	Round Function Master mode (CL = 20 pF I_{OL} = -5 mA, I_{OH} = 5 mA)	3tcp+0	3tcp+20	ns	

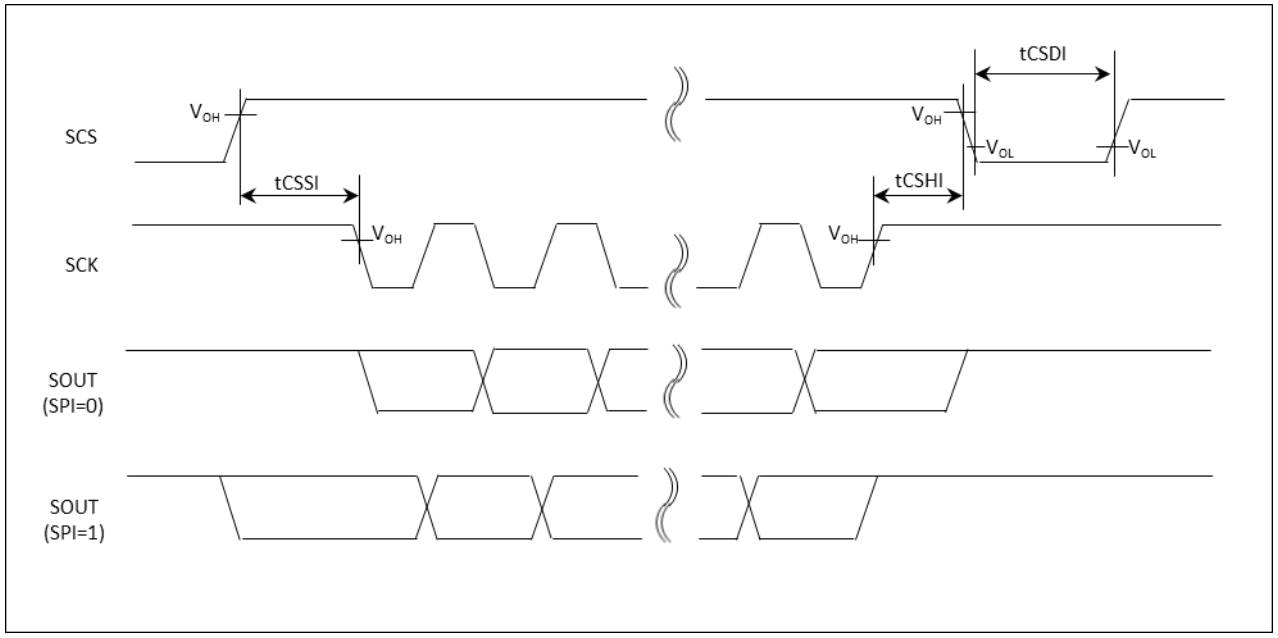
Notes:

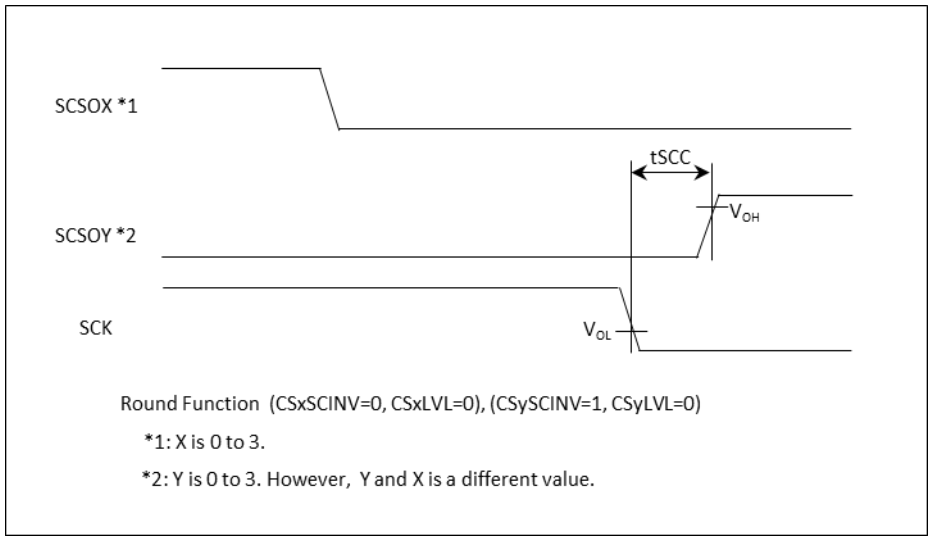
*1)SCSTR1.CSSU = 0. tCSSI can be configured.

*2)SCSTR0.CSHD = 0. tCSHI can be configured.

*3)SCSTR3/2.CSDS = 0. tCSDI can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





Round Function (CSxSCINV=0, CSxLVL=0), (CSySCINV=1, CSyLVL=0)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.

(8) Mark Level "L" of Serial Clock Output (SMR:SCINV=1) and Mark Level "L" of Serial Chip Select (SCSCR:CSLVL=0)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↑ →SCK ↑ setup time	t_{CSSI}	Master mode (CL = 20 pF I_{OL} = -5 mA, I_{OH} = 5 mA)	-20*1	-	ns	
SCK ↓ →SCS ↓ hold time	t_{CSHI}		-3*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↑ →SCS ↑ clock change time	t_{SCC}	Round Function Master mode (CL = 20 pF I_{OL} = -5 mA, I_{OH} = 5 mA)	3tcp+0	3tcp+20	ns	

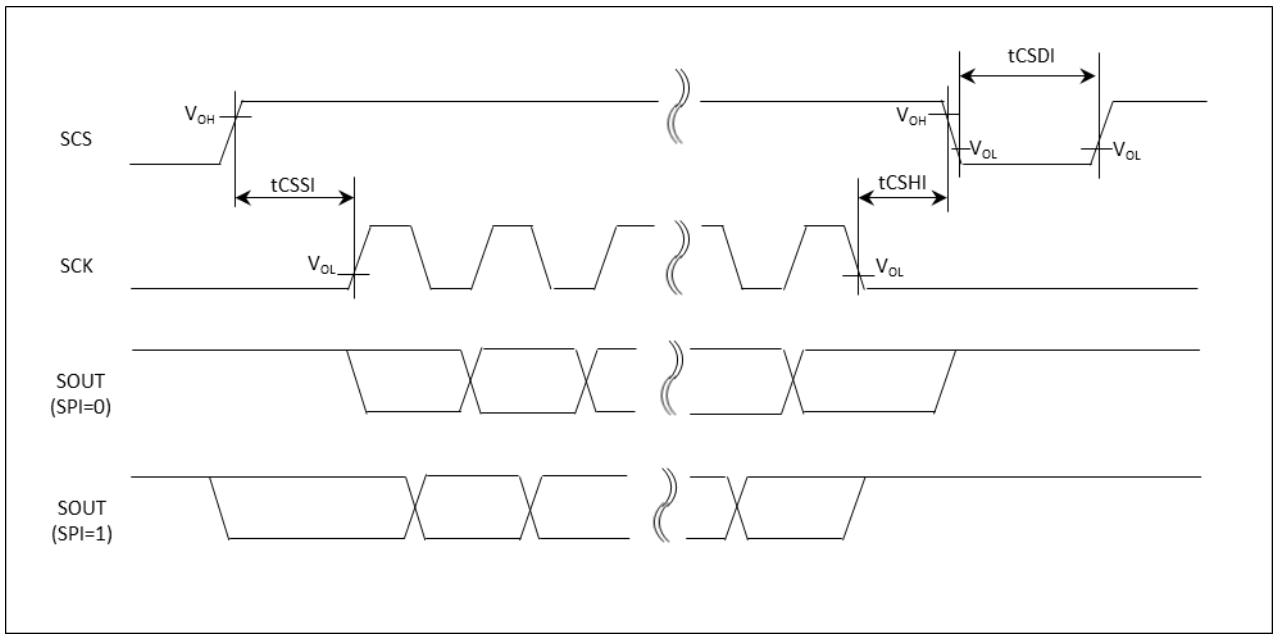
Notes:

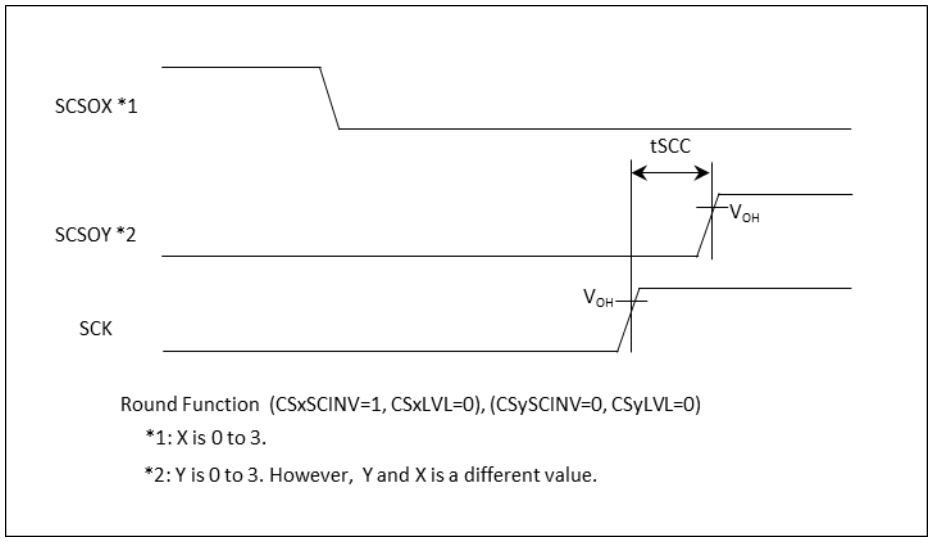
*1)SCSTR1.CSSU=0. tCSSI can be configured.

*2)SCSTR0.CSHD=0. tCSHI can be configured.

*3)SCSTR3/2.CSDS=0. tCSDI can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





Round Function (CSxSCINV=1, CSxLVL=0), (CSySCINV=0, CSyLVL=0)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.

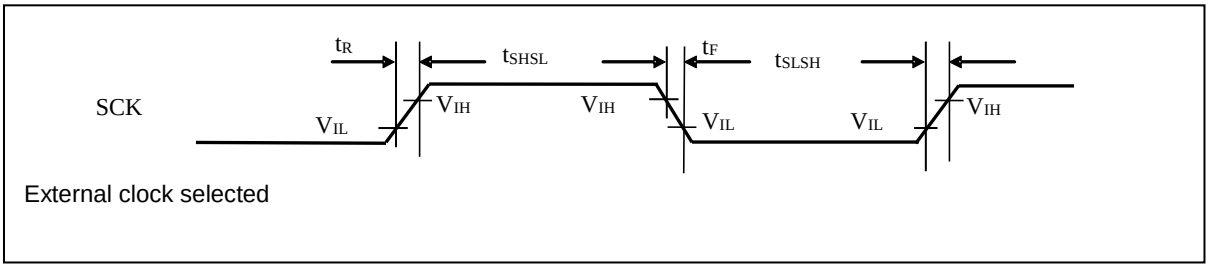
8.4.7.3 LIN Interface (v2.1) (LIN Communication Control Interface (v2.1)) Timing (SMR:MD2-0=0b011)

(1) External Clock Selected (BGR:EXT=1)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12	(CL = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (CL=20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	t_{CLK_LCPnA}*1+10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12		t_{CLK_LCPnA}*1+10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	
SCK rising time	t_R			-	5	ns	

*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12



External clock selected

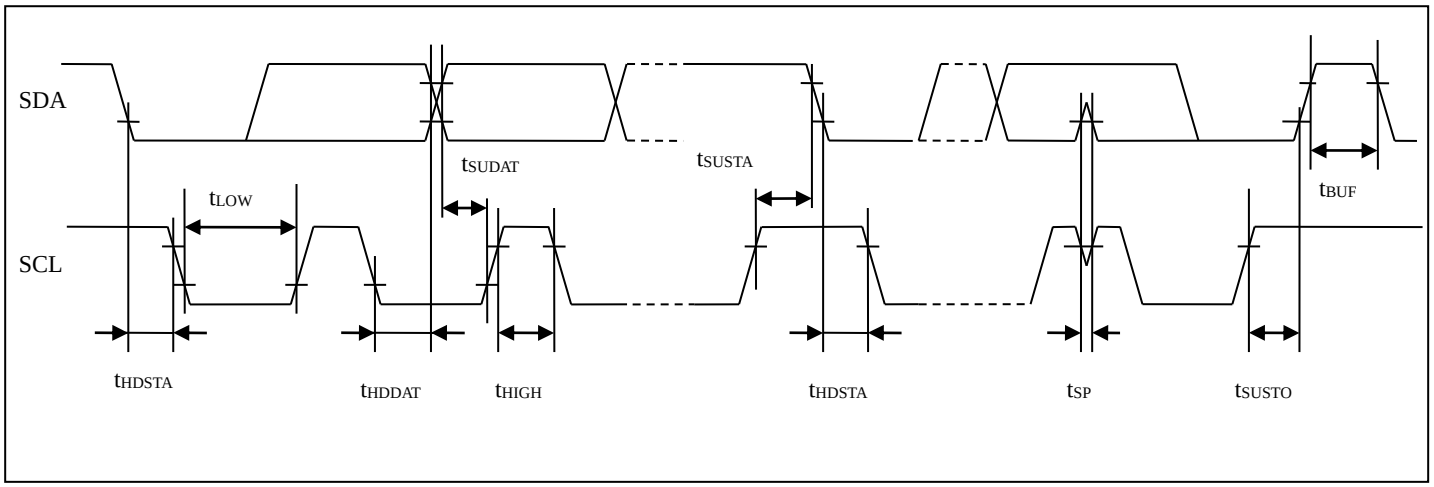
8.4.7.4 I^2C Timing (SMR:MD2-0=0b100)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Fast Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCL4, 10, 12, 16, and 17	(CL = 50 pF, I_{OL} = -2 mA, I_{OH} = 2 mA), (CL = 20 pF, I_{OL} = -1 mA, I_{OH} = 1 mA)	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		4.0	-	0.6	-	µs	
Period of "L" for SCL clock	t_{LOW}	SCL4, 10, 12, 16, and 17		4.7	-	1.3	-	µs	
Period of "H" for SCL clock	t_{HIGH}	SCL4, 10, 12, 16, and 17		4.0	-	0.6	-	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		0	3.45*1	0	0.9*2	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		250	-	100	-	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16 and 17		4.0	-	0.6	-	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	-		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-		$2t_{CLK_COMP}$	-	$2t_{CLK_COMP}$	-	ns	

Notes:

- **1: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.*
- **2: A fast mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".*
- *SCL4, 10, 12 and SDA4, 10, 12 only support the standard mode.*


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

8.4.8 Timer Input

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TWH}, t_{TWL}	PPG0_TIN1 to PPG11_TIN1	-	$4t_{CLK_LCPnA}$*1	-	ns	$4t_{CLK_LCPnA}$*1 ≥ 100 ns
				100			$4t_{CLK_LCPnA}$*1 < 100 ns
		ICU0_IN0 to ICU11_IN0, ICU0_IN1 to ICU11_IN1	-	$4t_{CLK_LCPnA}$*2	-	ns	$4t_{CLK_LCPnA}$*2 ≥ 100 ns
				100			$4t_{CLK_LCPnA}$*2 < 100 ns
		FRT0_TEXT to FRT11_TEXT	-	$4t_{CLK_LCPnA}$*2	-	ns	$4t_{CLK_LCPnA}$*2 ≥ 100 ns
				100			$4t_{CLK_LCPnA}$*2 < 100 ns
		TIN0 to TIN3, TIN16 to TIN19	-	$4t_{CLK_LCPnA}$*3	-	ns	$4t_{CLK_LCPnA}$*3 ≥ 100 ns
				100			$4t_{CLK_LCPnA}$*3 < 100 ns
		TIN32 to TIN35	-	$4t_{CLK_LLPBM2}$	-	ns	$4t_{CLK_LLPBM2}$ ≥ 100 ns
				100			$4t_{CLK_LLPBM2}$ < 100 ns
		TIN48 to TIN49	-	$4t_{CLK_COMP}$	-	ns	$4t_{CLK_COMP}$ ≥ 100 ns
				100			$4t_{CLK_COMP}$ < 100 ns

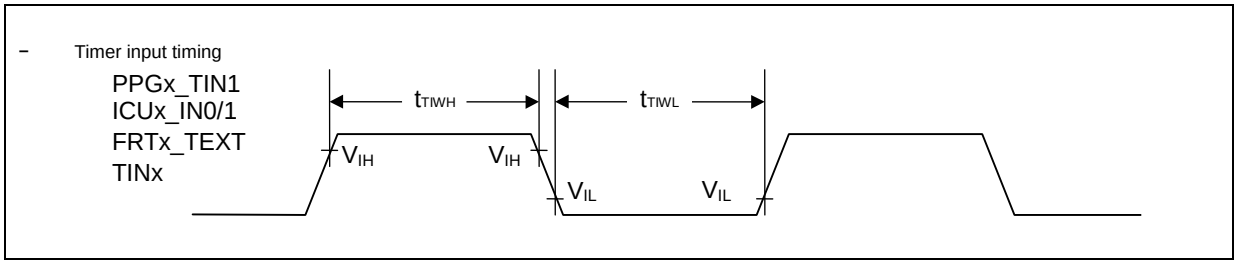
Notes:

*1: n = 0:ch.0 to ch.5, n = 1:ch.6 to ch.11

*2: n = 0:ch.0 to ch.7, n = 1:ch.8 to ch.11

*3: n = 0:ch.0 to ch.3, n = 1:ch.16 to ch.19

- Timer input timing

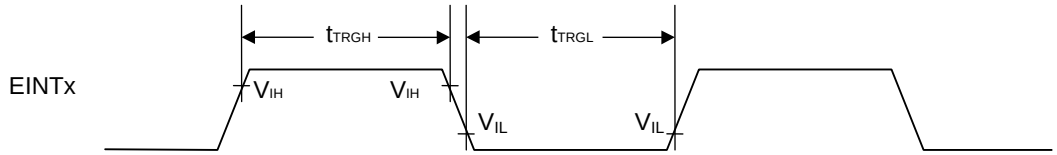


8.4.9 Trigger Input

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	EINT0 to EINT15	-	100	-	ns	

- Trigger input timing

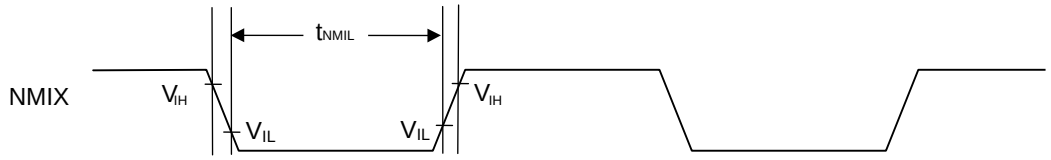


8.4.10 NMI Input

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	300	-	ns	

- NMIX input timing



8.4.11 Low-Voltage Detection

8.4.11.1 LVDL0

(Condition: See 8.2. Operation Assurance)

Parameter	Pin Name	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detection Voltage	-	-	0.9	0.95	1.0	V	*1
Release Voltage	-	-	0.925	1.025	1.125	V	
Level Detection Time	-	-	-	-	30	µs	*2

Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*

8.4.11.2 LVDH0

Note:

LVDH0 is only used to generate power-on reset. Refer to Power-On Conditions for related parameters.

8.4.11.3 LVDL1

(Condition: See 8.2. Operation Assurance)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU Operation Range	Remarks
			Min	Typ	Max			
Detection Voltage	-	LVDL1V = 10 (Default)	0.92	0.97	1.02	V	No	*1
Release Voltage	-		0.945	1.045	1.145	V		
Detection Voltage	-	LVDL1V = 11	1.02	1.07	1.12	V		
Release Voltage	-		1.095	1.145	1.195	V		
Detection Time	-	-	-	-	30	µs	-	*2

Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below the minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*

8.4.11.4 LVDH1

(Condition: See 8.2. Operation Assurance)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU Operation Range	Remarks
			Min	Typ	Max			
Supply Voltage Range	$V_{CC}5$	-	4.5	-	5.5	V		-
Detection Voltage	$V_{CC}5$	LVDH1V = 0000	2.20	2.35	2.50	V	No	*1
Release Voltage	$V_{CC}5$		2.30	2.45	2.60	V		
Detection Voltage	$V_{CC}5$	LVDH1V = 0001	2.60	2.75	2.90	V		
Release Voltage	$V_{CC}5$		2.70	2.85	3.00	V		
Detection Voltage	$V_{CC}5$	LVDH1V = 0010	2.70	2.85	3.00	V		
Release Voltage	$V_{CC}5$		2.80	2.95	3.10	V		
Detection Voltage	$V_{CC}5$	LVDH1V = 0011	3.40	3.60	3.80	V		
Release Voltage	$V_{CC}5$		3.50	3.70	3.90	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0100	3.60	3.80	4.00	V	Yes	-
Release Voltage	$V_{CC}5$		3.70	3.90	4.10	V		
Detection Voltage	$V_{CC}5$	LVDH1V = 0101	3.80	4.00	4.20	V		
Release Voltage	$V_{CC}5$		3.90	4.10	4.30	V		
Detection Voltage	$V_{CC}5$	LVDH1V = 0110 (Default)	4.00	4.20	4.40	V		
Release Voltage	$V_{CC}5$		4.10	4.30	4.50	V		
Detection Voltage	$V_{CC}5$	LVDH1V = 0111	4.20	4.40	4.60	V		
Release Voltage	$V_{CC}5$		4.30	4.50	4.70	V		
Detection Voltage	$V_{CC}5$	LVDH1V = Other	4.40	4.65	4.90	V		
Release Voltage	$V_{CC}5$		4.50	4.75	5.00	V		
Detection Time	-	-	-	-	30	µs		*2
Power supply voltage regulation	$V_{CC}5$	-	-2	-	2	V/ms		*3

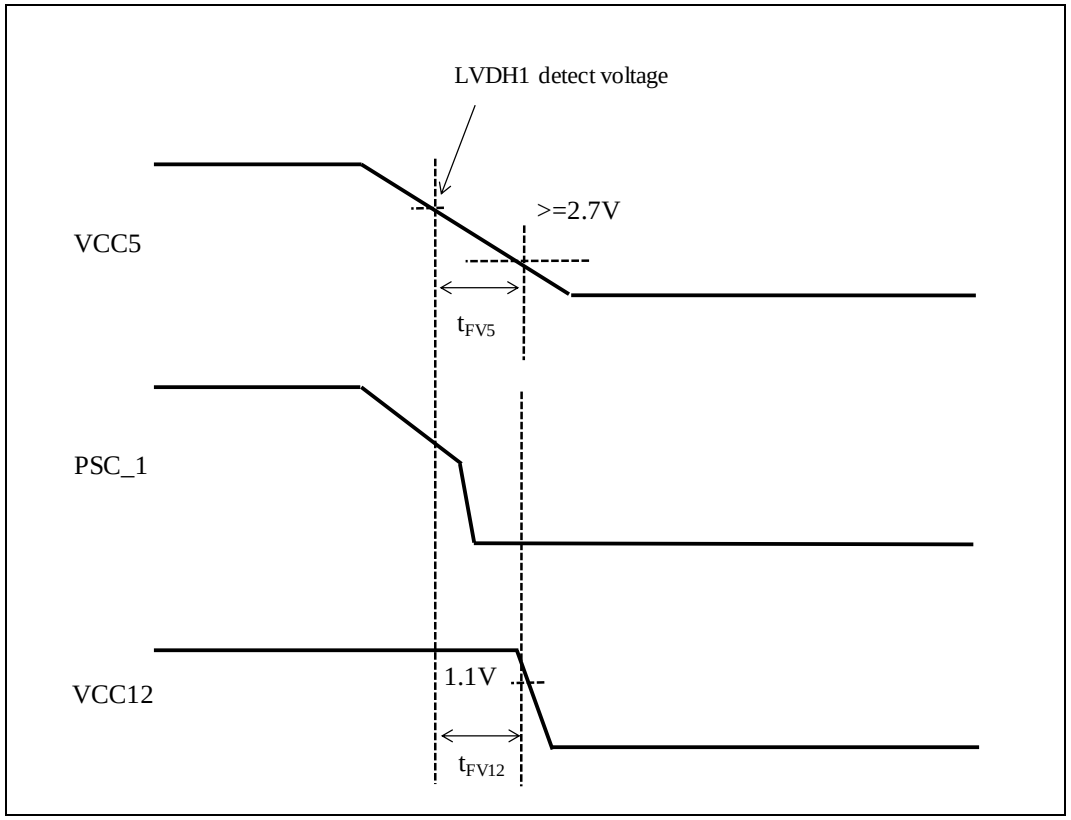
Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (3.5 V).*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*
- **3: Suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage.*

- *Following power supply voltage stability conditions need to be ensured*

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
VCC5 stability time after LVDH1 low voltage detection	t_{FV5}	VCC5	-	55	-	µs	VCC5 ≥ 2.7 V
VCC12 stability time after LVDH1 low voltage detection	t_{FV12}	VCC12		55	-	µs	VCC12 ≥ 1.1 V



** : The behavior of PSC_1 depends on EXVRSTCNT bit. If the bit is set to "1", PSC_1 keeps 'H' level.*

8.4.11.5 LVDL2

(Condition: See 8.2. Operation Assurance)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU operation range	Remarks
			Min	Typ	Max			
Supply Voltage Range	$V_{CC}12$	-	1.1	-	1.3	V	-	-
Detection Voltage	$V_{CC}12$	LVDL2V = 00 (Default)	0.72	0.77	0.82	V	No	*1

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU operation range	Remarks
			Min	Typ	Max			
Release Voltage	$V_{CC}12$		0.795	0.845	0.895	V		
Detection Voltage	$V_{CC}12$	LVDL2V = 01	0.82	0.87	0.92	V		
Release Voltage	$V_{CC}12$		0.895	0.945	0.995	V		
Detection Voltage	$V_{CC}12$	LVDL2V = 10	0.92	0.97	1.02	V		
Release Voltage	$V_{CC}12$		0.995	1.045	1.095	V		
Detection Voltage	$V_{CC}12$	LVDL2V = 11	1.02	1.07	1.12	V		
Release Voltage	$V_{CC}12$		1.095	1.145	1.195	V		
Detection Time	-	-	-	-	30	µs	-	*2

Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (1.1 V).*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*

8.4.11.6 LVDH2

(Condition: See 8.2. Operation Assurance)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU operation range	Remarks
			Min	Typ	Max			
Supply Voltage Range	$V_{CC}3$	-	3.0	-	3.6	V	-	-
Detection Voltage	$V_{CC}3$	LVDH2V = 0000 (Default)	2.2	2.35	2.5	V	No	*1
Release Voltage	$V_{CC}3$		2.3	2.45	2.6	V		
Detection Voltage	$V_{CC}3$	LVDH2V = 0001	2.6	2.75	2.9	V		
Release Voltage	$V_{CC}3$		2.7	2.85	3.0	V		
Detection Voltage	$V_{CC}3$	LVDH2V = 0010	2.7	2.85	3.0	V	Yes	-
Release Voltage	$V_{CC}3$		2.8	2.95	3.1	V		
Detection Time	-	-	-	-	30	µs	-	*2
Power supply voltage regulation	$V_{CC}5$	-	-2	-	2	V/ms	-	*3

Notes:

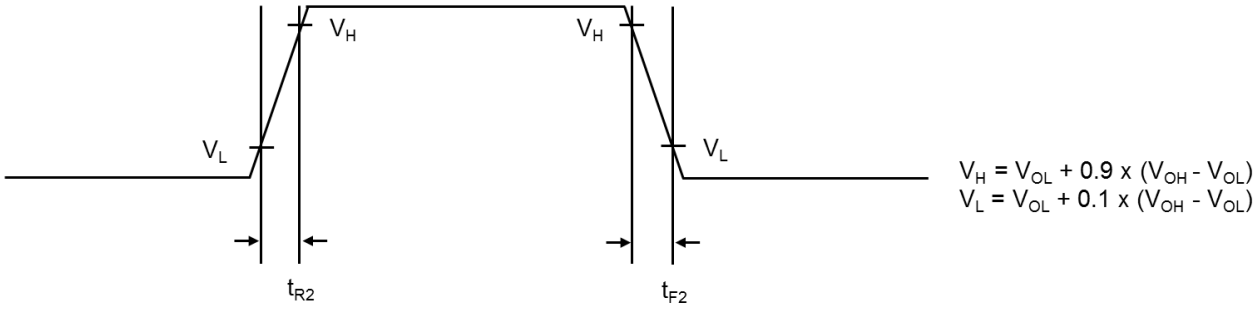
- **1: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7 V).*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*
- **3: Suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage.*

8.4.12 High Current Output Slew Rate

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise / fall time	t_{R2},t_{F2}	P3_21 to 31, P4_00 to 12	-	15	-	100	ns	Load capacitance 85 pF

・Slew rate output timing



8.4.13 Display Controller

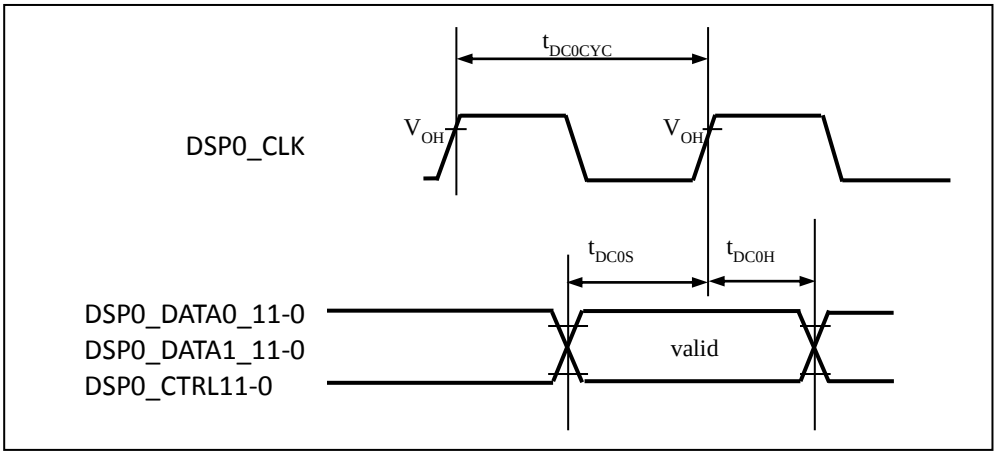
8.4.13.1 Display Controller0 Timing (TTL Mode)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Cycle	t_{DC0CYC}	DSP0_CLK	(CL = 20 pF, I_{OL} = -10 mA, I_{OH} = 10 mA)	15.625	-	ns	*1
				20	-	ns	*2
Data/Control output to DSP0_CLK time	t_{DC0S}	DSP0_DATA0_11-0 DSP0_DATA1_11-0 DSP0_CTRL4-0		t_{DCOCYC} – 8	-	ns	Pins in VCC3 domain
DSP0_CLK to Data/Control valid time	t_{DC0H}			-0.5	-	ns	
Data/Control output to DSP0_CLK time	t_{DC0S}	DSP0_CTRL11-0	(CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA)	t_{DCOCYC} – 9.3	-	ns	If any of DSP0_CTRL11-0 in VCC53 domain is used
DSP0_CLK to Data/Control valid time	t_{DC0H}			-1	-	ns	

Notes:

- *For *1, when used with DSP0_DATA* and DSP0_CTRL4-0 in the VCC3 area.*
- *For *2, when used with DSP0_CTRL11-0 in the VCC53 area.*
- *Values valid for unshifted display clock (dsp_ClockInvert=0, dsp_ClockShift=0).*
- *The clock output delay can be adjusted. See the "Graphic Subsystem" chapter in the TRM for details*



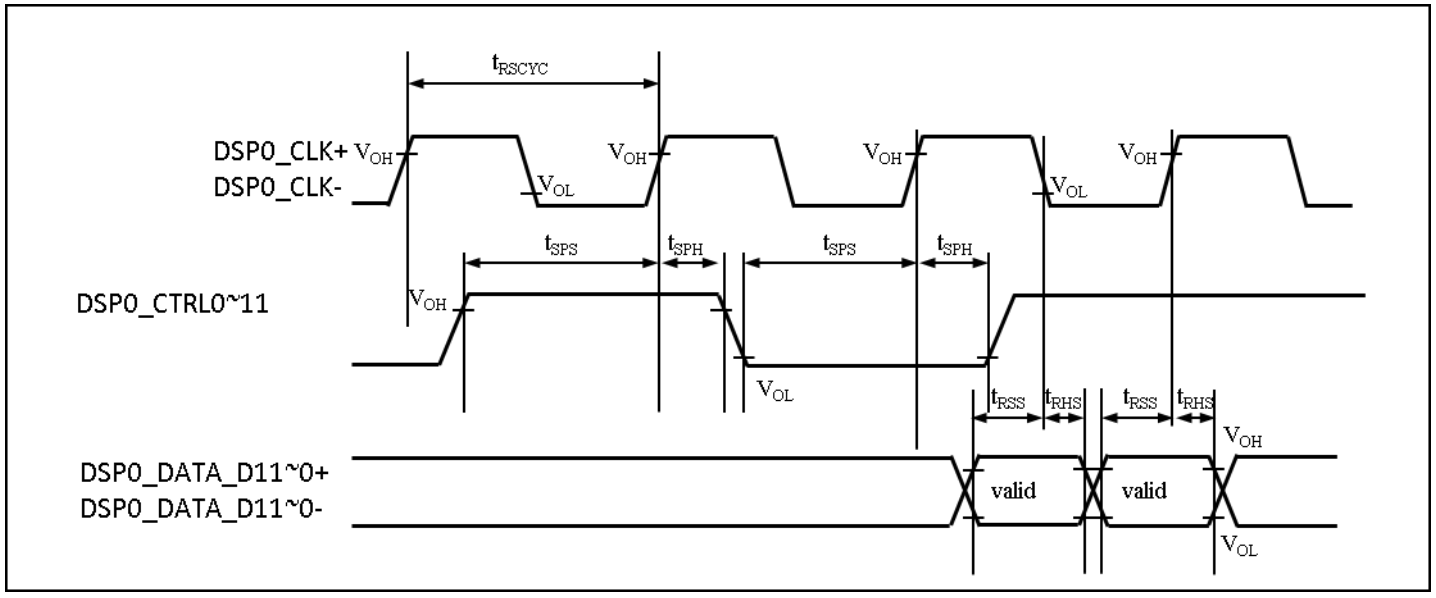
8.4.13.2 Display Controller0 Timing (RSDS)

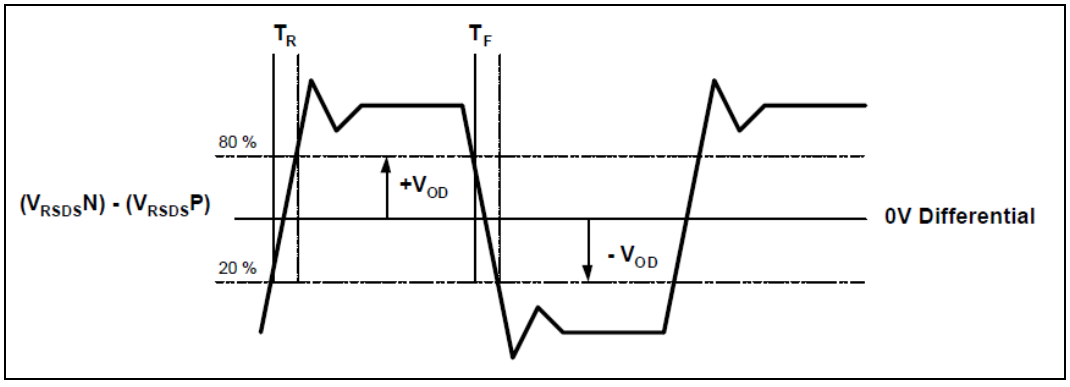
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Cycle	t_{RSCYC}	DSP0_CLK+ DSP0_CLK-	(CL = 20 pF, I_{OL} = -4 mA, I_{OH} = 4 mA)	15.625	-	ns	
Data output to DSP0_CLK time	t_{RSS}	DSP0_DATA_D11~0+ DSP0_DATA_D11~0-		$t_{RSCYC}/2$ – 5.7	-	ns	
DSP0_CLK to Data valid time	t_{RSH}			-0.1	-	ns	
Control output to DSP0_CLK time	t_{SPS}	DSP0_CTRL11~0		t_{RSCYC} – 9.5	-	ns	
DSP0_CLK to Control valid time	t_{SPH}			0.4	-	ns	

Note:

- *The clock output delay can be adjusted. See the "Graphic Subsystem" chapter in the TRM for details*
- *Values valid for unshifted display clock (dsp_ClockInvert=0, dsp_ClockShift=0).*





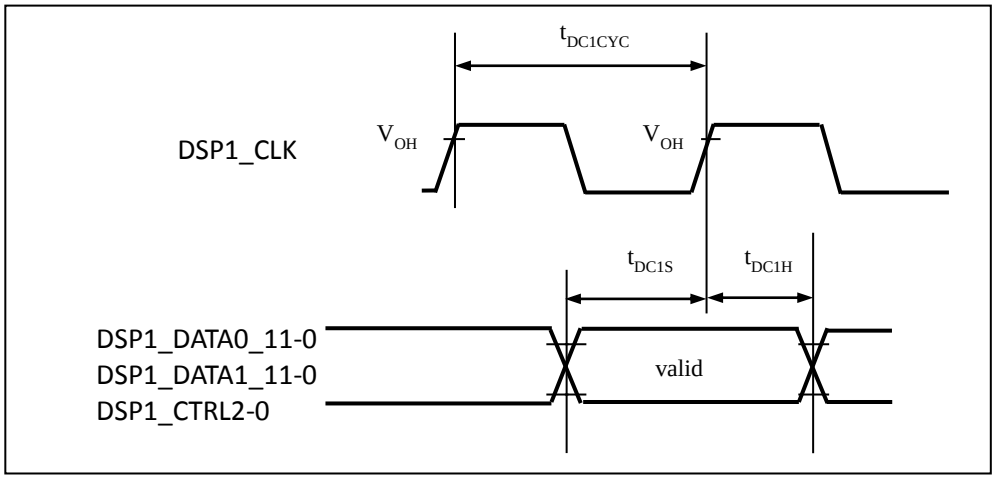
8.4.13.3 Display Controller1 Timing

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Cycle	t_{DC1CYC}	DSP1_CLK	(CL = 20 pF, IOL=-5 mA, IOH=5 mA)	20.0	-	ns	
Data/Control output to DSP1_CLK time	t_{DC1S}	DSP1_DATA0_11-0 DSP1_DATA1_11-0 DSP1_CTRL2-0		t_{DC1CYC} – 4.6	-	ns	
DSP1_CLK to Data/Control valid time	t_{DC1H}			-6	-	ns	

Notes:

- *The clock output delay can be adjusted. See the "Graphic Subsystem" chapter in the TRM for details*
- *Values valid for unshifted display clock (dsp_ClockInvert=0, dsp_ClockShift=0).*

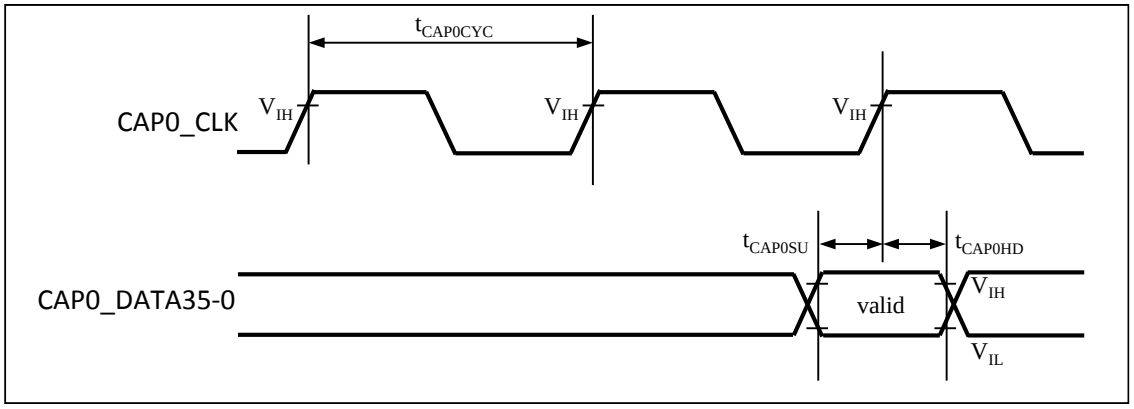


8.4.14 Video Capture

8.4.14.1 Video Capture Timing

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Cycle	$t_{CAP0CYC}$	CAP0_CLK	-	12.5	-	ns	
Capture data setup time	t_{CAP0SU}	CAP0_DATA35~0		4.0	-	ns	
Capture data hold time	t_{CAP0HD}	CAP0_DATA35~0		1.0	-	ns	



8.4.15 FPD-Link (LVDS)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Output clock frequency	f	-	5	-	50	MHz	
Differential output voltage	V_{OD}	R_L = 100 Ω C_L = 5 pF (differential)	210	300	390	mV	One of three is selectable
			250	350	450	mV	
			295	400	505	mV	
Variation of V_{OD}	delta V_{OD}		-	-	25	mV	
Common mode voltage	V_{CM}		1.075	1.200	1.325	V	One of two is selectable
			1.125	1.250	1.375	V	
Variation of V_{CM}	delta V_{CM}		-	-	25	mV	
Cycle time of TXCLKP/M	T_{CIP}	-	20	T	200	ns	Equals 1/f
Duty of TXCLKP/M	T_{CDT}	-	-	4/7 * T	-	ns	
Internal PLL lockup time	T_{PLLL}	-	-	-	10	ms	
Cycle-to-cycle jitter	T_{C2C}	-	-	-	0.11 * T / 7	ns	
Channel-to-Channel skew of TXOUTxP/M	T_{CSK}	-	-	-	200	ps	
Skew of TXOUTxP and TXOUTxM	T_{DSK}	-	-	-	50	ps	
Output pulse position for bit 0	T_0	f = 50 MHz	-0.235	0	+0.235	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -0.235	1 / 7 x T	1 / 7 x T +0.235	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.235	2 / 7 x T	2 / 7 x T +0.235	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -0.235	3 / 7 x T	3 / 7 x T +0.235	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.235	4 / 7 x T	4 / 7 x T +0.235	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.235	5 / 7 x T	5 / 7 x T +0.235	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.235	6 / 7 x T	6 / 7 x T +0.235	ns	
Output pulse position for bit 0	T_0	f = 40 MHz	-0.25	0	+0.25	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -0.25	1 / 7 x T	1 / 7 x T +0.25	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.25	2 / 7 x T	2 / 7 x T +0.25	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -0.25	3 / 7 x T	3 / 7 x T +0.25	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.25	4 / 7 x T	4 / 7 x T +0.25	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.25	5 / 7 x T	5 / 7 x T +0.25	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.25	6 / 7 x T	6 / 7 x T +0.25	ns	
Output pulse position for bit 0	T_0	f = 25 MHz	-0.45	0	+0.45	ns	

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Output pulse position for bit 1	T_1		1 / 7 x T -0.45	1 / 7 x T	1 / 7 x T +0.45	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.45	2 / 7 x T	2 / 7 x T +0.45	ns	
Output pulse position for bit 3	T_3		3 / 7 x T - 0.45	3 / 7 x T	3 / 7 x T +0.45	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.45	4 / 7 x T	4 / 7 x T +0.45	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.45	5 / 7 x T	5 / 7 x T +0.45	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.45	6 / 7 x T	6 / 7 x T +0.45	ns	
Output pulse position for bit 0	T_0	f = 5 MHz	-2.00	0	+2.00	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -2.00	1 / 7 x T	1 / 7 x T +2.00	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -2.00	2 / 7 x T	2 / 7 x T +2.00	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -2.00	3 / 7 x T	3 / 7 x T +2.00	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -2.00	4 / 7 x T	4 / 7 x T +2.00	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -2.00	5 / 7 x T	5 / 7 x T +2.00	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -2.00	6 / 7 x T	6 / 7 x T +2.00	ns	

Notes:

- *All the corresponding ports of products, which do not support FPD-Link, should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-, TxCLK+/-.*
- *Channel-to-Channel skew of TXOUTxP/M is included in output pulse position.*

Figure 8-5: LVDS AC Timing Chart

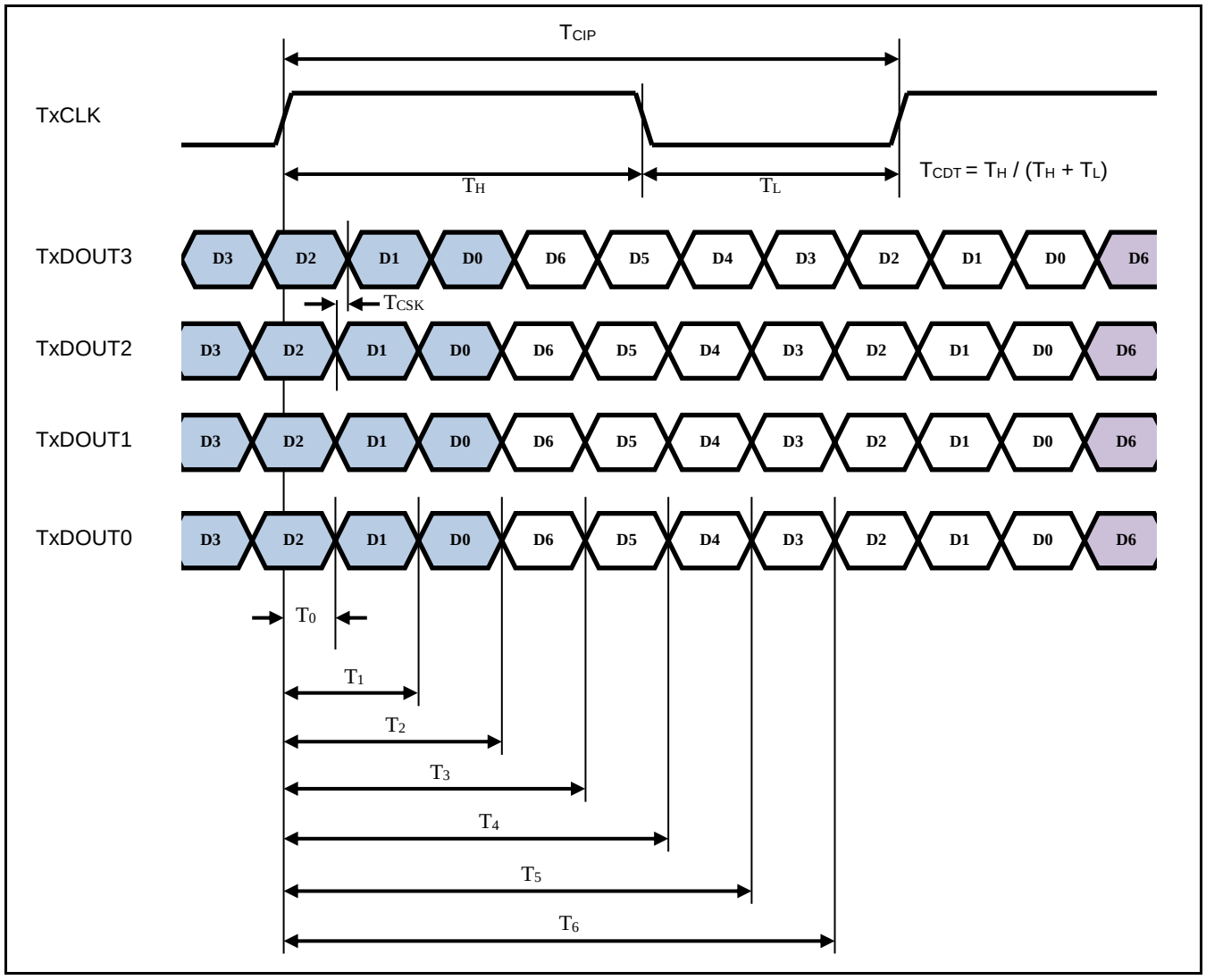
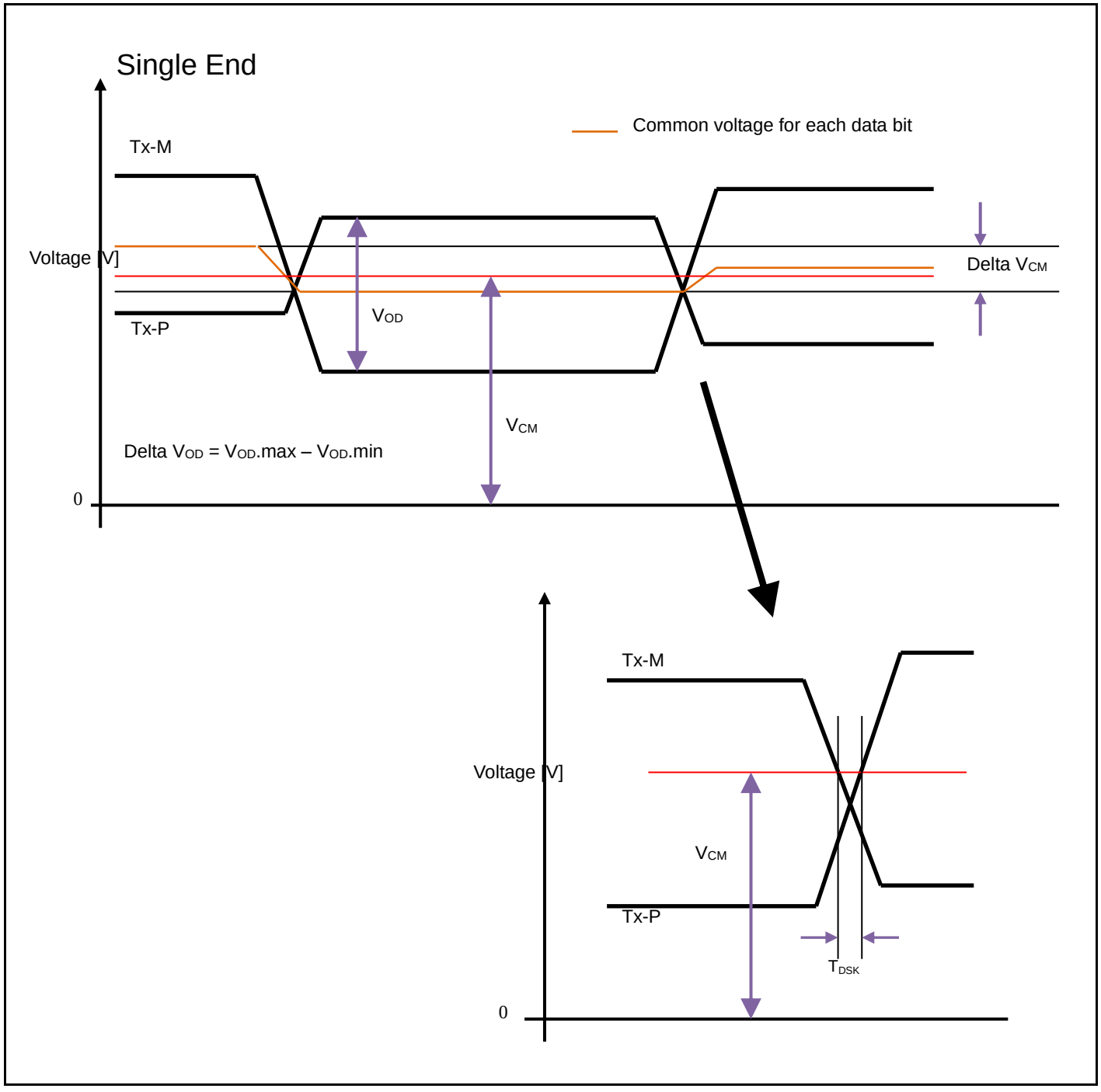


Figure 8-6: LVDS AC Timing Chart



8.4.16 DDR-HSSPI

The DDR-HSSPI AC characteristics are specified with the specific reference voltage of V_{IL}, V_{IH}, V_{OL}, V_{OH} = 0.5 Vcc3 as mentioned in Section 8.4.3, regardless of automotive input-level configuration, CMOS Schmitt, and TTL.

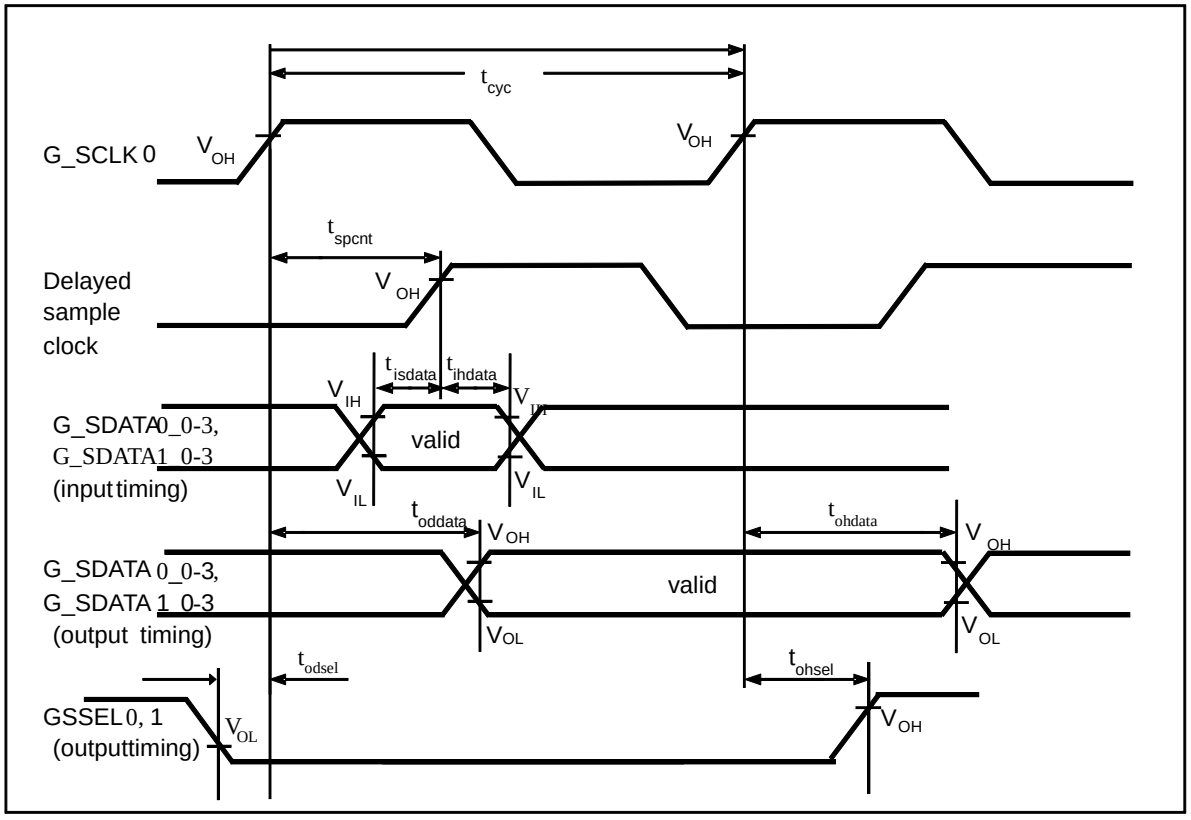
8.4.16.1 DDR-HSSPI Interface Timing (SDR Mode)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
HSSPI clock cycle	t_{cyc}	G_SCLK0 M_SCLK0	(CL = 20 pF, I_{OL} = -10 mA, I_{OH} = 10 mA),	10	-	ns	
				20	-		During Quad Page mode or Dual Quad mode
GSDATA -> G_SCLK↑ Input setup time	t_{isdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑ -> GSDATA Input hold time	t_{ihdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑ -> GSDATA Output delay time	t_{oddata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		-	tcyc/2 + 1.5	ns	
G_SCLK↑ -> GSDATA Output hold time	t_{ohdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		tcyc/2 – 2.5	-	ns	
GSSEL↓ -> G_SCLK↑ Output delay time	t_{odsel}	G_SSEL0, 1 M_SSEL0, 1		(SS2CD+ 0.5)*tcyc -3	-	ns	
G_SCLK↑ -> GSSEL↑ Output hold time	t_{ohsel}	G_SSEL0, 1 M_SSEL0, 1		2.5 * tcyc – 1.5	-	ns	

Notes:

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured. The delay should not exceed t_{cyc}.*


t cyc
G_SCLK 0
V OH
V OH
t spcnt
Delayed
sample
clock
V OH
t isdata
t ihdata
V IH
V IH
G_SDATA0_0-3,
G_SDATA1_0-3
(input timing)
valid
V IL
V IL
t oddata
t ohdata
V OH
V OH
G_SDATA 0_0-3,
G_SDATA 1_0-3
(output timing)
valid
VOL
V OL
t odsel
t ohsel
GSSEL 0, 1
(outputtiming)
V OL
V OH

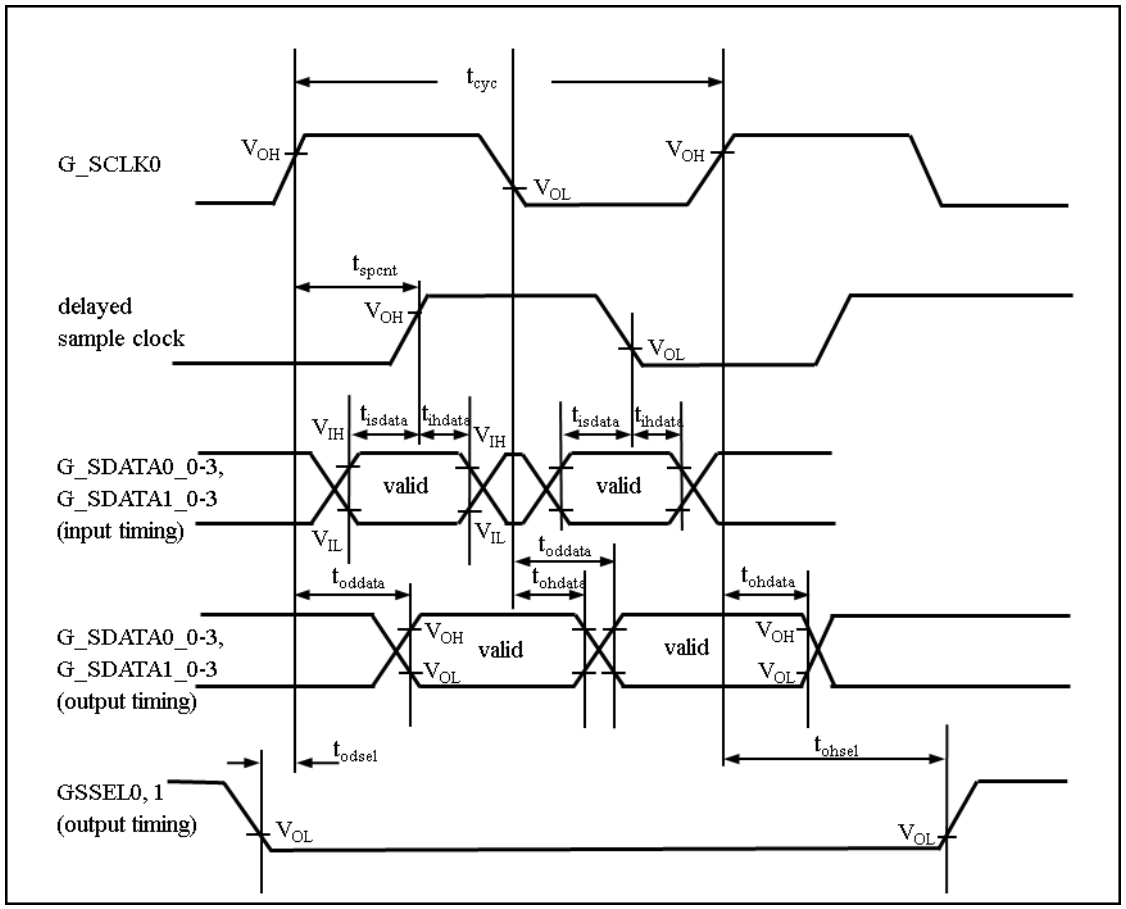
8.4.16.2 DDR-HSSPI Interface Timing (DDR Mode)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
HSSPI clock cycle	t_{cyc}	G_SCLK0 M_SCLK0	(CL = 20 pF, I_{OL} = -10 mA, I_{OH} = 10 mA),	12.5	-	ns	
				25	-	ns	During Quad Page mode or Dual quad mode
GSDATA -> G_SCLK↑ ↓ Input setup time	t_{isdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑ ↓ -> GSDATA Input hold time	t_{ihdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑ ↓ -> GSDATA Output delay time	t_{oddata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		-	tcyc/4 + 0.9	ns	
G_SCLK↑ ↓ -> GSDATA Output hold time	t_{ohdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		Tcyc/4 - 1.55	-	ns	
GSSEL ↓ -> G_SCLK ↑ Output delay time	t_{odsel}	G_SSEL0, 1 M_SSEL0, 1		(SS2CD+ 0.75)*tcyc - 3.375	-	ns	
G_SCLK↑ -> GSSEL↑ Output hold time	t_{ohsel}	G_SSEL0, 1 M_SSEL0, 1		2.25*tcyc - 0.05	-	ns	Direct Mode
				1.25*tcyc - 0.05	-	ns	Command sequencer Mode

Notes:

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured. The delay should not exceed t_{cyc}.*


tcyc
G_SCLK0
VOH
VOL
VOH
tspcnt
delayed
sample clock
VOH
VOL
VIH
tisdata
tihdata
VIH
tisdata
tihdata
G_SDATA0_0-3,
G_SDATA1_0-3
(input timing)
valid
valid
VIL
VIL
toddata
toddata
tohdata
tohdata
G_SDATA0_0-3,
G_SDATA1_0-3
(output timing)
VOH
VOL
valid
valid
VOH
VOL
todsel
tohsel
GSSEL0, 1
(output timing)
VOL
VOL

8.4.17 HyperBus

The HyperBus AC characteristics are specified with the specific reference voltage of V_{IL}, V_{IH}, V_{OL}, V_{OH} = 0.5 Vcc3 as mentioned in Section 8.4.3, regardless of automotive input-level configuration, CMOS Schmitt, and TTL.

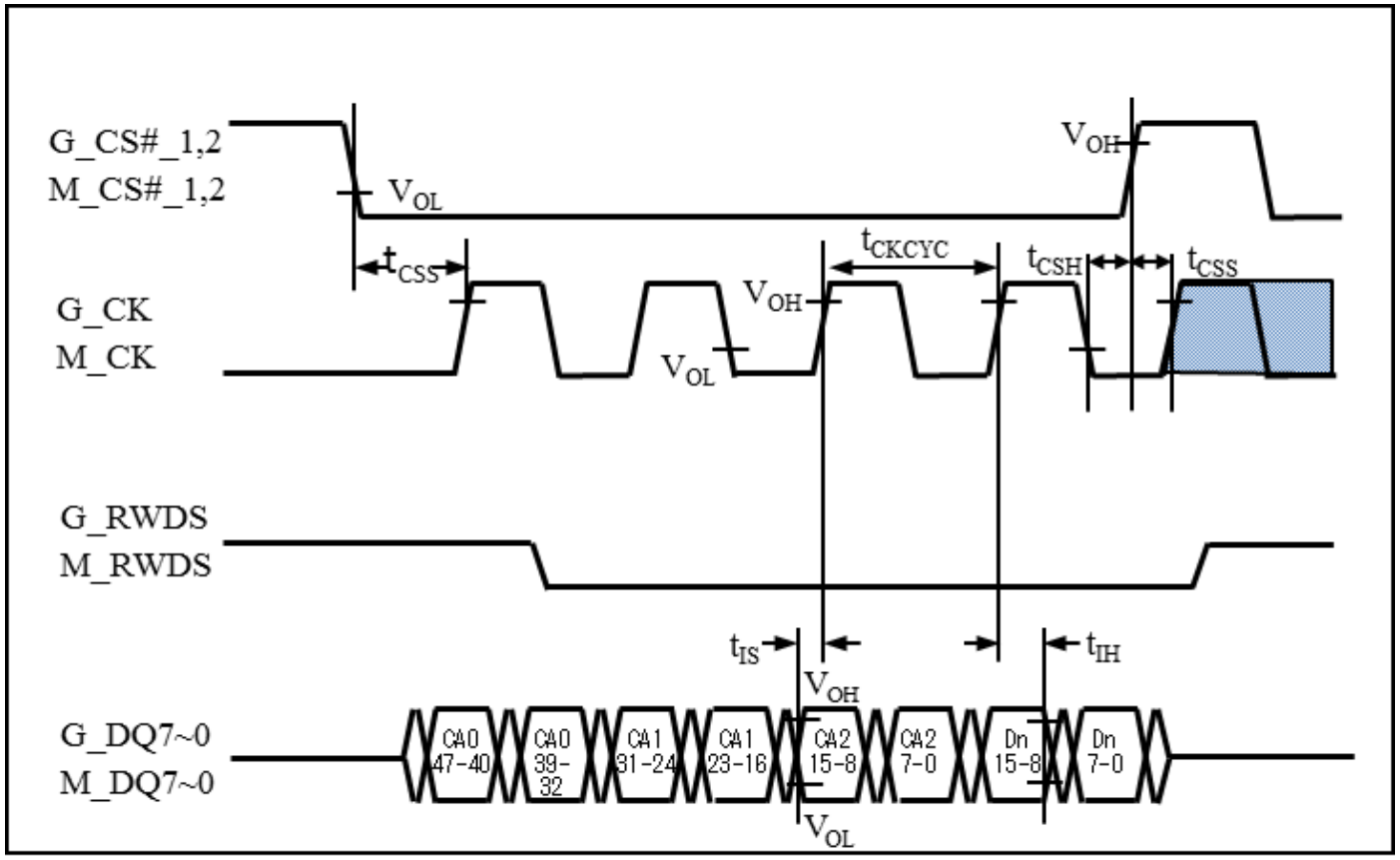
8.4.17.1 HyperBus Write Timing (HyperFlash)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
HyperBus clock cycle	t_{CKCYC}	G_CK M_CK	CL = 20 pF, I_{OL} = -10 mA, I_{OH} = 10 mA	10	-	ns	
CS ↑ ↓ -> CK ↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC} -2.0	-	ns	
DQ -> CK ↑ ↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC}/2	-	ns	

Note:

- *HyperBus clock cycle is always (1/F_{CLK_CD1})*4.*



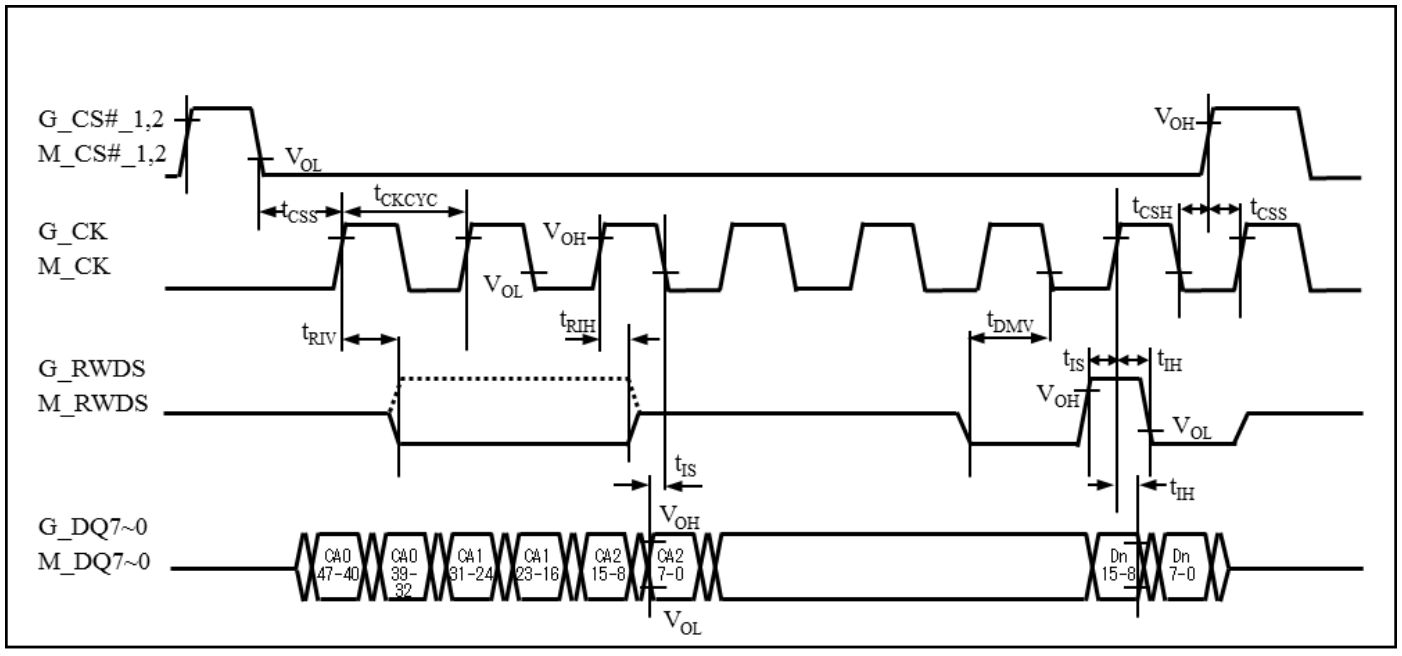
8.4.17.2 Hyper Bus Write Timing (HyperRAM)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Hyper Bus clock cycle	t_{CKCYC}	G_CK M_CK	(CL = 20 pF, I_{OL} = -10 mA, I_{OH} = 10 mA),	10	-	ns	
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC} - 2.0	-	ns	
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC}/2	-	ns	
RWDS↓-> CK↓ Data Mask Valid	t_{DMV}	G_RWDS M_RWDS		1	-	ns	
CK↑ -> RWDS↑↓ Refresh Indicator Valid	t_{RIV}	G_RWDS M_RWDS		-	6	ns	
CK↑ -> RWDS(Hi-z) Refresh Indicator Hold	t_{RIH}	G_RWDS M_RWDS		0	-	ns	

Note:

- *HyperBus clock cycle is always (1/F_{CLK_CD1})*4.*
- *When configuring the HyperBus clock cycle, consider the HyperRAM refresh interval.*



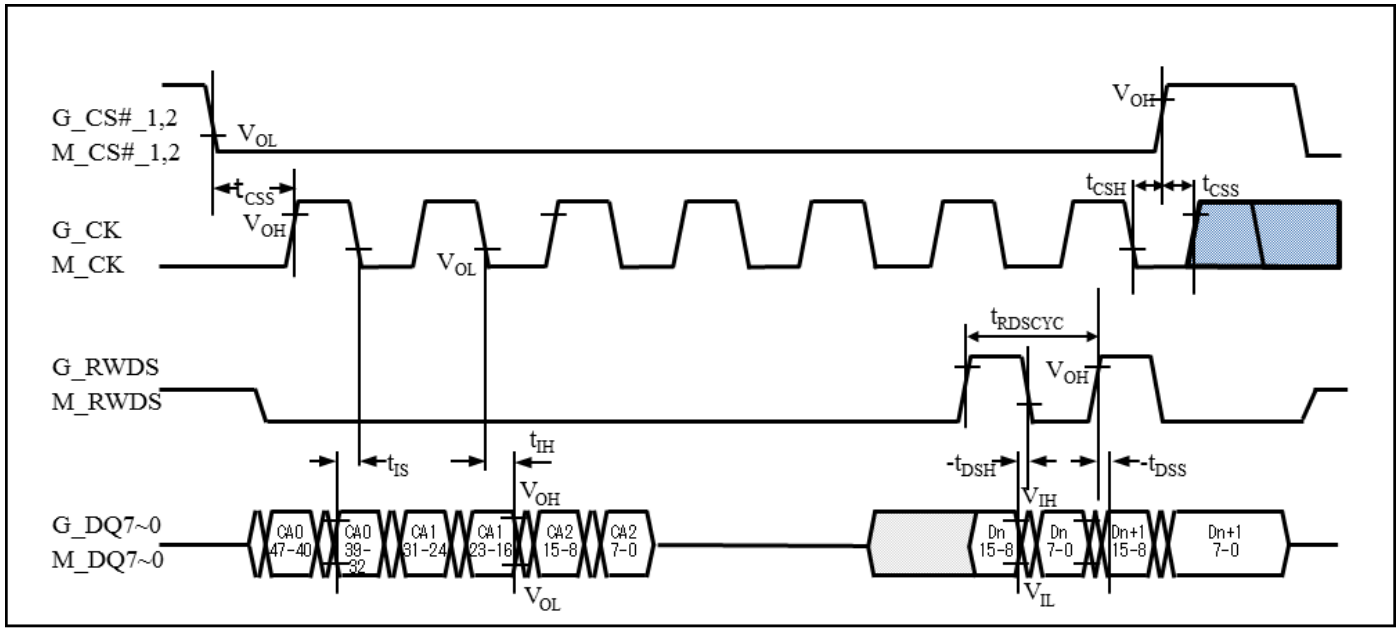
8.4.17.3 Hyper Bus Read Timing (HyperFlash)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Hyper Bus clock cycle	t_{RDSCYC}	G_CK, G_RWDS M_CK, M_RWDS	(CL = 20 pF, I_{OL} = -10 mA, I_{OH} = 10 mA),	10	-	ns	
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} -2.0	-	ns	
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} / 2	-	ns	
DQ -> RDS↑↓ Setup time	t_{DSS}	G_DQ7-0 M_DQ7-0		-0.9	-	ns	
RDS↑↓-> DQ Hold time	t_{DSH}	G_DQ7-0 M_DQ7-0		-1.0	-	ns	

Note:

- *HyperBus clock cycle is always (1/F_{CLK_CD1})*4.*



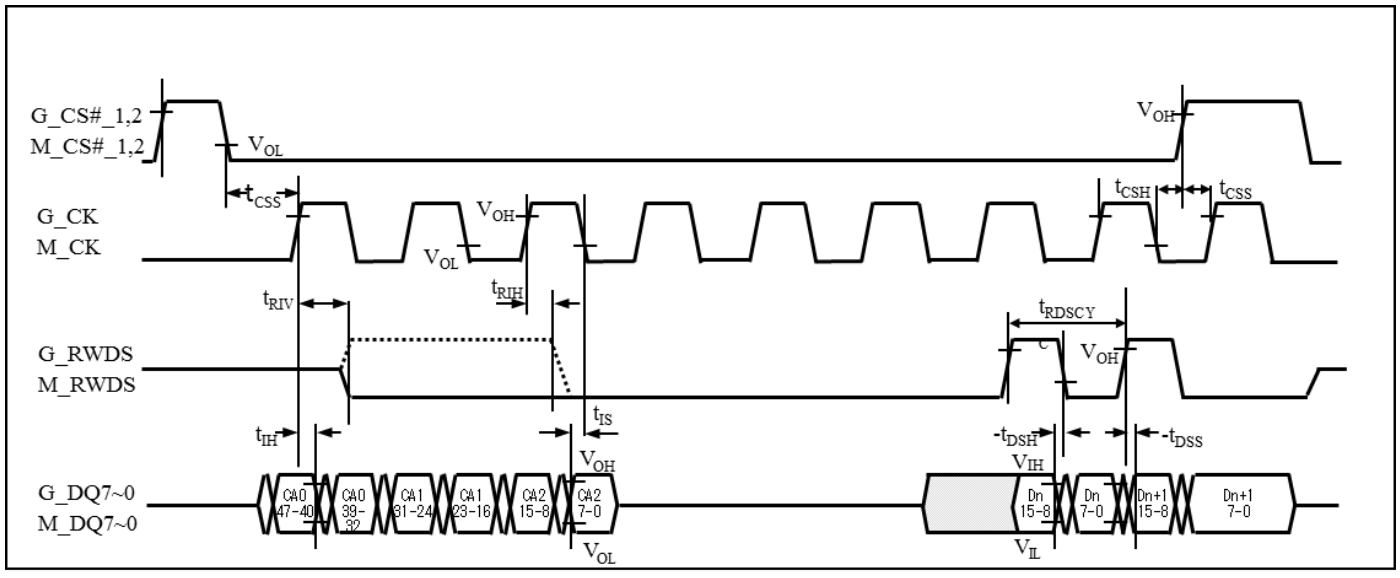
8.4.17.4 HyperBus Read Timing (HyperRAM)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
HyperBus clock cycle	t_{RDSCYC}	G_CK, G_RWDS M_CK, M_RWDS	(CL = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	10	-	ns	
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} -2.0	-	ns	
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} /2	-	ns	
DQ (valid) -> RWDS ↑↓ Setup time	t_{DSS}	G_DQ7-0 M_DQ7-0		-0.9	-	ns	
RWDS↑↓-> DQ (invalid) Hold time	t_{DSH}	G_DQ7-0 M_DQ7-0		-1.0	-	ns	
CK↑ -> RWDS↑↓ Refresh Indicator Valid	t_{RIV}	G_RWDS M_RWDS		-	6	ns	
CK↑ -> RWDS(Hi-z) Refresh Indicator Hold	t_{RIH}	G_RWDS M_RWDS		0	-	ns	

Note:

- *HyperBus clock cycle is always (1/F_{CLK_CD1})*4.*
- *When configuring the HyperBus clock cycle, consider the HyperRAM refresh interval.*

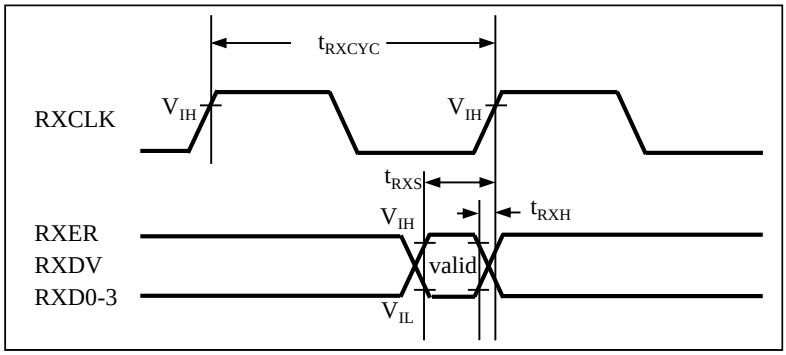


8.4.18 Ethernet AVB

8.4.18.1 Ethernet Receive Timing – MII Interface

(Condition: See 8.2. Operation Assurance)

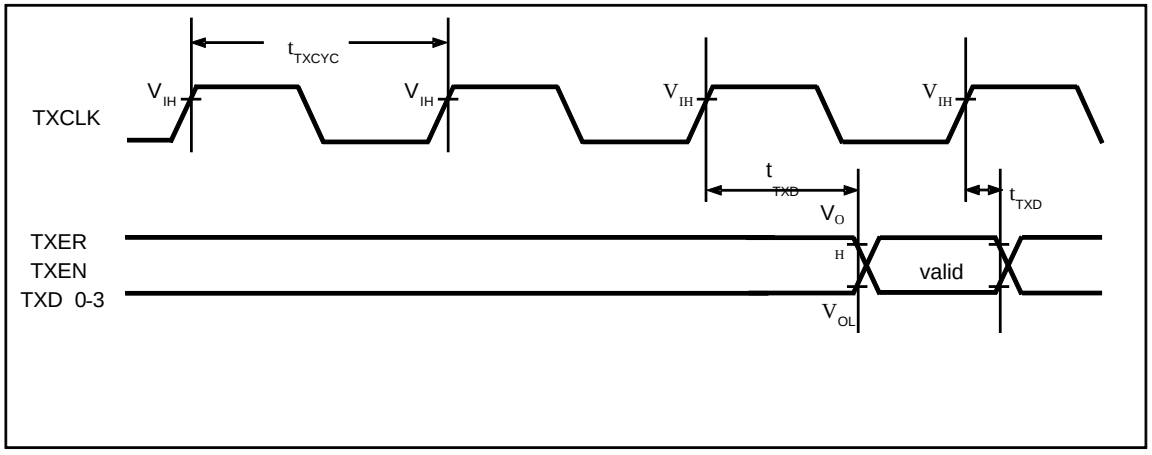
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RXCLK cycle	t_{RXCYC}	RXCLK	-	40.0	-	ns	
RX setup time	t_{RXS}	RXER RXDV RXD0-3		10.0	-	ns	t_{RXCYC} -30 ns
RX hold time	t_{RXH}	RXER RXDV RXD0-3		2	-	ns	



8.4.18.2 Ethernet Transmit Timing – MII Interface

(Condition: See 8.2. Operation Assurance)

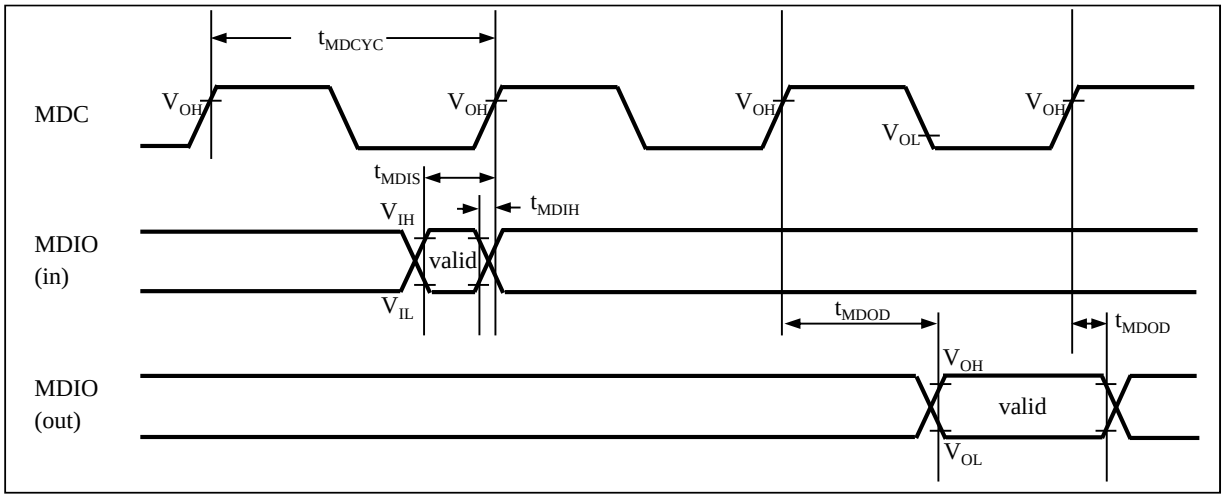
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TXCLK cycle	t_{TXCYC}	RXCLK	(CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA),	40.0	-	ns	
Tx delay time	t_{TXD}	TXER TXEN TXD0-3		0.5	25	ns	



8.4.18.3 MDIO Timing

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MDC cycle	t_{MDCYC}	MDC	(CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA),	400.0	-	ns	
MDIO input setup time	t_{MDIS}	MDIO		100.0	-	ns	
MDIO input hold time	t_{MDIH}	MDIO		0.0	-	ns	
MDIO output delay time	t_{MDOD}	MDIO		10.0	390.0	ns	



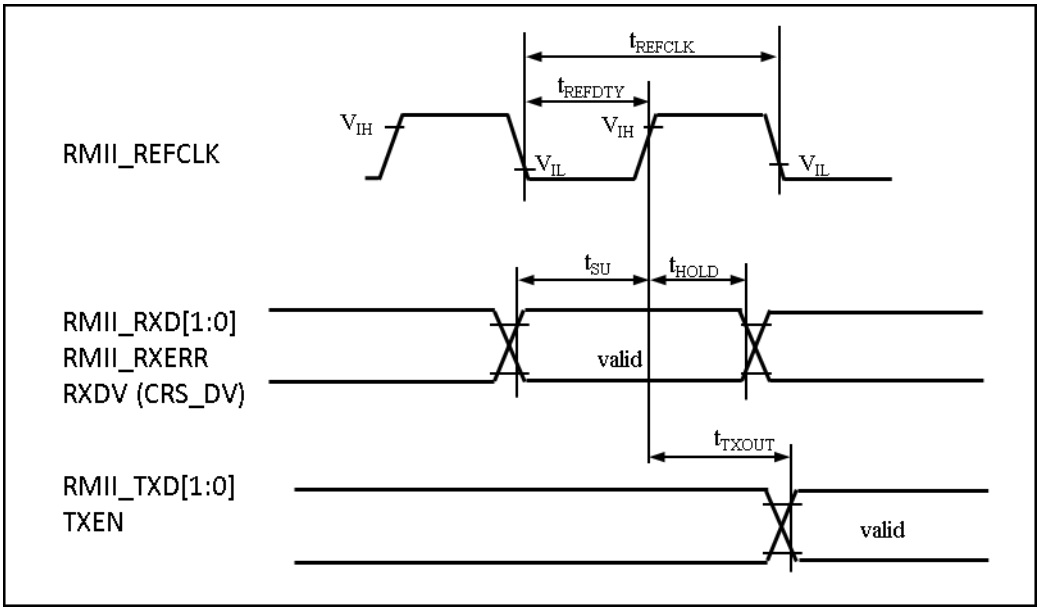
8.4.18.4 Ethernet Receive/Transmit Timing – RMII interface

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reference clock cycle	t_{REFCLK}	RMII_REFCLK	-	20	-	ns	
Reference clock duty cycle	t_{REFDTY}			35	65	%	
Data setup to RMII_REFCLK rising edge	t_{SU}	RMII_RXD[1:0], RMII_RXERR RXDV *1		4	-	ns	
Data hold from RMII_REFCLK rising edge	t_{HOLD}			2	-	ns	
Data output delay from RMII_REFCLK rising edge	t_{TXOUT}	RMII_TXD[1:0], TXEN	(CL = 25 pF, I_{OL} = -10 mA, I_{OH} = 10 mA)	2	13	ns	

Note:

- **1 RXDV pin is used for CRS_DV function of RMII interface*



8.4.19 MediaLB

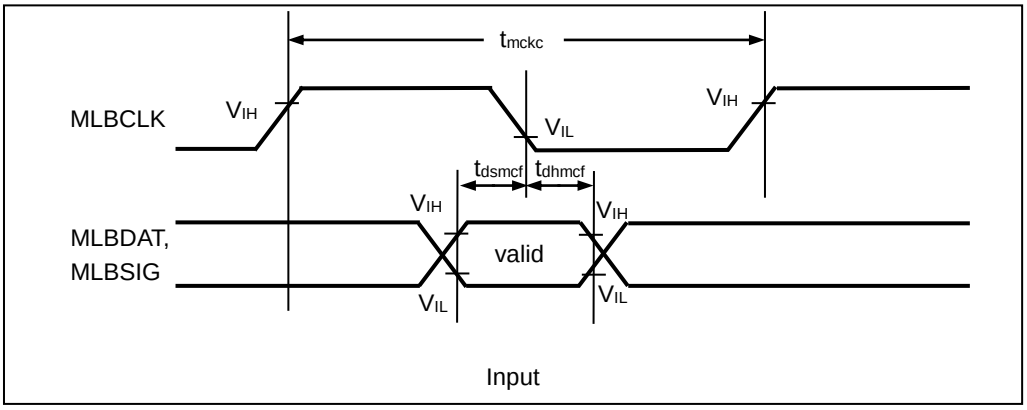
8.4.19.1 MediaLB Input Timing

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	-	39	-	ns	
MLBSIG, MLBDAT Input setup	t_{dsmcf}	MLBSIG MLBDAT		1.0	-	ns	
MLBSIG, MLBDAT Input hold	t_{dhmcf}	MLBSIG MLBDAT		4.0	-	ns	

Notes:

- *CLK_HAPP1B0(internal) frequency > MLBCLK(external) frequency*



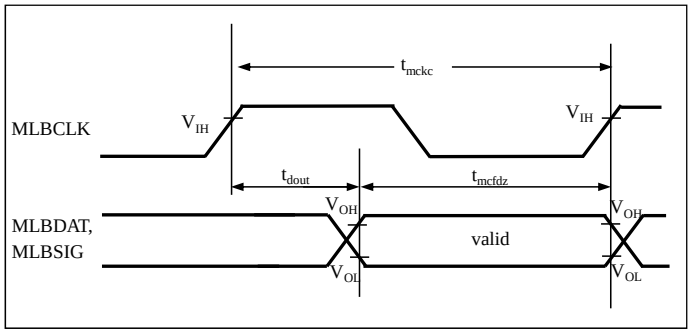
8.4.19.2 MediaLB Output Timing

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	(CL = 20 pF, I_{OL} = -6 mA, I_{OH} = 6 mA),	39	-	ns	
MLBSIG, MLBDAT output stop	t_{mcfdz}	MLBSIG MLBDAT		26.5	-	ns	t_{mckc} - t_{dout}
MLBSIG, MLBDAT output delay	t_{dout}	MLBSIG MLBDAT		0	12.5	ns	

Notes:

- *CLK_HAPP1B0(internal) frequency > MLBCLK(external) frequency*



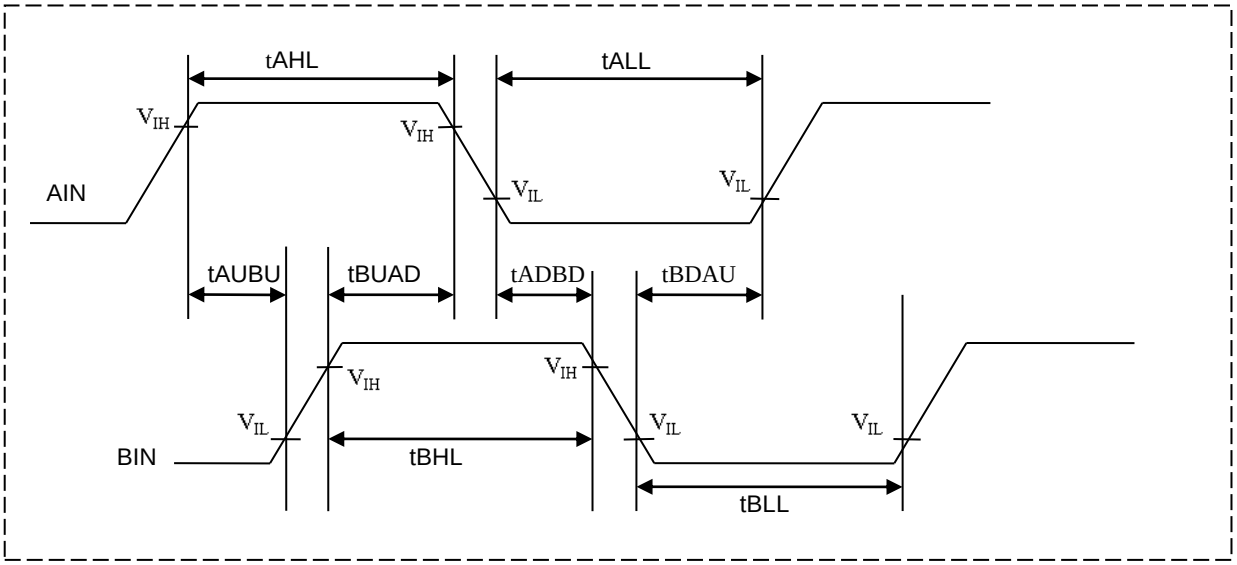
8.4.20 QPRC

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
"H" width of AIN	tAHL	AIN	—	4tCLK_LCP1A	—	ns	
"L" width of AIN	tALL	AIN	—	4tCLK_LCP1A	—		
"H" width of BIN	tBHL	BIN	—	4tCLK_LCP1A	—	ns	
"L" width of BIN	tBLL	BIN	—	4tCLK_LCP1A	—	ns	
Rising timing of BIN from "H" level of AIN	tAUBU	BIN	PC_Mode2 or PC_mode3	4tCLK_LCP1A	—	ns	
Falling timing of AIN from "H" level of BIN	tBUAD	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of BIN from "L" level of AIN	tADBD	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of AIN from "L" level of BIN	tBDAU	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of AIN from "H" level of BIN	tBUAU	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of BIN from "H" level of AIN	tAUBD	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of AIN from "L" level of BIN	tBDAD	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of BIN from "L" level of AIN	tADBU	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
"H" width of ZIN	tZHL	ZIN	QCR:CGSC = "0"	4tCLK_LCP1A	—	ns	
"L" width of ZIN	tZLL	ZIN	QCR:CGSC = "0"	4tCLK_LCP1A	—	ns	
Rising or falling timing of AIN/BIN from level valid timing of ZIN	tZABE	AIN/BIN	QCR:CGSC = "1"	4tCLK_LCP1A	—	ns	
Level valid timing of ZIN from falling or rising timing of AIN/BIN	tABEZ	ZIN	QCR:CGSC = "1"	4tCLK_LCP1A	—	ns	

Notes:

- *t is the period of peripheral clock(CLK)*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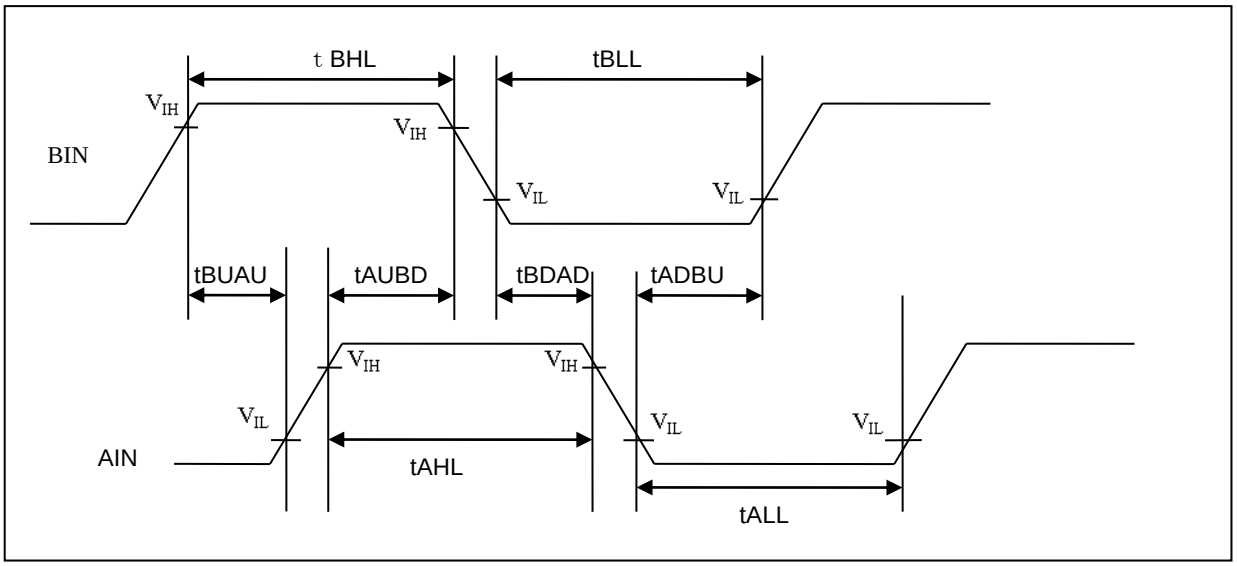
tALL
VIH
VIH
AIN
VIL
VIL
tAUBU
tBUAD
tADBD
tBDAU
VIH
VIH
VIL
VIL
VIL
BIN
tBHL
tBLL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tBLL
VIH
VIH
BIN
VIL
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tAUBD
tBDAD
tADBU
VIH
VIH
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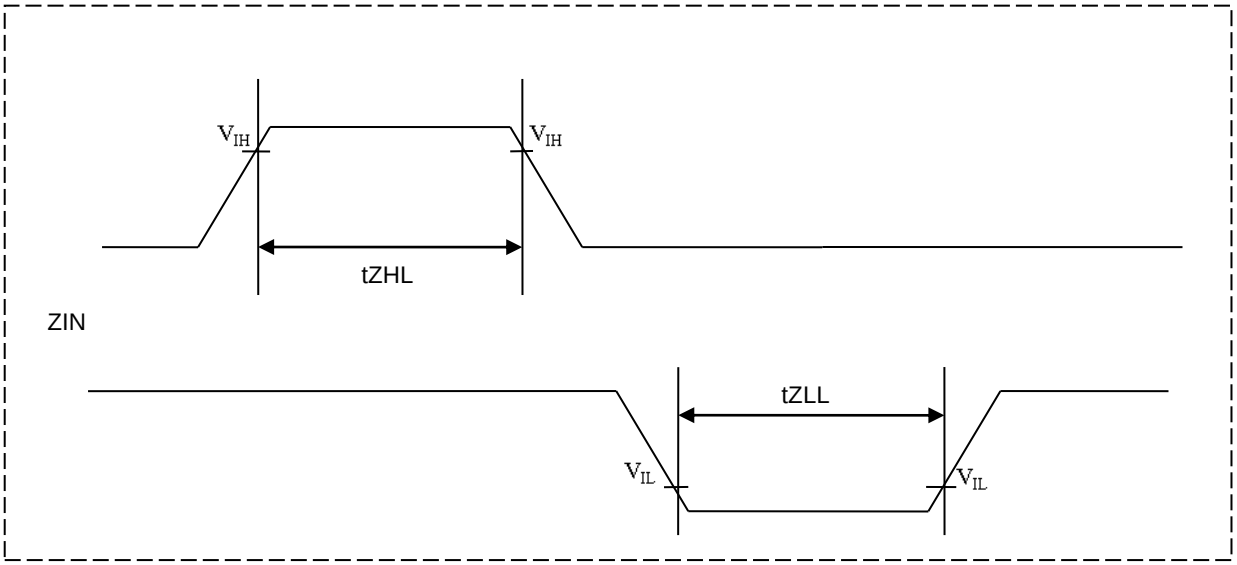
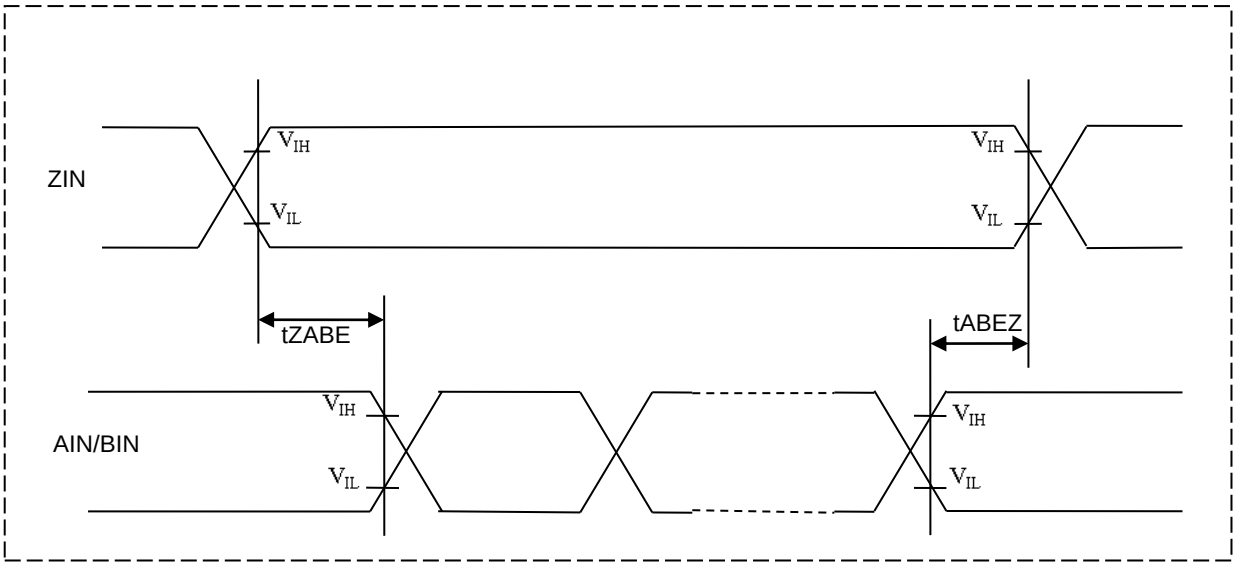
AIN
tAHL
tALL


VIH
VIH
tZHL
ZIN
tZLL
VIL
VIL


ZIN
V_{IH}
V_{IL}
V_{IH}
V_{IL}
tZABE
tABEZ
AIN/BIN
V_{IH}
V_{IL}
V_{IH}
V_{IL}

8.4.21 Port Noise Filter

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse filter time	-	All GPIOs	-	-	67	ns	*
		EINT0-15 TIN0-3, 16-19, 32-35, 48, 49	-	-	67	ns	-
		ADTRG	-	-	67	ns	-
		SCL4, 10, 12, 16, 17 SDA4, 10, 12, 16, 17	-	-	240	ns	-

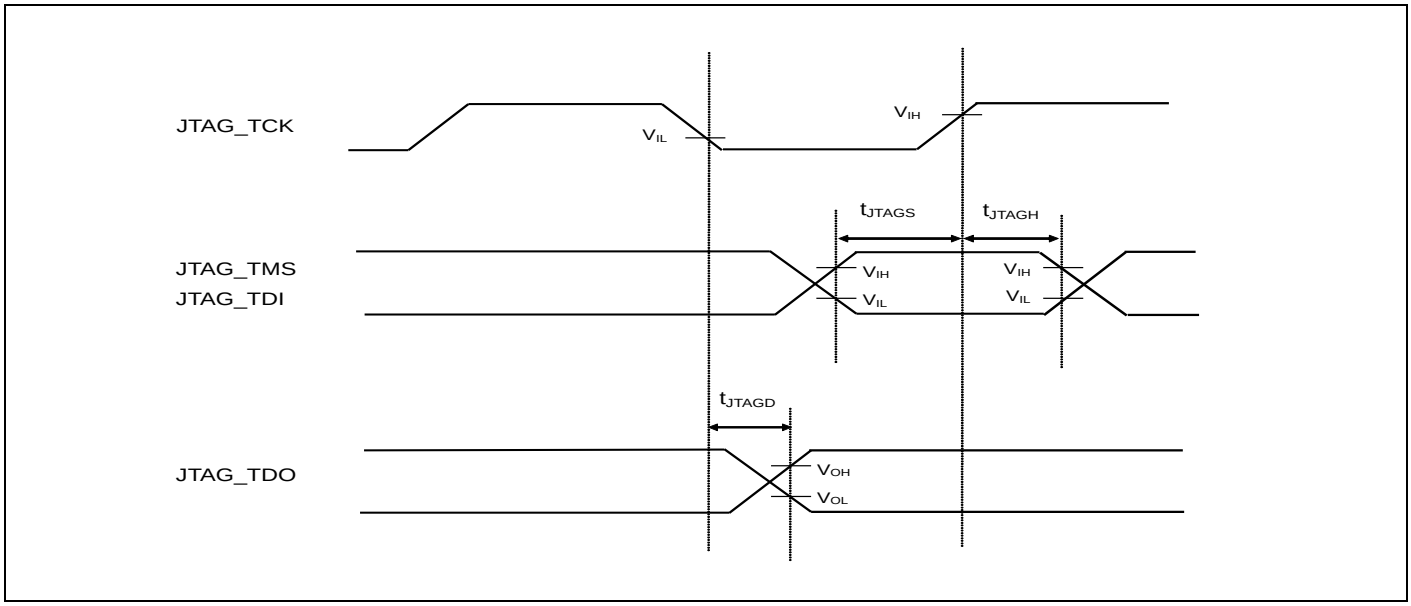
Note:

- *The spec guarantees that a rectangular pulse wider than the max filter time is never removed.*

8.4.22 JTAG

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	JTAG_TCK, JTAG_TMS, JTAG_TDI	(CL = 20 pF)	16	-	ns	
TMS, TDI hold time	T_{JTAGH}	JTAG_TCK, JTAG_TMS, JTAG_TDI		10	-	ns	
TDO delay time	T_{JTAGD}	JTAG_TCK, JTAG_TDO		-	25	ns	



8.4.23 I2S

8.4.23.1 I2S Timing – Master mode (MSMD=1)

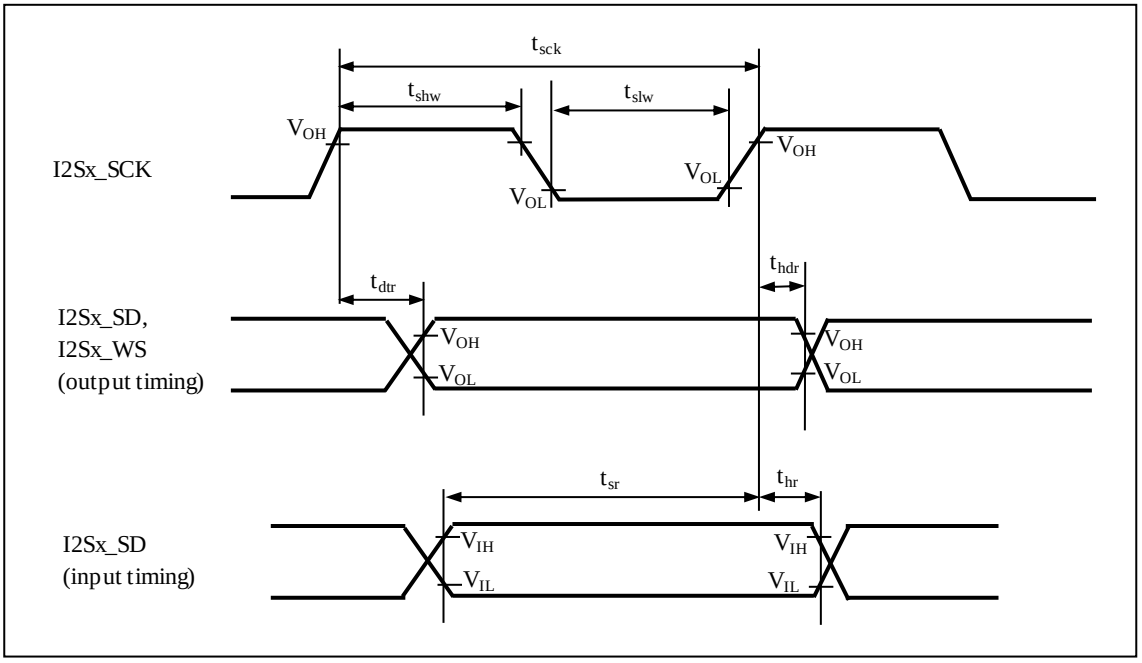
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
ECLK0/ECLK1 clock cycle	t_{eck}	ECLK0, ECLK1	(CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA) CPOL = 0, SMPL = 1	20	-	ns	Only relevant if external ECLK input is selected. *1
ECLK0/ECLK1 clock "H" pulse width	t_{ehw}			0.40* t_{eck}	0.60* t_{eck}	ns	
ECLK0/ECLK1 clock "L" pulse width	t_{elw}			0.40* t_{eck}	0.60* t_{eck}	ns	
I2S clock cycle (output SCK)	t_{sck}	I2S0_SCK, I2S1_SCK		66.66	-	ns	
I2S clock "H" pulse width	t_{shw}			0.35* t_{sck}	0.65* t_{sck}	ns	
I2S clock "L" pulse width	t_{slw}			0.35* t_{sck}	0.65* t_{sck}	ns	
Sender delay time SCK↑ -> SD/WS valid	t_{dtr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD, I2S0_WS, I2S1_WS		-	35	ns	*2
Sender hold time SCK↑ -> SD/WS invalid	t_{htr}			-10	-	ns	*2
Receiver setup time SD valid -> SCK↑	t_{sr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		40	-	ns	*2
Receiver hold time SCK↑ -> SD valid	t_{hr}			10	-	ns	*2

Notes:

*1: ECKM = 1. Refer to the Resource Input Configuration chapter in TRM for required RESSEL register settings.

*2: Refer to the I2S register description chapter in the TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values based on the table above will remain the same.



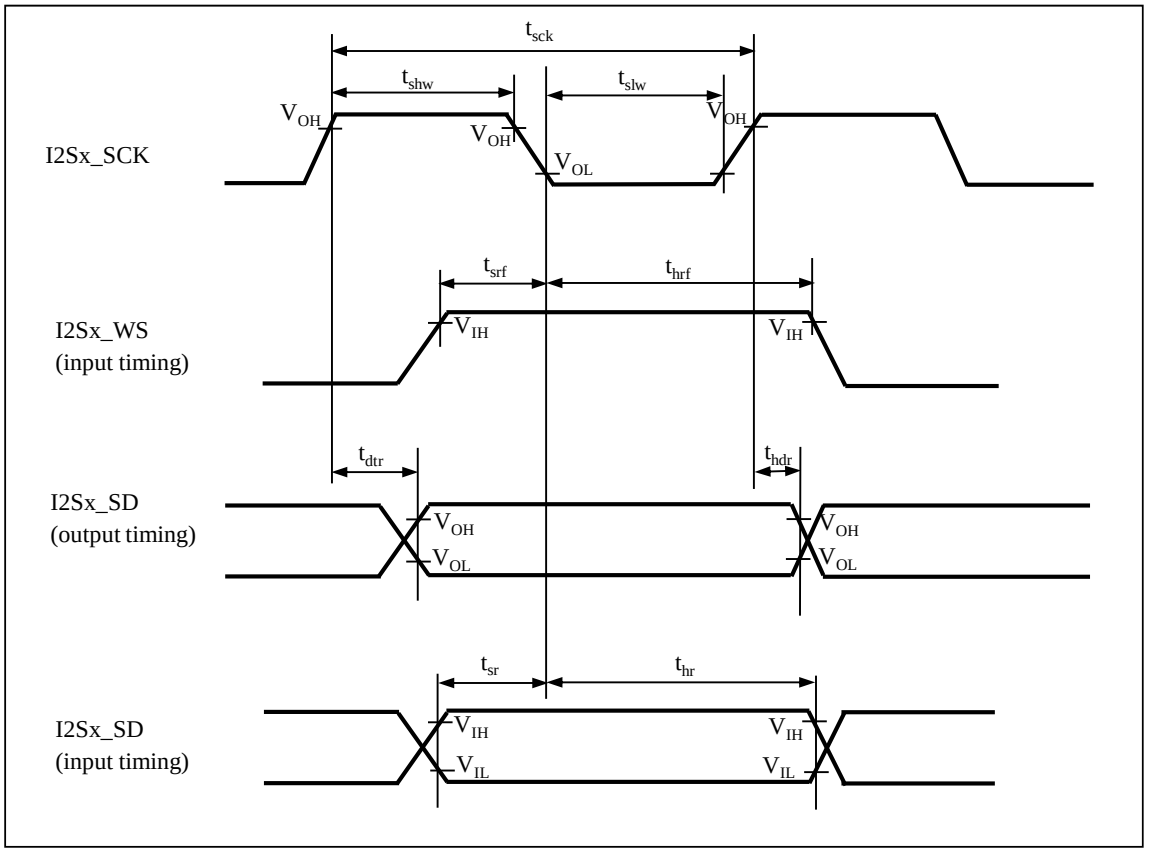
8.4.23.2 I2S Timing – Slave mode (MSMD=0)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
I2S clock cycle (input SCK)	t_{sck}	I2S0_SCK, I2S1_SCK	(CL = 20 pF, I_{OL} = -5 mA, I_{OH} = 5 mA) CPOL = 0, SMPL = 0	66.66	-	ns	
I2S clock “H” pulse width	t_{shw}	I2S0_SCK, I2S1_SCK		0.40* t_{sck}	0.60* t_{sck}	ns	
I2S clock “L” pulse width	t_{slw}			0.40* t_{sck}	0.60* t_{sck}	ns	
Setup time WS transition -> SCK↓	t_{srf}	I2S0_SCK, I2S1_SCK, I2S0_WS, I2S1_WS		40	-	ns	*1
Hold time SCK↓ -> WS transition	t_{hrf}			10	-	ns	*1
Sender delay time SCK↑ -> SD valid	t_{dtr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		-	35	ns	*1
Sender hold time SCK↑ -> SD invalid	t_{htr}			-10	-	ns	*1
Receiver setup time SD valid -> SCK↓	t_{sr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		40	-	ns	*1
Receiver hold time SCK↓ -> SD valid	t_{hr}			10	-	ns	*1

Notes:

*1: Refer to the I2S register description chapter in the TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values listed in the previous table will remain the same.



8.5 A/D Converter

8.5.1 Electrical Characteristics

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total Error	-	-	-	-	±12	LSb	*3
Integral Non linearity	-	-	-	-	±4.0	LSb	*4
Differential Non linearity	-	-	-	-	±1.9	LSb	*4
Zero transition voltage	V_{ZT}	AN0 to AN49	AVRL -11.5LSb	-	AVRL +12.5LSb	V	*5
Full-scale transition voltage	V_{FST}	AN0 to AN49	AVRH -13.5LSb	-	AVRH +10.5LSb	V	
Sampling time	t_{SMP}	-	0.3	-	-	µs	*1
Compare time	t_{CMP}	-	0.8	-	28	µs	*1
A/D conversion time	t_{CNV}	-	1.1	-	-	µs	*1
A/D trigger input time		ADTRG	$4t_{CLK_LCP1A}$	-	-	ns	$4t_{CLK_LCP1A} \geq 100$ ns
			100				$4t_{CLK_LCP1A} < 100$ ns
Resumption time	-	-	-	-	1	us	-

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Analog port input current	I_{AIN}	AN0 to AN17	-1.0	-	1.0	µA	$V_{AVSS} \leq V_{AIN} \leq V_{AVCC}$
		AN18 to AN25	-2.0	-	2.0	µA	
		AN26 to AN49	-3.0	-	3.0	µA	
Analog input voltage	V_{AIN}	AN0 to AN49	AVSS	-	AVRH	V	
Reference voltage	AVRH	AVRH5	4.5	-	5.5	V	$AV_{CC} \geq AVRH$
	AVRL	AVRL5/ AVSS	-	0.0	-	V	
Power supply current	I_A	AVCC	-	500	900	µA	
	I_{AH}		-	1.0	100	µA	*2
	I_R	AVRH	-	1.0	2.0	mA	
	I_{RH}		-	-	5.0	µA	*2
Variation between channels	-	AN0 to AN49	-	-	4.0	LSb	

Notes:

*1: Time per channel

*2: Definition of the power supply current (when $V_{CC} = AV_{CC} = 5.0$ V) while the A/D converter is not operating and in stop mode

*3: Total Error is a comprehensive static error that includes the linearity after trimming by software. 1 LSb = (AVRH-AVRL)/4096

*4: 1 LSb = (VFST-VZT)/4094

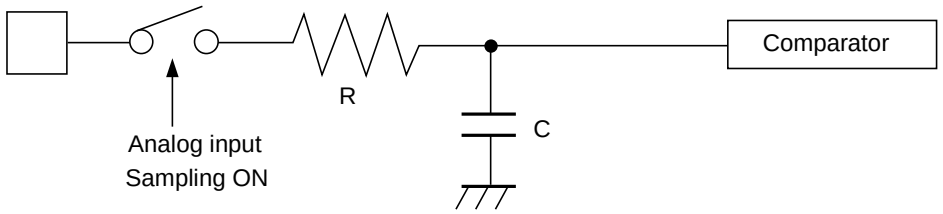
*5: 1 LSb = (AVRH-AVRL)/4096

8.5.2 Notes on A/D Converters

About the Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 µF) to an analog input pin.

Analog input circuit model



R	C		
12-bit A/D	3.9 kΩ (max)	11.0 pF (max)	(4.5 V≤AV_{CC}≤5.5 V)

Note: Use the numerical values provided here simply as a guide.

8.5.3 Glossary

Resolution: Analog change that can be identified by an A/D converter

Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics, includes zero transition error, full-scale transition error, and non linearity error.

Differential linearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSb.

Total error: Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.

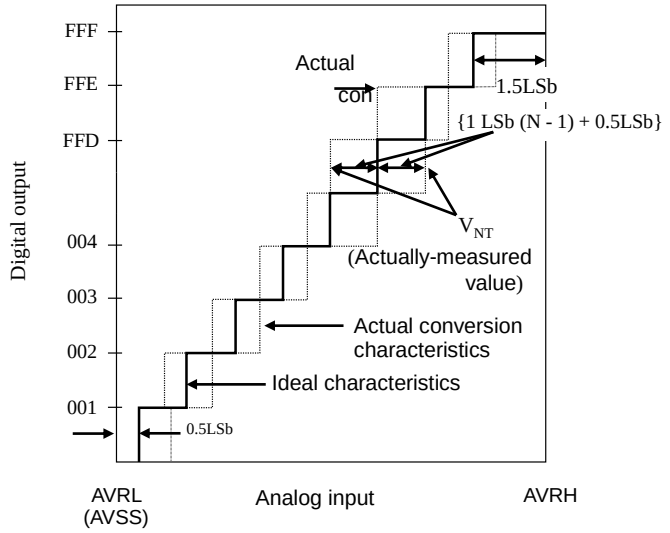
8.5.4 Calibration Condition

Calibration Condition should be the following

- AVCC = 5.0 V
- AVRH = 5.0 V
- T_A = 25 °C
- System clock frequency (CLK_LCP1A) = 10 MHz

See the A/D Converter Calibration section in the S6J3200 hardware manual.

Total error



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSb} \times (N-1) + 0.5\text{LSb}\}}{1\text{LSb}}\ [\text{LSb}]$$

$$1\ \text{LSb (Ideal value)} = \frac{\text{AVRH - AVRL}}{4096}\ [\text{V}]$$

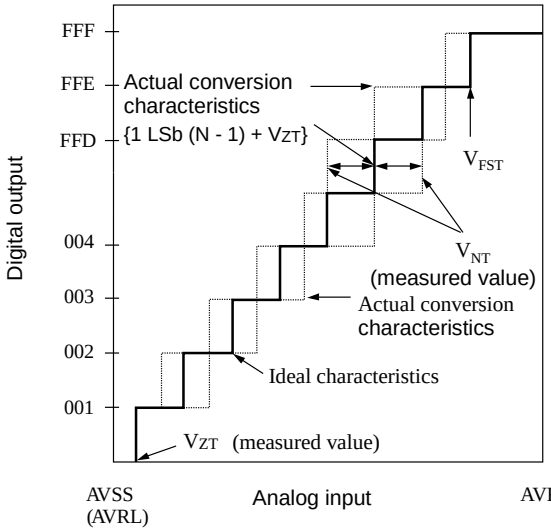
N: A/D converter digital output value.

$V_{ZT(}$Ideal value) = AVRL + 0.5LSb[V]

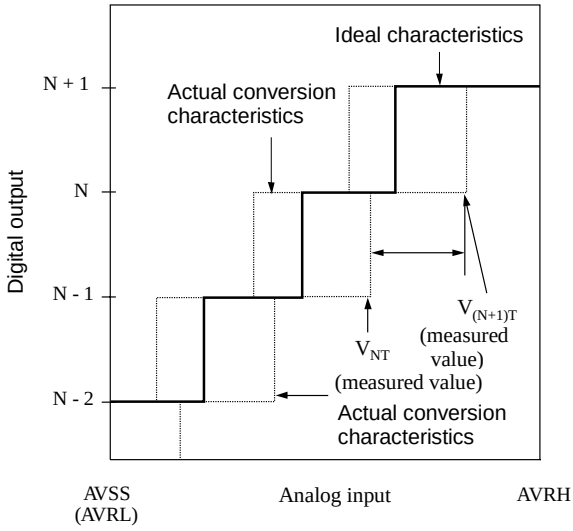
$V_{FST(}$Ideal value) = AVRH - 1.5LSb[V]

V_{NT}: Voltage at which the digital output changes from "(N – 1)" to "N".

Integral linearity error



Differential linearity error



$$\text{Integral linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSb} \times (N-1) + V_{ZT}\}}{1\text{LSb}}\ [\text{LSb}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1\text{LSb}} - 1\ \text{LSb}\ [\text{LSb}]$$

$$1\text{LSb} = \frac{V_{FST} - V_{ZT}}{4094}\ [\text{V}]$$

V_{ZT}: Voltage for which digital output changes from "0x000" to "0x001"

V_{FST}: Voltage for which digital output changes from "0xFFE" to "0xFFF".

8.6 Audio DAC

8.6.1 Electrical Characteristics

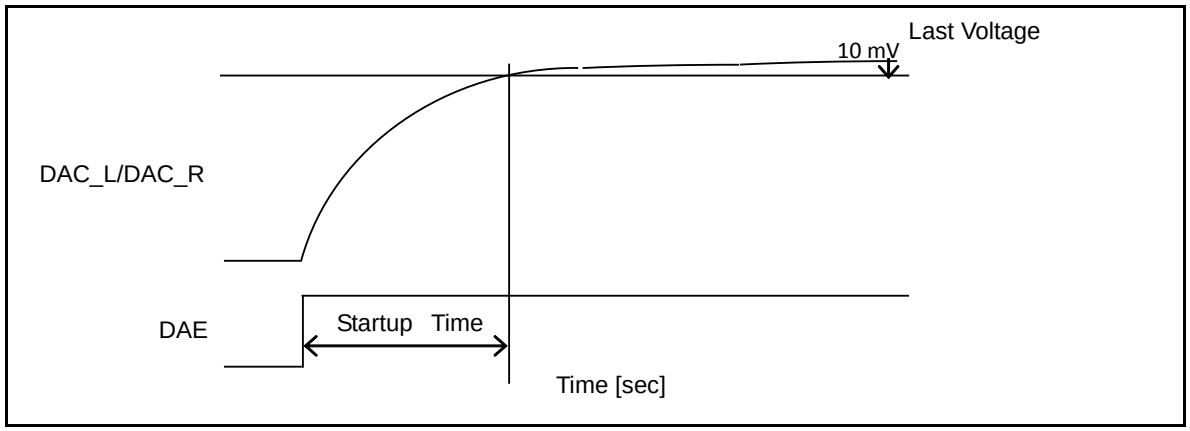
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions *1	Value			Unit	Remarks
				Min	Typ	Max		
system clock frequency	F_{CLKDA0}	-	-	2.048	-	18.432	MHz	
sampling clock	f_s	-	-	8	-	48	kHz	
Analog output load resistance *2	R_L	DAC_L DAC_R	-	20	-	-	kΩ	
Analog output load capacitance *2	C_L		-	-	-	100	pF	
capacitance	-	C_L C_R	-	5	10	20	µF	
Analog output single-end output range (±full scale)	-	DAC_L DAC_R	RL = 20 kΩ CL = 100 pF	-	0.673 AVCC3_DAC	-	V_{P-P}	
Analog output voltage (zero)	-		-	-	0.5 AVCC3_DAC	-	V	
THD+N *3	-	-	Signal frequency: 1 kHz LPF (fc: 20 kHz)	-	-82	-72	dB	
SNR *3	-	-	Signal frequency: 1 kHz LPF (fc: 20 kHz)— − A-weighting filter	85	89	-	dB	
Dynamic range *3	-	-		83	86	-	dB	
Out-of-Band Energy	-	-	20 kHz to 64f_s	-	-	-33	dB	
Channel Separation	-	-	-	-	80	-	dB	
Output impedance	-	-	-	150	200	250	Ω	
PSRR	-	-	Digital input: zero — noise 50 Hz	-	-35	-	dB	
			Digital input: zero — noise 1 kHz	-	-50	-	dB	
			Digital input: zero — noise 20 kHz	-	-40	-	dB	
			Digital input:full scale sine	-	-13	-	dB	
Supply current normal operation	-	AVCC3 _DAC	-	-	2.2	3.2	mA	
Supply current power-down	-	AVCC3 _DAC	-	-	-	100	µA	
Startup Time *4	-	-	DAE↑	-	650 *5	-	ms	

Notes:

- **1: All parameters specified f_s = 44.1 kHz, system clock 256f_s and 16-bit data, RL-20 kΩ, C_L = 100 pF, unless otherwise noted.*
- **2: Refer to Note 3 on R_L load connection.*
- **3: These values do not include the noise caused by the analog power supply. (Refer to Section 7. Use examples)*
- **4: 10 µF is connected to C_L, C_R.*
- **5: Startup time (Figure 8-7)*

Figure 8-7: Startup Time



Startup time can be calculated as follows.

1. Startup time (typ) = 650[ms]

2. CCOM = 10 µF × (1 ± α/100)

CCOM is a capacitor connected to Terminal C_L/C_R including capacitance variance.

α = Capacitance variance[%]

3. Startup time = Start up time (typ) × (1±α) [ms]

For example, CCOM = 11 µF then α = (11 µF – 10 µF)/10 µF = 10[%]

So, Startup time = 650 ms ×（1+10/100）= 715[ms]

Notes:

- *Two uses of R_L load connection:*
  - *Case1: R_L is connected to AVCC3_DAC /2 (Figure 8-8)*
  - *Case2: The coupling capacitance must be inserted as shown in (Figure 8-9).*

Figure 8-8: R_L is Connected to AVCC_DAC/2 (Example)

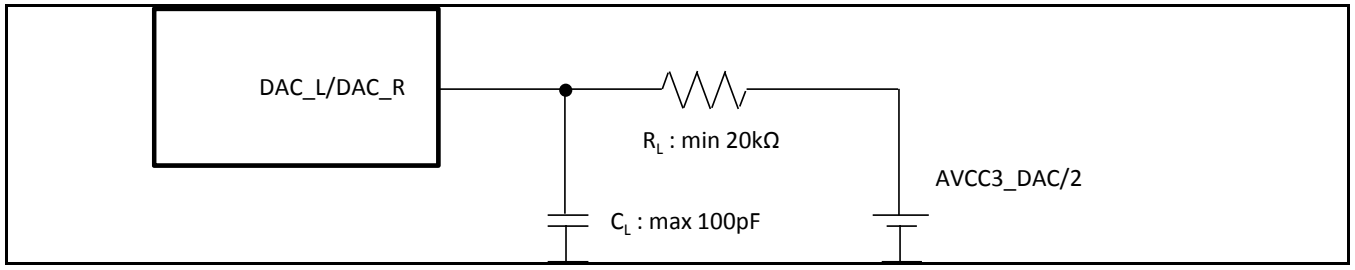
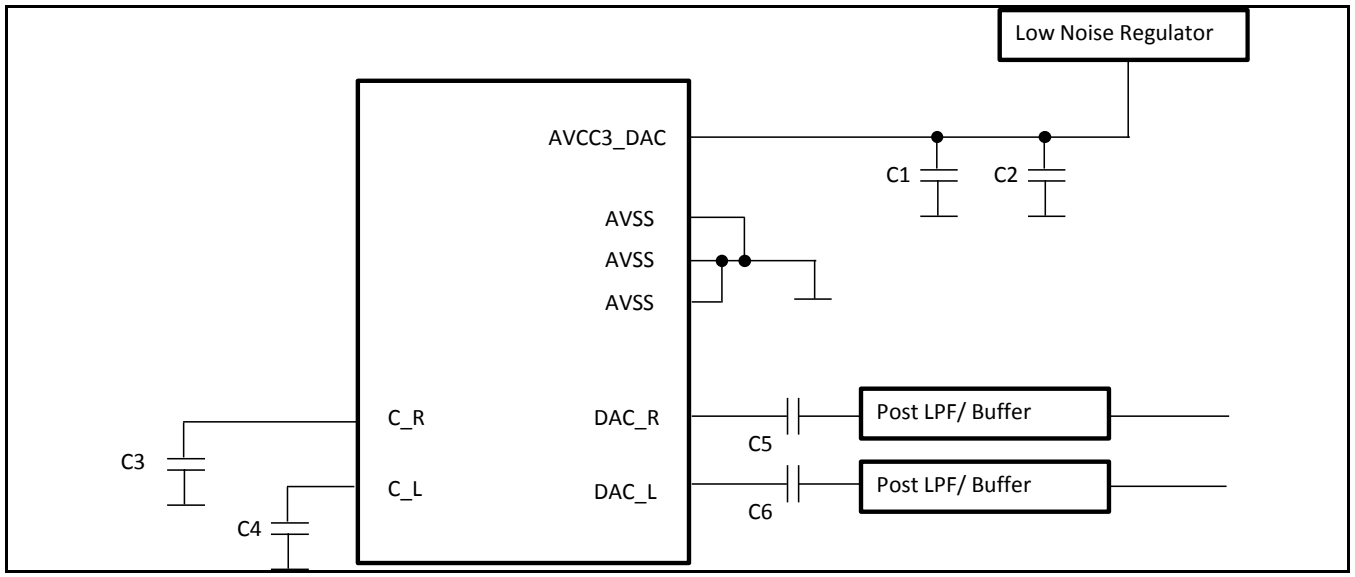


Figure 8-9: Coupling Capacitance (Example)



Notes:

- *C1: more than 10 µF low ESR capacitors*
- *C2: 0.1 µF ceramic capacitors*
- *C3, C4, C5, C6: 10 µF low ESR capacitors*
- *Impedance of each power line must be as low as possible.*

Notes:

- *When DAC is not used in your system, the related pins should be*
- *AVCC3_DAC = GND and AVSS = GND*
- *C_L = OPEN and C_R = OPEN*
- *DAC_L = OPEN and DAC_R = OPEN*

8.7 Flash Memory

8.7.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	300	1100	ms	8 KB sector*1 Internal preprogramming time included
	-	800	3700	ms	64 KB sector*1 Internal preprogramming time included
8bit write time	-	15	288	µs	System-level overhead time excluded*1
16bit write time	-	19	384	µs	System-level overhead time excluded*1
32bit write time	-	27	567	µs	System-level overhead time excluded*1
64bit write time	-	45	945	µs	System-level overhead time excluded*1
16bit (with ECC) write time	-	23	483	µs	System-level overhead time excluded*1
32bit (with ECC) write time	-	31	651	µs	System-level overhead time excluded*1
64bit (with ECC) write time	-	49	1029	µs	System-level overhead time excluded*1
Erase count*2 / Data retention time	1,000/20 years 10,000/10 years 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T_A = +85 °C

Notes:

- **1: Guaranteed value for up to 100,000 erases*
- **2: Number of erases for each sector*

8.7.2 Notes

While the Flash memory is written or erased, shutdown of the external power (VCC5 or VCC12) is prohibited.

In the application system, where VCC5 or VCC12 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function or external reset (RSTX).

For external power supply voltage stability conditions, see chapter 8.4.5.2 and 8.4.11.4.

9. Abbreviation

Abbreviation	Definition	Remark
A/D converter	Analog Digital Converter	
ADC	Analog Digital Converter	
AHB	Advanced High performance Bus	
AMBA™	Advanced Microcontroller Bus Architecture	
APB	Advanced Peripheral Bus	
ATCM	TCM-A port	
AXI	Advanced eXtensible Interface	
B0TCM	TCM B0 port	
B1TCM	TCM B1 port	
BBU	Bit Banding Unit	
BDR	Boot Description Record	
BT	Base Timer	
BTL	Bridge-Tied Load	
CAN	Control Area Network	
CD	Clock Domain	
CPU	Central Processing Unit	
CR	CR Oscillator	
CRC	Cyclic Redundancy Check	
CSV	Clock SuperVisor	
DAC	Digital Analog Converter	
DAP	Debug Access Port	
DED	Dual Error Detection	
DMA	Direct Memory Access	
DMAC	DMA Controller	
EAM	Exclusive Access Memory	
ECC	Error Correction Code	
ETM	Embedded Trace Macro	
EXT-IRC	External InteRrupt Controller	
FIQ	Fast Interrupt Request	
FPU	Floating Point Unit	
FRT	Free-Run Timer	
GPIO	General Purpose I/O	
HPM	High Performance Matrix	
HW-WDT	Hardware Watchdog Timer	
I/O	Input or Output	
I2S	Inter-IC Sound	
ICU	Input Capture Unit	
IPCU	Inter-Processor Communication Unit	
IRC	InteRrupt Controller	
IRQ	InteRrupt Request	
ISR	Interrupt Service Routine	
JTAG	Joint Test Action Group	
LLPP	Low Latency Peripheral Port	
LVD	Low Voltage Detector	
MCU	MicroController Unit	
MFS	Multi-Function Serial interface	

Abbreviation	Definition	Remark
NF	Noise Filter	
NMI	Non Maskable Interrupt	
OCU	Output Compare Unit	
OSC	OSCillator	
PCB	Printed Circuit Board	
PCBA	Printed Circuit Board Assembly	
PCM	Pulse Coded Module	
PD	Power Domain	
PLL	Phase Locked Loop	
PONR	Power ON Reset	
PPC	Port Pin Configuration	
PSS	Power Saving State	
QPRC	Quad Position & Revolution Counter	
PWM	Pulse Width Modulation	
RAM	Random Access Memory	
RIC	Resource Input Configuration	
RLT	Reload Timer	
ROM	Read Only Memory	
RSDS	Reduced Swing Differential Signal	
RTC	Real Time Clock	
RVD	Low Voltage Detection and Reset for RAM Retention	
SCT	Source Clock Timer	
SEC	Single Error Correction	
SECDED	Single Error Correction and Dual Error Detection	
SHE	Secure Hardware Extension	
SMC	Stepper Motor Controller	
SMIX	Sound Mixer	
SPI	Serial Peripheral Interface	
SRAM	Static RAM	
SSCG	Spread Spectrum Clock Generation	
SWFG	Sound Waveform Generator	
SW-WDT	Software Watchdog Timer	
SYSC	System Controller	
TCFLASH	FLASH connected to TCM	
TCM	Tightly Coupled Memory	
TCRAM	RAM connected to TCM	
TIC	Test Interface Controller	
TPU	Timing Protection Unit	
VIC	Vectored Interrupt Controller	
VRAM	Video RAM	
WDR	Watchdog Description Record	
WDT	Watchdog Timer	
WFG	Waveform Generator	
WorkFLASH	Work FLASH Memory	

10. Ordering Information

Table 10-1: Order Part Number Table

Part Number	Package
S6J32GEKSMSE2000A	LET208 (208-pin plastic TEQFP) - Not for new designs
S6J32GEKSNSE20000	LET208 (208-pin plastic TEQFP)
S6J32EELTMSC2000A	LEQ216 (216-pin plastic TEQFP) - Not for new designs
S6J32GEKSNSE20000	LET208 (208-pin plastic TEQFP)
S6J32EEKSNSE20000	LET208 (208-pin plastic TEQFP)
S6J32EELSNSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32FEKSNSE20000	LET208 (216-pin plastic TEQFP)
S6J32FELSNSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32GELSNSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32EELTPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32GELTPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32HELTNSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32FELTNSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32GELTNSC20000	LEQ216 (216-pin plastic TEQFP)

11. Errata

This section describes the errata for the S6J32E, S6J32F and S6J32G Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
S6J32GEKSMSE2000A
S6J32GEKSNSE20000
S6J32EELTMSC2000A
S6J32GEKSNSE20000
S6J32EEKSNSE20000
S6J32EELSNSC20000
S6J32FEKSNSE20000
S6J32FELSNSC20000
S6J32GELSNSC20000
S6J32EELTPSC20000
S6J32GELTPSC20000
S6J32HELTNSC20000
S6J32FELTNSC20000
S6J32GELTNSC20000

S6J32E, S6J32F and S6J32G Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available S6J32E, S6J32F and S6J32G Series devices.

Items	Part Number	Fix Status
MCAN wrong message transmission	S6J32GEKSMSE2000A S6J32GEKSNSE20000 S6J32EELTMSC2000A S6J32GEKSNSE20000 S6J32EEKSNSE20000 S6J32EELSNSC20000 S6J32FEKSNSE20000 S6J32FELSNSC20000 S6J32GELSNSC20000 S6J32EELTPSC20000 S6J32GELTPSC20000	Not be planned.

Items	Part Number	Fix Status
	S6J32HELTNSC20000 S6J32FELTNSC20000 S6J32GELTNSC20000	

1. MCAN wrong message transmission

■ Problem Definition

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

■ Trigger Condition

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2).

■ Scope of Impact

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.
- The M_CAN will start arbitration with wrong ID, format, and DLC.
- In case the ID won arbitration, a CAN message with valid CRC is transmitted.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

■ Workaround

Workaround 1:

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Request a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control filed information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

Workaround 2:

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Define a low priority message with DLC = 0 that can be sent without harm. E.g. loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configure sufficient Tx buffers – at least two - for this message type thus that there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

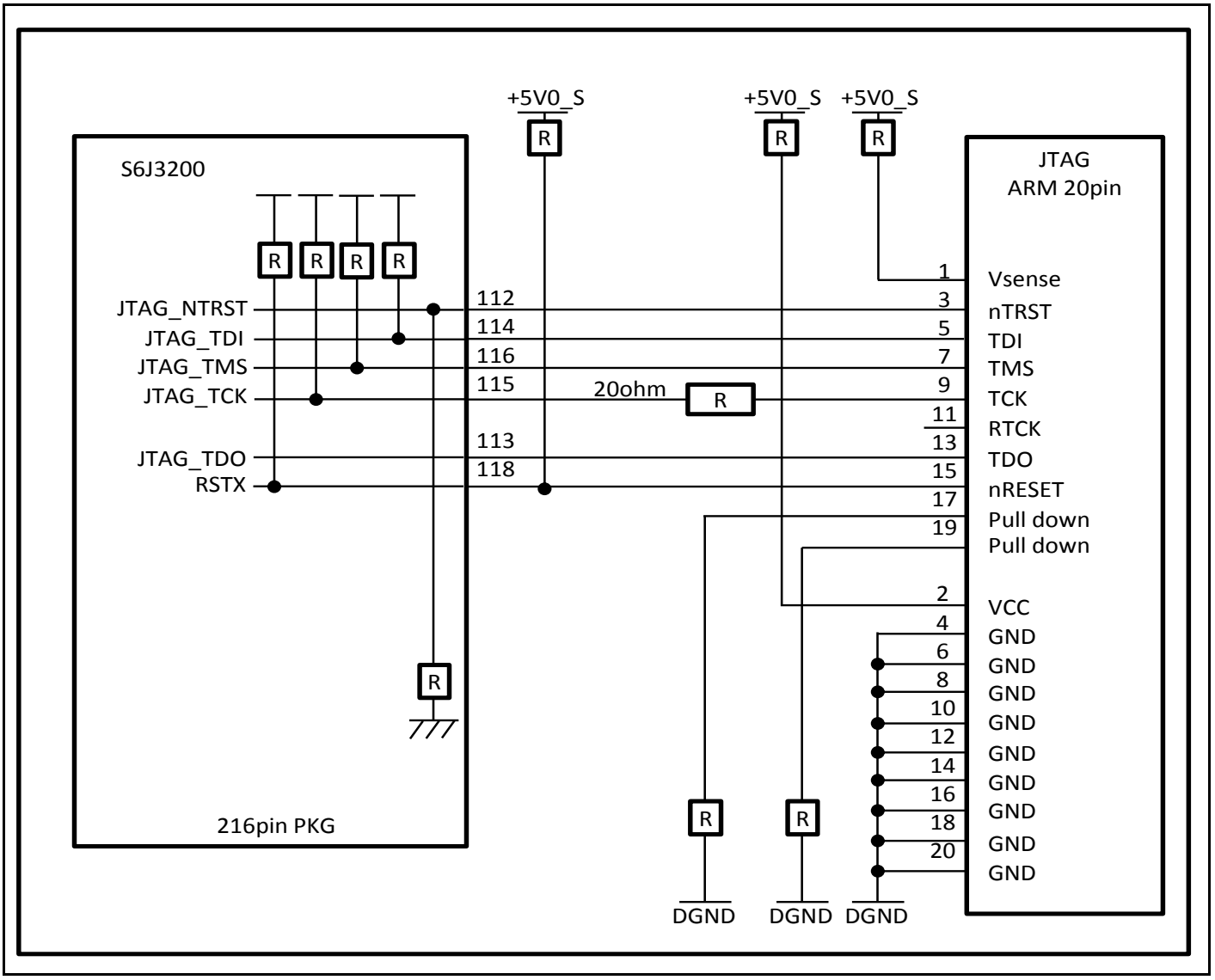
■ Fix Status

Not be planned.

12. Appendix

12.1 Application 1: JTAG Tool Connection

This is an application example of JTAG tool connection. See the application note AN209861 - Getting Started with the Traveo™ Family S6J3200 Series for details.



13. Document History

Document Title: S6J32E, S6J32F, S6J32G Series 32-Bit Microcontroller Traveo™ Datasheet
Document Number: 002-10689

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5078184	MFEU	02/04/2016	New Spec.
*A	5243447	ANMA/CASC/ ANZI	05/03/2016	Table 1-1 Document definition update Updated abbreviation table Added Figure 2-1: Option and Part Number"/" Table 2-2: Updated Function Digit Table. Table 2 1: Replaced 'optional' by actual feature if there was no change between E/F/G Section 2.2.2: Updated JTAG-ID table. Corrected LVDL0, LVDH0 release voltage min max values Section 3.2.1: Added description for RMII-pin usage. Updated Section 8.4.18 - MediaLB AC timing: updated to latest MediaLB standard (cycle time 40ns -> 39ns) Section 8.2: removed 2.7 V for LVDS-power supply Section 8.4.2.2: removed drawing for LER-208 Section 8.4.4: changed AC timing Section 8.4.12.2: updated AC spec Section 8.4.6.2: CSIO-timing: updated to actual design Section 8.4.15.2: Updated DDRHSSPI AC timing. SDR: added 'Dual Quad mode' for 50 MHz DDR: added 40 MHz limitation for Quad mode and Dual quad mode Removed RXx from list of trigger inputs DDRHSSPI-AC timing: added falling edge Section 8.4.16: Hyperbus: removed comments about revision A and B Section 8.4.17.4 Ethernet RMII: changed load and driving strength LVDS-AC Spec: Added minimum frequency of 5 MHz Table 8-1: FSSCG0 - Corrected frequency for MAX *1 (480MHz -> 464MHz) Updated figure in Section 8.4.3: Corrected min Vc12 voltage from 1.15 V to 1.1 V Section 8.2: Added $t_{PSC1VCC12}$
*B	5292130	ANZI	06/02/2016	Section 7.2.: Updated Latchup Prevention Section 8.1.: Added limit for analog input regarding AVCC5 Section 8.2.: Changed recommended power on sequence Added Ripple on FPD-Link PLL supply Section 8.4.5.: Defined condition for power-off time Added VCC12 stabilization time

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Section 8.4.14.: Updated MAX limit of T_{CIP} Added PLL lockup time Added Cycle to cycle jitter Added Output pulse position for frequencies 40, 25, 5 MHz
*C	5351068	CASC/ANMA/ANZI	07/14/2016	Section 3.2: - Table 3-1: Ethernet AVB: revision numbers deleted: "ETHERNETn_revision_reg : 0x30070106 (Initial value) for revision B ETHERNETn_designcfg_debug6 : 0x0302000E (Initial value) Section 8.1: Added note 13 about output voltage of ADC shared pins Added recommendation to set VCC and AVCC to same voltage (with explanation) Added comment to clarify meaning of "Analog pin input voltage" Section 8.2: Deleted "Supply stabilization time" (more detailed spec already added in 8.4.5) Section 8.3.1: VIH13/14: refers to DVcc, not Vcc5 VOL4/5/6: corrected list of applicable pins Deleted footnote *1 (about pins supplied with DVcc). Information is included in table IIL/RUP2/RDOWN1: corrected list of applicable pins (removed not existing pins) Section 8.3.2.2 and 8.3.2.3: Deleted reference to remark "*1" (which was already deleted) Section 8.4.3: Table 8-1: FPLL0 corrected max PLL freq 720->480MHz Deleted note "*4" (was unused) Section 8.4.4: Changed wording of RSTX noise filter spec Section 8.4.6.2: Changed tables according to Amber-P2 (not yet final): Added conditions "*2" and "*3" Changed cycle time and pulse widt spec from fixed time to number of clock cycles Changed tSLOVI spec (min and max values) Changed tSLOVE max value Changed tIVSHE and tSHIXE min values

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Added sub-sections (5)-(8) from Amber-P2 Section 8.4.12.1 Changed output delay from 8.5 ns to 9.3 ns Section 8.4.13 Added CL spec to pin load condition Added remark "Equals 1/f" for TCIP Changed format of output pulse position spec according to Amber-P2 Section 8.4.16 (all sub sections): Changed timing diagrams (removed timing parameter which are not specified) Section 8.4.16.3 and 8.4.16.4: Changed tDSS and tDSH spec (less restrictive than old spec) Section 8.5.17.4: Changed timing diagram (corrected signal names) Section 8.4.18.2: Changed tdout spec from 13.5 ns to 12.5 ns according to Section 8.6.1: Changed figure 8-7: corrected typo (volgate) Section 8.2: minor description change Section 8.4.16: added note about clock source Section 2.1: CRC channels 1 -> 4 Section 8.1: removed Clamp current “special spec” Section 8.4.10.3: removed LVDL1 setting “01” (useless) Section 3.2: Added comment to CAN-FD spec: “CAN-FD rev 3.2 is used.” Section 8.4.10.6: corrected typical release voltage for setting 0001 from 2.75 V to 2.85 V Section 2.2.1: deleted two notes about devices w/o FPD link Section 3.2: added initial main clock stabilization time in table 3-1 Section 8.4.6.4: changed name “High speed mode” to “Fast mode” Section 3.2: added “Interrupt Enable Register” in table 3-1 for HyperBus I/F not supported registers Section 8.4.9: Corrected release voltage for LVDL1 default level (without trimming) Section 3.2: “Reset” section in table 3-1: added description about not supported EX5VRST Section 8.4.11: renamed VOH8/VOL8 to VOH/VOL Section 3.2: “MFS” section in table 3-1: added note that I2C is not hot-swappable Section 3.2: “I2C” section in table 3-1: deleted comment about PPU Section 8.4.19: changed wording and added I2C filter time Section 7.2: added “Method to Switch off VCC12 during Power-off Sequence Section 8.4.5: “Power–On Conditions” copied from Amber-P2 DS, rev9281Section 8.3.2.2: Added load and MCGAIN setting in Remark column. External clock mode will be added after evaluation Added Section 11 (JTAG connection) Section 8.4.10: copied tables and notes from Amber-P2 DS, rev9281: added

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				description about guaranteed MCU operation range, updated notes, removed redundant LVDH0 spec Section 3.2: section “PLL/SSCG PLL” in Table3-1: Center spread mode usage is permitted (with conditions) Section 8.4.3:Added note about SSCG center spread mode Section 8.4.3: Added spec for Hyperbus VIH/VIL and VOH/VOL levels Section 8.4.16: Added description about VIH/VIL and VOH/VOL Section 7.2: Deleted note about “Power-on Time” Section 8.4.16.3 and 8.4.16.4: tDSS is setup time of “data-> clock “ Section 8.4.6.2: changed clock cycle time and H/L pulse width definitions (mainly removed “Remarks”) Section 8.4.8: removed spec for stop mode Section 8.4.6.2 MFS: aligned font size in tables (different sizes were used in the same table) Section 8.3.2.1: added 50 MHz as condition for ILVDS of AVCC3_LVDS_PLL Section 8.4.12.1/2/3 Display controller: revised method of specifying AC spec Section 8.4.12.1/2/3 Display controller: Updated waveforms according to new AC spec Section 8.4.12.1/2 Display controller/DSP0: change max frequency from 80 MHz to 64 MHz to match guaranteed performance of Graphic subsystem Section 8.4.6.3 MFS/CSIO: changed t_{SOVLI} and t_{SOVHI} to 2x tclk Section 8.4.6.2 (1)-(4) removed redundant information from t_{SCYC}, t_{SHSL}, t_{SLSH}, (1),(2)removed obsolete footnote *2 and changed footnote number *3 to *2 (3),(4) flipped footnote *2,*3 and updated footnote assignment at t_{SOVLI} (3),(4) added SOT16, 17 to Pin name of t_{SOVLI} (8) added figure for t_{SCC} Section 8.4.6.3 Lin Interface: corrected figure Section 8.4.16 corrected cross reference Section 8.4.10.5 corrected max value of LVDL2V=01 Section 3.2.1: RMII – corrected usage of CRS (to 'not used'), RX_DV (to 'used') Section 8.4.18.4: Ethernet RMII: AC: added RXDV and updated waveform for adding RXDV and note below the table Section 8.4.18.4: Moved IO-cell driving strength to output function only
*D	5429050	ANMA	09/07/2016	Section 2.2.1/Figure 2-1: Options and Part numbers: added Option 'M' for revised version. Section 2.2.2: Added Chip-ID and JTAG-ID for Revision 'M' Section 2.1 Function list: Graphic-TTL output/RSDS/FPD-link - added description about which channel can be used on which output type Section 2.1 Function list: Display clock – corrected from 80 MHz to 64 MHz Updated copyright information and added IoT link on the last page.

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	5563210	ANZI / GERH	12/22/2016	Section 3.2 Product Description: HyperBus I/F - Changed pointer for Hyperbus details Section 3.2.2 Product Description: section added to describe limitation of RAM Guarantee Section 4.1 Pin Assignment: Replaced pinning pictures by detailed pictures with function names Section 4.2.1 TEQFP-208; Chapter 4.2.2 TEQFP-216; Chapter 4.2.3 TEQFP-256: Exchanged package drawings Section 6.2 Remark: add the following note: "Only the specified GPIOs are allowed to be used as inputs. Otherwise, undesired chip behavior could occur." Section 8.1 Removed doubled row Section 8.3.1 Delta-VOH8 & Delta-VOL8 for the SMC pins -> Delta-VOH23 & Delta-VOL23; corrected table "Maximum deviation of VOL23" --> "...VOL23" Section 8.3.2.1 Port Function Characteristics: Updated ILVDS for pin AVCC3_LVDS_PLL to 9mA, for pin VCC3_LVDS_Tx to 75mA Section 8.3.1: VOH24 relaxed by 50mV to DVCC-0.53V Section 8.4.13 Removed DSP0_DATA0 from VCC53 Section 8.4.5 Reset: added subsection for supply stability conditions Section 8.4.5.2: added symbol for VCC12 stabilization time Section 8.4.6.1 added voltage ramp 100mV/us Section 8.4.7.2 CSIO Timing: Add LIN Tslove min parameter Section 8.4.7.2 CSIO Timing: Updated tSLOVE / tSHOVE & tIVSLE / tIVSHE Section 8.4.7.2 CSIO Timing: revised tSLOVE/tSHOVE, tIVDLE/tIVSHE Section 8.4.7.2 CSIO Timing: corrected clock names for Slave mode, Serial clock "L" pulse width Section 8.4.7.2 CSIO Timing: tCSHI changed Section 8.4.7.2 CSIO Timing: tslovi / tshovi changed Section 8.4.11.4 Low voltage detection/LVDH1: added note with supply stability conditions Section 8.4.13.1, 8.4.13.2 & 8.4.13.3 Display controller: Added note "Values valid for unshifted display clock (dsp_ClockInvert=0, dsp_ClockShift=0)." Section 8.4.13.1, 8.4.13.2 & 8.4.13.3 update timing parameter based on AC characterization Section 8.4.16.1 & 8.4.16.2 DDR-HSSPI: change note from "- For *1, the delay of the delay sample clock can be configured (DLP function)." to "- For *1, the delay of the delay sample clock can be configured." Section 8.4.16.1 DDR-HSSPI: removed tspcnt and extended note Section 8.4.16.1 & 8.4.16.2 DDR-HSSPI: changed timing value for G_SCLK -> GSSEL, G_SLCK -> GSDATA, GSSEL -> G_SCLK and GSSEL waveform

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Section 8.4.16.1 & 8.4.16.2 DDR-HSSPI: changed timing value for GSSEL↓ -> G_SCLK↑ Output delay time (parameter todsel) Section 8.4.16.2 DDR-HSSPI: removed tspcnt and extended note Section 8.4.17.1, 8.4.17.2, 8.4.17.3, 8.4.17.4 Hyperbus: Corrected VOH/VOL vs VIH/VIL in picture Section 8.4.18.1 Ethernet AVB: corrected TRXH min value Section 8.4.18.3 Ethernet AVB: changed the MDIO - tMDOD max value from 190ns to 390ns Section 8.4.18.2 Ethernet AVB: Removed COL/CRS timings (table & picture updated) Section 8.4.18.2 Ethernet AVB: corrected TXDV to TXEN Section 8.4.18.4 Ethernet AVB: renamed *TX -> *TXD / *RX -> *RXD to be consistent with other naming style Section 8.4.20 Port noise filter: Added QPRC AC specification Section 8.4.21 Port noise filter: Add ADTRG input noise filter information Section 8.4.22 JTAG AC spec: Added Section 8.7.1 Flash memory: Removed "8bit (with ECC) write time" Section 8.7.2 Flash memory: added VCC12 and RSTX in the note and replaced description for supply stability by references to section 8.4.5 and 8.4.11.4. Section 8.4.4, 8 & 8.4.16 specified DDR-HSSPI AC characteristics reference voltage of VIL, VIH, VOL, VOH = 0.5 Vcc3 Section 8.2.23 I2S: added AC characteristics Removed status "advance"
*F	5727929	ANMA	05/08/2017	Section 8.3.2.2, Section 8.3.2.3 Power supply current: Removed note '"The values will be evaluated after engineering samples release" because evaluation is complete. Section 8.3.2.2, Section 8.3.2.3 Power supply current: For modes with only PD1=ON, added information that PD4_0/1 are OFF not make the condition clearer Section 3.2.2: Moved the Ethernet-pin table to chapter 3.2.1 (content not changed) Section 7.2 “Method to Switch off VCC12 during Power-off Sequence” Corrected typo of reset pin (RTSX -> RSTX) Section 8.4.11.4: Added note below waveform about PSC_1 Section 8.4.23.2 I2S Slave timing: Added timing chart fir I2S slave timing Section 9 “Abbreviation”: Added TIC because it is used in TRM’s Master access table now Section 8.3.2.2 “PPS Timer mode Shutdown”: Added note that the current consumption values are with Regulator in standby mode. Section 8.3.2.2 “PPS Stop mode Shutdown”: Added note that the current consumption values are with Regulator in standby mode. Section 8.3.2.3 “PPS Stop mode Shutdown”: Added note that the current

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				consumption values are with Regulator in standby mode. Section 8.4.16.2 “Hyper Bus Write Timing (HyperRAM): Added note to consider HyperRAM refresh interval Section 8.4.16.4 “Hyper Bus Read Timing (HyperRAM): Added note to consider HyperRAM refresh interval Section 8.3.2.2 “PSS Timer Mode Shutdown (PD6=OFF)”: Added note that values are with CR-oscillator disabled Added Section 8.3.2.4 “Internal CR oscillator current consumption Section 3.2.1 “Ethernet” (pin list): Removed duplicated line for RXER Section 4.2.1 / 4.2.2 “Package dimensions”: Exchanged pictures to correct values for A1 from (0.00 .. 0.20)mm to (0.05 .. 0.15)mm Section 8.3.2.1 “Run mode current”: Added current consumption for a specific realistic use case (635mA) (“Example use case *3”) Section 8.3.2.1 “Run mode current”: Added note and footnote *2 for the worst case scenarios, explaining that this is an ‘unlikely condition’. Section 8.3.2.3 “PSS Stop Mode current”: Updated values to latest char results Section 8.7.1 Flash Memory/Electrical Characteristics: removed *3 at ‘Max’ because there is no footnote *3
*G	5917755	ANMA	10/12/2017	Section 2.2.2 ID: Added new table for IDs for and changed Chip-IDs and JTAG-IDs for S6J32xxxxN Section 6.1 Port description: removed CRS pin because it’s only required for Ethernet-Half duplex mode which is not supported Section 6.1 Port description: Added alternative pin 34 for RXDV except for revision M Section 3.2.1. Ethernet: removed CRS and COL pin from the pin list because it’s only required for Ethernet-Half duplex mode and collision detection which are not supported Section 4.1 Pin assignment: Added alternative location of RXDV for P5_27 for all packages Section 4.1 Pin Assignment: Removed CRS and COL from all packages because half duplex mode and collision detection are not supported Section 2.2.1 Basic Option: Added revision N for RXDV-pinning improvement Section 4.1. Pin Assignment: added table listing the pin functions which are only available at certain revisions (only RXDV at pin 34 included till now) Section 2.2.1 removed revH from Figure 2-1 Section 2.2.2 removed ID-tables for revH All: removed all occurrences of revision H, because this silicon is not provided anymore Section 10 added latest ordering information, removed S6J32EELTHSC20000 because not available Section 8.1: footnote *A: added note that simulation with IBIS model should be done to confirm that clamp current is not exceeded)

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Section 4.1 Pin assignment: changed AVSS to AVSS/AVRL5 because AVSS and AVRL5 are shared, but it was not explained Section 6: Port description: added AVRL5 to AVSS row because AVSS and AVRL5 are shared Section 8.2: allowed additional two power sequences. Same as in S6J3200-Datasheet Section 5.1 I/O Circuit type: Type E (3V IO) corrected pull-up/down from 50kOhm to 33 kOhm
*H	5991338	ANMA	12/12/2017	Section 1.2 Related Documents: Updated table with links and Spec numbers. Section 10 Ordering information: Corrected the following part numbers: S6J32GEKSMSC2000A -> S6J32GEKSMSE2000A and S6J32GEKSNSC20000 -> S6J32GEKSNSE20000. Corrected package code for TEQFP-208 from LEQ208 to LET208. Entire document: Fixed spaces in tables, added missing links to Cypress web pages
*I	6197700	ANMA	06/05/2018	Section 2.2.1 ‘Basic Options’: Added revision N in Figure 2-1. Section 2.2.1 ‘Basic Options’: Added option table for revision N. Section 2.2.1 ‘ID’: Added revision N and new option H. Section 4.1.2 TEQFP-216: Added function M_CK_0 to pin 65 (no spec check, pin was already listed in section 6.1 ‘Port description list’ but not shown in the drawing). Section 6.1. Port Description: Changed description of M_SSEL0/1 and G_SSEL0/1. Section 8.2 Operation Assurance Condition: Added the % in note 4 for temperature (“35% or more”). Section 8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF): Added values for Timer mode with external clock (w/o Crystal). Section 8.3.2.4 PSS Stop mode Shutdown: Added ICCH5 values for revisions except rev M/P from latest measurement results. Section 8.4.3 Internal clock timing: Changed description of unused clocks to reflect FL00028 and Platform TRM chapter 6 RUNCKEN1/2/3 (disabling of clocks not supported). Section 10 Ordering information: Added newly available devices. Marked revM as ‘not for new designs’. All sections: Removed package M (256-pin package). Added revision P as successor of revision M for fixed Flash Interface issue-PEN.
*J	6294104	MFEU	08/29/2018	Added Section 11. Errata with one item: 1. MCAN wrong message transmission

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