

### FEATURES:

- High Density uPOL Module
- 3A Output Current
- 91% Peak Efficiency at 12VIN
- Input Voltage Range from 4.5V to 17V
- Output Voltage Range from 0.8V to 5.5V
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (OCP: Non-latching, OTP)
- Adjustable Soft Start Function
- Compact Size: 3.0mm\*2.8mm\*1.5mm
- Pb-free for RoHS compliant
- MSL 2, 260°C Reflow

### APPLICATIONS:

- Point of Load Conversion
- LDOs Replacement
- Set Top Box / DSL Modem / AP Router
- Industrial Personal Computer

### GENERAL DESCRIPTION:

The uPOL module is non-isolated dc-dc converter that can deliver up to 3A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only needs input/output capacitors and one voltage dividing resistor to perform properly.

The module has automatic operation with PWM mode and power saving mode according to loading, through constant on-time control, the module offers a simpler control loop and faster transient response. Other features include remote enable function, internal soft-start, non-latching over current protection, power good, input under voltage locked-out capability.

The low profile and compact size package (3.0mm × 2.8mm × 1.5mm) is suitable for automated assembly by standard surface mount equipment. The uPOL module is Pb-free and RoHS compliance.

### TYPICAL APPLICATION CIRCUIT & PACKAGE:

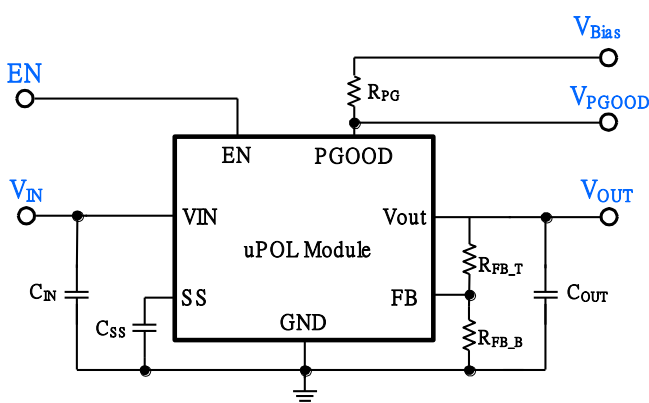


FIG.1 Typical Application Circuit

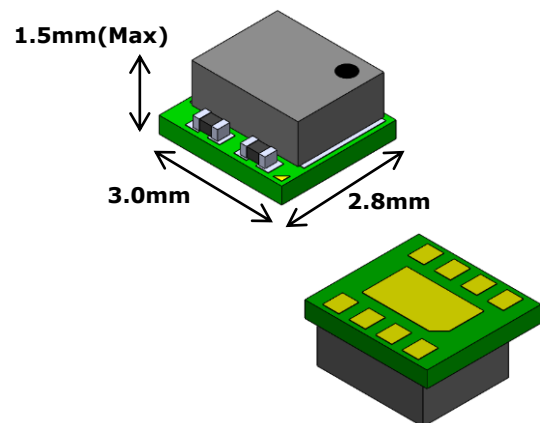
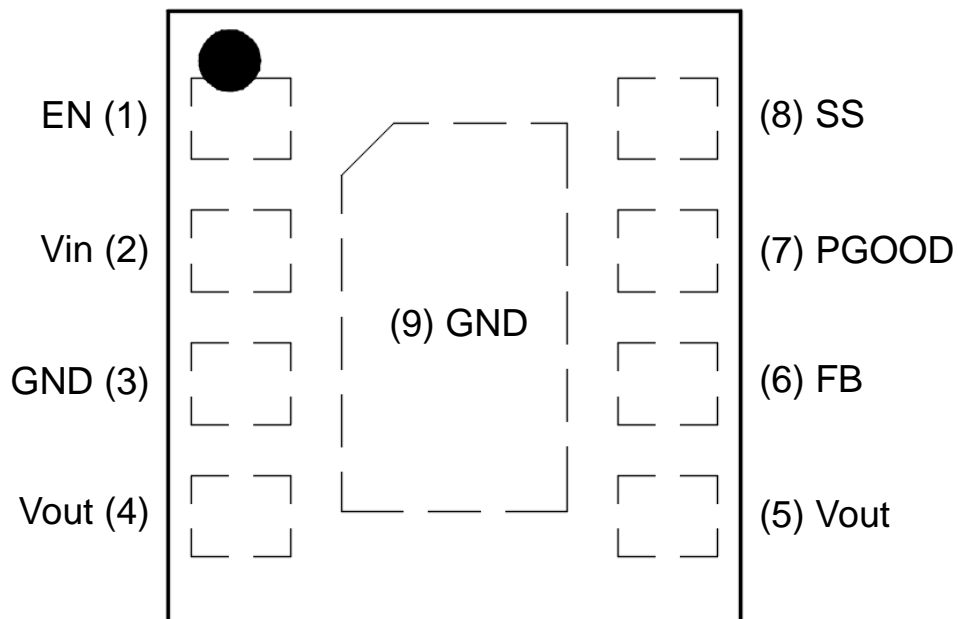


FIG.2 High Density Low Profile  
uPOL Module

**ORDER INFORMATION:**

Part Number	Operating Temperature Range (°C)	Package (Pb-Free)	MSL	Note
MUN12AD03-SEC	-40 ~ +125	DFN	Level 2	-

Order Code	Packing	Quantity
MUN12AD03-SEC	Tape and reel	2000

**PIN CONFIGURATION:**


Top View

**Fig.3 Pin configuration**

**PIN DESCRIPTION:**

<b>Symbol</b>	<b>Pin No.</b>	<b>Description</b>
EN	1	On/Off control pin for module. EN = LOW, the module is off. EN = HIGH, the module is on. Do not float.
VIN	2	Power input pin. It needs to be connected to input rail.
GND	3, 9	Power ground pin for signal, input, and output return path. This pin needs to be connected to one or more ground plane directly.
VOUT	4, 5	Power output pin. Connect to output for the load.
FB	6	Feedback input. Connect an external resistor divider to set the output voltage.
PGOOD	7	Power Good indicator. The pin output is an open drain that can connect to Vout by resistor.
SS	8	Soft startup pin.

**ELECTRICAL SPECIFICATIONS:**

CAUTION: Do not operate at or near absolute maximum rating listed for an extended period of time. This stress may adversely impact product reliability and result in failures outside of warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
<b>■ Absolute Maximum Ratings</b>					
VIN to GND		-	-	+19.0	V
VOUT to GND		-	-	+6.5	V
FB to GND		-	-	+4.0	V
EN to GND		-	-	VIN+0.3	V
PGOOD to GND		-	-	+19.0	V
Reflow Peak Temperature		-	-	+260	°C
Tc	Case Temperature of Inductor	-	-	+110	°C
Tj	Junction Temperature	-	-	+150	°C
Tstg	Storage Temperature	-40	-	+125	°C
ESD Rating	Human Body Model (HBM)	-	-	2k	V
	Machine Model (MM)	-	-	200	V
	Charge Device Model (CDM)	-	-	500	V
<b>■ Recommendation Operating Ratings</b>					
VIN	Input Supply Voltage	+4.5	-	+17.0	V
VOUT	Adjusted Output Voltage	+0.8	-	+5.5	V
PGOOD	Power Good Voltage	-	-	+17.0	V
Tj	Junction Temperature	-40	-	+125	°C
Ta	Operating Temperature Range (Note 2)	-40	-	+125	°C
<b>■ Thermal Information</b>					
Rth(jchoke-a)	Thermal resistance from junction to ambient. (Note 1)	-	39	-	°C/W

**NOTES:**

1. Rth(jchoke-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers, 1oz. The test condition is complied with JEDEC EIJ/JESD 51 Standards.
2. For maximum operating temperature, thermal derating to be taken into account.

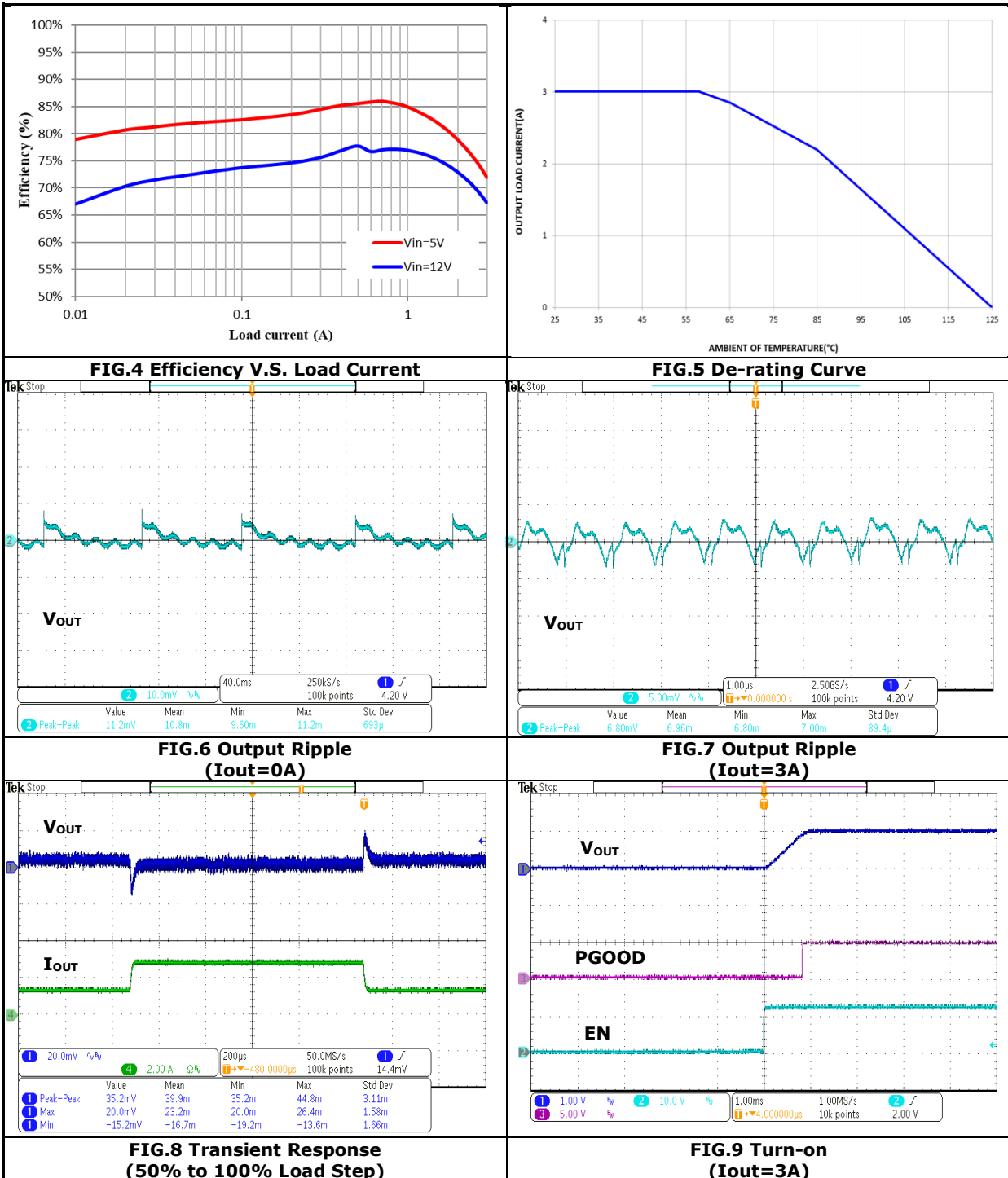
**ELECTRICAL SPECIFICATIONS: (Cont.)**

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz. The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.  $C_{in} = 10\mu\text{F}/25\text{V}/1206*1$ ,  $C_{out} = 22\mu\text{F}/10\text{V}/0805*2$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>■ Input Characteristics</b>						
$I_Q$	Quiescent current	$I_{out} = 0, V_{FB} = V_{REF} * 105\%$	-	100	-	$\mu\text{A}$
$I_{SD(IN)}$	Input shutdown current	$V_{in} = 12\text{V}, EN = \text{GND}$	-	5.5	-	$\mu\text{A}$
$I_{S(IN)}$	Input supply current	$V_{in} = 12\text{V}, EN = V_{IN}$	-	-	-	-
		$I_{out} = 0\text{A}, V_{out} = 1.8\text{V}$	-	0.13	-	$\text{mA}$
		$I_{out} = 3\text{A}, V_{out} = 1.8\text{V}$	-	0.58	-	$\text{A}$
<b>■ Output Characteristics</b>						
$I_{OUT(DC)}$	Output continuous current range		0	-	3	$\text{A}$
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line regulation accuracy	$V_{in} = 4.5\text{V to } 17\text{V}$ $V_{out} = 1.8\text{V}, I_{out} = 1.5\text{A}$	-	0.1	0.5	$\% V_{O(SET)}$
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load regulation accuracy	$I_{out} = 0.5\text{A to } 3\text{A}$ $V_{in} = 12\text{V}, V_{out} = 1.8\text{V}$	-	0.2	1	$\% V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	$V_{in} = 12\text{V}, V_{out} = 3.3\text{V}$	-	-	-	-
		$I_{out} = 0\text{A}$	-	28	-	$\text{mVp-p}$
		$I_{out} = 3\text{A}$	-	15	-	$\text{mVp-p}$
<b>■ Dynamic Characteristics</b>						
$\Delta V_{OUT-DP}$	Voltage change for positive load step	$I_{out} = 1.5\text{A to } 3\text{A}$ Current slew rate = $0.15\text{A}/\mu\text{S}$ $V_{in} = 12\text{V}, V_{out} = 1.8\text{V}$	-	25	-	$\text{mVp-p}$
$\Delta V_{OUT-DN}$	Voltage change for negative load step	$I_{out} = 3\text{A to } 1.5\text{A}$ Current slew rate = $0.15\text{A}/\mu\text{S}$ $V_{in} = 12\text{V}, V_{out} = 1.8\text{V}$	-	25	-	$\text{mVp-p}$
<b>■ Control Characteristics</b>						
$V_{FB}$	Feedback regulation voltage	PWM Mode	0.788	0.800	0.812	$\text{V}$
		PWM Mode, $T_a = -40\sim 85\text{ }^\circ\text{C}$	0.78	0.800	0.82	$\text{V}$
		PFM Mode, $T_a = -40\sim 85\text{ }^\circ\text{C}$	0.788	0.800	0.824	$\text{V}$
$D_{MAX}$	Maximum duty cycle	$V_{out(MAX)} = V_{in} * D_{MAX}$	70	-	-	$\%$
$F_{OSC}$	Oscillator frequency	PWM Operation	-	1.0	-	$\text{MHz}$
$V_{UVLO}$	Input UVLO threshold		-	-	4.5	$\text{V}$
$V_{PG}$	Power good threshold	$V_{FB}$ rising	88	90	92	$\% V_{REF}$
$V_{PG,HYS}$	Power good hysteresis			2		$\% V_{REF}$
$V_{PGL}$	PGOOD output low	$I_{PGOOD} = 4\text{mA}$	0.04	0.15	0.3	$\text{V}$
$V_{EN\_TH}$	Enable rising threshold voltage		1.5	-	-	$\text{V}$
	Enable falling threshold voltage		-	-	0.4	$\text{V}$
$T_{OTP}$	Over temp protection		-	150	-	$^\circ\text{C}$
OCP	Protection Output Current		3.8	-	5.2	$\text{A}$

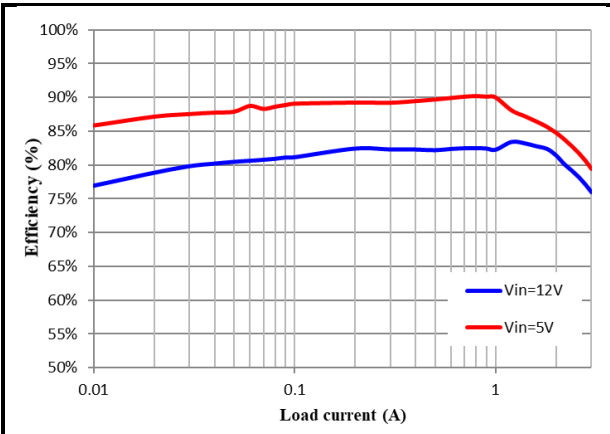
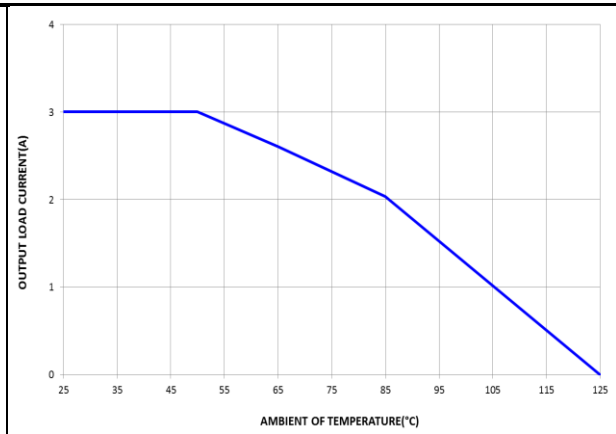
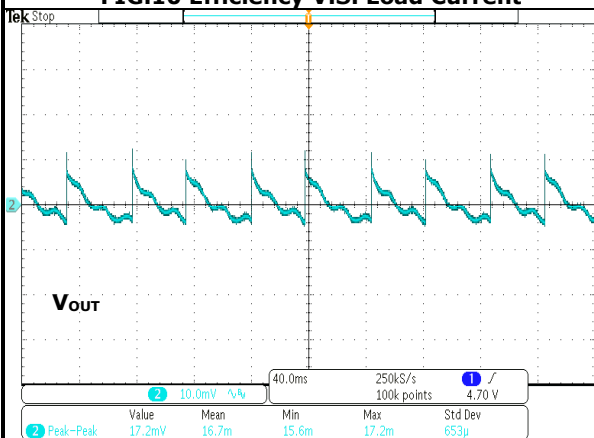
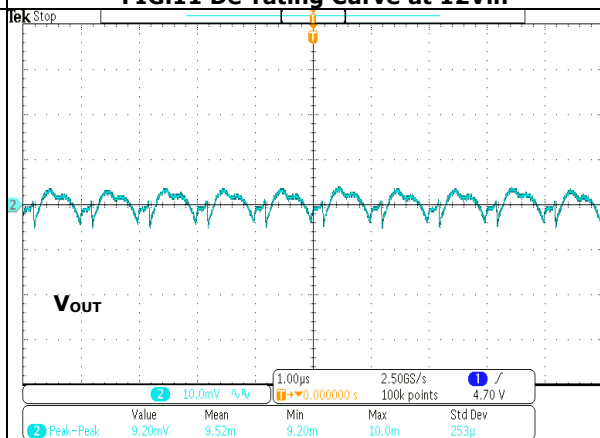
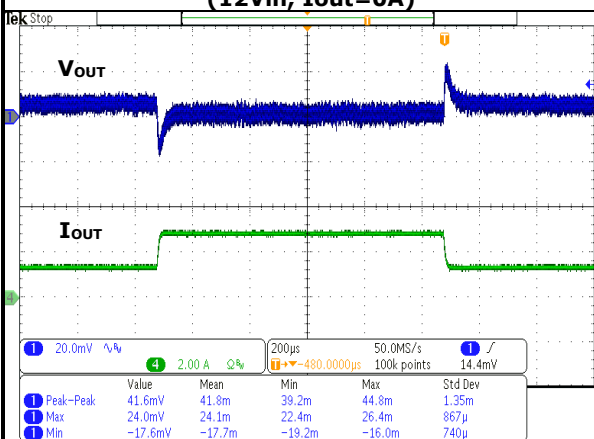
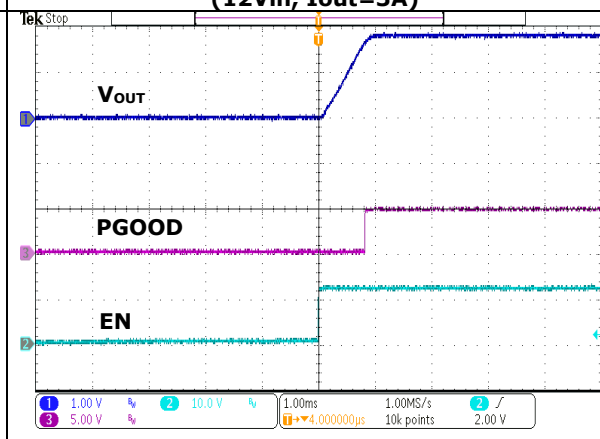
## TYPICAL PERFORMANCE CHARACTERISTICS: (1.0VOUT)

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz. The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.  $V_{in} = 12\text{ V}$ ,  $V_{out} = 1.0\text{ V}$ , unless otherwise noted.  $C_{in} = 10\mu\text{F}/25\text{V}/1206*1$ ,  $C_{out} = 22\mu\text{F}/10\text{V}/0805*2$ .



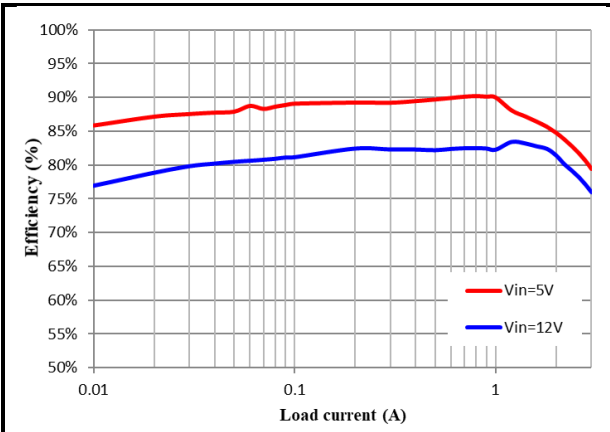
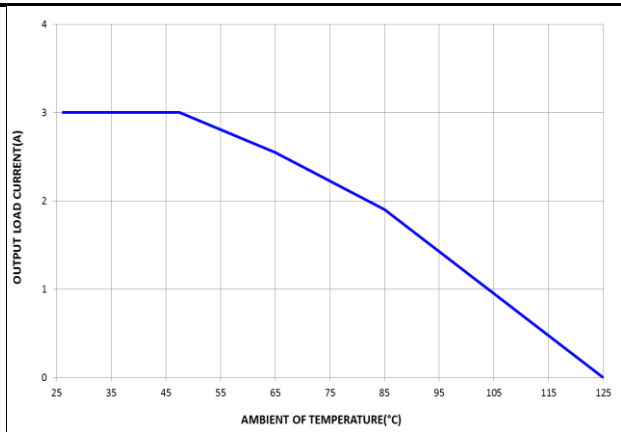
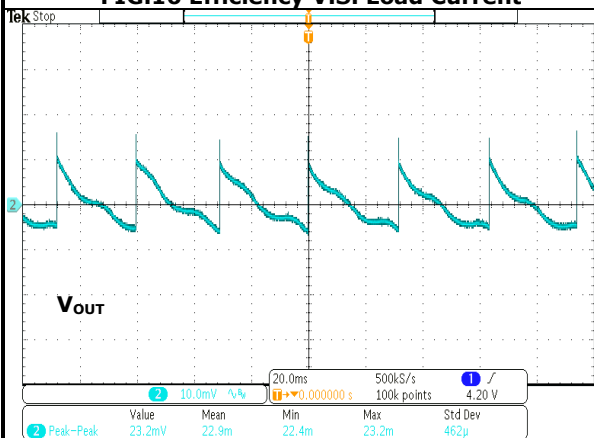
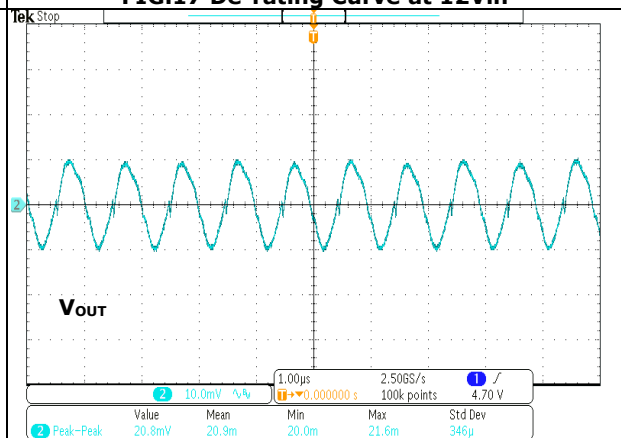
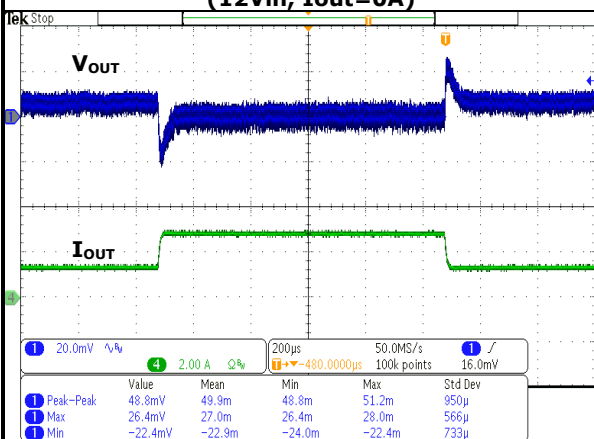
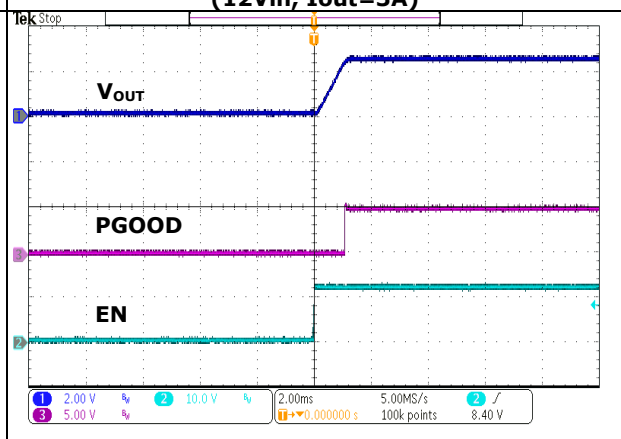
**TYPICAL PERFORMANCE CHARACTERISTICS: (1.8VOUT)**

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz. The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.  $V_{in} = 12\text{ V}$ ,  $V_{out} = 1.8\text{ V}$ , unless otherwise noted.  $C_{in} = 10\mu\text{F}/25\text{V}/1206*1$ ,  $C_{out} = 22\mu\text{F}/10\text{V}/0805*2$ .


**FIG.10 Efficiency V.S. Load Current**

**FIG.11 De-rating Curve at 12Vin**

**FIG.12 Output Ripple (12Vin, Iout=0A)**

**FIG.13 Output Ripple (12Vin, Iout=3A)**

**FIG.14 Transient Response (12Vin, 50% to 100% Load Step)**

**FIG.15 Turn-on (12Vin, Iout=3A)**

**TYPICAL PERFORMANCE CHARACTERISTICS: (2.5VOUT)**

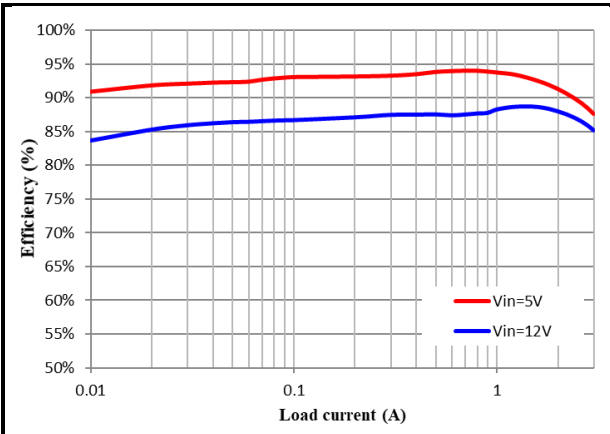
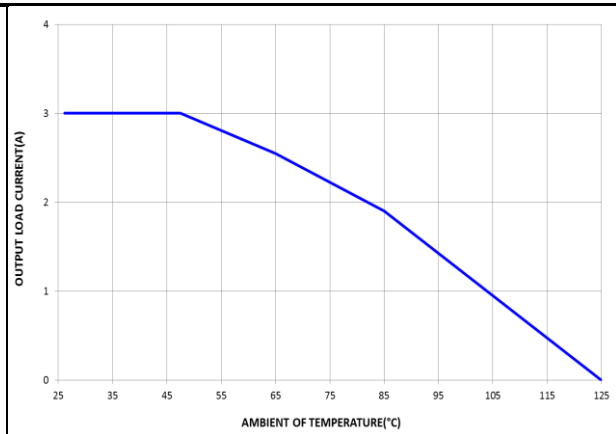
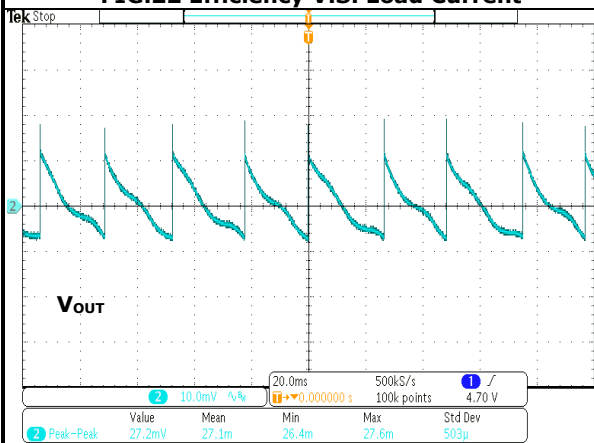
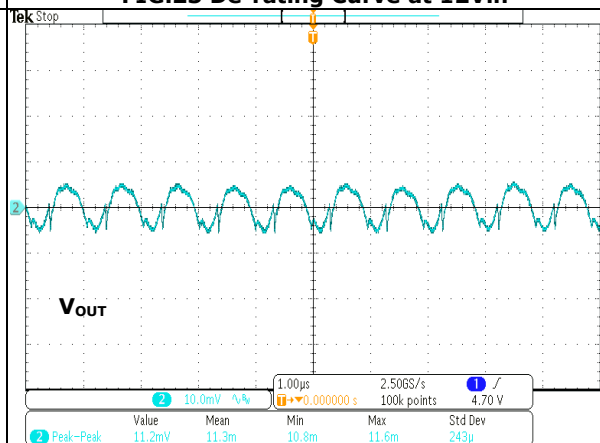
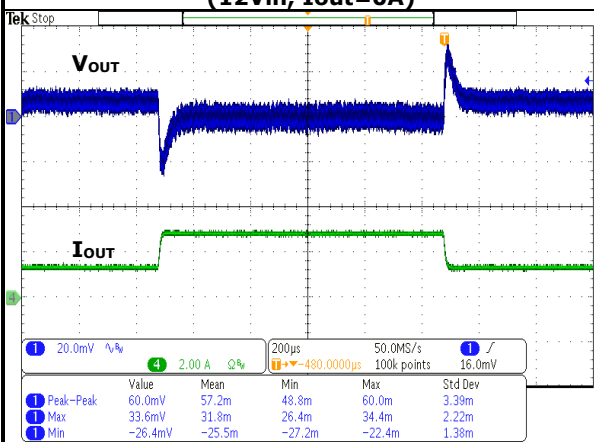
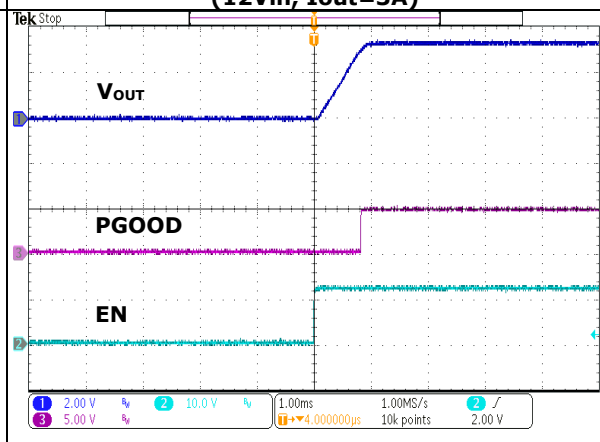
Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz. The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.  $V_{in} = 12\text{ V}$ ,  $V_{out} = 3.3\text{ V}$ , unless otherwise noted.  $C_{in} = 10\mu\text{F}/25\text{V}/1206*1$ ,  $C_{out} = 22\mu\text{F}/10\text{V}/0805*2$ .


**FIG.16 Efficiency V.S. Load Current**

**FIG.17 De-rating Curve at 12Vin**

**FIG.18 Output Ripple (12Vin, Iout=0A)**

**FIG.19 Output Ripple (12Vin, Iout=3A)**

**FIG.20 Transient Response (12Vin, 50% to 100% Load Step)**

**FIG.21 Turn-on (12Vin, Iout=3A)**



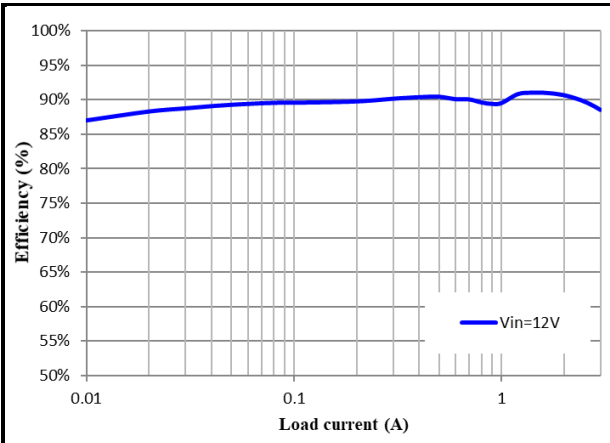
**TYPICAL PERFORMANCE CHARACTERISTICS: (3.3VOUT)**

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz. The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.  $V_{in} = 12\text{ V}$ ,  $V_{out} = 3.3\text{ V}$ , unless otherwise noted.  $C_{in} = 10\mu\text{F}/25\text{V}/1206*1$ ,  $C_{out} = 22\mu\text{F}/10\text{V}/0805*2$ .

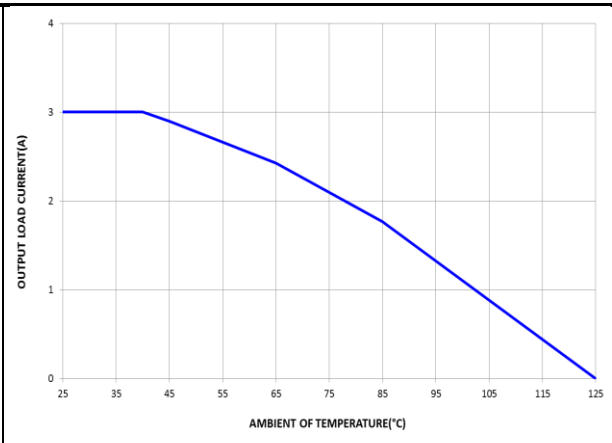

**FIG.22 Efficiency V.S. Load Current**

**FIG.23 De-rating Curve at 12Vin**

**FIG.24 Output Ripple (12Vin, Iout=0A)**

**FIG.25 Output Ripple (12Vin, Iout=3A)**

**FIG.26 Transient Response (12Vin, 50% to 100% Load Step)**

**FIG.27 Turn-on (12Vin, Iout=3A)**

## TYPICAL PERFORMANCE CHARACTERISTICS: (5.0VOUT)

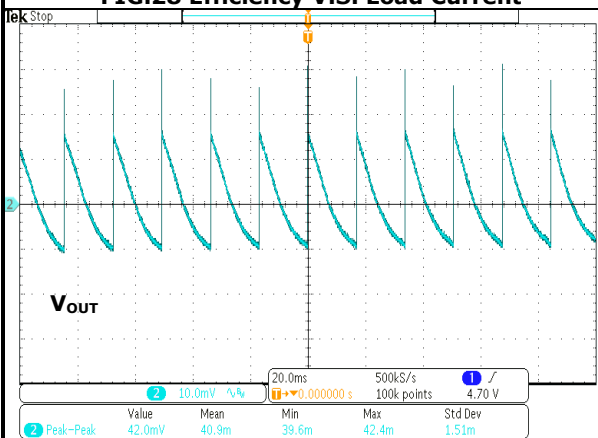
Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz. The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.  $V_{in} = 12\text{ V}$ ,  $V_{out} = 5.0\text{ V}$ , unless otherwise noted.  $C_{in} = 10\mu\text{F}/25\text{V}/1206*1$ ,  $C_{out} = 22\mu\text{F}/10\text{V}/0805*2$ .



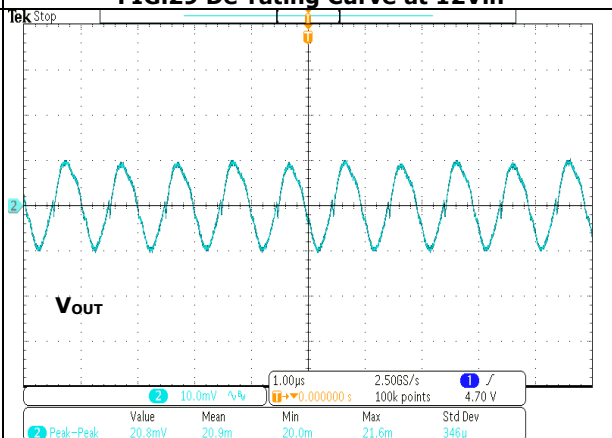
**FIG.28 Efficiency V.S. Load Current**



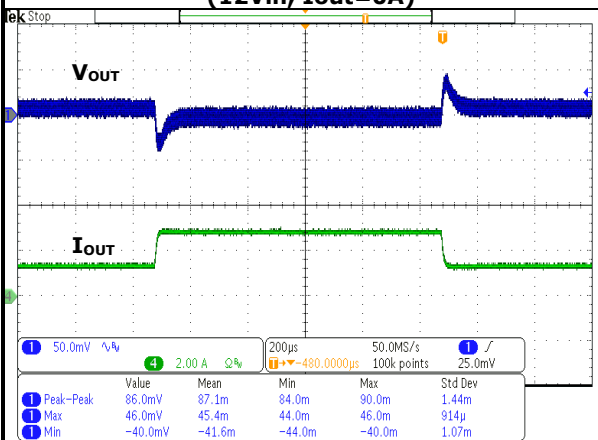
**FIG.29 De-rating Curve at 12Vin**



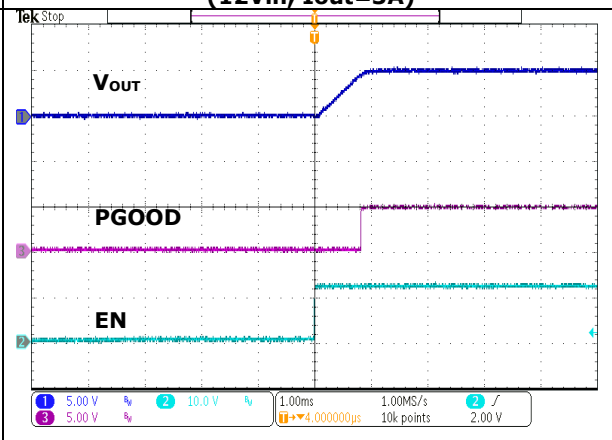
**FIG.30 Output Ripple (12Vin, Iout=0A)**



**FIG.31 Output Ripple (12Vin, Iout=3A)**



**FIG.32 Transient Response (12Vin, 50% to 100% Load Step)**



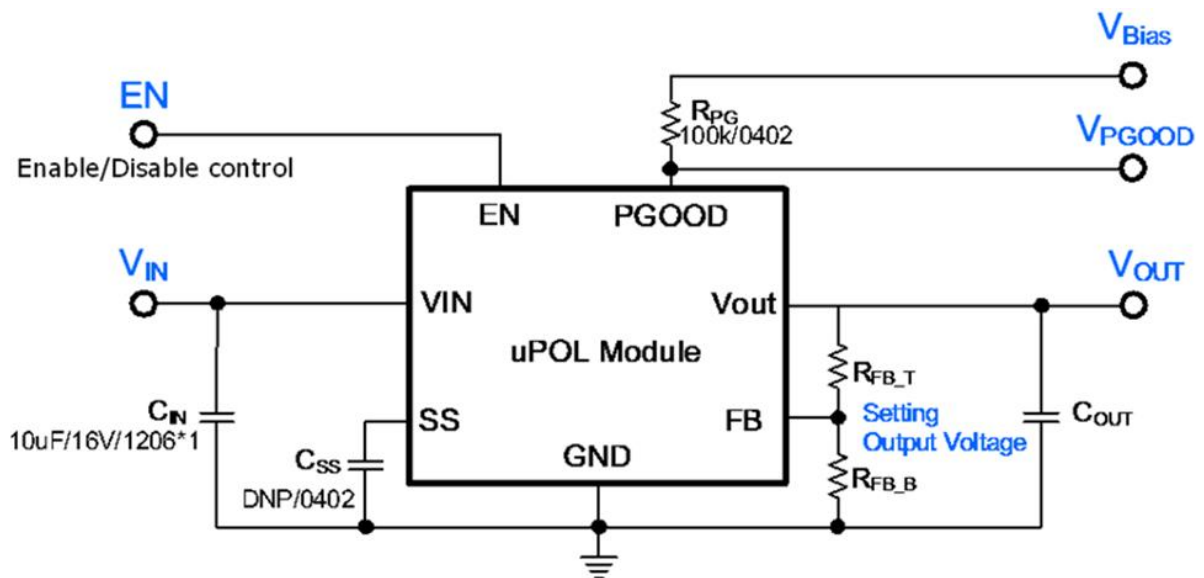
**FIG.33 Turn-on (12Vin, Iout=3A)**

**APPLICATIONS INFORMATION:**
**REFERENCE CIRCUIT FOR GENERAL APPLICATION:**

Figure 34 show the module application schematics for input voltage +12V. The output capacitor is selected to handle the output ripple noise requirements and system stability. The out capacitance have to be followed  $C_{OUT\_Min}$  shown in the TABLE 1

**TABLE 1 Output capacitor setting**

$V_{IN}$ (V)	$V_{OUT}$ (V)	$C_{OUT\_Min}$ (uF)
4.5~17	1	22
4.5~17	1.2	22
4.5~7	1.5	22*2
8~17	1.5	22
4.5~7	1.8	22*2
8~17	1.8	22
5~17	3.3	22*2
7~17	5	22*2


**FIG.34 Reference Circuit for General Application**

**APPLICATIONS INFORMATION: (Cont.)****SAFETY CONSIDERATIONS:**

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

**INPUT FILTERING:**

The module should be connected to a source supply of low AC impedance and high inductance in which line inductance can affect the module stability. An input capacitor must be placed as near as possible to the input pin of the module so to minimize input ripple voltage and ensure module stability.

**OUTPUT FILTERING:**

To reduce output ripple and improve the dynamic response as the step load changes, an additional capacitor at the output must be connected. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

**PROGRAMMING OUTPUT VOLTAGE:**

The module has an internal  $0.8V \pm 1.5\%$  reference voltage. The output voltage can be programmed by the dividing resistor ( $R_{FB\_T}$  and  $R_{FB\_B}$ ). The output voltage can be calculated by Equation 1, resistor choice may be referred to TABLE 2.

$$V_{OUT}(V) = 0.8 \times \left(1 + \frac{R_{FB\_T}}{R_{FB\_B}}\right) \quad (EQ.1)$$

**TABLE 2 Resistor values for common output voltages**

$V_{OUT}$ (V)	$R_{FB\_T}(k\Omega)$	$R_{FB\_B}(k\Omega)$
1.0	124	499
1.2	124	243
1.5	124	140
1.8	124	100
3.3	124	39.2
5.0	124	23.7

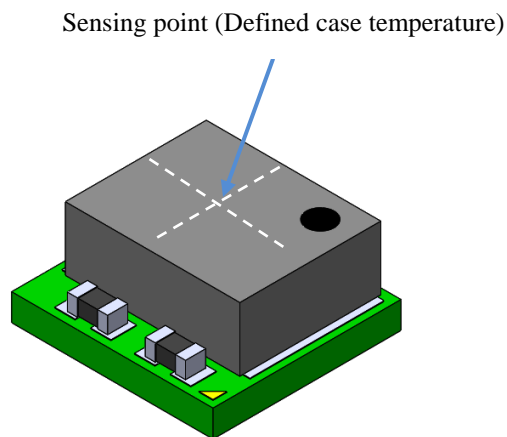
**APPLICATIONS INFORMATION: (Cont.)**
**Soft Startup Capacitor Selection**

Leave SS pin floating for default 1ms soft-start time. For longer than 1ms soft-start time, connect a capacitance between the SS pin and the GND allows programming the startup slope of the output voltage. A constant current of 4  $\mu$ A charges the external capacitor. The capacitance required for a given soft startup time for the output voltage is given by Equation 2:

$$C_{SS} = t_{SS} \times \frac{4\mu A}{0.8V} \quad (\text{EQ.2})$$

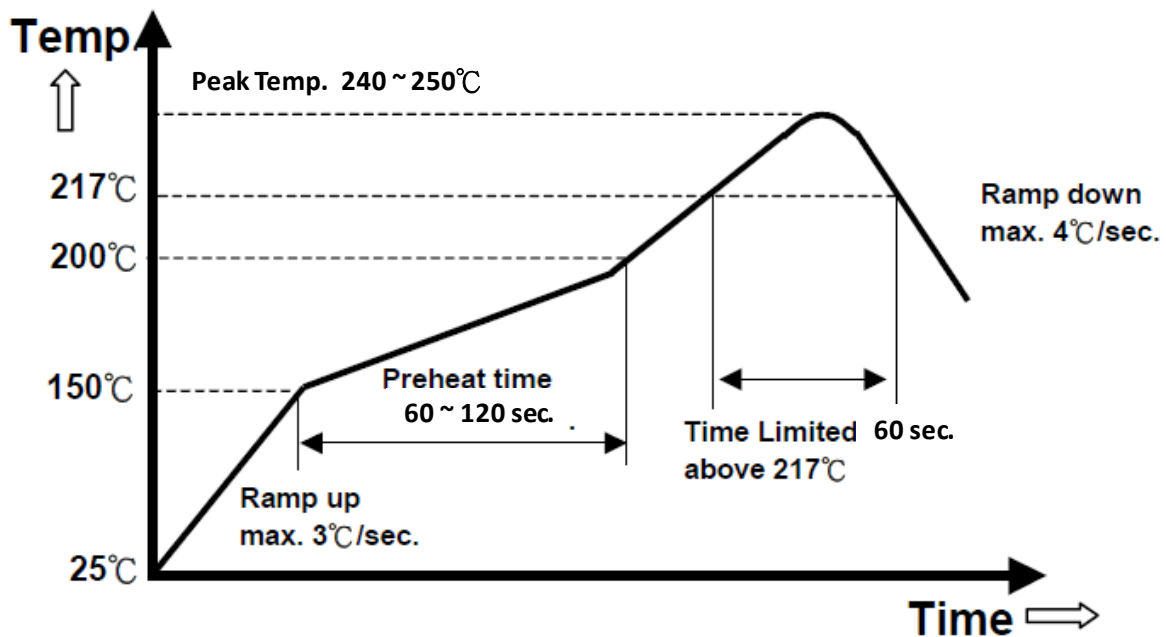
**Thermal Considerations:**

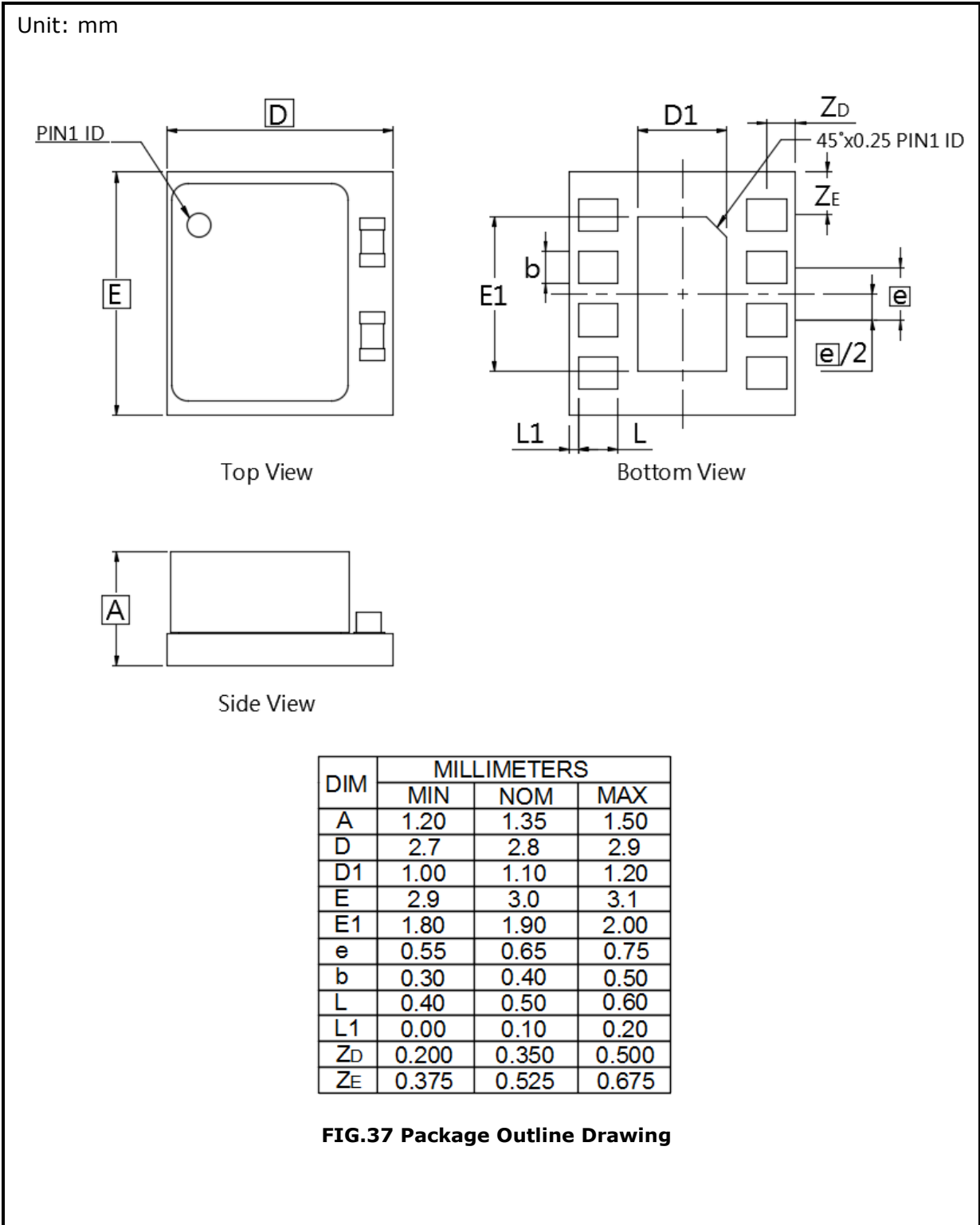
All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 2 layers. The case temperature of module sensing point is shown as Figure 35. Then  $R_{th(jchoke-a)}$  is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The MUN12AD03-SEC modules are designed for using when the case temperature is below 125°C regardless the change of output current, input/output voltage or ambient temperature.


**FIG. 35 Case Temperature Sensing Point**

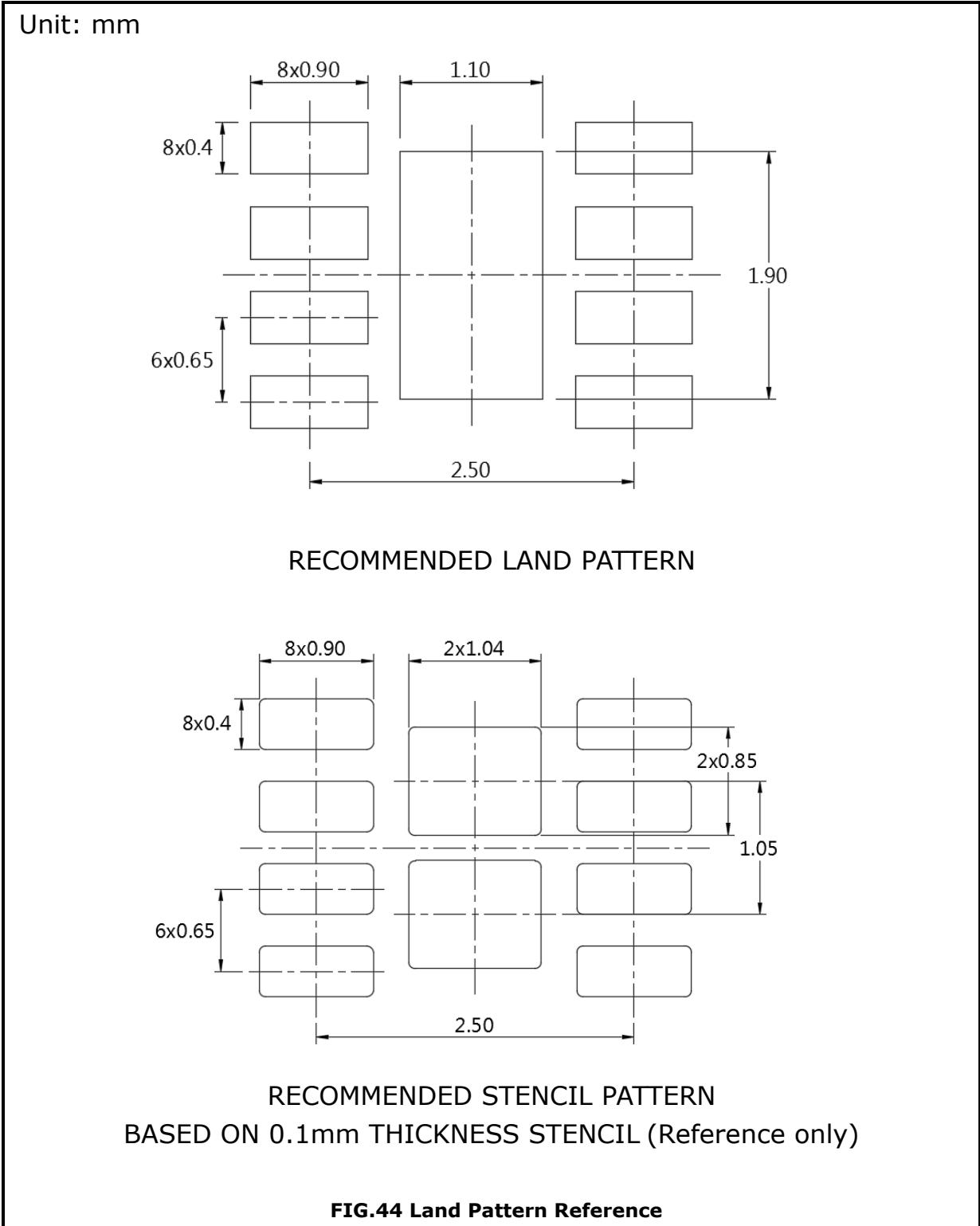
**REFLOW PARAMETERS:**

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 36 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.


**FIG.36 Recommendation Reflow Profile**

**PACKAGE OUTLINE DRAWING:**


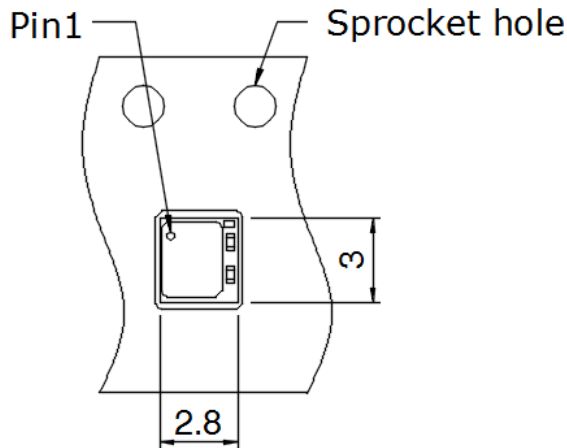
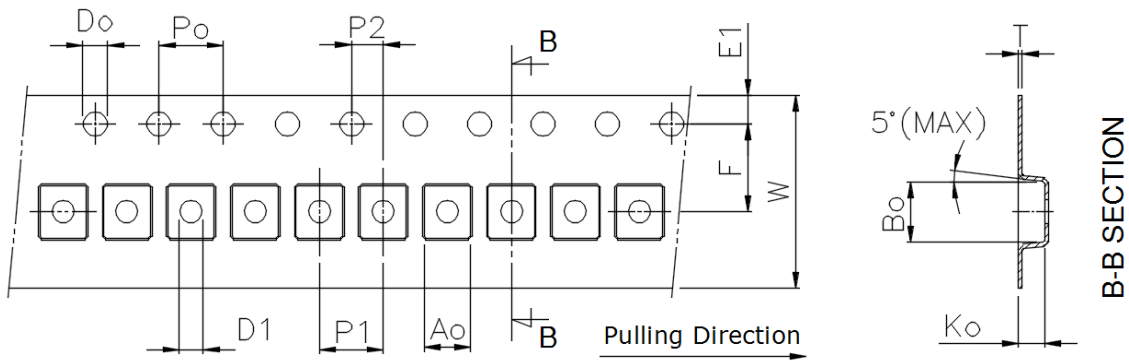
**LAND PATTERN REFERENCE:**





**PACKING REFERENCE:**

Unit: mm

**Package In Tape Loading Orientation**

**Tape Dimension**


A0	3.20 ± 0.10	E1	1.75 ± 0.10
B0	3.30 ± 0.10	K0	1.65 ± 0.10
F	5.50 ± 0.05	P0	4.00 ± 0.10
W	12.00 ± 0.30	P1	4.00 ± 0.10
D0	φ1.55 ± 0.05	P2	2.00 ± 0.05
D1	φ1.5 + 0.1/-0	T	0.25 ± 0.10

**FIG.38 Packing Reference**

**PACKING REFERENCE: (Cont.)**

Unit: mm

### Reel Dimension

See Detail A

Detail A

### Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.  
 The peel force of top cover tape shall be between 0.1N to 1.3N

TOP COVER TAPE

165~180°

0.1~1.3N

**REVISION HISTORY:**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
2020.07.22	00	Release the preliminary specification.
2022.02.21	01	Update module outline drawing.

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