uPOL Module

6A, High Efficiency uPOL Module

MUN12AD06-SM

FEATURES:

- High Density uPOL Module
- 6A Output Current
- Input Voltage Range from 4.5V to 24V
- Output Voltage Range from 0.6V to 6.0V
- 93% Peak Efficiency(@Vin=12V)
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (OCP, OTP, SCP, OVP, Non-latching)
- Internal Soft Start
- Compact Size: 6mm*6mm*3.5mm(Max)
- Pb-free for RoHS compliant
- MSL 2, 250℃ Reflow

APPLICATIONS:

- Distributed Power Supply
- Server, Workstation, and Storage
- Networking and Datacom

GENERAL DESCRIPTION:

The uPOL module is non-isolated dc-dc converters that can deliver up to 6A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package.

The module has automatic operation with PWM mode and power saving mode according to loading. Instant PWM architecture to achieve fast transient responses. Other features include remote enable function, internal soft-start, non-latching over current protection and power good.

The low profile and compact size package (6.0mm × 6.0mm x 3.5mm) is suitable for automated assembly by standard surface mount equipment. The uPOL module is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT:

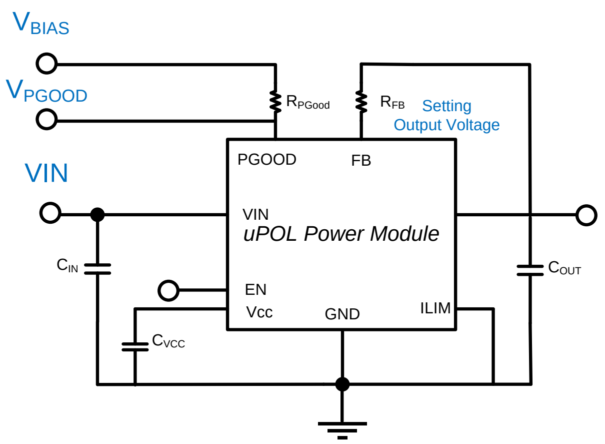


FIGURE. 1 TYPICAL APPLICATION CIRCUIT

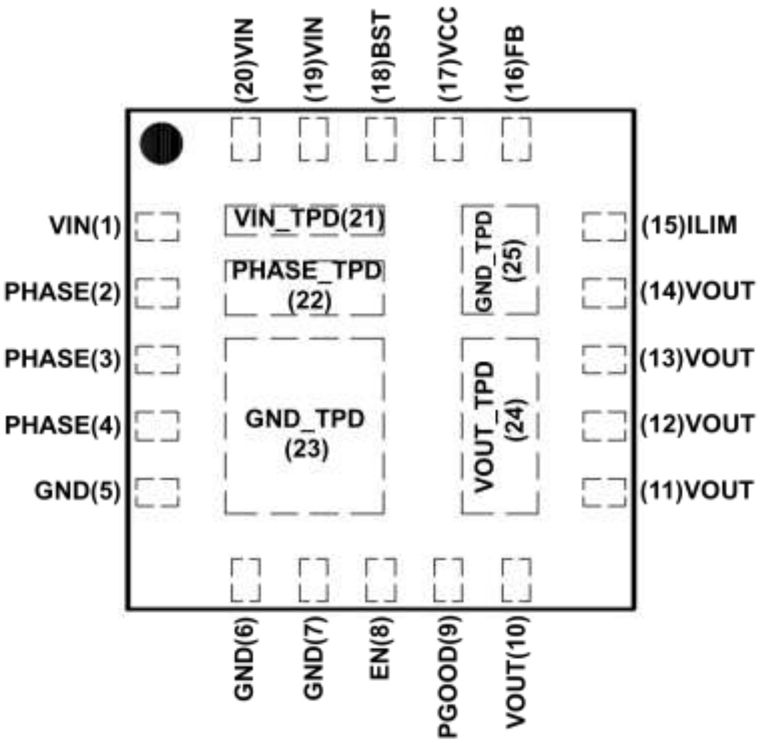
FIGURE. 2 HIGH DENSITY LDS MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MUN12AD06-SM	-40 ~ +85	QFN	Level 2	-

Order Code	Packing	Quantity
MUN12AD06-SM	Tape and reel	1000

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
VIN	1, 19, 20	Power input pin. It needs to connect input rail and thermal exposed pad of VIN_TPD(21) for heat transferring. Place the input ceramic type capacitor as closely as possible to this pin. One capacitor of 22uF at least for input capacitance.
PHASE	2, 3, 4	Switch output. Connect to thermal exposed pad of PHASE_TPD(22) for heat transferring.
GND	5, 6, 7	Power ground pin for signal, input, and output return path. This pin needs to connect one or more ground plane directly. Connect to thermal exposed pad of GND_TPD(23, 25) for heat transferring.
EN	8	On/Off control pin for module.
PGOOD	9	Power good signal pin. Open drain output when the output voltage is within 90% to 120% of regulation point.
VOUT	10, 11, 12, 13, 14	Power output pin. Connect to output and thermal exposed pad of VOUT_TPD(24) for heat transferring. Place the output capacitors as closely as possible to this pin.
ILIM	15	Current limit setting pin. Connect to GND for current limit setting.
FB	16	Feedback input. Connect an external resistor divider from the VOUT to FB to program the output voltage.
VCC	17	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Connect a 2.2uF for Bypass capacitor.
BST	18	Boot-Strap Pin. No need connect.
VIN_TPD	21	Power input pin. Connect input rail and using for heat transferring to heat dissipation layer by Vias connection.
PHASE_TPD	22	Phase node pin. Using for heat transferring to heat dissipation layer by Vias connection.
GND_TPD	23, 25	Power ground pin. It needs to connect one or more ground plane directly and using for heat transferring to heat dissipation layer by Vias connection.
VOUT_TPD	24	Power output pin. Connect to output and using for heat transferring to heat dissipation layer by Vias connection.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-	-	+30.0	V
VOUT to GND		-	-	+7.0	V
PHASE to GND		-	-	+30.0	V
PGOOD to GND		-	-	+30.0	V
ILIM to GND		-	-	+4.0	V
VCC to GND		-	-	+4.0	V
FB to GND		-	-	+4.0	V
EN to GND		-	-	+30.0	V
Tc	Case Temperature of Inductor	-	-	+110	˚C
Tstg	Storage Temperature	-40	-	+125	˚C
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.5	-	+24	V
VOUT	Adjusted Output Voltage(Note 1)	+0.6	-	+6.0	V
Ta	Ambient Temperature	-40	-	+85	˚C
■ Thermal Information					
$R_{th}(j_{choke}\text{-}a)$	Thermal resistance from junction to ambient (Note 2)	-	22	-	°C/W

NOTES:

1. $R_{th}(j_{choke}\text{-}a)$ is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Vin=12V Vout=3.3V
Cin = 4.7uF/50V/1206x2、100/25V/0805x1, Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{SD(IN)}$	Input shutdown current	Vin =12V, EN = GND	-	10	-	uA
$I_{Q(IN)}$	Input supply bias current	Vin = 12V, Iout = 10mA Vout = 3.3V, EN = VIN	-	300	-	uA
$I_{S(IN)}$	Input supply current	Vin = 12V, EN = VIN				
		Iout = 10mA,Vout =3.3V	-	2	-	mA
		Iout = 6A,Vout =3.3V	-	1.8	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range		0	-	6	A
$V_{O(SET)}$	Ouput Voltage Set Point	With 0.1% tolerance for external resistor used to set output voltage(Iout=3A)	-2%	-	+2%	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	Vin = 7.0V to 15V Vout = 3.3V, Iout = 10mA Vout = 3.3V, Iout = 6A	-	0.5%	-	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	Iout = 10mA to 6A Vin = 12V, Vout = 3.3V	-3%	-	+4%	% $V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	Vin = 12V, Vout = 3.3V EN = VIN,20MHz Bandwidth	-	-	-	-
		IOUT = 10mA	-	40	-	mVp-p
		IOUT = 6A	-	16	-	mVp-p
■ Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	Iout = 3 A to 6A Current slew rate = 0.15A/uS Vin = 12V, Vout = 3.3V	-	30	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	Iout = 6A to 3A Current slew rate = 0.15A/uS Vin = 12V, Vout = 3.3V	-	30	-	mVp-p
■ Control Characteristics						
F_{OSC}	Oscillator frequency		-	0.8	-	MHz
V_{REF}	Referance voltage		0.594	0.600	0.606	V
V_{PG}	Power good threshold	Vout = 3.3V	88	90	92	% V_{REF}
V_{PGL}	Power good LOW	I_{POOG}=4mA	0.04	0.15	0.3	
I_{ILIM}	Over current limit		8		14	A
V_{ENL}	EN Low threshold		0	-	0.4	V
V_{ENH}	EN High Threshold		1.7	-	VIN	V
OVP	Output Over Voltage protection	V_{FB} Rising	-	115	-	%V_{REF}
Duty	Duty Cycle		-	-	80	%

TYPICAL PERFORMANCE CHARACTERISTICS: (1.0VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/50V/1206x2、100nF/25V/0805x1, Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 1.0Vout.

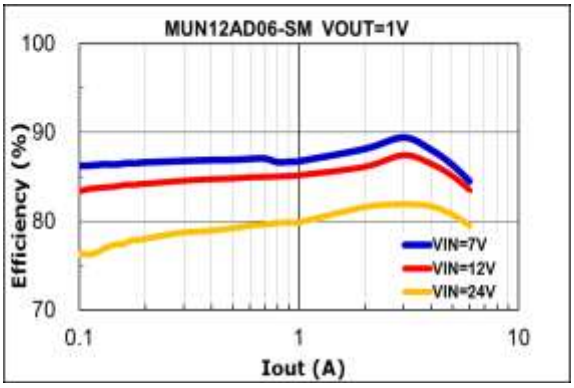


FIG.3 EFFICIENCY V.S. LOAD CURRENT

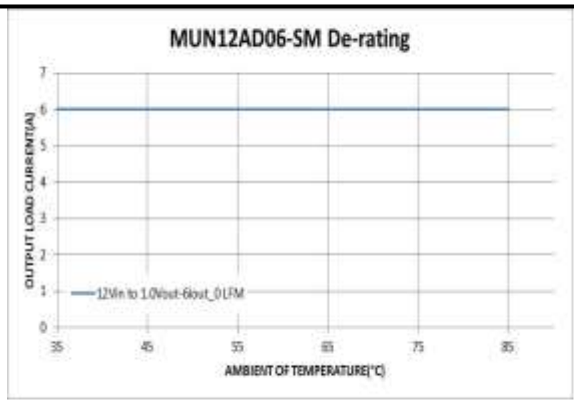


FIG.4 12VIN DE-RATING CURVE

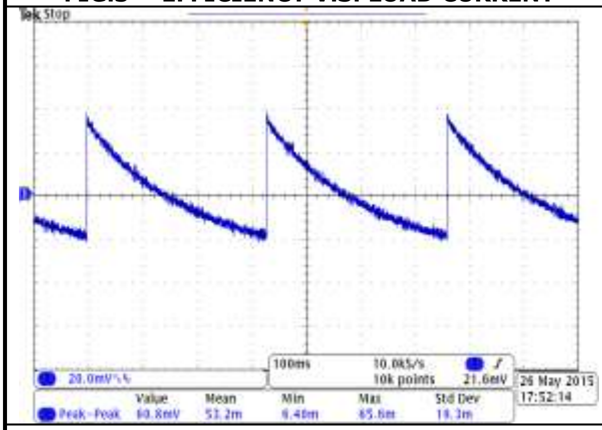


FIG.5 OUTPUT RIPPLE
(12VIN, 1VOUT, IOUT=0A)

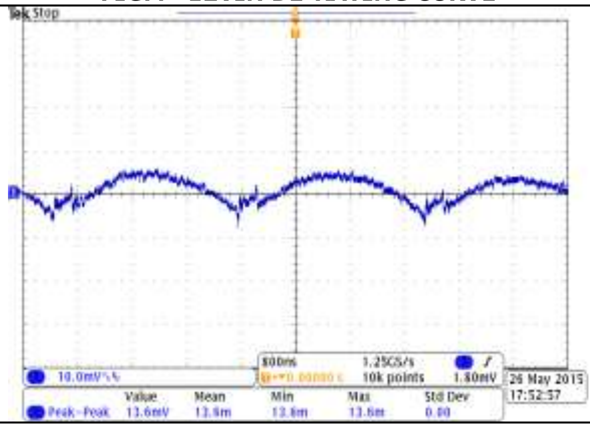


FIG.6 OUTPUT RIPPLE
(12VIN, 1VOUT, IOUT=6A)

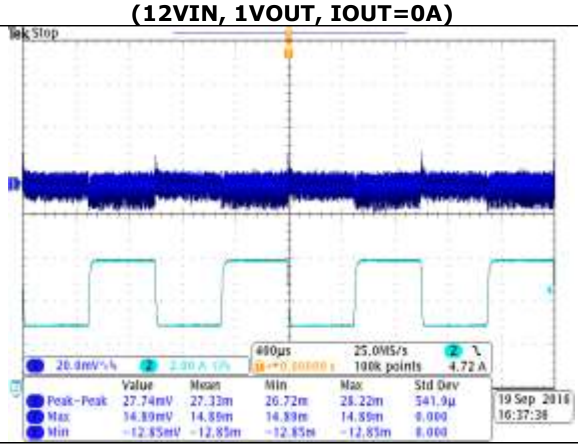


FIG.7 TRANSIENT RESPONSE
(12VIN, 1VOUT, 50% to 100% LOAD STEP)

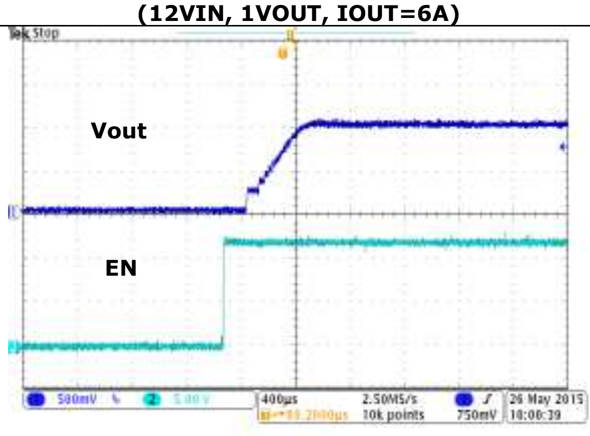


FIG.8 TURN-ON
(12VIN, 1VOUT, IOUT=6A)

TYPICAL PERFORMANCE CHARACTERISTICS: (1.2VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/50V/1206x2、100nF/25V/0805x1, Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 1.2Vout.

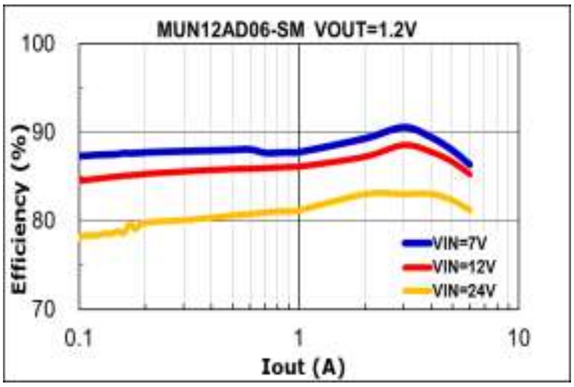


FIG.9 EFFICIENCY V.S. LOAD CURRENT

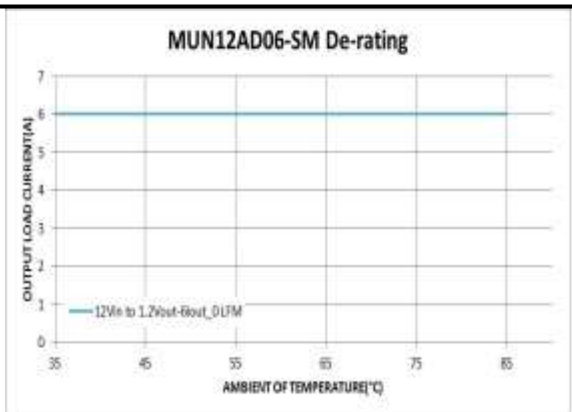


FIG.10 12VIN DE-RATING CURVE

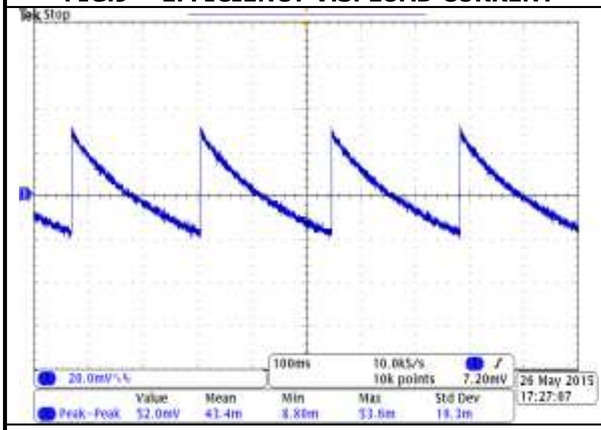


FIG.11 OUTPUT RIPPLE
(12VIN, 1.2VOUT, IOUT=0A)

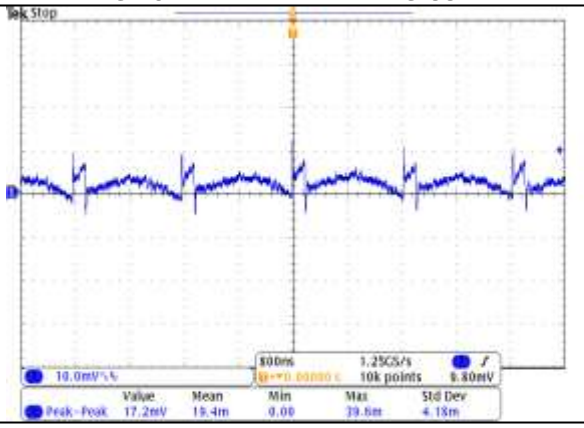


FIG.12 OUTPUT RIPPLE
(12VIN, 1.2VOUT, IOUT=6A)

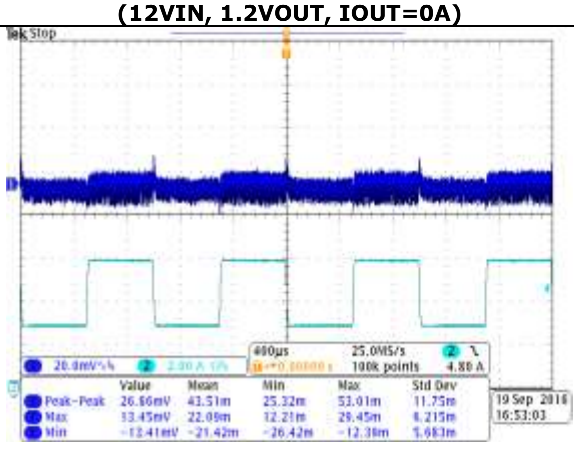


FIG.13 TRANSIENT RESPONSE
(12VIN, 1.2VOUT, 50% to 100% LOAD STEP)

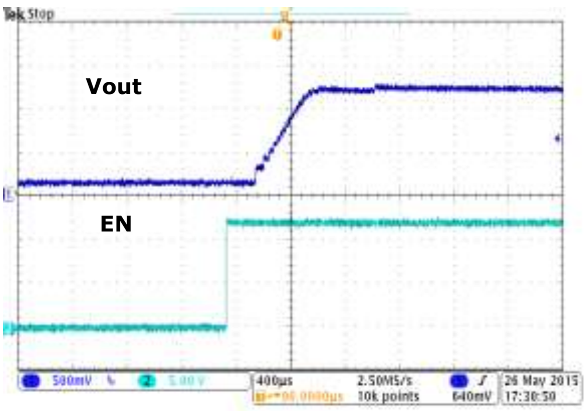


FIG.14 TURN-ON
(12VIN, 1.2VOUT, IOUT=6A)

TYPICAL PERFORMANCE CHARACTERISTICS: (1.8VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/50V/1206x2、100nF/25V/0805x1, Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 1.8Vout.

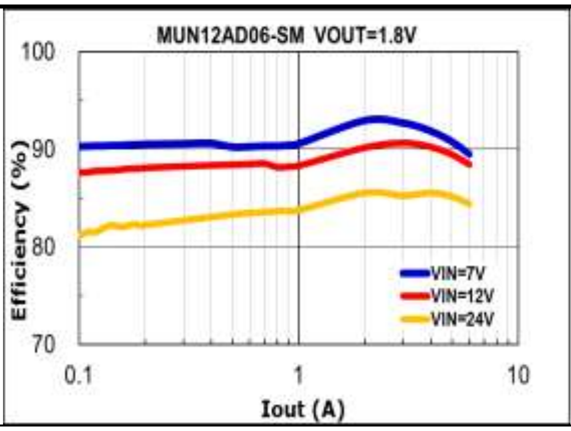


FIG.15 EFFICIENCY V.S. LOAD CURRENT

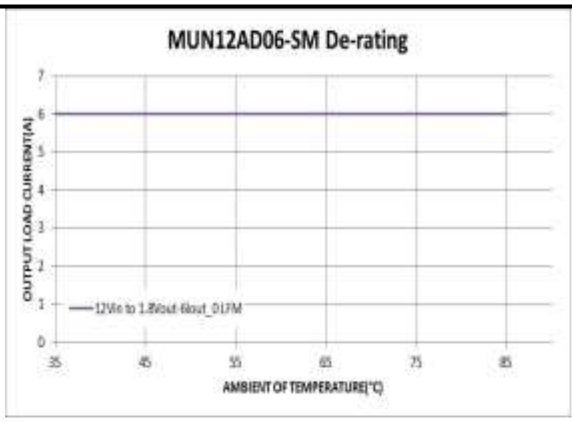


FIG.16 12VIN DE-RATING CURVE

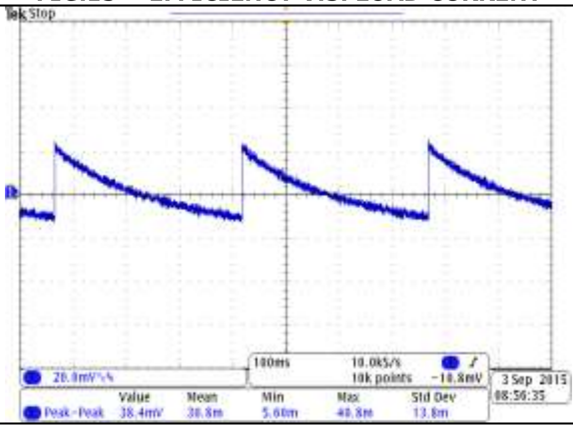


FIG.17 OUTPUT RIPPLE
(12VIN, 1.8VOUT, IOUT=0A)

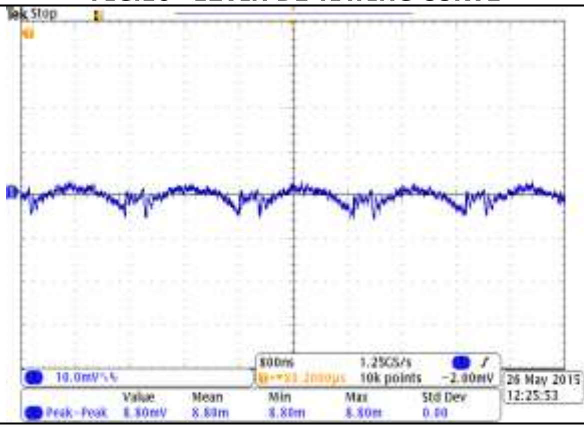


FIG.18 OUTPUT RIPPLE
(12VIN, 1.8VOUT, IOUT=6A)

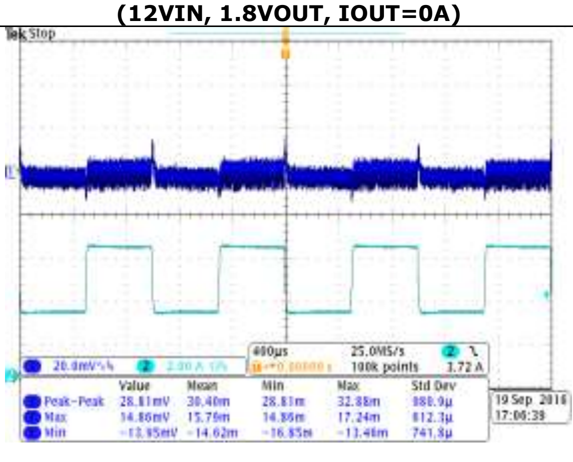


FIG.19 TRANSIENT RESPONSE
(12VIN, 1.8VOUT, 50% to 100% LOAD STEP)

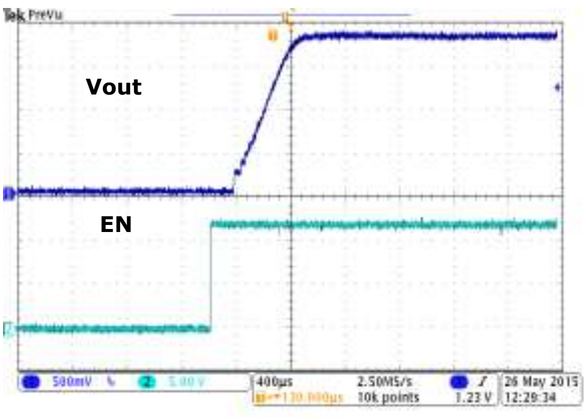


FIG.20 TURN-ON
(12VIN, 1.8VOUT, IOUT=6A)

TYPICAL PERFORMANCE CHARACTERISTICS: (2.5VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/50V/1206x2、100nF/25V/0805x1, Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 2.5Vout.

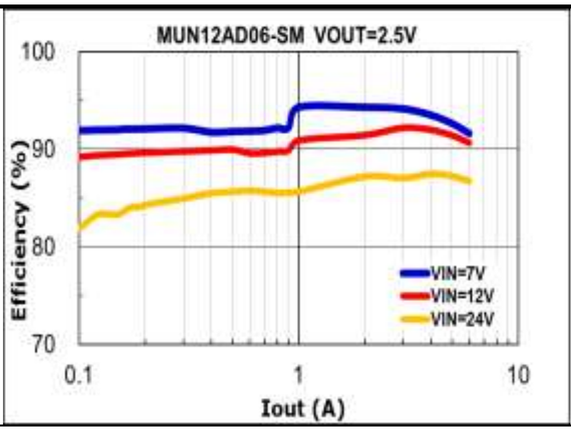


FIG.21 EFFICIENCY V.S. LOAD CURRENT

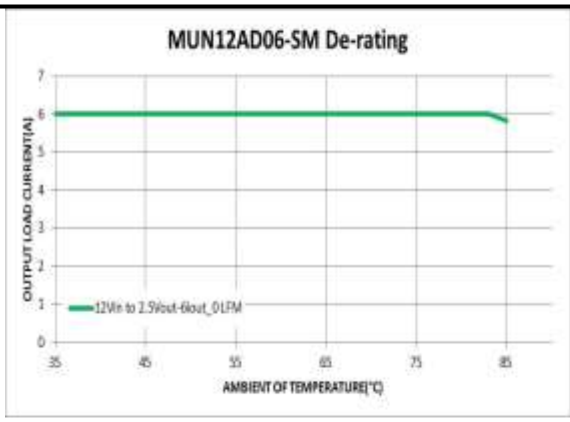


FIG.22 12VIN DE-RATING CURVE

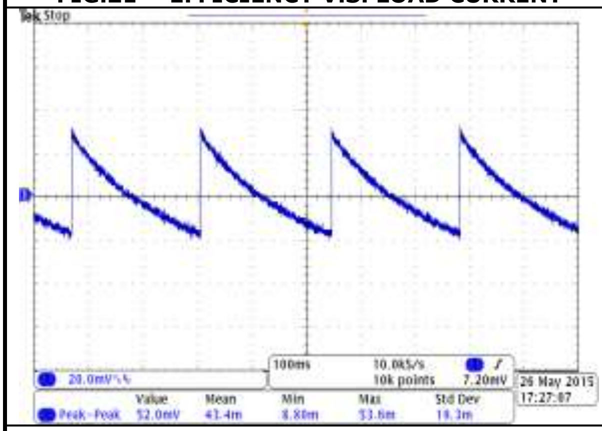


FIG.23 OUTPUT RIPPLE
(12VIN, 2.5VOUT, IOUT=0A)

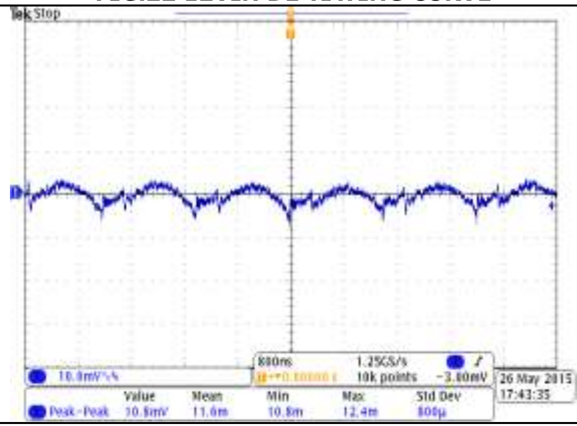


FIG.24 OUTPUT RIPPLE
(12VIN, 2.5VOUT, IOUT=6A)

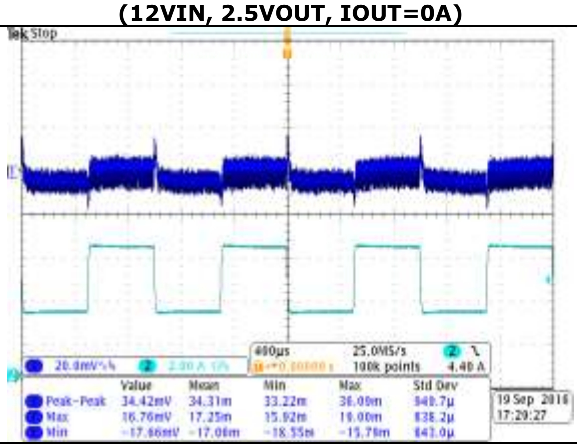


FIG.25 TRANSIENT RESPONSE
(12VIN, 2.5VOUT, 50% to 100% LOAD STEP)

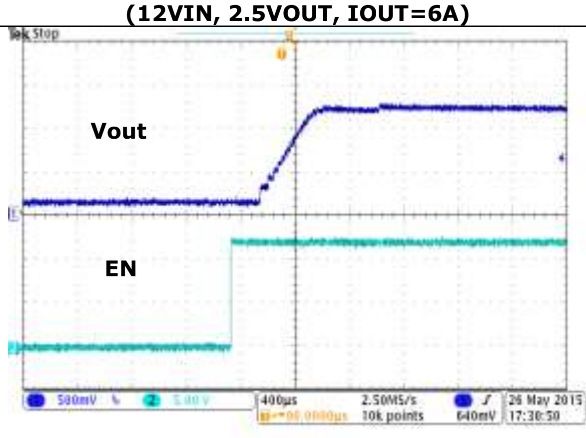


FIG.26 TURN-ON
(12VIN, 2.5VOUT, IOUT=6A)

TYPICAL PERFORMANCE CHARACTERISTICS: (3.3VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/50V/1206x2、100nF/25V/0805x1, Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 3.3Vout.

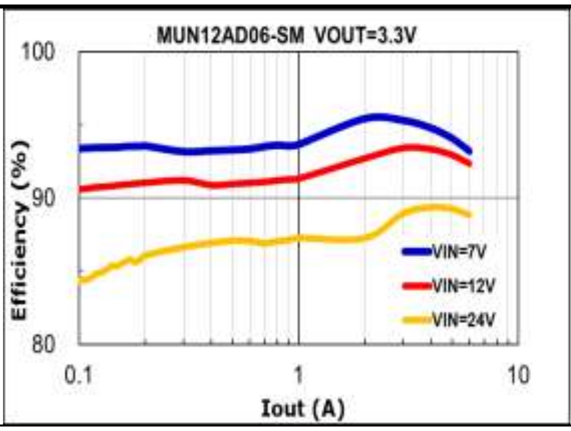


FIG.27 EFFICIENCY V.S. LOAD CURRENT

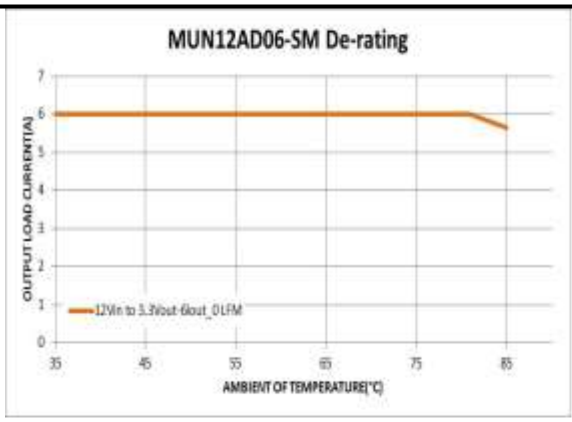


FIG.28 12VIN DE-RATING CURVE

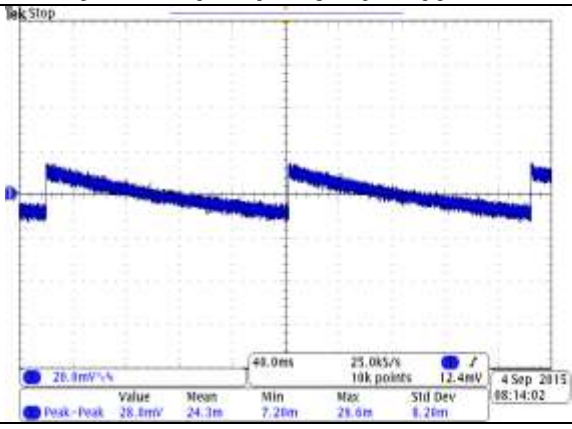


FIG.29 OUTPUT RIPPLE (12VIN, 3.3VOUT, IOUT=0A)

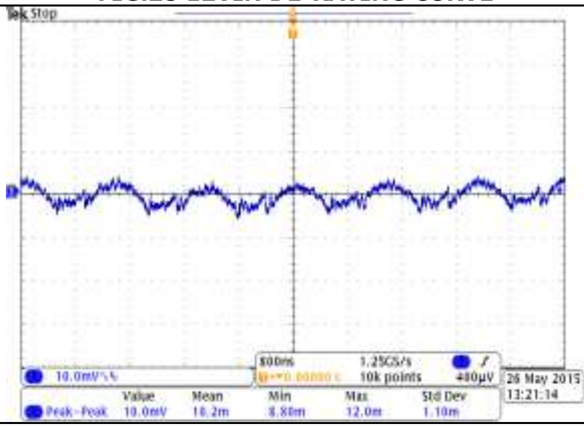


FIG.30 OUTPUT RIPPLE (12VIN, 3.3VOUT, IOUT=6A)

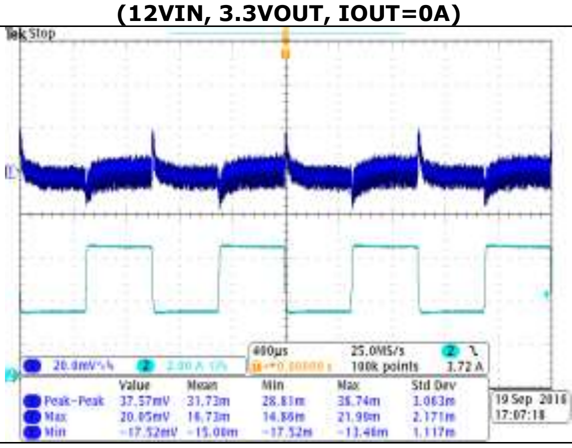


FIG.31 TRANSIENT RESPONSE (12VIN, 3.3VOUT, 50% to 100% LOAD STEP)

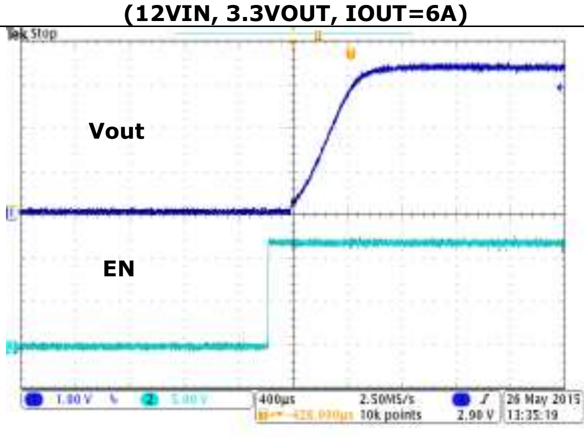


FIG.32 TURN-ON (12VIN, 3.3VOUT, IOUT=6A)

TYPICAL PERFORMANCE CHARACTERISTICS: (5.0VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz . The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.
Cin = 4.7uF/50V/1206x2、100nF/25V/0805x1 ,Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 5.0Vout.

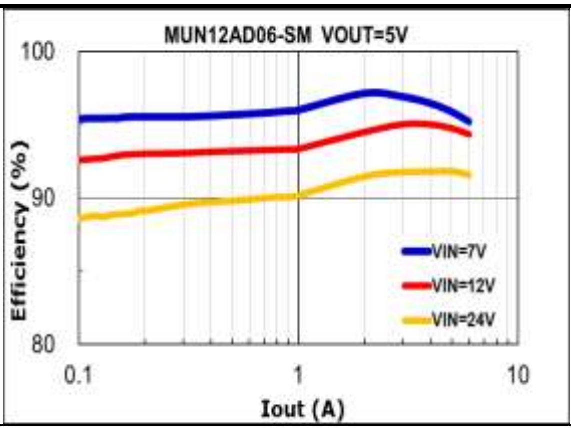


FIG.33 EFFICIENCY V.S. LOAD CURRENT

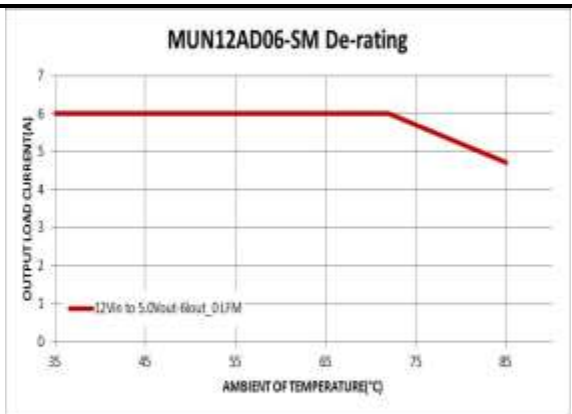


FIG.34 12VIN DE-RATING CURVE

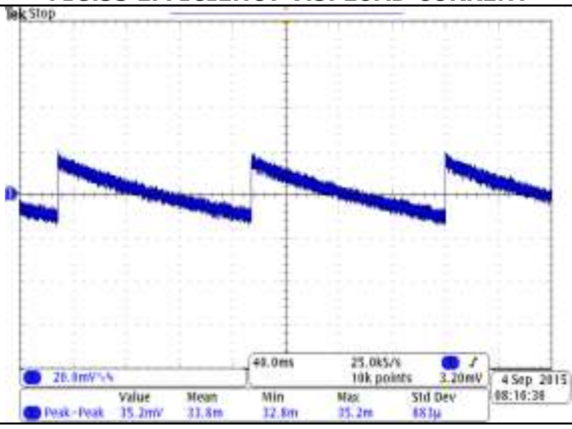


FIG.35 OUTPUT RIPPLE (12VIN, 5.0VOUT, IOUT=0A)

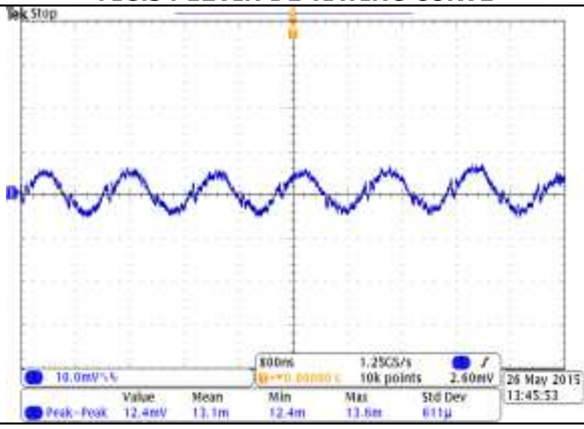


FIG.36 OUTPUT RIPPLE (12VIN, 5.0VOUT, IOUT=6A)

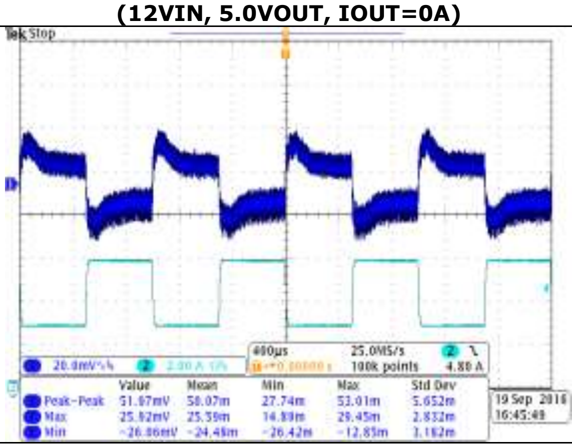


FIG.37 TRANSIENT RESPONSE (12VIN, 5.0VOUT, 50% to 100% LOAD STEP)

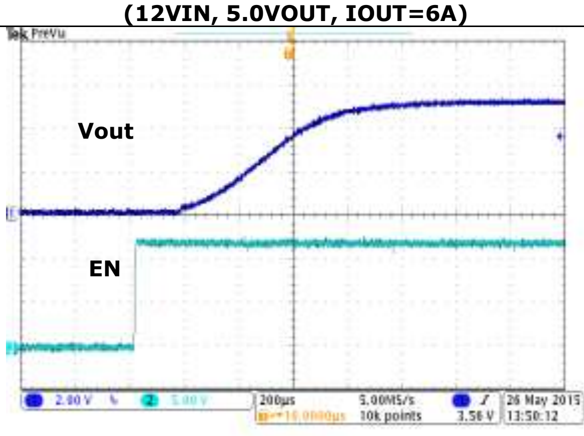


FIG.38 TURN-ON (12VIN, 5.0VOUT, IOUT=6A)

TYPICAL PERFORMANCE CHARACTERISTICS: (5.0VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.
Cin = 4.7uF/50V/1206x2、100nF/25V/0805x1 ,Cout = 47uF/6.3V/1206x1、100uF/6.3V/1206x1、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 5.0Vout.

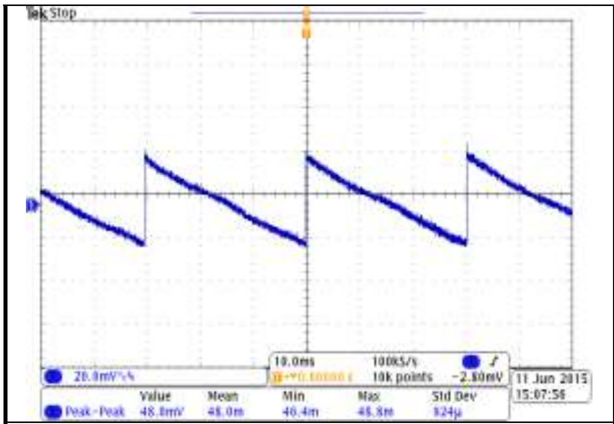


FIG.39 OUTPUT RIPPLE (19VIN, 5.0VOUT, IOUT=0A)

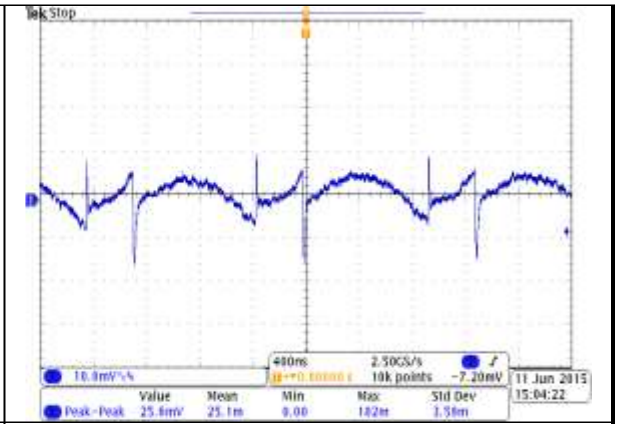


FIG.40 OUTPUT RIPPLE (19VIN, 5.0VOUT, IOUT=6A)

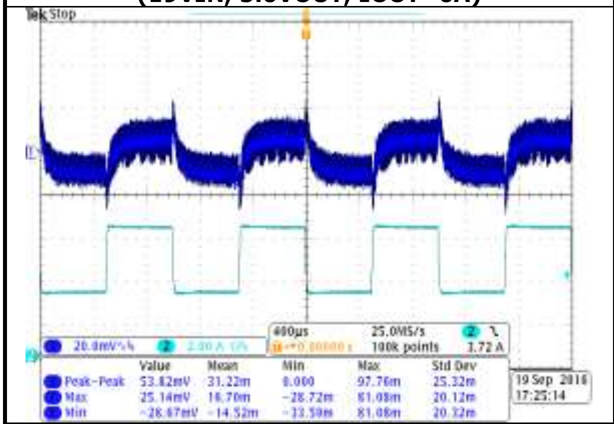


FIG.41 TRANSIENT RESPONSE (19VIN, 5.0VOUT, 50% to 100% LOAD STEP)

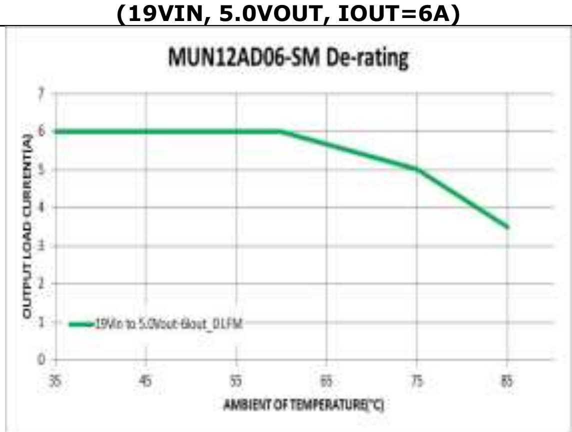


FIG.42 19VIN DE-RATING CURVE

APPLICATIONS INFORMATION:

REFERENCE CIRCUIT FOR GENERAL APPLICATION:

Figure 43 shows the module application schematics for input voltage +12V and turn on by input voltage directly through enable resistor (REN).

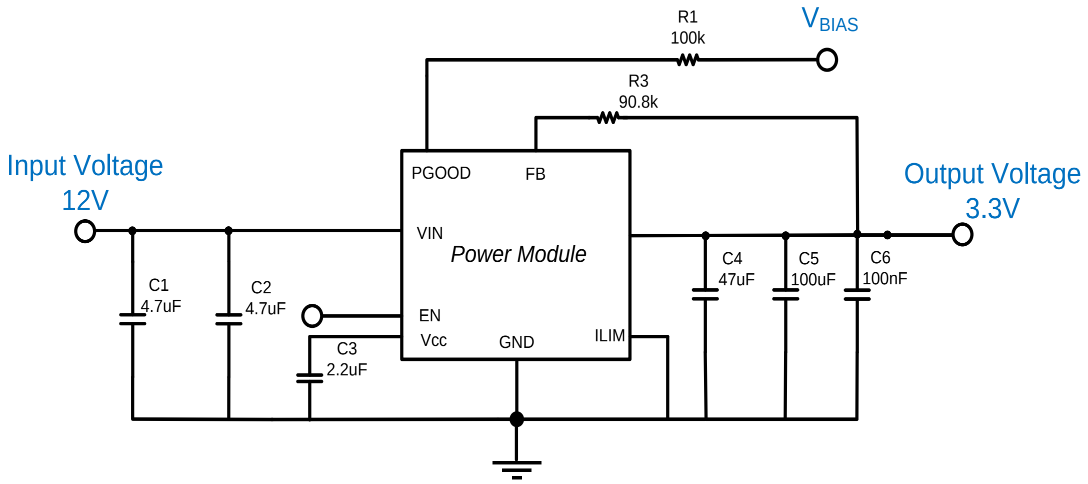


FIG.43 REFERENCE CIRCUIT FOR GENERAL APPLICATION

APPLICATIONS INFORMATION: (Cont.)

INPUT FILTERING:

The module should be connected to a source supply of low AC impedance and high inductance in which line inductance can affect the module stability. An input capacitor must be placed as near as possible to the input pin of the module so to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response as the step load changes, an additional capacitor at the output must be connected. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

LOAD TRANSIENT CONSIDERATIONS:

The MUN12AD06-SM module adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding C network CFF parallel with R_{FB} may further speed up the load transient responses.

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V±1.1% reference voltage. The output voltage can be programmed by the dividing resistor (R_{FB}) which connects to both Vout pin and FB pin. The output voltage can be calculated by Equation 1, resistor choice may be referred TABLE 1.

$$Vout\,(V) = 0.6 \times \left(1 + \frac{R_{FB}}{20K}\right) \qquad \text{(EQ.1)}$$

Vout (V)	R_{FB}(kΩ)
1.0	13.3(0.1%)
1.2	20.0(0.1%)
1.8	40.2(0.1%)
2.5	63.3(0.1%)
3.3	90.8(0.1%)
5.0	147(0.1%)

TABLE 1 Resistor values for common output voltages

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 44 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

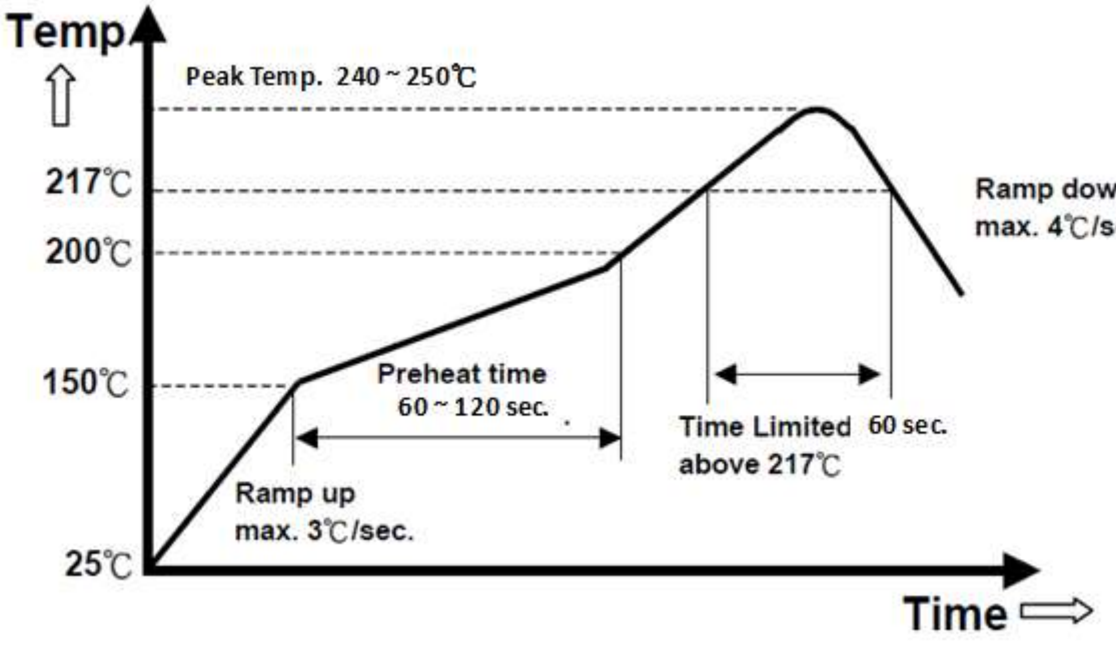


FIG.44 Recommendation Reflow Profile

APPLICATIONS INFORMATION: (Cont.)

Recommendation Layout Guide:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 45-48.

1. The ground connection between pin 23, pin25 and pin 5 to 7 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias
2. Place high frequency ceramic capacitors between pin 1, pin 19 to 21 (VIN), and pin 23, pin25, pin 5 to 7 (GND) for input side; and pin 24, pin 10 to 14 (VOUT), and pin 23, pin25, pin 5 to 7 (GND) for output side, as close to module as possible to minimize high frequency noise.
3. Keep the R_3 connection trace to the module pin 16 (FB) short.
4. Use large copper area for power path (VIN, VOUT, and GND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.
5. Avoid any sensitive signal traces near the pin 24, and pin 2 to 4 (PHASE).
6. The input decoupling capacitor must be close to module VIN pad and GND pad shown as figure 48. The C6 decoupling capacitor use to 100nF

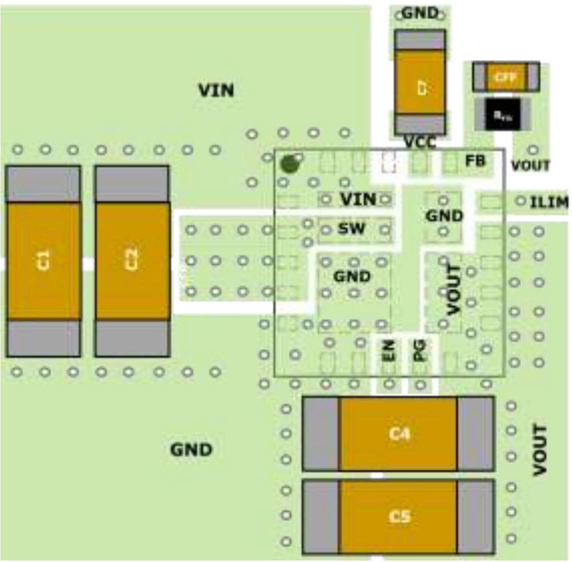


FIG.45 Recommendation Layout (Top)

APPLICATIONS INFORMATION: (Cont.)

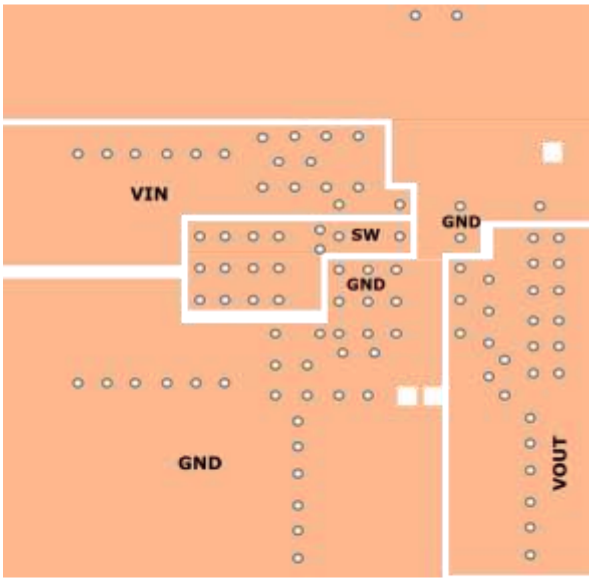


FIG.46 Recommendation Layout (Middle 1)

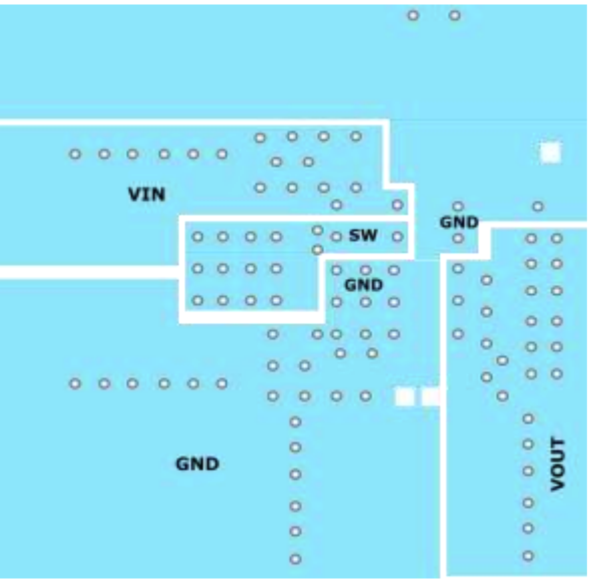


FIG.47 Recommendation Layout (Middle 2)

APPLICATIONS INFORMATION: (Cont.)

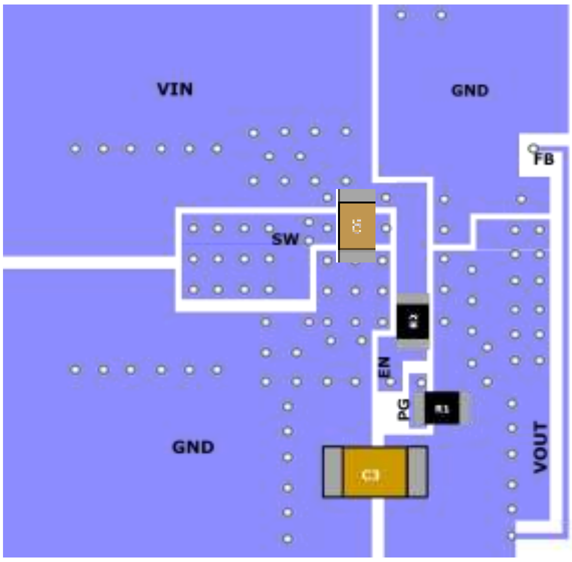
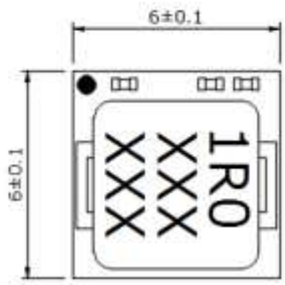


FIG.48 Recommendation Layout (Bottom)

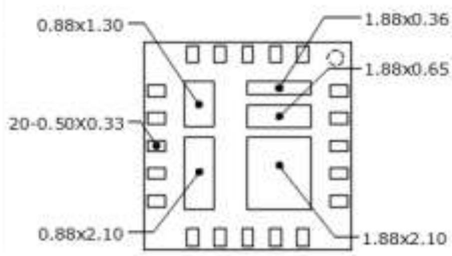
PACKAGE OUTLINE DRAWING:

Unit: mm

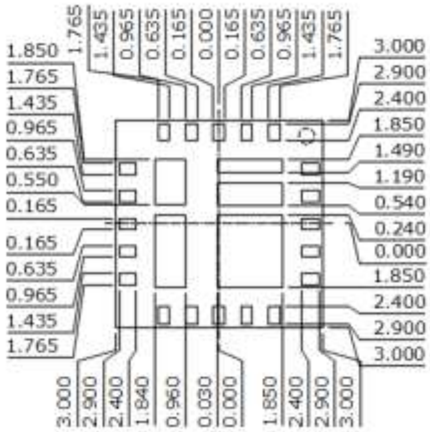
General Tolerance: +/- 0.1mm



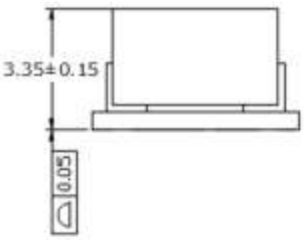
TOP VIEW



BOTTOM VIEW



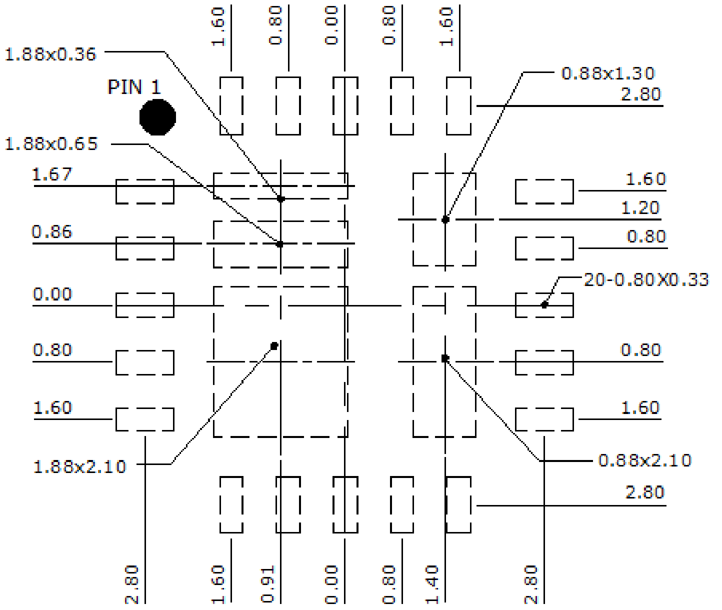
BOTTOM VIEW



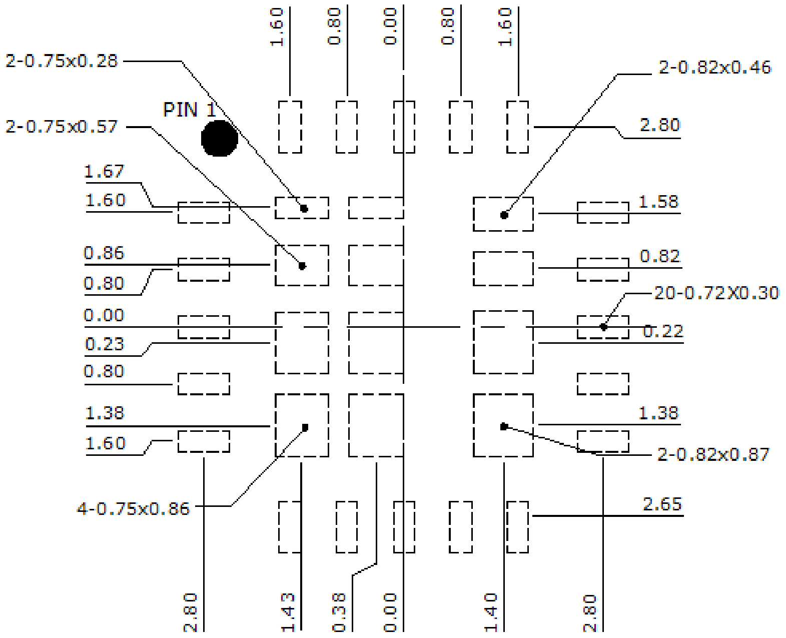
END VIEW

LAND PATTERN REFERENCE:

Unit: mm



RECOMMENDED LAND PATTERN

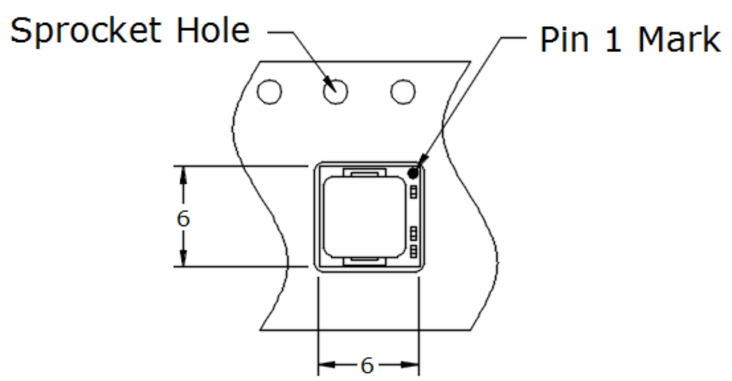


RECOMMENDED STENCIL PATTERN
BASED ON 0.1mm THICKNESS STENCIL

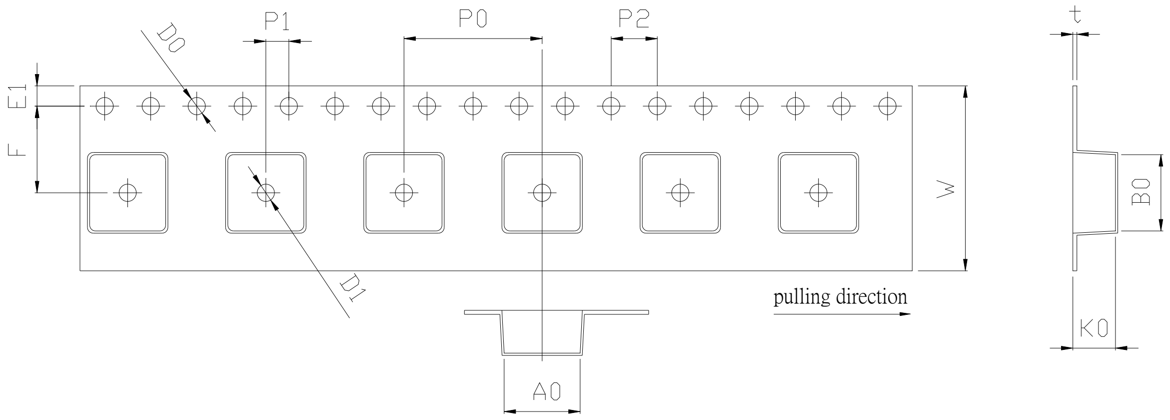
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension

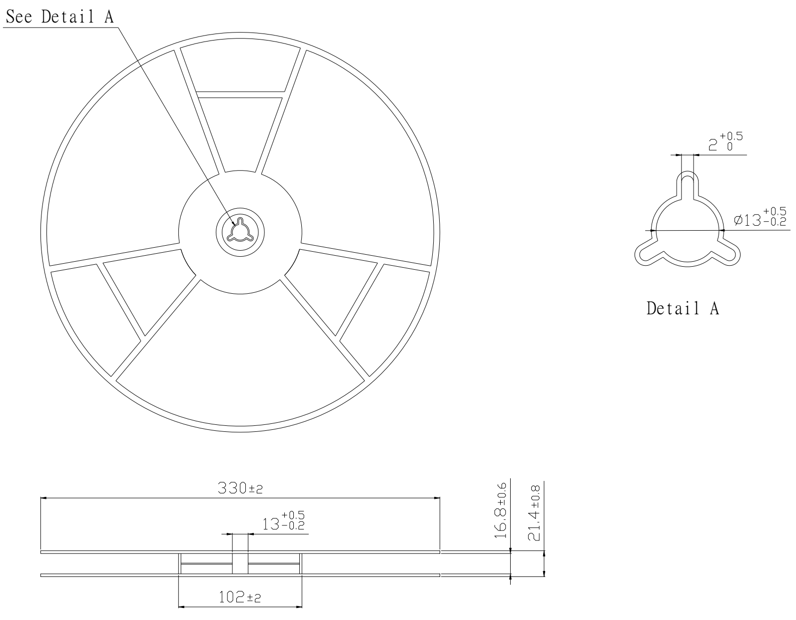


A0	6.60 ± 0.10	E1	1.75 ± 0.10
B0	6.60 ± 0.10	K0	3.70 ± 0.10
F	7.50 ± 0.10	P0	12.00 ± 0.10
W	16.00 ± 0.30	P1	2.00 ± 0.10
D0	φ1.5 +0.1/-0.0	P2	4.00 ± 0.10
D1	φ1.5 Min.	t	0.35 ± 0.05

PACKING REFERENCE: (Cont.)

Unit: mm

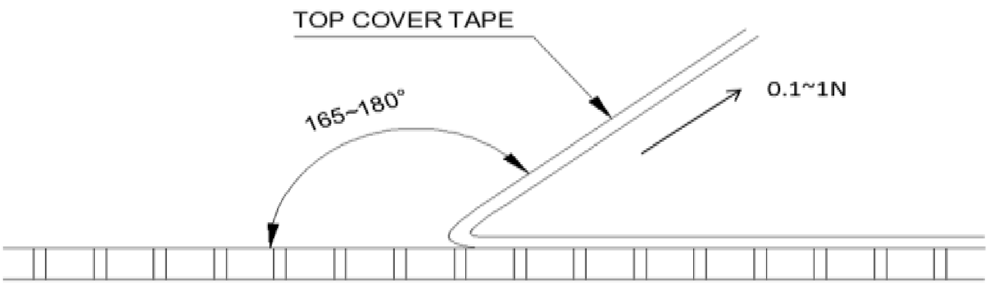
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1N to 1.3N



REVERSION HISTORY:

Date	Revision	Changes
2015.06.16	Preliminary	Release the preliminary specification.
2015.08.04	00	Official released.
2015.08.28	01	Change RFB resistor Upgrade Vout Voltage to 15V
2015.10.15	02	Add 12V,15V Wave Upgrade Recommendation Layout Guide Upgrade Input supply bias current
2016.01.18	03	Upgrade TYPICAL PERFORMANCE CHARACTERISTICS: Vout 12V (page 13)
2016.01.22	04	Upgrade Line & Load regulation and OCP Note
2016.06.28	05	Upgrade Adjusted Output Voltage use Condition Note Change LDS to uPOL Upgrade Land Pattern Add LOAD TRANSIENT CONSIDERATIONS
2016.09.20	06	Upgrade MSL Level and Over current limit Upgrade TRANSIENT RESPONSE Wave
2017.03.30	07	Add PGOOD sink current spec
2018.02.21	08	Upgrade EN Low threshold Voltage 0.8V → 0.4V
2019.01.21	09	Upgrade Vout Voltage down to 6V Upgrade Vin Voltage 7V down to 4.5V Add Duty max specification