OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-160128FC-2B**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	**Bazile Peter**	**Luo Luo**
Date: 15 Oct 10	Date: 15 Oct 10	Date: 15 Oct 10

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	22 Nov 06			First Issue	
B	26 Dec 10	4 5 7 8 18 6 11 17 19 29 4		1. Overall dimensions 2. Weight 3. Driver Supply Voltage 4. Operating current for VDDH 5. Optics Characteristics 6. Mechanical Drawing 7. Block Diagram 8. Add RGB interface 9. Power up sequence 10. Low Temperature Operation 11. Operating temperature	
C	07 Dec 11	30 to 33	9 10	Handling Precautions Support Acceories	
D	28 Nov 12	33	10	Errors on 10.1 DUO KIT	
E	24 Oct 14	6 7 11 16 19 20	2 3.2 3.4 3.5 5.2 5.4	Revised Drawing (sticky tape removed between glass and FPC) Electrical characteristic Block Diagram Serial Interface Power sequence Application Example	

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1 MAIN FEATURES

ITEM	CONTENTS
Display Format	160 (RGB) x 128 Dots
Overall Dimensions	Glass 39.9 x 34.0 x 1.6 mm
Colour	262,144 Colour
Active Area	33.575 x 26.864 mm
Viewing Area	35.575 x 28.864 mm
Display Mode	Passive Matrix (1.69”)
Driving Method	1/128 duty
Driver IC	SEPS525
Operating temperature	-40 ~ +70
Storage temperature	-40 ~ +80

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2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	160 (RGB) x 128	Dots
Overall Dimensions	Glass 39.9 x 34.0 x 1.6	mm
Viewing Area	35.575 x 28.864	mm
Active Area	33.575 x 26.864	mm
Dot Size	0.045 x RGB x 0.194	mm
Dot Pitch	0.07 x RGB x 0.21	mm
Weight	4.55	g
IC Controller/Driver	SEPS525F0A (COF)	

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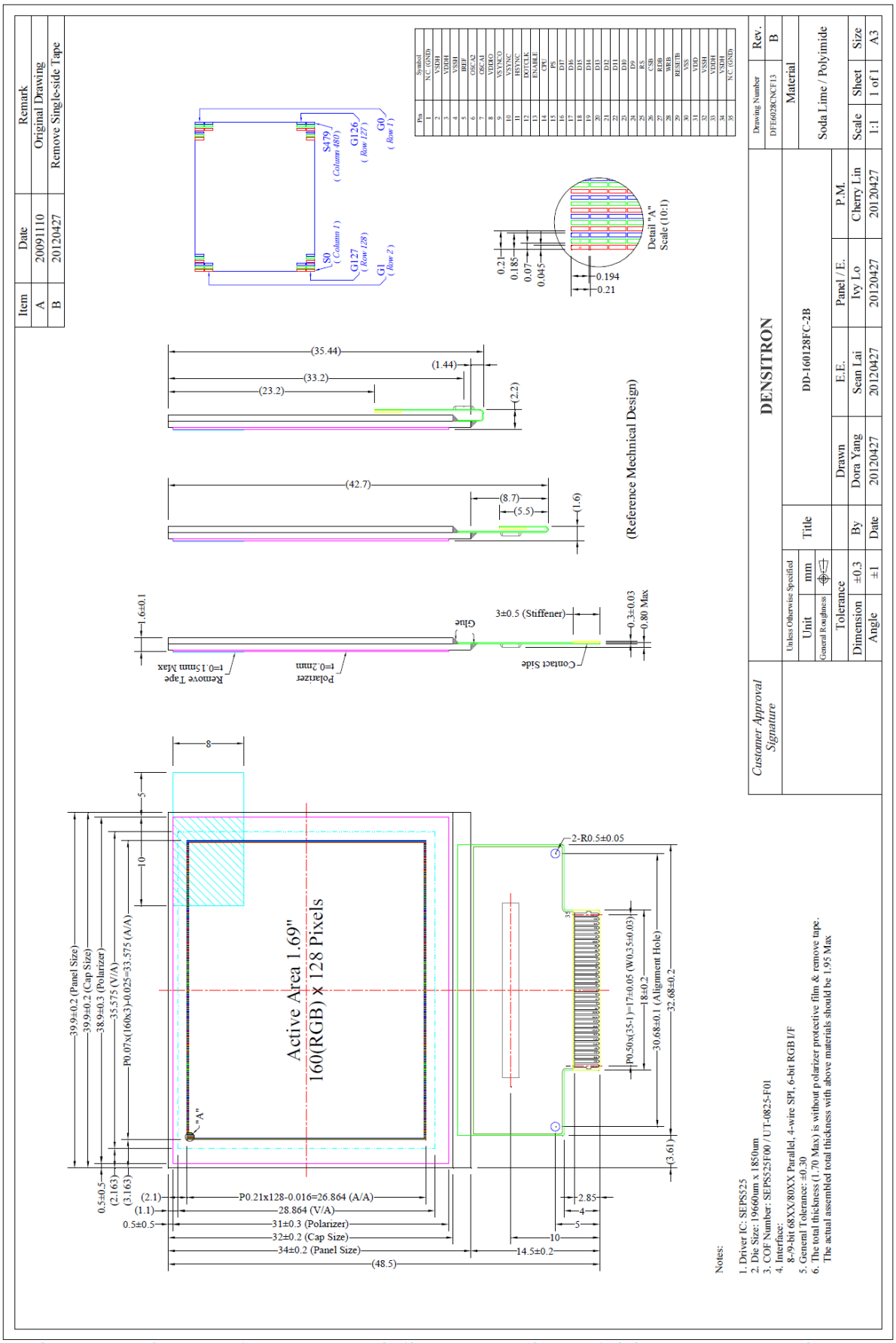
2.2 MECHANICAL DRAWING



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3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	-0.3	4	V	Note 1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	4	V	
Driver Supply Voltage	V_{DDH}	-0.3	16	V	
Operating Temperature	Top	-40	70	°C	
Storage Temperature	Tst	-40	85	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "VSS=0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

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3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.6	2.8	3.3	V
Supply Voltage x I/O pins	V_{DDIO}		1.6	2.8	3.3	V
Driver Supply Voltage	V_{DDH}	Note 1	13.5	14	14.5	V
High Level Input	V_{IH}		0.8xV_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH}	I_{OH} = -0.4mA	V_{DD}-0.4	-	-	V
Low Level Output	V_{OL}	I_{OL} = -0.1mA	-	-	0.4	V
Operating current for VDD	I_{DD}		-	2.5	3.5	mA
Operating current for VDDH	I_{DDH}	Note 2		10.5	13.2	mA
		Note 3	-	14.9	18.6	
		Note 4	-	26.2	32.8	
Sleep Mode Current for VDD	$I_{DD, Sleep}$			3	5	uA
Sleep Mode Current for VDDH	$I_{DDH, Sleep}$			1	5	uA

Note 1 Brightness (Lbr) and Supply Voltage for Display (VDDH) are subject to the change of the panel characteristics and the customer's request.
Note 2 VDD = 2.8V, VDDH = 14V, 30% Display Area Turn On
Note 3 VDD =2.8V, VDDH = 14V, 50% Display Area Turn On
Note 4 VDD = 2.8V, VDDH = 14V, 100% Display Area Turn On

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3.3 INTERFACE PIN ASSIGNMENT

Mating Connector type: 35-pin, 0.5 mm pitch FFC/FPC. Type: AVX 04-6238-035-000-800

No.	Symbol	Function
1	N.C.	Reserved Pin (Supporting Pin). The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground
2	VSDH	Ground of OEL Panel These are the ground pins for analog circuits. It must be connected to external ground. VSDH: Data Driver Ground
3	VDDH	Power supply of OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.
4	VSSH	Ground of OEL Panel These are the ground pins for analog circuits. It must be connected to external ground. VSSH: Scan Driver Ground
5	IREF	Current reference for brightness Adjustment This pin is segment (data) current reference pin. A 68KΩ Resistor should be connected between this pin and VSS
6	OSCA2	Fine Adjustment for Oscillation The frequency is controlled by external 5.1 kΩ Resistor between OSCA1 and OSCA2. The oscillator signal is used for system clock generation. When the external clock mode is selected, OSCA1 is used external clock input.
7	OSCA1	
8	VDDIO	Power supply for Interface logic level This is a voltage supply pin. It should be match with MCU interface voltage level. It must always be equal or lower than VDD
9	VSYNCO	RGB Mode functional Pins VSYNCO : Vertical Sync Output VSYNC: Vertical Sync Input HSYNC : Horizontal Sync Input DOTCLK : Dot Clock Input ENNABLE : Video Enable Input *While using MCU interface, it must be connected to VDD.*
10	VSYNC	
11	HSYNC	
12	DOTCLK	
13	ENABLE	
14	CPU	Select CPU type Low: 80-Series High: 68-Series
15	PS	*Select Parallel/Serial Interface* Low: Serial High: Parallel
16	D17	*Host Data Input/Output Bus.* These pins are 9-bit bi-directional data bus to be connected with MCU data bus. PS = 1: 8-bit Bus: D17 to D10; 9-bit Bus: D17 to D9
17	D16	
18	D15	
19	D14	
20	D13	
21	D12	
22	D11	

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23	D10	0	D[17] SCL: Synchronous Clock Input D[16] SDI: Serial Data Input D[15] SDO: Serial Data Output		
24	D9				
25	RS	*Selects Data/Command* Low: Command High: Parameter/data			
26	CSB	*Chip Select* Low: SEPS525 is selected and can be accessed High: SEPS525 is not selected and cannot be accessed			
27	RDB	Read or Read/Write enable 80-system bus interface: read strobe signal (active low) 68-system bus interface: bus enable strobe (active high) When serial mode, fix it to VDD or VSS level			
28	WRB	Write or Read/Write select 80-system bus interface: write strobe signal (active low) 68-system bus interface: read/write select Low: write, High: read When serial mode, fix it to VDD or VSS level			
29	RESETB	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed.			
30	VSS	Ground of Logic Circuit A reference for the logic pins. It must be connected to external ground			
31	VDD	Power supply for logic circuit This is a voltage supply pin. It must be connected to external source			
32	VSSH	Ground of OEL Panel These are the ground pins for analog circuits. It must be connected to external ground. VSSH: Scan Driver Ground			
33	VDDH	Power supply of OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.			
34	VSDH	Ground of OEL Panel These are the ground pins for analog circuits. It must be connected to external ground. VSDH: Data Driver Ground			
35	NC	Reserved Pin (Supporting Pin). The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground			

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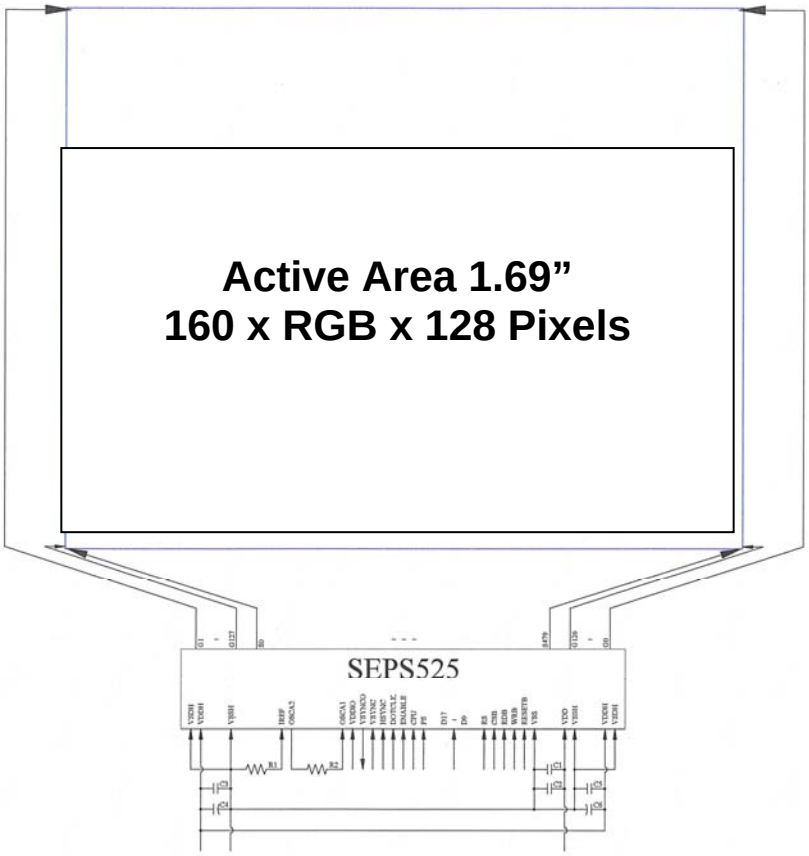
3.4 BLOCK DIAGRAM



MCU Interface Selection: CPU, PS
Pins connected to MCU interface: D17~D9, RS, CSB, RDB, WRB, and RESETB
Pins connected to RGB interface: D17~D12, VSYNC, HSYNC, DOTCLK, and ENABLE

C1, C3, C5	0.1µF	C4, C6	4.7µF/25V Tantalum Capacitor
C2	4.7µF	R2	5.1kΩ
R1:	68kΩ		

EIM=1(default)

Interface mode	PS	CPU	DFM1	DFM0	D17	D16	D15	D14	D13	D12	D11	D10	D9	RS	CSB	RDB	WRB	RESETB
4-wire SPI	0	X	X	X	SCL	SDI	**NC**	**0**	**0**	**0**	**0**	**0**	**0**	RS	CSB	**0**	**0**	RESETB
80xx parallel 9 bit	1	0	1	0	D8	D7	D6	D5	D4	D3	D2	D1	D0	RS	CSB	RDB	WRB	RESETB
80xx parallel 8 bit	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	**0**	RS	CSB	RDB	WRB	RESETB
68xx parallel 9 bit	1	1	1	0	D8	D7	D6	D5	D4	D3	D2	D1	D0	RS	CSB	E	R/W	RESETB
68xx parallel 8 bit	1	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0	**0**	RS	CSB	E	R/W	RESETB

EIM=0

Interface mode	RIM1	RIM0	D17	D16	D15	D14	D13	D12	D11	D10	D9	VSYNC	HSYNC	DOTCLK	ENABLE
6-bit RGB interface	1	0	D5	D4	D3	D2	D1	D0	**0**	**0**	**0**	VSYNC	HSYNC	DOTCLK	ENABLE

Note:
1. DFM1、DFM0 setting by Register 16h
2. EIM、RIM1、RIM0 setting by Register 14h
3. “X” : Don’t care, “NC” : Non-connection
   “1” : Connect to VDD or set to High level.
   “0” : Connect to GND or set to Low Level.

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3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

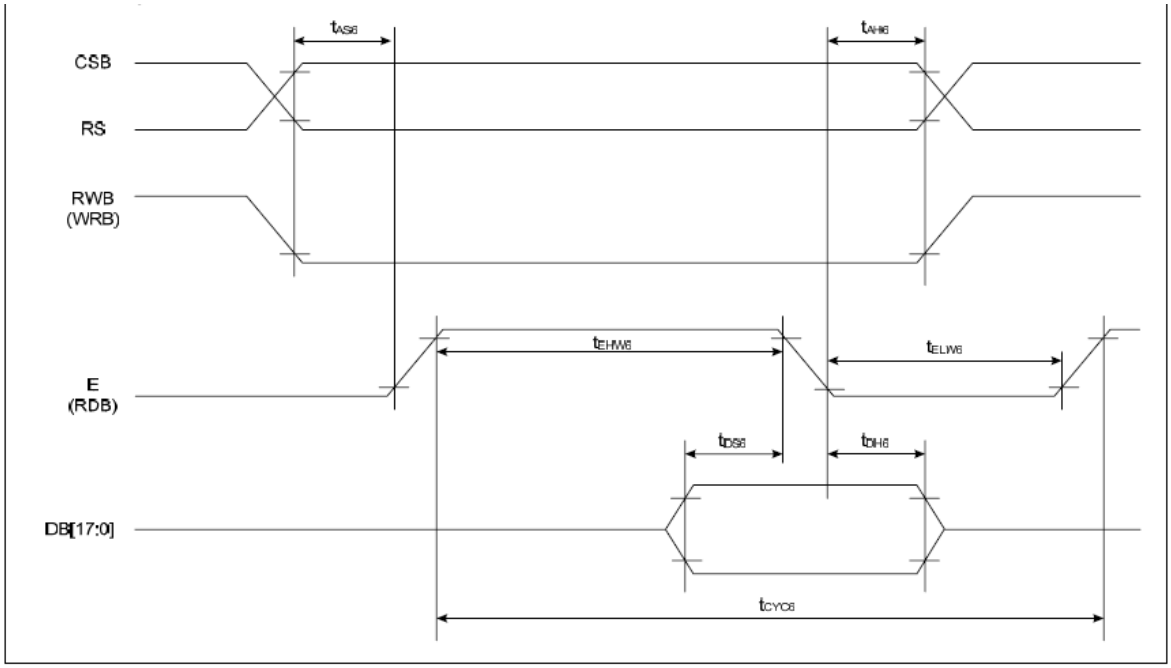
3.5.1.1 6800-Series MPU Parallel Interface Timing Characteristics

VDD = 2.8V, Ta = 25˚C

Characteristics	Symbol	Min	Max	Unit	Port
Write Timing					
Address hold timing	tAH6	5	-	nS	CSB
Address setup timing	tAS6	5			RS
System cycle timing Write	tCYC6	100	-	nS	E
"L" pulse width Write	tELW6	45			
"H" pulse width	tEHW6	45			
Data setup timing	tDS6	40	-	nS	DB[17:0]
Data hold timing	tDH6	10			
Read Timing					
Address hold timing	tAH6	10	-	nS	CSB
Address setup timing	tAS6	10			RS
System cycle timing Write	tCYC6	200	-	nS	E
"L" pulse width Write	tELW6	90			
"H" pulse width	tEHW6	90			
Data setup timing (CL= 15pF)	tDS6	0	70	nS	DB[17:0]
Data hold timing (CL= 15pF)	tDH6				

- ***All the timing should be based on 10% and 90% of V_{DD}.***

Write Timing



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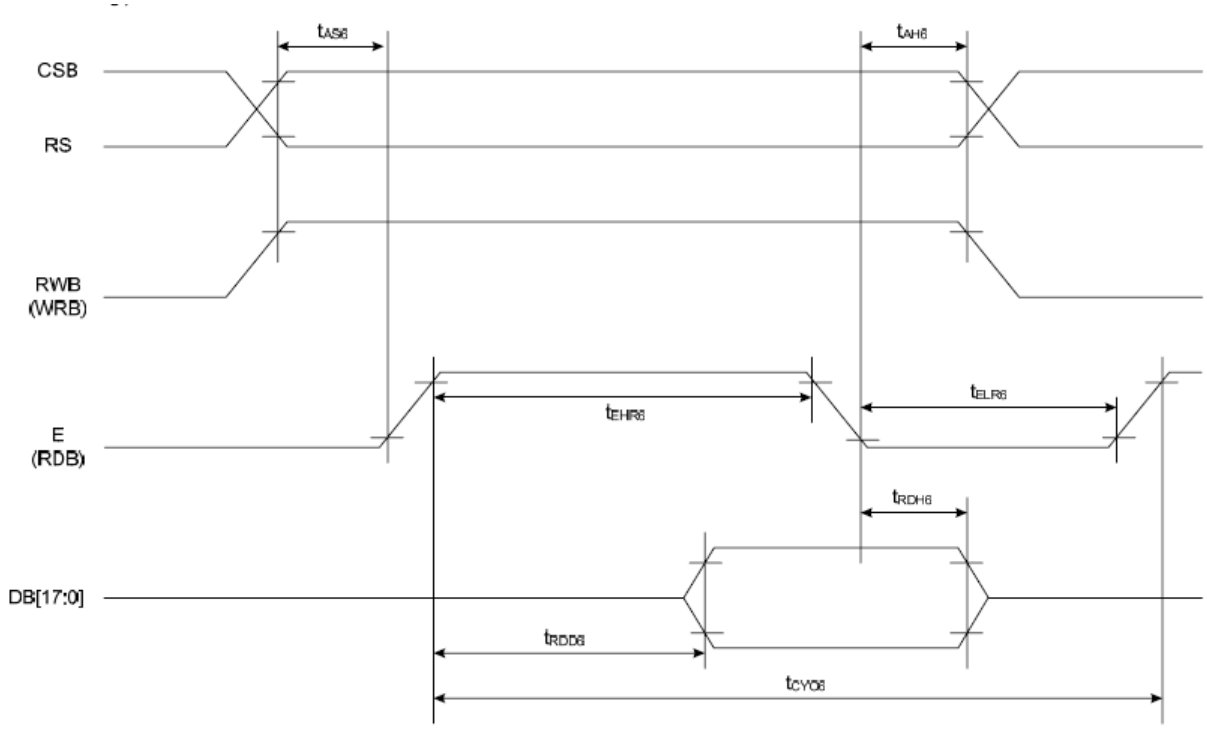
Read Timing



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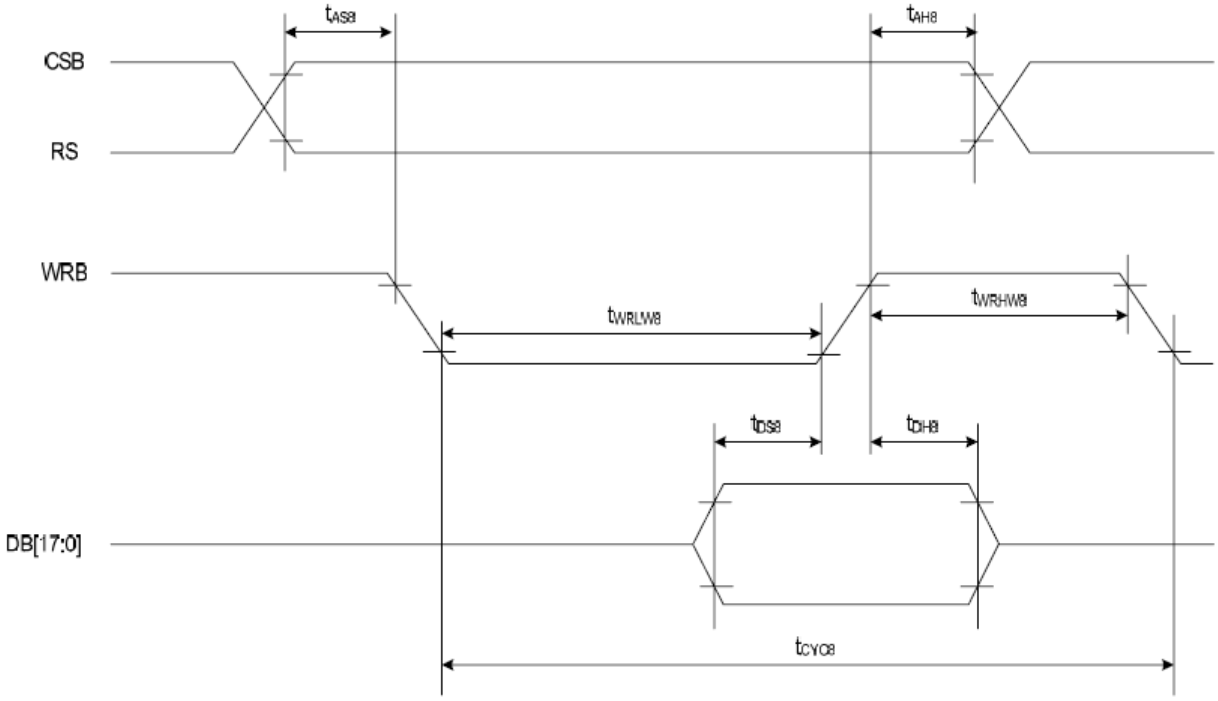
3.5.1.2 8080-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit	Port
Write Timing					
Address hold timing	tAH8	5	-	nS	CSB
Address setup timing	tAS8	5			RS
System cycle timing Write	tCYC8	100	-	nS	WRB
"L" pulse width Write	tELW8	45			
"H" pulse width	tEHW8	45			
Data setup timing	tDS8	30	-	nS	DB[17:0]
Data hold timing	tDH8	10			
Read Timing					
Address hold timing	tAH8	10	-	nS	CSB
Address setup timing	tAS8	10			RS
System cycle timing Write	tCYC8	200	-	nS	RDB
"L" pulse width Write	tELW8	90			
"H" pulse width	tEHW8	90			
Data setup timing (CL= 15pF)	tDS8	0	60	nS	DB[17:0]
Data hold timing (CL= 15pF)	tDH8				

**** All the timing should be based on 10% and 90% of V_{DD}***

Write Timing



Read timing

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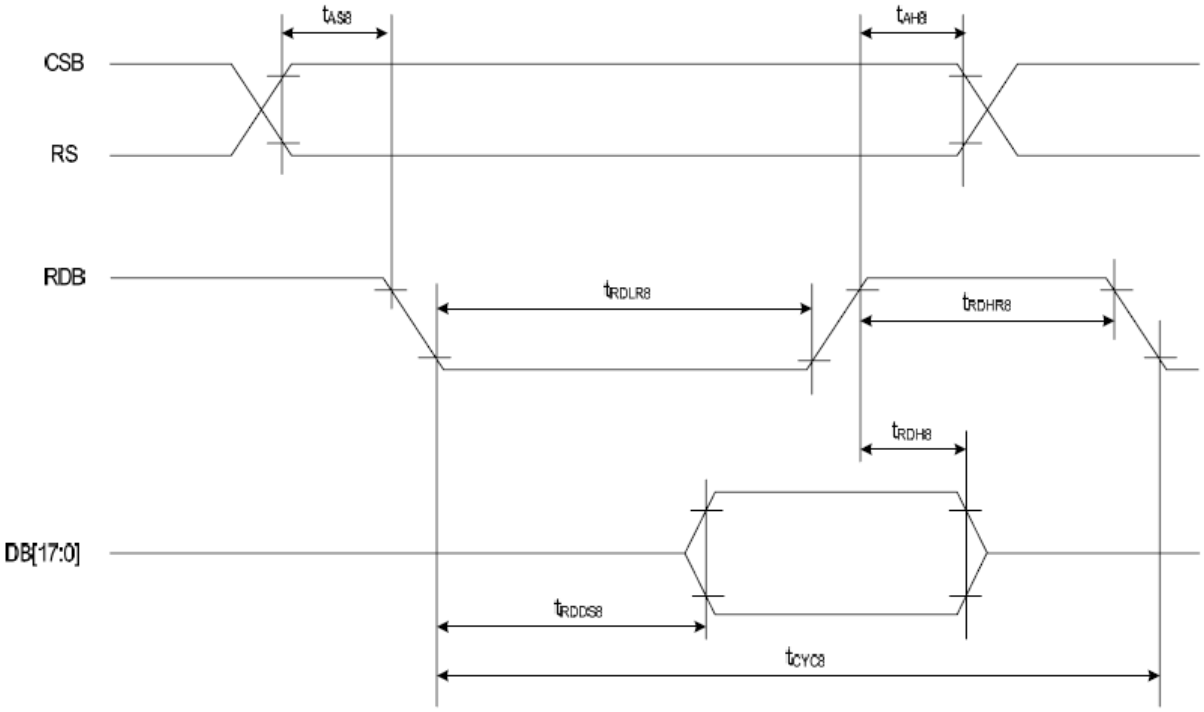

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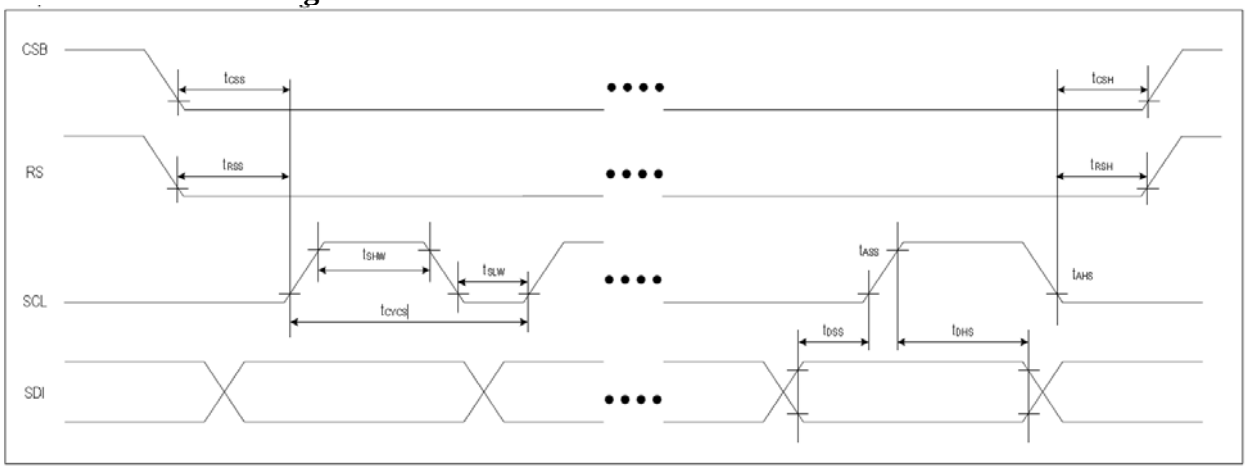
3.5.1.3 Serial Interface Timing Characteristics

VDD = 2.8V , Ta = 25˚C

ITEM	SYMBOL	MIN	MAX	UNIT	PORT
Serial clock cycle SCL	tCYCS	100	-	nS	SCL
"H" pulse width SCL	tSHW	45			
"L" pulse width	tSLW	45			
Data setup timing Data	tDSS	5	-	nS	SDI
Hold timing	tDHS	5			
CSB-SCL timing	tCSS	5	-	nS	CSB
CSB-hold timing	tCSH	5			
RSB-SCL timing	TRSS	5	-	nS	RS
RSB-hold timing	TRSH	5			

**** All the timing should be based on 10% and 90% of V_{DD}***

Serial Interface Timing



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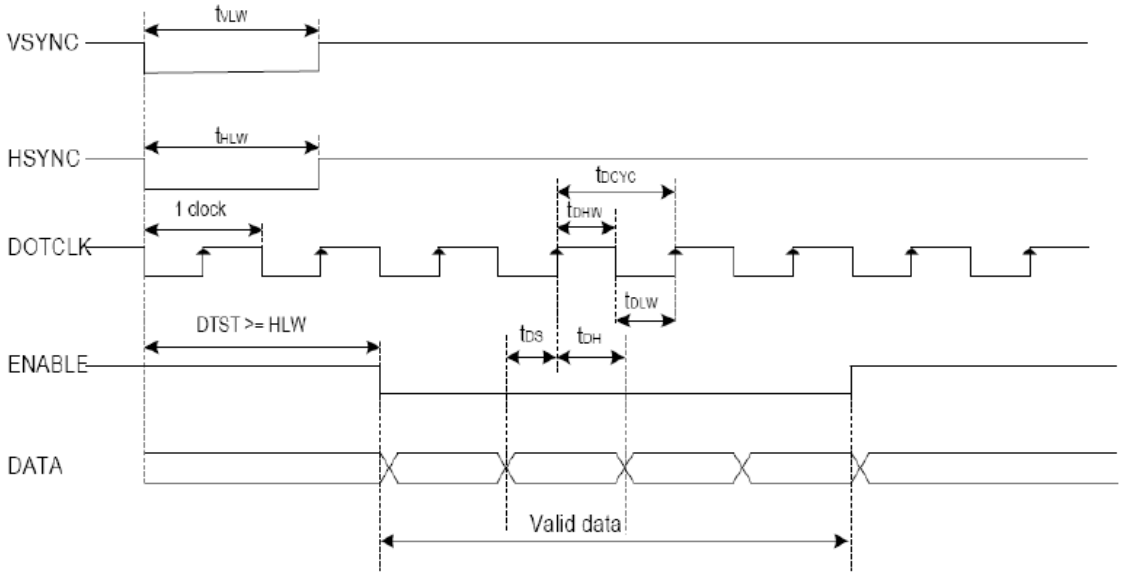
3.5.1.4 RGB Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Item	Min	Max	Unit	Port
t_{DCYC}	Dot Clock Cycle	100	-	ns	DOTCLK
t_{DLW}	Dot "L" Pulse Width	50	-	ns	
t_{DHW}	Dot "H" Pulse Width	50	-	ns	
t_{DS}	Data Setup Timing	5	-	ns	D[17:12]
t_{DH}	Data Hold Timing	5	-	ns	
t_{VLW}	Vsync Pulse Width	1	-	DOTCLK	VSYNC
t_{HLW}	Hsync Pulse Width	1	-	DOTCLK	HSYNC

* All the timing reference is 10% and 90% of V_{DD}.



DTST: Setup Time for Data Transmission

* VSYNC, HSYNC, ENABLE, and D[17:12] should be transmitted by 3 clocks for one pixel (RGB).

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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness(White)	L_{br}	Note 1	60	75	-	cd/m^2
C.I.E.(White)	(X)	C.I.E. 1931	0.26	0.30	0.34	-
	(Y)		0.29	0.33	0.37	
C.I.E.(Red)	(X)	C.I.E. 1931	0.60	0.64	0.68	-
	(Y)		0.30	0.34	0.38	
C.I.E.(Green)	(X)	C.I.E. 1931	0.27	0.31	0.35	-
	(Y)		0.58	0.62	0.66	
C.I.E.(Blue)	(X)	C.I.E. 1931	0.10	0.14	0.18	-
	(Y)		0.12	0.16	0.20	
Dark Room Contrast	CR		-	>10000:1	-	-
Viewing Angle			>160	-	-	degree

Note 1: Brightness (Lbr) and Supply Voltage for Display (VDDH) are subject to the change of the panel characteristics and the customer's request.
Optical measurement with polarizer is taken at VDD, VDDIO = 2.8V, VDDH = 14V and the software initial setting with section 5.4.1 Reference parameter table for normal operation mode.

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5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

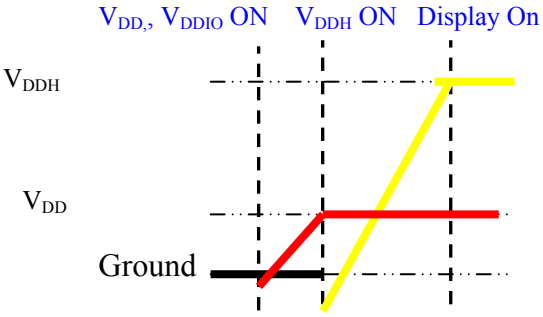
Please refer to the Technical Manual for the SEPS525

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

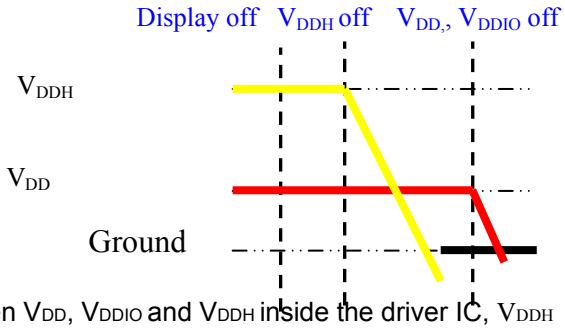
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD} & $V_{DD\ IO}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms (When V_{DD} & V_{DDIO} is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (When V_{DDH} reach 0 and panel is completely discharges)
4. Power down V_{DD} & V_{DDIO}



1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{DDH} inside the driver IC, V_{DDH} becomes lower than V_{DD} & V_{DDIO} whenever V_{DD} & V_{DDIO} is ON and V_{DDH} is OFF.
2) V_{DDH} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{DDH}) can never be pulled to ground under any circumstance.
4) V_{DD} & V_{DDIO} should not be power down before V_{DDH} power down.

5.3 RESET CIRCUIT

When RESETB input is low, the chip is initialized with the following status:

1. Frame frequency: 90Hz
2. OSC: internal OSC
3. Internal OSC: ON
4. DDRAM write horizontal address: MX1 = 00h, MX2 = 9Fh
5. DDRAM write vertical address: MY1 = 00h, MY2 = 7Fh
6. Display data RAM write: HC = 1, VC = 1, HV = 0
7. RGB data swap: OFF
8. Row scan shift direction: G0, G1, … , G126, G127
9. Column data shift direction: S0, S1, … , S478, S479
10. Display ON/OFF: OFF
11. Panel display size: FX1 = 00h, FX2 = 9Fh, FY1 = 00h, FY2 = 7Fh
12. Display data RAM read column/row address: FAC = 00h, FAR = 00h
13. Pre-charge time(R/G/B): 0 clock
14. Pre-charge current(R/G/B): 0 uA 15. Driving current(R/G/B): 0 uA

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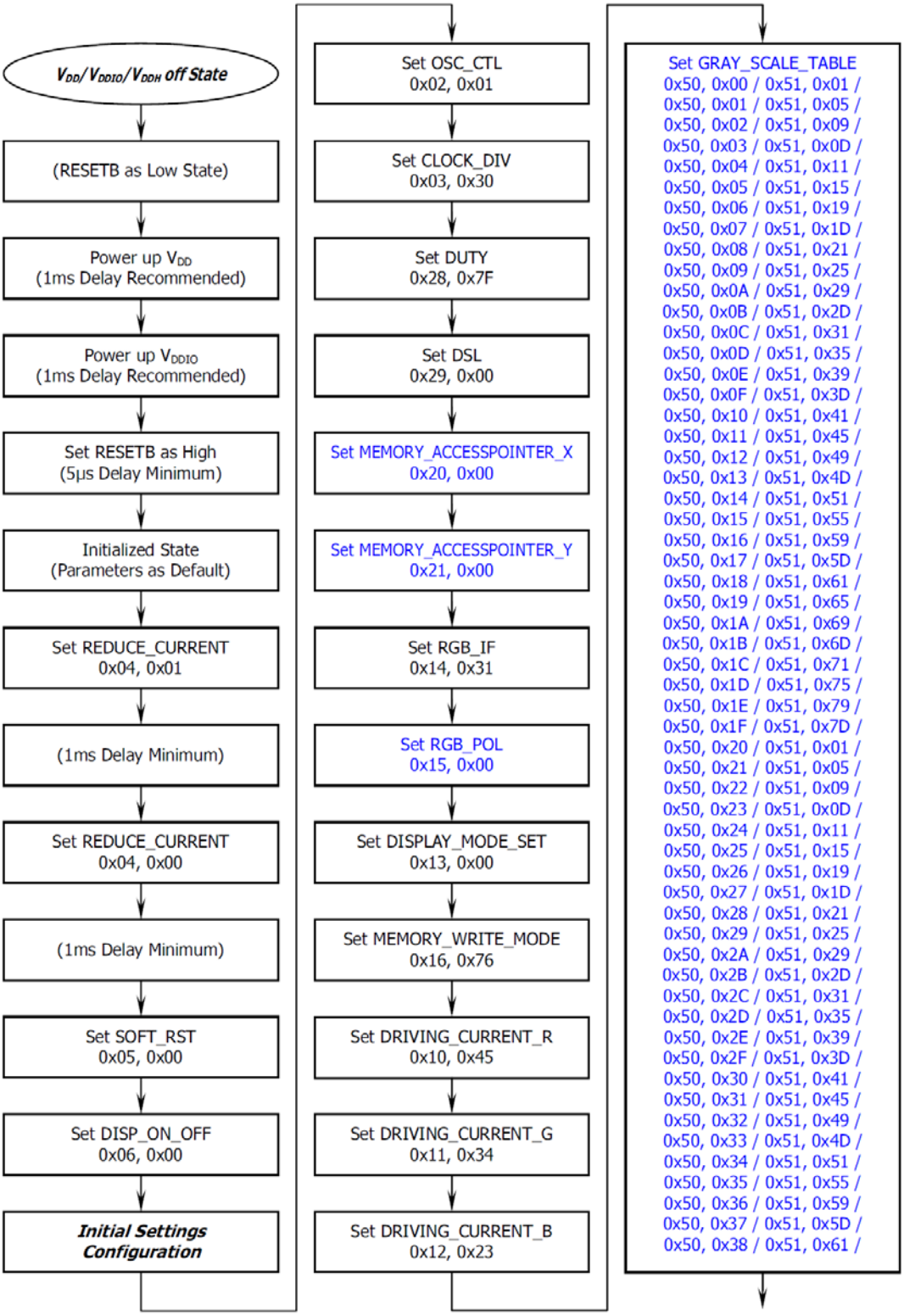
5.4 ACTUAL APPLICATION EXAMPLE

Power up Sequence



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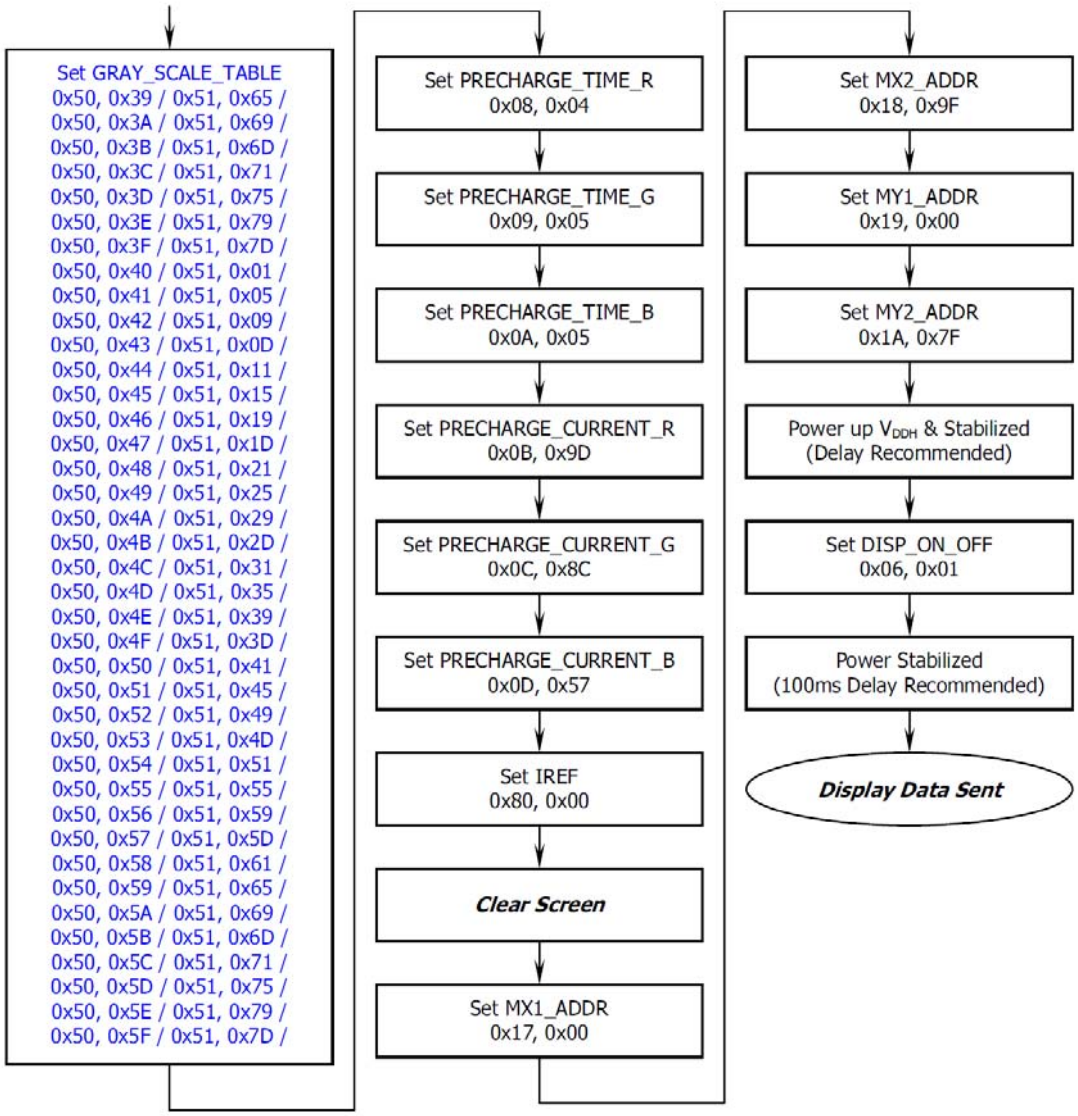
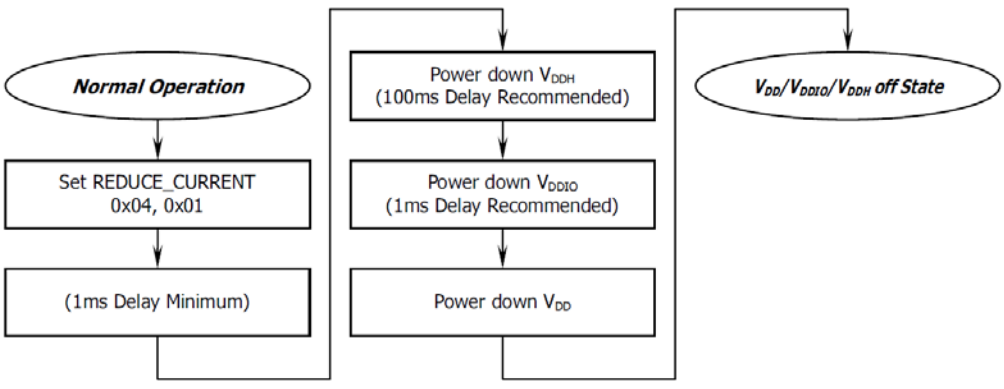


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function

Power down Sequence



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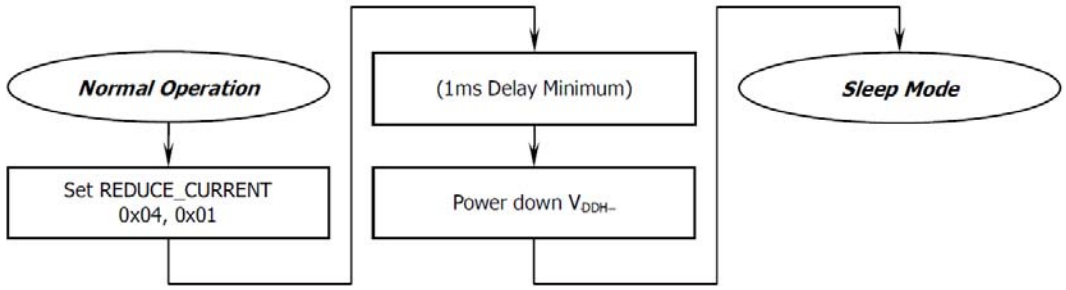
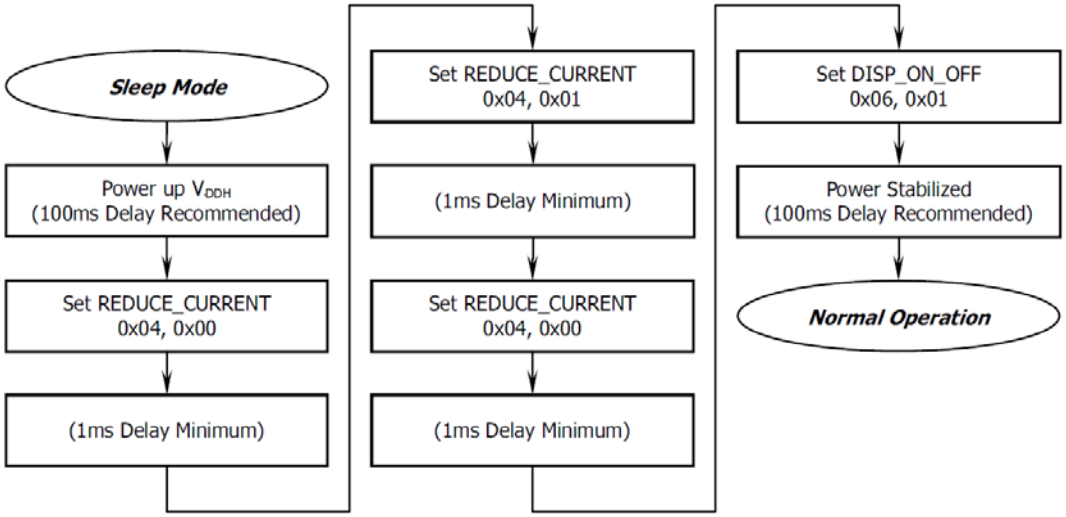
Entering Sleep mode



Exiting sleep mode



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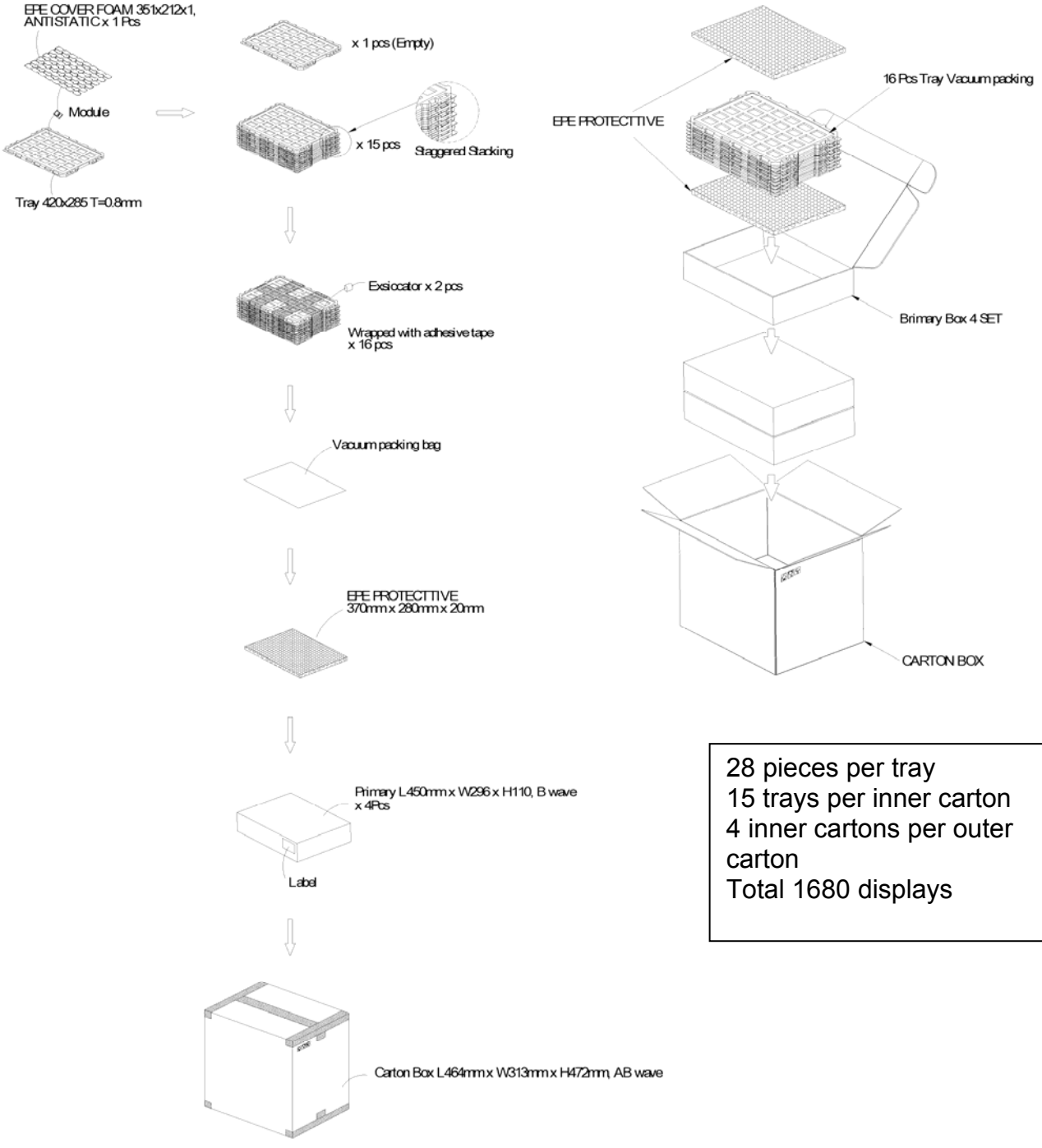
6 PACKAGING AND LABELLING SPECIFICATION

DENSITRON
DD-160128FC-2B
TW YY MM



28 pieces per tray
15 trays per inner carton
4 inner cartons per outer carton
Total 1680 displays

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7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

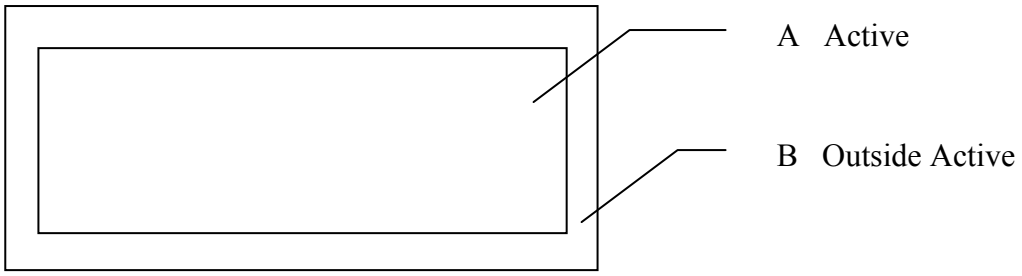
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

Test and measurement to be conducted under following conditions:

Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

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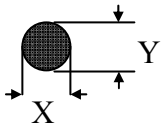
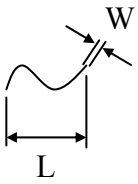
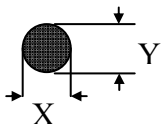
7.2.4 Standard of appearance inspection

Units: mm

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td rowspan="2">Packing & Label</td><td>Outside & inside package | Presence of product no., lot no., quantity</td></tr>
<tr><td>Critical</td><td>Product must not be mixed with others and quantity must not be different from that indicated on the label</td></tr>
<tr><td>Major</td><td>Dimension</td><td>Product dimensions must be according to specification and drawing</td></tr>
<tr><td>Major</td><td>Electrical</td><td>Product electrical characteristics must be according to specification</td></tr>
<tr><td>Critical</td><td>OLED Display</td><td>Missing lines, short circuits or wrong patterns on OLED display are not allowed</td></tr>
<tr><td>Minor</td><td>Black spot, white spot, dust</td><td>Round type: as per following drawing
∅ = (X+Y)/2
 

<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1<∅<0.2</td><td>3</td></tr><tr><td>0.2<∅<0.25</td><td>1</td></tr><tr><td>0.25<∅</td><td>0</td></tr></table>
Line type: as per following drawing
 

<table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>- -</td><td>W≤0.05</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>L≤2.0</td><td>W≤0.1</td><td>3</td></tr><tr><td>L>2.0</td><td></td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
<tr><td>Minor</td><td>Polariser scratch</td><td>Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>Minor</td><td>Polariser bubble</td><td>∅ = (X+Y)/2
 

<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.5</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>∅>0.5</td><td>0</td></tr></table></td></tr>
</table>

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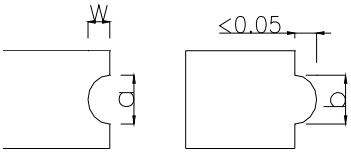
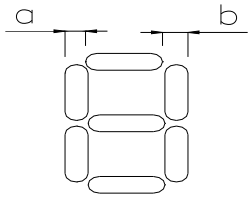
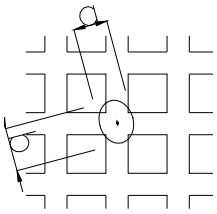
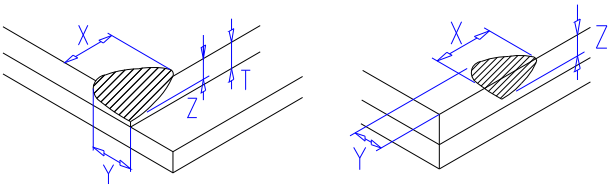
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Segment deformation</td><td>
1b. Pin hole on dot matrix display


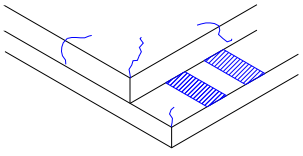
<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a,b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5<∅<1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

2. Segments / dots with different width


<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>

3. Alignment layer defect
∅ = (a+b)/2


<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>∅≤0.4</td><td>Any number</td></tr>
<tr><td>0.4<∅≤1.0</td><td>5</td></tr>
<tr><td>1.0<∅≤1.5</td><td>3</td></tr>
<tr><td>1.5<∅≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7
</td></tr>
<tr><td>Minor</td><td>Panel Chipping</td><td>
X ≤ 1/6 Panel length
Y ≤ 1
Z ≤ T


</td></tr>
<tr><td>Minor</td><td>Panel Cracking</td><td>
Cracks not allowed

</td></tr>
<tr><td>Minor</td><td>Cupper exposed (pin or film)</td><td>Not allowed if visible by eye inspection</td></tr>
<tr><td>Minor</td><td>Film or Trace Damage</td><td>Not allowed if affect electrical function</td></tr>
</table>

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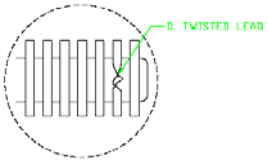
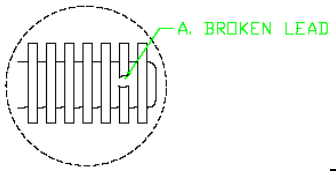
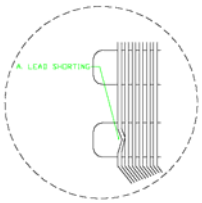
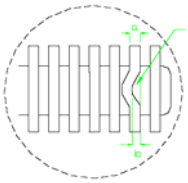
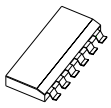
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Contact
Lead Twist</td><td>Not allowed
  </td></tr>
<tr><td>Minor</td><td>Contact
Lead
Broken</td><td>Not allowed
  </td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Contact
Lead Bent</td><td>Not allowed if
bent lead causes
short circuit
  </td></tr>
<tr><td>Not allowed if bent lead
extends horizontally
more than 50%
of its width
  </td></tr>
<tr><td>Minor</td><td>Colour
uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>Major</td><td rowspan="4">PCB
  </td><td>No unmelted solder paste should be present on PCB</td></tr>
<tr><td>Critical</td><td>Cold solder joints, missing solder connections, or oxidation are not allowed</td></tr>
<tr><td>Minor</td><td>No residue or solder balls on PCB are allowed</td></tr>
<tr><td>Critical</td><td>Short circuits on components are not allowed</td></tr>
<tr><td>Minor</td><td>Tray
particles</td><td>
<table>
<tr><th></th><th>Size</th><th>Quantity</th></tr>
<tr><td rowspan="2">On tray</td><td>∅<0.2</td><td>Any number</td></tr>
<tr><td>∅>0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>∅≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

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7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-40°C±2, 240 hours	No abnormalities in function and appearance
High Temperature Storage	80°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage(Operation)	60°C±2, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40°C 1 Hour, 85°C 1 Hour	No abnormalities in function and appearance

- The brightness should be greater than 50% of the initial brightness.
- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C; 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under 75 cd/m² brightness and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

8.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

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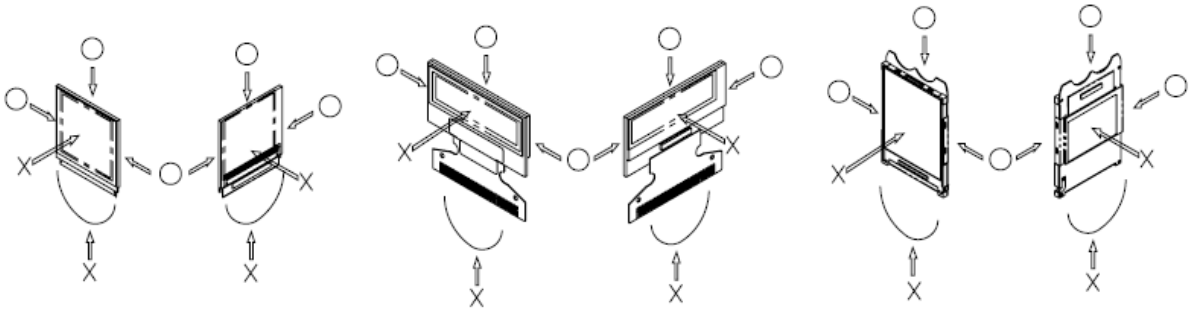
9 HANDLING PRECAUTIONS

9.1 HANDLING PRECAUTIONS

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

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11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

9.2 STORAGE PRECAUTIONS

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING PRECAUTIONS

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

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9.4 OTHER PRECAUTIONS

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

9.5 PRECAUTIONS WHEN DISPOSING OF THE OEL DISPLAY MODULES

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

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