

OLED DISPLAY MODULE

Product Specification

CUSTOMER	STANDARD	
PRODUCT NUMBER	DD-9664FC-2A	
CUSTOMER APPROVAL		

INTERNAL APPROVALS				
Product Mgr Doc Control Electr. Eng				
Bruno	Anthony	Bazile		
Recaldini	Perkins	Peter		



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A	Feb 2007			Production Release	

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1 MAIN FEATURES

ITEM	CONTENTS
Display Format	96 (R.G.B.) x 64 Dots
Overall Dimensions(W*H*T)	Glass 25.70 x 22.20 x 1.5 mm
Active Area(W*H)	20.14 x 13.42 mm
Viewing Area(W*H)	22.14 x 15.42 mm
Display Mode	Passive Matrix (0.95")
Display Colour	65,536 Colour
Driving Method	1 / 64 duty
Driver IC	SSD1331
Operating temperature	-30°C ∼ +70°C
Storage temperature	-40°C ∼ +80°C

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2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

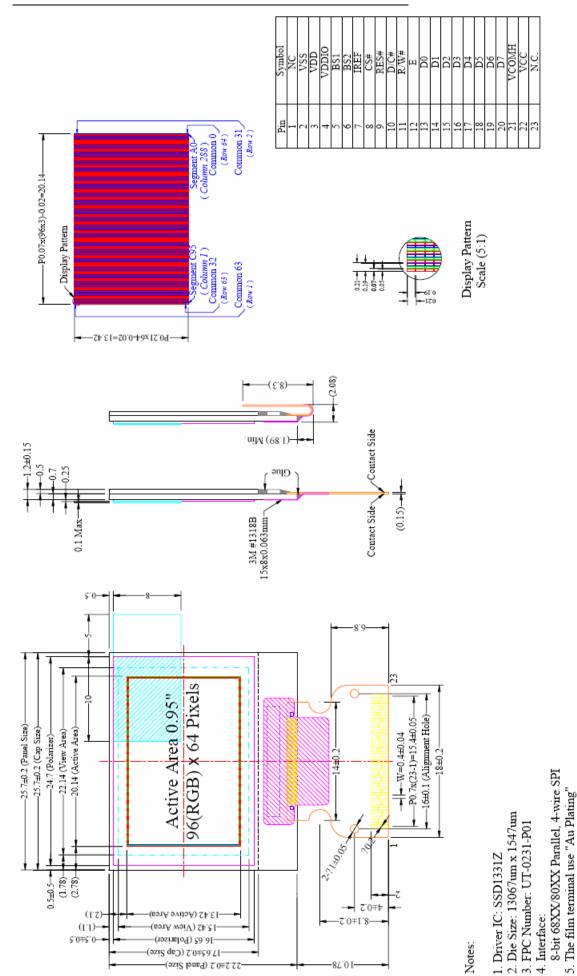
ITEM	CHARACTERISTIC	UNIT
Display Format	96 (RGB x 64	Dots
Overall Dimensions	25.70 x 22.20 x 1.50	mm
Active Area(W*H)	20.14 x 13.42	mm
Viewing Area(W*H)	22.14 x 15.42	mm
Dot Size	0. 05 x (RGB) x 0.19	mm
Dot Pitch	0.07 x (RGB) x 0.21	mm
Weight	1.8	g
IC Controller/Driver	SSD1331	

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2.2 MECHANICAL DRAWING



General Tolerance: ±0.30
 The total thickness (1.35 Max) is without Polarizer & Remove Tape.
 The actual assembled total thickness with above materials should be 1.70 Max.



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	-0.3	4	V	
Driver Supply Voltage	Vcc	0	15	V	Note 1,2
Vcc Supply Current	Icc	-	25	mA	
Operating Temperature	Тор	-30	70	°C	-
Storage Temperature	Tst	-40	80	°C	-
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "GND=0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it's desirable to use this module under the conditions according to Section 3 "Electrical Characteristics".

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3.2 ELECTRICAL CHARACTERISTICS

3.2.1 DC CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Тур	Max	Unit
Supply Logic	$V_{ m DD}$		2.4	2.8	3.5	V
Supply Voltage for I/O pins	$V_{ m DDIO}$		1.6	2.8	3.5	V
Driver Supply Voltage	Vcc		-	14.0	-	V
Operating Current for	Idd	Note 1	-	0.2	0.6	mA
V _{DD}	IDD	Note 2	-	0.2	0.6	mA
Operating Current for	Las	Note 1	-	8	11	mA
Vcc	Icc	Note 2	-	13.5	18	mA
Sleep Mode Current for VDD	Idd sleep		-	1	2	μΑ
Sleep Mode Current for VCC	Icc sleep		-	<2	2	μΑ
High Level Input	$V_{ m IH}$		$0.8 \mathrm{xV}_\mathrm{DD}$	-	$V_{ m DDIO}$	V
Low Level Input	$V_{\rm IL}$	I out = 100μ A,	0	-	$0.2xV_{DDIO}$	V
High Level Output	V_{OH}	3.3MHz	$0.9 \mathrm{xV}_{\mathrm{DDIO}}$	-	$V_{ m DDIO}$	V
Low Level Output	V_{OL}		0	-	$0.1 \text{xV}_{\text{DDIO}}$	V

Note 1: $V_{DD} = 2.8V$, $V_{CC} = 14V$, Software Initial Setting follow Section. 6 "Software initial setting", 50% Display area turn on.

Note 2: $V_{DD} = 2.8V$, $V_{CC} = 14V$, Software Initial Setting follow Section. 6 "Software initial setting", 100% Display area turn on.

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3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function		
1	N.C.	-	Reserved Pin (Supporting Pin). The supporting pins can reduce the influences from stresses on the function pins.		
2	VSS	P	Ground of System. This is a ground pin. It also acts as a reference for the logic pins, the OLED driving voltages and the analog circuits. It must be connected to external ground.		
3	VDD	P	Power Supply for Interface Logic Level. This is a voltage supply pin. It must be connected to external source.		
4.	VDDIO	P	Power Supply for Interface Logic Level. It Should match with the MCU interface voltage level. VDDIO must always be equal or lower than VDD		
5	BS1		Communicating Protocol Select. These pins are MCU interface selection input. See the following		
6	BS2	I	table: 68XX-parallel 80XX-parallel Serial BS1 0 1 0 BS2 1 1 0		
7	IREF	I	Current Reference for Brightness Adjustment. This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.		
8	CS#	I	Chip Select. This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.		
9	RES#	I	Power Reset for Controller and Driver. This pin is reset signal input. When the pin is low, initialization of the chip executed.		
10	D/C#	I	Data/Command Control. This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signal, please refer to the Timing Characteristics Diagrams.		
11	R/W#(WR#)	I	Read/Write Select or Write. This pin is MCU interface input. When interface to a 68XX-series microprocessor, this pin will be used as the Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.		
12	E(RD#)	I	Read/Write Enable or Read. This pin is MCU interface input. When interfacing to a 68XX-series microprocessor this pin will be used as the Enable (E) signal. Read/Write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.		
13~20	D0~D7	I/O	Host Data Input / Output Bus These pins are 8 bit bi-directional data bus to be connected to		

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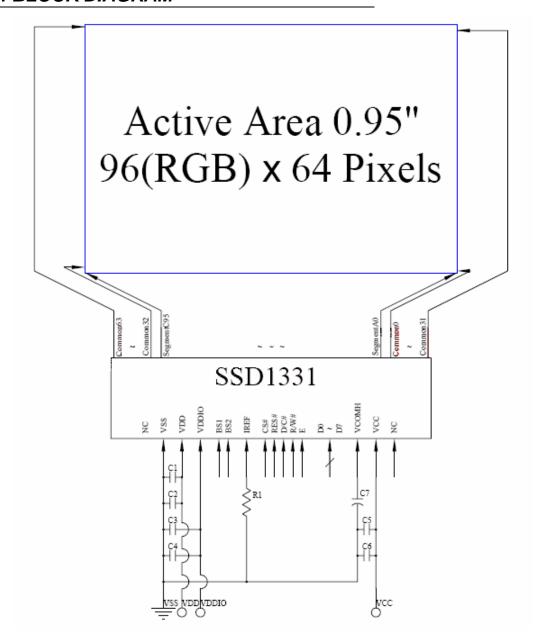


			the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
21	VCOMH	О	Voltage Output High Level for COM Signal. The COM signal deselected voltage level. A tantalum capacitor should be connected between this pin and VSS
22	VCC	P	Power Supply for OLED panel. This is the most positive voltage supply pin of the chip. It should be supplied externally.
23	N.C.	-	Reserved Pin (Supporting Pin). The supporting pins can reduce the influences from stresses on the function pins.

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MCU Interface Selection: BS1 and BS2

Pins connected to MCU interface : D7~D0, E/RD#, R/W#, CS#, D/C# and RES#

C1, C3, C5: 10µF

C2, C4, C6: 0.1 µF

C7 $4.7 \mu F/20V$ Tntalum CAP

R1: 1.2M, R1 = (Voltage at IREF – VSS) / IREF

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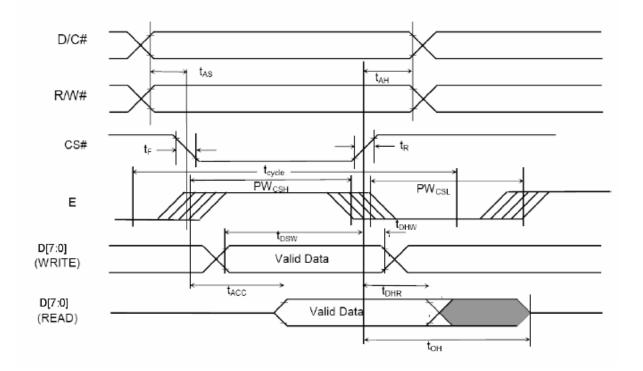
3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.1.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time (write cycle)	$t_{ m cycle}$	130	-	ns
Control Pulse Low Width (write cycle)	PWcsl	60	-	ns
Control Pulse High Width (write cycle)	PWcsh	60	-	ns
Clock Cycle Time (read cycle)	$t_{ m cycle}$	200	-	ns
Control Pulse Low Width (read cycle)	PWcsl	100	-	ns
Control Pulse High Width (read cycle)	PWcsh	100	-	ns
Address Setup Time	tAS	0	-	ns
Address Hold Time	tAH	10	-	ns
Data Setup Time	tDSW	40	-	ns
Data Hold Time	tDHW	10	-	ns
Access Time	tACC	-	140	ns
Output Disable Time	tACC	-	70	ns
Rise Time	t_{R}	-	15	ns
Fall Time	$t_{ m F}$	-	15	ns

*($V_{DD} - V_{SS} = 2.4V$ to 3.5V, $V_{DDIO} = 2.4V$ to V_{DD} , $T_a = -40$ to +85°C)



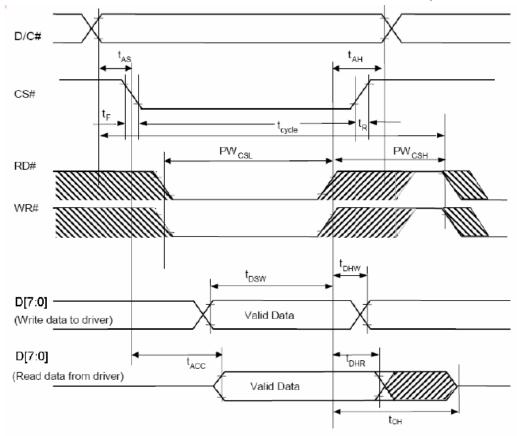
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3.5.1.2 8080-Series MPU Parallel Interface Timing Characteristics:

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t _{cycle}	130	-	ns
Address Setup Time	t_{AS}	0	-	ns
Address Hold Time	$t_{ m AH}$	10	-	ns
Write Data Setup Time	$t_{ m DSW}$	40	-	ns
Write Data Hold Time	$t_{ m DHW}$	15	-	ns
Read Data Hold Time	t _{DHR}	20	-	ns
Output Disable Time	t _{OH}	_	70	ns
Access Time	t _{ACC}	_	140	ns
Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	PW _{CSL}	120 60	-	ns
Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	PW_{CSH}	60 60	-	ns
Rise Time	t_R	_	15	ns
Fall Time	t_{F}	-	15	ns

* $(V_{DD} - V_{SS} 2.4V \text{ to } 3.5V, V_{DDIO} = 2.4V \text{ to } V_{DD}, Ta = -40 \text{ to } +85^{\circ}C)$



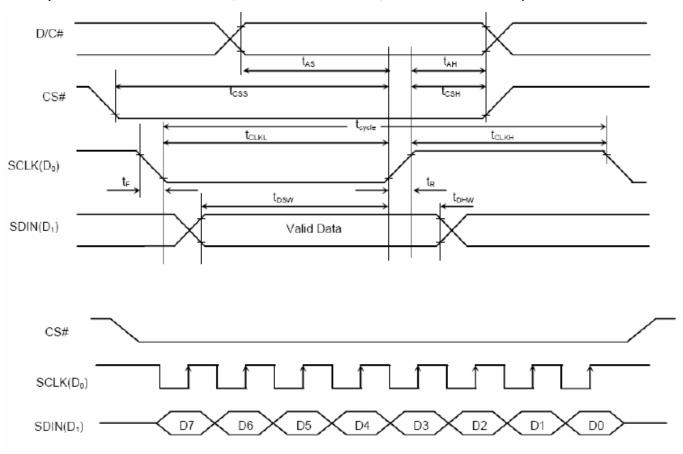
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3.5.1.3 Serial Interface Timing Characteristics:

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t _{cycle}	150	-	ns
Address Setup Time	t_{AS}	40	-	ns
Address Hold Time	t_{AH}	40	-	ns
Chip Select Setup Time	t _{CSS}	75	-	ns
Chip Select Hold Time	t _{CSH}	60	-	ns
Write Data Setup Time	$t_{ m DSW}$	40	-	ns
Write Data Hold Time	$t_{ m DHW}$	40	-	ns
Clock Low Time	t_{CLKL}	75	-	ns
Clock High Time	$t_{ m CLKH}$	75		ns
Rise Time	t_{R}	-	15	ns
Fall Time	t_{F}	-	15	ns

* ($V_{DD} - V_{SS} = 2.4V$ to 3.5V, $V_{DDIO} = 2.4V$ to V_{DD} , Ta = -40 to $+85^{\circ}C$)



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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Тур	Max	Unit
Brightness(White)	L_{br}	With Polarizer Note 1	80	100	-	cd/m ²
C.I.E.(White)	(X)	With Polarizer	0.26	0.30	0.34	
C.I.E.(WIIIte)	(Y)		0.29	0.33	0.37	-
C.I.E.(Red)	(X)	With Polarizer	0.60	0.64	0.68	
C.I.E.(Red)	(Y)		0.30	0.34	0.38	-
C.I.E.(Green)	(X)	With Polarizer	0.28	0.32	0.36	
C.I.E.(Gleen)	(Y)		0.58	0.62	0.66	-
C I E (Plus)	(X)	With Polarizer	0.11	0.15	0.19	
C.I.E.(Blue)	(Y)		0.16	0.20	0.24	-
Frame Rate			-	100	-	F/sec
Dark Room Contrast	CR	Shown as below	-	>1:1000	-	-
View Angle			>160	-	-	degree

Optical measurement taken at VDD = 2.8V, VCC = 14V and software configuration follows Section 6 "Software Initial Setting"

Note 1: Brightness (Lbr) and Driver Supply Voltage (Vcc) are subject to the change of the panel characteristics and the customer's request.

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5 APPLICATION NOTES

5.1 COMMANDS

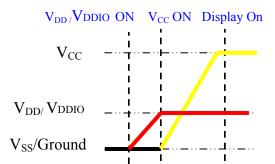
Please refer to the Technical Manual for the SSD1331.

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

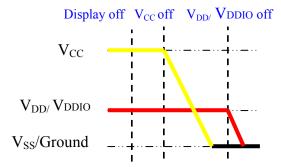
5.2.1 POWER UP SEQUENCE:

- 1. Power up V_{DD} & V_{DDIO}
- 2. Send Display off command
- 3. Clear Screen
- 4. Power up V_{CC}
- 5. Delay 100ms (When V_{DD}& V_{DDIO} is stable)
- 6. Send Display on command



5.2.2 POWER DOWN SEQUENCE:

- 1. Send Display off command
- 2. Power down V_{CC}
- 3. Delay 100ms (when V_{CC} is reach 0 and panel is completely discharges)
- 4. Power down V_{DD}& V_{DDIO}



5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

- 1. Display is off
- 2. 64MUX Display Mode
- 3. Display start line is set at display RAM address 0
- 4. Display offset set to 0
- 5. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
- 6. Column address counter is set at 0
- 7. Master contrast control register is set at 0FH
- 8. Individual contrast control registers of colour A, B and C are set at 80H.
- 9. Shift register data clear in serial interface
- 10. Normal display mode (Equivalent to A4 command)

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5.4 APPLICATION EXAMPLE

Command usage and explanation of an actual example

< Initialization Setting > Set Display On/Off (1010111X) 10101110=>0xAE (Display Off)

Set Display Mode (101001XX) 10100100=>0xA4 (Normal Display Mode)

Set Display Clock Divide Ratio / Oscillator Frequency (10110011 with XXXXXXXX)

Set Display Offset (10100010 with XXXXXXXX)

Set Multiplex Ratio (11001000 with XXXXXXXX)

Set Master Configuration (10101101 with 1000111X) 10001110=>0x8E (External VCC supply selected)

Set Display Start Line (10100001 with XXXXXXXX) Set Segment Re-map & Data Format (10100000 with XXXXXXXXX)

Set Pre-charge Level
(10111011 with **XXXXXX)
Set Second Pre-charge speed of colour A
(10001010 with XXXXXXXX
Set Second Pre-charge speed of Colour B
(10001011 with XXXXXXXXX)
Set Second Pre-charge speed of Colour C
(10001100 with XXXXXXXXX)
Set VCOMH
(10111110 with 00XXXXXX)

Set Phase 1 & 2 Period Adjustment (10110001 with XXXXXXXX)

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Set Power Saving Mode (10110000 with 000XXXXX)

Set Display On/Off (1010111X) 10101111=> 0xAF (Display On)

<Display Boundary Settings>
Set Colum Address
(00010101 with XXXXXXXXX for Start & XXXXXXXXX for End)
Set Row Address
(01110101 with XXXXXXXXX for Start & XXXXXXXXX for End)

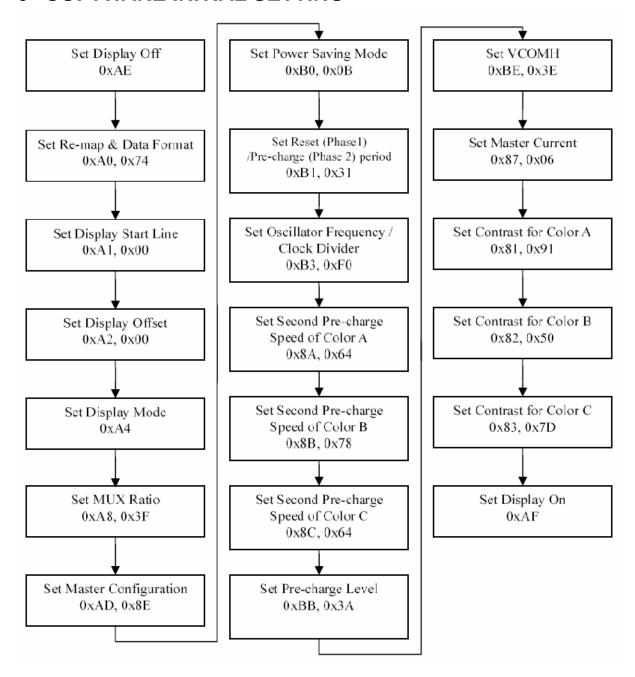
If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

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6 SOFTWARE INITIAL SETTING



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7 PACKAGING AND LABELLING SPECIFICATION

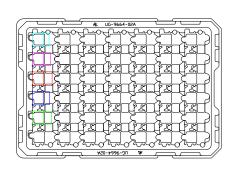
7.1 PACKAGING

7.1.1 Material

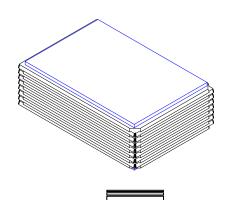
	Item	Part code	Dimensions (mm)	Unit weight (kg)	Quantity
1	Module	DD-9664FC-2A	25.7*22.1*1.5	0.002	2520
2	Tray	****	***	0.010	
3	Inner box	****	***	0.250	4
4	Carton	****	***	1.100	1
5	Inner box bag	****	***	***	***
6	Total weight	7.54 K	g	± 5%	

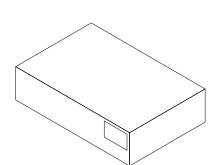
7.1.2 Specification and quantity

Modules x tray Quantity per row Quantity per column 6 7 = 42Modules per box Quantity per tray Quantity of trays 15 = 63042 X Total no. of modules Quantity per box Quantity of boxes 630 x = 2520

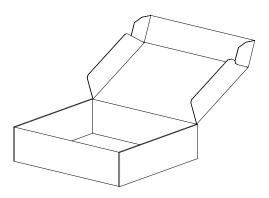








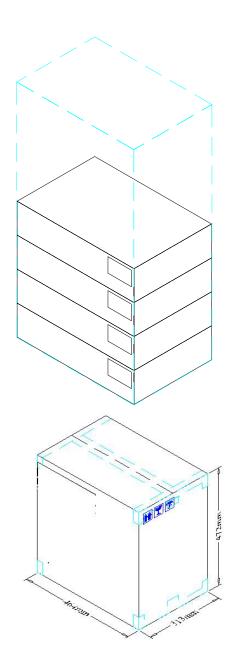




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7.2 LABELLING & MARKING

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8 QUALITY ASSURANCE SPECIFICATION

8.1 CONFORMITY

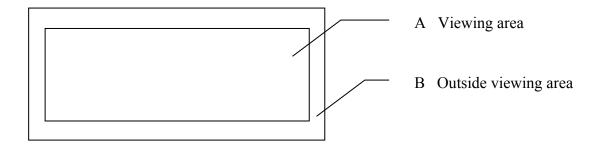
The performance, function and reliability of the shipped products conform to the Product Specification.

8.2 DELIVERY ASSURANCE

8.2.1 Delivery inspection standards

• IPC-AA610 rev. C, class 2 electronic assemblies standard

8.2.2 Zone definition



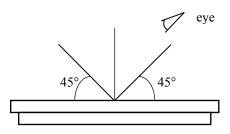
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8.2.3 Visual inspection

- Inspect under 30W fluorescent lamp leaving 50 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
- Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
- Inspect the module at 45° right and left, top and bottom.
- Use the optimum viewing angle during the contrast inspection.



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8.2.4 Standard of appearance inspection

Units: mm

Units. in						
Class	Item	Criteria				
Minor	Packing &	Outside & in	nside package	Presence of pro	oduct no., lot no.,	quantity
Critical	Label	Product mus	t not be mixe	d with others and	quantity must not	be different from
			d on the labe			
Major	Dimension	Product dim	ensions must	be according to sp	pecification and d	rawing
Major	Electrical	Product elec	trical charact	eristics must be ac	ccording to specifi	cation
Critical	OLED Display	Missing line	s or wrong pa	atterns on display	are not allowed	
Minor	Black spot, white spot,	Round type: $\emptyset = (X+Y)/2$	as per follow	ving drawing		
	dust			A	cceptable quantity	/
				Size	Zone A	Zone B
			<u> </u>	Ø<0.1	Any number	
			Y	0.1<Ø<0.2	3	A my my maham
		→ ,,	F	0.2<Ø<0.25	1	Any number
		X		0.25<Ø	0	
		Line type: as	s per followin		ble quantity Zone A	Zone B
				W≤0.05	Any number	Zone B
			L≤2.0	W≤0.1	3	Any number
			L>2.0		0]
		L	Total accep	table quantity: 3		
Minor	Polariser	Scratch on protective film is permitted				
2.51	scratch		olariser: sam	e as No. 1		
Minor	Polariser	$\emptyset = (X+Y)/2$	2			
	bubble	Acceptable quantity				
				Size	Zone A	Zone B
			<u>k</u>	Ø<0.5	Any number	Any number
		X	Y	Ø>0.5	0	
		Total acceptable quantity: 3				

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Class	Item	Criteria		
Minor	Segment deformation	1b. Pin hole on dot matrix display	Acceptable Size $a,b<0.1$ $(a+b)/2\leq0.1$ $0.5<\varnothing<1.0$ Total acceptable	Any number Any number 3
		2. Segments / dots with different width	Accep a≥b a <b< td=""><td>table a/b≤4/3 a/b>4/3</td></b<>	table a/b≤4/3 a/b>4/3
		3. Alignment layer defect $\emptyset = (a+b)/2$	Acceptable Size $\emptyset \leq 0.4$ $0.4 < \emptyset \leq 1.0$ $1.0 < \emptyset \leq 1.5$ $1.5 < \emptyset \leq 2.0$ Total acceptable	Any number 5 3 2
Minor	Panel Chipping	$X \le 1/6$ Panel length $Y \le 1$ $Z \le T$		7
Minor	Panel Cracking	Cracks not allowed		
Minor	Cupper exposed (pin or film)	Not allowed if visible by eye inspection		
Minor	Film or Trace Damage	Not allowed if affects electrical function		

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Class	Item	Criteria			
Minor	Contact Lead Twist	Not allowed			
Minor	Contact Lead Broken	Not allowed			
Minor	Contact Lead Bent	Not allowed if bent lead causes short circuit			
		Not allowed if bent extends horizontall more than 50% of its width	/ 1111111		
Minor	Colour uniformity	Level of sample for approval set as limit sample			
Major	PCB	No unmelted solder paste should be present on PCB			
Critical		Cold solder joints, missing solder connections, or oxidation are not allowed			
Minor		No residue or solder balls on PCB are allowed			
Critical	30	Short circuits on components are not allowed			
Minor	Tray	,		Size	Quantity
	particles		On tray	Ø<0.2	Any number 4
				Ø>0.25 Ø≥0.25	2
			On display	L = 3	1
					-

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8.3 DEALING WITH CUSTOMER COMPLAINTS

8.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

8.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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9 RELIABILITY SPECIFICATION

9.1 CONTENTS OF RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-30°C±2, 240 hours	No abnormalities in function and appearance
High Temperature Storage	80°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Operation	60°C, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycles of -40°C to 85°C, 1 hour dwell	No abnormalities in function and appearance

^{*} The samples used for the above tests do not include polarizer.

9.2 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples wewe left at room temperature for 2 hrs prior to conducting the failure teat at 23 ± 5 °C; $55\pm15\%$ RH.

9.3 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under ordinary operating and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

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^{*} No moisture condensation is observed during tests.



10 HANDLING PRECAUTIONS

Safety

If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes. If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface. Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS} . Do not input any signals before power is turned on.

Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.

To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions

When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH.

Store the display in a clean environment, free from dust, organic solvents and corrosive gases. Do not crash, shake or jolt the display (including accessories).

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