

# OLED DISPLAY MODULE

## Application Notes

<b>PRODUCT NUMBER</b>	<b>DD-9664FC-2A with EVK board</b>
---------------------------	------------------------------------

## TABLE OF CONTENTS

<b>1</b>	<b>EVK SCHEMATIC.....</b>	<b>4</b>
<b>2</b>	<b>SYMBOL DEFINITION .....</b>	<b>5</b>
<b>3</b>	<b>TIMING CHARACTERISTICS .....</b>	<b>6</b>
<b>4</b>	<b>CONNECTION BETWEEN OLED AND EVK .....</b>	<b>9</b>
<b>5</b>	<b>MODULE POWER UP SEQUENCE .....</b>	<b>11</b>
5.1	POWER DOWN AND POWER UP SEQUENCE.....	11
<b>6</b>	<b>HOW TO USE THE DD-9664FC-2A .....</b>	<b>12</b>
<b>7</b>	<b>HOW TO USE THE DD-9664FC-2A .....</b>	<b>13</b>
7.1	RECOMMENDED INITIAL CODE .....	13

Product No.	DD-9664FC-2A	REV. A

Page	2 / 15
------	--------

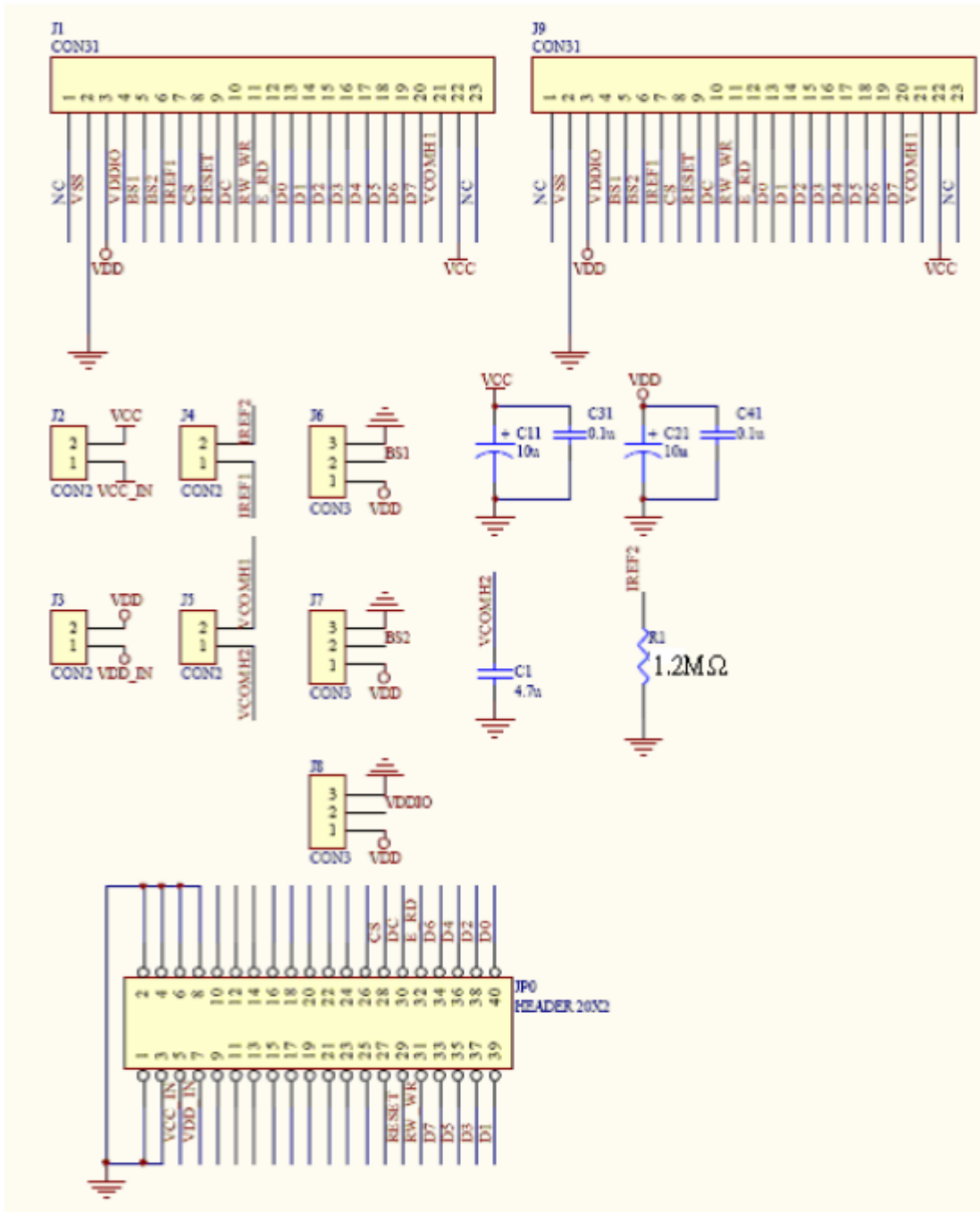
REVISION RECORD

<b>Rev.</b>	<b>Date</b>	<b>Page</b>	<b>Chapt.</b>	<b>Comment</b>	<b>ECR no.</b>
A	14 <sup>th</sup> Sep 2007			First Issue	

Product No.	DD-9664FC-2A	REV. A

Page	3 / 15
------	--------

# 1 EVK Schematic



Product No.	DD-9664FC-2A	REV. A

Page	4 / 15
------	--------

## 2 Symbol Definition

**D0-D7** : These pins are 8-bit bi-directional data bus to be connected to the MCU's data bus.

**BS1, BS2** : These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table. User can fix these pins by jumper (J6, J7) or can setup by programme.

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS1	<b>0</b>	<b>1</b>	<b>0</b>
BS2	<b>1</b>	<b>1</b>	<b>0</b>

**Table 1 – MCU Interface Selection Setting**

**E/RD#** : This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD) must be connected to VSS.

**R/W#** : This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When 8080 interface mode is selected, this pin is the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W must be connected to VSS.

**D/C#** : This pin is Data/Command control pin. When the pin is pulled high, the data at D0-D8 is treated as display data. When the pin is pulled low, the data at D0-D8 is transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams at following pages and datasheet.

**RESET#** : This pin is reset signal input. When the pin is low, initialization of the chip is executed.

**CS#** : This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

**VCC** : This is the most positive voltage supply pin of the chip.

**VDD** : Power supply pin for logic operation of the driver.

**VCC\_IN**: This is the external most positive voltage supply. This pin should be shorted with VCC by Jumper 2 (J2)

**VDD\_IN**: This is the external positive voltage supply. This pin should be shorted with VDD by Jumper 3 (J3)

**VDDIO**: Power supply for interface logic level. It should be match with the MCU interface voltage level. VDDIO must always be equal or lower than VDD (J8)

Product No.	DD-9664FC-2A	REV. A

Page	5 / 15
------	--------

### 3 Timing characteristics

VDD = 2.4 to 3.5V, TA = -40 to 85°C

(VDD - VSS = 2.4V to 3.5V, VDDIO = 2.4V to VDD, TA = -40 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time (write cycle)	130	-	-	ns
PW <sub>CSL</sub>	Control Pulse Low Width (write cycle)	60	-	-	ns
PW <sub>CSH</sub>	Control Pulse High Width (write cycle)	60	-	-	ns
$t_{cycle}$	Clock Cycle Time (read cycle)	200	-	-	ns
PW <sub>CSL</sub>	Control Pulse Low Width (read cycle)	100	-	-	ns
PW <sub>CSH</sub>	Control Pulse High Width (read cycle)	100	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
$t_{AH}$	Address Hold Time	10	-	-	ns
$t_{OSW}$	Data Setup Time	40	-	-	ns
$t_{DHW}$	Data Hold Time	10	-	-	ns
$t_{ACC}$	Data Access Time	-	-	140	ns
$t_{OH}$	Output Hold time	-	-	70	ns
$t_r$	Rise Time	-	-	15	ns
$t_f$	Fall Time	-	-	15	ns

Table 2 6800-Series MPU Parallel Interface Timing Characteristics

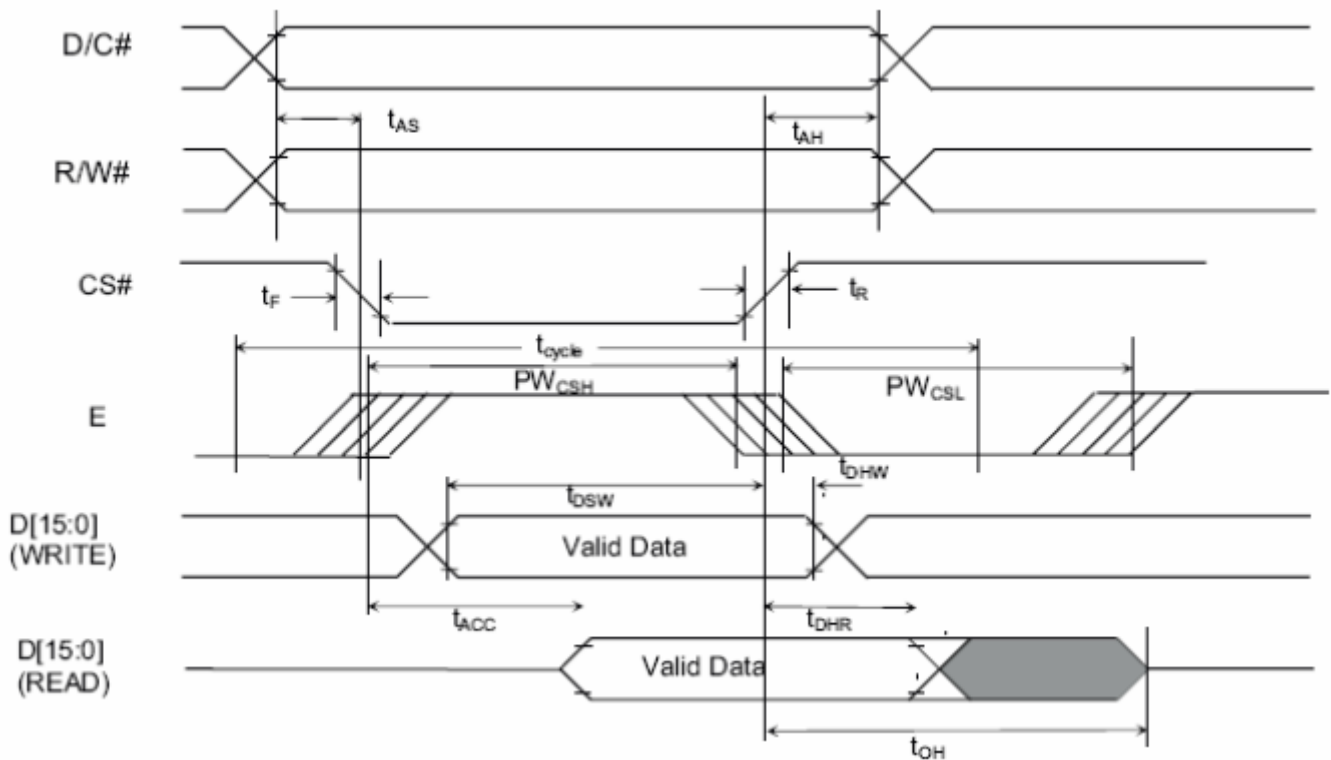


Figure 1 6800-series MPU parallel interface characteristics

Product No.	DD-9664FC-2A	REV. A

Page	6 / 15
------	--------

(VDD - VSS = 2.4V to 3.5V, VDDIO = 2.4V to VDD, TA = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	130	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
$t_{AH}$	Address Hold Time	10	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	10	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read)	100	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

TABLE 3 8080-SERIES MPU Parallel Interface Timing Characteristics

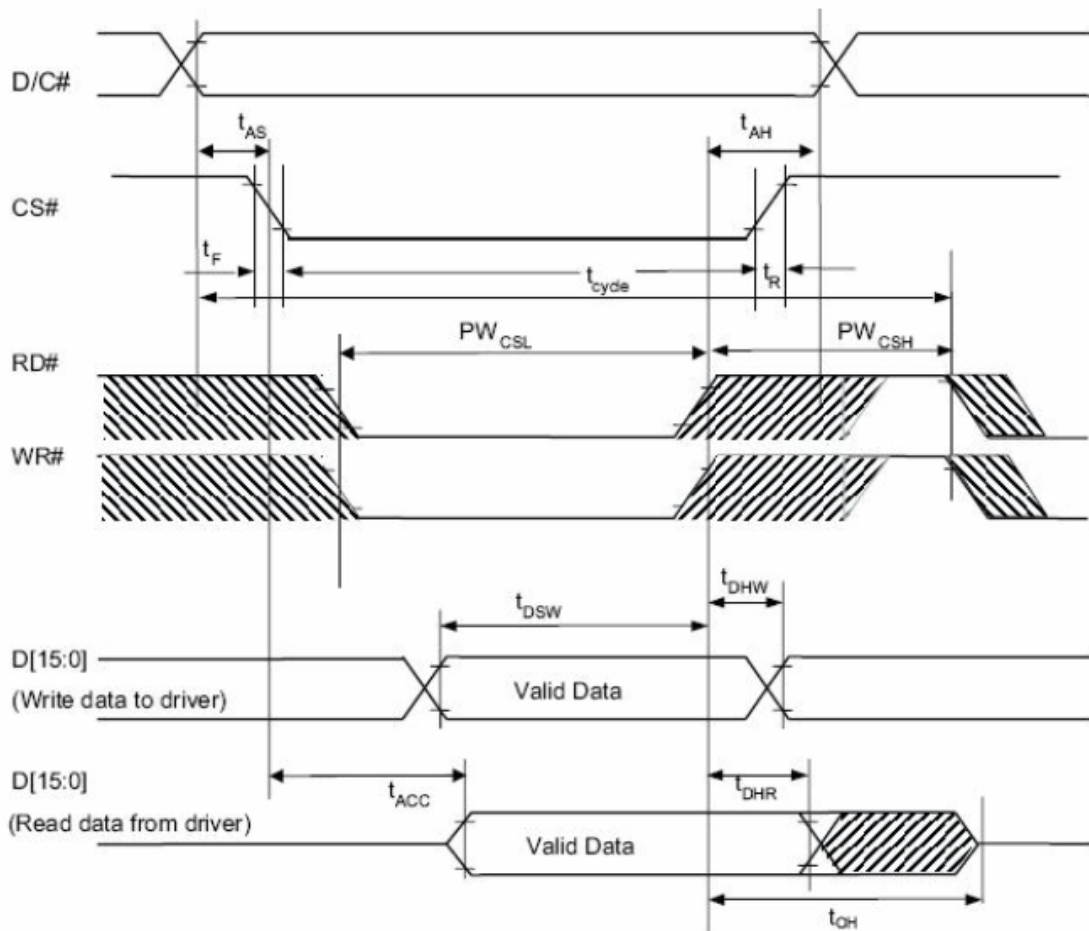


Figure 2 8080-series MPU parallel interface characteristics

Note : When 8 bit used: D<sub>0</sub> ~ D<sub>7</sub> instead.

Product No.	DD-9664FC-2A	REV. A

Page	7 / 15
------	--------

(VDD - VSS = 2.4V to 3.5V, VDDIO = 2.4V to VDD, TA = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	150	-	-	ns
$t_{AS}$	Address Setup Time	40	-	-	ns
$t_{AH}$	Address Hold Time	40	-	-	ns
$t_{CSS}$	Chip Select Setup Time	75	-	-	ns
$t_{CSH}$	Chip Select Hold Time	60	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	40	-	-	ns
$t_{CLKL}$	Clock Low Time	75	-	-	ns
$t_{CLKH}$	Clock High Time	75	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

Table 4 Serial Interface Timing Characteristics

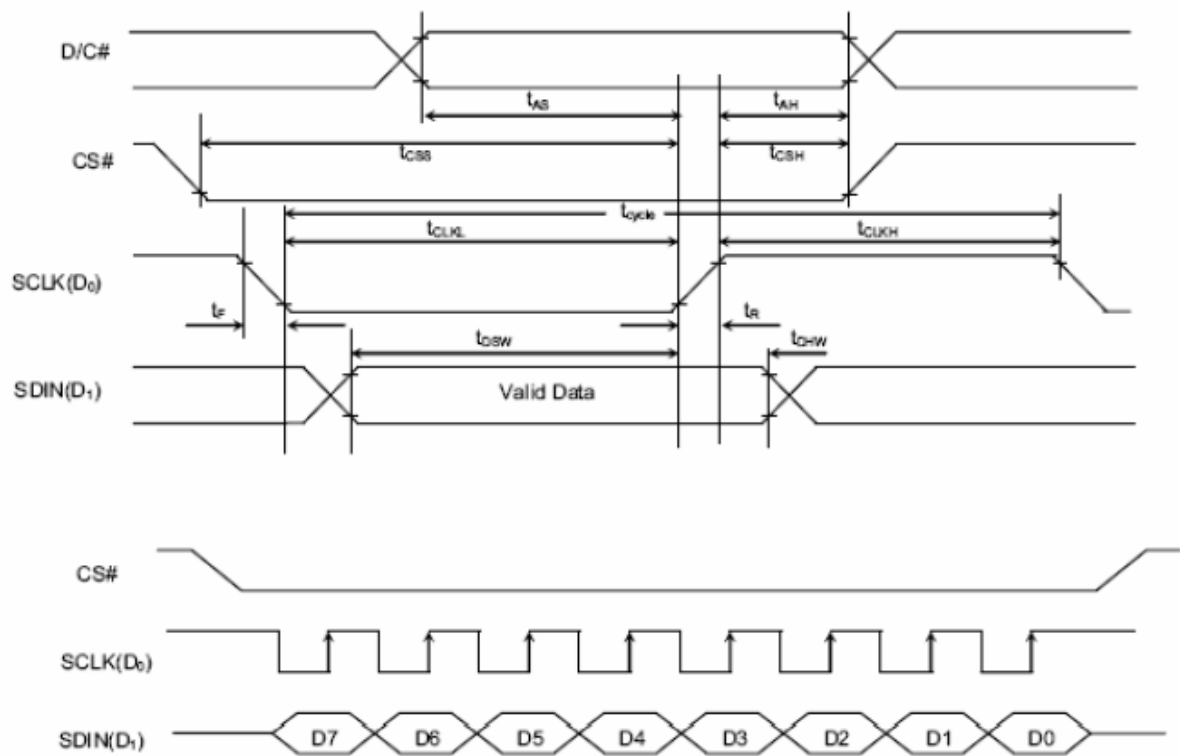


Figure 3 Serial interface characteristics



## 4 Connection Between OLED and EVK

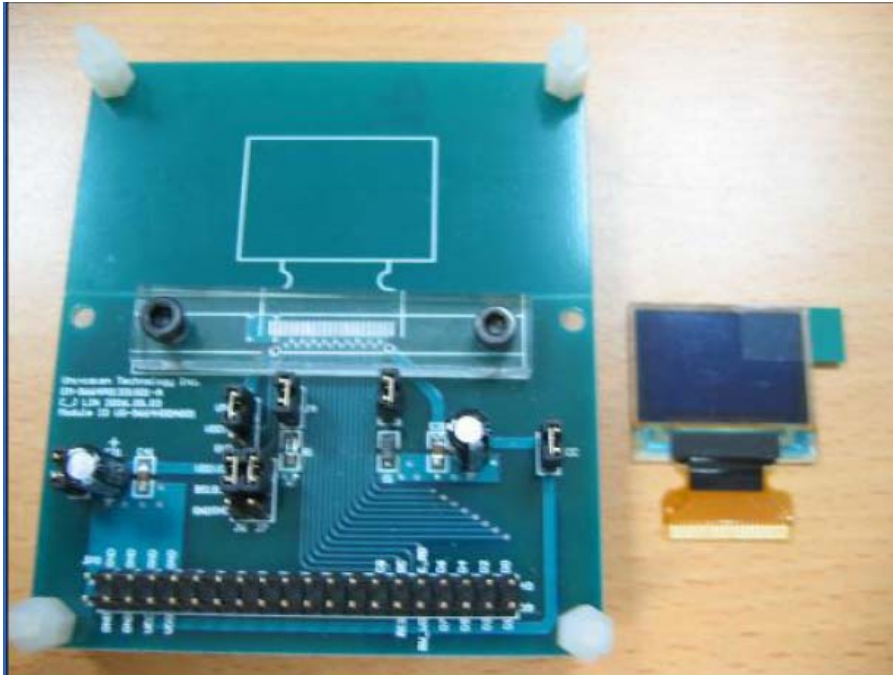


Figure 4 EVK PCB and DD-9664FC-2A Module

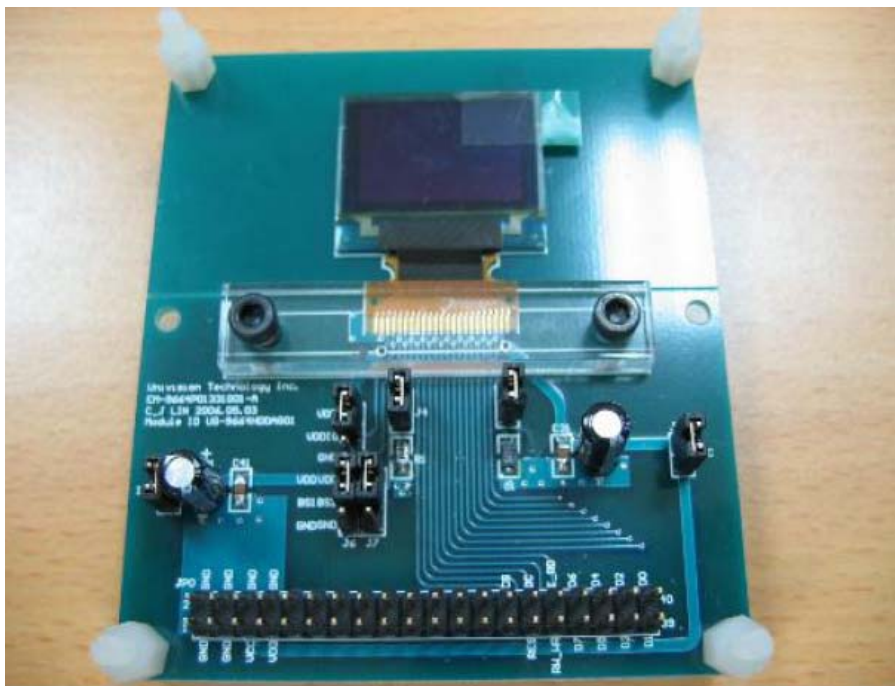
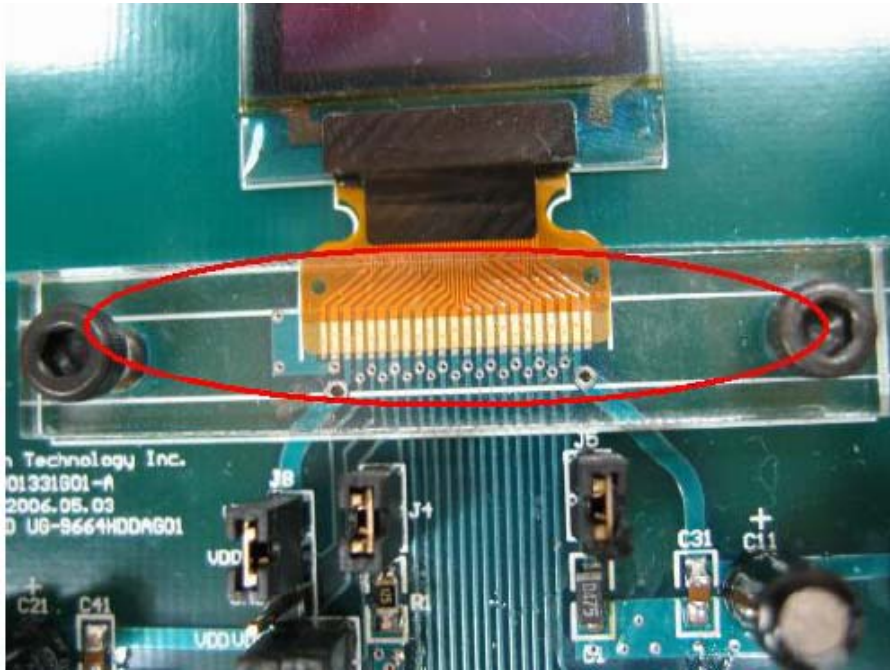


Figure 5 the DD-9664FC-2A and EVK assembled (Top view)

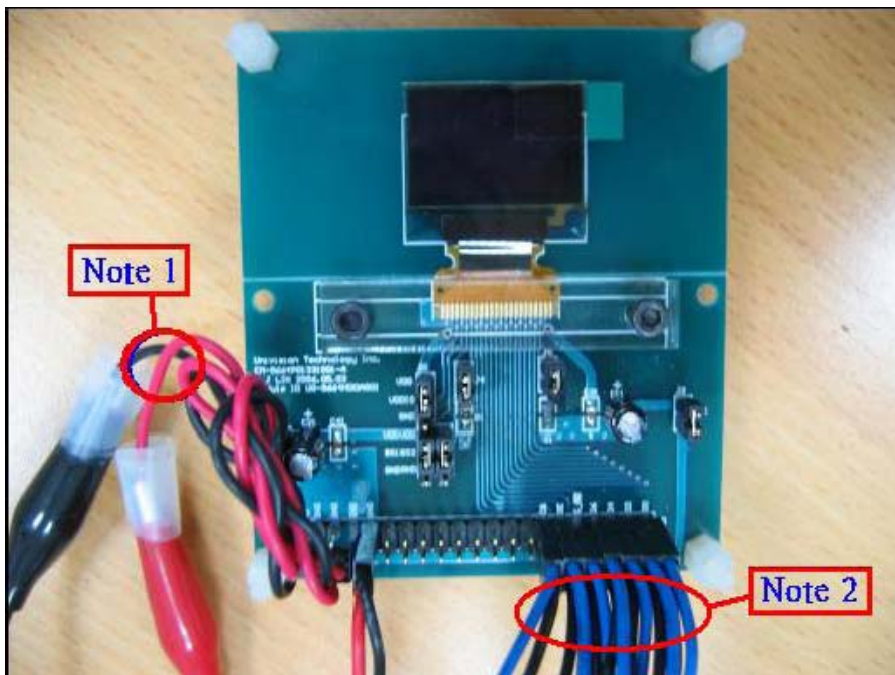
Product No.	DD-9664FC-2A	REV. A

Page	9 / 15
------	--------



**Figure 6 control MCU (not supplied ) connected with EVK**

DD-9664FC-2A is a COG type module, please refer to Fig 5, Fig 6. The user can use leading wire to connect EVK with customers system. The example shows as Fig 7.



**Figure 7 control MCU connected with EVK**

Note 1: It is the external most positive voltage supply. In this sample is connected to power supply.

Note 2: The leading wire has 13 pins totally in this case. (D0-D7, E/RD#, R/W#, E/RD~,RES#,CS#)

Product No.	DD-9664FC-2A	REV. A

Page	10 / 15
------	---------

## 5 Module Power Up Sequence

### 5.1 Power down and Power up sequence

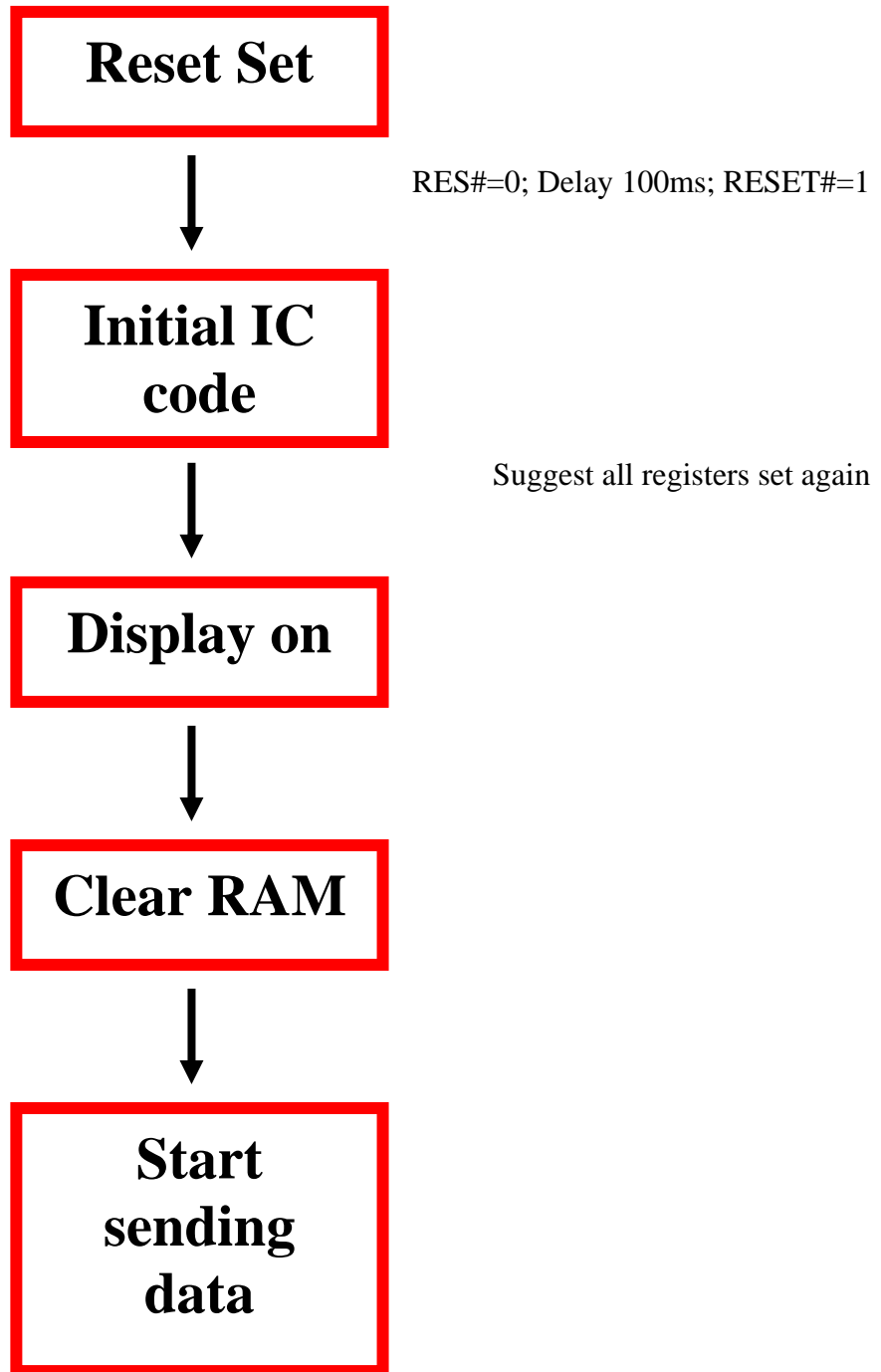
To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

<p>1.1 Power up Sequence:</p> <ol style="list-style-type: none"> <li>1. Power up <math>V_{DD}</math></li> <li>2. Send Display off command</li> <li>3. Driver IC Initial Setting</li> <li>4. Clear Screen</li> <li>5. Power up <math>V_{DDH}</math></li> <li>6. Delay 100ms (when <math>V_{DD}</math> is stable)</li> <li>7. Send Display on command</li> </ol>	
<p>1.2 Power down Sequence:</p> <ol style="list-style-type: none"> <li>1. Send Display off command</li> <li>2. Power down <math>V_{DDH}</math></li> <li>3. Delay 100ms (when <math>V_{DDH}</math> is reach 0 and panel is completely discharges)</li> <li>4. Power down <math>V_{DD}</math></li> </ol>	

Product No.	DD-9664FC-2A	REV. A
-------------	--------------	--------

Page	11 / 15
------	---------

## 6 How to use the DD-9664FC-2A



Product No.	DD-9664FC-2A	REV. A

Page	12 / 15
------	---------

## 7 How to use the DD-9664FC-2A

### 7.1 Recommended Initial code

---

```

Void Initial_ic(void)

{
  IOCLR=0xffffffff; //data=0

  IOSET=bBS1|bBS2|bRES|bCS|bE_RD;

  IOCLR=bD_C|bR_W;

  Reset_SSD1331Z();

  Write_Register (0xae); //Display off

  Write_Register(0x81); //set contrast for colorA
  Write_Register(0x91); //145
  Write_Register(0x82); //set contrast for colorB

  Write_Register(0x50); //80

  Write_Register(0x83); //set contrast for colorC

  Write_Register(0x7d); //125

  Write_Register(0x87); //master current control

  Write_Register(0x06); //6

  Write_Register(0x8a); //Set Second Pre-change Speed For ColorA
  Write_Register(0x64); //100
  Write_Register(0x8b); //Set Second Pre-change Speed For ColorB
  Write_Register(0x78); //120
  Write_Register(0x8c); //Set Second Pre-change Speed For ColorC
  Write_Register(0x64); //100
  Write_Register(0xa0); //set re=map & data format
  Write_Register(0x74);
  Write_Register(0xa1); //set display start line

  Write_Register(0x00);
  Write_Register(0xa2); //set display offset
  Write_Register(0x00);

```

Product No.	DD-9664FC-2A	REV. A

Page	13 / 15
------	---------

```

Write_Register(0xa4);    //set display mode

Write_Register(0xa8);    //set multiplex ratio

Write_Register(0x3f);

Write_Register(0xad);    //set master configuration
Write_Register(0x8e);

Write_Register(0xb0);    //set power save

Write_Register(0x00);

Write_Register(0xb1);    //phase 1 and 2 period adjustment

Write_Register(0x31);
Write_Register(0xb3);    //display clock divider / oscillator frequency
Write_Register(0xf0);

Write_Register(0xbb);    //Set Pre-Change Level

Write_Register(0x3a);    //58

Write_Register(0xbe);    //set vcomh

Write_Register(0x3e);    //62

Write_Register(0xaf);    //set display on}

void Reset_SSD1331Z(void)
{

IOCLR=bRES;
Delay_1ms(10);
IOSET=bRES;

void Write_Register (unsigned char out_command)
{

IOCLR=bD_C;
IOCLR=bCS;
IOCLR=bR_W;
IOCLR=0x000000ff;
IOSET= out_command; IOSET=bR_W;
IOSET=bCS;
}

```

Product No.	DD-9664FC-2A	REV. A

Page	14 / 15
------	---------

```
void Write_Data (unsigned char out_data)
```

```
IOSET=bD_C;  
IOCLR=bCS;
```

```
IOCLR=bR_W;  
IOCLR=0x000000ff;  
IOSET=out_data;  
IOSETbR_W;  
IOSET=bCS;  
}
```

```
void Delay_1ms(int Cycle)
```

```
{  
  
unsigned int i,k;  
for (i=0 ;i<Cycle;i++)  
for(k=0;k<0x2fff;k++);  
  
}
```

Product No.	DD-9664FC-2A	REV. A

Page	15 / 15
------	---------

## **X-ON Electronics**

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [densitron](#) manufacturer:*

Other Similar products are found below :

[DMT024QVNUNT0-2C](#) [DMT028QVNTNT0S-1A](#) [DMT028QVHXCMI-1A](#) [DMT024QVNUCMI-2A](#) [LMR4048BG2C16HNG/5V](#)