Dersonic®
德信立業 創新開拓

獨石電容器承認書

APPROVAL SPECIFICATIONS FOR MONOLITHIC CAPACITORS

(AEC-Q200 REV.)

客戶 CUSTOMER	立創商城		
客戶料號 CUSTOMER P/N	C3293121		
規格描述 DESCRIPTION	100V/224K/F5.08/L24/X7R/0805/AEC-Q200		
產品品號 PART NUMBER	CD2A224KC9IER1EZAE		
日期 DATE	2022-07-08	文件編號 DOC. NO.	DEC-SA-WI010

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1. APPLICATION

This specification is applied to ZAE series monolithic capacitor in accordance with AEC-Q200 requirements used for automotive electronic equipment.

ZAE series monolithic capacitor has the following characteristics:

- Complies AEC-Q200 requirements
- Miniature size, large capacitance, tape and reel packaging suitable for auto-placement.
- Epoxy coating creates excellent performance in humidity resistance, mechanical strength and heat resistance.
- Standard size, various lead configurations.
- Comply with RoHS 2.0, reach, halogen-free available.

2. PART NUMBER (RATING)

CD	2A	224	K	C	9	I	E	R1	E	ZAE
Type	Rated voltage	Nominal capacitance	Capacitance tolerance	Lead spacing	Lead style	Lead length or taping	Coating	Temp. Char.	Chip	Series

■ Type: CD: Monolithic capacitors

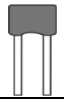
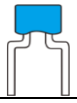
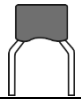
■ Rated voltage: 1H: DC50V; **2A: DC100V**; 2E: DC250V; 2J: DC630V; 3A: DC1KV

■ Nominal capacitance: The first two digits denote significant figures; the last digit denotes the multiplier of 10 in pF.
ex.) In case of **224**
$22\times10^4=220000pF=0.22\mu F$

■ Capacitance tolerance: J: ±5%; **K: ±10%**; M: ±20%

■ Lead spacing (F): A: 2.54mm; **C: 5.08mm**

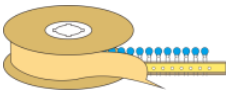
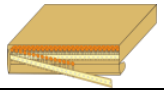
■ Lead style (L):

1: 
9: 
0: 

■ Lead length or taping:

● **Lead length (Bulk)**

4: 3.5mm	6: 4mm
8: 5mm	9: 6mm
A: 8mm	B: 10mm
I: 24mm	M: 32mm

● Taping
T: Reel packing 
P: Ammo packing 

■ Coating: **E: Epoxy coating (Blue)**

■ Temperature characteristic:

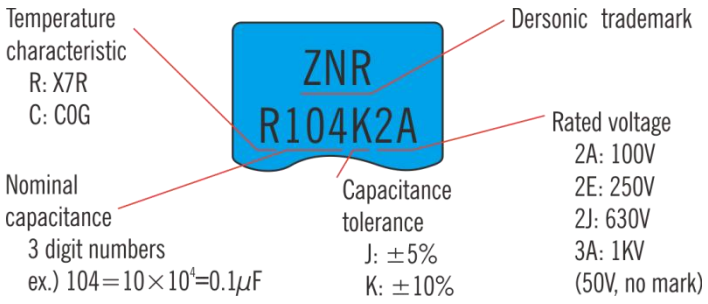
Code	Temperature characteristic	Temperature range	Temperature coefficient	Standard temperature	Operating temp. range
CH	C0G	-55～25℃	0+30/-72ppm/℃	25℃	-55～125℃
		25～125℃	0±30ppm/℃		

Code	Temperature characteristic	Temperature range	Capacitance change	Standard temperature	Operating temp. range
R1	**X7R**	**-55～125℃**	**±15%**	**25℃**	**-55～125℃**

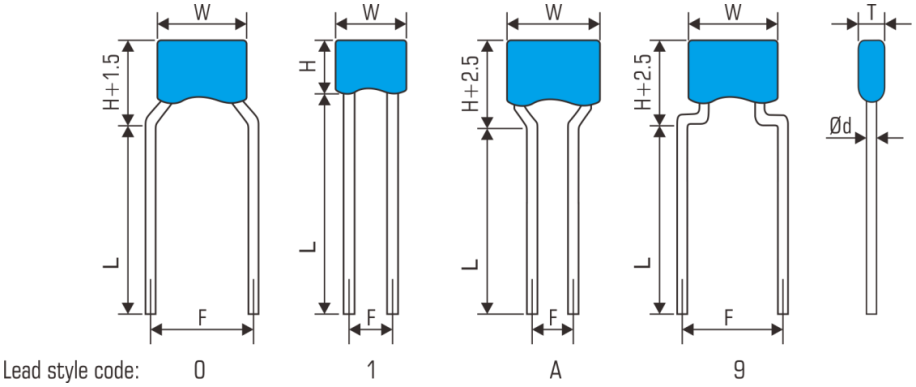
■ Chip: **E: 0805**; F: 1206; G: 1210

■ Series: **ZAE: complies AEC-Q200 requirements**

3. MARKING



4. SPECIFICATIONS LIST

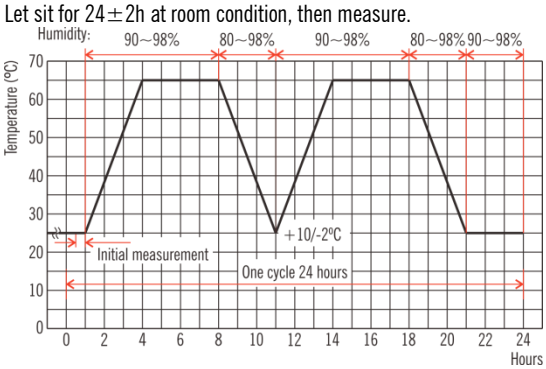


Chip	Temperature characteristic	Capacitance range	Tolerance	Dimensions (mm) W max	H max	T max	F ±0.8	Ød ±0.1	Lead style
0805	C0G	50V: 100-103 100V: 100-682 250V: 100-222 630V: 100-391	±5% ±10%	4.5	3.8	3.5	2.54 5.08	0.47	1 9 0
	X7R	50V: 101-224 100V: 101-104 250V: 101-223 630V: 101-103	±10%						
1206	C0G	50V: 100-103 100V: 100-103 250V: 100-472 630V: 100-222 1KV: 100-102	±5% ±10%	5.5	4.5	4.0	5.08	0.47	9 0
	X7R	50V: 151-475 100V: 151-105 250V: 101-104 630V: 101-103	±10%						
1210	C0G	50V: 100-473 100V: 100-473 250V: 100-153 630V: 100-103 1KV: 100-102	±5% ±10%	5.5	6.5	4.5	5.08	0.47	9 0
	X7R	50V: 102-105 100V: 102-105 250V: 101-474 630V: 101-223 1KV: 101-103	±10%						

5. AEC-Q200 MURATA STANDARD SPECIFICATIONS AND TEST METHODS

Test and measurement shall be made at the room condition (temperature 15 to 35℃, relative humidity 45 to 75%, atmosphere pressure 86 to 106kPa).

Unless otherwise specified herein, If doubt occurred on the value of measurement, and measurement was requested by customer capacitors shall be measured at the reference condition (temperature 25±2℃, relative humidity 60 to70%, atmosphere pressure 86 to 106kPa).

No	Test Item		Specification	Test Method
1	Pre-and Post-Stress Electrical Test			
2	High Temperature Exposure (Storage)	Appearance	No defects or abnormalities.	Sit the capacitor for 1000±12h at 150±3℃. Let sit for 24±2h at, room condition then measure. ■ Pretreatment Perform the heat treatment at 150+0/-10℃ for 60±5 min and then let sit for 24±2h at room condition.
		ΔC/C	C0G: Within ±3% or ±0.3pF (Whichever is larger) X7R: within ±12.5%	
		DF or Q	C0G: ≥30pF, Q>350 <30pF, Q>275+5C/2 X7R: 0.04 max.	
		IR	More than 10% initial specified value.	
3	Temperature Cycling	Appearance	No defects or abnormalities.	Perform the 1000 cycles according to the four heat treatments listed in the following table. Let sit for 24±2h at room condition, then measure. Step / 1 / 2 / 3 / 4 Temp (℃) / -55 +0/-3 / Room temp. / 125 +3/-0 / Room temp. Time (min.) / 15±3 / 1 / 15±3 / 1 ■ Pretreatment Perform the heat treatment at 150+0/-10℃ for 60±5 min and then let sit for 24±2h at room condition.
		ΔC/C	C0G: Within ±5% or ±0.5pF (Whichever is larger) X7R: within ±12.5%	
		DF	C0G: ≥30pF, Q>350 <30pF, Q>275+5C/2 X7R: 0.05 max.	
		IR	More than 10% initial specified value.	
4	Moisture Resistance	Appearance	No defects or abnormalities.	Apply the 24h heat (25 to 65℃) and humidity (80 to 98%) treatment shown below, 10 consecutive times. Let sit for 24±2h at room condition, then measure.  ■ Pretreatment Perform the heat treatment at 150+0/-10℃ for 60±5 min and then let sit for 24±2h at room condition.
		ΔC/C	C0G: Within ±5% or ±0.5pF (Whichever is larger) X7R: within ±12.5%	
		DF	C0G: ≥30pF, Q>200 <30pF, Q>100+10C/3 X7R: 0.05 max.	
		IR	More than 10% initial specified value.	
5	Biased Humidity	Appearance	No defects or abnormalities.	Apply the rated voltage and DC1.3+0.2/-0V (add 100kΩ resistor) at 85±3℃ and 80 to 85% humidity for 1000±12h. Remove and let sit for 24±2 h at *room condition, then measure. The charge/discharge current is less than 50mA. Pretreatment Perform the heat treatment at 150+0/-10℃ for 60±5 min and then let sit for 24±2 h at *room condition.
		ΔC/C	C0G: Within ±5% or ±0.5pF (Whichever is larger) X7R: within ±12.5%	
		DF	C0G: ≥30pF, Q>200 <30pF, Q>100+10C/3 X7R: 0.05 max.	
		IR	More than 10% initial specified value.	

<table>
<tr><th>No</th><th colspan="2">Test Item</th><th>Specification</th><th>Test Method</th></tr>
<tr><td rowspan="4">6</td><td rowspan="4">Operational Life</td><td>Appearance</td><td>No defects or abnormalities.</td><td rowspan="4">Apply voltage in Table for 1000±12h at 125±3℃. Let sit for 24±2h at room condition, then measure. The charge/discharge current is less than 50mA.
■ Pretreatment
Apply test voltage for 60±5 min at test temperature. Remove and let sit for 24±2h at room condition.<table><tr><th>Rated voltage</th><th>Test voltage</th></tr><tr><td>DC50V/DC100V</td><td>200% of the rated voltage</td></tr><tr><td>DC250V</td><td>150% of the rated voltage</td></tr><tr><td>DC630V</td><td>120% of the rated voltage</td></tr><tr><td>DC1000V</td><td>110% of the rated voltage</td></tr></table></td></tr>
<tr><td>ΔC/C</td><td>C0G: Within ±3% or ±0.3pF
(Whichever is larger)
X7R: within ±12.5%</td></tr>
<tr><td>DF</td><td>C0G: ≥30pF, Q＞350
<30pF, Q＞275+5C/2
X7R: 0.04 max.</td></tr>
<tr><td>IR</td><td>More than 10% initial specified value.</td></tr>
<tr><td>7</td><td colspan="2">External Visual</td><td>No defects or abnormalities.</td><td>Visual inspection.</td></tr>
<tr><td>8</td><td colspan="2">Physical Dimension</td><td>Within the specified dimensions.</td><td>Using calipers and micrometers.</td></tr>
<tr><td>9</td><td colspan="2">Marking</td><td>To be easily legible.</td><td>Visual inspection.</td></tr>
<tr><td rowspan="4">10</td><td rowspan="4">Resistance to Solvents</td><td>Appearance</td><td>No defects or abnormalities.</td><td rowspan="4">Per MIL-STD-202 Method 215
Solvent 1 : 1 part (by volume) of isopropyl alcohol
3 parts (by volume) of mineral spirits
Solvent 2 : Terpene defluxer
Solvent 3 : 42 parts (by volume) of water
1 part (by volume) of propylene glycol monomethyl ether
1 part (by volume) of monoethanolamine</td></tr>
<tr><td>Capacitance</td><td>Within the specified tolerance.</td></tr>
<tr><td>DF</td><td>C0G: ≥30pF, Q＞1000
<30pF, Q＞400+20C
X7R: 0.025 max.</td></tr>
<tr><td>IR</td><td>More than 10,000MΩ or 500MΩμF
(Whichever is smaller)</td></tr>
<tr><td rowspan="3">11</td><td rowspan="3">Mechanical Shock</td><td>Appearance</td><td>No defects or abnormalities.</td><td rowspan="3">Three shocks in each direction should be applied along 3 mutually perpendicular axes of the test specimen (18 shocks).
The specified test pulse should be Half-sine and should have a duration 0.5ms, peak value 1500G and velocity change 4.7m/s.</td></tr>
<tr><td>Capacitance</td><td>Within the specified tolerance.</td></tr>
<tr><td>DF</td><td>C0G: ≥30pF, Q＞1000
<30pF, Q＞400+20C
X7R: 0.025 max.</td></tr>
<tr><td rowspan="3">12</td><td rowspan="3">Vibration</td><td>Appearance</td><td>No defects or abnormalities.</td><td rowspan="3">The capacitor should be subjected to a simple harmonic motion having total amplitude of 1.5mm, the frequency being varied uniformly between the approximate limits of 10 and 2,000Hz. The frequency range, from 10 to 2000Hz and return to 10Hz, should be traversed in approximately 20 min.
This motion should be applied for 12 items in each 3 mutually perpendicular directions (total of 36 times).</td></tr>
<tr><td>Capacitance</td><td>Within the specified tolerance.</td></tr>
<tr><td>DF</td><td>C0G: ≥30pF, Q＞1000
<30pF, Q＞400+20C
X7R: 0.025 max.</td></tr>
<tr><td rowspan="3">13-1</td><td rowspan="3">Resistance to Soldering Heat (Non-Preheat)</td><td>Appearance</td><td>No defects or abnormalities.</td><td rowspan="3">The lead wires should be immersed in the melted solder 1.5 to 2.0mm from the root of terminal at 260±5℃ for 10±1 seconds.
Pre-treatment
Capacitor should be stored at 150+0/-10℃ for 1h, then place at room condition for 24±2h before initial measurement.
■ Post-treatment
Capacitor should be stored for 24±2h at room condition.</td></tr>
<tr><td>ΔC/C</td><td>C0G: Within ±2.5% or ±0.25pF
(Whichever is larger)
X7R: within ±7.5%</td></tr>
<tr><td>TV
(Lead to lead)</td><td>No defects</td></tr>
<tr><td rowspan="3">13-2</td><td rowspan="3">Resistance to Soldering Heat (On-Preheat)</td><td>Appearance</td><td>No defects or abnormalities.</td><td rowspan="3">First the capacitor should be stored at 120+0/-5℃ for 60+0/-5 seconds. Then, the lead wires should be immersed in the melted solder 1.5 to 2.0mm from the root of terminal at 260±5℃ for 7.5+0/-1 seconds.
■ Pre-treatment
Capacitor should be stored at 150+0/-10℃ for 1h, then place at room condition for 24±2h before initial measurement.
■ Post-treatment
Capacitor should be stored for 24±2h at room condition.</td></tr>
<tr><td>ΔC/C</td><td>C0G: Within ±2.5% or ±0.25pF
(Whichever is larger)
X7R: within ±7.5%</td></tr>
<tr><td>TV
(Lead to lead)</td><td>No defects</td></tr>
</table>

No	Test Item		Specification	Test Method
13-3	Resistance to Soldering Heat (soldering iron method)	Appearance	No defects or abnormalities.	Temperature of iron-tip : 350±10℃ Soldering time: 3.5±0.5 seconds Soldering position Straight Lead: 1.5 to 2.0mm from the root of terminal Crimp Lead: 1.5 to 2.0mm from the end of lead bend ■ Pre-treatment Capacitor should be stored at 150+0/-10℃ for 1h, then place at room condition for 24±2h before initial measurement. ■ Post-treatment Capacitor should be stored for 24±2h at room condition.
		ΔC/C	C0G: Within ±2.5% or ±0.25pF (Whichever is larger) X7R: within ±7.5%	
		TV (Lead to lead)	No defects or abnormalities	
14	Thermal Shock	Appearance	No defects or abnormalities.	Perform the 300 cycles according to the two heat treatments listed in the following table (Maximum transfer time is 20s.). Let sit for 24±2h at room condition, then measure. Step / 1 / 2 Temp. (℃) / -55+3/-0 / 125+3/-0 Time (min.) / 15±3 / 15±3 ■ Pretreatment Perform the heat treatment at 150+0/-10℃ for 60±5 min and then let sit for 24±2h at room condition.
		ΔC/C	C0G: Within ±5% or ±0.5pF (Whichever is larger) X7R: within ±12.5%	
		DF	C0G: ≥30pF, Q>350 <30pF, Q>275+5C/2 X7R: 0.05 max.	
		IR	More than 10% initial specified value.	
15	ESD	Appearance	No defects or abnormalities.	Per AEC-Q200-002
		Capacitance	Within the specified tolerance	
		DF	C0G: ≥30pF, Q>1000 <30pF, Q>400+20C X7R: 0.025 max.	
		IR	More than 10,000MΩ or 100MΩμF (Whichever is smaller)	
16	Solderability		Lead wire should be soldered with uniform coating on the axial direction over 95% of the circumferential direction.	Should be placed into steam aging for 8h±15 min. The terminal of capacitor is dipped into a solution of ethanol and rosin (25% rosin in weight proportion). Immerse in solder solution for 2±0.5 seconds. In both cases the depth of dipping is up to about 1.5 to 2mm from the terminal body. Temp. of solder : 245±5℃ Lead Free Solder (Sn-3.0Ag-0.5Cu) 235±5℃ H60A or H63A Eutectic Solder
17	Electrical Characterization	Appearance	No defects or abnormalities.	Visual inspection.
		Capacitance	Within the specified tolerance	The capacitance/DF should be measured at 25℃ at the frequency and voltage shown in the table. Frequency / Voltage C0G: ≤1000pF, 1±0.1MHz; >1000pF, 1±0.1kHz / 1±0.2Vrms X7R: 1±0.1kHz / 1±0.2Vrms
		DF	C0G: ≥30pF, Q>1000 <30pF, Q>400+20C X7R: 0.025 max.	
		IR	More than 10,000MΩ or 100MΩμF (Whichever is smaller)	The insulation resistance should be measured with rated voltage or DC500V (Whichever is smaller) at 25℃ within 2 min. of charging.
		TV (Lead to lead)	No defects or abnormalities	The capacitor should not be damaged when voltage in Table is applied between the terminations for 1 to 5 seconds. (Charge/Discharge current ≤50mA.) Rated voltage / Test voltage DC50V/ DC100V / 250% of the rated voltage DC250V / 200% of the rated voltage DC630V / 150% of the rated voltage DC1000V / 120% of the rated voltage
		TV (Body Insulation)	No defects or abnormalities	The capacitor is placed in a container with metal balls of 1mm diameter so that each terminal, short-circuit is kept approximately 2mm from the balls, and 200% of the rated DC voltage (DC1300V in case of rated voltage: DC630V, DC1000V) is impressed for 1 to 5 seconds between capacitor terminals and metal balls.

No	Test Item		Specification	Test Method
18	Terminal Strength	Tensile Strength	Termination not to be broken or loosened.	As in the figure, fix the capacitor body, apply the force gradually to each lead in the radial direction of the capacitor until reaching 10N and then keep the force applied for 10±1 seconds.
		Bending Strength	Termination not to be broken or loosened.	Each lead wire should be subjected to a force of 2.5N and then be bent 90° at the point of egress in one direction. Each wire is then returned to the original position and bent 90° in the opposite direction at the rate of one bend per 2 to 3 seconds.
19	Capacitance Temperature Characteristics		C0G: 25～125℃: 0±30ppm/℃ -55～25℃: 0+30/-72ppm/℃ X7R: Within ±15%	The ΔC/C should be measured after 5min. at each specified temperature step. Step 1: 25℃ (±2℃) Step 2: -55℃ (±2℃) Step 3: 25℃ (±2℃) Step 4: 125℃ (±2℃) Step 5: 25℃ (±2℃) C0G The temperature coefficient is determined using the capacitance measured in step 3 as a reference. When cycling the temperature sequentially from step 1 through 5 (-55°C to 125°C) the capacitance should be within the specified tolerance for the temperature coefficient and capacitance change as table. The capacitance drift is calculated by dividing the differences between the maximum and minimum measured values in the step 1, 3 and 5 by the capacitance value in step 3. X7R The ranges of ΔC/C compared with the above 25℃ value over the temperature ranges shown in the table should be within the specified ranges. ■ Pretreatment Perform the heat treatment at 150+0/-10℃ for 60±5 min and then let sit for 24±2h at room condition. Perform the initial measurement.

6. PACKING AND STORAGE

6.1. STORAGE ENVIRONMENT

The insulating coating of capacitors does not form a perfect seal; therefore, do not use or store capacitors in a corrosive atmosphere, especially where chloride gas, sulfide gas, acid, alkali, salt or the like are present. And avoid exposure to moisture. Before cleaning, bonding, or molding this product, verify that these processes do not affect product quality by testing the performance of a cleaned, bonded or molded product in the intended equipment.

Store the capacitors where the temperature and relative humidity do not exceed 5～40℃ and 20～70%.

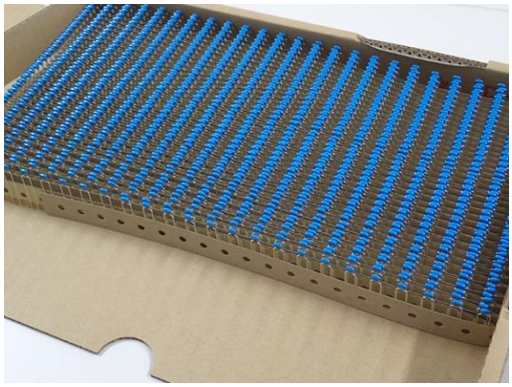
Use capacitors within 6 months. For more than 6 months, confirm the solderability and capacitance before use.

6.2. MINIMUM PACKAGE QUANTITY

- Bulk type

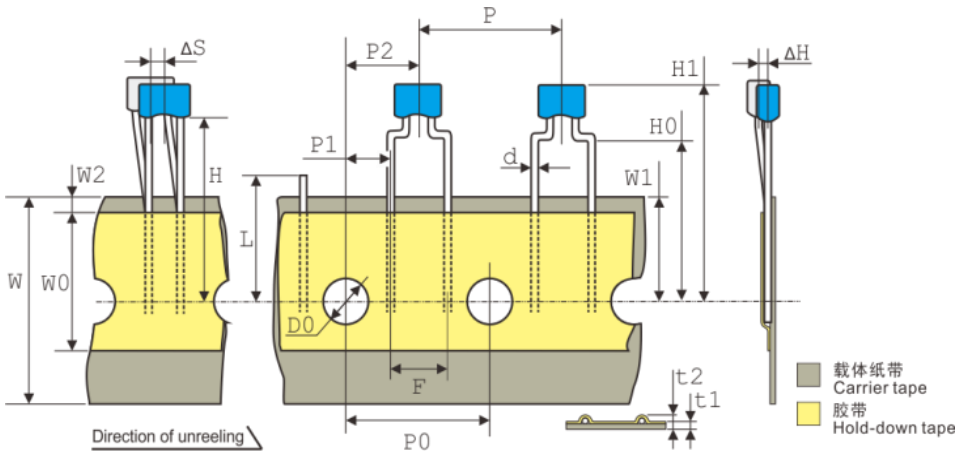
Minimum package quantity: 1000pcs/bag

- Taping



Minimum package quantity: 1000pcs/box

6.3. TAPING SPECIFICATIONS



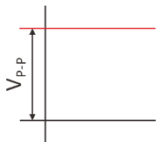
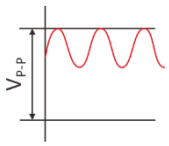
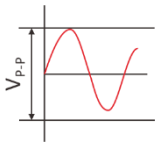
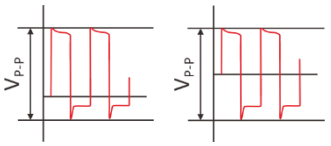
Item		Symbol	Specification (mm)	Remarks
Lead-wire diameter		d	0.47±0.05	
Pitch of component		P	12.7±1.0	
Feed hole pitch		P0	12.7±0.3	Cumulative pitch error: 1.0mm/20 pitch
Feed hole center to lead		P1	5.10±0.7 3.85±0.7	
Hole center to component center		P2	6.35±1.3	
Lead-to-lead distance		F	2.54±0.8 5.08±0.8	
Component alignment		Δh	≤2.0	
Deviation along tape, Left or right		ΔS	≤1.3	
Tape width		W	18.0+1.0/-0.5	
Hold-down tape width		W0	≥7.0	
Hole position		W1	9.0+0.75/-0.5	
Hole-down tape position		W2	≤3.0	
Height of component from tape center	Straight lead	H	18.0+2/-0	
	Kinked lead	H0	16.0±0.5	
Component height		H1	≤32.25	
Feed hole diameter		D0	4.0±0.3	
Total tape thickness		t1	≤0.9	Ground paper: 0.5±0.1mm
Total thickness, tape and lead wire		t2	≤1.5	
Length of snipped		L	≤11.0	

7. CAUTION

7.1. OPERATING VOLTAGE

When DC-rated capacitors are to be used in AC or ripple current circuits, be sure to maintain the Vp-p value of the applied voltage or the Vo-p which contains DC bias within the rated voltage range. When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use a capacitor within rated voltage containing this irregular voltage.

When DC-rated capacitors are to be used in input circuits from commercial power source (AC filter), be sure to use Safety Recognized Capacitors because various regulations on withstand voltage or impulse withstand established for each equipment should be taken into considerations.

VOLTAGE	DC VOLTAGE	DC+AC VOLTAGE	AC VOLTAGE	PULSE VOLTAGE
POSITIONAL MEASUREMENT				

7.2. OPERATING TEMPERATURE AND SELF-GENERATED HEAT

Keep the surface temperature of a capacitor below the upper limit of its rated operating temperature range.
Be sure to take into account the heat generated by the capacitor itself.
When the capacitor is used in a high-frequency current, pulse current or the like, it may have the self-generated heat due to dielectric-loss. In case of Class 2 capacitors (Temp. Char. : X7R), applied voltage should be the load such as self-generated heat is within 20℃ on the condition of atmosphere temperature 25℃. Please contact us if self-generated heat is occurred with Class 1 capacitors (Temp. Char. : C0G). When measuring, use a thermocouple of small thermal capacity-K of Ø0.1mm and be in the condition where capacitor is not affected by radiant heat of other components and wind of surroundings. Excessive heat may lead to deterioration of the capacitor's characteristics and reliability.

7.3. FAIL-SAFE

Be sure to provide an appropriate fail-safe function on your product to prevent a second damage that may be caused by the abnormal function or the failure of our product.

7.4. VIBRATION AND IMPACT

Do not expose a capacitor or its leads to excessive shock or vibration during use.

7.5. SOLDERING

When soldering this product to a PCB/PWB, do not exceed the solder heat resistance specification of the capacitor. Subjecting this product to excessive heating could melt the internal junction solder and may result in thermal shocks that can crack the ceramic element.

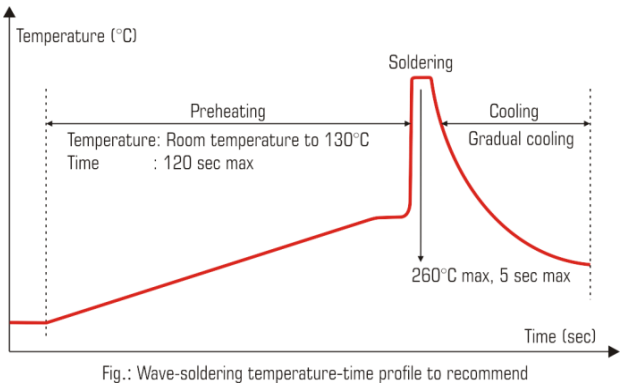


Fig.: Wave-soldering temperature-time profile to recommend

When soldering capacitor with a soldering iron, it should be performed in the following conditions.
Temperature of iron-tip: 350℃ Max.
Soldering iron wattage: 40W max.
Soldering time: 3.0s Max.

7.6. BONDING AND RESIN MOLDING, RESIN COAT

In case of bonding, molding or coating this product, verify that these processes do not affect the quality of capacitor by testing the performance of a bonded or molded product in the intended equipment.
In case of the amount of applications, dryness / hardening conditions of adhesives and molding resins containing

organic solvents (ethyl acetate, methyl ethyl ketone, toluene, etc.) are unsuitable, the outer coating resin of a capacitor is damaged by the organic solvents and it may result, worst case, in a short circuit.

The variation in thickness of adhesive or molding resin may cause a outer coating resin cracking and/or ceramic element cracking of a capacitor in a temperature cycling.

7.7. TREATMENT AFTER BONDING AND RESIN MOLDING, RESIN COAT

When the outer coating is hot (over 100℃) after soldering, it becomes soft and fragile.

So please be careful not to give it mechanical stress.

Failure to follow the above cautions may result, worst case, in a short circuit and cause fuming or partial dispersion when the product is used.

7.8. LIMITATION OF APPLICATIONS

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects which might directly cause damage to the third party's life, body or property.

- Aircraft equipment
- Aerospace equipment
- Undersea equipment
- Power plant control equipment
- Medical equipment
- Transportation equipment (vehicles, trains, ships, etc.)
- Traffic signal equipment
- Disaster prevention / crime prevention equipment
- Data-processing equipment exerting influence on public
- Application of similar complexity and/or reliability requirements to the applications listed in the above.

8. NOTICE

8.1. CLEANING (ULTRASONIC CLEANING)

To perform ultrasonic cleaning, observe the following conditions.

Rinse bath capacity : Output of 20 watts per liter or less.

Rinsing time : 5 min maximum.

Do not vibrate the PCB/PWB directly.

Excessive ultrasonic cleaning may lead to fatigue destruction of the lead wires.

8.2. SOLDERING AND MOUNTING

Insertion of the Lead Wire

- When soldering, insert the lead wire into the PCB without mechanically stressing the lead wire.
- Insert the lead wire into the PCB with a distance appropriate to the lead space.

8.3. CAPACITANCE CHANGE OF CAPACITORS

- Class 2 capacitors (Temp. Char. : X7R)

  Class 2 capacitors an aging characteristic, whereby the capacitor continually decreases its capacitance slightly if the capacitor leaves for a long time. Moreover, capacitance might change greatly depending on a surrounding temperature or an applied voltage. So, it is not likely to be able to use for the time constant circuit.

  Please contact us if you need a detail information.

9. NOTE

1) Please make sure that your product has been evaluated in view of your specifications with our product being mounted to your product.
2) You are requested not to use our product deviating from this specification.

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