USB3.0-IPHSMC demo board[AB08-USB3HSMC] Manual [Ver1.2E]

Introduction

Thank you for choosing USB3.0-IP HSMC demo board [Part Number：AB08-USB3HSMC] (“demo board” in this manual).

The demo board will connect with Altera Evaluation board that furnishes HSMC (High Speed Mezzanine Card) extention connector, so that user can evaluate USB3.0-IP from DesignGateway. The demo board can be applicable to both USB3.0 Device-IP (Product number: USB3D-IPxxx) evaluation and Host-IP (Product number: USB3H-IPxxx) evaluation. **Take enough care that HSMC interface voltage is fixed to 2.5V so that user shall never use any Altera board that cannot set HSMC I/O voltage to 2.5V. Otherwise, Altera board will be damaged!** User can try USB3.0 SuperSpeed real board operation by using Altera FPGA board with this demo board and sof-file for evaluation provided from DesignGateway.

The demo board mainly mounts following parts.

- TUSB1310A (USB3.0 PHY device from T.I) and related power supply circuit.
- A-type USB3.0 connector
- HSMC connector (Samtec: QTH-909-01-L-D-A)

The 1meter-length USB3.0 AtoA cable is attached with the demo board product. USB3.0 Device-IP core (Product Name: USB3D-IPxxx) evaluation needs to use this USB3.0 cable. Note that USB3.0 AtoB cable is not attached with the product, so that user needs to arrange USB3.0 AtoB cable to evaluate USB3.0 Host-IP core (Product Name: USB3H-IPxxx).

Note that the demo board only supports SuperSpeed (5Gbps) communication and does not support any legacy USB speed. (There is no DM/DP signal connection resource for USB2.0 or earlier standard) because the demo board is dedicated to USB3.0-IP from DesignGateway only.

Package List

The demo board includes following items in its product.

- USB3HSMC board: 1pcs
- USB3.0 AtoA cable: 1pcs.（AtoA cable is for Device-IP core evaluation）

Board Outline

The demo board size is 78mm width and 54mm length.
Following figure-1 shows board outline.

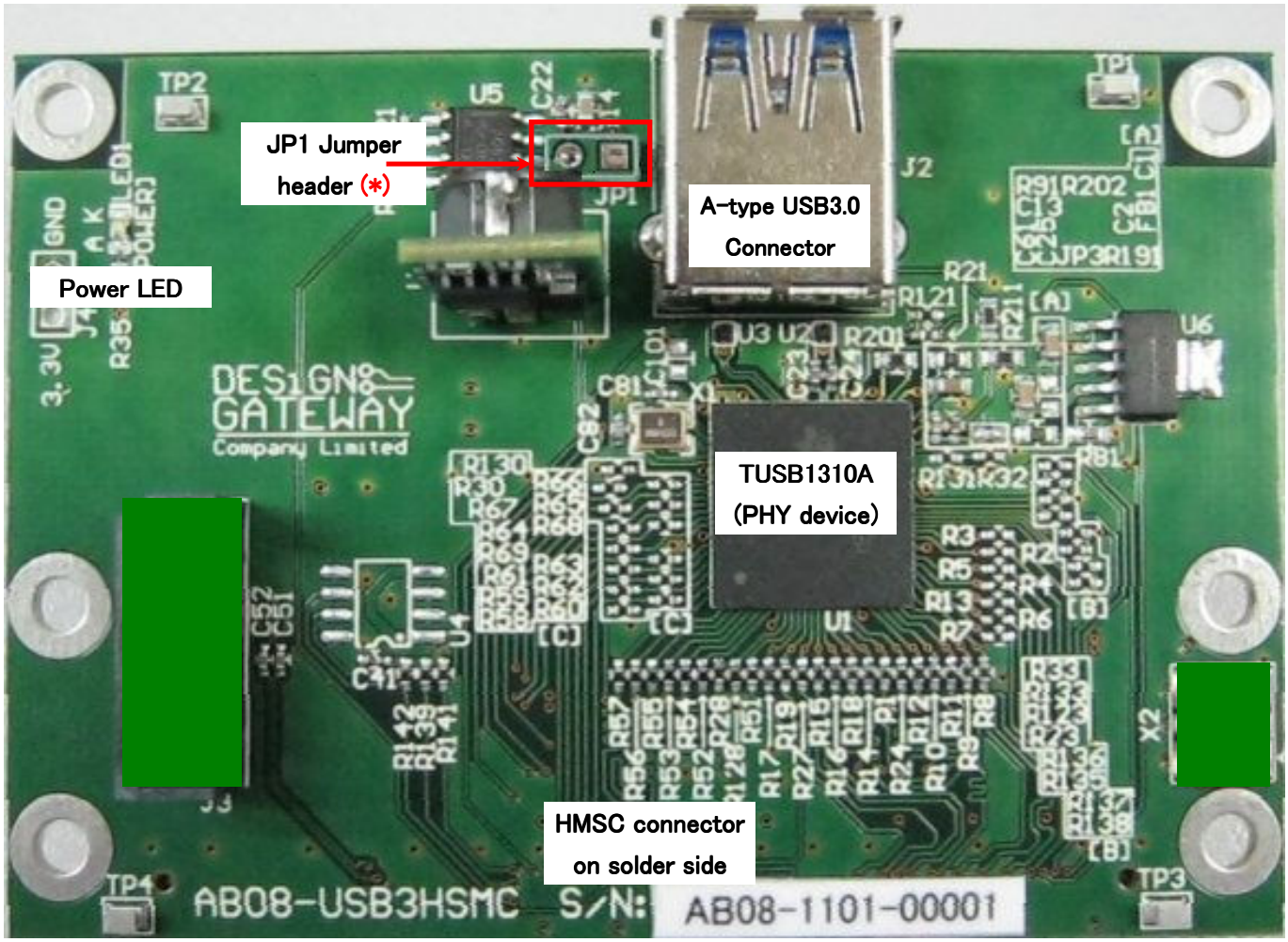

Figure-1: AB08-USB3HSMC board outline

Note(*): JP1 Jumper header is to set short or open between 5V power supply from USB (VUSB) and on-board 5V power supply output.

When evaluate Device-IP, do not set Jumper Socket on JP1.

When evaluate Host-IP, set Jumper Socket on JP1.

Pin Assignment

Pin assignment between FPGA I/O pin and TUSB1310 is listed following table-1 when the demo board is connected to 'HSMA' channel.

HSMC Pin#	Samtec Pin#	HSMC signal definition	PHY (TUSB1310A) connection	Stratix4GX Pin#	ArriaIIGX Pin#	Cyclone4GX Pin#	Remark
41	61	D0	IPL_DC0	AW10	L1	AC27	Not used
42	62	D1	RX_STATUS2	AV10	R6	Y27	
43	63	D2	IPL_DD0	AW7	K1	AF30	Not used
44	64	D3	RX_POLARITY	AV7	M1	A25	
47	67	TX_D_P0	RX_DATA11	AN9	AA10	C29	
48	68	RX_D_P0	RX_DATA14	AT9	AC5	D29	
49	69	TX_D_N0	PWRPRESENT	AP9	AA9	C30	
50	70	RX_D_N0	RX_DATAK0	AU9	AC4	D30	
53	73	TX_D_P1	RX_DATA9	AN7	Y11	E27	
54	74	RX_D_P1	RX_DATA15	AT8	AE4	G26	
55	75	TX_D_N1	USB_OVCR	AP7	Y10	E28	Not used
56	76	RX_D_N1	RX_DATAK1	AU8	AF4	G27	
59	79	TX_D_P2	RX_DATA10	AE13	AH2	F26	
60	80	RX_D_P2	RX_DATA13	AP8	AF1	N24	
61	81	TX_D_N2	USB_PWEN	AE12	AH1	F27	Not used
62	82	RX_D_N2		AR8	AG1	M25	
65	85	TX_D_P3	RX_DATA7	AL8	AB10	F30	
66	86	RX_D_P3	RX_DATA12	AW6	AE2	N25	
67	87	TX_D_N3		AM8	AB9	E30	
68	88	RX_D_N3		AW5	AE1	M26	
71	91	TX_D_P4	RX_DATA8	AK9	Y8	F28	
72	92	RX_D_P4	RX_DATA6	AV5	AC1	R24	
73	93	TX_D_N4		AL9	Y7	F29	
74	94	RX_D_N4		AW4	AD1	P25	
77	97	TX_D_P5	RX_DATA5	AK8	AF3	H30	
78	98	RX_D_P5	RX_DATA4	AT7	AB2	N27	
79	99	TX_D_N5	PHY_STATUS	AK7	AF2	G30	
80	100	RX_D_N5		AU7	AB1	N28	
83	103	TX_D_P6	RX_DATA3	AH10	AD4	G28	
84	104	RX_D_P6	RX_DATA1	AT6	Y1	M29	
85	105	TX_D_N6	PHY_STATUS	AJ10	AE3	G29	
86	106	RX_D_N6	RX_STATUS1	AU6	AA1	M30	
89	109	TX_D_P7	RX_DATA2	AH9	V4	J29	
90	110	RX_D_P7	RX_DATA0	AR5	Y2	N29	
91	111	TX_D_N7	RX_VALID	AH8	V3	J30	
92	112	RX_D_N7		AT5	W1	N30	
95	115	CLK_OUT_P1	TX_CLK	AL10	AD7	P21	
96	116	CLK_IN_P1	PCLK	AC6	U6	T29	
97	117	CLK_OUT_N1		AM10	AD6	N21	
98	118	CLK_IN_N1		AC5	U5	T30	

Table-1: Pin connection list

(Notes: 'HSMC Pin#' means pin number defined in the HSMC standard, while 'Samtec Pin#' means pin number of QTH-090-01-L-D-A connector specification)

HSMC Pin#	Samtec Pin#	HSMC signal definition	PHY (TUSB1310A) connection	Stratix4GX Pin#	ArriaIIGX Pin#	Cyclone4 GX Pin#	Remark
101	121	TX_D_P8	TX_DATA15	AG8	AA7	L30	
102	122	RX_D_P8	TX_DATA14	AP6	V2	P27	
103	123	TX_D_N8	RX_STATUS0	AG7	Y6	K30	
104	124	RX_D_N8	RX_TERM	AP5	V1	P28	
107	127	TX_D_P9	TX_DATAK1	AG10	W7	J28	
108	128	RX_D_P9	TX_DATAK0	AN6	W4	R30	
109	129	TX_D_N9	POWER_DOWN1	AG9	W6	H28	
110	130	RX_D_N9	TX_ELECIDLE	AN5	W3	P30	
113	133	TX_D_P10	TX_DATA13	AF11	Y5	J27	
114	134	RX_D_P10	TX_DATA12	AM6	U2	R27	
115	135	TX_D_N10		AF10	AA4	H27	
116	136	RX_D_N10	RX_ELECIDLE	AM5	U1	R28	
119	139	TX_D_P11	TX_DATA8	AD10	AC3	L27	
120	140	RX_D_P11	TX_DATA10	AL6	Y4	T28	
121	141	TX_D_N11		AD9	AC2	L28	
122	142	RX_D_N11	POWER_DOWN0	AL5	Y3	R29	
125	145	TX_D_P12	TX_DATA9	AE11	W10	M27	
126	146	RX_D_P12	TX_DATA11	AK6	AB4	R25	
127	147	TX_D_N12		AE10	Y9	M28	
128	148	RX_D_N12	PHY_RESETN	AK5	AB3	R26	
131	151	TX_D_P13	TX_DATA7	AD13	R7	K26	
132	152	RX_D_P13	TX_DATA2	AJ6	AB6	T26	
133	153	TX_D_N13		AD12	T7	K27	
134	154	RX_D_N13	OUT_ENABLE	AJ5	AB5	T27	
137	157	TX_D_P14	TX_DATA6	AB13	R2	K25	
138	158	RX_D_P14	TX_DATA3	AH6	U7	U25	
139	159	TX_D_N14		AB12	P1	J26	
140	160	RX_D_N14	TX_DEEMPH1	AH5	V7	T25	
143	163	TX_D_P15	TX_DATA5	AB11	V11	J25	
144	164	RX_D_P15	TX_DATA0	AG6	AB8	T23	
145	165	TX_D_N15	RESETN	AB10	V10	H25	
146	166	RX_D_N15	TXDET_RXLPBK	AG5	AB7	T24	
149	169	TX_D_P16	TX_DATA4	AC11	U11	M21	
150	170	RX_D_P16	TX_DATA1	AB9	AC7	U21	
151	171	TX_D_N16	TX_DEEMPH0	AC10	U10	M22	
152	172	RX_D_N16	TX_MARGIN0	AC8	AC6	T21	

Table-1: Pin connection list (cont'd)

(Notes: 'HSMC Pin#' means pin number defined in the HSMC standard, while 'Samtec Pin#' means pin number of QTH-090-01-L-D-A connector specification)

Disclaimer

The manufacturer of the product limits liability in fillowing situation or use.

- Any damage to the connected Host-PC via USB interface.
- Any damage to the FPGA evaluation board, especially, when user mistakenly connect HSMC with non-2.5V interface).
- Any misoperation in Device-IP evaluation when attached USB3.0 AtoA cable is not used.
- Any misoperation in Host-IP evaluation when USB3.0 cable is not USB3.0 standard compliant.
- DesignGateway does not guarantee transfer speed performance.
- DesignGateway is exempted from any misoperation under user's original environment.

[Inquiry]
URL : http://www.design-gateway.com
Email : info@design-gateway.com

Revision History

Revision	Date	Description
1.1E	11-Jul-2012	Initial English manual
1.2E	23-Mar-2015	Remove SATA description

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Sockets & Adapters ***category:***

Click to view products by Design Gateway ***manufacturer:***

Other Similar products are found below :

6508-0-00-01-00-00-33-0 AC164348 1262 22827 AC164353 TDGL015 SA247 SM64TQ-ACTEL-1 70-0036 8.06.03 DS91230+ SMPA-ISP-ACTEL-3-KIT 16017 LFVDBGF KIT 70601-3 SM132CQ-ACTEL R0E000010ACB20 IPC0181 IPC0175 IPC0165 AC164397 conga-Thin MITX/eDP to DP Adapter SLG46536V-SKT SLG46621V-SKT SLG46538V-SKT SLG46535V-SKT SLG46722V-SKT ML-ADP-EVN TOOLSTICK990MPP 110-83-320-41-605101 110-83-632-41-605101 110-83-640-41-605101 110-83-628-41-605101 116-83-306-41-001101 PA0003 PA0007 PA0009 PA0035 PA0085 PA0096 IPC0079 ATARD-DBGADPT 80-000286 ATSTK600-RC88 ATSTK600-SC06 ATSTK600-RC78 SPC560PADPT64S AC164345 AC164342 AC164038