

Features

- Single 1.7V - 2.0V Supply
- Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI) Compatible
 - Supports SPI Modes 0 and 3
 - Supports Dual Output Read and Quad I/O Program and Read
 - Supports QPI Program and Read
 - 133 MHz Maximum Operating Frequency
 - Clock-to-Output (t_{V1}) of 6 ns
 - Up to 66 MB/s Continuous Data Transfer Rate
- Full Chip Erase
- Flexible, Optimized Erase Architecture for Code and Data Storage Applications
 - 0.6 ms Typical Page Program (256 Bytes) Time
 - 60 ms Typical 4-Kbyte Block Erase Time
 - 200 ms Typical 32-Kbyte Block Erase Time
 - 350 ms Typical 64-Kbyte Block Erase Time
- Hardware Controlled Locking of Status Registers via \overline{WP} Pin
- 4 Kbit secured One-Time Programmable Security Register
- Hardware Write Protection
- Serial Flash Discoverable Parameters (SFDP) Register
- Flexible Programming
 - Byte/Page Program (1 to 256 Bytes)
 - Dual or Quad Input Byte/Page Program (1 to 256 Bytes)
- Erase/Program Suspend and Resume
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
 - 2 μ A Deep Power-Down Current (Typical)
 - 10 μ A Standby current (Typical)
 - 5 mA Active Read Current (Typical)
- Endurance: 100,000 program/erase cycles (4KB, 32KB or 64KB blocks)
- Data Retention: 20 Years
- Industrial Temperature Range: -40°C to +85°C
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
 - 8-lead SOIC (208-mil)
 - 8-pad DFN (6 x 5 x 0.6 mm)
 - 8-ball WLCSP (dBGAs)
 - Die in Wafer Form

1. Introduction

The Adesto® AT25SL641 is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25SL641 is ideal for data storage as well, eliminating the need for additional data storage devices.

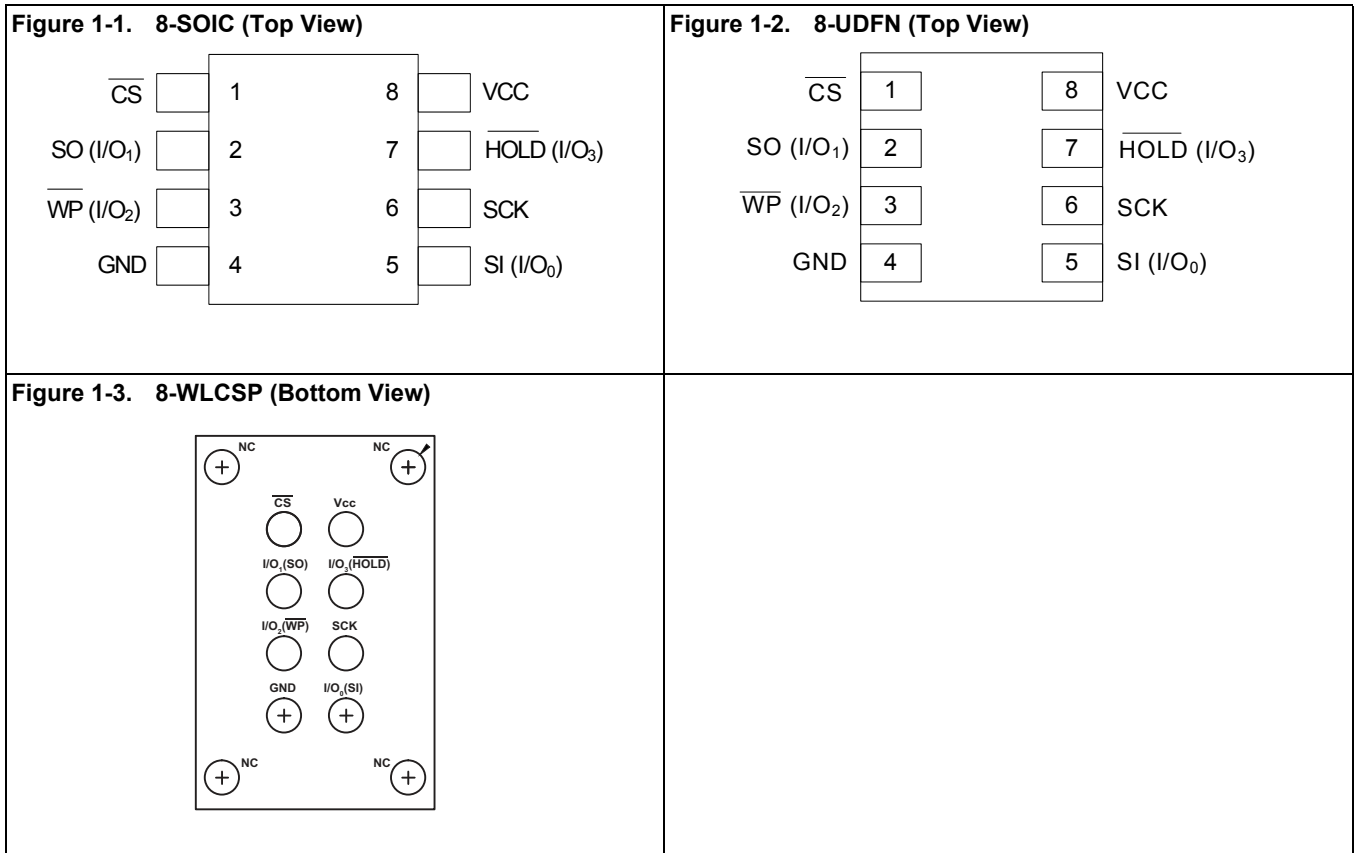
The erase block sizes of the AT25SL641 have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

SPI clock frequencies of up to 133 MHz are supported allowing equivalent clock rates of 266 MHz for Dual Output and 532 MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O instructions. The AT25SL641 array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased 4KB Block, 32KB Block, 64KB Block or the entire chip.

The devices operate on a single 1.7V to 1.95V power supply with current consumption as low as 5 mA active and 2 μ A for Deep Power Down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with a 4 Kbit Secured OTP.

2. Pinouts and Pin Descriptions

The following figures show the available package types.



During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC} (min) to V_{CC} (max).

All of the input and output signals must be held high or low (according to voltages of V_{IH} , V_{OH} , V_{IL} or V_{OL}).

Table 1-1. Pin Descriptions

| Symbol | Name and Function | Asserted State | Type |
|-------------------------------------|---|----------------|--------------|
| \overline{CS} | <p>CHIP SELECT</p> <p>When this input signal is high, the device is deselected and serial data output pins are at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device will be in the standby power mode (this is not the deep power down mode). Driving Chip Select (\overline{CS}) low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select (\overline{CS}) is required prior to the start of any instruction.</p> | Low | Input |
| SCK | <p>SERIAL CLOCK</p> <p>This input signal provides the timing for the serial interface. Instructions, addresses, or data present at serial data input are latched on the rising edge of Serial Clock (SCK). Data are shifted out on the falling edge of the Serial Clock (SCK).</p> | - | Input |
| SI (I/O ₀) | <p>SERIAL INPUT</p> <p>The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK.</p> <p>With the Dual-Output and Quad-Output Read commands, the SI Pin becomes an output pin (I/O₀) in conjunction with other pins to allow two or four bits of data on (I/O₃₋₀) to be clocked in on every falling edge of SCK</p> <p>To maintain consistency with the SPI nomenclature, the SI (I/O₀) pin is referenced as the SI pin unless specifically addressing the Dual-I/O and Quad-I/O modes in which case it is referenced as I/O₀.</p> <p>Data present on the SI pin is ignored whenever the device is deselected (\overline{CS} is deasserted).</p> | - | Input/Output |
| SO (I/O ₁) | <p>SERIAL OUTPUT</p> <p>The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK.</p> <p>With the Dual-Output Read commands, the SO Pin remains an output pin (I/O₀) in conjunction with other pins to allow two bits of data on (I/O₁₋₀) to be clocked in on every falling edge of SCK</p> <p>To maintain consistency with the SPI nomenclature, the SO (I/O₁) pin is referenced as the SO pin unless specifically addressing the Dual-I/O modes in which case it is referenced as I/O₁. The SO pin is in a high-impedance state whenever the device is deselected (\overline{CS} is deasserted).</p> | - | Input/Output |
| \overline{WP} (I/O ₂) | <p>WRITE PROTECT</p> <p>The Write Protect (\overline{WP}) pin can be used to protect the Status Register against data modification. Used in company with the Status Register's Block Protect (SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect SRP) bits, a portion or the entire memory array can be hardware protected. The \overline{WP} pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the \overline{WP} pin (Hardware Write Protect) function is not available since this pin is used for IO₂. See figures 1-1, 1-2, and 1-3 for the pin configuration of Quad I/O and QPI operation.</p> | - | Input/Output |

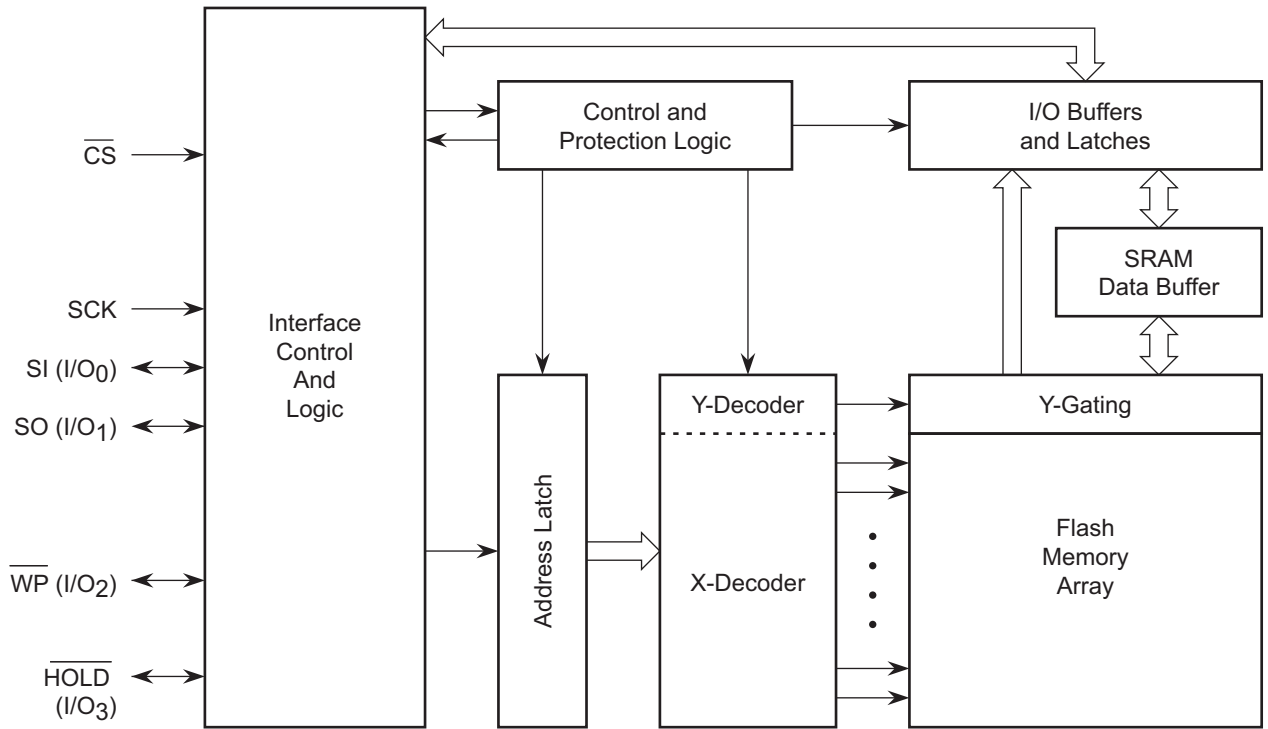
Table 1-1. Pin Descriptions (Continued)

| Symbol | Name and Function | Asserted State | Type |
|---|--|----------------|--------------|
| $\overline{\text{HOLD}}$ (I/O ₃) | <p>HOLD</p> <p>The $\overline{\text{HOLD}}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{\text{HOLD}}$ pin is asserted, transitions on the SCK pin and data on the SI pin are ignored and the SO pin is placed in a high-impedance state.</p> <p>The $\overline{\text{CS}}$ pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle.</p> <p>With the Quad-Input Byte/Page Program command, the $\overline{\text{HOLD}}$ pin becomes an input pin (I/O₃) and with other pins, allows four bits (on I/O₃₋₀) of data to be clocked in on every rising edge of SCK. With the Quad-Output Read commands, the $\overline{\text{HOLD}}$ Pin becomes an output pin (I/O₃) in conjunction with other pins to allow four bits of data on (I/O₃₋₀) to be clocked in on every falling edge of SCK. To maintain consistency with SPI nomenclature, the $\overline{\text{HOLD}}$ (I/O₃) pin is referenced as the $\overline{\text{HOLD}}$ pin unless specifically addressing the Quad-I/O modes in which case it is referenced as I/O₃. The $\overline{\text{HOLD}}$ pin is internally pulled-high and may be left floating if the Hold function is not used. However, it is recommended that the $\overline{\text{HOLD}}$ pin also be externally connected to V_{CC} whenever possible. See figures 1-1, 1-2, and 1-3 for the pin configuration of Quad I/O and QPI operation.</p> | - | Input/Output |
| V _{CC} | <p>DEVICE POWER SUPPLY: V_{CC} is the supply voltage. It is the single voltage used for all device functions including read, program, and erase. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.</p> | - | Power |
| GND | <p>GROUND: V_{SS} is the reference for the V_{CC} supply voltage. The ground reference for the power supply. GND should be connected to the system ground.</p> | - | Power |

2. Block Diagram

Figure 2-1 shows a block diagram of the AT25SL641 serial Flash.

Figure 2-1. AT25SL641 Block Diagram



Note: I/O₃₋₀ pin naming convention is used for Dual-I/O and Quad-I/O commands.

3. Memory Array

To provide the greatest flexibility, the memory array of the AT25SL641 can be erased in four levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. The Memory Architecture Diagram illustrates the breakdown of each erase level.

Figure 3-1. Memory Architecture Diagram

| Block Erase Detail | | | | Page Program Detail | |
|--------------------|------|-----|---------------------|---------------------|--------------------|
| 64KB | 32KB | 4KB | Block Address Range | 1-256 byte | Page Address Range |
| 64KB | 32KB | 4KB | 7FFFFFFh – 7FF000h | 256 bytes | 7FFFFFFh – 7FFF00h |
| | | 4KB | 7FEFFFh – 7FE000h | 256 bytes | 7FFEFFh – 7FFE00h |
| | | 4KB | 7FDFFFh – 7FD000h | 256 bytes | 7FFDFFh – 7FFD00h |
| | | 4KB | 7FCFFFh – 7FC000h | 256 bytes | 7FFCFFh – 7FFC00h |
| | | 4KB | 7FBFFFh – 7FB000h | 256 bytes | 7FFBFFh – 7FFB00h |
| | | 4KB | 7FAFFFh – 7FA000h | 256 bytes | 7FFAFFh – 7FFA00h |
| | | 4KB | 7F9FFFh – 7F9000h | 256 bytes | 7FF9FFh – 7FF900h |
| | | 4KB | 7F8FFFh – 7F8000h | 256 bytes | 7FF8FFh – 7FF800h |
| | 32KB | 4KB | 7F7FFFh – 7F7000h | 256 bytes | 7FF7FFh – 7FF700h |
| | | 4KB | 7F6FFFh – 7F6000h | 256 bytes | 7FF6FFh – 7FF600h |
| | | 4KB | 7F5FFFh – 7F5000h | 256 bytes | 7FF5FFh – 7FF500h |
| | | 4KB | 7F4FFFh – 7F4000h | 256 bytes | 7FF4FFh – 7FF400h |
| | | 4KB | 7F3FFFh – 7F3000h | 256 bytes | 7FF3FFh – 7FF300h |
| | | 4KB | 7F2FFFh – 7F2000h | 256 bytes | 7FF2FFh – 7FF200h |
| | | 4KB | 7F1FFFh – 7F1000h | 256 bytes | 7FF1FFh – 7FF100h |
| | | 4KB | 7F0FFFh – 7F0000h | 256 bytes | 7FF0FFh – 7FF000h |
| 64KB | 32KB | 4KB | 7EFFFFh – 7EF000h | 256 bytes | 7EFFFFh – 7EFE00h |
| | | 4KB | 7EDFFFh – 7ED000h | 256 bytes | 7FEDFFh – 7FED00h |
| | | 4KB | 7ECFFFh – 7EC000h | 256 bytes | 7FECFFh – 7FEC00h |
| | | 4KB | 7EBFFFh – 7EB000h | 256 bytes | 7FEBFFh – 7FEB00h |
| | | 4KB | 7EAFh – 7EA000h | 256 bytes | 7FEAFFh – 7FEA00h |
| | | 4KB | 7E9FFFh – 7E9000h | 256 bytes | 7FE9FFh – 7FE900h |
| | | 4KB | 7E8FFFh – 7E8000h | 256 bytes | 7FE8FFh – 7FE800h |
| | | 4KB | 7E7FFFh – 7E7000h | 256 bytes | 7FE7FFh – 7FE700h |
| | 32KB | 4KB | 7E6FFFh – 7E6000h | 256 bytes | 7FE6FFh – 7FE600h |
| | | 4KB | 7E5FFFh – 7E5000h | 256 bytes | 7FE5FFh – 7FE500h |
| | | 4KB | 7E4FFFh – 7E4000h | 256 bytes | 7FE4FFh – 7FE400h |
| | | 4KB | 7E3FFFh – 7E3000h | 256 bytes | 7FE3FFh – 7FE300h |
| | | 4KB | 7E2FFFh – 7E2000h | 256 bytes | 7FE2FFh – 7FE200h |
| | | 4KB | 7E1FFFh – 7E1000h | 256 bytes | 7FE1FFh – 7FE100h |
| | | 4KB | 7E0FFFh – 7E0000h | 256 bytes | 7FE0FFh – 7FE000h |
| | | ⋮ | ⋮ | ⋮ | ⋮ |
| 64KB | 32KB | 4KB | 00FFFFh – 00F000h | 256 bytes | 0017FFh – 001700h |
| | | 4KB | 00EFFFh – 00E000h | 256 bytes | 0016FFh – 001600h |
| | | 4KB | 00DFFFh – 00D000h | 256 bytes | 0015FFh – 001500h |
| | | 4KB | 00CFFFh – 00C000h | 256 bytes | 0014FFh – 001400h |
| | | 4KB | 00BFFFh – 00B000h | 256 bytes | 0013FFh – 001300h |
| | | 4KB | 00AFFh – 00A000h | 256 bytes | 0012FFh – 001200h |
| | | 4KB | 009FFFh – 009000h | 256 bytes | 0011FFh – 001100h |
| | | 4KB | 008FFFh – 008000h | 256 bytes | 0010FFh – 001000h |
| | 32KB | 4KB | 007FFFh – 007000h | 256 bytes | 000FFFh – 000F00h |
| | | 4KB | 006FFFh – 006000h | 256 bytes | 000EFFh – 000E00h |
| | | 4KB | 005FFFh – 005000h | 256 bytes | 000DFFh – 000D00h |
| | | 4KB | 004FFFh – 004000h | 256 bytes | 000CFFh – 000C00h |
| | | 4KB | 003FFFh – 003000h | 256 bytes | 000BFFh – 000B00h |
| | | 4KB | 002FFFh – 002000h | 256 bytes | 000AFFh – 000A00h |
| | | 4KB | 001FFFh – 001000h | 256 bytes | 0009FFh – 000900h |
| | | 4KB | 000FFFh – 000000h | 256 bytes | 0008FFh – 000800h |

4. Device Operation

4.1 Standard SPI Operation

The AT25SL641 features a serial peripheral interface on four signals: Serial Clock (SCK), Chip Select (\overline{CS}), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI instructions use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of SCK. The SO output pin is used to read data or status from the device on the falling edge of SCK.

SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the SCK signal is normally low on the falling and rising edges of \overline{CS} . For Mode 3 the SCK signal is normally high on the falling and rising edges of \overline{CS} .

4.2 Dual SPI Operation

The AT25SL641 supports Dual SPI operation. This instruction allows data to be transferred to or from the device at two times the rate of the standard SPI. The Dual Read instruction is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions the SI and SO pins become bidirectional I/O pins; IO₀ and IO₁.

4.3 Quad SPI Operation

The AT25SL641 supports Quad SPI operation. This instruction allows data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read instruction offers a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction the SI and SO pins become bidirectional IO₀ and IO₁, and the \overline{WP} and \overline{HOLD} pins become IO₂ and IO₃ respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

4.4 QPI Operation

The AT25SL641 supports Quad Peripheral Interface (QPI) operation when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the Enable QPI (38h) instruction. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the SI and SO pins become bidirectional IO₀ and IO₁, and the \overline{WP} and \overline{HOLD} pins become IO₂ and IO₃ respectively.

The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four I/O pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. The enable QPI (38h) and Disable QPI/Disable QPI 2 (FFh) instructions are used to switch between these two modes. Upon power-up or after software reset using the Reset (99h) instruction, the default state of the device is Standard/Dual/Quad SPI mode.

5. Write Protection

To protect inadvertent writes by the possible noise, several means of protection are applied to the Flash memory.

5.1 Write Protect Features

- While Power-on reset, all operations are disabled and no instruction is recognized.
- An internal time delay of t_{PUW} can protect the data against inadvertent changes while the power supply is outside the operating specification. This includes the Write Enable, Page program, Block Erase, Chip Erase, Write Security Register and the Write Status Register instructions.
- For data changes, Write Enable instruction must be issued to set the Write Enable Latch (WEL) bit to “0”. Power-up, Completion of Write Disable, Write Status Register, Page program, Block Erase and Chip Erase are subjected to this condition.
- Using setting the Status Register protect (SRP) and Block protect (SEC, TB, BP2, BP1, and BP0) bits a portion of memory can be configured as reading only called software protection.
- Write Protect (\overline{WP}) pin can control to change the Status Register under hardware control.
- The Deep Power Down mode provides extra protection from unexpected data changes as all instructions are ignored under this status except for Release Deep Power Down instruction.

6. Status Register

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection and the Quad SPI setting. The Write Status Register instruction can be used to configure the devices writes protection features and Quad SPI setting. Write access to the Status Register is controlled by in some cases of the WP pin.

Table 6-1. Status Register-1

| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
|--|-------------------------------|---|------------------------------|------------------------------|------------------------------|--------------------|----------------------------|
| SRP | SEC | TB | BP2 | BP1 | BP0 | WEL | BUSY |
| Status Register Protect 0 (Non-Volatile) | Sector Protect (Non-Volatile) | Top/Bottom Write Protect (Non-Volatile) | Block Protect (Non-Volatile) | Block Protect (Non-Volatile) | Block Protect (Non-Volatile) | Write Enable Latch | Erase or Write in Progress |

Table 6-2. Status Register-2

| S15 | S14 | S13 | S12 | S11 | S10 | S9 | S8 |
|----------------|-----------------------------------|----------|----------|----------|----------|----------------------------|-----------------------------------|
| SUS | CMP | (R) | (R) | (R) | (R) | QE | SRP1 |
| Suspend Status | Complement Protect (Non-Volatile) | Reserved | Reserved | Reserved | Reserved | Quad Enable (Non-Volatile) | Register Protect 1 (Non-Volatile) |

6.1 Busy

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Erase, Write Status Register or Write Security Register instruction. During this time the device will ignore further instruction except for the Read Status Register and Erase / Program Suspend instruction (see t_W , t_{PP} , t_{SE} , t_{BE1} , t_{BE2} and t_{CE} in AC Characteristics). When the Program, Erase, Write Status Register or Write Security Register instruction has completed, the BUSY bit is cleared to a 0 state indicating the device is ready for further instructions.

6.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable instruction. The WEL status bit is cleared to a 0 when device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Erase and Write Status Register.

6.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide write protection control and status. Block protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

6.4 Top/Bottom Block protect (TB)

The Top/Bottom bit (TB) is non-volatile bits in the status register (S5) that controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB = 0) or the Bottom (TB = 1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB = 0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

6.5 Sector/Block Protect (SEC)

The Sector protect bit (SEC) is non-volatile bits in the status register (S6) that controls if the Block Protect bits (BP2, BP1, BP0) protect 4KB Sectors (SEC = 1) or 64KB blocks (SEC = 0) in the Top (TB = 0) or the Bottom (TB = 1) of the array as shown in the Status Register Memory protection table. The default setting is SEC = 0.

6.6 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 6-3. Status Register Protection

| SRP1 | SRP0 | \overline{WP} | Status Register | Description |
|------|------|-----------------|------------------------|---|
| 0 | 0 | X | Software Protected | \overline{WP} pin no control. The register can be written to after a Write Enable instruction, WEL = 1. [Factory Default] |
| 0 | 1 | 0 | Hardware Protected | When \overline{WP} pin is low the Status Register locked and can not be written to. |
| 0 | 1 | 1 | Hardware Unprotected | When \overline{WP} pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL = 1. |
| 1 | 0 | X | Power Supply Lock-Down | Status Register is protected and cannot be written to again until the next power down, power-up cycle (Note 1). |
| 1 | 1 | X | One Time Program | Status Register is permanently protected and cannot be written to. |

Note: 1. When SRP1, SRP0 = (1,0), a power down, power-up cycle changes SRP1, SRP0 to the (0,0) state.

6.7 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad operation. When the QE bit is set to a 0 state (factory default) the \overline{WP} pin and \overline{HOLD} are enabled. When the QE pin is set to a 1 the Quad IO₂ and IO₃ pins are enabled.

WARNING: The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the \overline{WP} or \overline{HOLD} pins are tied directly to the power supply or ground.

6.8 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 are reversed. For instance, when CMP = 0, a top 4KB sector can be protected while the rest of the array is not; when CMP = 1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP = 0.

6.9 Erase/Program Suspend Status (SUS)

The Suspend Status bit (SUS) is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power down, power-up cycle.

Table 6-4. Status Register Memory Protection (CMP = 0)

| Status Register Bits | | | | | Memory Protection | | | |
|----------------------|----|-----|-----|-----|-------------------|--------------------|---------|------------|
| SEC | TB | BP2 | BP1 | BP0 | Sector(s) | Addresses | Density | Portion |
| x | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 126 and 127 | 7E0000h - 7FFFFFFh | 128KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 124 - 127 | 7C0000h - 7FFFFFFh | 256KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 120 - 127 | 780000h - 7FFFFFFh | 512KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 112 - 127 | 700000h - 7FFFFFFh | 1MB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 96 - 127 | 600000h - 7FFFFFFh | 2MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 64 - 127 | 400000h - 7FFFFFFh | 4MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 and 1 | 000000h - 01FFFFh | 128KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 - 3 | 000000h - 03FFFFh | 256KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 - 7 | 000000h - 07FFFFh | 512KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 - 15 | 000000h - 0FFFFFFh | 1MB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 - 31 | 000000h - 1FFFFFFh | 2MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 - 63 | 000000h - 3FFFFFFh | 4MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 - 127 | 000000h - 7FFFFFFh | 8MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 127 | 7FF000h - 7FFFFFFh | 4KB | U – 1/2048 |
| 1 | 0 | 0 | 1 | 0 | 127 | 7FE000h - 7FFFFFFh | 8KB | U – 1/1024 |
| 1 | 0 | 0 | 1 | 1 | 127 | 7FC000h - 7FFFFFFh | 16KB | U – 1/512 |
| 1 | 0 | 1 | 0 | X | 127 | 7F8000h - 7FFFFFFh | 32KB | U – 1/256 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h - 000FFFh | 4KB | L – 1/2048 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h - 001FFFh | 8KB | L – 1/1024 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h - 003FFFh | 16KB | L – 1/512 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h - 007FFFh | 32KB | L – 1/256 |

Note:

1. X = Don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 1 in Appendix A for details.

Table 6-5. Status Register Memory Protection (CMP = 1)

| Status Register Bits | | | | | Memory Protection | | | |
|----------------------|----|-----|-----|-----|-------------------|--------------------|---------|-------------------|
| SEC | TB | BP2 | BP1 | BP0 | Sector(s) | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | 0 - 127 | 000000h - 7FFFFFFh | 8MB | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 - 125 | 000000h - 7DFFFFh | 8,064KB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 0 and 121 | 000000h - 7BFFFFh | 7,936KB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 0 - 119 | 000000h - 77FFFFh | 7,680KB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 0 - 111 | 000000h - 6FFFFFFh | 7,168KB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 0 - 95 | 000000h - 5FFFFFFh | 6MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 0 - 63 | 000000h - 3FFFFFFh | 4MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 2 - 127 | 020000h - 7FFFFFFh | 8,064KB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 4 and 127 | 040000h - 7FFFFFFh | 7,936KB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 8 - 127 | 080000h - 7FFFFFFh | 7,680KB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 16 - 127 | 100000h - 7FFFFFFh | 7,168KB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 32 - 127 | 200000h - 7FFFFFFh | 6MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 64 - 127 | 400000h - 7FFFFFFh | 4MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 - 127 | 000000h - 7FEFFFFh | 8,188KB | L – 2047/2048 |
| 1 | 0 | 0 | 1 | 0 | 0 - 127 | 000000h - 7FDFFFFh | 8,184KB | L – 1023/1024 |
| 1 | 0 | 0 | 1 | 1 | 0 - 127 | 000000h - 7FBFFFFh | 8,176KB | L – 511/512 |
| 1 | 0 | 1 | 0 | X | 0 - 127 | 000000h - 7F7FFFh | 8,160KB | L – 255/256 |
| 1 | 1 | 0 | 0 | 1 | 0 - 127 | 001000h - 7FFFFFFh | 8,188KB | U – 2047/2048 (4) |
| 1 | 1 | 0 | 1 | 0 | 0 - 127 | 002000h - 7FFFFFFh | 8,184KB | U – 1023/1024 |
| 1 | 1 | 0 | 1 | 1 | 0 - 127 | 004000h - 7FFFFFFh | 8,176KB | U – 511/512 |
| 1 | 1 | 1 | 0 | X | 0 - 127 | 008000h - 7FFFFFFh | 8,160KB | U – 255/256 |

Note:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 2 in Appendix A for details.

7. Instructions

The SPI instruction set of the AT25SL641 consists of thirty eight basic instructions and the QPI instruction set of the AT25SL641 consists of thirty one basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (\overline{CS}) and are completed with the rising edge of edge \overline{CS} . The first byte of data clocked into the input pins (SI or IO_{3:0}) provides the instruction code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Clock relative timing diagrams are included for each instruction below. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (\overline{CS} driven high after a full 8-bit have been clocked), otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Register will be ignored until the program or erase cycle has completed.

Table 7-1. Manufacturer and Device Identification

| | | ID code | Instruction |
|------------------|-----------|---------|--------------------|
| Manufacturer ID | Adesto | 1Fh | 90h, 92h, 94h, 9Fh |
| Device ID | AT25SL641 | 16h | 90h, 92h, 94h, ABh |
| Memory Type ID | SPI / QPI | 43h | 9Fh |
| Capacity Type ID | 64M | 17h | 9Fh |

7.1 Instruction Set Tables

Table 7-2. Instruction Set Table 1 (SPI Instructions)

| Instruction Name (Clock Number) | Byte 1 (0 - 7) | Byte 2 (8 - 15) | Byte 3 (16 - 23) | Byte 4 (24 - 31) | Byte 5 (32 - 39) | Byte 6 (40 - 47) |
|---|-------------------|---------------------------|---------------------|---------------------|------------------------|---------------------|
| Write Enable | 06h | | | | | |
| Write Enable For Volatile Status Register | 50h | | | | | |
| Write Disable | 04h | | | | | |
| Read Status Register-1 | 05h | (SR7-SR0) ⁽²⁾ | | | | |
| Read Status Register-2 | 35h | (SR15-SR8) ⁽²⁾ | | | | |
| Write Status Register-1 | 01h | (SR7-SR0) | (SR15-SR8) | | | |
| Write Status Register-2 | 31h | (SR15-SR8) | | | | |
| Read Data | 03h | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | |
| Fast Read Data | 0Bh | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Page Program | 02h | A23-A16 | A15-A8 | A7-A0 | (D7-D0) ⁽³⁾ | |
| Enable QPI | 38h | | | | | |
| Block Erase (4KB) | 20h | A23-A16 | A15-A8 | A7-A0 | | |
| Block Erase (32KB) | 52h | A23-A16 | A15-A8 | A7-A0 | | |
| Block Erase (64KB) | D8h | A23-A16 | A15-A8 | A7-A0 | | |
| Chip Erase | 60h/C7h | | | | | |

Table 7-2. Instruction Set Table 1 (SPI Instructions) (Continued)

| Instruction Name | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 |
|--|---------|-------------------------------|--------------------------|----------------------------|--------------------------|-------------|
| (Clock Number) | (0 - 7) | (8 - 15) | (16 - 23) | (24 - 31) | (32 - 39) | (40 - 47) |
| Erase/Program Suspend | 75h | | | | | |
| Erase/Program Resume | 7Ah | | | | | |
| Deep Power Down | B9h | | | | | |
| Release Deep Power Down/Device ID ⁽⁴⁾ | ABh | dummy | dummy | dummy | (ID7-ID0) ⁽²⁾ | |
| Read Manufacturer/Device ID ⁽⁴⁾ | 90h | 00h | 00h | 00h or 01h | (MID7-MID0) | (DID7-DID0) |
| Read JEDEC ID | 9Fh | (MID7-MID0) (Manufacturer) | (D7-D0) (Memory Type) | (D7-D0) (Capacity Type) | | |
| Reset Enable | 66h | | | | | |
| Reset | 99h | | | | | |
| Enter Secured OTP | B1h | | | | | |
| Exit Secured OTP | C1h | | | | | |
| Read Security Register | 2Bh | (SC7-SC0) ⁽¹⁰⁾ | | | | |
| Write Security Register | 2Fh | | | | | |
| Read Serial Flash Discovery Parameters | 5Ah | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |

Table 7-3. Instruction Set Table 2 (Dual SPI Instructions)

| Instruction Name | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 |
|---|---------|-----------------------|-------------------------------|---|-----------|------------------------|
| (Clock Number) | (0 - 7) | (8 - 15) | (16 - 23) | (24 - 31) | (32 - 39) | (40 - 47) |
| Fast Read Dual Output | 3Bh | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) ⁽⁶⁾ |
| Fast Read Dual I/O | BBh | A23-A8 ⁽⁵⁾ | A7-A0, M7-M0 | (D7-D0, ...) ⁽⁶⁾ | | |
| Read Dual Manufacturer/Device ID ⁽⁴⁾ | 92h | 0000h | (00h, xxxx) or (01h, xxxx) | (MID7-MID0) (DID7-DID0) ⁽⁶⁾ | | |

Table 7-4. Instruction Set Table 3 (Quad SPI Instructions)

| Instruction Name | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 |
|-----------------------|---------|---------------------------------------|---------------------------------|-----------------------------|-----------|------------------------|
| (Clock Number) | (0 - 7) | (8 - 15) | (16 - 23) | (24 - 31) | (32 - 39) | (40 - 47) |
| Fast Read Quad Output | 6Bh | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) ⁽⁸⁾ |
| Fast Read Quad I/O | EBh | A23-A0, M7-M0 ⁽⁷⁾ | (xxx, D7-D0,...) ⁽⁹⁾ | (D7-D0, ...) ⁽⁸⁾ | | |
| Quad Page Program | 33h | A23-A0 (D7-D0, ...) ⁽⁸⁾ | | | | |

Table 7-4. Instruction Set Table 3 (Quad SPI Instructions) (Continued)

| Instruction Name | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 |
|--|---------|--|---|------------------------|-----------|-----------|
| (Clock Number) | (0 - 7) | (8 - 15) | (16 - 23) | (24 - 31) | (32 - 39) | (40 - 47) |
| Read Quad Manufacturer /Device ID ⁽⁴⁾ | 94h | (00_0000h, xx) or (00_0001h, xx) | (xxxx,MID7-MID0) (xxxx,DID7-DID0) ⁽⁹⁾ | | | |
| Word Read Quad I/O | E7h | A23-A0, M7-M0 ⁽⁷⁾ | (xx, D7-D0..) | (D7-D0) ⁽⁸⁾ | | |
| Set Burst with Wrap | 77h | xxxxxx, W6-W4 ⁽⁷⁾ | | | | |

Table 7-5. Instruction Set Table 4 (QPI Instructions)

| Instruction Name | Byte 1 | Byte 3 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 |
|---|---------------|---------------------------|------------|--------|------------------------|----------|----------|----------|----------|
| (Clock Number) | (0, 1) | (2, 3) | (4, 5) | (6, 7) | (8, 9) | (10, 11) | (12, 13) | (14, 15) | (16, 17) |
| Write Enable | 06h | | | | | | | | |
| Write Enable for Volatile Status Register | 50h | | | | | | | | |
| Write Disable | 04h | | | | | | | | |
| Read Status Register-1 | 05h | (SR7-SR0) ⁽²⁾ | | | | | | | |
| Read Status Register-2 | 35h | (SR15-SR8) ⁽²⁾ | | | | | | | |
| Write Status Register-1 ⁽⁵⁾ | 01h | (SR7-SR0) | (SR15-SR8) | | | | | | |
| Write Status Register-2 | 31h | (SR15-SR8) | | | | | | | |
| Set Read Parameter | C0h | P7-P0 | | | | | | | |
| Fast Read Data | >80 MHz | 0Bh | A23-A16 | A15-A8 | A7-A0 | Dummy | Dummy | (D7-D0) | |
| | >104 MHz | | A23-A16 | A15-A8 | A7-A0 | Dummy | Dummy | Dummy | (D7-D0) |
| | up to 133 MHz | | A23:A16 | A15:A8 | A7:A0 | Dummy | Dummy | Dummy | Dummy |
| Page Program | 02h | A23-A16 | A15-A8 | A7-A0 | (D7-D0) ⁽³⁾ | | | | |
| Block Erase (4KB) | 20h | A23-A16 | A15-A8 | A7-A0 | | | | | |
| Block Erase (32KB) | 52h | A23-A16 | A15-A8 | A7-A0 | | | | | |
| Block Erase (64KB) | D8h | A23-A16 | A15-A8 | A7-A0 | | | | | |
| Chip Erase | 60h/C7h | | | | | | | | |
| Erase/Program Suspend | 75h | | | | | | | | |
| Erase/Program Resume | 7Ah | | | | | | | | |
| Deep Power Down | B9h | | | | | | | | |
| Release Deep Power Down | ABh | | | | | | | | |

Table 7-5. Instruction Set Table 4 (QPI Instructions) (Continued)

| Instruction Name | Byte 1 | Byte 3 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 |
|--|---------------|---------------------------|---------------------|-----------------------|-------------|-------------|----------|----------|----------|
| (Clock Number) | (0, 1) | (2, 3) | (4, 5) | (6, 7) | (8, 9) | (10, 11) | (12, 13) | (14, 15) | (16, 17) |
| Read Manufacturer/Device ID ⁽⁴⁾ | 90h | 00h | 00h | 00h or 01h | (MID7-MID0) | (DID7-DID0) | | | |
| Read JEDEC ID ⁽⁴⁾ | 9Fh | (MID7-MID0) Manufacturer | (D7-D0) Memory Type | (D7-D0) Capacity Type | | | | | |
| Enter Security | B1h | | | | | | | | |
| Exit Security | C1h | | | | | | | | |
| Read Security Register | 2Bh | (SC7-SC0) ⁽¹⁰⁾ | | | | | | | |
| Write Security Register | 2Fh | | | | | | | | |
| Fast Read Quad I/O ⁽¹¹⁾ | >80 MHz | EBh | A23-A16 | A15-A8 | A7-A0 | (M7-M0) | Dummy | (D7-D0) | |
| | >104 MHz | | A23-A16 | A15-A8 | A7-A0 | (M7-M0) | Dummy | Dummy | (D7-D0) |
| | up to 133 MHz | | A23-A16 | A15-A8 | A7-A0 | (M7-M0) | Dummy | Dummy | Dummy |
| Reset Enable | 66h | | | | | | | | |
| Reset | 99h | | | | | | | | |
| Disable QPI | FFh | | | | | | | | |
| Burst Read with Wrap | >80 MHz | 0Ch | A23-A16 | A15-A8 | A7-A0 | Dummy | Dummy | (D7-D0) | |
| | >104 MHz | | A23-A16 | A15-A8 | A7-A0 | Dummy | Dummy | Dummy | (D7-D0) |
| | up to 133 MHz | | A23-A16 | A15-A8 | A7-A0 | Dummy | Dummy | Dummy | Dummy |
| Quad Page Program | 33h | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | | | | |

Notes:

- Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “()” indicate data being read from the device on the IO pin.
- SR = status register, The Status Register contents and Device ID repeats continuously until \overline{CS} terminates the instruction.
- At least one byte of data input is required for Page Program, Quad Page Program and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.
- See Manufacturer and Device Identification table for Device ID information.
- Dual Input Address
 IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
 IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
- Dual Output data
 IO0 = (D6, D4, D2, D0)
 IO1 = (D7, D5, D3, D1)
- Quad Input Address
 IO0 = A20, A16, A12, A8, A4, A0, M4, M0
 IO1 = A21, A17, A13, A9, A5, A1, M5, M1
 IO2 = A22, A18, A14, A10, A6, A2, M6, M2
 IO3 = A23, A19, A15, A11, A7, A3, M7, M3

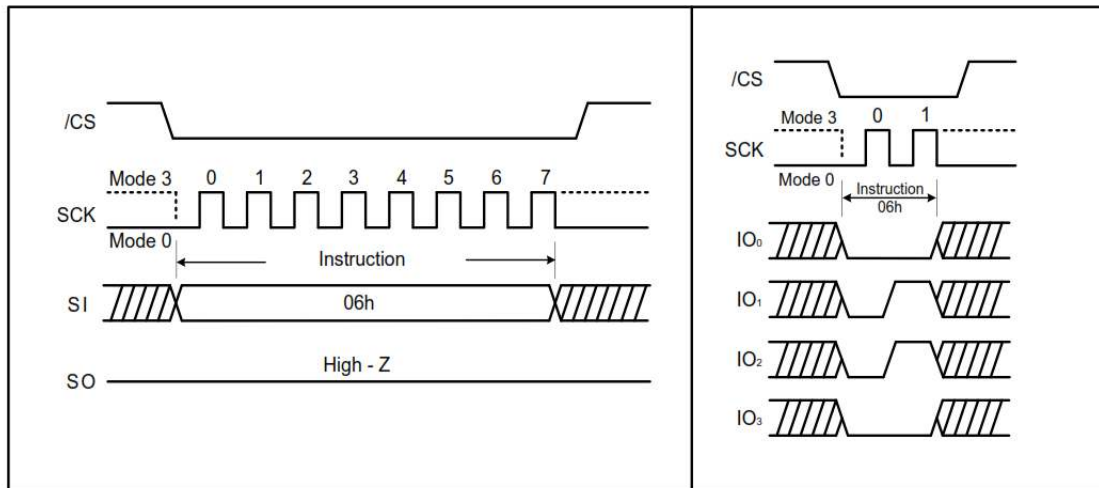
Set Burst with Wrap Input
 IO0 = x, x, x, x, x, x, W4, x
 IO1 = x, x, x, x, x, x, W5, x
 IO2 = x, x, x, x, x, x, W6, x
 IO3 = x, x, x, x, x, x, x

8. Quad Input/ Output Data
 IO0 = (D4, D0...)
 IO1 = (D5, D1...)
 IO2 = (D6, D2...)
 IO3 = (D7, D3...)
9. Fast Read Quad I/O Data Output
 IO0 = (x, x, x, x, D4, D0...)
 IO1 = (x, x, x, x, D5, D1...)
 IO2 = (x, x, x, x, D6, D2...)
 IO3 = (x, x, x, x, D7, D3...)
10. SC = security register
11. The M7-M0 bits are counted as dummy clocks.

7.2 Write Enable (06h)

Write Enable instruction is for setting the Write Enable Latch (WEL) bit in the Status Register. The WEL bit must be set prior to every Program, Erase and Write Status Register instruction. To enter the Write Enable instruction, \overline{CS} goes low prior to the instruction (06h) being driven onto the SI pin on the rising edge of SCK, and then driving \overline{CS} high.

Figure 7-1. Write Enable Instruction for SPI Mode (left) and QPI Mode (right)

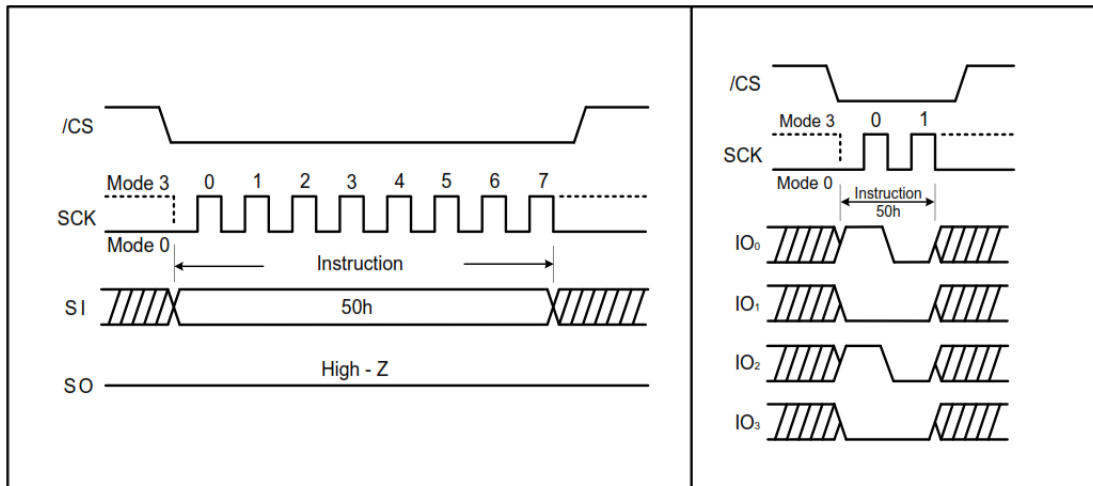


7.3 Write Enable for Volatile Status Register (50h)

This instruction gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction.

The Write Enable for Volatile Status Register instruction (Figure 7-2) does not set the Write Enable Latch (WEL) bit. Once Write Enable for Volatile Status Register is set, a Write Enable instruction should not have been issued prior to setting Write Status Register instruction (01h or 31h). When the Write Enable for Volatile Status Register (50h) is executed in QPI Mode, the SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 must be driven to high after Write Status Register instruction (01h). Once the Read Status Register (05h or 31h) instruction is issued, the read values of the SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 are ignored.

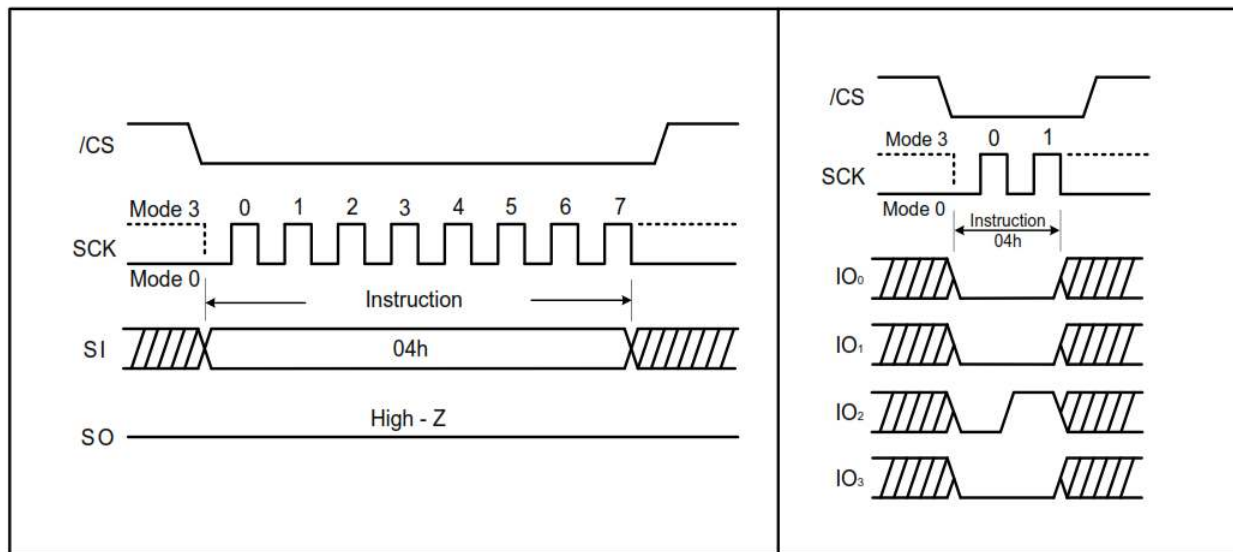
Figure 7-2. Write Enable for Volatile Status Register Instruction for SPI Mode (left) and QPI Mode (right)



7.4 Write Disable (04h)

The Write Disable instruction is to reset the Write Enable Latch (WEL) bit in the Status Register. To enter the Write Disable instruction, $\overline{\text{CS}}$ goes low prior to the instruction 04h being driven onto the SI pin on the rising edge of SCK, and then driving $\overline{\text{CS}}$ high. The WEL bit is automatically reset write-disable status of “0” after power-up and upon completion of the every Program, Erase and Write Status Register instruction.

Figure 7-3. Write Disable Instruction for SPI Mode (left) and QPI Mode (right)



7.5 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions 05h and 35h are used to read Status Registers 1 and 2 respectively. The Read Status Register can be read at any time (even in program/erase/write Status Register and Write Security Register condition). It is recommended to check the BUSY bit before sending a new instruction when a Program, Erase, Write Status Register or Write Status Register operation is in progress.

The instruction is entered by driving $\overline{\text{CS}}$ low and sending the instruction code (05h) for Status Register-1 or (35h) for Status Register-2 onto the SI pin on the rising edge of SCK. The Status Register bits are then shifted out on the SO pin at the falling

edge of SCK with most significant bit (MSB) first as shown in (Figure 7-4 and Figure 7-5). The Status Register can be read continuously. The instruction is completed by driving \overline{CS} high.

Figure 7-4. Read Status Register Instruction (SPI Mode)

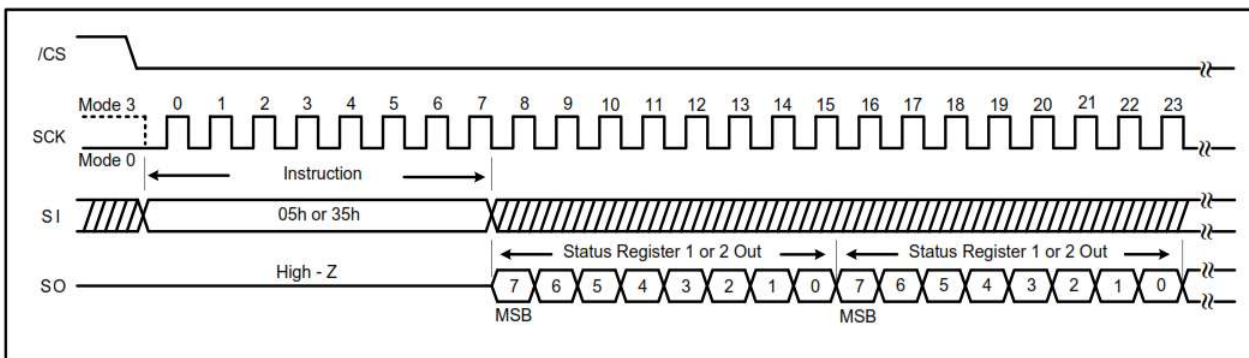
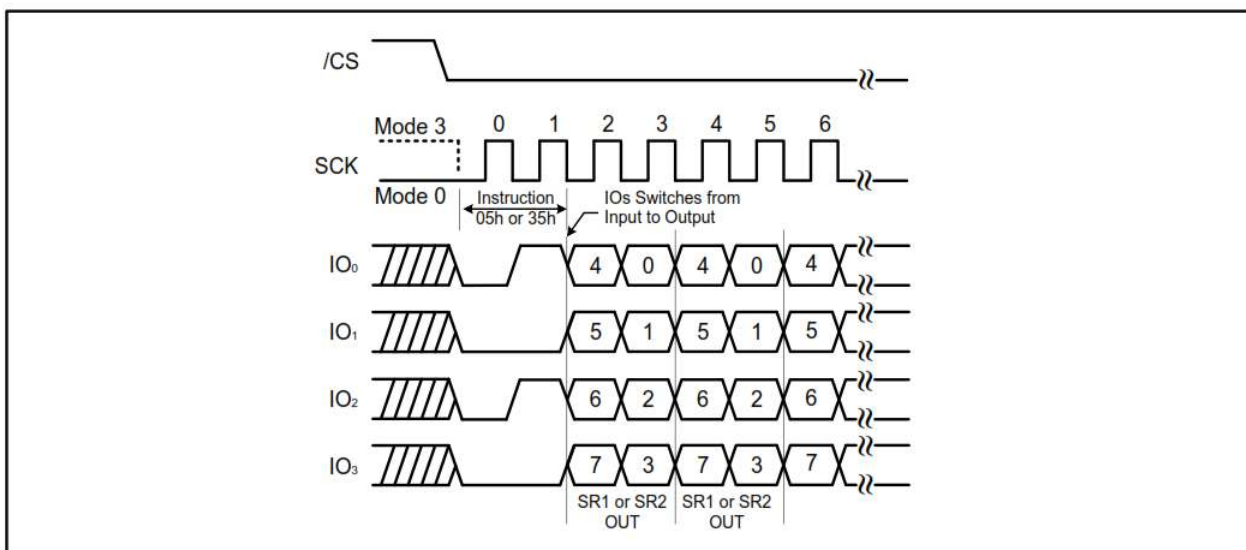


Figure 7-5. Read Status Register Instruction (QPI Mode)



7.6 Write Status Register (01h)

The Write Status Register instruction is used to write the non-volatile Status Register-1 bit (SRP0) and Status Register-2 bits (QE and SRP1). All other Status Register bit locations are read-only and are not affected by the Write Status Register instruction.

A Write Enable instruction must previously have been issued prior to setting Write Status Register Instruction (Status Register bit WEL must equal 1). Once the write is enabled, the instruction is entered by driving \overline{CS} low, sending the instruction code, and then writing the status register data byte as illustrated in Figure 7-6 and Figure 7-7.

The \overline{CS} pin must be driven high after either the eighth or sixteenth bit of data is clocked in. If this is not done, the Write Status Register instruction will not be executed. If \overline{CS} is driven high after the eighth clock, the CMP, QE, and SRP1 bits are cleared to 0. After \overline{CS} is driven high, the self-timed Write Status Register cycle commences for a time duration of t_w (See AC Characteristics).

While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is driven high during the Write Status Register cycle and driven low when the cycle has finished and is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in Status Register is cleared to 0.

Figure 7-6. Write Status Register Instruction (SPI Mode)

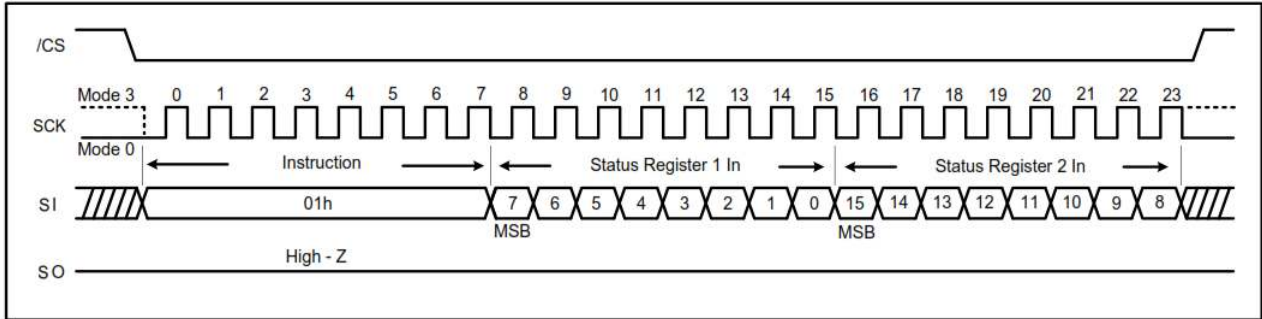
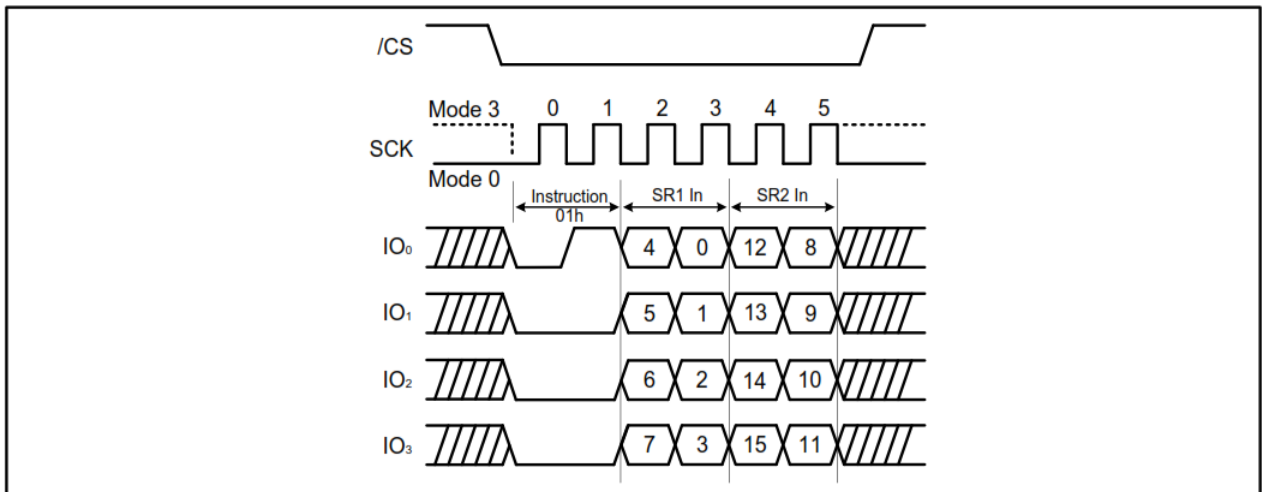


Figure 7-7. Write Status Register Instruction (QPI Mode)



7.7 Write Status Register-2 (31h)

The Write Status Register-2 instruction is used to write only non-volatile Status Register-2 bits (CMP, QE and SRP1). A Write Enable instruction must previously have been issued prior to setting Write Status Register Instruction (Status Register bit WEL must equal 1). Once write is enabled, the instruction is entered by driving CS low, sending the instruction code, and then writing the Status Register data byte as illustrated in [Figure 7-8](#) and [Figure 7-9](#).

Using Write Status Register-2 (31h) instruction, software can individually access each one-byte Status Register via different instructions.

Figure 7-8. Write Status Register-2 Instruction (SPI Mode)

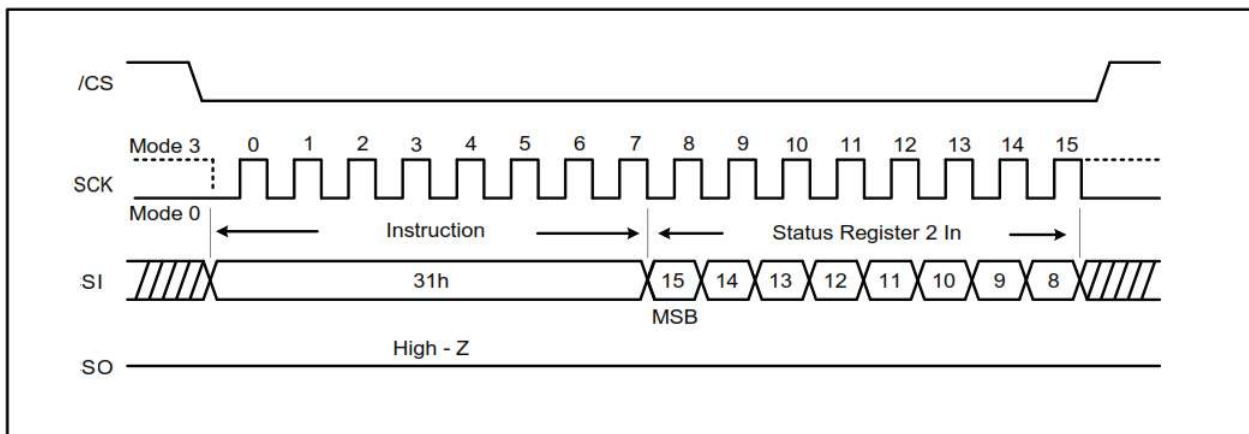
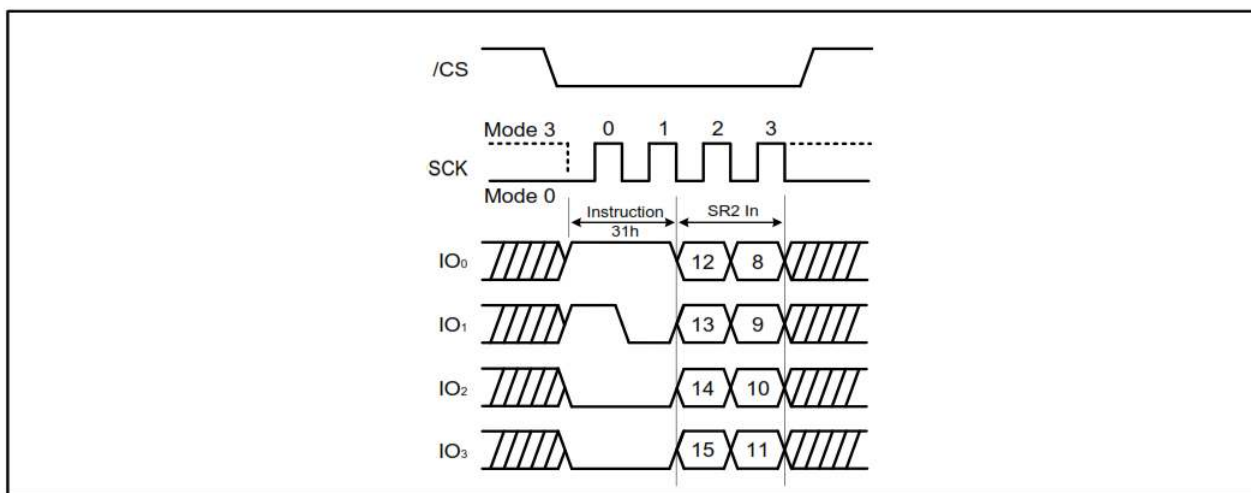


Figure 7-9. Write Status Register-2 Instruction (QPI Mode)



7.8 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, the Set Read Parameters (C0h) instruction can be used to configure the number of dummy clocks for the Fast Read (0Bh), Fast Read Quad I/O (EBh), and Burst Read with Wrap (0Ch) instructions, and to configure the number of bytes of wrap length for the Burst Read with Wrap (0Ch) instruction.

In Standard SPI mode, the Set Read Parameters (C0h) instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed. The wrap length is set by the W6-W5 bits in the Set Burst with Wrap (77h) instruction. This setting remains unchanged when the device is switched from Standard SPI mode to QPI mode.

The default wrap length after a power up or a Reset instruction is 8 bytes, and the default number of dummy clocks is 4.

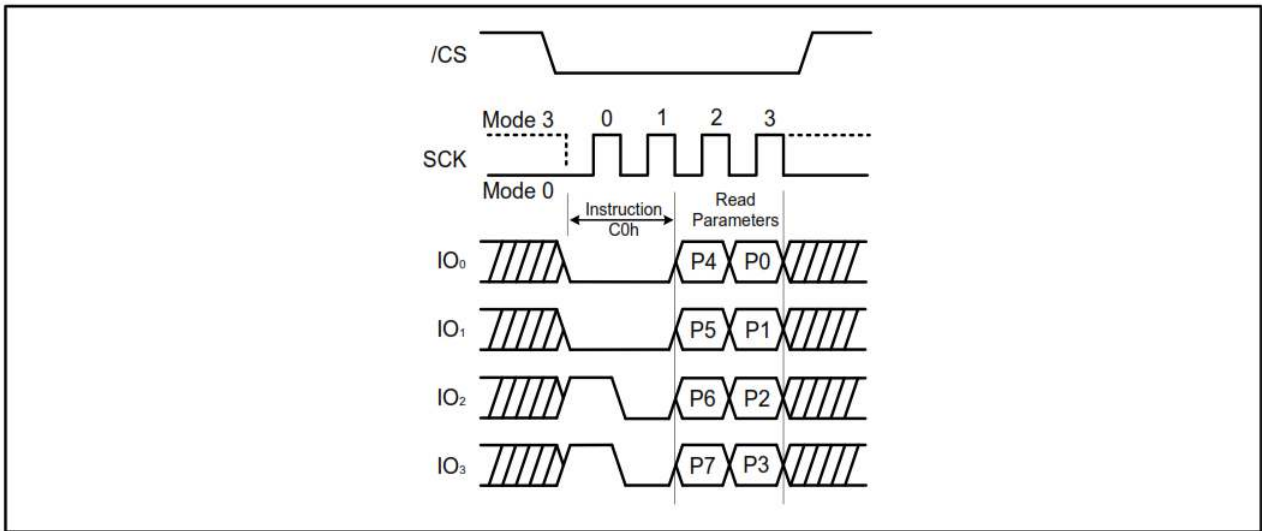
Table 7-6. Encoding of the P[5:4] Bits

| P5, P4 | Dummy Clocks | Maximum Read Frequency |
|--------|--------------|------------------------|
| 00 | 4 | 80 MHz |
| 01 | 4 | 80 MHz |
| 10 | 6 | 104 MHz |
| 11 | 8 | 133 MHz |

Table 7-7. Encoding of the P[1:0] Bits

| P1, P0 | Wrap Length |
|--------|-------------|
| 0 0 | 8-byte |
| 0 1 | 16-byte |
| 1 0 | 32-byte |
| 1 1 | 64-byte |

Figure 7-10. Set Read Parameters Instruction (QPI Mode)



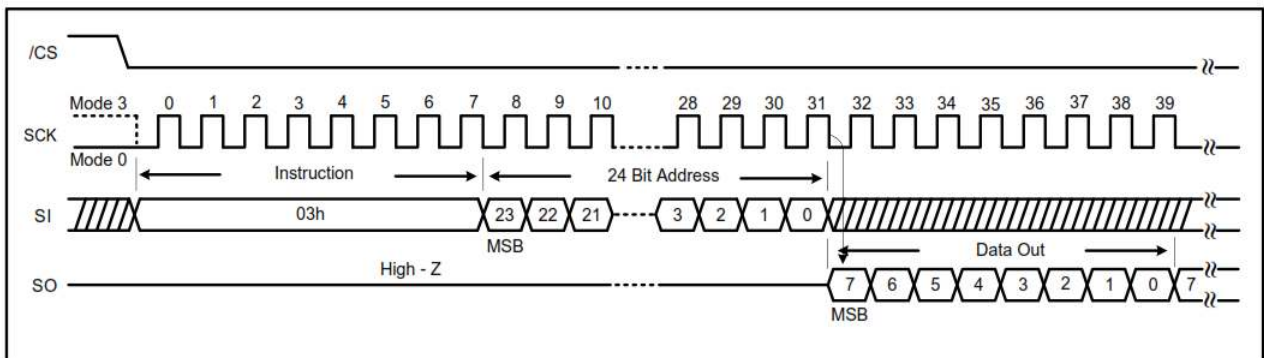
7.9 Read Data (03h)

The Read Data instruction is used to read data out from the device. The instruction is initiated by driving the \overline{CS} pin low and then sending the instruction code 03h, followed by a 24-bit address (A23- A0), onto the SI pin. After the address is received, the data byte of the addressed memory location is shifted out on the SO pin at the falling edge of SCK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address and the next byte of data is shifted out, allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues.

The instruction is completed by driving \overline{CS} high. The Read Data instruction sequence is shown in [Figure 7-11](#). If a Read Data instruction is issued while an Erase, Program or Write Status Register cycle is in process (BUSY = 1) the instruction is ignored

and does not effect the current cycle. The Read Data instruction allows clock rates from D.C to a maximum of f_R (see AC Electrical Characteristics).

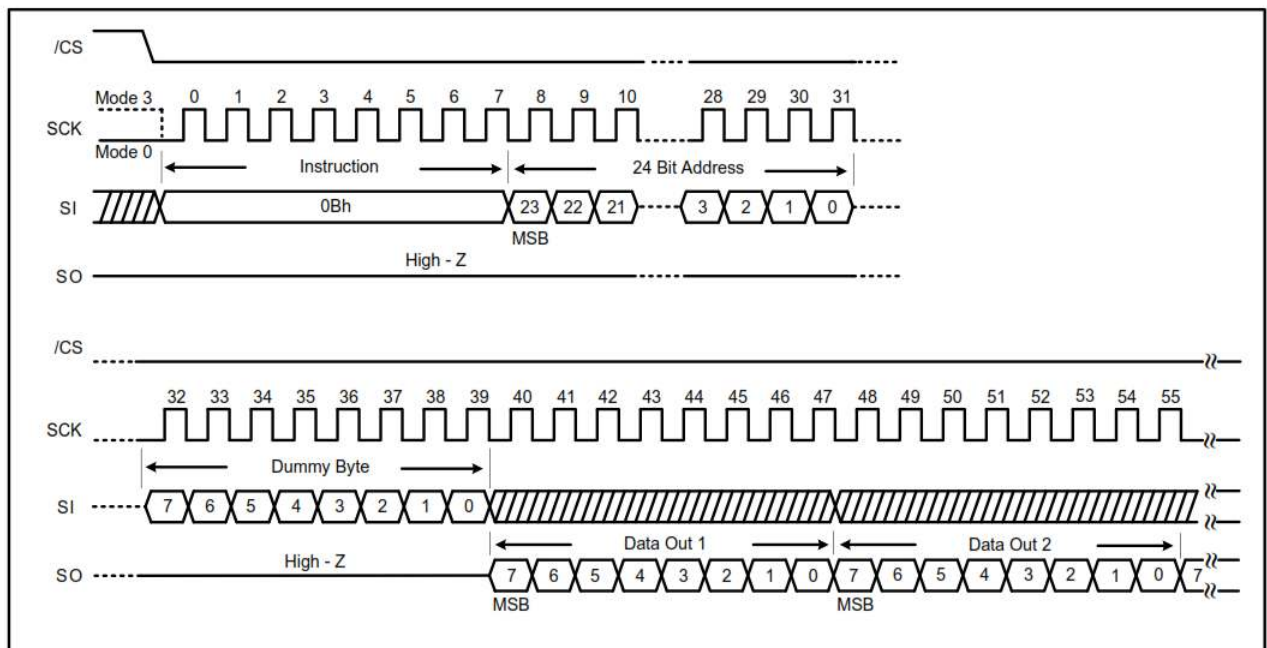
Figure 7-11. Read Data Instruction



7.10 Fast Read (0Bh)

The Fast Read instruction is a high speed reading mode that can operate at the highest possible frequency of F_R . The address is latched on the rising edge of the SCK. After the 24-bit address, eight dummy clocks are shifted in as shown in [Figure 7-12](#). The dummy clocks allow the internal circuits the time required to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. Data of each bit shifts out on the falling edge of SCK.

Figure 7-12. Fast Read Instruction (SPI Mode)

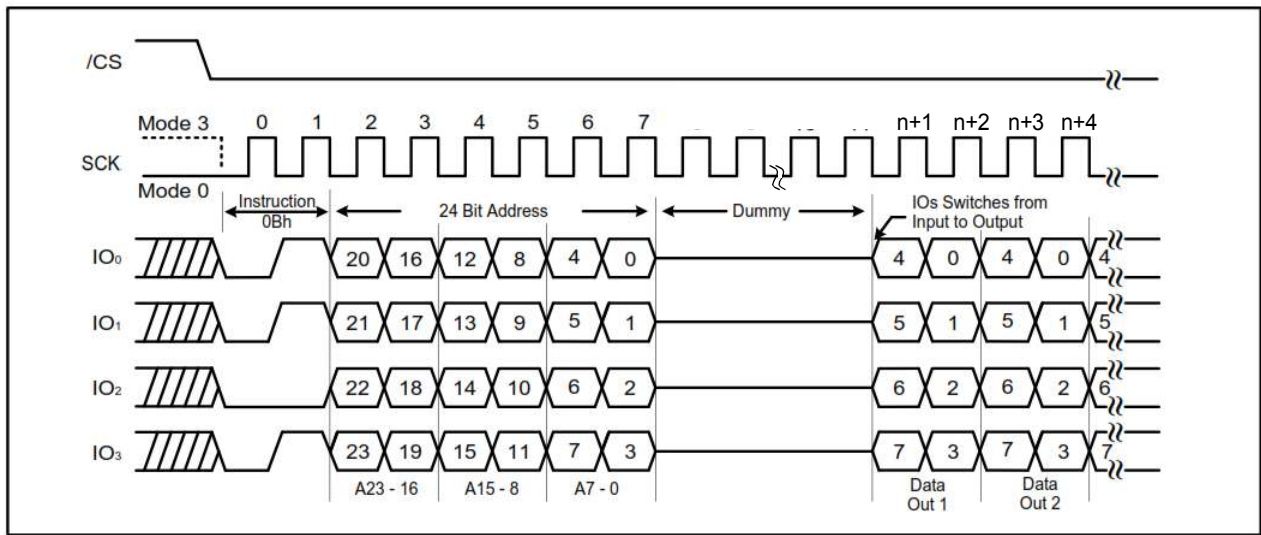


Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the Set Read Parameters (C0h) instruction to accommodate a wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. The number of dummy clock cycles can be configured as either 4, 6 or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command as shown in [Table 7-6, Encoding of the P\[5:4\] Bits](#). The

default number of dummy clocks upon power up or after a Reset instruction is 4. Please refer to [Figure 7-13](#).

Figure 7-13. Fast Read Instruction (QPI Mode)

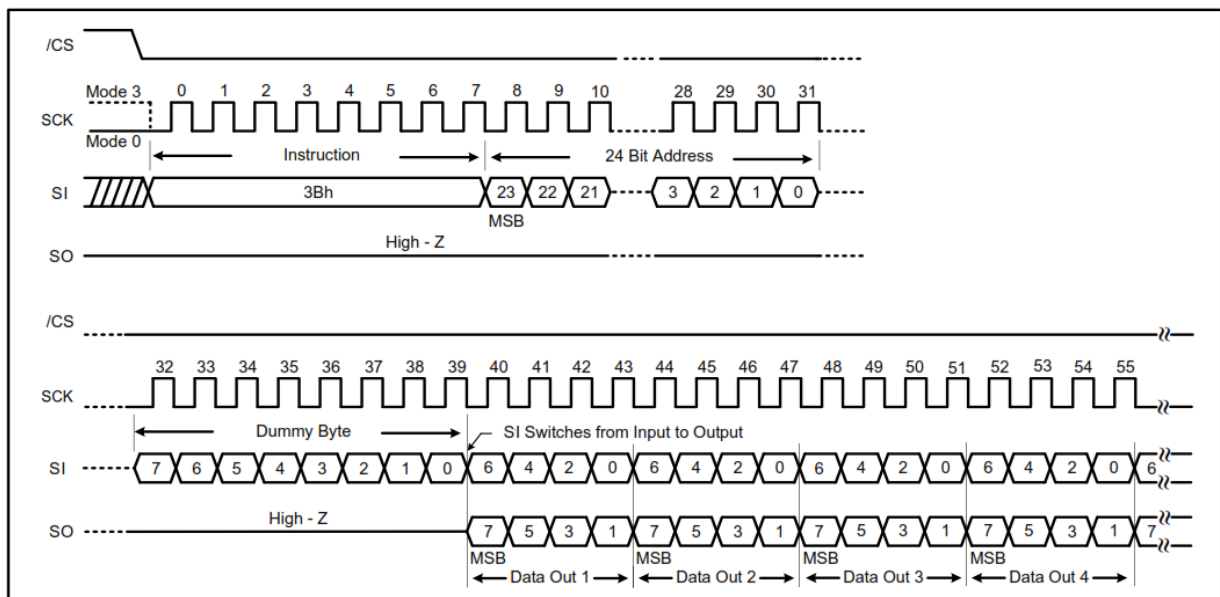


7.11 Fast Read Dual Output (3Bh)

By using two pins (IO_0 and IO_1 , instead of just IO_0), the Fast Read Dual Output instruction allows data to be transferred from the AT25SL641 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution.

The Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). After the 24-bit address, eight dummy clocks are driven on the SI pin as shown in [Figure 7-14](#). The dummy clocks allow the internal circuits the time required for setting up the initial address. During the dummy clocks, the data value on the SO pin is a “don't care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

Figure 7-14. Fast Read Dual Output instruction (SPI Mode)

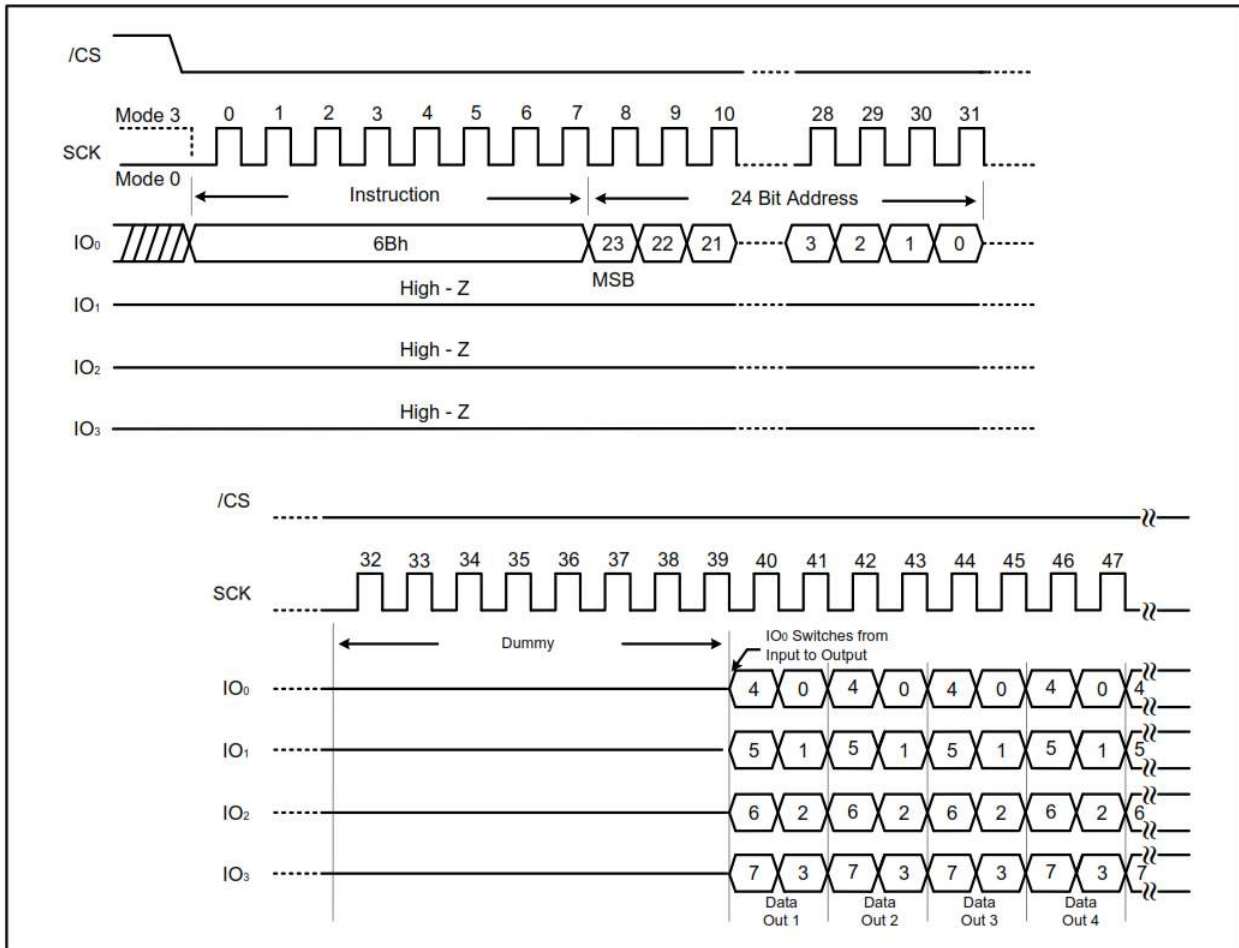


7.12 Fast Read Quad Output (6Bh)

By using four pins (IO_0 , IO_1 , IO_2 , and IO_3), the Fast Read Quad Output instruction allows data to be transferred from the AT25SL641 at four times the rate of standard SPI devices. Prior to executing the 6Bh instruction, the Quad Enable (QE) bit of Status Register 2 must be set.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight dummy clocks after the 24-bit address as shown in Figure 7-15. The dummy clocks allow the internal circuits the time required to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

Figure 7-15. Fast Read Quad Output Instruction (SPI Mode)



7.13 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O instruction reduces cycle overhead by using two IO pins: IO_0 and IO_1 to transfer data.

Continuous Read Mode

The Fast Read Dual I/O instruction supports a continuous read mode using the Mode bits (M7-0), which are shifted into the device after address bits (A23-0). The upper nibble of the Mode (M7-4) controls whether the instruction code must be driven to the device on subsequent access. If the Mode bits (M7-0) equal “Ax” hex, then the next Fast Dual I/O instruction (after \overline{CS} is raised and then lowered) does not require the instruction (BBh) code, as shown in Figure 7-16 and Figure 7-17. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after \overline{CS} is asserted low.

If Mode bits (M7-0) are any value other "Ax" hex, the next instruction (after \overline{CS} is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A mode bit reset can be used to reset Mode bits (M7-0) before issuing normal instructions.

The bits of the lower nibble (M3-0) are don't care ("X"). However, the I/O pins should be high-impedance prior to the falling edge of the first data out clock.

Figure 7-16. Fast Read Dual I/O Instruction (initial instruction or previous M7-0 \neq Axh)

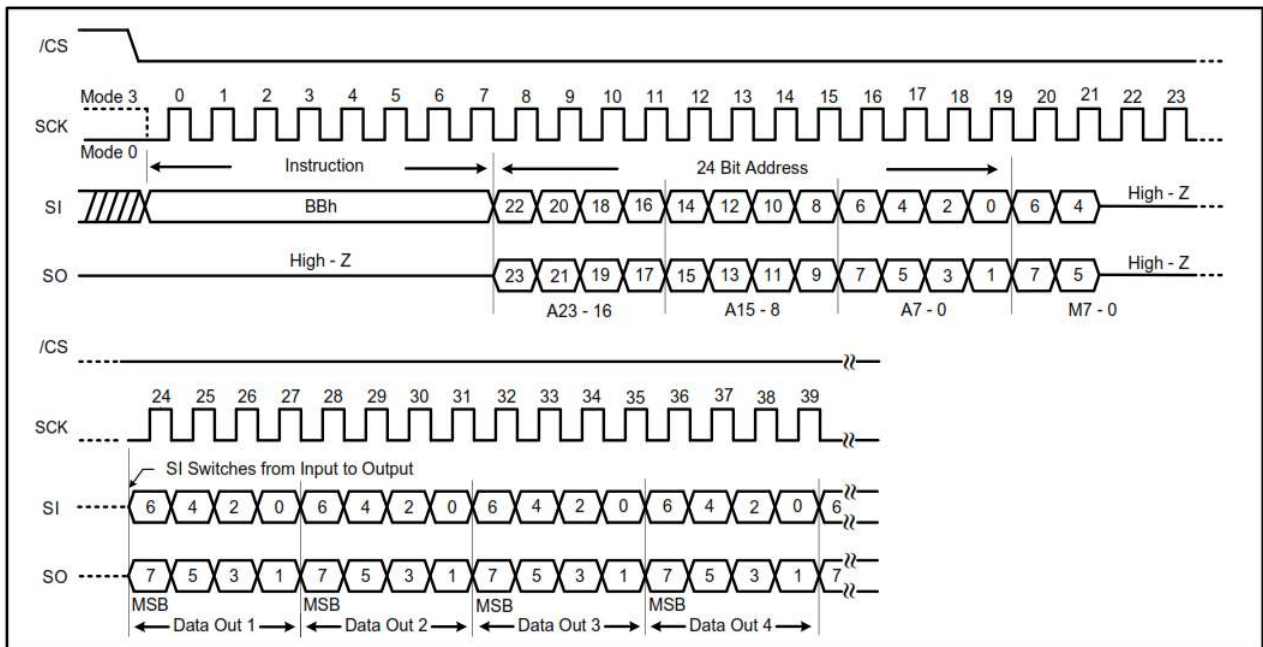
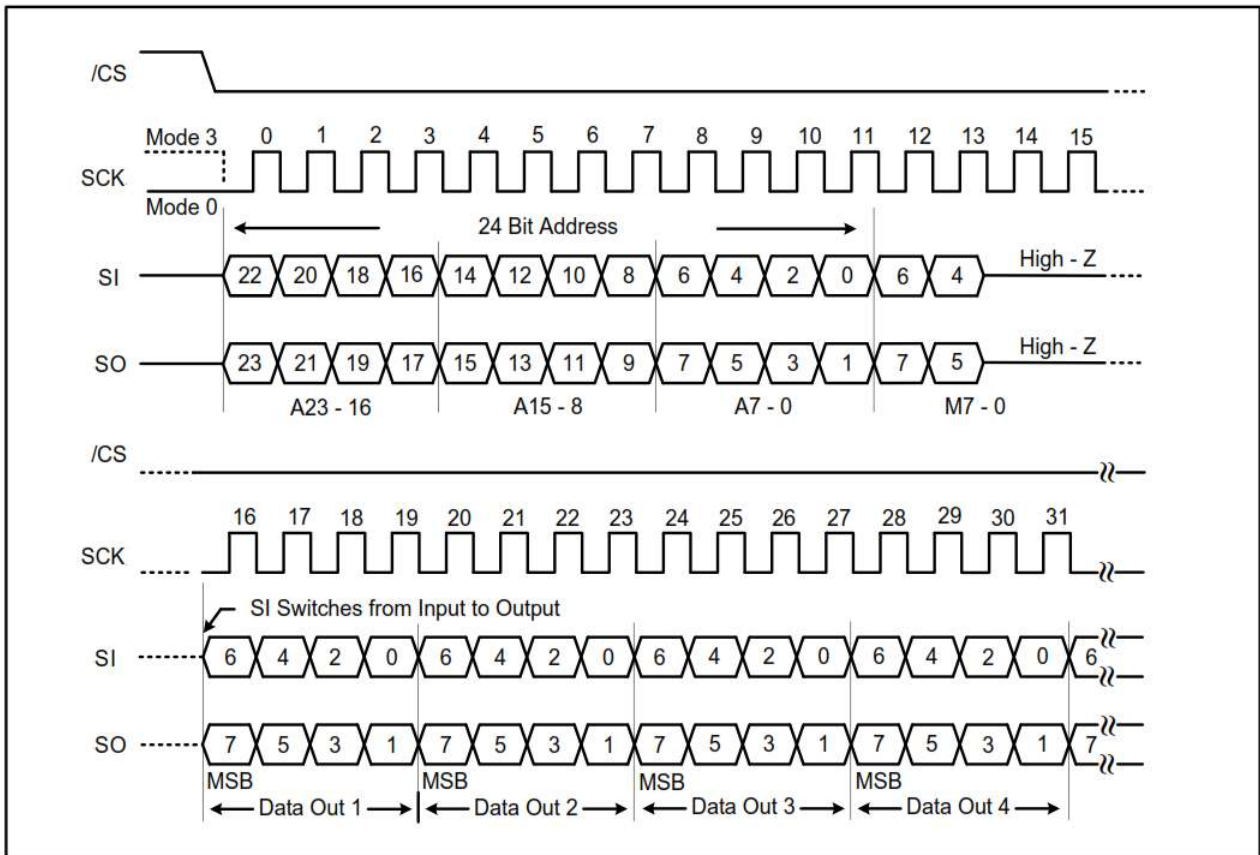


Figure 7-17. Fast Read Dual I/O Instruction (previous M7-0 = Axh)



7.14 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O instruction reduces cycle overhead through quad access using four IO pins: IO₀, IO₁, IO₂, and IO₃. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast read Quad I/O Instruction.

Continuous Read Mode

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Mode bits (M7-0) with following the input Address bits (A23-0), as shown in Figure 7-18. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0) are don't care ("X"). However, the I/O pins should be high-impedance prior to the falling edge of the first data out clock. Note that the mode bits are counted as dummy clocks.

If the Mode bits (M7-0) equal Ax hex, then the next Fast Read Quad I/O instruction (after \overline{CS} is raised and then lowered) does not require the EBh instruction code, as shown in Figure 7-19. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after \overline{CS} is asserted low. If the Mode bits (M7-0) are any value other than "Ax" hex, the next instruction (after \overline{CS} is raised and then lowered) requires the first byte instruction code, thus retuning normal operation. A mode bit reset can be used to reset Mode bits (M7-0) before issuing normal instructions.

Figure 7-18. Fast Read Quad I/O Instruction (Initial instruction or previous M7-0 ≠ Axx, SPI mode)

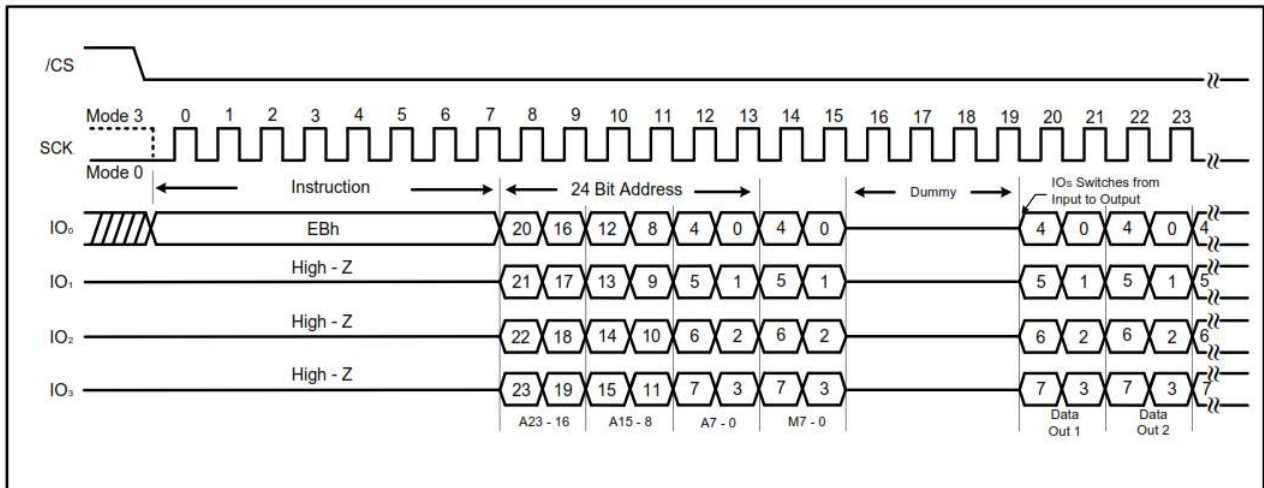
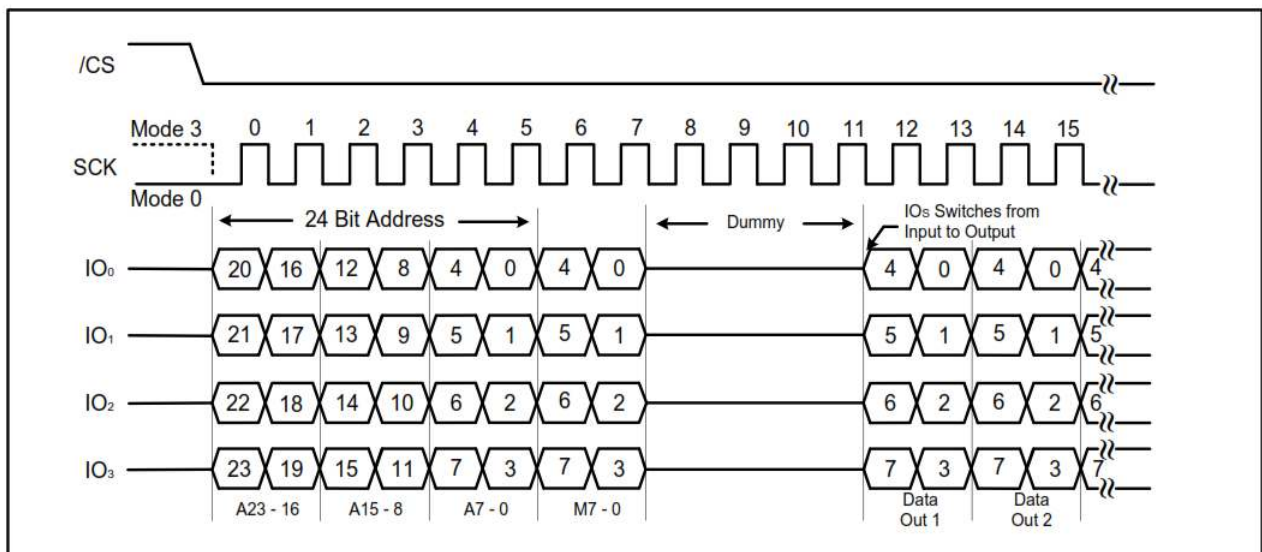


Figure 7-19. Fast Read Quad I/O Instruction (previous M7-0 = Axx, SPI mode)



Wrap Around in SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) instruction prior to issuing the Fast Read Quad I/O (EBh) instruction. The Set Burst with Wrap (77h) instruction can either enable or disable the Wrap Around feature for the following Fast Read Quad I/O instruction.

When Wrap Around is enabled, the data being accessed can be limited to an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until \overline{CS} is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions. (Please refer to [Section 7.32 Set Burst with Wrap](#)).

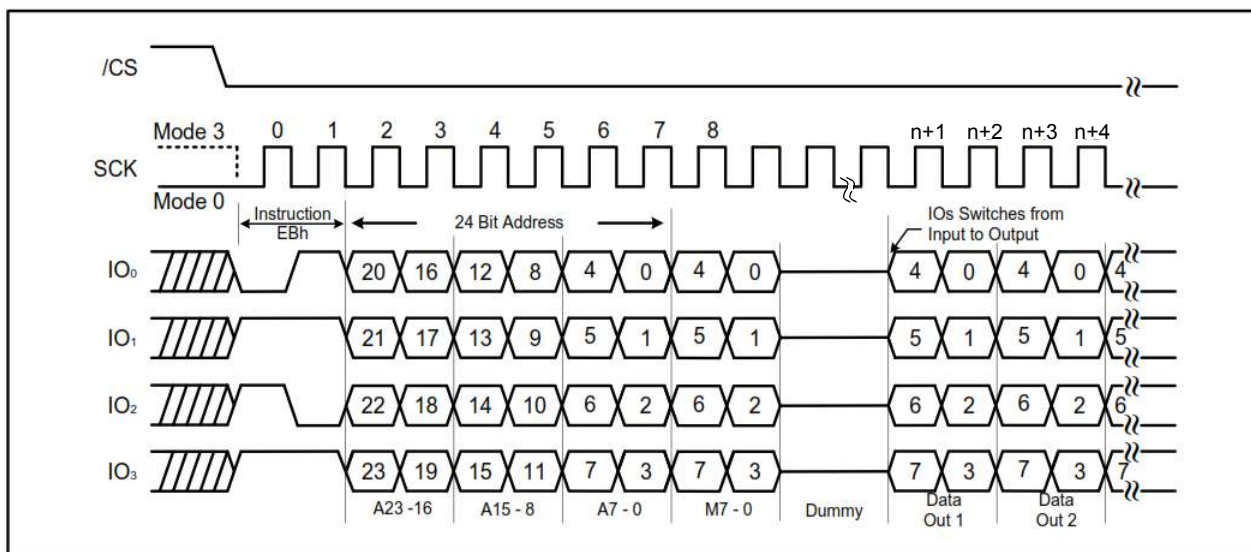
Fast Read Quad I/O in QPI Mode

When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) instruction to accommodate a wide range of applications with different needs for either maximum fast read frequency or minimum data access latency. The number of dummy clock cycles can be configured as either 4, 6 or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command as shown in [Table 7-6, Encoding of P\[5:4\] Bits](#). The default number of dummy clocks upon power up or after a Reset (99h) instruction is four.

The Continuous Read Mode feature is also available in QPI mode for Fast Read Quad I/O instruction. In QPI mode, the Continuous Read Mode bits M7-M0 are also considered as dummy clocks.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a Burst Read with Wrap (0Ch) instruction must be used. Please refer to [Section 7.33, Burst Read with Wrap](#).

Figure 7-20. Fast Read Quad I/O Instruction (Initial instruction or previous M7-0 ≠ A_{xh}, QPI mode)



7.15 Page Program (02h)

The Page Program instruction is used for programming the memory to “0”. A Write Enable instruction (06h) must be issued before the device accepts the Page Program Instruction (Status Register bit WEL = 1). After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL) bit in the Status Register. The instruction is entered by driving the $\overline{\text{CS}}$ pin low and then sending the instruction code 02h followed by a 24-bit address (A23-A0) and at least one data byte on the $\overline{\text{SI}}$ pin. The $\overline{\text{CS}}$ pin must be driven low for the entire time of the instruction while data is being sent to the device. The $\overline{\text{CS}}$ pin must be driven low for the entire time of the instruction while data is being sent to the device. Please refer to [Figure 7-21](#) and [Figure 7-22](#).

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing wraps to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing wraps to the beginning of the page and overwrites previously sent data.

The $\overline{\text{CS}}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction is not executed. After $\overline{\text{CS}}$ is driven high, the self-timed Page Program instruction commences for a time duration of t_{pp} (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program

cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Figure 7-21. Page Program Instruction (SPI Mode)

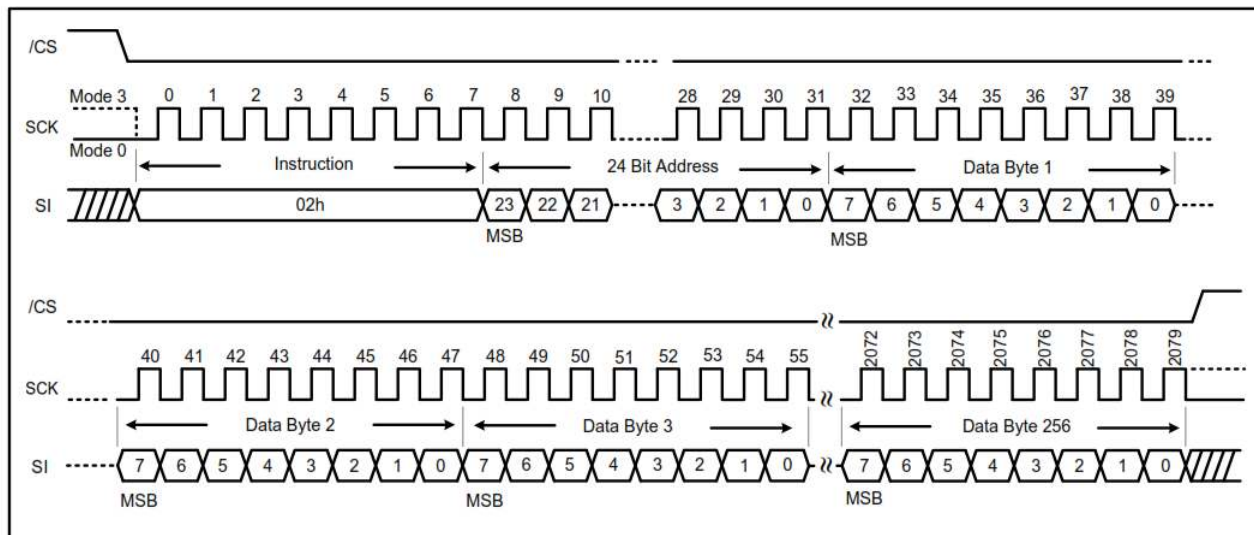
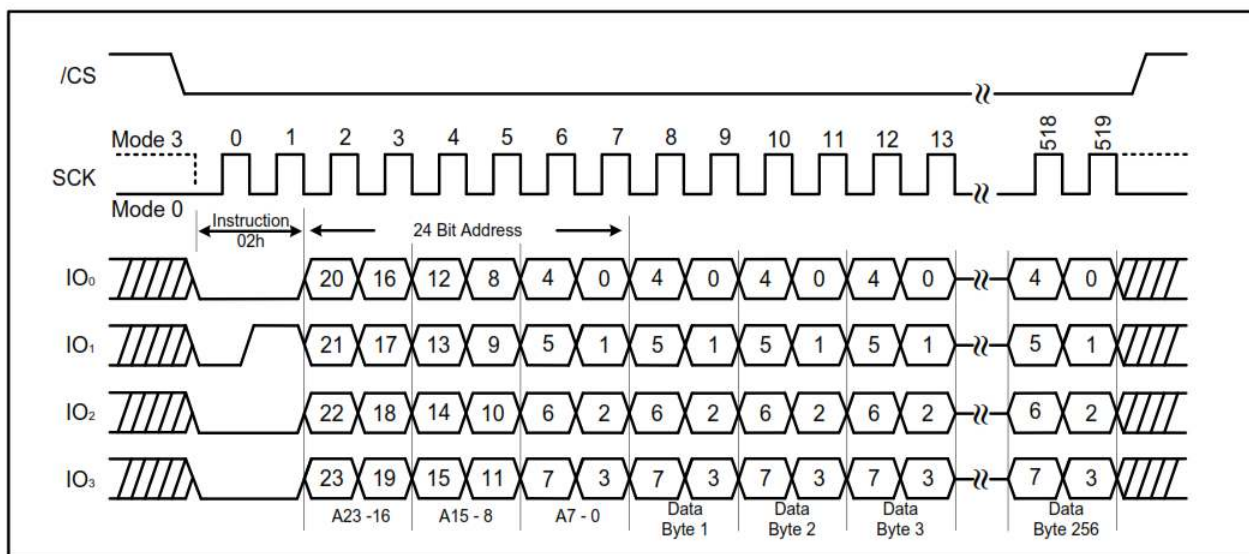


Figure 7-22. Page Program Instruction (QPI Mode)



7.16 Quad Page Program (33h)

The Quad Page Program instruction is used to program the memory to “0” at previously erased memory areas. The Quad Page Program uses four pins to transfer address and data: IO₀, IO₁, IO₂ and IO₃. This improves performance and data throughput of lower clock frequencies of less than 5MHz. Systems using faster clock speed will not get more benefit for the Quad Page Program as the required internal page program time is far more than the time required to clock data in.

To use Quad Page Program, the Quad Enable bit must be set, A Write Enable (06h) instruction must be executed before the device can accept the Quad Page Program instruction (Status Register-1, WEL = 1). The instruction is initiated by driving the $\overline{\text{CS}}$ pin low, then sending the instruction code 33h followed by a 24-bit address (A23 - A0) and at least one data, into the I/O pins. The $\overline{\text{CS}}$ pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are the same as the standard Page Program. Please

refer to Figure 7-23 and Figure 7-24.

Figure 7-23. Quad Page Program Instruction (SPI mode)

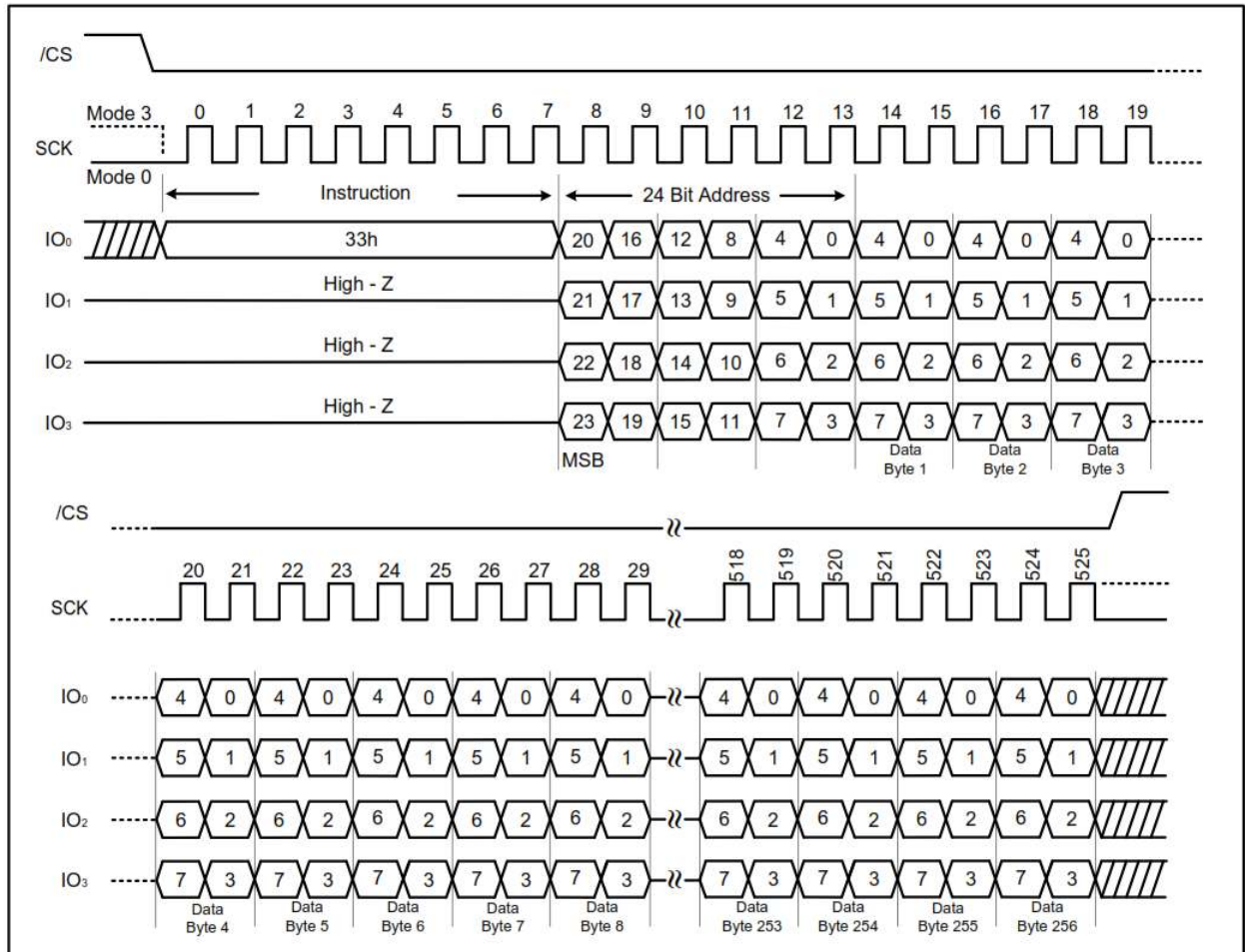
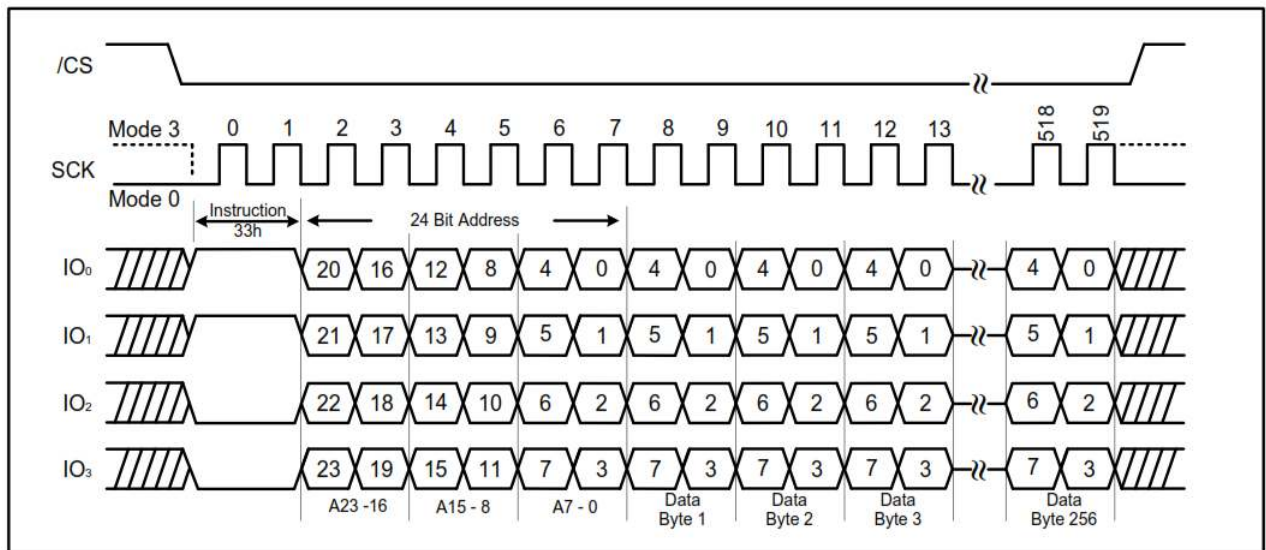


Figure 7-24. Quad Page Program Instruction (QPI mode)



7.17 4 KByte Block Erase (20h)

The Block Erase instruction is used to erase the data of the selected block by setting the memory locations to “1”. The instruction is used to erase a 4 KB block. Prior to the Block Erase Instruction, the Write Enable instruction must be issued. The instruction is initiated by driving the \overline{CS} pin low and shifting the instruction code 20h followed by a 24-bit block address (A23 - A0). (Please refer to Figure 7-25 and Figure 7-26).

The \overline{CS} pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction will not be executed. After \overline{CS} goes high, the self-timed Block Erase instruction commences for a time duration of t_{SE} (See AC Characteristics).

While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Figure 7-25. 4 KByte Block Erase Instruction (SPI Mode)

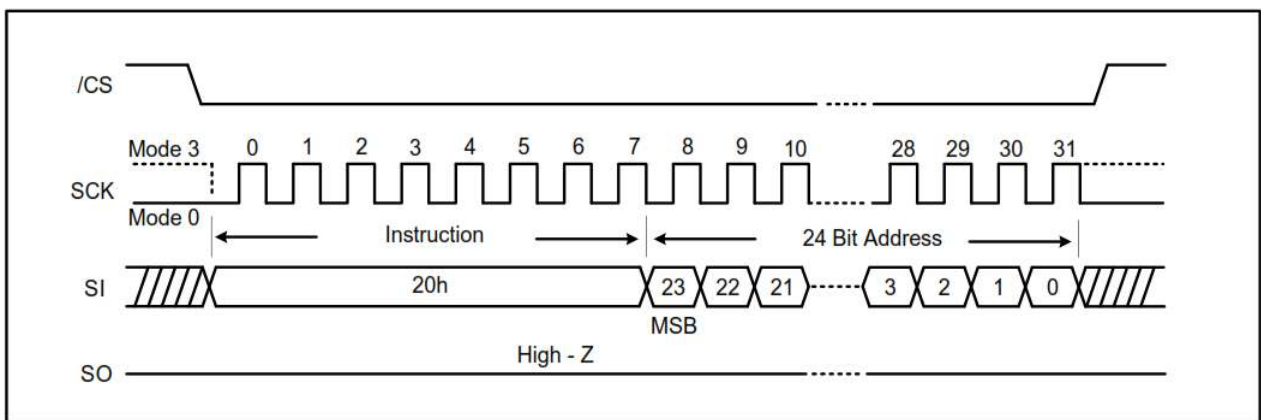
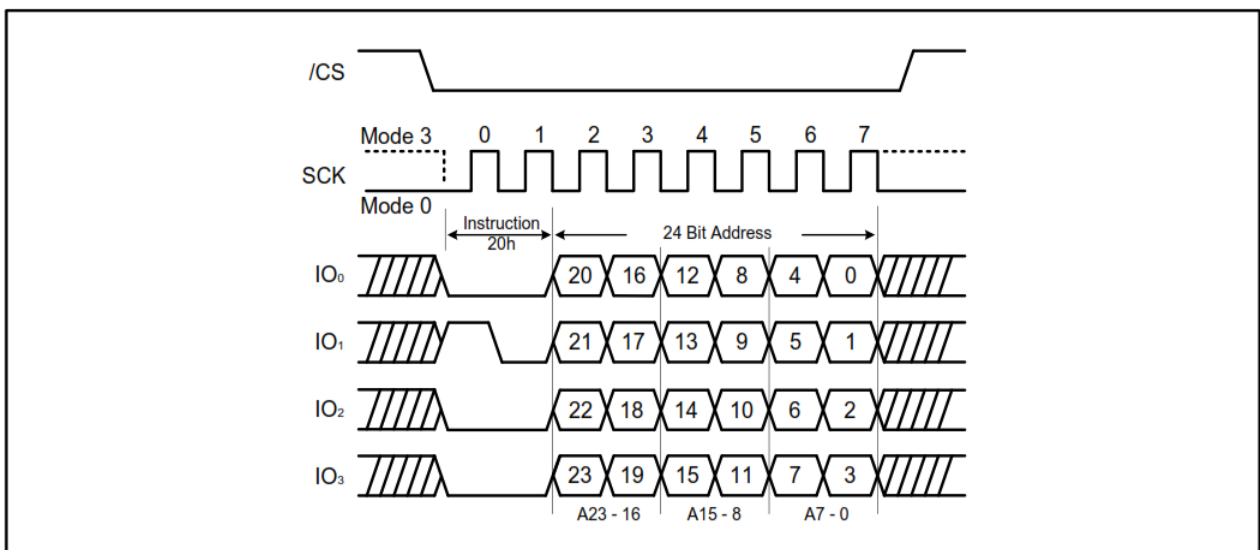


Figure 7-26. 4 KByte Block Erase Instruction (QPI Mode)



7.18 32 KByte Block Erase (52h)

The Block Erase instruction is used to erase the data of the selected block by setting the memory locations to “1”. The instruction is used for a 32 KB Block erase operation. Prior to the Block Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the \overline{CS} pin low and shifting the instruction code 52h followed by a 24-bit block address (A23 - A0). Please refer to [Figure 7-27](#) and [Figure 7-28](#).

The \overline{CS} pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction will not be executed. After \overline{CS} is driven high, the self-timed Block Erase instruction commences for a time duration of t_{BE1} . See AC Characteristics.

While the Block Erase cycle is in progress, the Read Status Register instruction may still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Figure 7-27. 32 KByte Block Erase Instruction (SPI Mode)

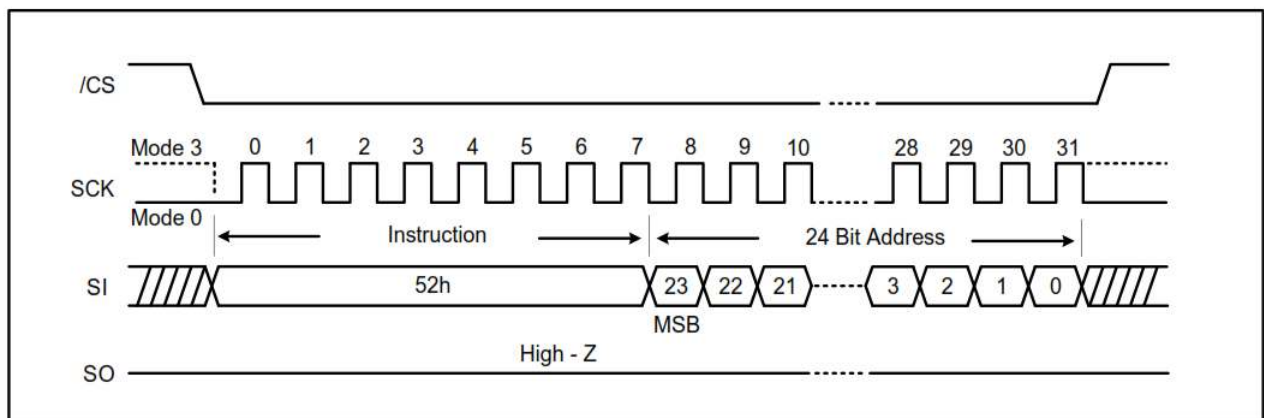
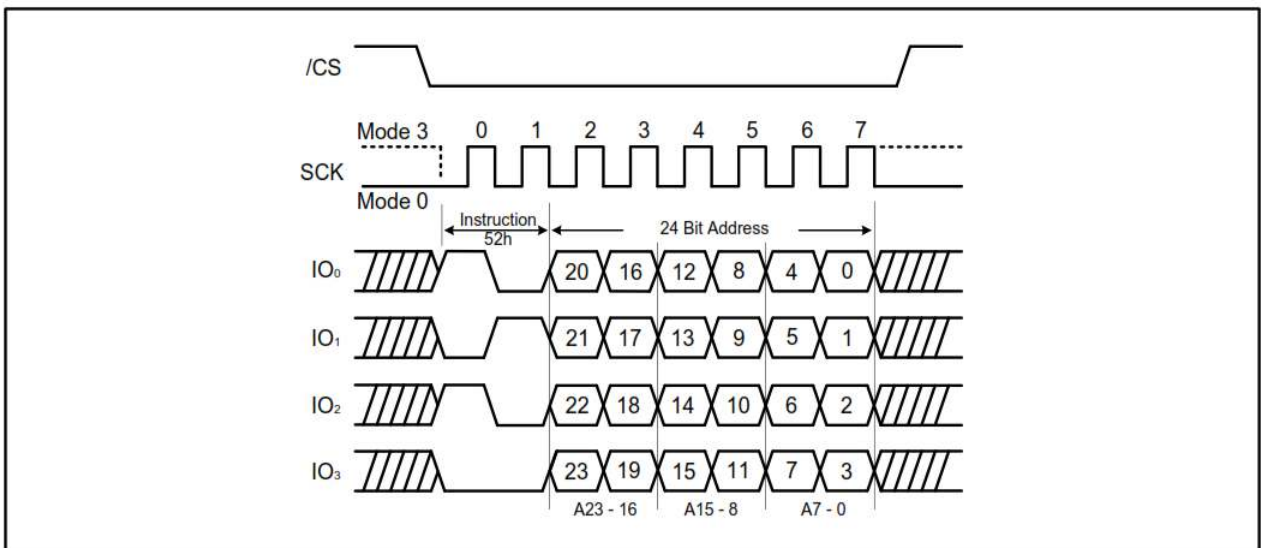


Figure 7-28. 32 KByte Block Erase Instruction (QPI Mode)



7.19 64 KByte Block Erase (D8h)

The Block Erase instruction is used to erase the data of a selected block by setting the memory locations of that block to “1”. The instruction is used for 64 KB block erase operation. Prior to the Block Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the \overline{CS} pin low and shifting the instruction code D8h followed by a 24-bit block address (A23 - A0). Please refer to [Figure 7-29](#) and [Figure 7-30](#).

The \overline{CS} pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction will not be executed. After \overline{CS} is driven high, the self-timed Block Erase instruction commences for a time duration of t_{BE2} (See AC Characteristics).

While the Block Erase cycle is in progress, the Read Status Register instruction may still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Figure 7-29. 64 KByte Block Erase Instruction (SPI Mode)

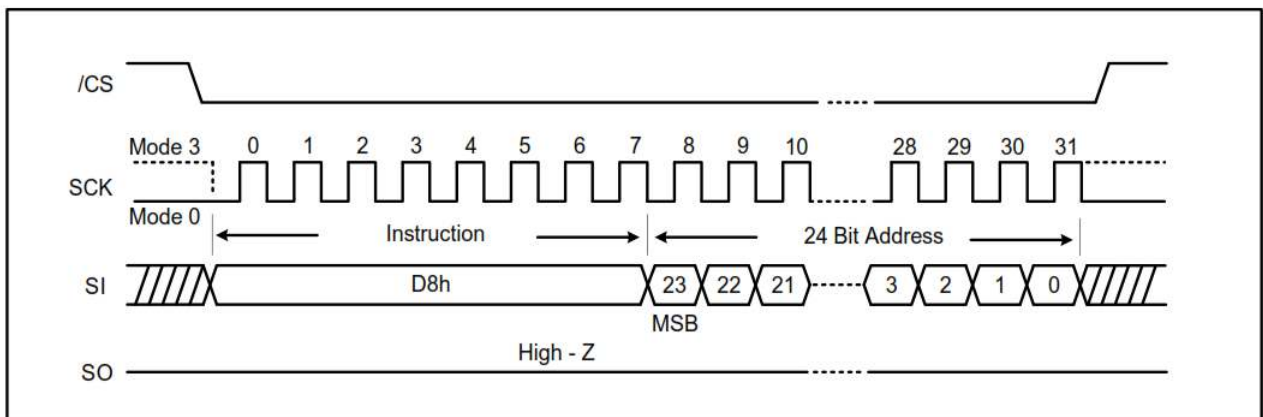
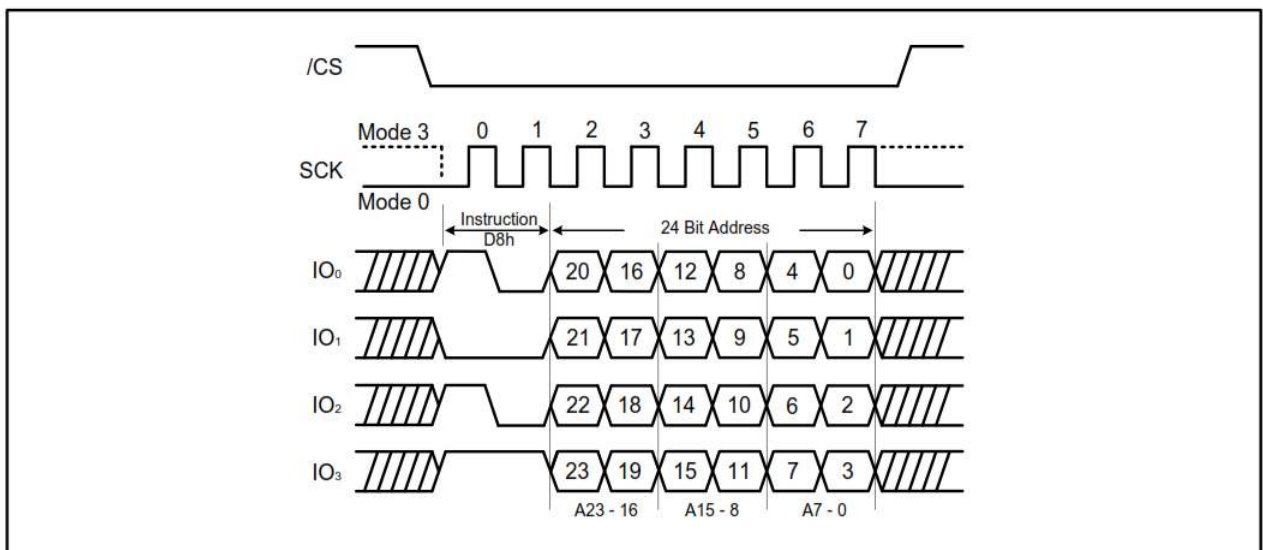


Figure 7-30. 64 KByte Block Erase Instruction (QPI Mode)



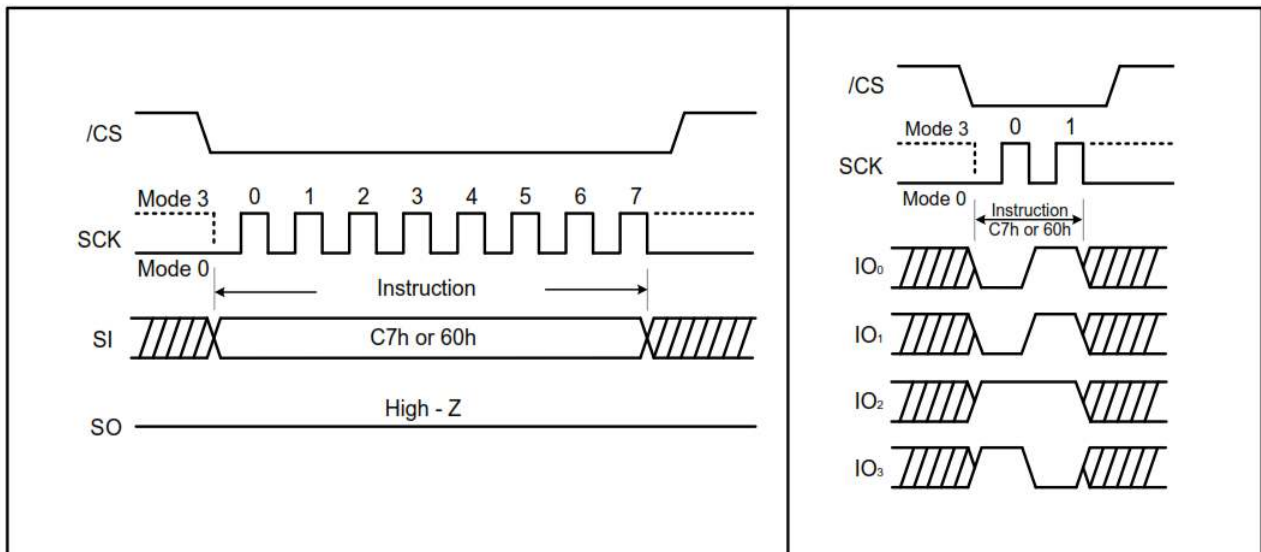
7.20 Chip Erase (C7h / 60h)

The Chip Erase instruction clears all bits in the device to FFh (all 1s). Prior to the Chip Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the $\overline{\text{CS}}$ pin low and shifting the instruction code C7h or 60h. Please refer to Figure 7-31.

The $\overline{\text{CS}}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Chip Erase instruction will not be executed. After $\overline{\text{CS}}$ is driven high, the self-timed Chip Erase instruction commences for a duration of t_{CE} (See AC Characteristics).

While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Figure 7-31. Chip Erase Instruction for SPI Mode (left) and QPI Mode (right)



7.21 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction allows the system to interrupt a Block Erase, Block Erase operation or a Page Program, Quad Data Input Page Program, Quad Page Program operation.

Erase Suspend is valid only during a Block Erase operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) instruction and Erase instructions (20h, 52h, D8h, C7h, 60h) are not allowed during an Erase Suspend. During the Chip Erase operation, the Erase Suspend instruction is ignored.

Program Suspend is valid only during the Page Program, Quad Data Input Page Program or Quad Page Program operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) instruction, Program instructions (02h and 33h) and Erase Instructions (20h, 52h, D8h, C7h, 60h) are not allowed during Program Suspend.

The Erase/Program Suspend instruction 75h is accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction is ignored by the device. A maximum of time of t_{SUS} (See AC Characteristics) is required to suspend the erase or program operation.

After executing the Erase/Program Suspend, the SUS bit in the Status Register is toggled from 0 to 1 immediately. The BUSY bit in the Status Register is cleared from 1 to 0 within t_{SUS} . For a previously resumed Erase/Program operation, it is also required that the Suspend instruction 75h is not issued earlier than a minimum of time of t_{SUS} following the preceding Resume instruction 7Ah.

Unexpected power-off during the Erase/Program suspend state resets the device and releases the suspend state. The SUS bit in the Status Register is also reset to 0. The data within the page or block that was being suspended may become corrupted. It is recommended for the user implement system design techniques to guard against the accidental power interruption and preserve data integrity during the erase/program suspend state. (Please refer to [Figure 7-32](#) and [Figure 7-33](#)).

Figure 7-32. Erase Suspend Instruction (SPI Mode)

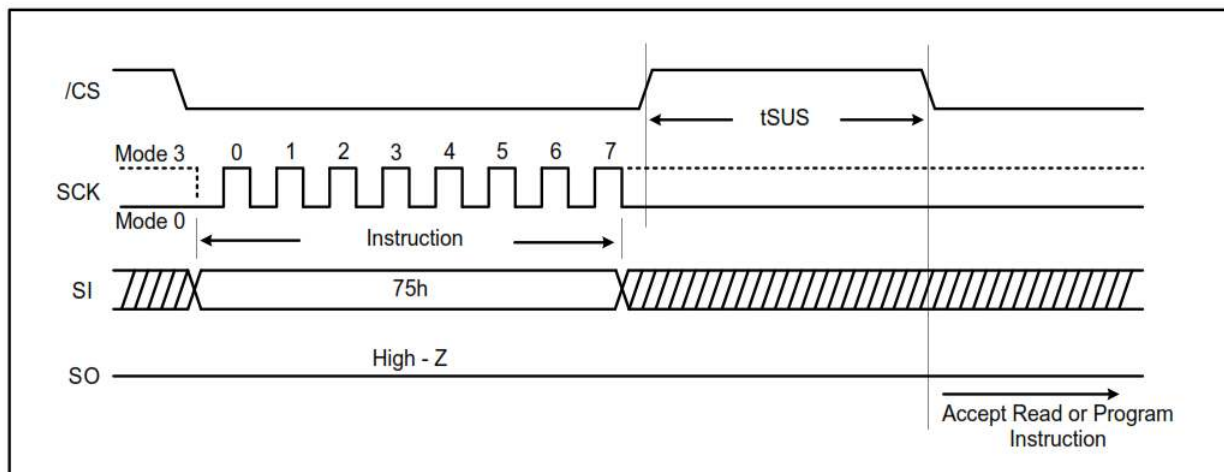
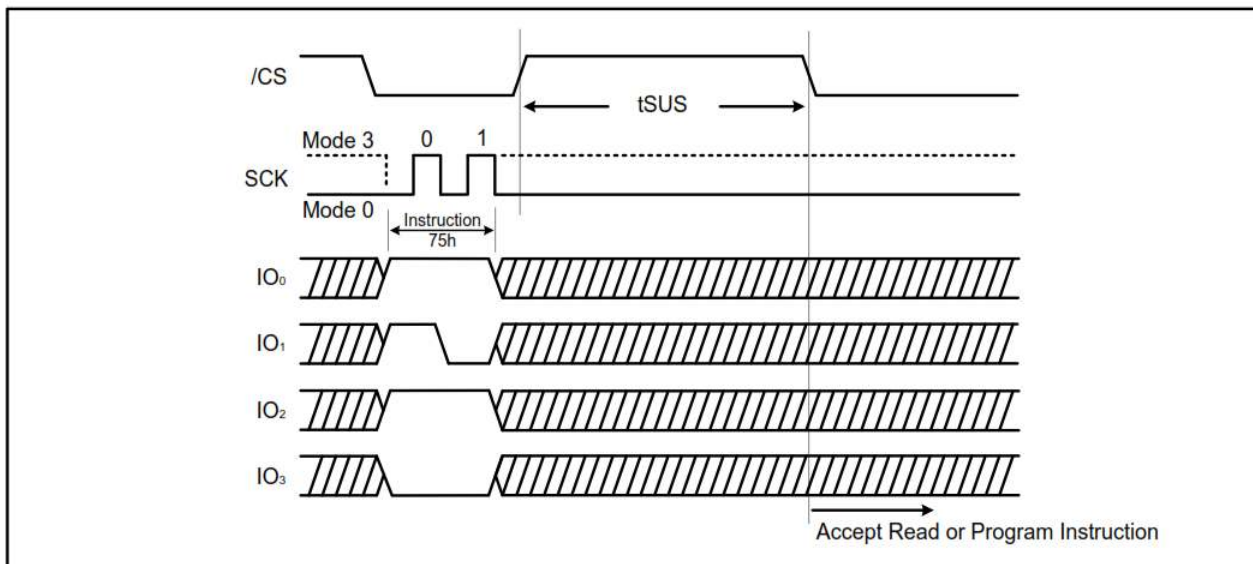


Figure 7-33. Erase Suspend Instruction (QPI Mode)



7.22 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction 7Ah is used to restart the Block Erase operation or the Page Program operation after an Erase/Program Suspend (75h). The Resume instruction 7Ah is accepted by the device only if the SUS bit in the Status Register is set and the BUSY bit is cleared. After the 7Ah instruction is issued, hardware clears the SUS bit immediately and sets the BUSY bit within 200ns. The block completes the erase operation or the page completes the program operation. If either the SUS bit is cleared or the BUSY bit is set, the Resume instruction 7Ah is ignored by the device.

The Resume instruction cannot be accepted if the previous Erase/Program Suspend operation was interrupted by unexpected power-off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of t_{SUS} following a previous Resume instruction. (Please refer to [Figure 7-34](#) and [Figure 7-35](#)).

Figure 7-34. Erase / Program Resume Instruction (SPI Mode)

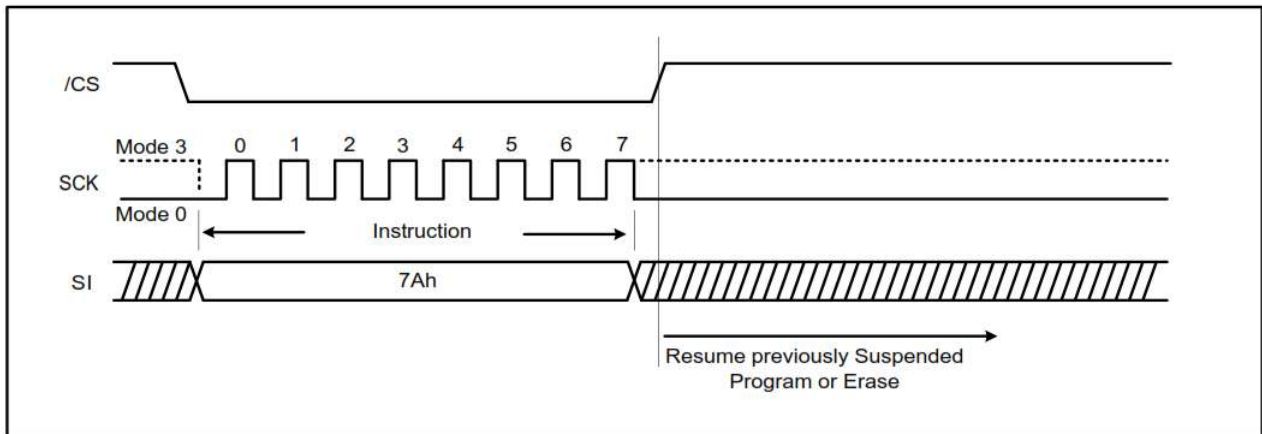
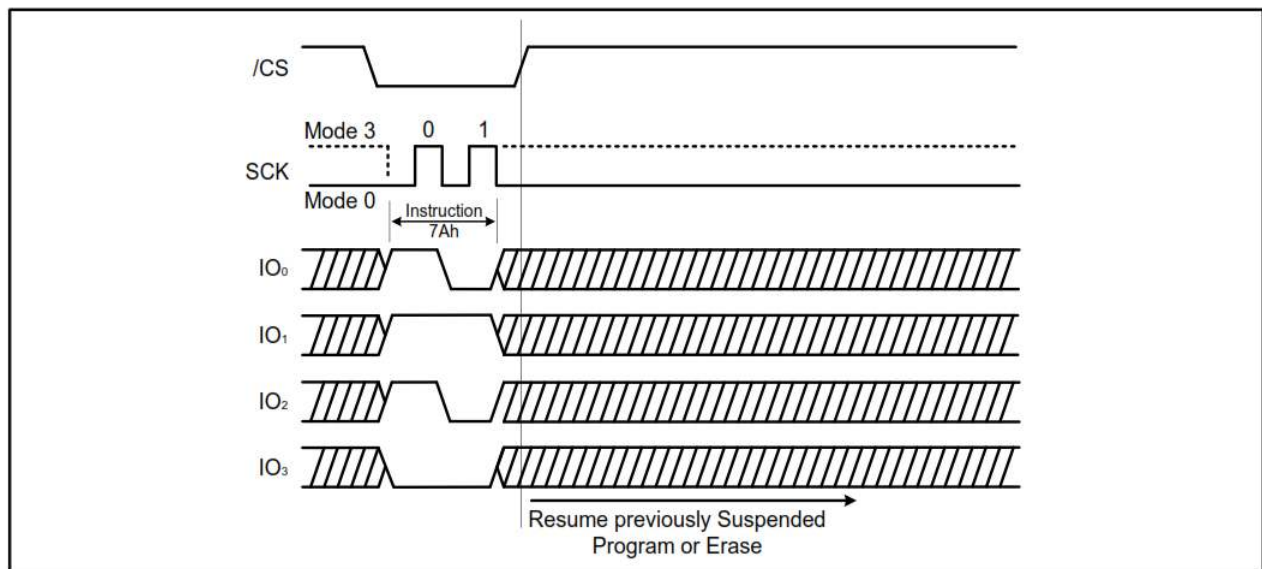


Figure 7-35. Erase / Program Resume Instruction (QPI Mode)



7.23 Deep Power Down (B9h)

Executing the Deep Power Down instruction is the best way to put the device in the lowest power consumption. The Deep Power Down instruction reduces the standby current (from I_{CC1} to I_{CC2} as specified in AC characteristics). The instruction is entered by driving the \overline{CS} pin low following execution of the B9h instruction. (Please refer to [Figure 7-36](#) and [Figure 7-37](#)).

The \overline{CS} pin must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the Deep Power Down instruction is not executed. After \overline{CS} goes high, it requires a delay of t_{DP} and the Deep Power Down mode is entered. While in the Deep Power Down mode, the Release Deep Power Down / Device ID instruction is used to restore the device to normal operation. All other instructions are ignored, including the Read Status Register instruction, which is always available during normal operation.

Figure 7-36. Deep Power Down Instruction (SPI Mode)

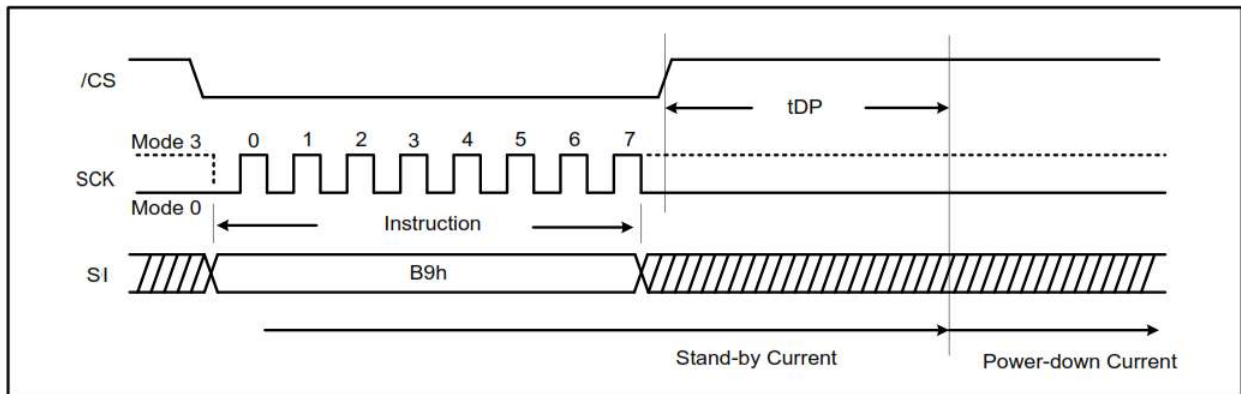
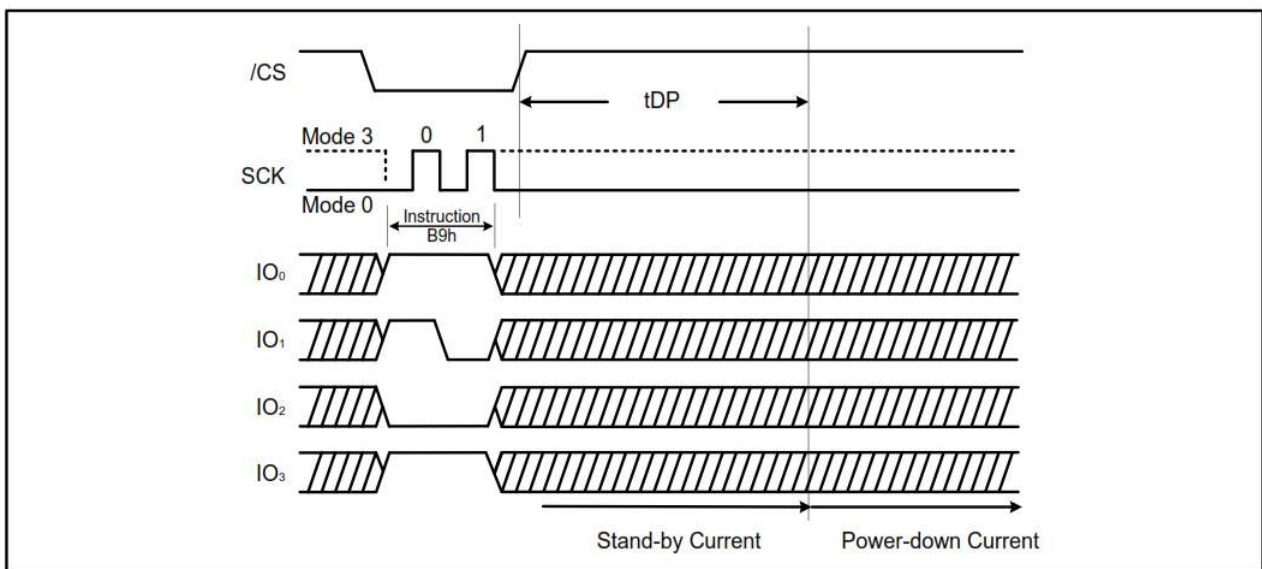


Figure 7-37. Deep Power Down Instruction (QPI Mode)



7.24 Release Deep Power Down / Device ID (ABh)

The Release Deep Power Down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Deep Power Down state or obtain the device identification (ID).

The instruction is issued by driving the $\overline{\text{CS}}$ pin low and driving a value of ABh onto the bus, then driving $\overline{\text{CS}}$ high as shown in Figure 7-38 and Figure 7-39. The Release from Deep Power Down instruction requires the time duration of t_{RES1} (See AC Characteristics) before accepting other instructions. The $\overline{\text{CS}}$ pin must keep high during the t_{RES1} time duration.

The Device ID can be read during SPI mode only. In other words, the Device ID feature is not available in QPI mode for the Release Deep Power Down/Device ID instruction. To obtain the Device ID in SPI mode, the instruction is initiated by driving the $\overline{\text{CS}}$ pin low and sending the instruction code ABh followed by 3-dummy bytes. The Device ID bits are then shifted on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 7-40. After $\overline{\text{CS}}$ is driven high it must keep high for a time duration of t_{RES2} (See AC Characteristics). The Device ID can be read continuously. The instruction is completed by driving $\overline{\text{CS}}$ high.

If the Release from Deep Power Down /Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and does not have any effect on the current cycle.

Figure 7-38. Release Power Down Instruction (SPI Mode)

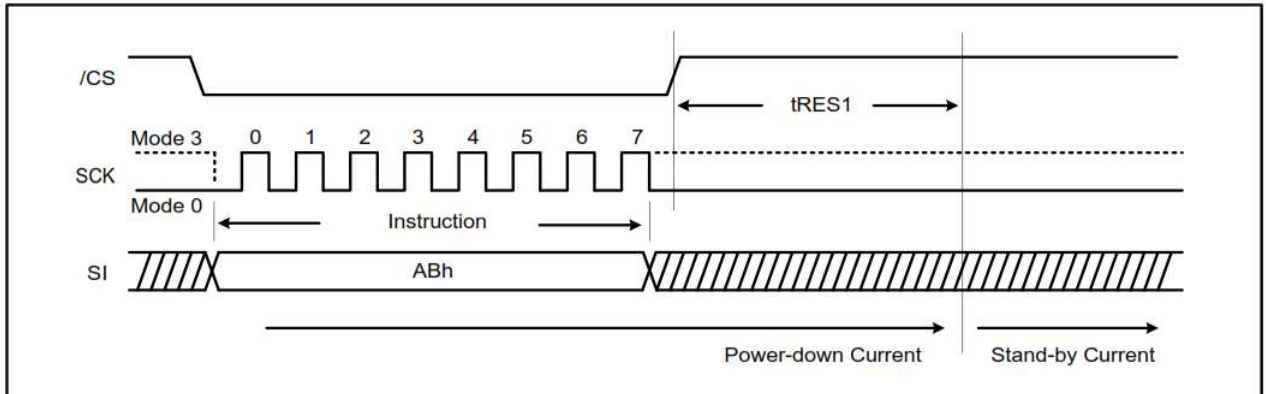


Figure 7-39. Release Power Down Instruction (QPI Mode)

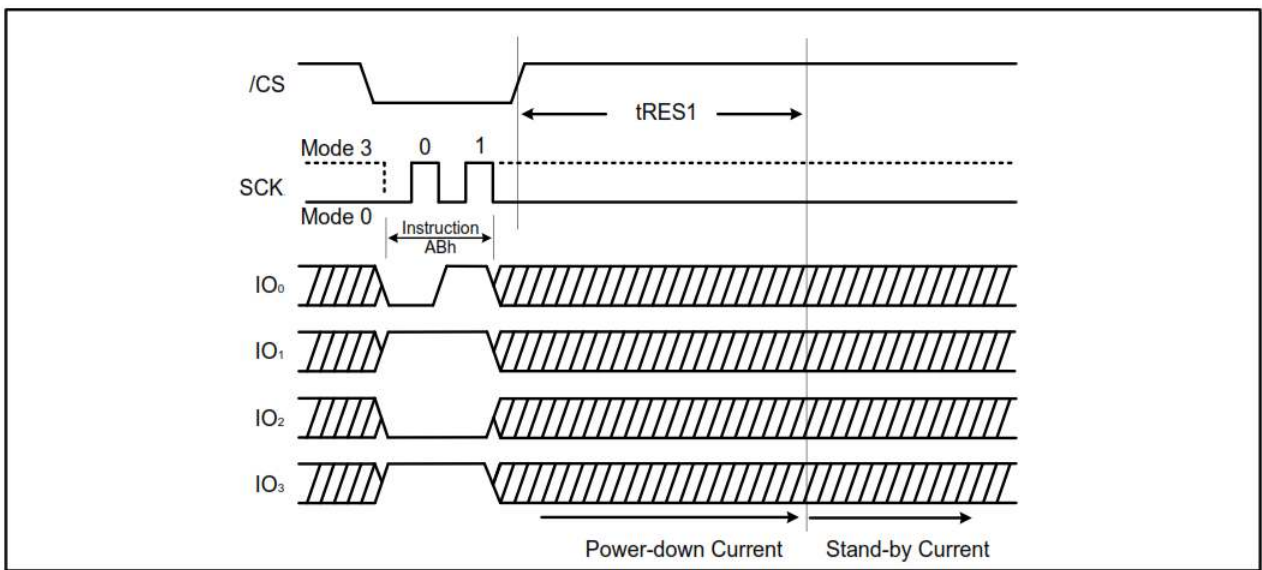
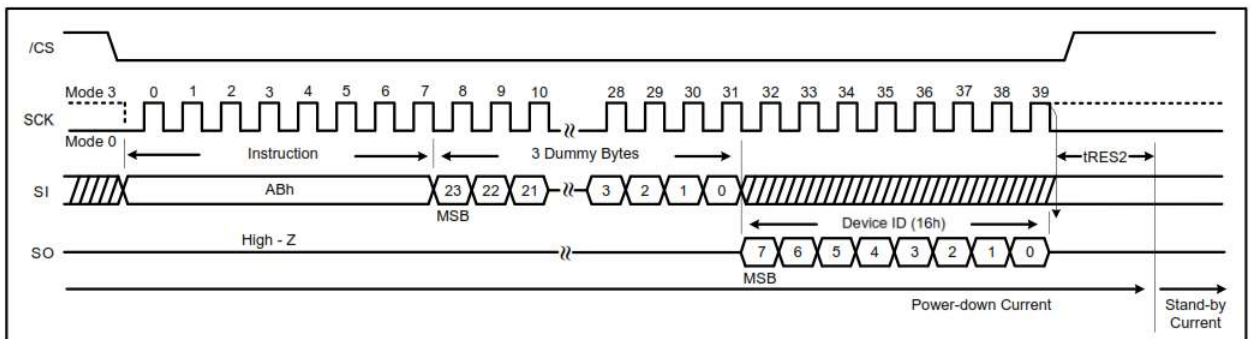


Figure 7-40. Release Power Down / Device ID Instruction (SPI Mode)



7.25 Read Manufacturer / Device ID (90h)

The Read Manufacturer/ Device ID instruction provides both the JEDEC assigned manufacturer ID and the specific device ID. This instruction can be issued in both SPI mode and QPI mode. In SPI mode, the 90h instruction is called a 1-1-1 transfer, where the instruction, address, and data are all driven on a single pin (SI for instruction and address, and SO for data). In QPI mode, the 90h instruction is called a 4-4-4 transfer, where the instruction, address, and data are driven on the bidirectional IO₀ - IO₃ pins.

Note that in QPI mode, the following events must occur in the order shown.

1. Set the QE bit in Status Register-2
2. Execute the QPI Enable (38h) instruction
3. Execute the 90h instruction

In SPI mode, the operation is initiated by driving the $\overline{\text{CS}}$ pin low and then driving the instruction code 90h onto the SI pin, followed by a 24-bit address (A23-A0) of 000000h. The 90h instruction requires 8 clocks to transfer, and the 24-bit address requires 24 clocks to transfer. The Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the SO pin on the falling edge of SCK with most significant bit (MSB) first. A minimum of 16 clocks are required to transfer the manufacturer and device ID information. If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{\text{CS}}$ high.

In QPI mode, the SI, SO, $\overline{\text{WP}}$, and $\overline{\text{HOLD}}$ pins are configured as bidirectional pins IO₀, IO₁, IO₂, and IO₃ respectively. The 90h operation the operation is initiated by driving the $\overline{\text{CS}}$ pin low and then driving the instruction code 90h onto the IO₀ - IO₃ pins, followed by a 24-bit address (A23-A0) of 000000h. The 90h instruction requires 2 clocks to transfer, and the 24-bit address requires 6 clocks to transfer. The Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the bidirectional IO₀ - IO₃ pins on the falling edge of SCK, with most significant bit (MSB) first. A minimum of 4 clocks are required to transfer the manufacturer and device ID information. If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving $\overline{\text{CS}}$ high.

Figure 7-41 shows the 90h command as executed in SPI mode. In this mode the instruction and address are driven on the SI pin.

Figure 7-42 shows the 90h command as executed in QPI mode. In this mode the instruction and address are driven on all four I/O pins.

Figure 7-41. Read Manufacturer/ Device ID Instruction (SPI Mode)

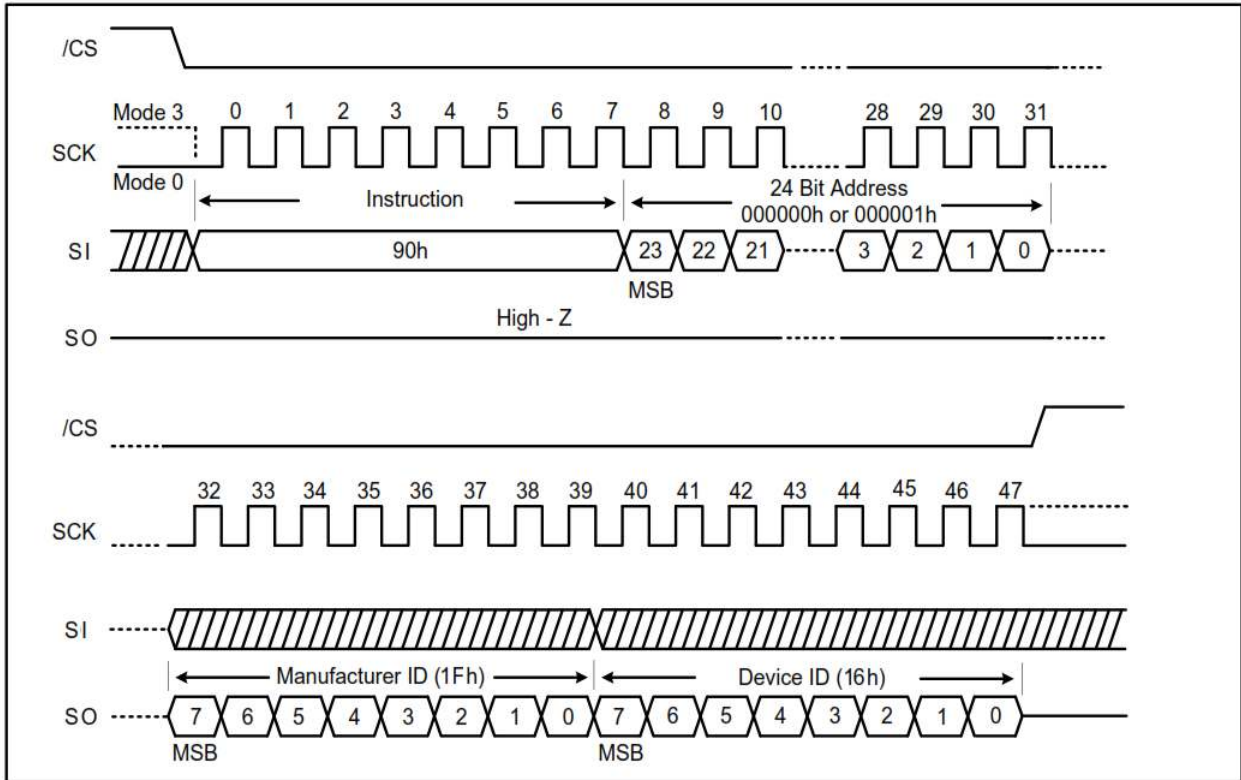
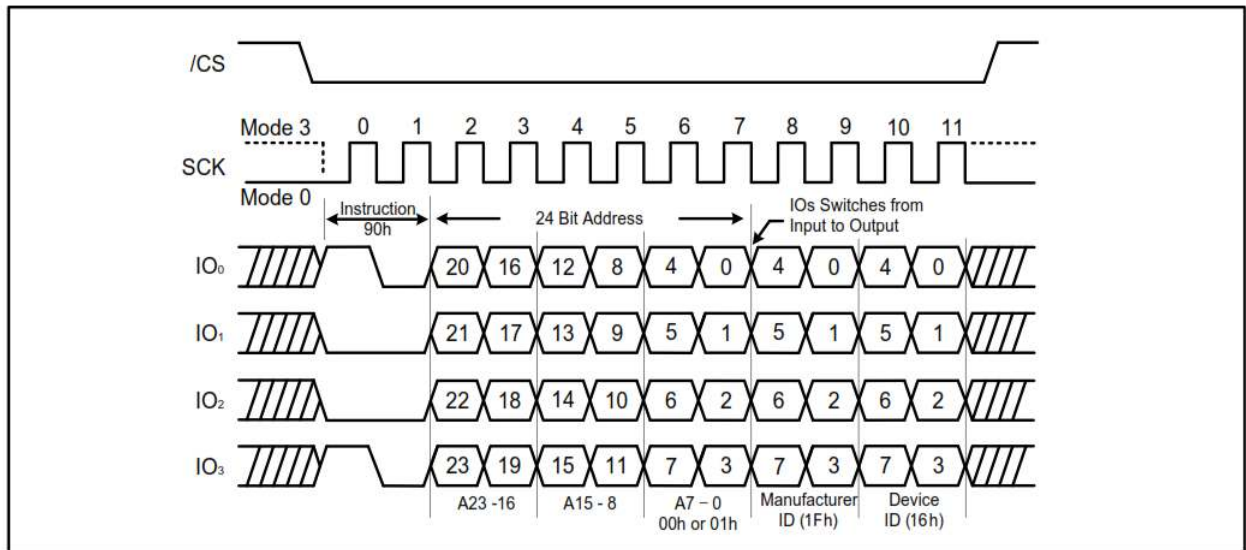


Figure 7-42. Read Manufacturer/ Device ID Instruction (QPI Mode)

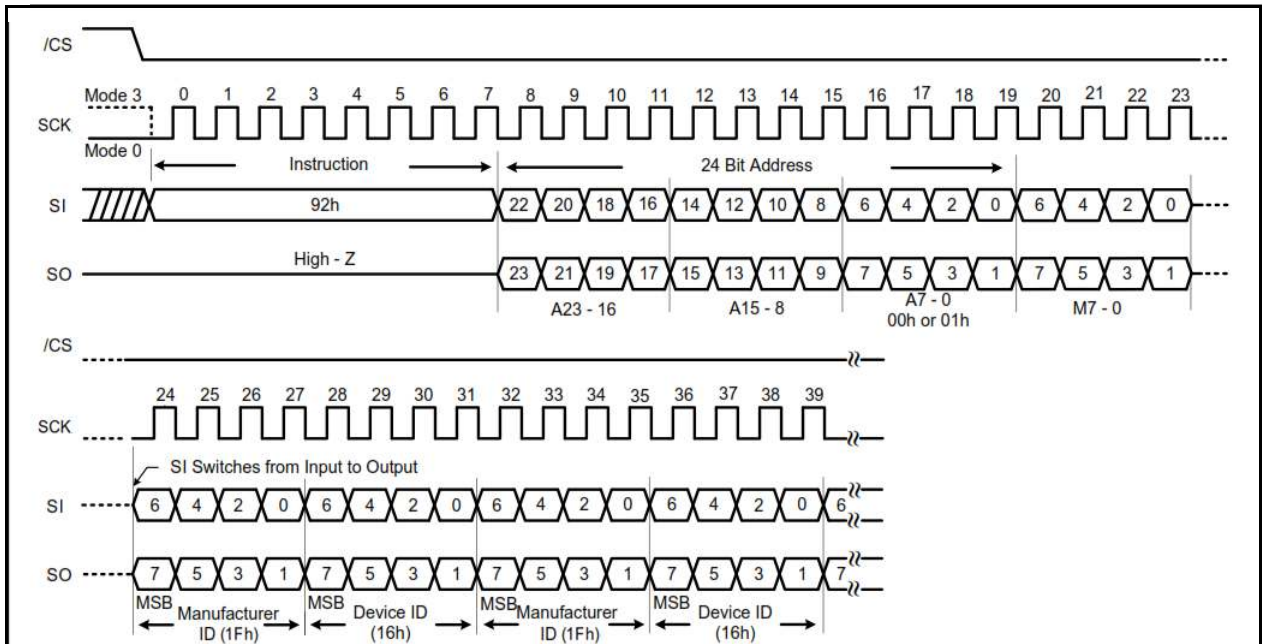


7.26 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer/ Device ID Dual I/O instruction provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID instruction is very similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the \overline{CS} pin low and shifting the instruction code 92h followed by a 24-bit address (A23-A0) of 000000h. The Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 7-43. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving \overline{CS} high.

Figure 7-43. Read Dual Manufacturer/ Device ID Dual I/O Instruction (SPI Mode)

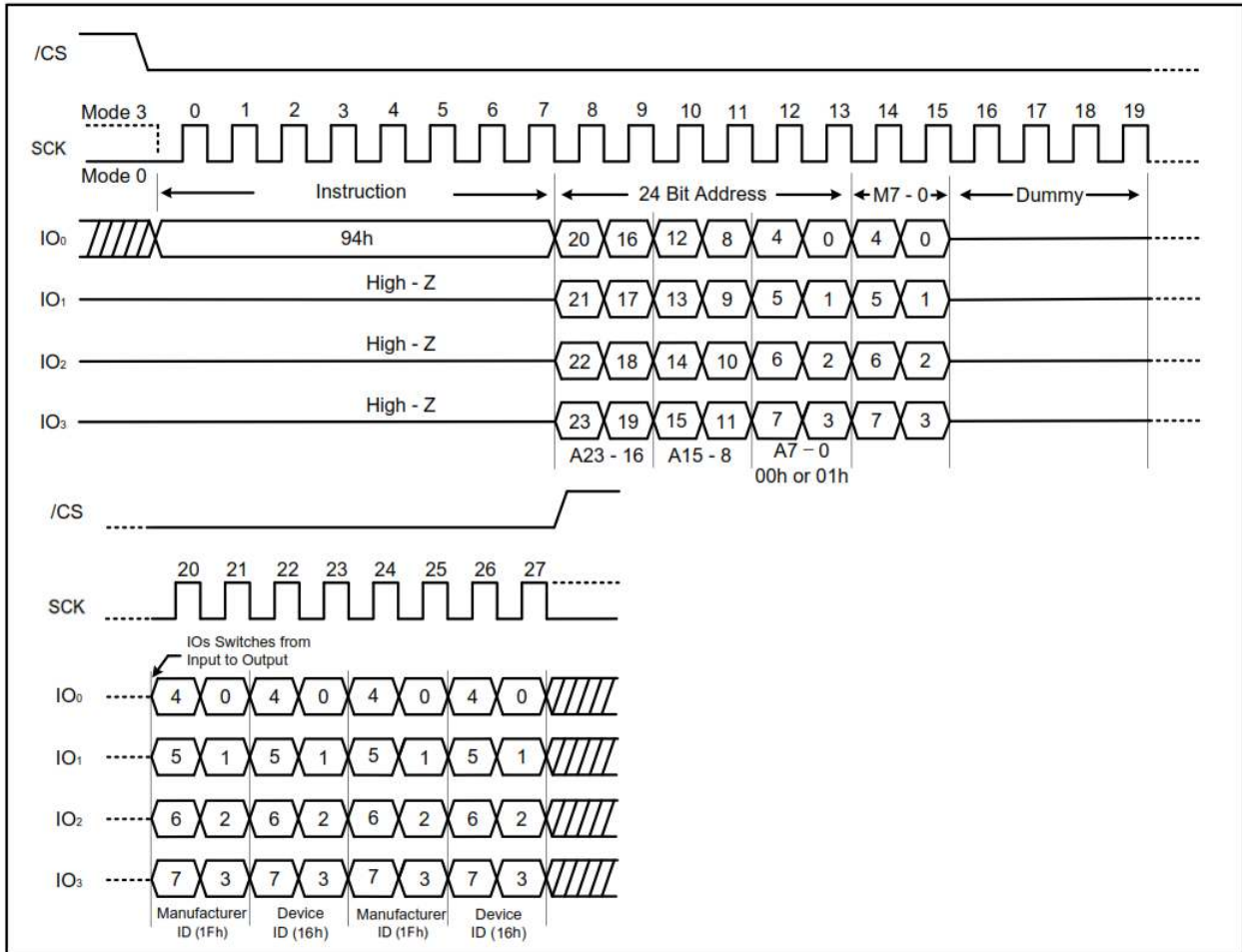


7.27 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer/ Device ID Quad I/O instruction provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID Quad I/O instruction is very similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the \overline{CS} pin low and shifting the instruction code 94h followed by a 24-bit address (A23-A0) of 000000h. The Manufacturer ID for Adesto (1Fh) and the Device ID (17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 7-44. If the 24-bit address is initially set to 000001h the Device ID is read first, followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving CS high.

Figure 7-44. Read Quad Manufacturer/ Device ID Quad I/O Instruction (SPI Mode)



7.28 JEDEC ID (9Fh)

For compatibility reasons, the AT25SL641 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is congruous with the JEDEC standard for SPI compatible serial flash memories that was adopted in 2003.

The instruction is entered by driving the $\overline{\text{CS}}$ pin low with following the instruction code “9Fh”. JEDEC assigned Manufacturer ID byte for Adesto (1Fh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of SCK with most significant bit (MSB) first shown in Figure 7-45 and Figure 7-46. For memory type and capacity values refer to Manufacturer and Device Identification table. The JEDEC ID can be read continuously. The instruction is terminated by driving $\overline{\text{CS}}$ high.

Figure 7-45. Read JEDEC ID Instruction (SPI Mode)

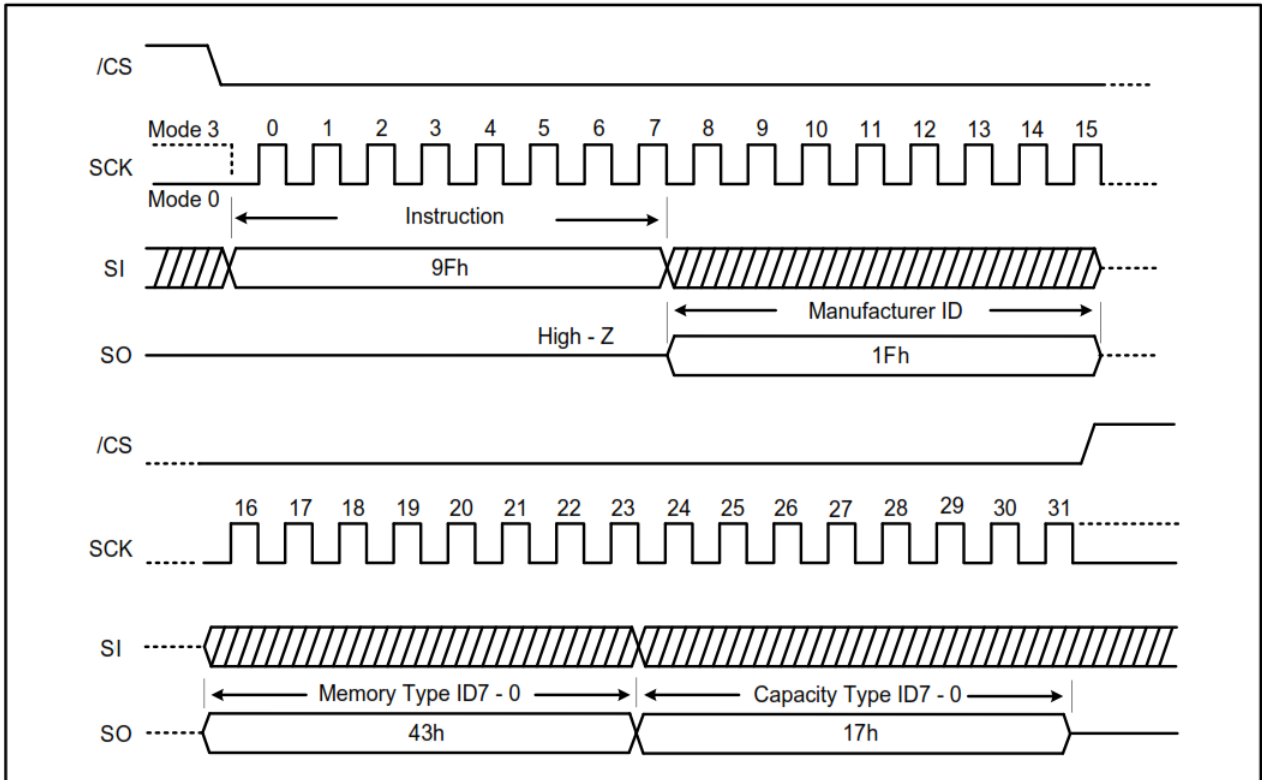
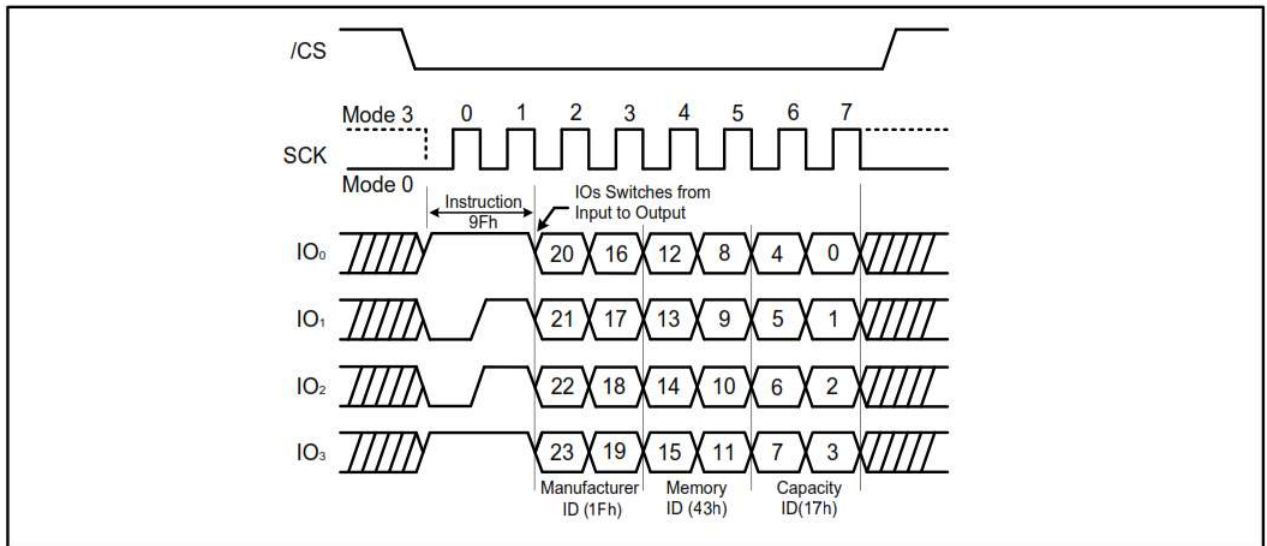


Figure 7-46. Read JEDEC ID Instruction (QPI Mode)



7.29 Enable QPI (38h)

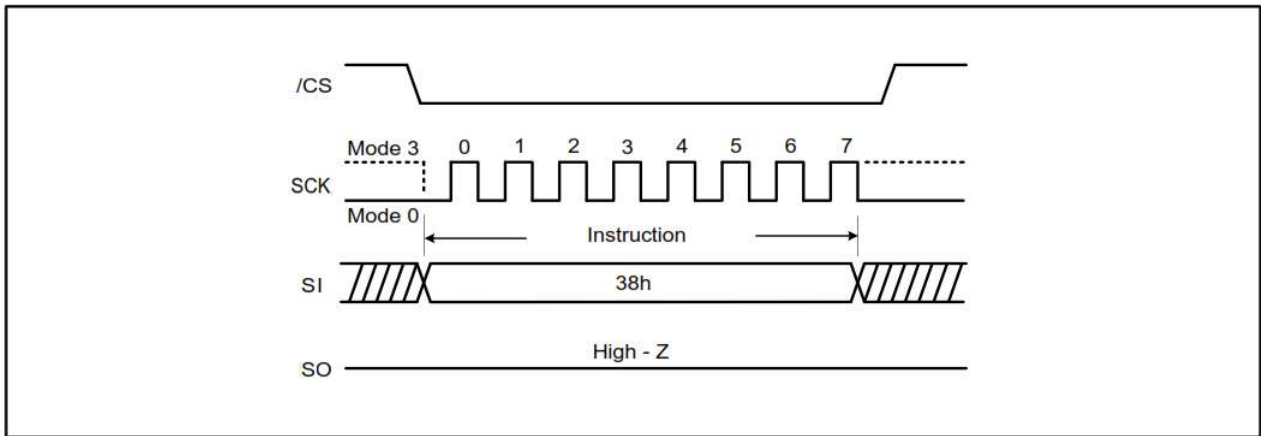
The AT25SL641 supports both the Standard/Dual/Quad Serial Peripheral interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. The Enable QPI instruction is used to switch the device from SPI mode to QPI mode.

To switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set, followed by an Enable QPI instruction. If the Quad Enable (QE) bit is 0, the Enable QPI instruction is ignored and the device remains in SPI mode.

After power-up, the default state of the device is SPI mode. See the instruction Set [Table 7-2](#) for all the commands supported in SPI mode and the instruction Set [Table 7-5](#) for all the instructions supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

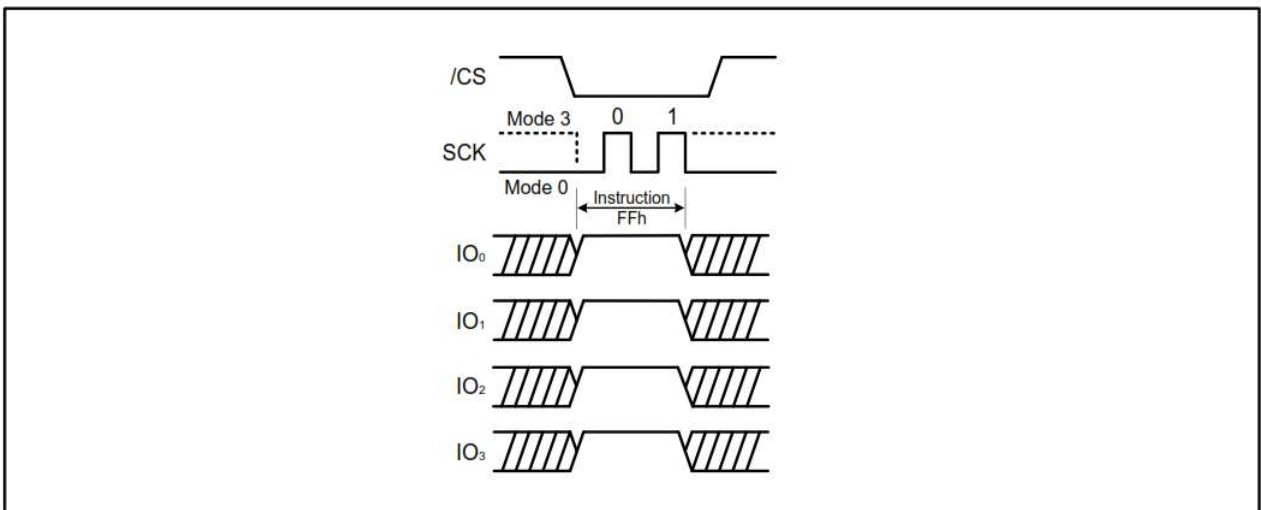
Figure 7-47. Enable QPI Instruction (SPI Mode only)



7.30 Disable QPI (FFh)

By issuing a Disable QPI (FFh) instruction, the device is reset back to SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length settings remains unchanged.

Figure 7-48. Disable QPI Instruction for QPI Mode



7.31 Word Read Quad I/O (E7h)

The Quad I/O dramatically reduces instruction overhead, allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O instruction. The lowest Address bit (A0) must equal 0 and only two dummy clocks are required prior to the data output.

Continuous Read Mode

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 7-49. The upper nibble of the (M7-4) controls the length of the next Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M[3:0]) are don't care ("X"). However, the I/O pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits $M[7-4] = Ah$, then the next Fast Read Quad I/O instruction (after \overline{CS} is raised and then lowered) does not require the E7h instruction code, as shown in Figure 7-50. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after \overline{CS} is asserted low. If the Continuous Read Mode bits $M[7:4]$ do not equal to Ah (1,0,1,0) the next instruction (after \overline{CS} is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 7-49. Word Read Quad I/O Instruction (Initial instruction or previous set $M7-0 \neq Ah$, SPI Mode)

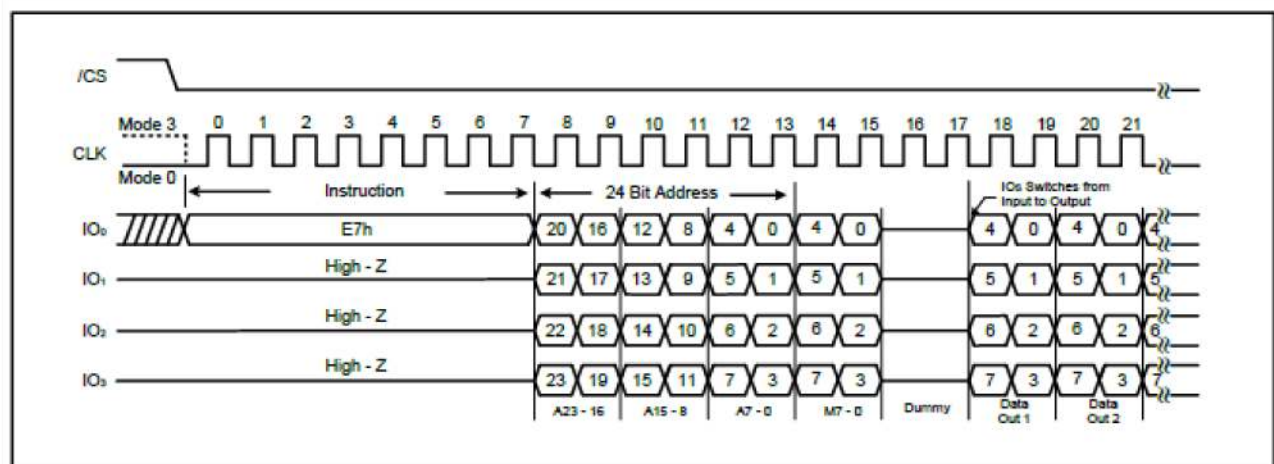
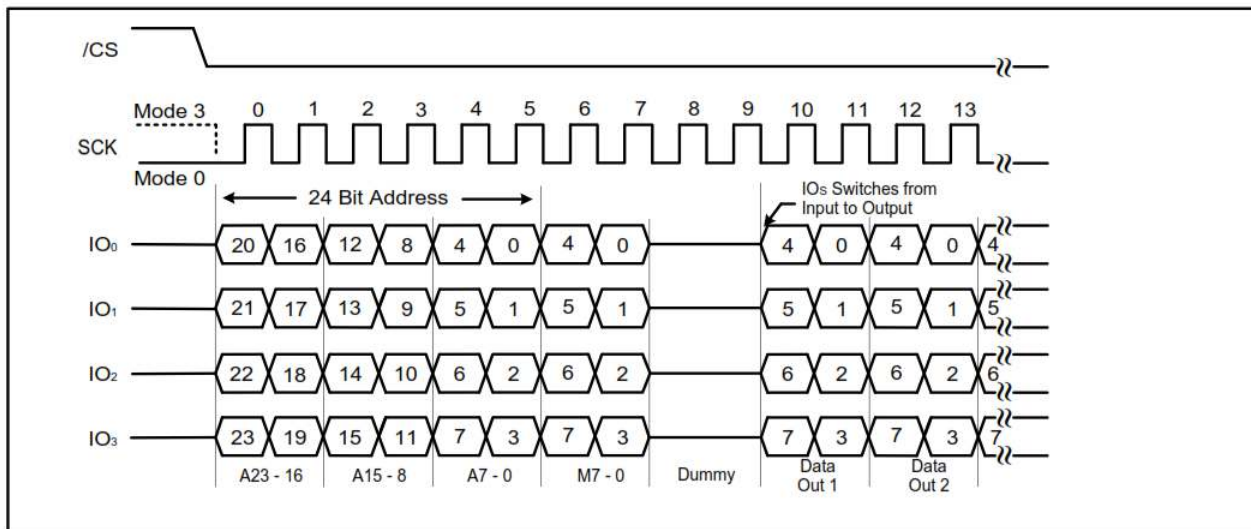


Figure 7-50. Word Read Quad I/O Instruction (Previous instruction set M7-0 = Axh, SPI Mode)



Wrap Around in SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) instruction prior to E7h. The Set Burst with Wrap instruction can either enable or disable the Wrap Around feature for the following E7h commands. When Wrap Around is enabled, the output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until \overline{CS} is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing read instructions.

The Set Burst with Wrap instruction allows three wrap bits, W6-4, to be set. The W4 bit is used to enable or disable the Wrap Around operation, while W6-5 is used to specify the length of the wrap around section within a page.

7.32 Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) instruction is used in conjunction with Fast Read Quad I/O and Word Read Quad I/O instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance. Before the device accepts the Set Burst with Wrap instruction, a Quad enable of Status Register-2 must be executed (Status Register bit QE must equal 1).

The Set Burst with Wrap instruction is initiated by driving the \overline{CS} pin low and then shifting the instruction code 77h followed by 24 dummy bits and 8 wrap bits, W7 - W0. The instruction sequence is shown in Set Burst with Wrap Instruction Sequence. Wrap bit W7 and W3-0 are not used.

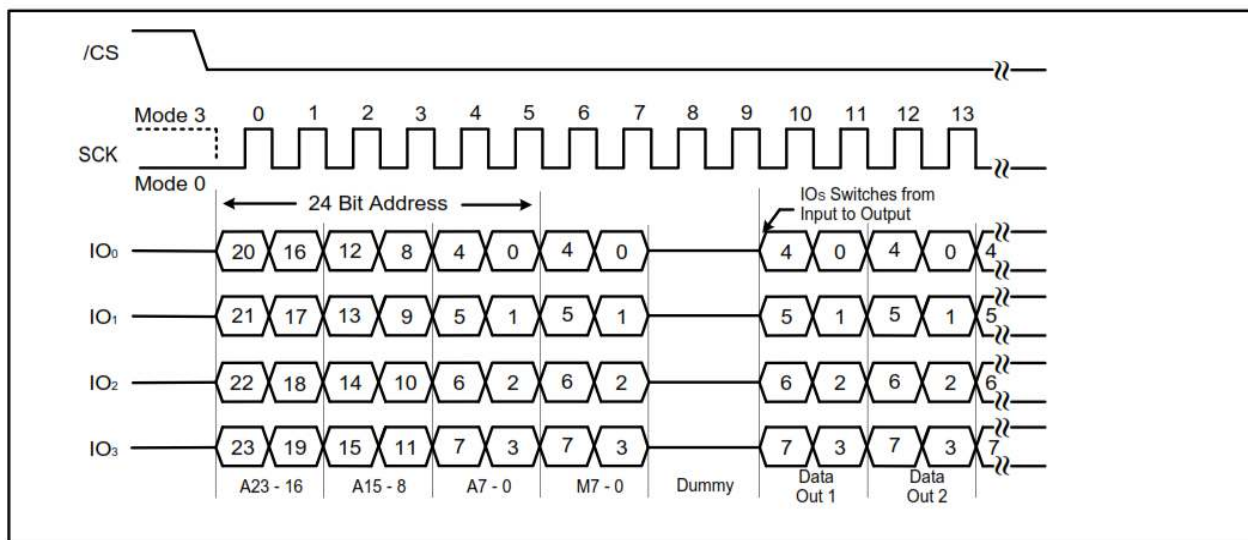
Table 7-8. Encoding of W6 - W4 Wrap Bits

| W6, W5 | W4 = 0 | | W4 = 1(Default) | |
|--------|-------------|-------------|-----------------|-------------|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 00 | Yes | 8-byte | No | N/A |
| 01 | Yes | 16-byte | No | N/A |
| 10 | Yes | 32-byte | No | N/A |
| 11 | Yes | 64-byte | No | N/A |

Once W6-4 is set by a Set Burst with Wrap instruction, all the following Fast Read Quad I/O and Word Read Quad I/O instructions use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the Wrap Around function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1.

The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction or Reset (99h) instruction to reset W4 = 1 prior to any normal Read instructions since the AT25SL641 does not have a hardware reset pin.

Figure 7-51. Set Burst with Wrap Instruction Sequence

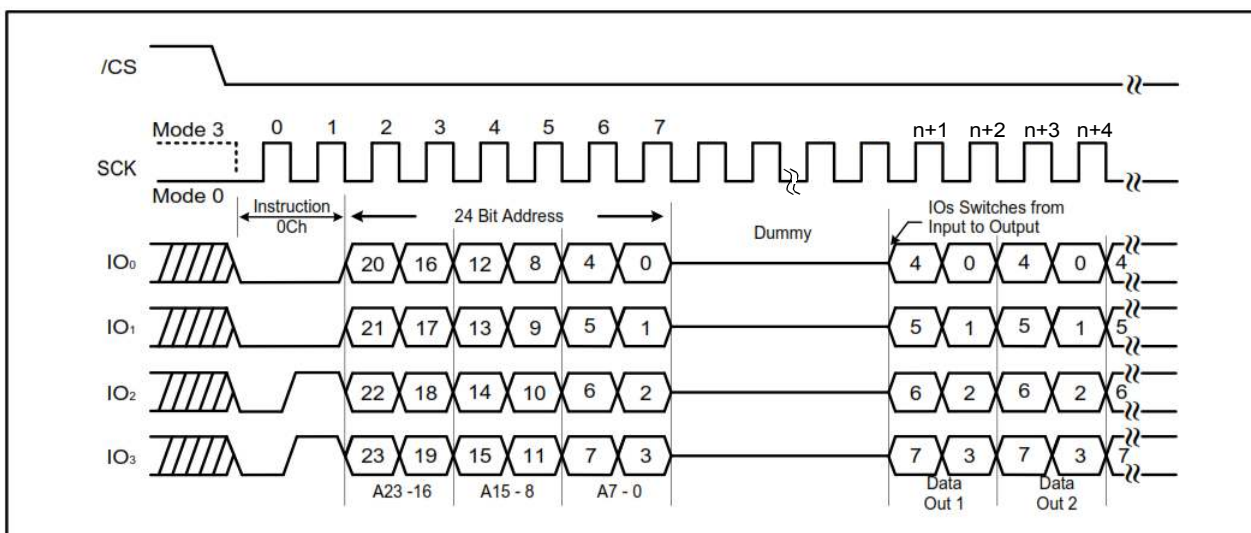


7.33 Burst Read with Wrap (0Ch)

The Burst Read with Wrap (0Ch) instruction provides an alternative way to perform the read operation with Wrap Around in QPI mode. The instruction is similar to the Fast Read (0Bh) instruction in QPI mode, except the addressing of the read operation wraps around to the beginning boundary of the wrap length once the ending boundary is reached.

The number of dummy clock cycles can be configured as either 4, 6 or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command as shown in [Table 7-6, Encoding of P\[5:4\] Bits](#).

Figure 7-52. Burst Read with Wrap Instruction (QPI Mode)



7.34 Enable Reset (66h) and Reset (99h)

For eight-pin packages, the AT25SL641 provide a software Reset instruction (99h) instead of a dedicated RESET pin.

Once the Reset instruction is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting, Read parameter setting and Wrap bit setting.

The Enable Reset (66h) and Reset (99h) instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. The execution of any instruction other than Reset (99h) after the Reset Enable (66h) instruction is executed disables the reset enable state. A new sequence of Enable Reset (66h) and Reset (99h) would then be required to reset the device. Once the Reset instruction is accepted by the device, it takes approximately $t_{RST} = 30\mu s$ to reset. During this period, no instruction is accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

Figure 7-53. Enable Reset and Reset Instruction (SPI Mode)

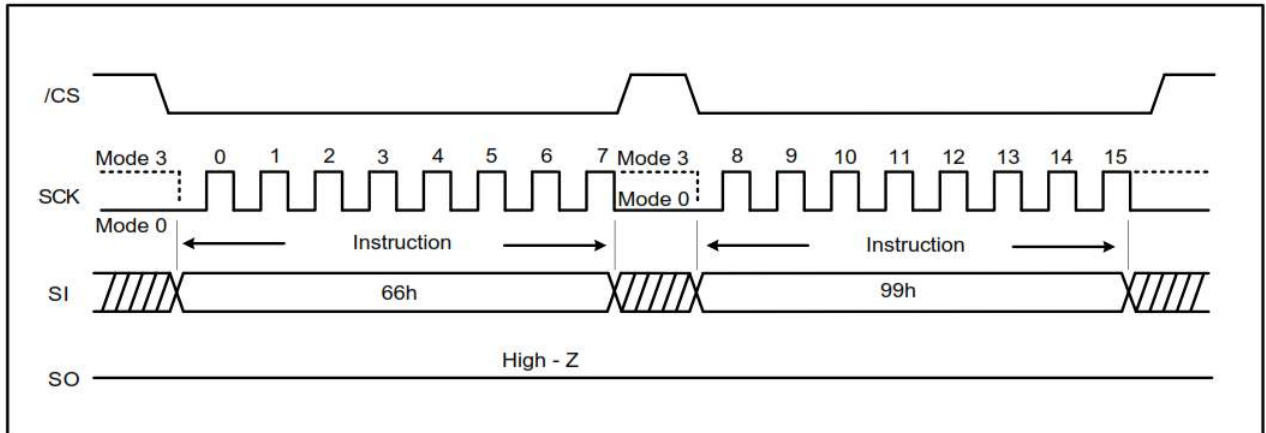
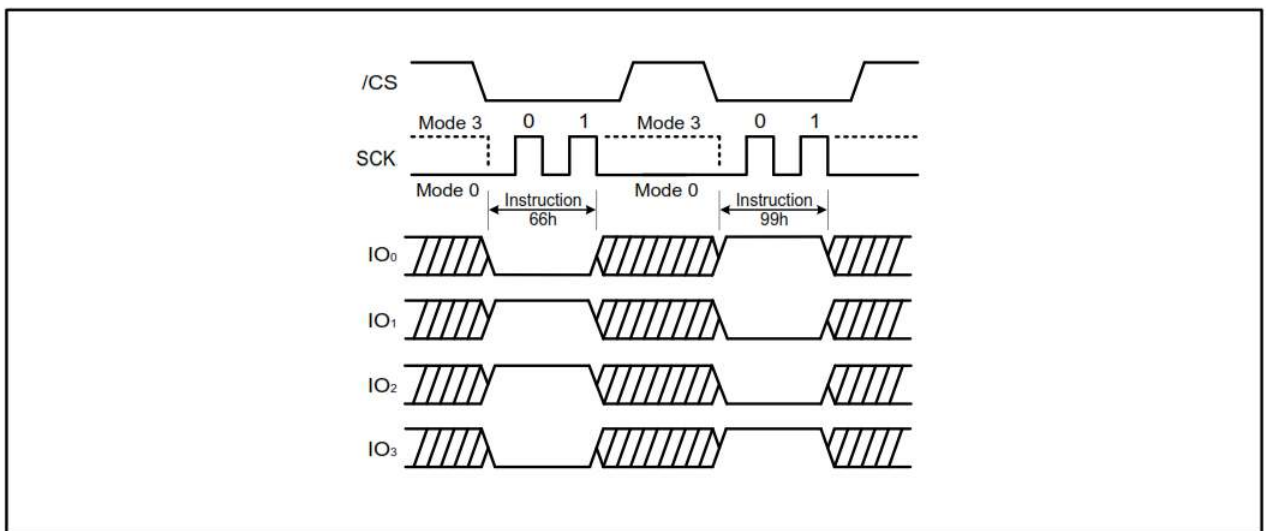


Figure 7-54. Enable Reset and Reset Instruction (QPI Mode)



7.35 Read Serial Flash Discovery Parameter (5Ah)

The Read Serial Flash Discovery Parameter (SFDP) instruction allows reading the Serial Flash Discovery Parameter area (SFDP). This SFDP area is composed of 2048 read-only bytes containing operating characteristics and vendor specific information. The SFDP area is factory programmed. If the SFDP area is blank, the device is shipped with all the SFDP bytes at FFh. If only a portion of the SFDP area is written to, the portion not used is shipped with bytes in erased state (FFh).

The instruction sequence for the read SFDP has the same structure as that of a Fast Read instruction. First, the device is selected by driving Chip Select (\overline{CS}) low. Next, the 8-bit instruction code (5Ah) and the 24-bit address are shifted in, followed by 8 dummy clock cycles. The bytes of SFDP content are shifted out on the Serial Data Output (SO) starting from the specified address. Each bit is shifted out during the falling edge of Serial Clock (SCK). The instruction sequence is shown here. The Read SFDP instruction is terminated by driving Chip Select (\overline{CS}) High at any time during data output.

Figure 7-55. Read SFDP Register Instruction

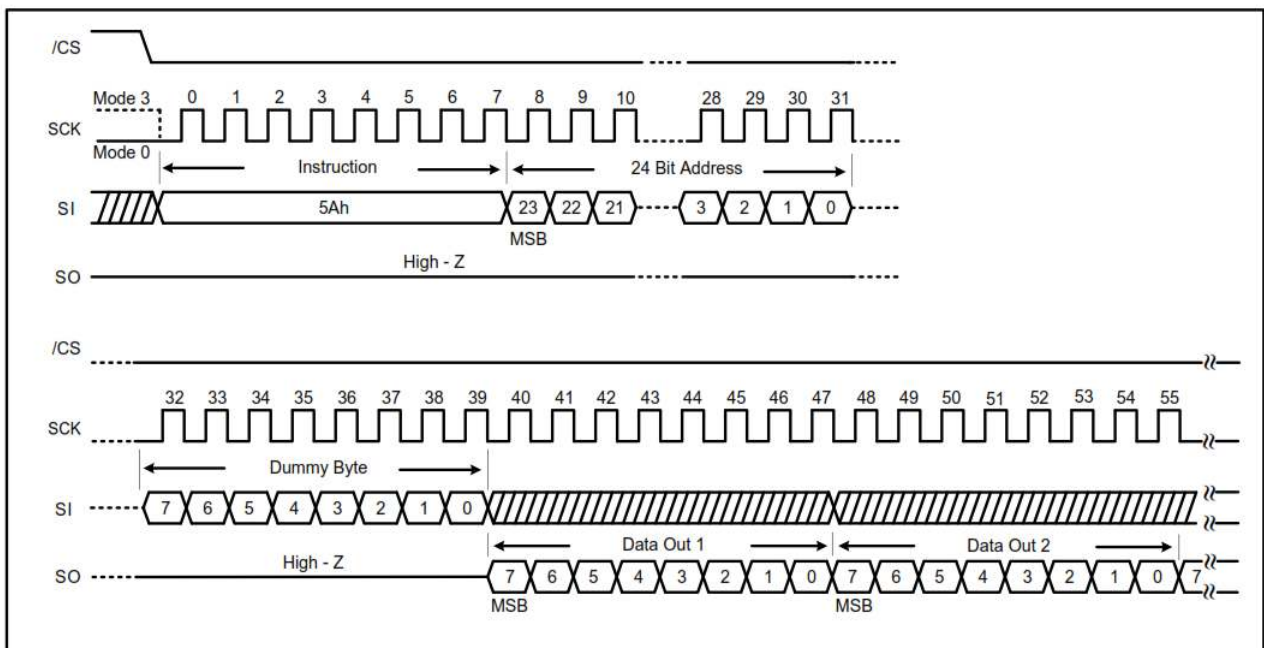


Table 7-9. SFDP Signature and Headers

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|------------------------------|----------------|------------------|---------------|----------------|-----------------|
| SFDP Signature | | 00h | 07:00 | 0101 0011 | 53h |
| | | 01h | 15:08 | 0100 0110 | 46h |
| | | 02h | 23:16 | 0100 0100 | 44h |
| | | 03h | 31:24 | 0101 0110 | 50h |
| SFDP Minor Revision | Start from 00h | 04h | 07:00 | 0000 0110 | 06h |
| SFDP Major Revision | Start from 01h | 05h | 15:08 | 0000 0001 | 01h |
| Number of Parameters Headers | Start from 00h | 06h | 23:16 | 0000 0001 | 01h |

Table 7-9. SFDP Signature and Headers

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|---------------------------------------|--|------------------|---------------|----------------|-----------------|
| Reserved | FFh | 07h | 31:24 | 1111 1111 | FFh |
| JEDEC Parameter ID (LSB) | JEDEC Parameter ID (LSB) = 00h | 08h | 07:00 | 0000 0000 | 00h |
| Parameter Table Minor Revision | Start from 00h | 09h | 15:08 | 0000 0110 | 06h |
| Parameter Table Major Revision | Start from 01h | 0Ah | 23:16 | 0000 0001 | 01h |
| Parameter Table Length (double words) | How many DWORDs in the parameter table | 0Bh | 31:24 | 0001 0000 | 10h |
| Parameter Table Pointer | Address of Adesto Parameter Table | 0Ch | 07:00 | 0011 0000 | 30h |
| | | 0Dh | 15:08 | 0000 0000 | 00h |
| | | 0Eh | 23:16 | 0000 0000 | 00h |
| JEDEC Parameter ID (MSB) | JEDEC Parameter ID (MSB):FFh | 0Fh | 31:24 | 1111 1111 | FFh |
| JEDEC Parameter ID (LSB) | Adesto Manufacturer ID | 10h | 07:00 | 0001 1111 | 1Fh |
| Parameter Table Minor Revision | Start from 00h | 11h | 15:08 | 0000 0000 | 00h |
| Parameter Table Major Revision | Start from 01h | 12h | 23:16 | 0000 0001 | 01h |
| Parameter Table Length (double words) | How many DWORDs in the parameter table | 13h | 31:24 | 0000 0010 | 02h |
| Parameter Table Pointer (PTP) | Address of Adesto Parameter Table | 14h | 07:00 | 1000 0000 | 80h |
| | | 15h | 15:08 | 0000 0000 | 00h |
| | | 16h | 23:16 | 0000 0000 | 00h |
| Reserved | FFh | 17h | 31:24 | 0000 0001 | 01h |

Table 7-10. SFDP Parameters Table 1

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|--|---|------------------|---------------|----------------|-----------------|
| Erase Granularity | 01: 4KB available 11: 4KB not available | 30h | 01:00 | 01 | E5h |
| Write Granularity | 0: 1 Byte 1: 64 bytes or larger | | 02 | 1 | |
| Volatile Status Register Block Protect Bits | 0: Nonvolatile status bit 1: Volatile status bit | | 03 | 0 | |
| Volatile Status Register Write Enable Opcode | 0: 50h Opcode to enable, if bit 3 = 1 | | 04 | 0 | |
| Reserved | | | 07:05 | 111 | |
| 4KB Erase Opcode | Opcode or FFh | 31h | 15:08 | 0010 0000 | 20h |
| Fast Dual Read Output (1-1-2) | 0: Not supported, 1: Supported | 32h | 16 | 1 | F1h |
| Number of Address Bytes | 00: 3 Byte only 01: 3 or 4 Byte 10: 4 Byte only 11: Reserved | | 18:17 | 00 | |
| Double Transfer Rate (DTR) Clocking | 0: Not supported, 1: Supported | | 19 | 0 | |
| Fast Dual I/O Read (1-2-2) | 0: Not supported, 1: Supported | | 20 | 1 | |
| Fast Quad I/O Read (1-4-4) | 0: Not supported, 1: Supported | | 21 | 1 | |
| Fast Quad Output Read (1-1-4) | 0: Not supported, 1: Supported | | 22 | 1 | |
| Reserved | FFh | | 23 | 1 | |
| Reserved | FFh | | 33h | 31:24 | |
| Flash Memory Density | | 34h | 07:00 | 1111 1111 | FFh |
| | | 35h | 15:08 | 1111 1111 | FFh |
| | | 36h | 23:16 | 1111 1111 | FFh |
| | | 37h | 31:24 | 0000 0011 | 03h |
| Fast Quad I/O (1-4-4) Number of dummy clocks | Number of dummy clocks | 38h | 04:00 | 00100 | 44h |
| | | | 07:05 | 010 | |
| Fast Quad I/O (1-4-4) Read Opcode | Opcode or FFh | 39h | 15:08 | 1110 1011 | EBh |

Table 7-10. SFDP Parameters Table 1

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|--|-----------------------------------|------------------|---------------|----------------|-----------------|
| Fast Quad Output (1-1-4) Number of dummy clocks | Number of dummy clocks | 3Ah | 20:16 | 01000 | 08h |
| Fast Quad Output (1-1-4) Number of mode bits | Number of mode bits | | 23:21 | 000 | |
| Fast Quad Output (1-1-4) Read Opcode | Opcode or FFh | 3Bh | 31:24 | 0110 1011 | 6Bh |
| Fast Dual Output (1-1-2) Number of dummy clocks | Number of dummy clocks | 3Ch | 04:00 | 01000 | 08h |
| Fast Dual Output (1-1-2) Number of mode bits | Number of mode bits | | 07:05 | 000 | |
| Fast Dual Output (1-1-2) Read Opcode | Opcode or FFh | 3Dh | 15:08 | 0011 1011 | 3Bh |
| Fast Dual I/O (1-2-2) Number of dummy clocks | Number of dummy clocks | 3Eh | 20:16 | 00000 | 80h |
| Fast Dual I/O (1-2-2) Number of mode bits | Number of mode bits | | 23:21 | 100 | |
| Fast Dual I/O (1-2-2) Read Opcode | Opcode or FFh | 3Fh | 31:24 | 1011 1011 | BBh |
| Fast Dual DPI (2-2-2) | 0: Not supported, 1: Supported | 40h | 0 | 0 | FEh |
| Reserved | FFh | | 03:01 | 111 | |
| Fast Quad QPI (4-4-4) | 0: Not supported, 1: Supported | | 04 | 1 | |
| Reserved | FFh | | 07:05 | 111 | |
| Reserved | FFh | 41h | 15:08 | 1111 1111 | FFh |
| Reserved | FFh | 42h | 23:16 | 1111 1111 | FFh |
| Reserved | FFh | 43h | 31:24 | 1111 1111 | FFh |
| Reserved | FFh | 44h | 07:00 | 1111 1111 | FFh |
| Reserved | FFh | 45h | 15:08 | 1111 1111 | FFh |
| Fast Dual DPI (2-2-2) Number of dummy clocks | Number of dummy clocks | 46h | 20:16 | 0 0000 | 00h |
| Fast Dual DPI (2-2-2) Number of mode bits | Number of mode bits | | 23:21 | 000 | |
| Fast Dual DPI(2-2-2) Read Opcode | Opcode or FFh | 47h | 31:24 | 1111 1111 | FFh |
| Reserved | FFh | 48h | 07:00 | 1111 1111 | FFh |
| Reserved | FFh | 49h | 15:08 | 1111 1111 | FFh |

Table 7-10. SFDP Parameters Table 1

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|---|--|--------------------------|---------------|----------------|--------------------------|
| Fast Quad QPI (4-4-4) Number of dummy clocks | Number of dummy clocks | 4Ah | 20:16 | 00010 | 42h |
| Fast Quadl QPI (4-4-4) Number of mode bits | Number of mode bits | | 23:21 | 010 | |
| Fast Quad QPI(4-4-4) Read Opcode | Opcode or FFh | 4Bh | 31:24 | 1110 1011 | EBh |
| Erase type-1 Size | 4KB = 2 ⁰ Ch, 32KB = 2 ⁰ Fh, 64KB = 2 ¹ 0h; (2 ^N nbyte) | 4Ch | 07:00 | 0000 1100 | 0Ch |
| Erase type-1 Opcode | Opcode or FFh | 4Dh | 15:08 | 0010 0000 | 20h |
| Erase type-2 Size | 4KB = 2 ⁰ Ch, 32KB = 2 ⁰ Fh, 64KB = 2 ¹ 0h; (2 ^N nbyte) | 4Eh | 23:16 | 0000 1111 | 0Fh |
| Erase type-2 Opcode | Opcode or FFh | 4Fh | 31:24 | 0101 0010 | 52h |
| Erase Type-3 Size | 4KB = 2 ⁰ Ch, 32KB = 2 ⁰ Fh, 64KB = 2 ¹ 0h; (2 ^N nbyte) | 50h | 07:00 | 0001 0000 | 10h |
| Erase Type-3 Opcode | Opcode or FFh | 51h | 15:08 | 1101 1000 | D8h |
| Erase Type-4 Size | 4KB = 2 ⁰ Ch, 32KB = 2 ⁰ Fh, 64KB = 2 ¹ 0h; (2 ^N nbyte) | 52h | 23:16 | 0000 0000 | 00h |
| Erase Type-4 Opcode | Opcode or FFh | 53h | 31:24 | 1111 1111 | FFh |
| Erase Maximum/Typical Ratio | Maximum = 2 * (COUNT + 1) * Typical | 54h 55h 56h 57h | 03:00 | 0011 | 33h 62h D5h 00h |
| Erase type-1 Typical time | Count or 00h | | 08:04 | 0 0011 | |
| Erase type-1 Typical units | 00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s | | 10:09 | 01 | |
| Erase type-2 Typical time | Count or 00h | | 15:11 | 0110 0 | |
| Erase type-2 Typical units | 00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s | | 17:16 | 01 | |
| Erase type-3 Typical time | Count or 00h | | 22:18 | 101 01 | |
| Erase type-3 Typical units | 00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s | | 24:23 | 01 | |
| Erase type-4 Typical time | Count or 00h | | 29:25 | 00 000 | |
| Erase type-4 Typical units | 00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s | | 31:30 | 00 | |

Table 7-10. SFDP Parameters Table 1

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|---------------------------------------|--|-------------------|---------------|----------------|-------------------|
| Program Maximum/Typical Ratio | Maximum = 2 * (COUNT + 1) * Typical | 58h | 03:00 | 0100 | 84h |
| Page Size | 2^N bytes | | 07:04 | 1000 | |
| Program Page Typical time | Count or 00h | 59h 5Ah 5Bh | 12:08 | 0 1001 | 29h 01h C7h |
| Program Page Typical units | 0: 8μs, 1: 64μs | | 13 | 1 | |
| Program Byte Typical time, 1st byte | Count or 00h | | 17:14 | 01 00 | |
| Program Byte Typical units, 1st byte | 0: 1μs, 1: 8μs | | 18 | 0 | |
| Program Additional Byte Typical time | Count or 00h | | 22:19 | 000 0 | |
| Program Additional Byte Typical units | 0: 1μs, 1: 8μs | | 23 | 0 | |
| Erase Chip Typical time | Count or 00h | | 28:24 | 0 0111 | |
| Erase Chip Typical units | 00b: 16ms 01b: 256ms 10b: 4s 11b: 64s | | 30:29 | 10 | |
| Reserved | 1h | | 31 | 1 | |
| Prohibited Op during Program Suspend | see datasheet | | 5Ch | 03:00 | |
| Prohibited Op during Erase Suspend | see datasheet | 07:04 | | 1110 | |

Table 7-10. SFDP Parameters Table 1

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|--------------------------------|---|-------------------|---------------|----------------|-------------------|
| Reserved | 1h | 5Dh 5Eh 5Fh | 08 | 1 | A1h 07h 3Dh |
| Program Resume to Suspend time | Count of 64μs | | 12:09 | 0 000 | |
| Program Suspend Maximum time | Count or 00h | | 17:13 | 11 101 | |
| Program Suspend Maximum units | 00b: 128ns, 01b: 1μs, 10b: 8μs, 11b: 64μs | | 19:18 | 01 | |
| Erase Resume to Suspend time | Count of 64μs | | 23:20 | 0000 | |
| Erase Suspend Maximum time | Count or 00h | | 28:24 | 1 1101 | |
| Erase Suspend Maximum units | 00b: 128ns, 01b: 1μs, 10b: 8μs, 11b: 64μs | | 30:29 | 01 | |
| Suspend / Resume supported | 0: Program and Erase suspend supported 1: not supported | | 31 | 0 | |
| Program Resume Opcode | Opcode or FFh | 60h | 7:0 | 0111 1010 | 7Ah |
| Program Suspend Opcode | Opcode or FFh | 61h | 15:8 | 0111 0101 | 75h |
| Resume Opcode | Opcode or FFh | 62h | 23:16 | 0111 1010 | 7Ah |
| Suspend Opcode | Opcode or FFh | 63h | 31:24 | 0111 0101 | 75h |
| Reserved | 11b | 64h | 01:00 | 11 | F7h |
| Status Register Busy Polling | xxxx1b: Opcode = 05h, bit 0 = 1 Busy, xxxx1xb: Opcode = 70h, bit 7 = 0 Busy, Others: reserved | | 07:02 | 1111 01 | |
| Exit Deep Power-down time | Count or 00h | 65h 66h 67h | 12:08 | 0 0010 | A2h D5h 5Ch |
| Exit Deep Power-down units | 00b: 128ns, 01b: 1μs, 10b: 8μs, 11b: 64μs | | 14:13 | 01 | |
| Exit Deep Power-down Opcode | Opcode or FFh | | 22:15 | 101 0101 1 | |
| Enter Deep Power-down Opcode | Opcode or FFh | | 30:23 | 101 1100 1 | |
| Deep Power-down Supported | 0: Deep Power-down supported, 1: not supported | | 31 | 0 | |

Table 7-10. SFDP Parameters Table 1

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|--|--|-------------------|---------------|----------------|-------------------|
| Disable 4-4-4 Read Mode | | 68h 69h 6Ah | 03:00 | 1001 | 19h F6h 1Ch |
| Enable 4-4-4 Read Mode | | | 08:04 | 0 0001 | |
| Fast Quad I/O Continuous (0-4-4) supported | 0: not supported, 1: Quad I/O 0-4-4 supported | | 09 | 1 | |
| Fast Quad I/O Continuous (0-4-4) Exit | | | 15:10 | 1111 01 | |
| Fast Quad I/O Continuous (0-4-4) Enter | | | 19:16 | 1100 | |
| Quad Enable Requirements (QER) | | | 22:20 | 001 | |
| HOLD or RESET Disable | 0: not supported, 1: use Configuration register bit 4 | | 23 | 0 | |
| Reserved | FFh | 6Bh | 31:24 | 1111 1111 | FFh |
| Status Register Opcode | | 6Ch | 06:00 | 110 1000 | E8h |
| Reserved | 1h | | 07 | 1 | |
| Soft Reset Opcodes | | 6Dh | 13:08 | 01 0000 | 10h C0h |
| 4-Byte Address Exit | | 6Eh | 23:14 | 1100 0000 00 | |
| 4-Byte Address Enter | | 6Fh | 31:24 | 1000 0000 | 80h |

Table 7-11. SFDP Parameters Table 2

| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|---------------------|--|------------------|---------------|------------------------|-----------------|
| VCC Minimum Voltage | 1650h: 1.65V, 1700h: 1.70V, 2300h: 2.30V, 2500h: 2.50V, 2700h: 2.70V | 80h 81h | 15:0 | 0000 0000 0001 0111 | 00h 17h |
| VCC Maximum Voltage | 1950h: 1.95V, 3600h: 3.60V, 4000h: 4.00V, 4400h: 4.40V | 82h/83h | 31:16 | 0000 0000 0010 0000 | 00h 20h |

Table 7-11. SFDP Parameters Table 2

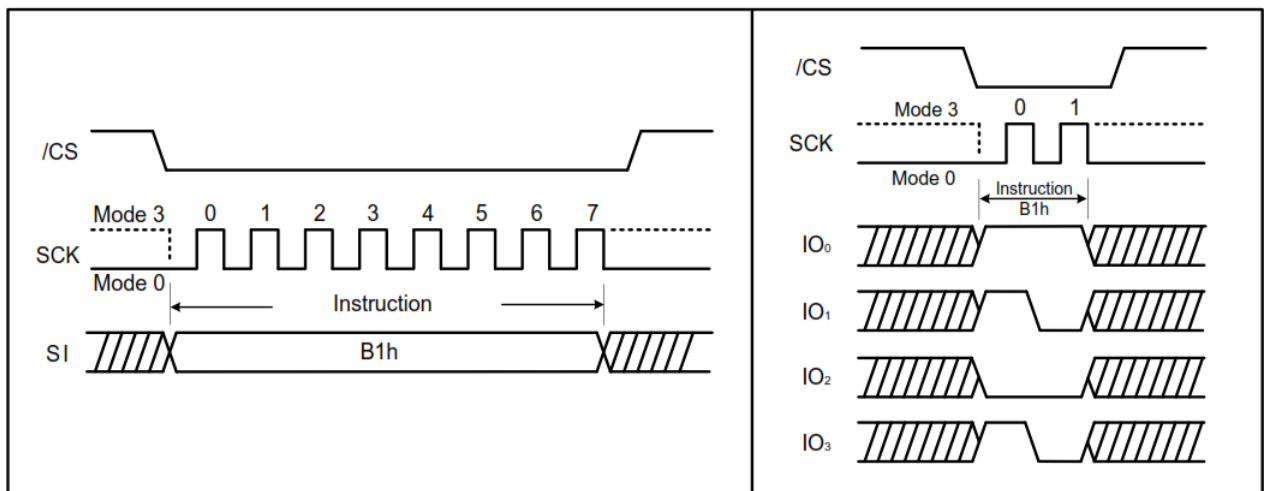
| Description | Comment | Address (h) Byte | Address (Bit) | Data (b) (Bit) | Data (h) (Byte) |
|------------------------------------|--|------------------|---------------|----------------|-----------------|
| Array Protection Method | 10b: Use non-volatile Status register | 84h 85h | 01:00 | 00 | 00h 00h |
| Power up Protection default | 0: power up unprotected 1: power up protected | | 02 | 0 | |
| Protection Disable Opcodes | 011b: Use status register | | 05:03 | 000 | |
| Protection Enable Opcodes | 011b: Use status register | | 08:06 | 0 00 | |
| Protection Read Opcodes | 011b: Use status register | | 11:09 | 000 | |
| Protection Register Erase Opcode | 00b: Not supported, 01b: Opcodes 3Dh, 2Ah, 7Fh, CFh, | | 13:12 | 00 | |
| Protection Register Program Opcode | 00b: Not supported 01b: Opcodes 3Dh, 2Ah, 7Fh, FCh | | 15:14 | 00 | |
| Reserved | FFh | 86h | 23:16 | 1111 1111 | FFh |
| Reserved | FFh | 87h | 31:24 | 1111 1111 | FFh |
| Reserved | FFh | 88h - FFh | | | Reserved |

7.36 Enter Secured OTP (B1h)

The Enter Secured OTP instruction is used for entering the additional 4 Kbit secured OTP mode. The OTP array is independent from main array, which may be used to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is locked down.

Note that the Write Status Register-1, Write Status Register-2 and Write Security Register instructions are not acceptable during the access to the secure OTP region. Once security OTP is locked down, only commands related with read are valid. The Enter Secured OTP instruction sequence is shown in Figure 7-56.

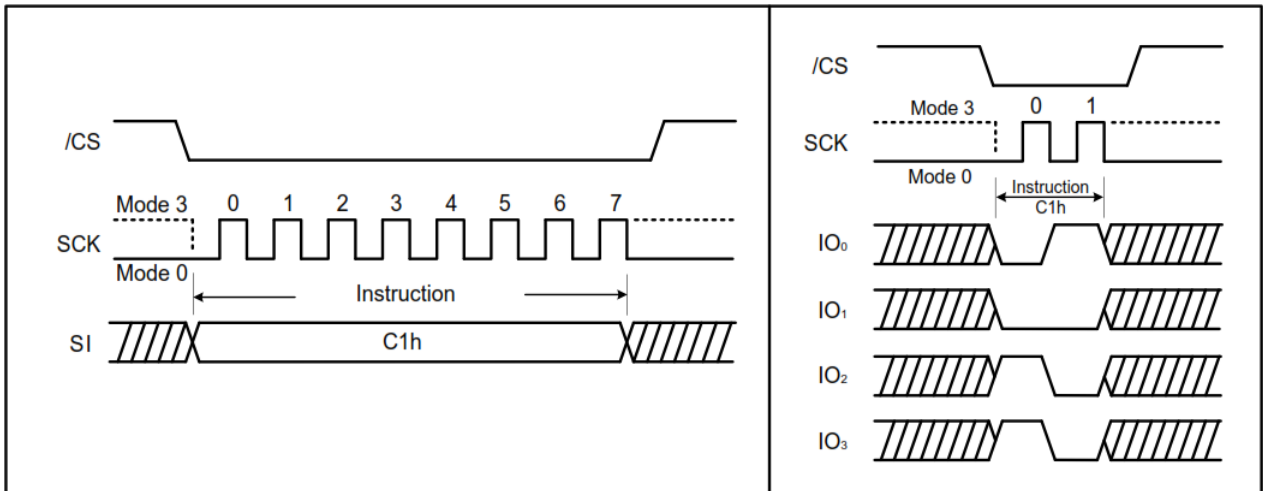
Figure 7-56. Enter Secured OTP Instruction for SPI Mode (left) and QPI Mode (right)



7.37 Exit Secured OTP (C1h)

The Exit Secured OTP instruction is for exiting the additional 4 Kbit secured OTP mode. (Please refer to Figure 7-57).

Figure 7-57. Exit Secured OTP instruction for SPI Mode (left) and QPI Mode (right)



7.38 Read Security Register (2Bh)

The Read Security Register read the value of Security Register bits at any time (even in program/erase/write status register-1 and write status register-2 condition) and continuously.

Secured OTP Indicator bit. The Secured OTP indicator bit shows whether the chip is factory-locked or non-factory-locked. When the bit is “0”, it indicates a non-factory lock, a “1” indicates a factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing Write Security Register instruction, the LDSO bit may be set to “1” for customer lock-down purpose. However, once the bit is set to “1” (Lock-down), the LDSO bit and the 4 Kbit Secured OTP area cannot be updated any more. While it is in 4 Kbit Secured OTP mode, array access is not allowed to write.

Table 7-12. Security Register Definition

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--|--|
| x | x | x | x | x | x | LDSO (indicate if lock- down) | Secured OTP indicator bit |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | 0: no lock down 1: lock- down (cannot program/ erase OTP) | 0: non factory lock 1: factory lock |
| Volatile bit | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Non Volatile bit | Non-Volatile bit |

Figure 7-58. Read Security Register Instruction (SPI Mode)

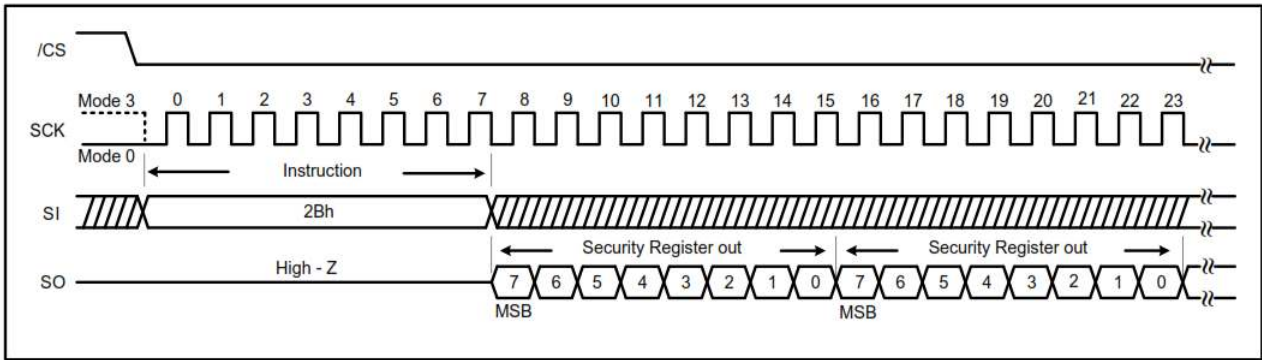
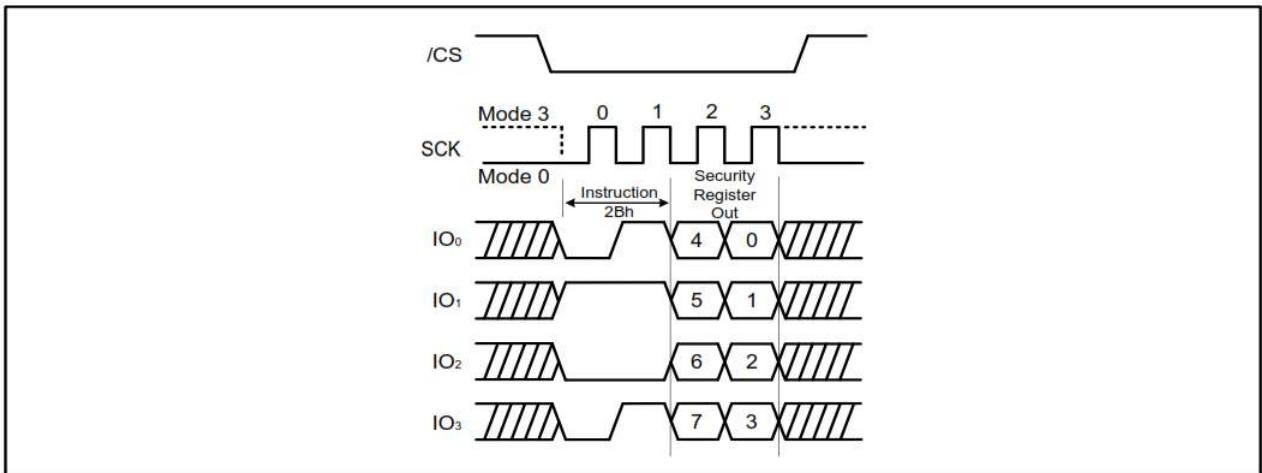


Figure 7-59. Read Security Register Instruction (QPI Mode)

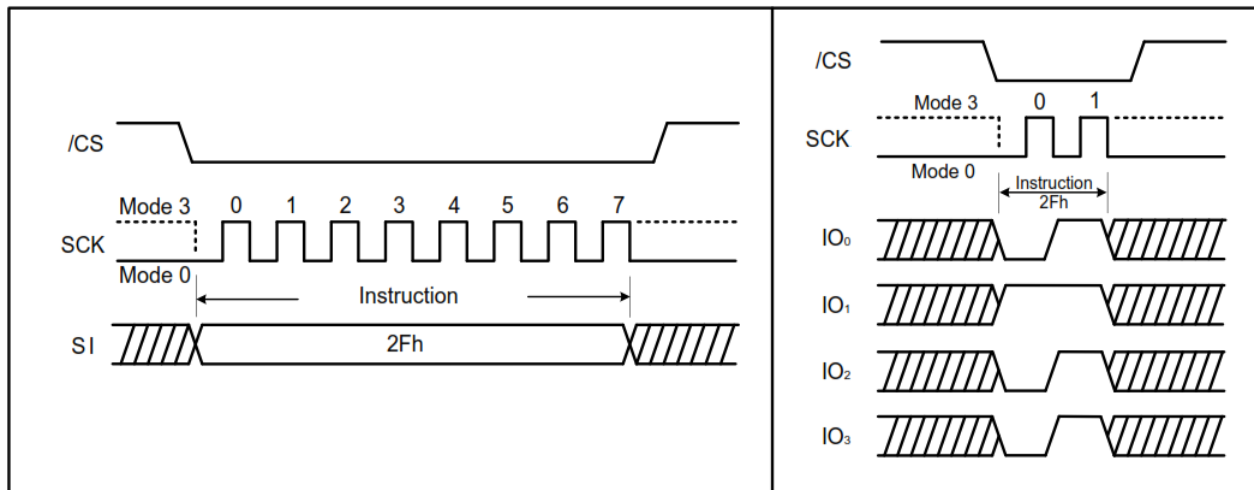


7.39 Write Security Register (2Fh)

The Write Security Register instruction is for changing the values of Security Register bits. Unlike the Write Status Register, the Write Enable instruction is not required before executing the Write Security Register instruction. The Write Security Register instruction may change the value of bit 1 (LDSO) for customer to lock-down the 4 Kbit Secured OTP area. Once the LDSO bit is set, the Secured OTP area can no longer be updated.

The $\overline{\text{CS}}$ must go high exactly at the boundary; otherwise, the instruction is rejected and not executed.

Figure 7-60. Write Security Register Instruction for SPI Mode (left) and QPI Mode (right)



7.40 4 Kbit Secured OTP

This value provides a 4 Kbit one-time-program area for setting the device unique serial number which may be set by the factory or the customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command) and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command
- The customer may lock-down bit 1 as “1”.

Note. Once the value is locked down by either the factory the or customer, it can no longer be changed. While in 4 Kbit secured OTP mode, array access is not allowed to write.

Table 7-13. Encoding of 4K bit Secured OTP Address

| Address Range | Size | Standard | Customer Lock |
|-----------------|------------|--------------------------------|------------------------|
| 000000 ~ 00000F | 128 bits | ESN (Electrical Serial Number) | Determined by customer |
| 000010 ~ 0001FF | 3,968 bits | N/A | |

8. Electrical Characteristics

Table 8-1. Absolute Maximum Ratings⁽¹⁾

| Parameter | Symbol | Conditions | Range | Unit |
|---------------------------------|--------|---------------------------------------|-------------------------|------|
| Supply Voltage | VCC | | -0.6 to VCC+0.4 | V |
| Voltage Applied to Any Pin | VIO | Relative to Ground | -0.6 to VCC +0.4 | V |
| Transient Voltage on any Pin | VIOT | <20nS Transient Relative to Ground | -1.0V to VCC +1.0V | V |
| Storage Temperature | TSTG | | -65 to +150 | °C |
| Lead Temperature | TLEAD | | See Note ⁽²⁾ | °C |
| Electrostatic Discharge Voltage | VESD | Human Body Model ⁽³⁾ | -2000 to +2000 | V |

Notes:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. The “Absolute Maximum Ratings” are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

8.1 Operating Ranges

Table 8-2. Device Operating Rate

| Parameter | Symbol | Conditions | Min | Max | Unit |
|-------------------------------|----------------|--|-----|-----|------|
| Supply Voltage | VCC | $f_R = 133$ MHz (Single/Dual/Quad SPI) $f_R = 50$ MHz (Read Data 03h) | 1.7 | 2.0 | V |
| Ambient Operating Temperature | T _A | Industrial | -40 | +85 | °C |

8.2 Endurance and Data Retention

Table 8-3. Endurance and Data Retention

| Parameter | Condition | Min | Max | Unit |
|----------------------|---------------------------------------|---------|-----|--------|
| Erase/Program Cycles | 4KB block, 32/64KB block or full chip | 100,000 | | Cycles |
| Data Retention | Full temperature range | | 20 | Years |

8.3 Power-up Timing and Write Inhibit Threshold

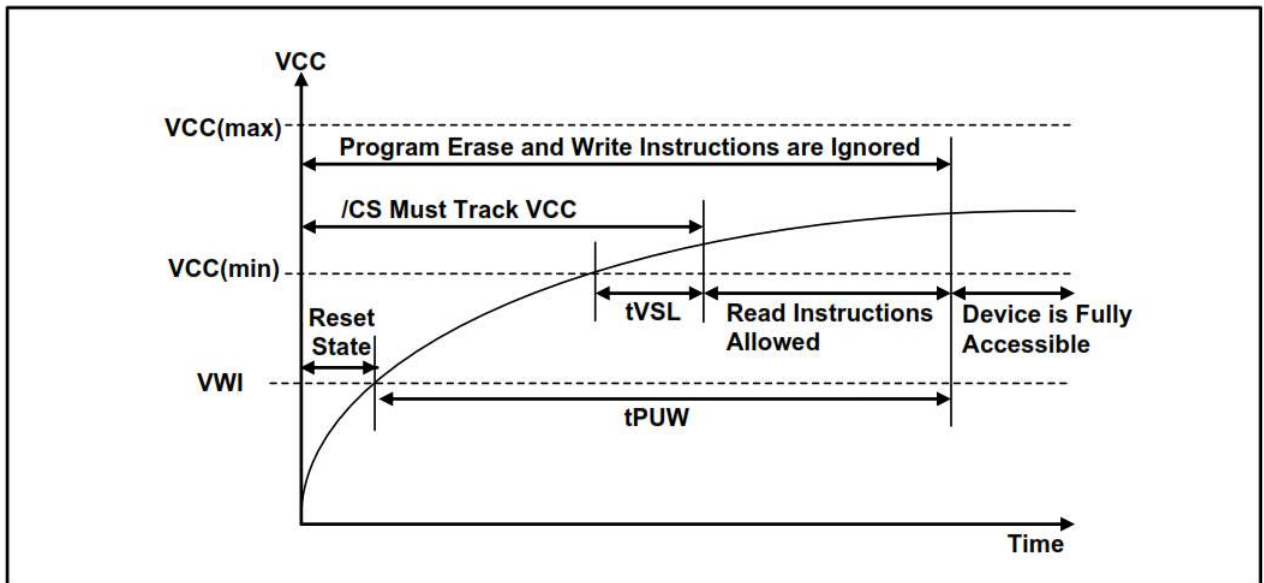
Table 8-4. Power-up Timing and Write Inhibit Threshold Parameters

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------------|-----------------|-----|-----|---------|
| VCC (min) to \overline{CS} Low | $t_{VSL}^{(1)}$ | 15 | | μs |
| Time Delay Before Write Instruction | $t_{PUW}^{(1)}$ | 1 | 10 | ms |
| Write Inhibit Threshold Voltage | $V_{WIT}^{(1)}$ | 1.0 | 1.4 | V |

Note:

1. These parameters are characterized at -10C & +85C only

Figure 8-1. Power-up Timing and Voltage Levels



8.4 DC Electrical Characteristics

Table 8-5. DC Electrical Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------|-----------------|--|-----|-----|---------|---------|
| Input Capacitance | $C_{IN}^{(1)}$ | $V_{IN} = 0V^{(2)}$ | | | 6 | pF |
| Output Capacitance | $C_{OUT}^{(1)}$ | $V_{OUT} = 0V^{(2)}$ | | | 8 | pF |
| Input Leakage | ILI | | | | ± 2 | μA |
| I/O Leakage | ILO | | | | ± 2 | μA |
| Standby Current | ICC1 | $\overline{CS} = VCC$, $V_{IN} = GND$ or VCC | | 10 | 50 | μA |
| Power Down Current | ICC2 | $\overline{CS} = VCC$, $V_{IN} = GND$ or VCC | | 2 | 20 | μA |

Table 8-5. DC Electrical Characteristics (Continued)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|--------|-----------------------------------|-----------|-----|-----------|------|
| Current Read Data/ Dual/Quad 1 MHz ⁽²⁾ | ICC3 | C = 0.1 VCC / 0.9VCC IO = Open | | | 7 | mA |
| Current Read Data/ Dual/Quad 50 MHz ⁽²⁾ | ICC3 | C = 0.1 VCC / 0.9VCC IO = Open | | | 15 | m |
| Current Read Data/ Dual/Quad 80 MHz ⁽²⁾ | ICC3 | C = 0.1 VCC / 0.9VCC IO = Open | | | 18 | mA |
| Current Read Data/ Dual/Quad 104 MHz ⁽²⁾ | ICC3 | C = 0.1 VCC / 0.9VCC IO = Open | | | 20 | mA |
| Current Read Data/ Dual/Quad 133 MHz ⁽²⁾ | ICC3 | C = 0.1 VCC / 0.9VCC IO = Open | | | 27 | mA |
| Current Write Status Register | ICC4 | $\overline{CS} = VCC$ | | 10 | 20 | mA |
| Current Page Program | ICC5 | $\overline{CS} = VCC$ | | 15 | 25 | mA |
| Current Block Erase | ICC6 | $\overline{CS} = VCC$ | | 15 | 25 | mA |
| Current Chip Erase | ICC7 | $\overline{CS} = VCC$ | | 15 | 25 | mA |
| Input Low Voltage | VIL | | -0.5 | | VCC x 0.2 | V |
| Input High Voltage | VIH | | VCC x 0.8 | | VCC + 0.4 | V |
| Output Low Voltage | VOL | IOL = 100 μ A | | | 0.2 | V |
| Output High Voltage | VOH | IOH = -100 μ A | VCC - 0.2 | | | V |

Notes:

1. Tested on sample basis and specified through design and characterization data, TA = 25°C, VCC = 1.8V.
2. Checked Board Pattern.

8.5 AC Measurement Conditions

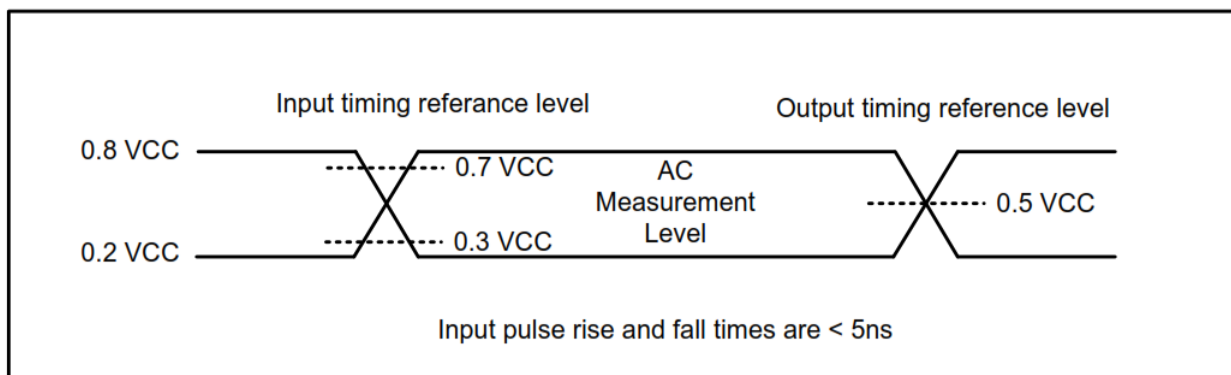
Table 8-6. AC Measurement Conditions

| Parameter | Symbol | Min | Max | Unit |
|----------------------------------|--------|--------------------|-----|------|
| Load Capacitance | CL | | 30 | pF |
| Input Rise and Fall Times | TR, TF | | 5 | ns |
| Input Pulse Voltages | VIN | 0.2 VCC to 0.8 VCC | | V |
| Input Timing Reference Voltages | IN | 0.3 VCC to 0.7 VCC | | V |
| Output Timing Reference Voltages | OUT | 0.5 VCC to 0.5 VCC | | V |

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven

Figure 8-2. AC Measurement I/O Waveform



8.6 AC Electrical Characteristics

Table 8-7. AC Electrical Characteristics

| Parameter ⁽⁵⁾ | Symbol | Alt | Min | Typ | Max | Unit |
|---|--|------------------|------|-----|-----|------|
| Clock frequency for all instructions, except Read Data and Fast Read Data in SPI mode (03h, 0Bh) 1.7V - 2.0V VCC and industrial temperature | F _R | f _c | D.C. | | 133 | MHz |
| Clock freq. Fast Read Data instruction in SPI mode (0Bh) | f _R | | D.C. | | 104 | MHz |
| Clock freq. Read Data instruction in SPI mode (03h) | f _R | | D.C. | | 50 | MHz |
| Clock High, Low Time except Read Data (03h) | t _{CLH} , t _{CLL} ⁽¹⁾ | | 3.5 | | | ns |
| Clock High, Low Time for Read Data (03h) instructions | t _{CRLH} , t _{CRLL} ⁽¹⁾ | | 8 | | | ns |
| Clock Rise Time peak to peak | t _{CLCH} ⁽²⁾ | | 0.1 | | | V/ns |
| Clock Fall Time peak to peak | t _{CHCL} ⁽²⁾ | | 0.1 | | | V/ns |
| $\overline{\text{CS}}$ Active Setup Time relative to Clock | t _{SLCH} | t _{CSS} | 5 | | | ns |
| $\overline{\text{CS}}$ Not Active Hold Time relative to Clock | t _{CHSL} | | 5 | | | ns |
| Data In Setup Time | t _{DVCH} | t _{DSU} | 2 | | | ns |
| Data In Hold Time | t _{CHDX} | t _{DH} | 3 | | | ns |
| $\overline{\text{CS}}$ Active Hold Time relative to Clock | t _{CHSH} | | 5 | | | ns |
| $\overline{\text{CS}}$ Not Active Setup Time relative to Clock | t _{CHSH} | | 5 | | | ns |
| $\overline{\text{CS}}$ Deselect Time (for Read instructions/Write, Erase and Program instructions) | t _{SHSL} | t _{CSH} | 100 | | | ns |
| Output Disable Time | t _{SHQZ} ⁽²⁾ | t _{DIS} | | | 7 | ns |
| Clock Low to Output Valid | t _{CLQV} | t _{V1} | | | 6 | ns |
| Clock Low to Output Valid (Except Main Read) ⁽³⁾ | t _{CLQV} | t _{V2} | | | 7 | ns |
| Output Hold Time | t _{CLQX} | t _{HO} | 1.5 | | | ns |

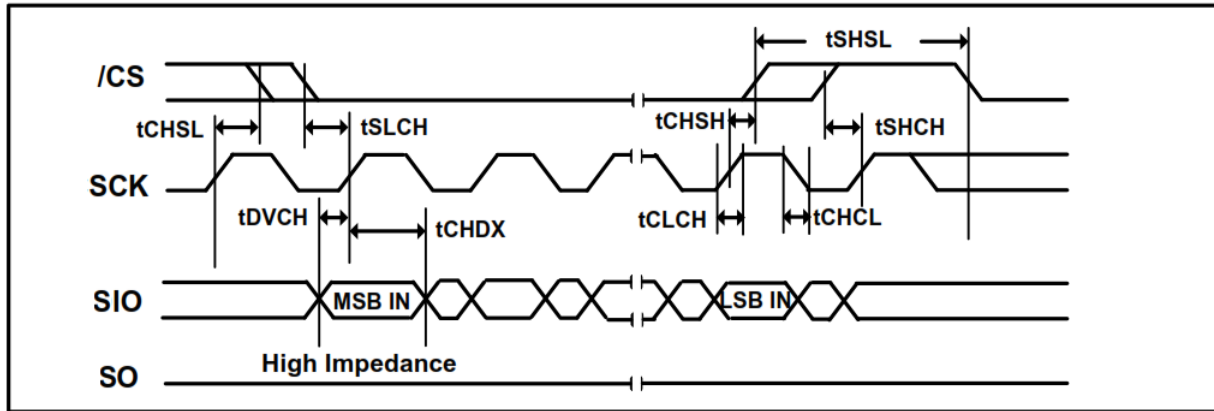
Table 8-7. AC Electrical Characteristics (Continued)

| Parameter ⁽⁵⁾ | Symbol | Alt | Min | Typ | Max | Unit |
|---|-------------------------|-----|-----|------|-----|---------------|
| $\overline{\text{HOLD}}$ Active Setup Time relative to Clock | t_{HLCH} | | 5 | | | ns |
| $\overline{\text{HOLD}}$ Active Hold Time relative to Clock | t_{CHHH} | | 5 | | | ns |
| $\overline{\text{HOLD}}$ Not Active Setup Time relative to Clock | t_{HHCH} | | 5 | | | ns |
| $\overline{\text{HOLD}}$ Not Active Hold Time relative to Clock | t_{CHHL} | | 5 | | | ns |
| $\overline{\text{HOLD}}$ to Output Low-Z | $t_{\text{HHQX}}^{(2)}$ | tLZ | | | 7 | ns |
| $\overline{\text{HOLD}}$ to Output High-Z | $t_{\text{HLQZ}}^{(2)}$ | tHZ | | | 12 | ns |
| Write Protect Setup Time Before $\overline{\text{CS}}$ Low | $t_{\text{WHSL}}^{(4)}$ | | 20 | | | ns |
| Write Protect Setup Time After $\overline{\text{CS}}$ High | $t_{\text{SHWL}}^{(4)}$ | | 100 | | | ns |
| $\overline{\text{CS}}$ High to Power Down Mode | $t_{\text{DP}}^{(2)}$ | | | | 3 | μs |
| $\overline{\text{CS}}$ High to Standby Mode without Electronic Signature Read | $t_{\text{RES1}}^{(2)}$ | | | | 3 | μs |
| $\overline{\text{CS}}$ High to Standby Mode with Electronic Signature Read | $t_{\text{RES2}}^{(2)}$ | | | | 1.8 | μs |
| $\overline{\text{CS}}$ High to next Instruction after Suspend | $t_{\text{SUS}}^{(2)}$ | | | | 30 | μs |
| $\overline{\text{CS}}$ High to next Instruction after Reset | $t_{\text{RST}}^{(2)}$ | | | | 30 | μs |
| Write Status Register Time | t_{W} | | | 5 | 15 | ms |
| Byte Program Time | t_{BP} | | | 5 | 150 | μs |
| Page Program Time | t_{PP} | | | 0.6 | 5 | ms |
| Page Program Time (ACC = 9V) | t_{PP} | | | 0.3 | 3 | ms |
| Block Erase Time (4KB) | t_{SE} | | | 0.06 | 0.4 | s |
| Block Erase Time (32KB) | t_{BE1} | | | 0.2 | 1.5 | s |
| Block Erase Time (64KB) | t_{BE2} | | | 0.35 | 2 | s |
| Chip Erase Time | t_{CE} | | | 60 | 150 | s |

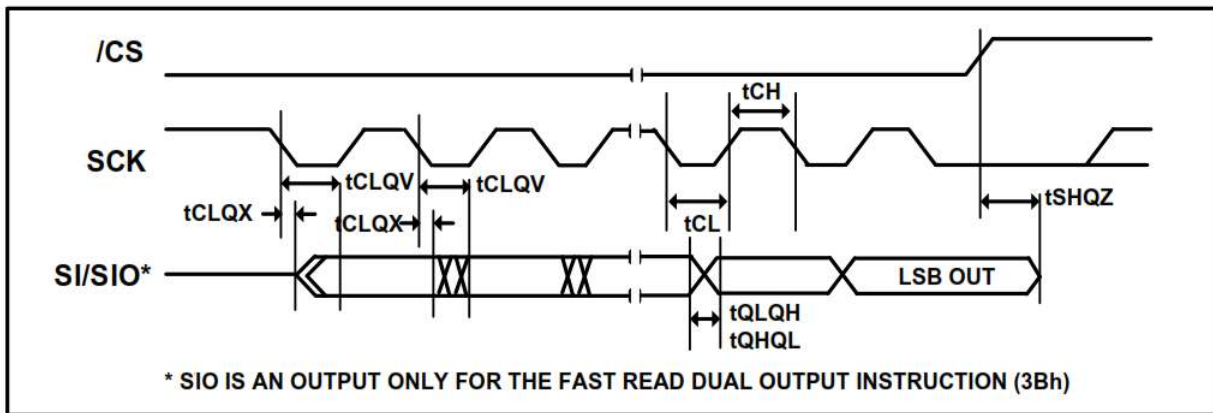
Notes:

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Contains: Read Status Register-1,2/ Read Manufacturer/Device ID, Dual, Quad/ Read JEDEC ID/ Read Security Register/ Read Serial Flash Discovery Parameter.
4. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.
5. Commercial temperature only applies to Fast Read (FR). Industrial temperature applies to all other parameters.

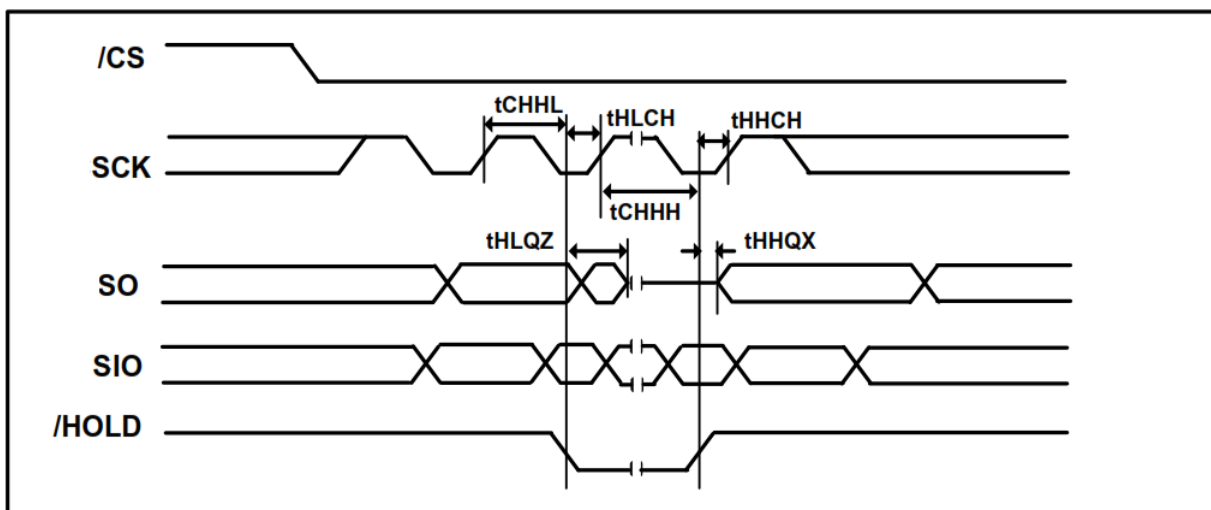
8.7 Input Timing



8.8 Output Timing

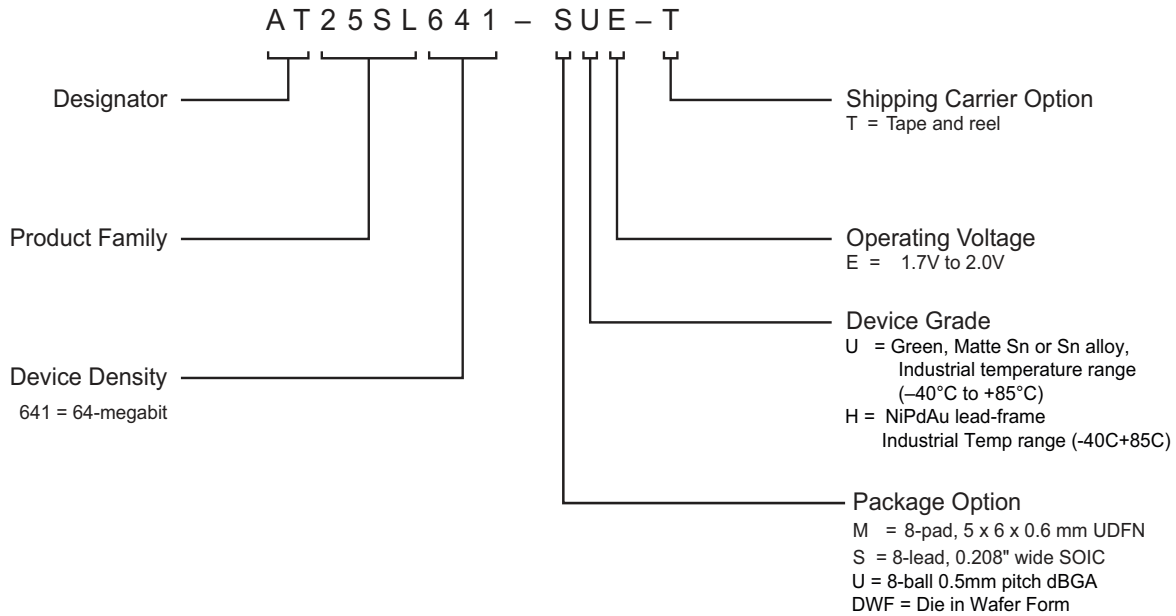


8.9 Hold Timing



9. Ordering Information

9.1 Ordering Code Detail



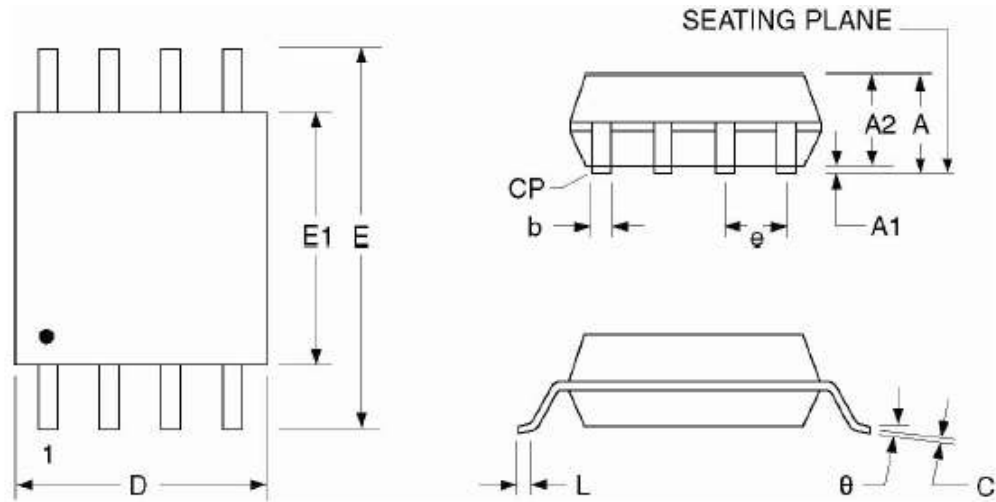
| Ordering Code ⁽¹⁾ | Package | Lead Finish | Operating Voltage | Max. Freq. (MHz) | Operation Range |
|------------------------------|---------|-------------|-------------------|------------------|---|
| AT25SL641-MHE-T | 8MA1 | NiPdAu | 1.7V - 2.0V | 133 MHz | -40°C to 85°C (Industrial Temperature Range) |
| AT25SL641-SUE-T | 8S4 | SnAgCu | | | |
| AT25SL641-UUE-T | 8-WLCSP | | | | |
| AT25SL641-DWF ⁽²⁾ | DWF | | | | |

- The shipping carrier option code is not marked on the devices.
- Contact Adesto for mechanical drawing or sales information.

| Package Type | |
|--------------|---|
| 8S4 | 8-lead, 0.208" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC) |
| 8MA1 | 8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra-Thin Dual Flat No-lead (UDFN) |
| 8-WLCSP | 8-ball, 0.5mm pitch, die Ball Grid Array (dBGA) |
| DWF | Die in Wafer Form |


10. Packaging Information

10.1 8S4 – 8-lead, .208" EIAJ SOIC

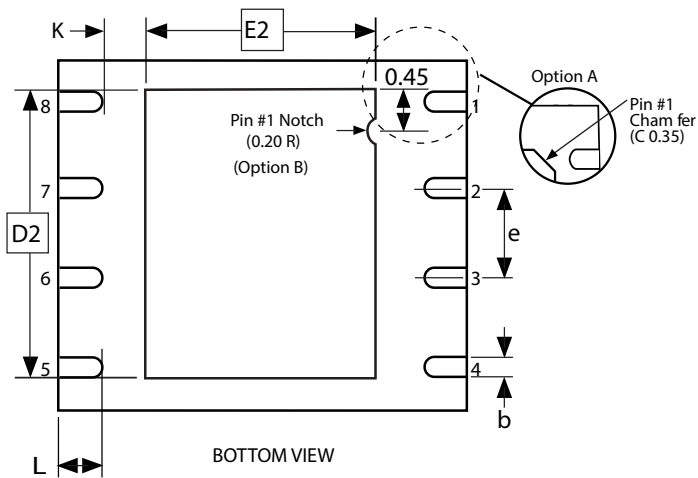
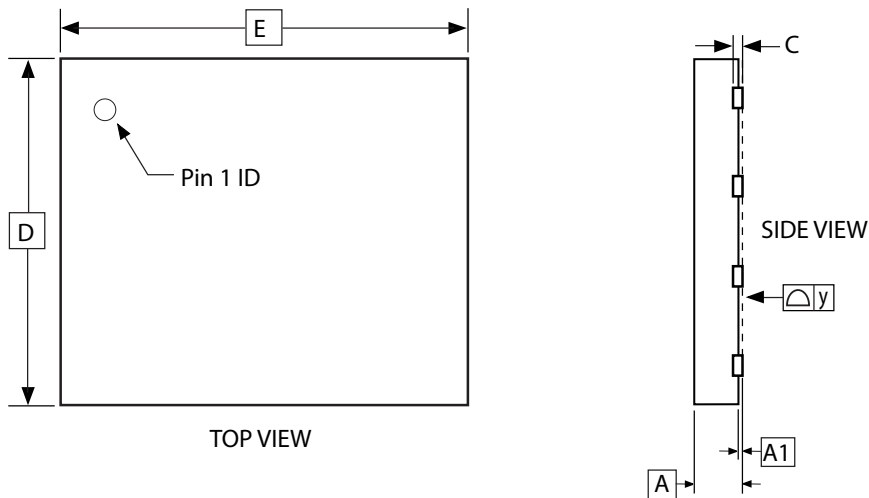


| SYMBOL | MILLIMETERS | | | INCHES | | |
|--------|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.75 | 1.95 | 2.16 | 0.069 | 0.077 | 0.085 |
| A1 | 0.05 | 0.15 | 0.25 | 0.002 | 0.006 | 0.010 |
| A2 | 1.70 | 1.80 | 1.91 | 0.067 | 0.071 | 0.075 |
| B | 0.35 | 0.42 | 0.48 | 0.014 | 0.017 | 0.019 |
| C | 0.19 | 0.20 | 0.25 | 0.007 | 0.008 | 0.010 |
| D | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| E | 7.70 | 7.90 | 8.10 | 0.303 | 0.311 | 0.319 |
| E1 | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.50 | 0.65 | 0.80 | 0.020 | 0.026 | 0.031 |
| θ | 0° | - | 8° | 0° | - | 8° |
| Y | - | - | 0.10 | - | - | 0.004 |

5/5/16

| | | | | |
|---|---|-----|-------------|------|
|  Package Drawing Contact: contact@adestotech.com | TITLE 8S4, 8-lead (0.208" Wide Body) Plastic Gull Wing Small Outline Package (EIAJ) | GPC | DRAWING NO. | REV. |
| | | STN | 8S3 | A |

10.2 8MA1 – UDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|------|------|------|
| A | 0.45 | 0.55 | 0.60 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| b | 0.35 | 0.40 | 0.48 | |
| C | 0.152 REF | | | |
| D | 4.90 | 5.00 | 5.10 | |
| D2 | 3.80 | 4.00 | 4.20 | |
| E | 5.90 | 6.00 | 6.10 | |
| E2 | 3.20 | 3.40 | 3.60 | |
| e | 1.27 | | | |
| L | 0.50 | 0.60 | 0.75 | |
| y | 0.00 | - | 0.08 | |
| K | 0.20 | - | - | |

- Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

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Package Drawing Contact:
contact@adestotech.com

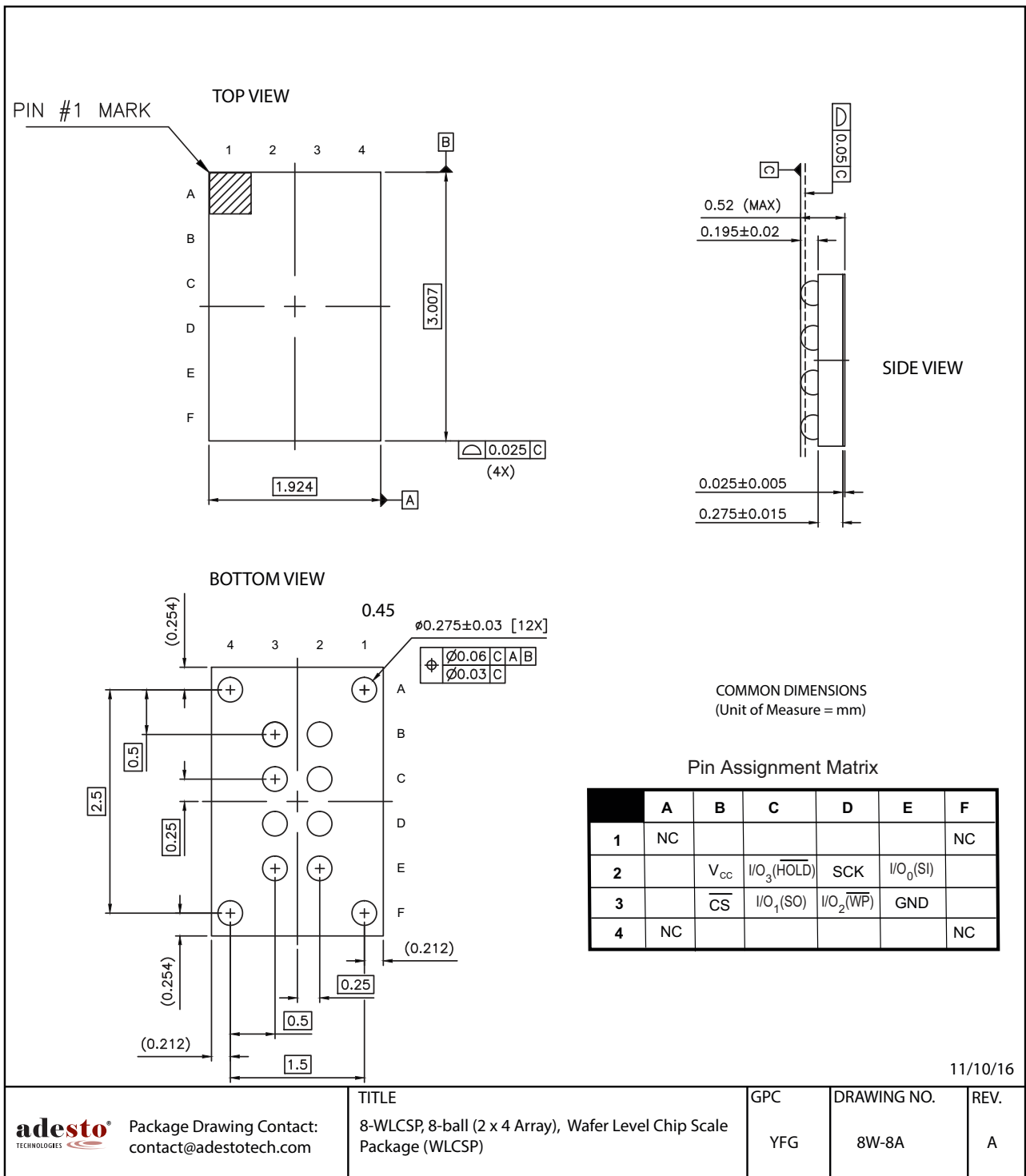
TITLE
8MA1, 8-pad (5 x 6 x 0.6 mm Body), Thermally
Enhanced Plastic Ultra Thin Dual Flat No Lead
Package (UDFN)

GPC
YFG

DRAWING NO.
8MA1

REV.
D

10.3 8-WLCSP — Die Ball Grid Array



Package Drawing Contact:
contact@adestotech.com

TITLE
8-WLCSP, 8-ball (2 x 4 Array), Wafer Level Chip Scale
Package (WLCSP)

GPC
YFG

DRAWING NO.
8W-8A

REV.
A

11. Revision History

| Revision Level | Date | Change History |
|----------------|---------|--|
| A | 6/2016 | Initial release of AT25SL641A data sheet. |
| B | 8/2016 | Added 8-WLCSP package. Added 18-WLCSP package. Updated voltage range. Removed Sector and Block Protect descriptions. Removed Status Register Memory Protection tables. Updated t_{CSH} specification. |
| C | 11/2016 | Updated UDFN and 8-WLCSP package drawing and dimensions. Updated SFDP tables (to version 1.6). Added description to Write Status Register in QPI mode. |
| D | 2/2017 | Updated Note 1 on Table 8.1. |
| E | 11/2017 | Updated Table 1-1 (\overline{WP} pin description). Updated 5.1 (Write Protect Features). Updated Tables 6-1 and 6-2. Restored Sector and Block Protect descriptions. Restored Status Register Memory Protection tables (Tables 6-3 and 6-4). Updated document status from Advanced to Complete. Added Errata 11.1. Removed references to 133 MHz option. Removed RESET option. Removed 18-WLCSP and 24-ball BGA package options. Removed references to ACC feature. |
| F | 12/2018 | Updated maximum frequency to 133 MHz on first page. Updated maximum frequencies in Section 1, Introduction. Added 133 MHz entry to the EBh instruction (Fast Read Quad I/O) in Table 7-5, QPI instructions. Added 133 MHz entry to the 0Ch instruction (Burst Read with Wrap) in Table 7-5, QPI instructions. Updated maximum frequency to 133 MHz in Figure 7-13, Fast Read instruction (0Bh). Updated maximum frequency to 133 MHz in Figure 7-21, Fast Read Quad I/O instruction (EBh). Replaced Figure 7-50, Word Read Quad I/O (E7h). Updated maximum frequency to 133 MHz in Figure 7-54, Burst Read with Wrap instruction (0Ch). Section 7.33, Set Parameters (C0h) renamed to Section 7.8, Set Parameters (C0h). Added title and number to the first table (now Table 7-6) and added P5:P4 = 11 encode row. Added title and number to the second table (now Table 7-7) and added P1:P0 = 11 encode row. Updated maximum frequency to 133 MHz in Section 8.2, Operating Ranges. Added 133 MHz ICC3 entry to Table 8.5, DC Characteristics. Reworked first four rows of Section 8.7, AC Characteristics to include 133 MHz and differentiate between the 03h and 0Bh instructions. Updated maximum frequency to 133 MHz in Section 9.1, Ordering Codes. Standardization of all tables in document. Reformat as necessary. Updated package type text at the bottom of the 8S4 package drawing. Modified text for the 90h command in Section 7.25 to clarify QPI operation. |

11.1 Errata:

Appendix A

1. If Status Register-2 CMP bit is 0, and Status Register-1 bits {SEC,TB,BP2,BP1,BP} are {1,0,0,0,1}, address 7FF000h-7FFFFFFh *is protected* from any Program or Erase commands. However, this setting does *not* protect the rest of Sector 127 or the rest of Block 255 from 64Kbit or 32kbit Block Erase commands. If a 64Kbit Block Erase Command is issued to Sector 127, address 7F0000h-7FEFFFFh *will* be erased. If a 32Kbit Block Erase Command is issued to Block 255, address 7F8000h-7FEFFFFh *will* be erased.

Workaround: If this protection bit combination is used and the behavior described in Note 3 is required, avoid using 64Kbit or 32kbit Block Erase commands for this specific memory region.

2. If Status Register-2 CMP bit is 1, and Status Register-1 bits {SEC,TB,BP2,BP1,BP} are {1,1,0,0,1}, address 001000h-7FFFFFFh *is protected* from any Program or Erase commands. However, this setting does *not* protect the rest of Sector 0 or the rest of Block 0 from 64Kbit or 32kbit Block Erase commands. If a 64Kbit Block Erase Command is issued to Sector 0, address 000000h-000FFFFh *will* be erased. If a 32Kbit Block Erase Command is issued to Block 0, address 000000h-000FFFFh *will* be erased.

Workaround: If this protection bit combination is used and the behavior described in Note 3 is required, avoid using 64Kbit or 32kbit Block Erase commands for this specific memory region.



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[90PFVGTSFLE1](#) [MBM29F800BA-70PFTN-SFLE1](#) [AT25DF011-MAHN-T](#) [AT25DF011-SSHN-T](#) [AT25DF011-XMHN-T](#) [AT25DF041B-](#)
[MHN-Y](#) [AT45DB161E-CCUD-T](#) [RP-SDCCTH0](#) [S29PL127J70BAI020](#) [S99-50052](#) [MX25L6473EM2I-10G](#) [W29GL256SL9T](#)
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[S26KL256SDABHB030](#) [S26KL128SDABHB020](#) [PC28F640J3F75B](#) [W29GL256SH9C](#) [S99-50239](#) [S29GL032N11FFIS12](#)
[S26KS512SDABHB030](#) [S26KL256SDABHA020](#) [S25FS128SAGMFV100](#) [S25FS064SDSNFN030](#) [S29AL016D90MAI020\(SPANSION\)](#)
[AM29F200BT-70EF\(SPANSION\)](#) [LE25S40MB-AH](#)