AC/DC Primary-Side DLNK Rapid Charge™ Controller with High Performance Voltage/Current Control

NDA Confidential

1 Description

The iW1799 is a high performance AC/DC power supply controller for rapid charge applications that supports high resolution voltage/current control. The device can support high power applications with power ratings of 45W or up and it can support 10mV voltage step requests up to 21V. It uses Dialog's ***PrimAccurate***™ technology to minimize external component count and simplify system design. The device operates in quasi-resonant mode to provide high efficiency and it also provides a number of key built-in protection features. The iW1799 can achieve tight multi-level constant voltage and multi-level constant current regulation without a traditional secondary feedback circuit. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions.

The iW1799 is optimized to work with Dialog's secondary-side controllers that use the proprietary digital link (DLNK) technology. The iW1799 and DLNK-based secondary-side controller chipset together can implement various rapid charge protocols, such as USB Power Delivery (USB PD), Qualcomm® Quick Charge™ 2.0 and 3.0 (QC2.0 and QC3.0) technologies, Huawei Fast Charge (FCP) and Super Charge (SCP) technologies, etc. to achieve fast and smooth voltage transitions upon request by mobile devices (MD). The iW1799 and compatible secondary-side controller from Dialog use the DLNK communction protocol for output voltage requests, output current limits, output voltage undershoot and over voltage information from the secondary to the primary. The iW1799 can also provide the unique protection features, such as Vin OVP or X-cap discharge for different applications.

The iW1799 can provide no-load power consumption for a typical 5V output setting of less than 75mW with ample margin. The no-load power consumption can be reduced to less than 20mW with an optional, external active start-up DFET.

Dialog's innovative proprietary technology ensures that power supplies designed with the iW1799 and Dialog's secondary-side controllers can provide output voltage configurations of 3.3V to 21V for USB PD, 5V/9V/12V for QC2.0 and 3.6V to 12V in 200mV increments for QC3.0, 5V/9V for Huawei FCP; 3V to 5.5V for Huawei SCP and other proprietary protocols.

Qualcomm® Quick Charge™ 2.0 and 3.0 are products of QualcommTechnologies, Inc.

2 Features

- Supports 45W or up application circuit designs
- Supports 10mV DLNK voltage step request up to 21V required by USB PD programmable power supply (PPS) or other proprietary rapid charge protocols
- RC charging V_{CC} technology enables ultra-low no-load power of <75mW with ample margin at 230V_{AC} and 5V output voltage setting
  - <20mW achievable (at 230V_{AC}/5V_{OUT}) with an external active startup circuit
- High V_{CC} pin voltage rating eliminates external V_{CC} LDO
- Tight multi-level constant-voltage and multi-level constant-current regulation with primary-side feedback and control
- Proprietary optimized load adaptive maximum constant frequency PWM switching with quasi-resonant operation achieves best size, efficiency, and common mode noise
- Backward compatible with QC2.0/3.0, Huawei FCP/SCP and other proprietary rapid charge protocols with secondary-side interface circuits
- Multi-mode PWM/PFM control improves efficiency at various load conditions
- No audible noise over entire operating range
- User-configurable 4-level cable drop compensation independent of output voltage
- Proprietary secondary-to-primary digital communication with single optocoupler for all the rapid charge information:
  - Output voltage request
  - Output current limit
  - Output voltage undershoot detection for fast dynamic load response
  - Over-voltage protection
- ***EZ-EMI***® design enhances manufacturability
- Built-in single-point fault protections against output short-circuit including soft short and half short, output over-voltage, and output over-current
- Advanced fault control technology addresses issues of soft shorts in cables and connectors by effectively reducing the average output power at fault conditions without latch
- Dual over-temperature protection with both internal OTP and external shutdown control
- DET pin provides V_{IN} OVP or X-cap discharge protection

3 Applications

- Rapid-charging AC/DC adapters for smart phones, tablets and other portable devices.

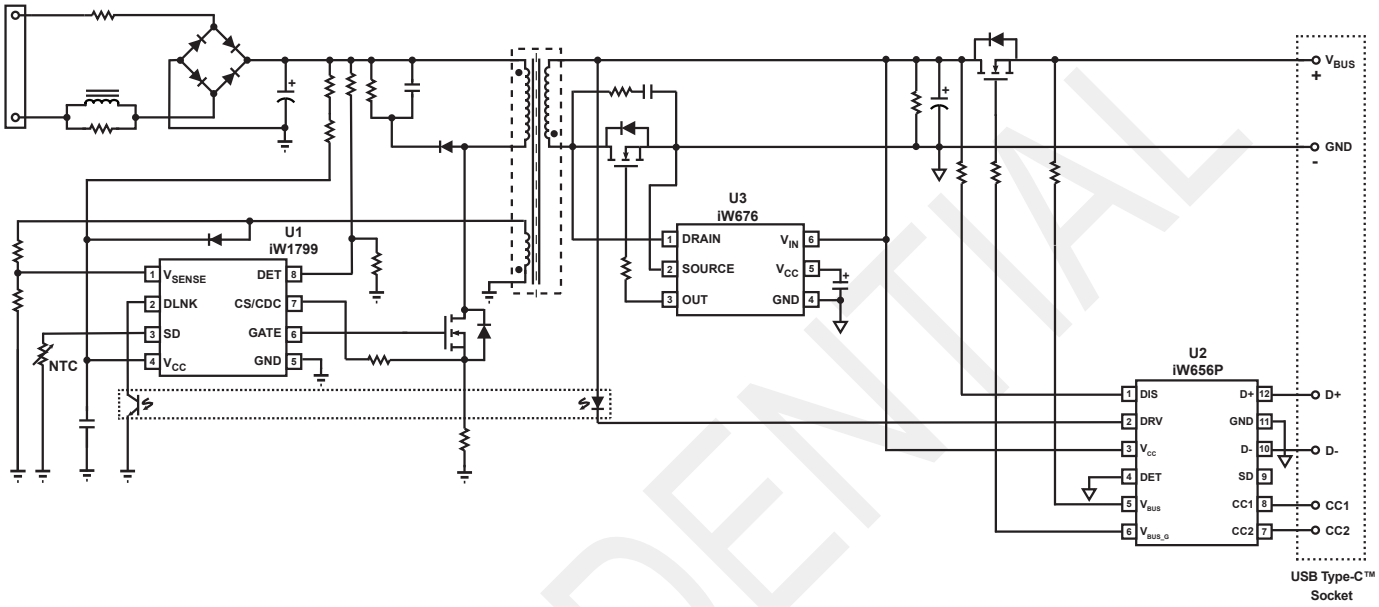


Figure 3.1 : iW1799 Typical Application Circuit for USB PD (DET Pin is Enabled for V_{IN} OVP Protection) (Using iW656P as Secondary-Side Controller for USB PD and iW676 as Synchronous Rectifier Controller.)

4 Pinout Description

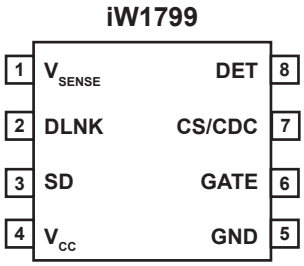


Figure 4.1 : 8-Lead SOIC Package

Pin Number	Pin Name	Type	Pin Description
1	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation.
2	DLNK	Analog Output	Digital communication link signal. Used for secondary-side to primary- side communication for all rapid charge information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	SD	Analog Input	Used for external shutdown control. Can be configured for external over-temperature protection (OTP) by connecting an NTC resistor from this pin to ground.
4	V_{CC}	Power Input	IC power supply.
5	GND	Ground	Ground.
6	GATE	Output	Gate drive for external MOSFET switch.
7	CS/CDC	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation. During configuration stage, used to configure the CDC compensation level.
8	DET	Analog Input	Used for external V_{IN} OVP protection or X-Cap discharge function.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to the Electrical Characteristics section.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 4, I_{CC} = 20mA max)	V_{CC}	-0.3 to 45.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
V_{SENSE} input (pin 1, I_{VSENSE} ≤ 10mA)		-0.7 to 10.0	V
DLNK (pin 2)		-0.7 to 5.0	V
CS/CDC (pin 7)		-0.7 to 5.0	V
SD (pin 3)		-0.7 to 5.0	V
GATE (pin 6)		-0.3 to 30	V
DET (pin 8)		-0.7 to 5.0	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Thermal resistance junction-to-ambient	θ_{JA}	160	°C/W
ESD rating per JEDEC JESD22-A114		±2,000	V
Latch-up test per JESD78D		±100	mA

Note 1. Stresses beyond those listed under “Absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{cc} SECTION (Pin 4)						
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising		21.5		V
Under-voltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling		8.2		V
Latch release threshold	$V_{CC(RLS)}$	V_{CC} falling		7		V
V_{CC} over-voltage protection level (Note 1)	$V_{CC(OVP)}$	V_{CC} rising		42		V
Start-up current	$I_{IN(ST)}$	V_{CC} = 16V			7	µA
Quiescent current	I_{CCQ}	V_{CC} = 20V, excluding gate driver switching current		2.5		mA
No-load operating current (Note 1)	I_{CC_NL}	No-load operation		0.22		mA
V_{SENSE} SECTION (Pin 1)						
Nominal voltage at 5V output	$V_{SENSE\_5V(NOM)}$	5V V_{OUT}, T_A = 25°C, negative edge		0.93		V
Output OVP threshold with no CDC compensation at 5V output (Note1) (Note 2)	$V_{SENSE\_5V(MAX)}$	5V V_{OUT}, T_A = 25°C, negative edge		1.116		V
DLNK SECTION (Pin 2)						
Detection threshold (falling edge)	$V_{DLNK-TH(F)}$			1.6		V
Recovery threshold (rising edge)	$V_{DLNK-TH(R)}$			1.8		V
DLNK current source	I_{DLNK}			500		µA
CS/CDC SECTION (Pin 7)						
Switching-cycle over-current threshold	V_{OCP}			0.92		V
CS regulation upper limit (Note 1)	$V_{IPK(HIGH)}$			0.8		V
CS regulation lower limit (Note 1)	$V_{IPK(LOW)}$	(Note 1)		0.184		V
Configuration current source	I_{CFG}			500		µA

Electrical Characteristics (cont.)

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GATE SECTION (Pin 6)						
Driver pull-down ON-resistance	$R_{DS(ON)PD}$	I_{SINK} = 5mA		12		Ω
Driver pull-up ON-resistance	$R_{DS(ON)PU}$	I_{SOURCE} = 5mA		99		Ω
Rise time (Note 1)	t_R	T_A = 25°C, C_L = 330pF 10% to 90%		95		ns
Fall time (Note 1)	t_F	T_A = 25°C, C_L = 330pF 90% to 10%		14		ns
Maximum GATE pin voltage at switching mode	$V_{GATE(MAX)}$	T_A = 25°C		10.3		V
Maximum switching frequency at < 8V V_{OUT} (Note 3)	$f_{SW\_LV\_PWM}$	At PWM mode		76		kHz
Maximum switching frequency at ≥ 8V V_{OUT} (Note 3)	$f_{SW\_HV\_PWM}$	At PWM mode		86		kHz
SD (Pin 3) SECTION						
Shutdown threshold (falling edge)	$V_{SD-TH(F)}$			1.0		V
Shutdown threshold before start-up	$V_{SD-TH(ST\_F)}$			1.2		V
Shutdown current source	I_{SD}			100		µA
DET (Pin 8) SECTION						
OVP detection threshold	V_{OVP_TH}			0.5		V
THERMAL CHARACTERISTICS						
Thermal Shutdown Threshold (Note 1)	T_{SD}			140		°C
Thermal Shutdown Recovery (Note 1)	T_{SD-R}			130		°C

Notes:

Note 1. These parameters are not 100% tested. They are guaranteed by design and characterization.

Note 2. The output OVP threshold depends on the CDC setup, see Section 9.12 for more details.

Note 3. Operating frequency varies based on the load conditions, see Section 9.6 for more details.

7 Typical Performance Characteristics

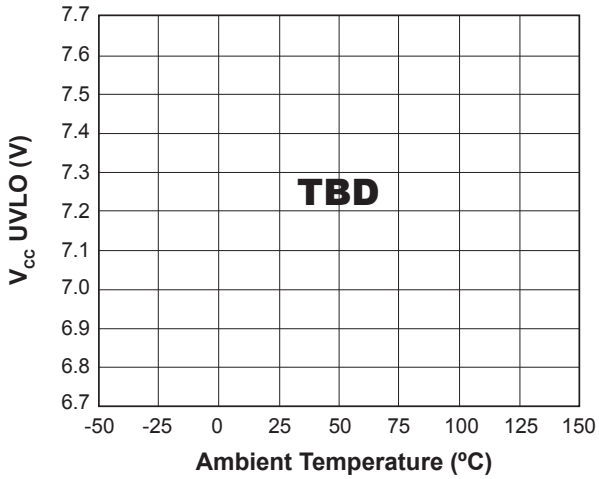


Figure 7.1 : V_{CC} UVLO vs. Temperature

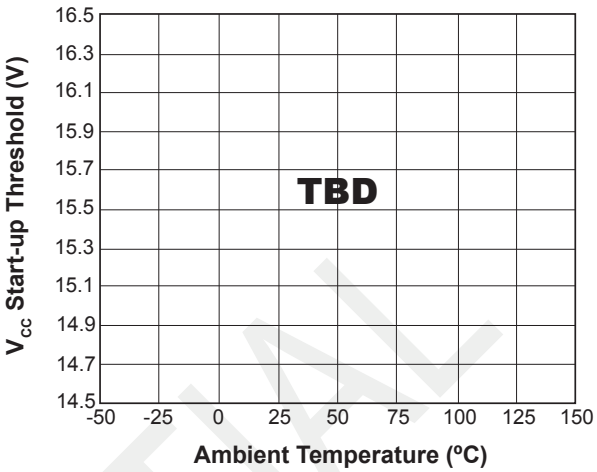


Figure 7.2 : Start-Up Threshold vs. Temperature

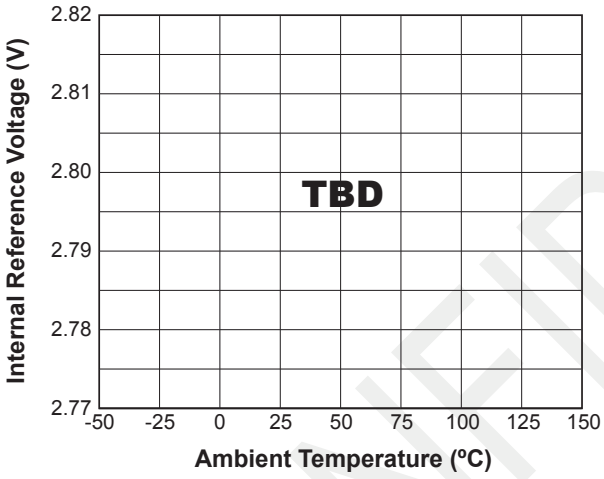


Figure 7.3 : Internal Reference vs. Temperature

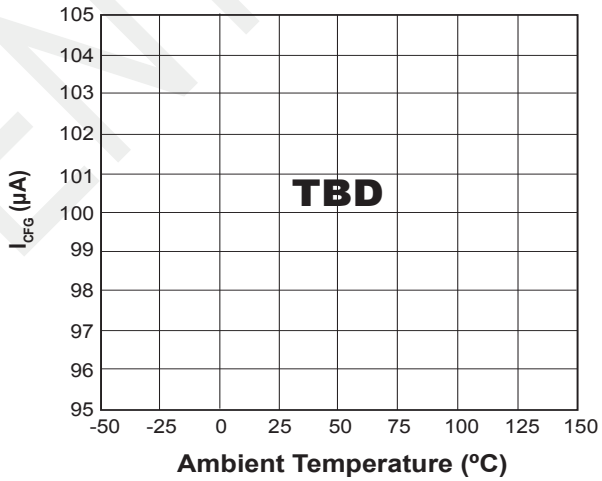


Figure 7.4 : I_{CFG} vs. Temperature

8 Functional Block Diagram

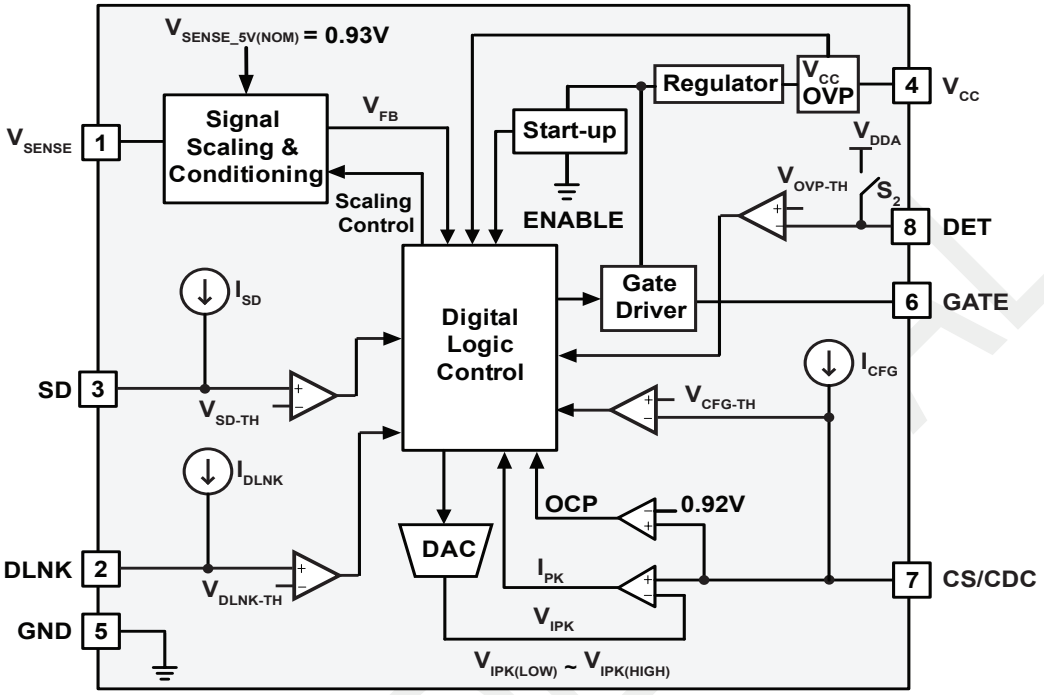


Figure 8.1 : iW1799 Functional Block Diagram

9 Theory of Operation

The iW1799 is a digital controller for rapid charge applications, which uses a proprietary primary-side control technology to eliminate secondary regulation and feedback circuits required in traditional designs. The core control circuit uses fixed-frequency PWM Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, Dialog's digital control technology enables fast dynamic response, tight multi-level output voltage and multi-level current regulation, and full-featured circuit protections.

The iW1799 is optimized to work with Dialog's secondary-side controllers that use the proprietary digital link (DLNK) technology, for rapid charge protocol interface and secondary-to-primary-side communication, to achieve fast and smooth voltage and current transition upon request from mobile devices (MD).

The iW1799 has a built-in circuit to decode the different pulse patterns for voltage configuration, current limit setting, V_{OUT} under-voltage and over-voltage detection, and the iW1799 responds accordingly based on the decoded information.

Figure 8.1 shows the iW1799 operates under peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the external MOSFET gate voltage. The CS/CDC pin is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the CS/CDC pin voltage to compare with, and it varies in the range of $V_{IPK(LOW)}$ to $V_{IPK(HIGH)}$ under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1799 uses an advanced digital control algorithm to reduce system design time and increase reliability. Furthermore, accurate secondary constant current operation is achieved without the need for traditional secondary-side feedback and control circuits.

The iW1799 uses adaptive multi-mode PWM/PFM control to dynamically change the MOSFET switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique MOSFET quasi-resonant switching to further improve efficiency and reduce EMI. The built-in single-point fault protection features include over-voltage protection (OVP), output short-circuit protection, over-current protection (OCP), over-temperature protection (OTP), and current sense fault detection. In particular, it ensures that power supplies built with the iW1799 can achieve with ample margin less than 75mW no-load power consumption in a typical 15W multi-level output voltage AC/DC off-line power adapter applications.

Dialog's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control.

9.1 Pin Detail

Pin 1 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation. This pin is also used for transformer communication signal.

Pin 2 – DLNK

Digital communication link signal. Used for secondary-side to primary-side communication for all rapid charge information, including output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.

Pin 3 – SD

External shutdown control. If the voltage at this pin is lower than 1.2V (typical) at the beginning of start-up or lower than 1.0V (typical) during normal operation, then the IC shuts down. Leave this pin unconnected if the shutdown control is not used.

Pin 4 – V_{CC}

Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 20.5V (typical) and shuts down when the V_{CC} voltage drops below 8.2V (typical). A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND in addition to 2.2-4.7µF electrolytic cap.

Pin 5 – GND

Ground.

Pin 6 – GATE

Gate drive for the external power MOSFET switch.

Pin 7 – CS/CDC

Primary-side current sense and external cable drop compensation (CDC). Used for cycle-by-cycle peak current control and limit.

Pin 8 - DET

Used for external OVP detection or X-Cap discharge function.

9.2 Active Start-up and Soft-Start

The iW1799 utilizes RC charging V_{CC} technology to charge up V_{CC} at start-up. Prior to start-up, the ENABLE signal is low. When the AC line voltage applied, RC charge current will flow through to charge the V_{CC} bypass capacitor.The ENABLE signal becomes active only when V_{CC} is charged to $V_{CC(ST)}$. Then, the iW1799 begins to perform the initial OTP check (see Section 9.13), followed by CDC configuration (see Section 9.12). Afterwards, the iW1799 commences the soft-start function. During this start-up process, an adaptive soft-start control algorithm is applied, where the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator. If at any time the V_{CC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$, the iW1799 goes to shutdown. Then, the ENABLE signal becomes low and the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new start-up cycle.

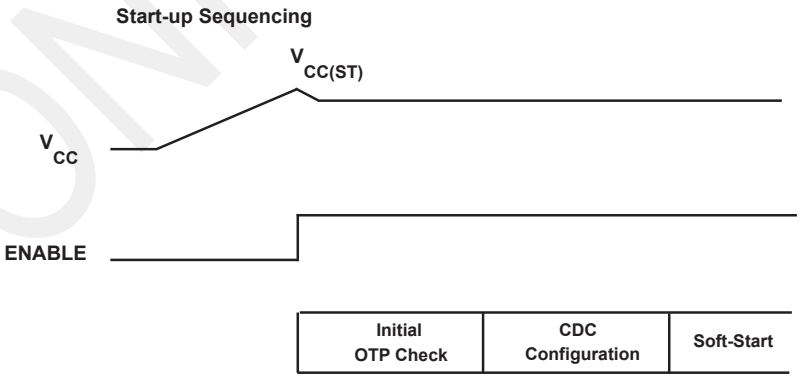


Figure 9.1 : Start-up Sequencing Diagram

It is recommended that the V_{SENSE} voltage divider is set for 5V default output voltage. The power adapter starts up to default 5V state and waits for further voltage/current requests.

9.3 Understanding Primary Feedback

Figure 9.2 illustrates a simplified flyback converter. When the switch Q_1 conducts during $t_{ON}(t)$, the current $I_g(t)$ is directly drawn from the rectified. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D_1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q_1 turns off, D_1 conducts and the stored energy $E_g(t)$ is delivered to the output.

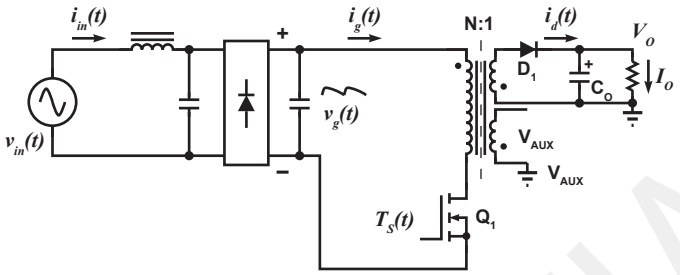


Figure 9.2 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q_1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $V_g(t)$, assuming the voltage dropped across Q_1 is zero. The current in Q_1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (9.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (9.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave.

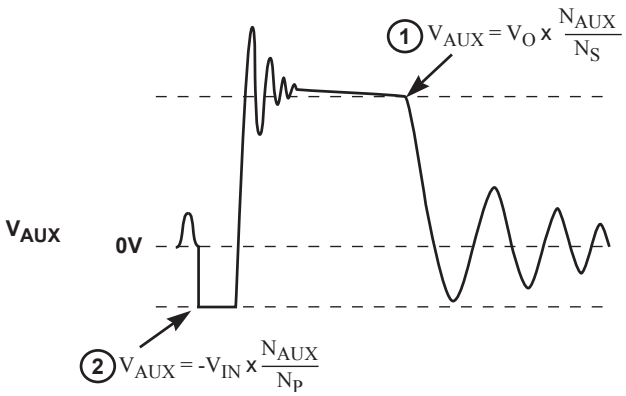


Figure 9.3 : Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (9.5)$$

and reflects the output voltage as shown in Figure 9.3.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small. With the iW1799, ΔV can be ignored.

The real-time waveform analyzer in the iW1799 reads this information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

9.4 Multi-Level Constant Voltage Operation

The iW1799 is designed for the Dialog's ***Rapid Charge*** technology and it is optimized to work with Dialog's secondary-side controllers, such as the iW656P or iW657P. Compatible secondary-side controllers have a built-in encoder to generate different pulse patterns and drive the internal switch of DRV pin so that the different voltage information together with the associated constant current (CC) limit setting can be sent to the primary side through an optocoupler. These patterns function as digital communication signals and are received at the DLNK pin of the iW1799. They are then decoded into different information including voltage requests, current limit settings, over-voltage and under-voltage.

After soft-start has been completed, the default output voltage should be 5V and the actual output voltage is related to the external V_{SENSE} voltage divider network and transformer secondary-to-auxiliary winding turns ratio. The digital control block measures the output conditions. It determines the output power levels and adjusts the control system according to a light load or a heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (t_{ON}) and off time (t_{OFF}) in order to meet the output voltage regulation requirements. At the steady-state CV operation of the 5V setting, the V_{SENSE} pin voltage at the instant corresponding to point 1 (as indicated in Figure 9.3) is regulated to $V_{SENSE\_5V(NOM)}$ in most conditions, e.g. 0.930V(typical).

If the default output voltage is set to 5V, the iW1799 changes the output voltage according to USB PD2.0/3.0, QC2.0/QC3.0 or other protocols with built-in V_{SENSE} scaling & conditioning circuit and $V_{SENSE(NOM)}$ or reference voltage adjustment.

If no voltage is detected on V_{SENSE}, it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1799 shuts down.

9.5 Multi-Level Current Limit and Constant Current Operation

The iW1799 also determines the CC limit information associated with voltage request. The CC limit is given by

$$I_{CC\_LIMIT} = k_{CC} \times 0.4 \times \frac{N}{R_S} \times \eta_x \qquad (9.6)$$

where N is the transformer primary-to-secondary winding turns ratio, R_S is the current sense resistor, η_X is the transformer conversion efficiency, and k_{CC} is a coefficient set by the secondary side controllers, such as the iW656P (see the secondary-side controller datasheet for pre-defined k_{CC} information).

Because rapid charge protocols introduce fine voltage steps, the CC limits are set to avoid abrupt changes. At low output voltage levels, same CC limit is used. As the output voltage setting goes up with one fixed CC limit, constant power limit is reached. After that, CC limit decreases as output voltage level goes up such that the envelop of multi-level CV/CC maximum power is approximately constant. Some adjacent V_{BUS} levels can share one same CC limit if the percentage difference between adjacent V_{BUS} level is not significant.

In an overload condition, the iW1799 enters CC mode to limit the output current on a cycle-by-cycle basis. In this mode of operation, the output current is limited to a constant level regardless of the output voltage, while avoiding continuous conduction mode operation. In case of very heavy loading when the output voltage is low enough, the iW1799 shuts down.

The iW1799 senses the load current indirectly through the primary current, which is detected by the pin CS/CDC through a resistor between CS/CDC pin and ground.

When operating in the CC mode, with the decrease of equivalent load resistance or battery voltage, both the output voltage and V_{CC} decrease. After the V_{CC} voltage is below UVLO threshold the iW1799 shuts down (see Section 9.10). Meanwhile, the iW1799 monitors the output voltage, and shuts down the system when the detected output voltage is lower than certain level; this is known as the “CC shutdown voltage.” The shutdown can occur under either one of the above two conditions.

The “CC shutdown voltage” here refers to the voltage at the cable end, and the output voltage at the PCB end is the sum of the “CC shutdown voltage” and the “cable comp” (specified in Section 9.12). As a result, the “CC shutdown voltage” option can adaptively match the cable voltage drop at CC mode. For instance, at 5V/2A operation state, if the cable resistance is around 150mΩ, the voltage drop across the cable is around 300mV under both the CV mode full load and CC mode conditions. Assuming the iW1799 product option (with 3.3V CC shutdown voltage for the 5V output voltage setting) at full load with no CDC configured, the voltage at the PCB will be around 5V and the voltage at the end of the cable will be around 4.7V. Then the CC shutdown occurs when the voltage at the PCB end decreases to 3.3V, and the voltage at the cable end decreases to 3V. Normally a CDC is needed in this design to achieve a desirable voltage regulation at CV mode, for example, the CDC is configured as 300mV.

Then at CV full load, the voltage at the PCB end is around 5.3V, and the voltage at the cable end is around 5V. Correspondingly the CC shutdown occurs when the voltage at the PCB end decreases to 3.6V, and the voltage at the cable end decreases to 3.3V.

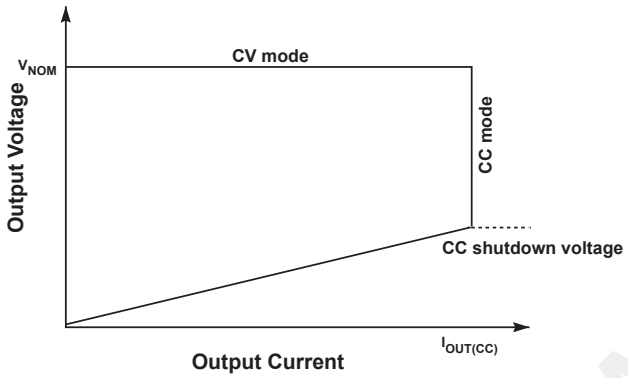


Figure 9.4 : Power Envelope

9.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching

The iW1799 uses a proprietary load/line adaptive multi-mode PWM/PFM control to dramatically improve the light-load efficiency and thus the overall average efficiency.

During the constant voltage (CV) operation, the iW1799 normally operates in a pulse-width-modulation (PWM) mode under heavy load conditions. In the PWM mode, the switching frequency keeps around constant. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. During the PFM mode, the MOSFET is turned on for a set duration under a given instantaneous rectified AC input voltage, but its off time is modulated by the load current. With a decreasing load current, the off-time increases and thus the switching frequency decreases.

When the switching frequency approaches to human ear audio band, the iW1799 transitions to a second level of PWM mode, namely the Deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 22kHz in order to avoid audible noise. As the load current is further reduced, the iW1799 transitions to a second level of PFM mode, namely the Deep PFM mode (DPFM), which can reduce the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level in the DPWM mode before transitioning to the DPFM mode. Therefore, the power converter practically produces no audible noise, while achieving high efficiency across varying load conditions.

The iW1799 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley mode turn on for every PWM/PFM switching cycle, during all PFM and PWM modes and in both CV and CC operations. This unique feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI. The innovative digital control architecture and algorithms together enable the iW1799 to achieve the highest overall efficiency and lowest EMI, without causing audible noise over the entire operating range.

9.7 Less Than 75mW No-Load Power at Typical 5V Output Setting

Under the no-load condition, the iW1799 is operating in the DPFM mode, where the switching frequency can drop as low as 82Hz and still maintain a tight closed-loop control of output voltage. The distinctive DPFM operation allows the use of a relatively large pre-load resistor which helps to reduce the no-load power consumption. In the meantime, the iW1799 implements an intelligent low-power management technique that achieves ultra-low chip operating current at the no-load less than 220µA. Altogether these features ensure with the lowest system cost power supplies built with the iW1799 can achieve with ample margin less than 75mW no-load power consumption at typical 5V output setting and maintain very tight constant voltage and constant current regulation over the entire operating range including the no-load operation. In addition, the no-load power consumption can be reduced to less than 20mW with an optional, external active start-up DFET. No load power consumption is usually measured with load disconnected. The power supply designed with the iW1799 and secondary side controllers, such as the iW656P can detect the load disconnection or portable device unplug and change the output voltage to default 5V. For example, even if the adapter is at 9V or 12V state, it goes to 5V state when no load power consumption is measured with load removed.

9.8 Fast Dynamic Load Response with Secondary-Side Voltage Undershoot Detection

While achieving ultra-low no-load power consumption, the iW1799 implements an innovative proprietary digital control technology via the DLNK pin to ensure fast dynamic load response to sudden load changes on the output.

When a load transient event from light load to heavy load occurs, the output voltage drops. If the output voltage drops to the voltage undershoot threshold, the iW656P or iW657P turns on the LED of the optocoupler by controlling the DRV pin sink current, and the DLNK pin of the iW1799 is pulled down by the transistor of the optocoupler. After the iW1799 receives this DLNK pin signal, it can intelligently confirm if this signal is caused by an undershoot event and distinguish it from a voltage and current request, and then it promptly increases the switching frequency and the t_{ON} to delivery more power to the secondary side in order to bring the output voltage back to regulation.

9.9 Internal Loop Compensation

The iW1799 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

9.10 Voltage Protection Features

The secondary maximum output DC voltage V_{BUS} is limited by the iW1799. In most conditions, when the V_{SENSE} signal at point 1 as indicated in Figure 9.4 exceeds the output OVP threshold, the iW1799 shuts down. While the iW1799 can protect against the V_{OUT} over-voltage through the V_{SENSE} signal in most conditions, it is difficult for the iW1799 to protect the over-voltage caused by output voltage setting mismatch between the iW1799 and the secondary side controller in some abnormal scenarios. For example, if the the secondary-side controller is reset to 5V due to a reset signal from the MD or certain other abnormal signals while the iW1799 stays at present 9V or 12V setting, the over-voltage cannot be detected through V_{SENSE} at the primary side. The iW1799 and Dialog's proprietary secondary-side controller chipset adds one more layer of OVP. When V_{OUT} rises above the over-voltage threshold of the secondary side controller's present state, Dialog's proprietary secondary-side controller drives its DRV pin in a special switching pattern serving as an OVP signal and turns on both the fast and slow discharge. After the iW1799 receives this OVP signal, it shuts down the power supply promptly.

In case of the communication channel failure when the secondary-side controller is not able to send the OVP signal to the iW1799, the iW1799 has a built-in protection scheme to detect the communication channel failures and go to the default 5V state.

Although there is no pin available to directly sense the input voltage, the iW1799 uses an innovative proprietary digital control method to detect and analyze the switch ON time, which provides real-time indirect sensing and monitoring of the magnitude and shape of the DC bulk capacitor voltage. This enables the iW1799 to determine and distinguish various conditions of the AC input voltage such as brown-out, brown-in, and unplug, and to take appropriate actions. When the AC input voltage drops to a below normal operation range and the power supply input is still connected to the AC source, the iW1799 initiates a brown-out protection and shuts down the power supply adaptively according to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis. In the case of the power supply input being unplugged or disconnected from the AC source, the iW1799 continues to control the switching actions to discharge the DC bulk capacitor voltage to a safe level before shutting down the power supply.

Also, the iW1799 monitors the voltage on the V_{CC} pin, and the IC shuts down immediately when the voltage on this pin is below the UVLO threshold. The iW1799 also has a V_{CC} over-voltage protection (V_{CC} OVP). During an abnormal event, if the V_{CC} voltage is higher than the protection threshold, the switching is stopped and the iW1799 shuts down.

When any of these faults are met, the IC remains biased to discharge the V_{CC} supply. Once the V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new start-up cycle. The controller continues to attempt a start-up until the fault condition is removed.

9.11 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built into the iW1799. With the CS/CDC pin the iW1799 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. During any t_{ON} period, if the CS/CDC pin voltage exceeds 0.92V after leading edge blanking, the iW1799 immediately turns off the gate driver until the next switching cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW1799 shuts down.

If the current sense resistor is shorted prior to the power supply startup there is a potential danger that over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault before start-up and the startup process will not be pursued if the fault exists. The V_{CC} is discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up, but does not fully start up until the fault condition is removed.

9.12 CDC Configuration

The iW1799 uses a multi-function CS/CDC pin to allow users to configure cable drop compensation (CDC) externally. This configuration is only performed once. It is completed after the initial OTP check but before the soft-start commences. During the CDC configuration, the internal digital control block senses the external resistance value between the CS/CDC pin and ground, and then sets a corresponding CDC level to allow the device to compensate for IR drop in the secondary circuitry during normal operation.

The iW1799 provides four levels of CDC configurations: 0, 150mV, 300mV, and 450mV. Table 9.1 on the following page shows the resistance range for each of the four CDC levels. In practice, it is recommended to select resistance in the middle of the range wherever possible.

The “Cable Comp” specified in Table 9.1 refers to the voltage increment at the PCB end from no-load to full-load conditions in the CV mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “Cable Comp” is specified based on the CC limit of 5V output and is independent of output voltage. For other output voltages, the actual voltage increment can be the same or lower depending on the CC limit setting.

To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply it by the maximum output current.

R_{CDC} Range (kΩ)		Cable Comp (mV)	V_{SENSE} Threshold for Output OVP at 5V Setting (V)
Min	Max		
0	0.85	300	1.171
1.17	1.76	450	1.199
2.27	2.67	0	1.115
3.36	4.1	150	1.143

Table 9.1: Recommended Resistance Range and Corresponding CDC Levels for 5V Output

9.13 Internal OTP

The iW1799 features an internal OTP which shuts down the device if the internal die junction temperature reaches above T_{SD}. The device is kept off until the junction temperature drops below T_{SD-R}, when the device initiates a new smart start-up process to build up the output voltage.

9.14 External OTP

The iW1799 can be configured to provide external OTP by connecting a Negative-Temperature-Coefficient (NTC) resistor from the SD pin to GND. Internally, a 100µA current source is injected to the SD pin, which generates a voltage proportional to the NTC resistance. At high ambient temperature, the NTC resistance becomes low, which results in a low voltage at the SD pin. If the SD pin voltage drops below an internally-set threshold, then the OTP is triggered, and the iW1799 shuts down.

In the iW1799, the external OTP has a built-in hysteresis by having two thresholds. Before start-up, the OTP is triggered if the SD pin voltage is less than 1.2V; otherwise the device begins the CDC configuration (see Section 9.12), then followed by a normal soft-start process. During normal operation, the OTP threshold is switched to 1.0V, and the device only shuts down when the SD pin voltage is less than 1.0V.

9.15 Advanced Fault Control Technology

In the traditional AC/DC adapter designs, once the control IC detects a fault and shuts down, there are two common ways to responde to a fault:

(a) Shutdown and auto-restart—The switching pulses are sent out in every power-on-reset (POR) cycle after V_{CC} reaches the start-up threshold. In case of the USB cable short or partial short, this can have a high average output current from the USB and high average input power in the adapter, it may generate excessive heat and cause damages. The auto-restart is commonly called “hiccup”.

(b) Shutdown and latch—This normally requires the users to unplug the adapter from the AC input and recycle the power, which can create an inconvenient or bad experience.

To address this issue, the iW1799 implements Dialog’s innovative and proprietary advanced fault control technology. With advanced fault control technology, the power supply only re-starts after pre-defined minimum waiting period. In the iW1799, the advanced fault control technology applies to the faults including output short and “CC shutdown,” etc. With advanced fault control, the minimum restart time after a fault is controlled regardless of AC line voltage. This operation mode continues until the faults are removed. In this way, the advanced fault control technology effectively controls the re-start time and reduces the average output power at the fault conditions.

9.16 V_{IN} OVP and X-cap Discharge

iW1799 provides unique features for V_{IN} OVP protection, or X-cap discharge function, depending on product option. With production options in which V_{IN} OVP is enabled, the DET pin voltage will be used to monitor the input capacitor voltage continuously. If the DET pin voltage is higher than 0.5V, OVP protection will trigger and the iW1799 will shutdown and restart.

With the production options in which the X-cap discharge function is enabled, the DET pin voltage will be used to monitor the X-cap voltage before bridge rectifier. If the DET pin senses that the AC line is disconnected, the X-cap discharge function will be activated.

9.17 Design Considerations

This section provides some design considerations for the iW1799.

IC V_{CC} Supply

If USB PD Rapid Charge applications need to support multiple output voltages ranging from 3.3V to 21V and V_{CC} voltage is usually supplied from an auxiliary winding during normal operation. The transformer should be designed properly to ensure sufficient V_{CC} margin above UVLO at 3.3V output and an external LDO may be needed to keep V_{CC} below maximum operating voltage (40V) at 21V output.

Multi-Level Output Voltage Setting

The default 5V output voltage setting is still determined by the transformer secondary-to-auxiliary winding turns ratio and the external voltage divider connected to the V_{SENSE} pin. Once the 5V default output is set correctly, the other output voltage regulation is guaranteed by an internal circuit and digital controller automatically.

Output Current Limit Setting

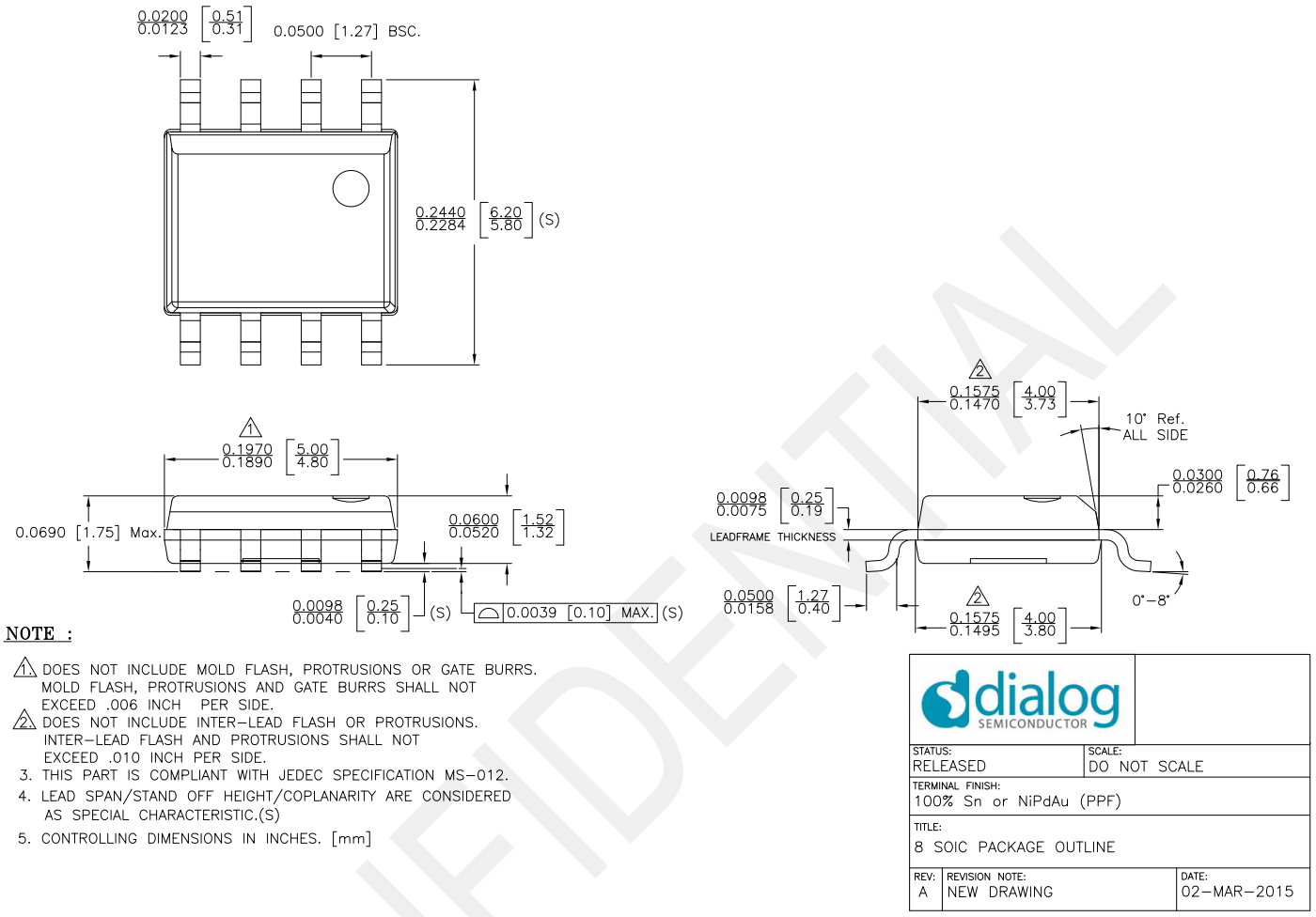
The output CC limit setting is determined by Equation 9.7. Once the secondary-side controller product option, transformer turns ratio, and current sense resistor are determined, the CC limits for all the voltage levels are all set.

9.18 iW1799 Product Options

In order to support a variety of applications with different system requirements, the iW1799 provides several product options. Each product option varies in latching functions, default k_{CC} value at startup, CC shutdown voltage value, and supported DLNK voltage information resolution. Please refer to the Ordering Information table in section 11 for details.

In the ordering information, supported DLNK voltage information resolution only refers to the supported minimum voltage step request in DLNK protocol. It does not represent the actual output voltage regulation resolution.

10 Physical Dimensions



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 INCH PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS–012.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. CONTROLLING DIMENSIONS IN INCHES. [mm]

STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: 100% Sn or NiPdAu (PPF)	
TITLE: 8 SOIC PACKAGE OUTLINE	
REV: A	REVISION NOTE: NEW DRAWING — DATE: 02–MAR–2015

Figure 11.1 : 8-Lead SOIC package outline drawing

11 Ordering Information

Part Number	Options							Package	Description
	Protocol Supported	Default k_{CC} at Start-up	CC Shutdown Voltage	OVP/ OTP Latch	CC Shut-down Latch	Supported DLNK Voltage Information Resolution	V_{IN} OVP or X-cap discharge		
iW1799-02	USB PD/QC	0.422	disabled	No	No	10mV/Step up to 12V	V_{IN} OVP	SOIC-8	Tape & Reel[1]
iW1799-23	USB PD/QC	0.422	2.9V for V_{BUS} < 3.4V; 3.0V for 3.4V ≤ V_{BUS} < 9V; 6.5V for 9V ≤ V_{BUS} < 12V; 10V for V_{BUS} ≥ 12V	Yes	No	10mV/Step up to 12V	V_{IN} OVP	SOIC-8	Tape & Reel[1]
iW1799-32	USB PD/QC	0.422	disabled	No	No	10mV/Step up to 21V	V_{IN} OVP	SOIC-8	Tape & Reel[1]
iW1799-33	USB PD/QC	0.422	disabled	No	No	10mV/Step up to 21V	X-cap discharge	SOIC-8	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

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