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SLG46121

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GreenPAK
Dual Supply Programmable Mixed-signal Matrix

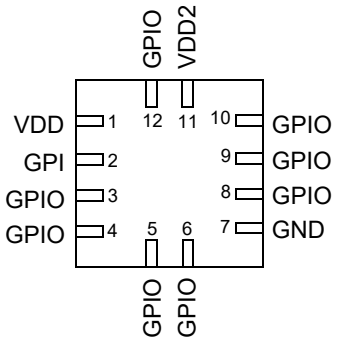
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- 1.8 V (±5%) to 5 V (±10%) VDD
- 1.8 V (±5%) to 5 V (±10%) VDD2 (VDD2 ≤ VDD)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free 12-pin STQFN: 1.6 x 1.6 x 0.55 mm, 0.4 mm pitch

Applications

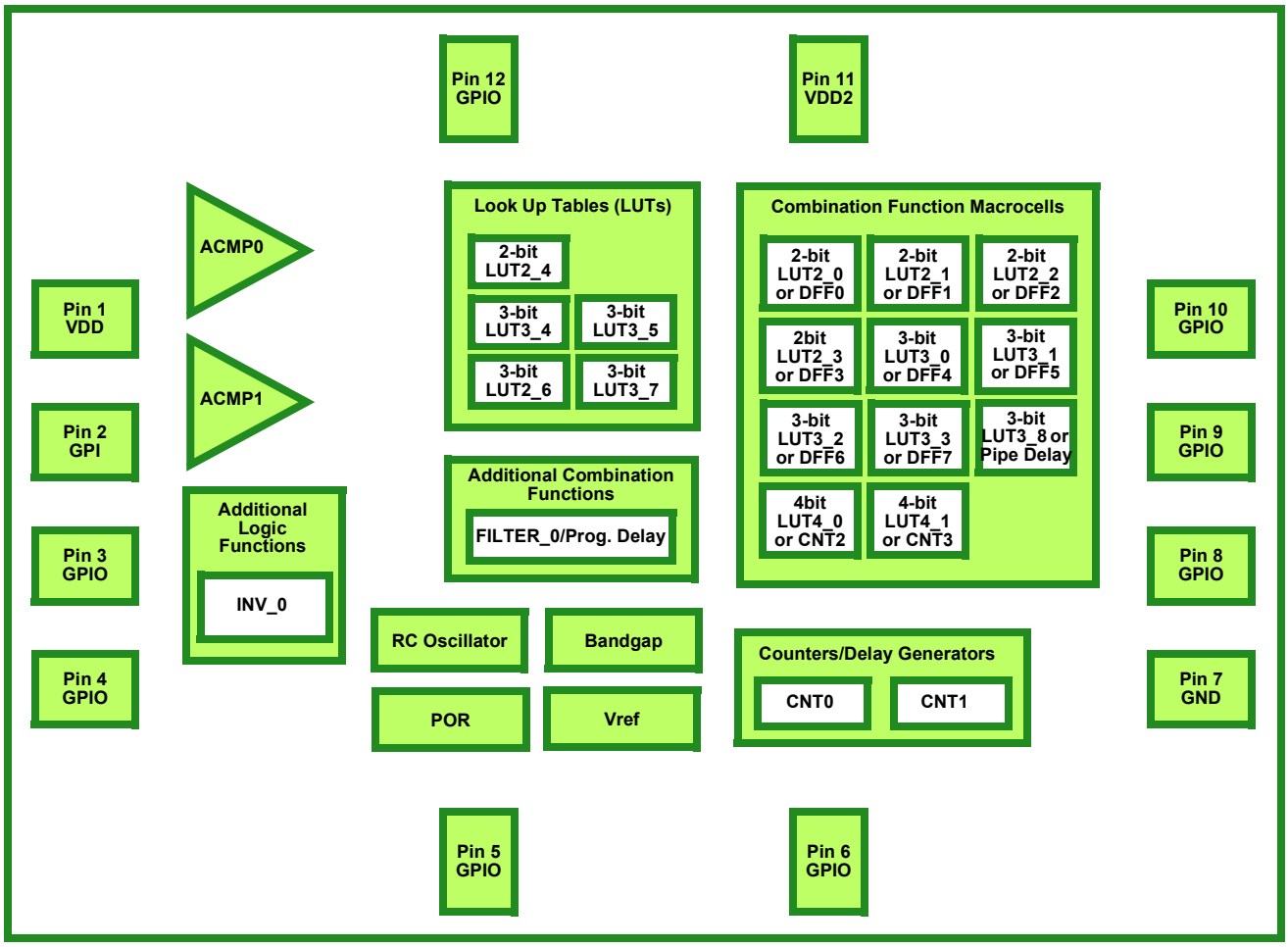
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



STQFN-12
(Top View)

Block Diagram



1.0 Overview

The SLG46121 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46121. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

The additional power supply (VDD2) on the SLG46121 provides the ability to interface two independent voltage domains within the same design. Users can configure pins, dedicated to each power supply, as inputs, outputs, or both (controlled dynamically by internal logic) to both VDD and VDD2 voltage domains. Using the available macrocells designers can implement mixed-signal functions bridging both domains or simply pass through level-translation in both High to Low and Low to High directions.

The macrocells in the device include the following:

- Two Analog Comparators (ACMP)
- Voltage References (Vref)
- Five Combinatorial Look Up Tables (LUTs)
  - One 2-bit LUTs
  - Four 3-bit LUTs
- Twelve Combination Function Macrocell
  - Four Selectable DFF/Latch or 2-bit LUTs
  - Four Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage / 2 output, one 1 stage fixed output
  - Two Selectable Counter/Delay or 4-bit LUT
  - One Programmable Delay / Deglitch Filter
- Two Counter / Delay Generators (CNT/DLY)
  - One 8-bit counter/delay
  - One 14-bit counter/delay with external clock/reset
- Eight D Flip-Flop / Latches (DFF) (Part of Combination Function Macrocell)
- Additional Logic Function - 1 Inverter
- Pipe Delay – 8 stage/2 output (Part of Combination Function Macrocell)
- One Bandgap
- RC Oscillator (RC OSC)
- Power On Reset (POR)

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply (PIN 2, 3, 4, 5, 6)
2	GPI	General Purpose Input
3	GPIO	General Purpose I/O or Analog Comparator 0 (+)
4	GPIO	General Purpose I/O or Analog Comparator 0 (-)
5	GPIO	General Purpose I/O
6	GPIO	General Purpose I/O or Analog Comparator 1 (+) with OE
7	GND	Ground
8	GPIO	General Purpose I/O
9	GPIO	General Purpose I/O
10	GPIO	General Purpose I/O with OE and Vref output
11	VDD2	Power Supply (PIN 8, 9, 10, 12)
12	GPIO	General Purpose I/O or External Clock Input

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46121's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

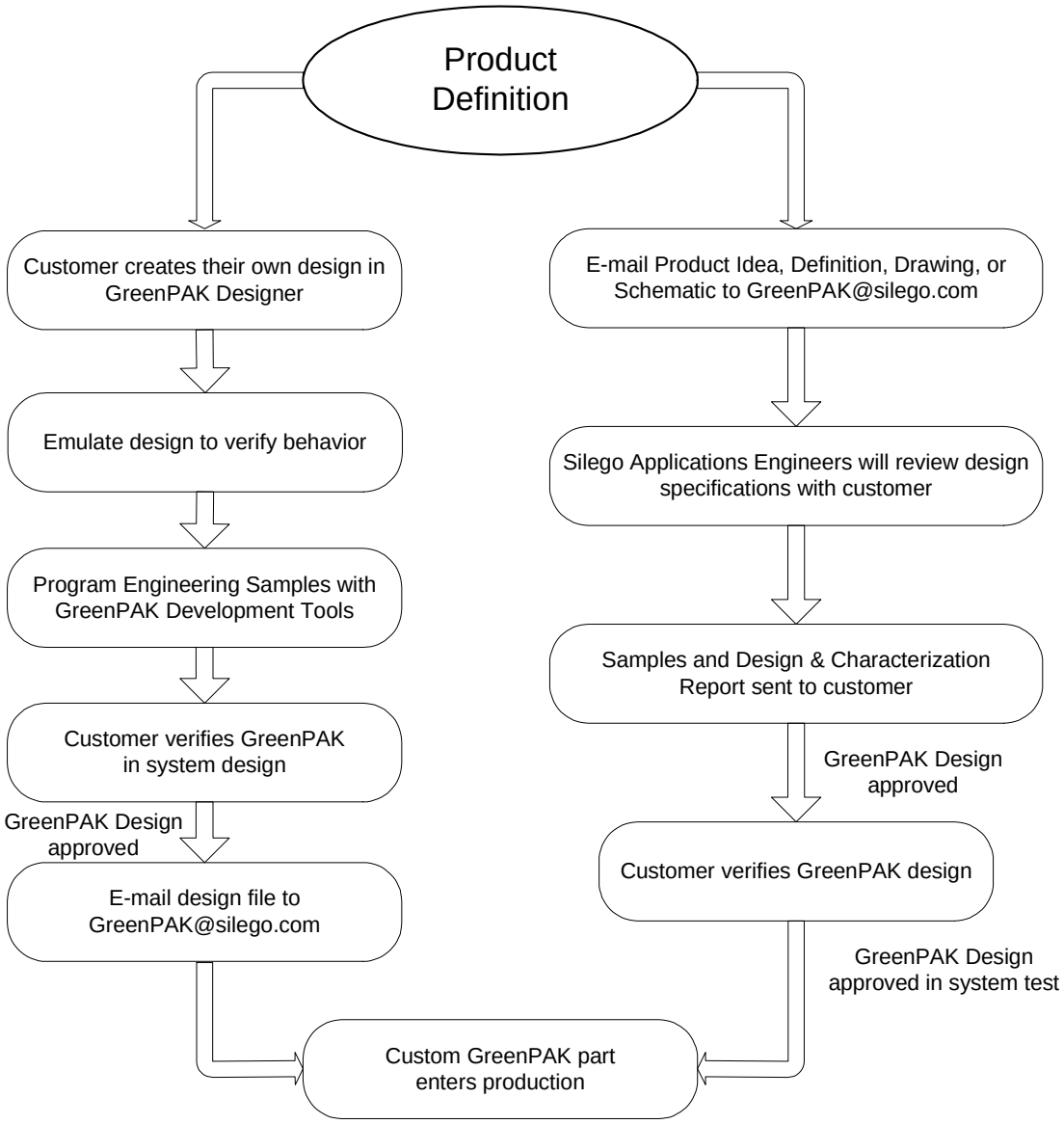


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46121V	12-pin STQFN
SLG46121VTR	12-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	Pins 2,3,4,5,6	GND - 0.5	VDD + 0.5	V
	Pins 8,9,10,12		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
	Push-Pull 2x	--	17	
	OD 1x	--	18	
	OD 2x	--	28	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	VDD2 ≤ VDD	1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.5	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	
		Negative Input	0	--	1.1	
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD}	V
		Low-Level Logic Input	0.980	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.280	0.445	0.600	V
I_{LGK}	Input leakage PIN 2, 3, 4, 5, 6 (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.800	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, I_{OL}= 100 µA	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.010	0.010	V
I_{OH}	HIGH-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.100	2.680	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.136	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	975.92	1061.05	1132.72	kΩ
		100 k Pull Up	99.56	107.15	114.11	kΩ
		10 k Pull Up	11.51	12.86	14.36	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	975.32	1061.05	1133.17	kΩ
		100 k Pull Down	100.43	107.26	114.05	kΩ
		10 k Pull Down	11.17	12.48	13.86	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.75	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	1.780	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V_{DD}	V
		Low-Level Logic Input	1.130	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.498	0.685	0.866	V
I_{LGK}	Input leakage PIN 2, 3, 4, 5, 6 (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.720	3.090	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.850	3.190	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, I_{OL}= 3 mA	--	0.180	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.050	0.070	V
I_{OH}	HIGH-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	6.010	10.150	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.460	19.610	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, V_{OL} = 0.4 V	4.060	6.440	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	8.130	12.360	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	8.130	12.410	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	16.260	22.900	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	976.93	1060.60	1140.64	kΩ
		100 k Pull Up	98.50	106.38	113.21	kΩ
		10 k Pull Up	10.22	11.66	12.95	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	974.63	1060.65	1132.96	kΩ
		100 k Pull Down	99.69	106.50	113.26	kΩ
		10 k Pull Down	9.94	11.46	12.85	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	1.0	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	2.640	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.160	--	V_{DD}	V
		Low-Level Logic Input	1.230	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.694	0.923	1.182	V
I_{LGK}	Input leakage PIN 2, 3, 4, 5, 6 (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.170	4.740	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.320	4.860	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, I_{OL}= 5 mA	--	0.230	0.330	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.070	0.090	V
I_{OH}	HIGH-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	21.980	29.010	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	41.886	55.990	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, V_{OL} = 0.4 V	6.010	9.730	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	11.590	19.460	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	11.760	19.460	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	19.120	35.952	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	972.75	1060.76	1134.23	kΩ
		100 k Pull Up	98.89	106.16	112.84	kΩ
		10 k Pull Up	9.27	11.11	12.62	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	968.47	1060.59	1138.02	kΩ
		100 k Pull Down	99.49	106.23	113.02	kΩ
		10 k Pull Down	9.06	10.97	12.57	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.5 Electrical Characteristics (1.8V ±5% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	VDD2 ≤ VDD	1.71	1.80	1.89	V
I_{LGK}	Input leakage PIN 8, 9, 10, 12 (Absolute Value)		--	1	1000	nA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input	1.100	--	V_{DD2}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD2}	V
		Low-Level Logic Input	0.980	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.800	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 100 µA	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.010	0.010	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.100	2.680	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.136	--	mA
I_{VDD2}	Maximum Average or DC Current Through VDD2 Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.6 Electrical Characteristics (3.3V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	VDD2 ≤ VDD	1.71	--	V_{DD2}	V
I_{LGK}	Input leakage PIN 8, 9, 10, 12 (Absolute Value)		--	1	1000	nA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	1.100	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.270	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.980	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	--	--	0.690	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	--	--	0.440	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	--	--	0.520	V
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.700	1.800	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.010	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	2.100	2.680	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	3.060	5.136	--	mA
I_{VDD2}	Maximum Average or DC Current Through VDD2 Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.7 Electrical Characteristics (5V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	VDD2 ≤ VDD	1.71	--	V_{DD2}	V
I_{LGK}	Input leakage PIN 8, 9, 10, 12 (Absolute Value)		--	1	1000	nA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 3.3 V	1.780	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	2.130	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	1.130	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 3.3 V	--	--	1.210	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	--	--	0.950	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	--	--	0.690	V
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA, V_{DD2} = 3.3 V	2.720	3.090	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA, V_{DD2} = 3.3 V	2.850	3.190	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.180	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.090	0.130	V
		Open Drain NMOS 1X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.090	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.050	0.070	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V, V_{DD2} = 3.3 V	6.010	10.150	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V, V_{DD2} = 3.3 V	11.460	19.610	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	4.060	6.440	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	8.130	12.360	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	8.130	12.410	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	16.260	22.900	--	mA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.270	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.980	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	--	--	0.690	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	--	--	0.440	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	--	--	0.520	V
I_{IH2}	HIGH-Level Input Current PIN 8, 9, 10, 12	Logic Input Pins; V_{IN} = 1.8 V, V_{DD2} = 1.8 V	-1.0	--	1.0	µA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{IL2}	LOW-Level Input Current PIN 8, 9, 10, 12	Logic Input Pins; V_{IN} = 0 V, V_{DD2} = 1.8 V	-1.0	--	1.0	µA
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.700	1.800	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.010	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	2.100	2.680	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	3.060	5.136	--	mA
I_{VDD2}	Maximum Average or DC Current Through VDD2 Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.8 IDD Estimator

Table 1. Typical Current estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	µA
		Vref	55.7	56.0	62.5	µA
		Vref Buffer (each)	0.6	14.1	14.6	µA
		OSC 25 kHz, predivide = 1	3.1	4.7	6.4	µA
		OSC 25 kHz, predivide = 8	3.0	4.3	5.8	µA
		OSC 2 MHz, predivide = 1	29.3	51.0	79.8	µA
		OSC 2 MHz, predivide = 8	17.4	23.2	29.0	µA
		1st ACMP used (includes Vref)	59.6	60.0	66.5	µA
		Each additional ACMP add	3.9	4.0	4.0	µA

5.9 Timing Estimator

Table 2. Typical Delay estimated for each macrocell.

Symbol	Parameter	Note	V_{DD}/V_{DD2} = 1.8V		V_{DD}/V_{DD2} = 3.3V		V_{DD}/V_{DD2} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull	44.2	43.5	17.8	18.2	12.7	13.0	ns
tpd	Delay	Digital Input with Schmitt Trigger -- Push Pull	43.3	42.5	17.7	18.0	12.6	13.0	ns
tpd	Delay	Low Voltage Digital input -- Push Pull	45.6	517.0	18.1	215.3	12.7	144.9	ns
tpd	Delay	Digital Input without Schmitt Trigger -- NMOS	—	83.8	—	29.9	—	19.5	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	44.8	—	17.9	—	12.6	—	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0		43.4		17.7		12.8	ns
tpd	Delay	2-bit LUT	18.7	22.1	8.0	8.7	5.8	6.0	ns
tpd	Delay	Latch (2-bit LUT shared macrocell inputs)	26.5	30.8	11.3	12.3	8.1	8.5	ns
tpd	Delay	3-bit LUT	21.3	24.4	9.1	9.6	6.5	6.6	ns
tpd	Delay	3-bit LUT (LATCH shared macrocell inputs)	26.8	25.4	11.2	10.2	8.0	7.1	ns
tpd	Delay	Latch with nRST/nSET (3-bit LUT shared macrocell inputs)	29.7	34.7	12.6	13.9	9.1	9.6	ns
tpd	Delay	4-bit LUT (shared macrocell inputs)	34.0	32.6	14.4	13.0	10.3	9.1	ns
tpd	Delay	2-bit LUT (Latch shared macrocell inputs)	26.8	25.4	11.2	10.2	8.0	7.1	ns
tpd	Delay	CNT/DLY	44.2	38.8	18.7	16.4	13.3	11.8	ns
tpd	Delay	CNT/DLY (shared macrocell inputs)	43.2	39.7	18.4	16.8	13.0	12.1	ns
tpd	Delay	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	38.2	—	16.0	—	11.4	—	ns
tpd	Delay	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	—	40.4	—	16.4	—	11.6	ns
tpd	Delay	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	38.2	40.5	15.9	16.5	11.3	11.5	ns
tpd	Delay	Filter	191.6	193	77.4	77.8	50.7	52.1	ns

5.10 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
offset	25 kHz	auto	19	14	12	µs
offset	2 MHz	auto	7	4	4	µs
frequency settling time	25 kHz	auto	19	14	12	µs
frequency settling time	2 MHz	auto	14	14	14	µs
variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25 kHz/ 2 MHz	either	35	14	10	ns

5.11 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical).

Symbol	Parameter	Note	V_{DD}/V_{DD2}= 1.8V	V_{DD}/V_{DD2}= 3.3V	V_{DD}/V_{DD2} = 5.0V	Unit
time1	Width, 1 cell	PDLY mode:(any)edge detect, edge detect output	256.7	120.8	110	ns
time1	Width, 2 cell	PDLY mode:(any)edge detect, edge detect output	564.4	262.7	225	ns
time1	Width, 3 cell	PDLY mode:(any)edge detect, edge detect output	873.5	405	340	ns
time1	Width, 4 cell	PDLY mode:(any)edge detect, edge detect output	11.82.3	547.5	450	ns
time2	Delay, 1 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20	14	ns
time2	Delay, 2 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20.1	14	ns
time2	Delay, 3 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20.1	14	ns
time2	Delay, 4 cell	PDLY mode:(any)edge detect, edge detect output	48.3	20.1	14	ns
time1	Delay, 1 cell	PDLY mode: both edge delay (shared macrocell inputs)	357.9	162.2	110	ns
time1	Delay, 2 cell	PDLY mode: both edge delay (shared macrocell inputs)	666.1	304.3	220	ns
time1	Delay, 3 cell	PDLY mode: both edge delay (shared macrocell inputs)	974.7	446.3	335	ns
time1	Delay, 4 cell	PDLY mode: both edge delay (shared macrocell inputs)	1283.8	588.8	450	ns
time1	Width	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	136.6	73.4	140	ns
time1	Width	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	130.6	71	140	ns
time1	Width	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	133.05	72	140	ns

5.12 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance.

Parameter	V_{DD}/V_{DD2}= 1.8V	V_{DD}/V_{DD2}= 3.3V	V_{DD}/V_{DD2}= 5.0V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain NMOS and Open Drain PMOS Outputs
- Push Pull Outputs
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV and selectable gain 1x/0.5x/0.33x/0.25x

6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins

6.5 Combinational Logic Look Up Tables (LUTs – 5 total)

- One 2-bit Lookup Tables
- Four 3-bit Lookup Tables

6.6 Combination Function Macrocells (12 total)

- Four Selectable DFF/Latches or 2-bit LUTs
- Four Selectable DFF/Latches or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- Two Selectable CNT/DLYs or 4-bit LUTs
- One Programmable Delay or Deglitch Filter

6.7 Delays/Counters (2 total)

- One 8-bit delay/counter with external clock/reset: Range 1-255 clock cycles
- One 14-bit delay/counter with external clock: Range 1-16383 clock cycles

6.8 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1-8 stage selectable outputs
- One 1 stage fixed output

6.9 Additional Logic Functions (Part of Combination Function Macrocell)

- One Deglitch filter macrocell
- One Programmable Delay
  - 163 ns / 305 ns / 446 ns / 588 ns @ 3.3 V
  - Includes Edge Detection function

6.10 Additional Logic Function

- One Inverter

6.11 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First Stage Clock pre=divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider control with two outputs, OUT0 and OUT1 (8): selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

6.12 Power On Reset (POR)

7.0 I/O Pins

The SLG46121 has a total of 9 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference). Refer to Section 2.0 Pin Description for pin definitions.

All of the 9 user defined I/O pins on the SLG46121, except Pin 2 can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

The high side of the user selectable push-pull or open-drain pin output structures for each GPIO is connected to either VDD or VDD2. This allows for the appropriate voltage level output compatible with each voltage domain. The level shifters are located in lower power IO PADs (pins 8, 9, 10 and 12) powered from VDD2. All configuration registers of the SLG46121 are powered from VDD, so it is possible to maintain the configuration information even after VDD2 was turned off, discharged and turned back on again.

Pins 2, 3, 4, 5 and 6 are powered V_{DD} and pins 8, 9, 10 and 12 are powered from $V_{DD2.}$ All internal macrocells are powered from $V_{DD.}$ Voltage on V_{DD2} Pin must be less or equal voltage on V_{DD} Pin.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as input, ESD pin protection diodes must be considered when applying an input signal to the pin. This will cause a significant current leakage.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as Output, the pin will behave as NMOS Open Drain.

It is not recommended to connect V_{DD2} to the GND.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. Pins 3, 4, and 6 can also be configured to serve as analog inputs to the on-chip comparators.

7.2 Output Modes

Pins 3, 4, 5, 6, 8, 9, 10, and 12 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 6. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	reg <624:623>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	reg <626:625>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 7. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	reg <629:627>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 3 Pull Up/Down Resistor Value Selection	reg <631:630>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <632>	0: Pull Down Resistor 1: Pull Up Resistor
PIN3 Driver Strength Selection	reg <633>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 8. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control	reg <636:634>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 4 Pull Up/Down Resistor Value Selection	reg <638:637>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	reg <639>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 4 Driver Strength Selection	reg <640>	0: 1X 1: 2X

7.4.4 PIN 5 Register Settings

Table 9. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Mode Control	reg <643:641>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved & Open Drain NMOS
PIN 5 Pull Up/Down Resistor Value Selection	reg <645:644>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	reg <646>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 5 Driver Strength Selection	reg <647>	0: 1X 1: 2X

7.4.5 PIN 6 Register Settings

Table 10. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control (sig_PIN6_oe =0)	reg <649:648>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input / Output
PIN 6 Mode Control (sig_PIN6_oe =1)	reg <651:650>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 6 Pull Up/Down Resistor Value Selection	reg <653:652>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	reg <654>	0: Pull Down Resistor 1: Pull Up Resistor

7.5 PIN 8 Register Settings

Table 11. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	reg <657:655>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
PIN 8 Pull Up/Down Resistor Value Selection	reg <659:658>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	reg <660>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <661>	0: 1X 1: 2X

7.5.1 PIN 9 Register Settings

Table 12. PIN 9 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 9 Mode Control	reg <664:662>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open drain NMOS
PIN 9 Pull Up/Down Resistor Value Selection	reg <666:665>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 9 Pull Up/Down Resistor Selection	reg <667>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <668>	0: 1X 1: 2X

7.6 PIN 10 Register Settings

Table 13. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control (sig_PIN10_oe =0)	reg <670:669>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 10 Mode Control (sig_PIN10_oe =1)	reg <672:671>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 10 Pull Up/Down Resistor Value Selection	reg <674:673>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	reg <675>	0: Pull Down Resistor 1: Pull Up Resistor

7.7 PIN 12 Register Settings

Table 14. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control	reg <685:683>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain NMOS 111: Open Drain NMOS
PIN 12 Pull Up/Down Resistor Value Selection	reg <687:686>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	reg <688>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 Driver Strength Selection	reg <689>	0: 1X 1: 2X

7.8 GPI IO Structure

7.8.1 GPI IO Structure (for Pin 2)

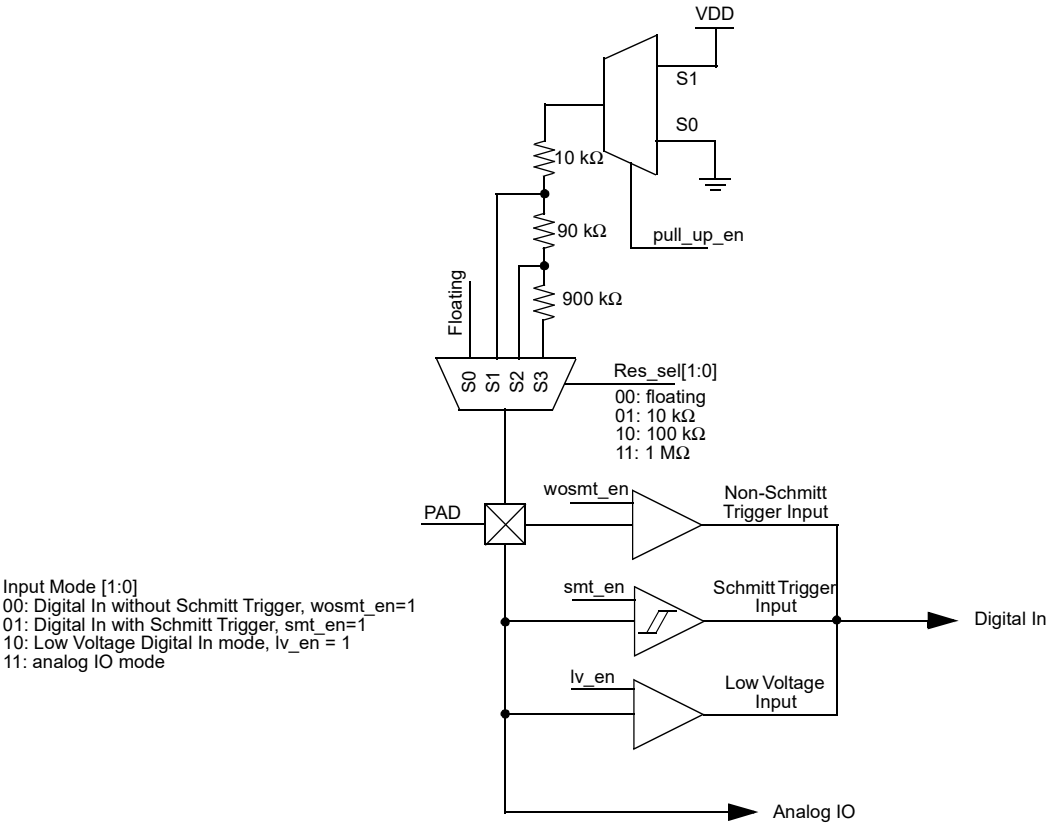


Figure 2. PIN 2 GPI IO Structure Diagram

7.9 Matrix OE IO Structure

7.9.1 Matrix OE IO Structure (for Pin 6)

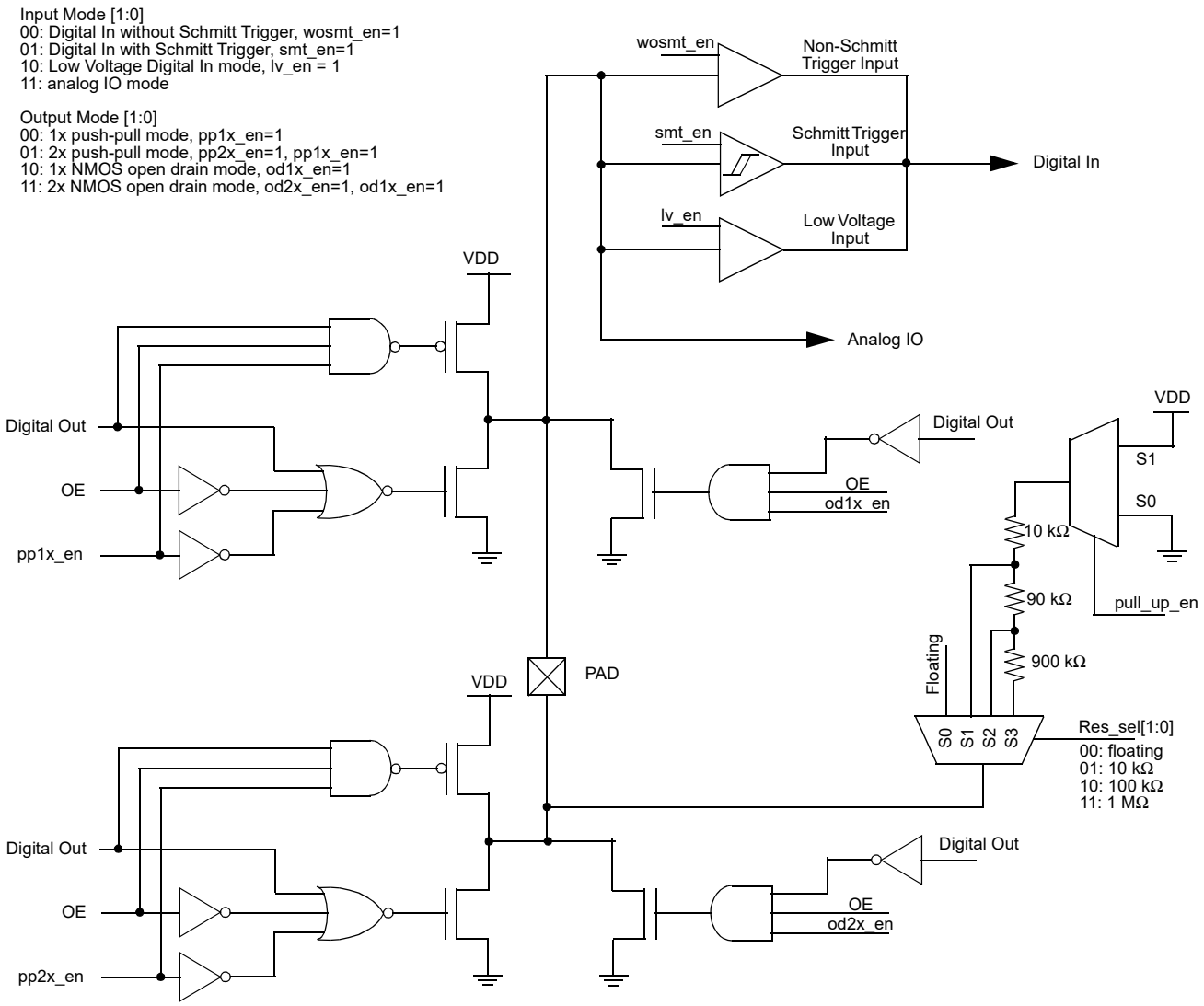


Figure 3. Matrix OE IO Structure Diagram

7.9.2 Matrix OE IO Structure (for Pin 10)

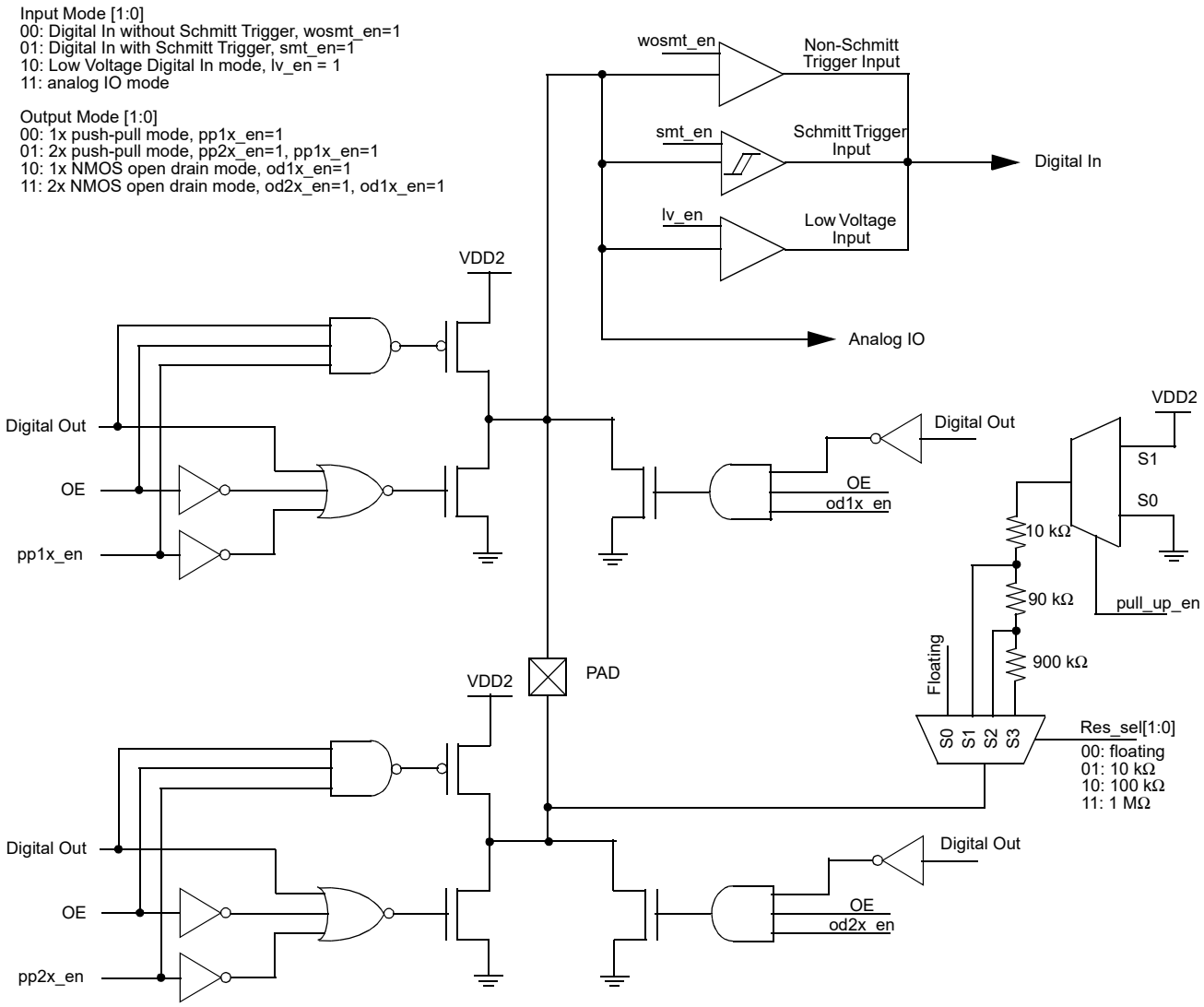


Figure 4. Matrix OE IO Structure Diagram

7.10 Register OE IO Structure

7.10.1 Register OE IO Structure (for Pins 3, 4, 5)

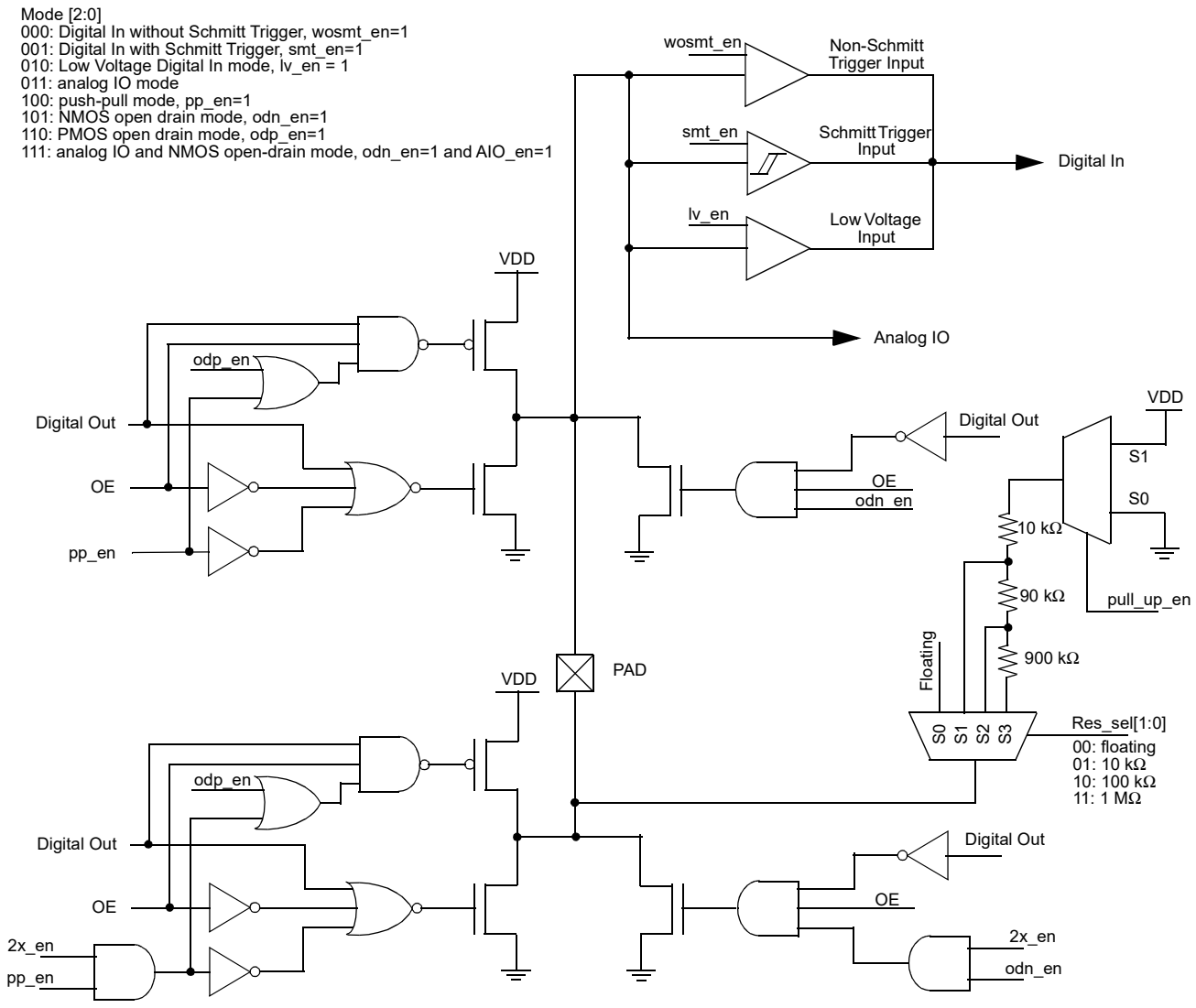


Figure 5. Register OE IO Structure Diagram

7.10.2 Register OE IO Structure (for Pins 8, 9, 12)

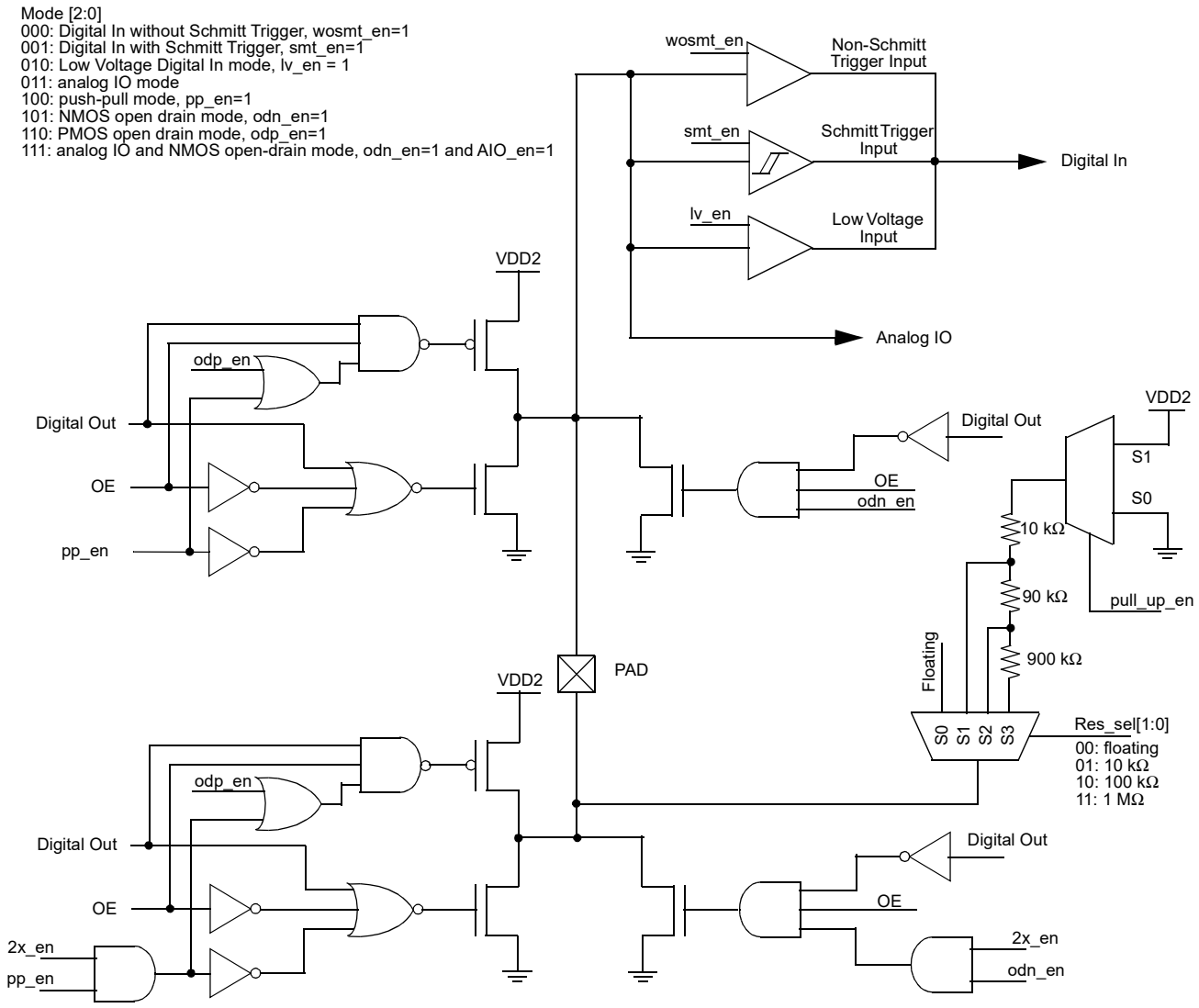


Figure 6. Register OE IO Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46121 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection points for each logic cell within the SLG46121 have a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 768 register bits within the SLG46121 are programmed a fully custom circuit will be created.

The Connection Matrix has 40 inputs and 64 outputs. Each of the 40 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, analog comparators, other digital resources and V_{DD} and V_{SS}. The input to a digital macrocell uses a 6-bit register to select one of these 40 input lines.

For a complete list of the SLG46121’s register table, see Section 17.0 Appendix A - SLG46121 Register Definition.

Matrix Input Signal Functions	N
VSS	0
Pin 2 Digital In	1
Pin 3 Digital In	2
Pin 4 Digital In	3
⋮	⋮
PIN12 Digital In	38
VDD	39

Matrix Inputs

Matrix Outputs

N	0	1	2	⋯	63
Registers	reg <5:0>	reg <11:6>	reg <17:12>	⋯	reg <383:378>
Function	PIN3 Digital Output Source	PIN4Digital Output Source	PIN5 Digital Output Source	⋯	PIN10 Output Enable

Figure 7. Connection Matrix

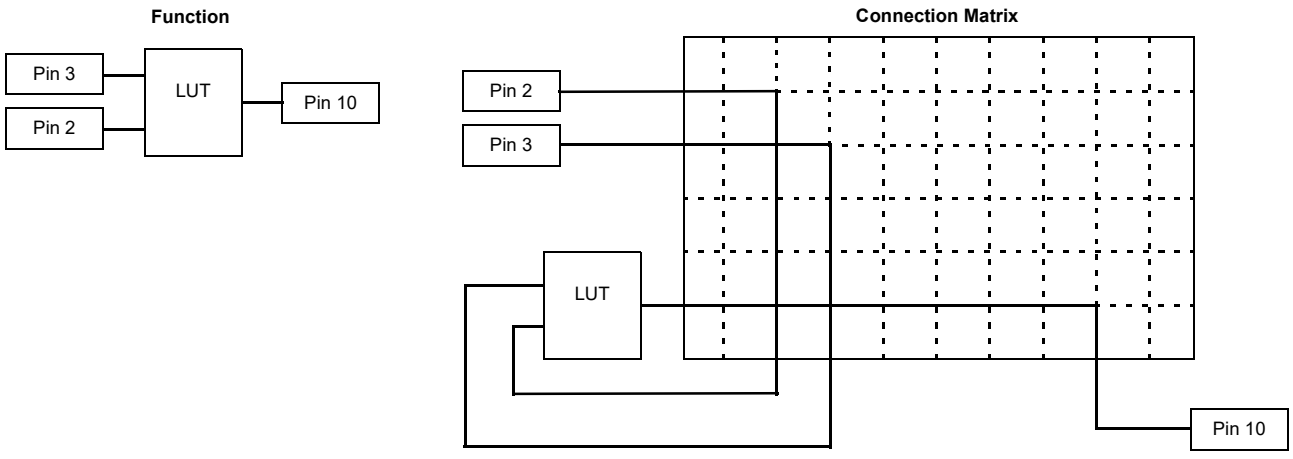


Figure 8. Connection Matrix Example

8.1 Matrix Input Table

Table 15. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	VSS	0	0	0	0	0	0
1	pin2 digital Input	0	0	0	0	0	1
2	pin3 digital Input	0	0	0	0	1	0
3	pin4 digital Input	0	0	0	0	1	1
4	pin5 digital Input	0	0	0	1	0	0
5	pin6 digital Input	0	0	0	1	0	1
6	LUT2_0 output (DFF/LATCH_0 output)	0	0	0	1	1	0
7	LUT2_1 output (DFF/LATCH_1 output)	0	0	0	1	1	1
8	LUT2_2 output (DFF/LATCH_2 output)	0	0	1	0	0	0
9	LUT2_3 output (DFF/LATCH_3 output)	0	0	1	0	0	1
10	LUT2_4 output	0	0	1	0	1	0
11	sig_1pipe_dly_out (1st stage pipe delay output)	0	0	1	0	1	1
12	LUT3_0 output (DFF/LATCH_4 output with resetb or seb)	0	0	1	1	0	0
13	LUT3_1 output (DFF/LATCH_5 output with resetb or seb)	0	0	1	1	0	1
14	LUT3_2 output (DFF/LATCH_6 output with resetb or seb)	0	0	1	1	1	0
15	LUT3_3 output (DFF/LATCH_7 output with resetb or seb)	0	0	1	1	1	1
16	LUT3_4 output	0	1	0	0	0	0
17	LUT3_5 output	0	1	0	0	0	1
18	LUT3_6 output	0	1	0	0	1	0
19	LUT3_7 output	0	1	0	0	1	1
20	LUT3_8 output (pipe delay output0)	0	1	0	1	0	0
21	LUT4_0 output (CNT_DLY3 output (8 bit w/ ext CK,reset))	0	1	0	1	0	1
22	LUT4_1 output (CNT_DLY4 output (8 bit w/ ext CK,reset))	0	1	0	1	1	0
23	CNT_DLY0(14bit) output	0	1	0	1	1	1
24	CNT_DLY1 output (8 bit w/ ext CK,reset)	0	1	1	0	0	0
25	Edge detector output from CNT_DLY4	0	1	1	0	0	1
26	ACMP_0 output	0	1	1	0	1	0
27	ACMP_1 output	0	1	1	0	1	1
28	pipe delay output1	0	1	1	1	0	0
29	Programmable delay with edge detector output (Deglitch filter output)	0	1	1	1	0	1
30	internal oscillator output (one of /1, /2, /3, /4, /8, /12, /24, /64 selected by REG)	0	1	1	1	1	0
31	internal oscillator output (one of /1, /2, /3, /4, /8, /12, /24, /64 selected by REG)	0	1	1	1	1	1
32	Bandgap OK signal	1	0	0	0	0	0
33	Resetb_core as matrix input	1	0	0	0	0	1
34	pin8 digital Input	1	0	0	0	1	0
35	pin9 digital Input	1	0	0	0	1	1

Table 15. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
36	pin10 digital Input	1	0	0	1	0	0
37	Inverter INV_0 Output	1	0	0	1	0	1
38	Pin12 digital Input	1	0	0	1	1	0
39	VDD	1	0	0	1	1	1

8.2 Matrix Output Table

Table 16. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <5:0>	Pin 3 digital out source	0
reg <11:6>	Pin 4 digital out source	1
reg <17:12>	Pin 5 digital out source	2
reg <23:18>	Pin 6 digital out source	3
reg <29:24>	Pin 6 output enable	4
reg <35:30>	in0 of LUT2_0 (Clock Input of DFF0)	5
reg <41:36>	in1 of LUT2_0 (Data Input of DFF0)	6
reg <47:42>	in0 of LUT2_1 (Clock Input of DFF1)	7
reg <53:48>	in1 of LUT2_1 (Data Input of DFF1)	8
reg <59:54>	in0 of LUT2_2 (Clock Input of DFF2)	9
reg <65:60>	in1 of LUT2_2 (Data Input of DFF2)	10
reg <71:66>	in0 of LUT2_3 (Clock Input of DFF3)	11
reg <77:72>	in1 of LUT2_3 (Data Input of DFF3)	12
reg <83:78>	in0 of LUT2_4	13
reg <89:84>	in1 of LUT2_4	14
reg <95:90>	in0 of Inverter INV_0	15
reg <101:96>	Pin 12 digital out source	16
reg <107:102>	in0 of LUT3_0 (Clock Input of DFF4 with nReset/nSet)	17
reg <113:108>	in1 of LUT3_0 (Data input of DFF4 with nReset/nSet)	18
reg <119:114>	in2 of LUT3_0 (Resetb or Setb of DFF4 with nReset/nSet)	19
reg <125:120>	in0 of LUT3_1 (Clock Input of DFF5 with nReset/nSet)	20
reg <131:126>	in1 of LUT3_1 (Data input of DFF5 with nReset/nSet)	21
reg <137:132>	in2 of LUT3_1 (Resetb or Setb of DFF5 with nReset/nSet)	22
reg <143:138>	in0 of LUT3_2 (Clock Input of DFF6 with nReset/nSet)	23
reg <149:144>	in1 of LUT3_2 (Data input of DFF6 with nReset/nSet)	24
reg <155:150>	in2 of LUT3_2 (Resetb or Setb of DFF6 with nReset/nSet)	25
reg <161:156>	in0 of LUT3_3 (Clock Input of DFF7 with nReset/nSet)	26
reg <167:162>	in1 of LUT3_3 (Data input of DFF7 with nReset/nSet)	27
reg <173:168>	in2 of LUT3_3 (Resetb or Setb of DFF7 with nReset/nSet)	28
reg <179:174>	in0 of LUT3_4	29
reg <185:180>	in1 of LUT3_4	30
reg <191:186>	in2 of LUT3_4	31
reg <197:192>	in0 of LUT3_5	32
reg <203:198>	in1 of LUT3_5	33
reg <209:204>	in2 of LUT3_5	34
reg <215:210>	in0 of LUT3_6	35
reg <221:216>	in1 of LUT3_6	36
reg <227:222>	in2 of LUT3_6	37

Table 16. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <233:228>	in0 of LUT3_7	38
reg <239:234>	in1 of LUT3_7	39
reg <245:240>	in2 of LUT3_7	40
reg <251:246>	in0 of LUT3_8 (Input of pipe delay)	41
reg <257:252>	in1 of LUT3_8 (Resetb of pipe delay)	42
reg <263:258>	in2 of LUT3_8 (Clock of pipe delay)	43
reg <269:264>	in0 of LUT4_0 (Input for Delay2 ext. clock or Counter2 8bit external Clock)	44
reg <275:270>	in1 of LUT4_0 (Input for delay2 or counter2 reset input)	45
reg <281:276>	in2 of LUT4_0	46
reg <287:282>	in3 of LUT4_0	47
reg <293:288>	in0 of LUT4_1 (Input for Delay3 ext. clock or Counter3 8bit external Clock)	48
reg <299:294>	in1 of LUT4_1 (Input for delay3 or counter3 reset input)	49
reg <305:300>	in2 of LUT4_1	50
reg <311:306>	in3 of LUT4_1	51
reg <317:312>	Input for delay0 or counter0 (14bits) external clock	52
reg <323:318>	Input for Delay1 ext. clock or Counter1 8bit external Clock	53
reg <329:324>	Input for delay1 or counter1 reset input	54
reg <335:330>	Not used	55
reg <341:336>	pdb for ACMP0	56
reg <347:342>	pdb for ACMP1	57
reg <353:348>	Input for programmable delay for edge detector (Deglitch filter input)	58
reg <359:354>	Power down for osc. (higher priority) (high = power down).	59
reg <365:360>	Pin 8 digital out source	60
reg <371:366>	Pin 9 digital out source	61
reg <377:372>	Pin 10 digital out source	62
reg <383:378>	Pin 10 output enable	63

9.0 Combinatorial Logic

Combinatorial logic is supported via five Lookup Tables (LUTs) within the SLG46121. There is one 2-bit LUT and four 3-bit LUTs. The device also includes 11 Combination Function Macrocells that can be used as LUTs. For more details, please see Section 10.0 Combination Function Macrocells.

Inputs/Outputs for the four LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-Bit LUT

The one 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. ..

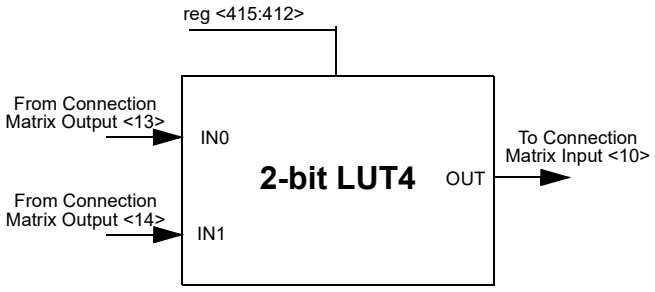


Figure 9. 2-bit LUT

Table 17. 2-bit LUT4 Truth Table.

IN1	IN0	OUT
0	0	reg <412>reg
0	1	reg <413>reg
1	0	reg <414>reg
1	1	reg <415>reg

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT4 is defined by reg <415:412>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 18. 2-bit LUT Standard Digital Functions.

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.2 3-Bit LUT

The four 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

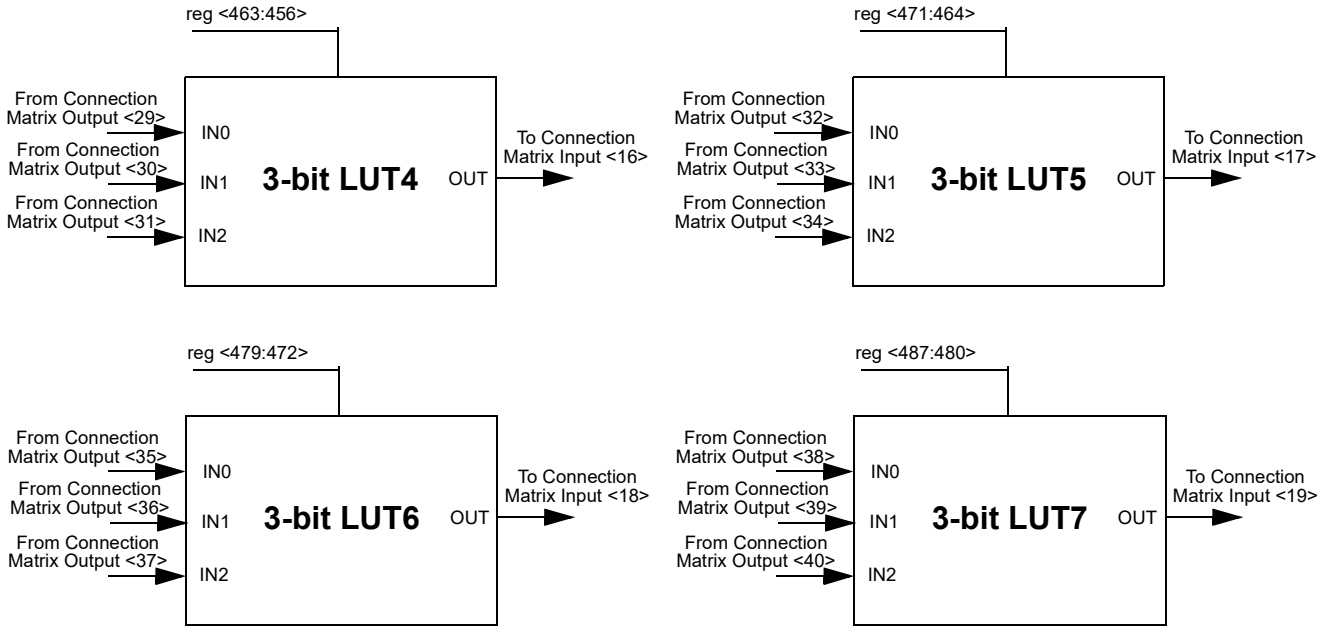


Figure 10. 3-bit LUTs

Table 19. 3-bit LUT4 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <456>
0	0	1	reg <457>
0	1	0	reg <458>
0	1	1	reg <459>
1	0	0	reg <460>
1	0	1	reg <461>
1	1	0	reg <462>
1	1	1	reg <463>

Table 20. 3-bit LUT5 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <464>
0	0	1	reg <465>
0	1	0	reg <466>
0	1	1	reg <467>
1	0	0	reg <468>
1	0	1	reg <469>
1	1	0	reg <470>
1	1	1	reg <471>

Table 21. 3-bit LUT6 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <472>
0	0	1	reg <473>
0	1	0	reg <474>
0	1	1	reg <475>
1	0	0	reg <476>
1	0	1	reg <477>
1	1	0	reg <478>
1	1	1	reg <479>

Table 22. 3-bit LUT7 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <480>
0	0	1	reg <481>
0	1	0	reg <482>
0	1	1	reg <483>
1	0	0	reg <484>
1	0	1	reg <485>
1	1	0	reg <486>
1	1	1	reg <487>

Each 3-bit LUT uses a 8-bit register signal to define their output functions;

3-Bit LUT4 is defined by reg <463:456>

3-Bit LUT5 is defined by reg <471:464>

3-Bit LUT6 is defined by reg <479:472>

3-Bit LUT7 is defined by reg <487:480>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 3-bit LUT logic cells.

Table 23. 3-bit LUT Standard Digital Functions.

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

10.0 Combination Function Macrocells

The SLG46121 has twelve combination function macrocells that can serve more than one logic or timing function. In elven of these cases, they can serve as a Look Up Table (LUT), or as another logic or timing function. In the last case, it can serve as either a programmable delay or deglitch filter. See the list below for the functions that can be implemented in these macrocells.

- Four macrocells that can serve as either 2-bit LUTs or as D Flip Flops
- Four macrocells that can serve as either 3-bit LUTs or as D Flip Flops
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- Two macrocells that can serve as either 4-bit LUTs or as 8-Bit Counter / Delays
- One macrocell that can serve as either a Programmable Delay or as a Deglitch Filter

Inputs/Outputs for the eleven combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

When used as a D Flip Flop / Latch, the source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state, and all have the option to connect both the Q and Q Bar outputs to the connection matrix. The macrocells DFF4, DFF5, DFF6 and DFF7 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CLK = 0, then Q = D

10.1 2-Bit LUT or D Flip Flop Macrocells

There are four macrocells that can serve as either 2-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (d) and clock (clk) inputs for the Flip Flop, with the output going back to the connection matrix.

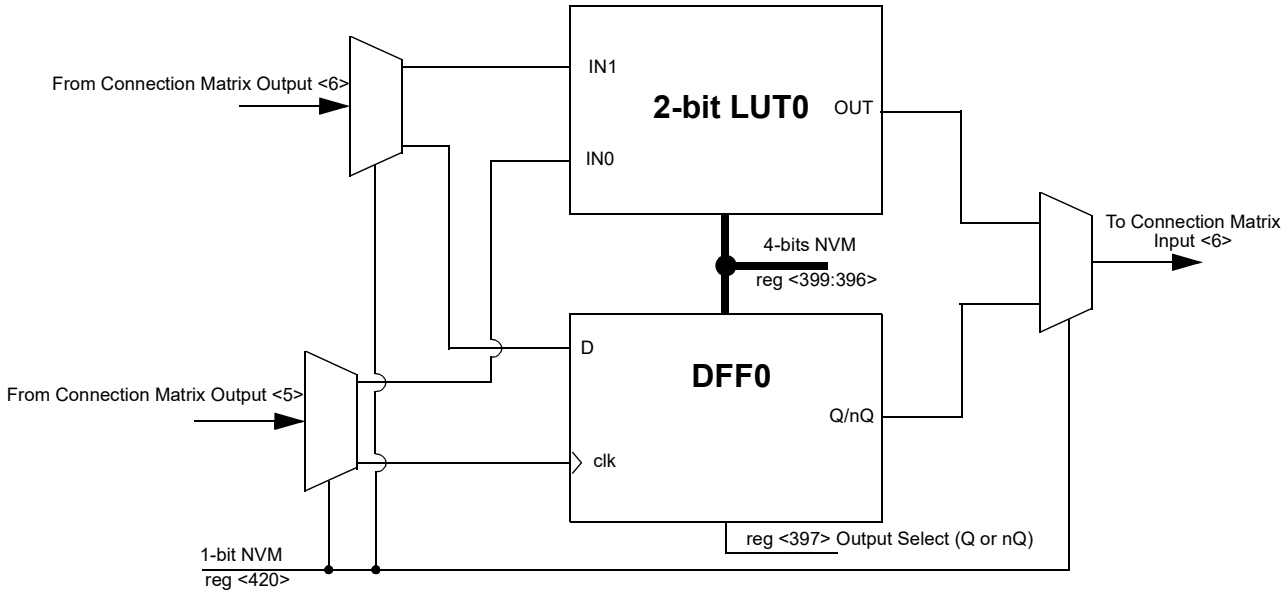


Figure 11. 2-bit LUT0 or DFF0

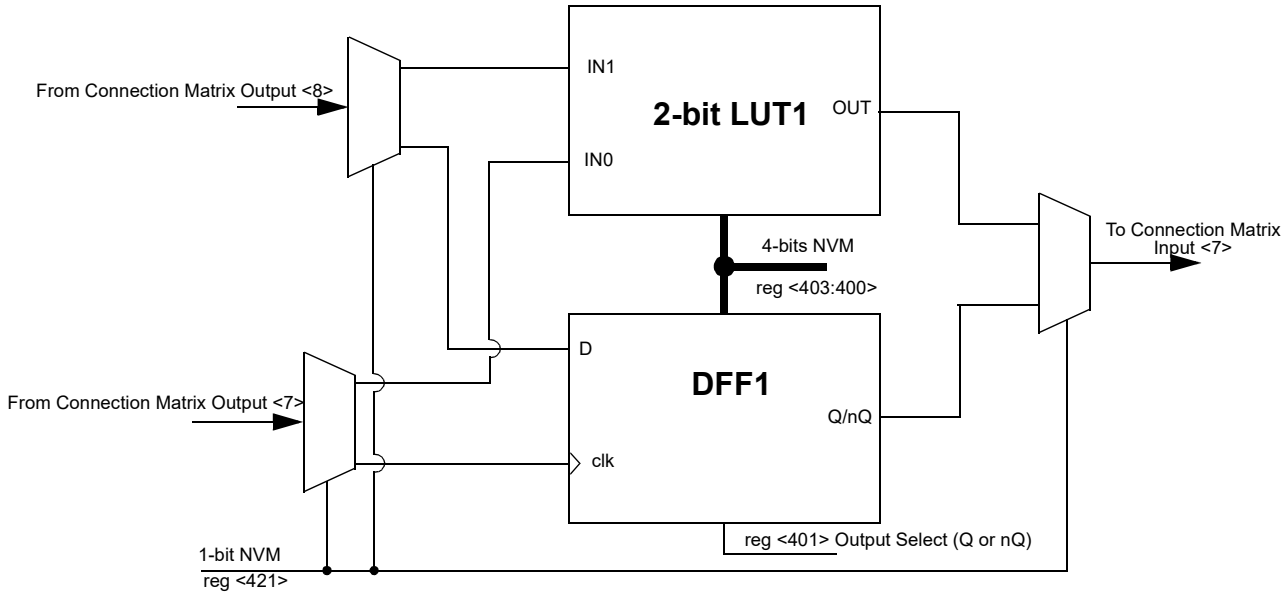


Figure 12. 2-bit LUT1 or DFF1

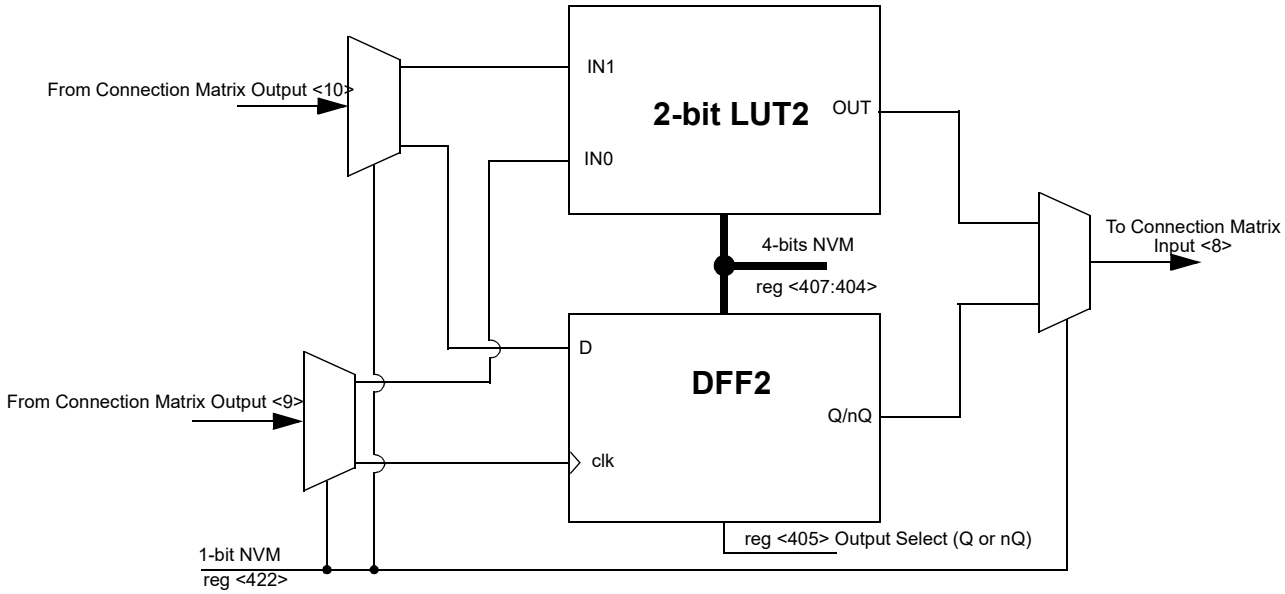


Figure 13. 2-bit LUT2 or DFF2

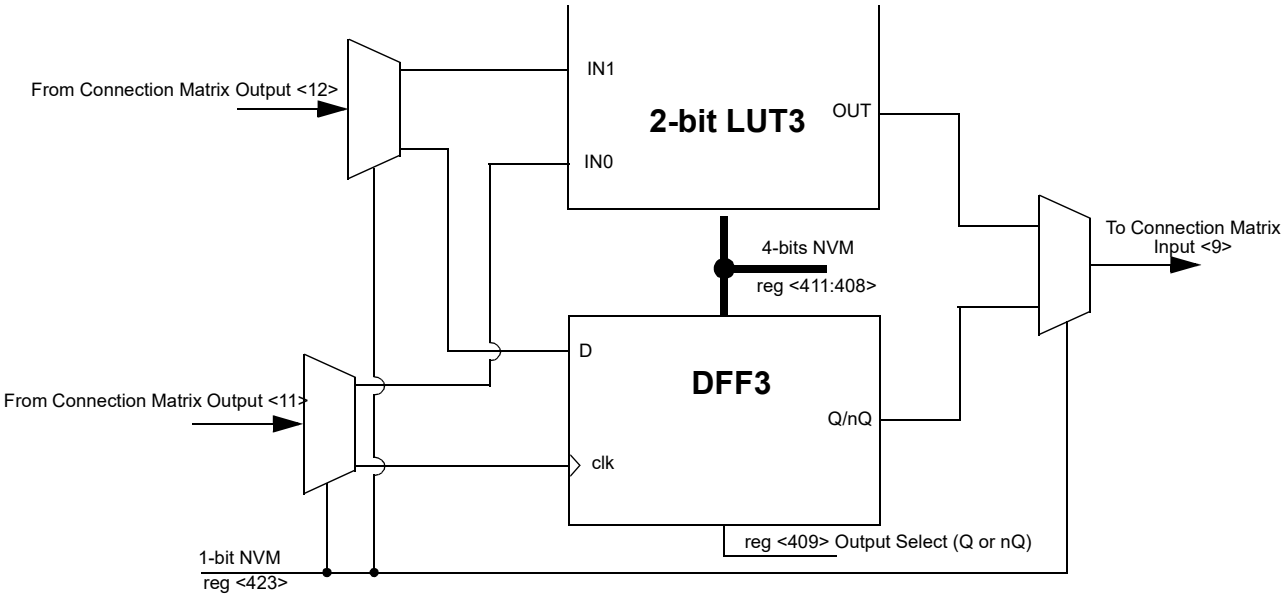


Figure 14. 2-bit LUT3 or DFF3

10.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Table 24. 2-bit LUT0 Truth Table.

IN1	IN0	OUT
0	0	reg <396>
0	1	reg <397>
1	0	reg <398>
1	1	reg <399>

Table 25. 2-bit LUT1 Truth Table.

IN1	IN0	OUT
0	0	reg <400>
0	1	reg <401>
1	0	reg <402>
1	1	reg <403>

Table 26. 2-bit LUT3 Truth Table.

IN1	IN0	OUT
0	0	reg <404>
0	1	reg <405>
1	0	reg <406>
1	1	reg <407>

Table 27. 2-bit LUT4 Truth Table.

IN1	IN0	OUT
0	0	reg <408>
0	1	reg <409>
1	0	reg <410>
1	1	reg <411>

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg <399:396>

2-Bit LUT1 is defined by reg <403:400>

2-Bit LUT2 is defined by reg <407:404>

2-Bit LUT3 is defined by reg <411:408>

10.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 28. DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF0 or Latch select	reg <396>	0: DFF function 1: Latch function
DFF0 output select	reg <397>	0: Q output 1: nQ output
DFF0 initial polarity select	reg <398>	0: Low 1: High
LUT2_0 data	reg <399:396>	LUT2_0 data
LUT2_0 or DFF0 select	reg <420>	0: LUT2_0 1: DFF0

Table 29. DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF1 or Latch select	reg <400>	0: DFF function 1: Latch function
DFF1 output select	reg <401>	0: Q output 1: nQ output
DFF1 initial polarity select	reg <402>	0: Low 1: High
LUT2_1 data	reg <403:400>	LUT2_1 data
LUT2_1 or DFF1 select	reg <421>	0: LUT2_1 1: DFF1

Table 30. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF2 or Latch select	reg <404>	0: DFF function 1: Latch function
DFF2 output select	reg <405>	0: Q output 1: nQ output
DFF2 initial polarity select	reg <406>	0: Low 1: High
LUT2_2 data	reg <407:404>	LUT2_2 data
LUT2_2 or DFF2 select	reg <422>	0: LUT2_2 1: DFF2

Table 31. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF3 or Latch select	reg <408>	0: DFF function 1: Latch function
DFF3 output select	reg <409>	0: Q output 1: nQ output
DFF3 initial polarity select	reg <410>	0: Low 1: High
LUT2_3 data	reg <411:408>	LUT2_3 data
LUT2_3 or DFF3 select	reg <423>	0: LUT2_3 1: DFF3

10.2 3-Bit LUT or D Flip Flop with Set/Reset Macrocells

There are four macrocells that can serve as either 3-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (d) and clock (clk) and Set/Reset (nRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix..

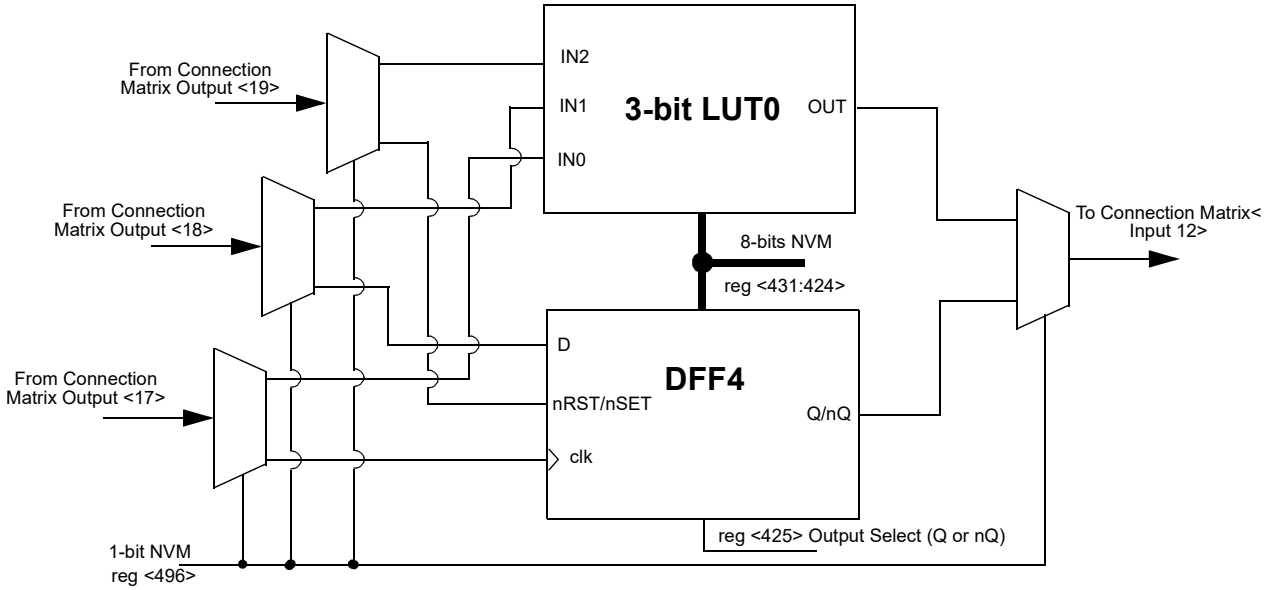


Figure 15. 3-bit LUT0 or DFF4

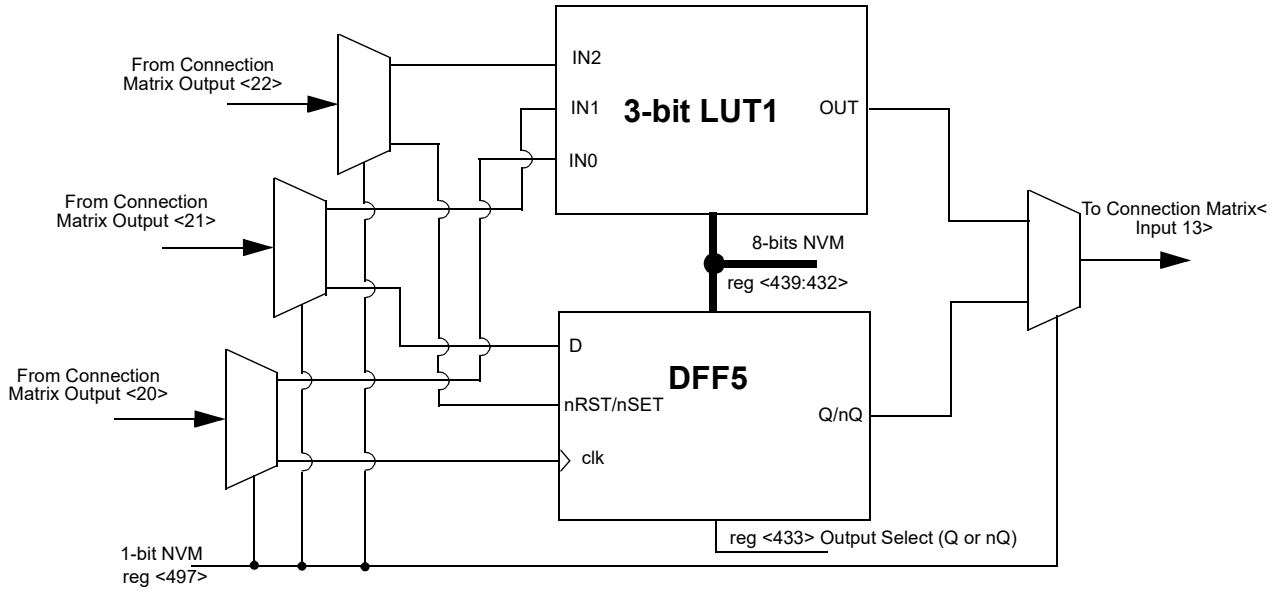


Figure 16. 3-bit LUT1 or DFF5

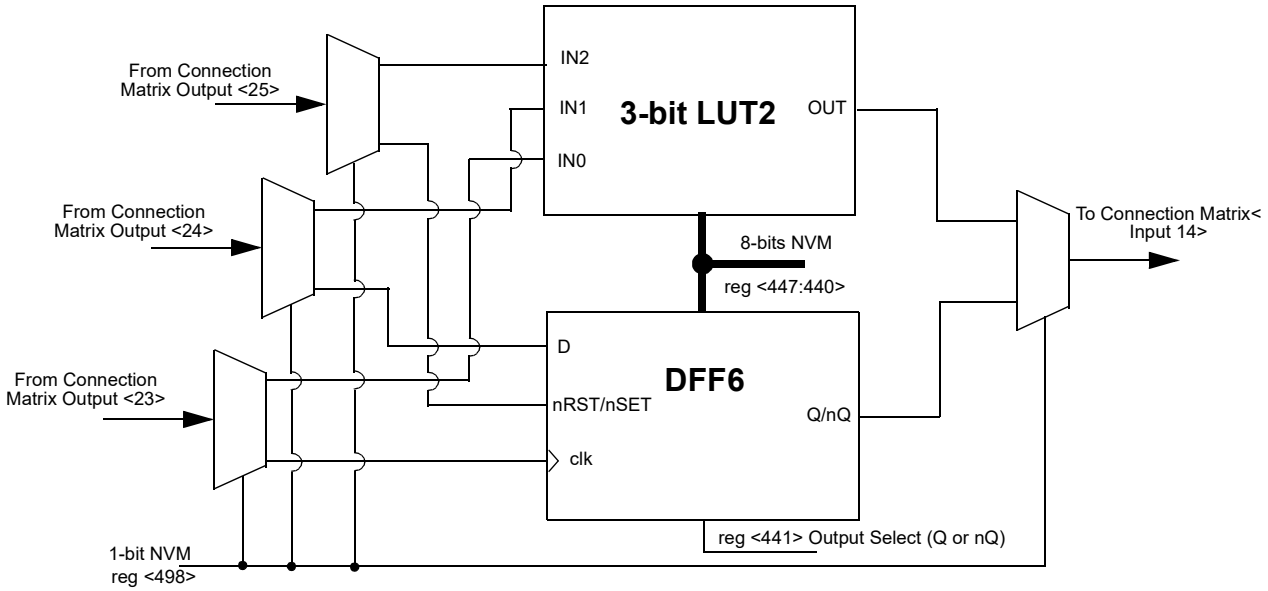


Figure 17. 3-bit LUT2 or DFF6

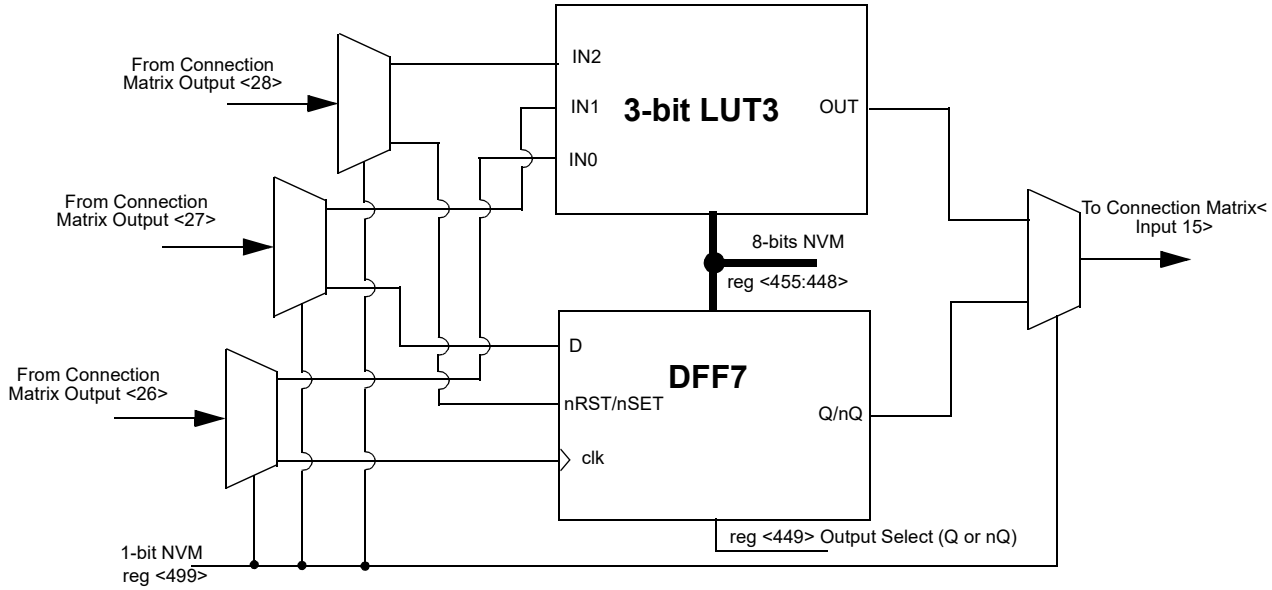


Figure 18. 3-bit LUT3 or DFF7

10.2.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

Table 32. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <424>
0	0	1	reg <425>
0	1	0	reg <426>
0	1	1	reg <427>
1	0	0	reg <428>
1	0	1	reg <429>
1	1	0	reg <430>
1	1	1	reg <431>

Table 33. 3-bit LUT1 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <432>
0	0	1	reg <433>
0	1	0	reg <434>
0	1	1	reg <435>
1	0	0	reg <436>
1	0	1	reg <437>
1	1	0	reg <438>
1	1	1	reg <439>

Table 34. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <440>
0	0	1	reg <441>
0	1	0	reg <442>
0	1	1	reg <443>
1	0	0	reg <444>
1	0	1	reg <445>
1	1	0	reg <446>
1	1	1	reg <447>

Table 35. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <448>
0	0	1	reg <449>
0	1	0	reg <450>
0	1	1	reg <451>
1	0	0	reg <452>
1	0	1	reg <453>
1	1	0	reg <454>
1	1	1	reg <455>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by reg <431:424>

3-Bit LUT1 is defined by reg <439:432>

3-Bit LUT2 is defined by reg <447:440>

3-Bit LUT3 is defined by reg <455:448>

10.2.2 3-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 36. DFF4 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF4 or Latch select	reg <424>	0: DFF function 1: Latch function
DFF4 output select	reg <425>	0: Q output 1: nQ output
DFF4 rstb/setb Select	reg <426>	1: setb from matrix out 0: resetb from matrix out
DFF4 initial polarity select	reg <427>	0: Low 1: High
LUT3_0 data	reg <431:424>	LUT3_0 data
LUT3_0 or DFF4 select	reg <496>	0: LUT3_0 1: DFF4

Table 37. DFF5 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF5 or Latch Select	reg <432>	0: DFF function 1: Latch function
DFF5 Output Select	reg <433>	0: Q output 1: nQ output
DFF5 rstb/setb Select	reg <434>	1: setb from matrix out 0: resetb from matrix out
DFF5 initial polarity select	reg <435>	0: Low 1: High
LUT3_1 data	reg <439:432>	LUT3_1 data
LUT3_1 or DFF5 select	reg <497>	0: LUT3_1 1: DFF5

Table 38. DFF6 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF6 or Latch select	reg <440>	0: DFF function 1: Latch function
DFF6 output select	reg <441>	0: Q output 1: nQ output
DFF6 rstb/setb Select	reg <442>	1: setb from matrix out 0: resetb from matrix out
DFF6 initial polarity select	reg <443>	0: Low 1: High
LUT3_2 data	reg <447:440>	LUT3_2 data
LUT3_2 or DFF6 select	reg <498>	0: LUT3_2 1: DFF6

Table 39. DFF7 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF7 or Latch Select	reg <448>	0: DFF function 1: Latch function
DFF7 Output Select	reg <449>	0: Q output 1: nQ output
DFF7 rstb/setb Select	reg <450>	1: setb from matrix out 0: resetb from matrix out
DFF7 initial polarity select	reg <451>	0: Low 1: High
LUT3_3 data	reg <455:448>	LUT3_3 data
LUT3_3 or DFF7 select	reg <499>	0: LUT3_3 1: DFF7

10.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as an 8-stage pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (nRESET). The pipe delay macrocell is built from 8 D Flip-Flop logic cells that provide three register shifted options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (1 PIPE OUT) is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 to 8 stages of delay.

The overall time of the delay is based on the clock used in the SLG46121 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46121). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

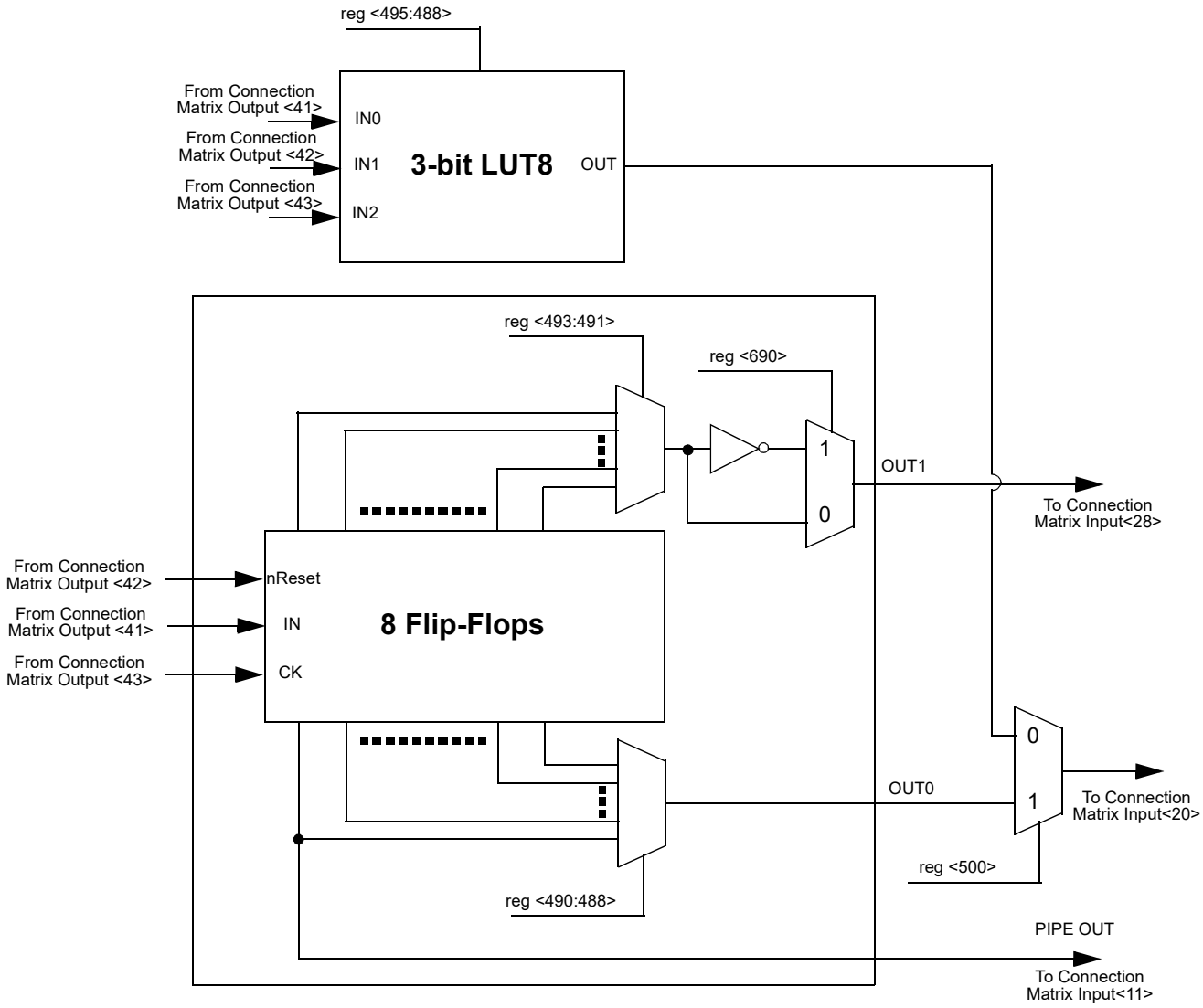


Figure 19. 3-bit LUT4 or Pipe Delay

10.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 40. 3-bit LUT8 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <488>
0	0	1	reg <489>
0	1	0	reg <490>
0	1	1	reg <491>
1	0	0	reg <492>
1	0	1	reg <493>
1	1	0	reg <494>
1	1	1	reg <495>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT8 is defined by reg <495:488>

10.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 41. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 select	reg <490:488>	data (pipe number)
OUT1 select	reg <493:491>	data (pipe number)
Unused if Pipe Delay selected	reg <495:494>	Unused
LUT3_8 or pipe delay output select	reg <500>	0: LUT3_8 1: pipe delay

10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells

There are two macrocells that can serve as either a 4-bit LUT or as a Counter / Delay. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delay function, two of the four input signals from the connection matrix go to the external clock (ext_clk) and reset (DLY_n/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

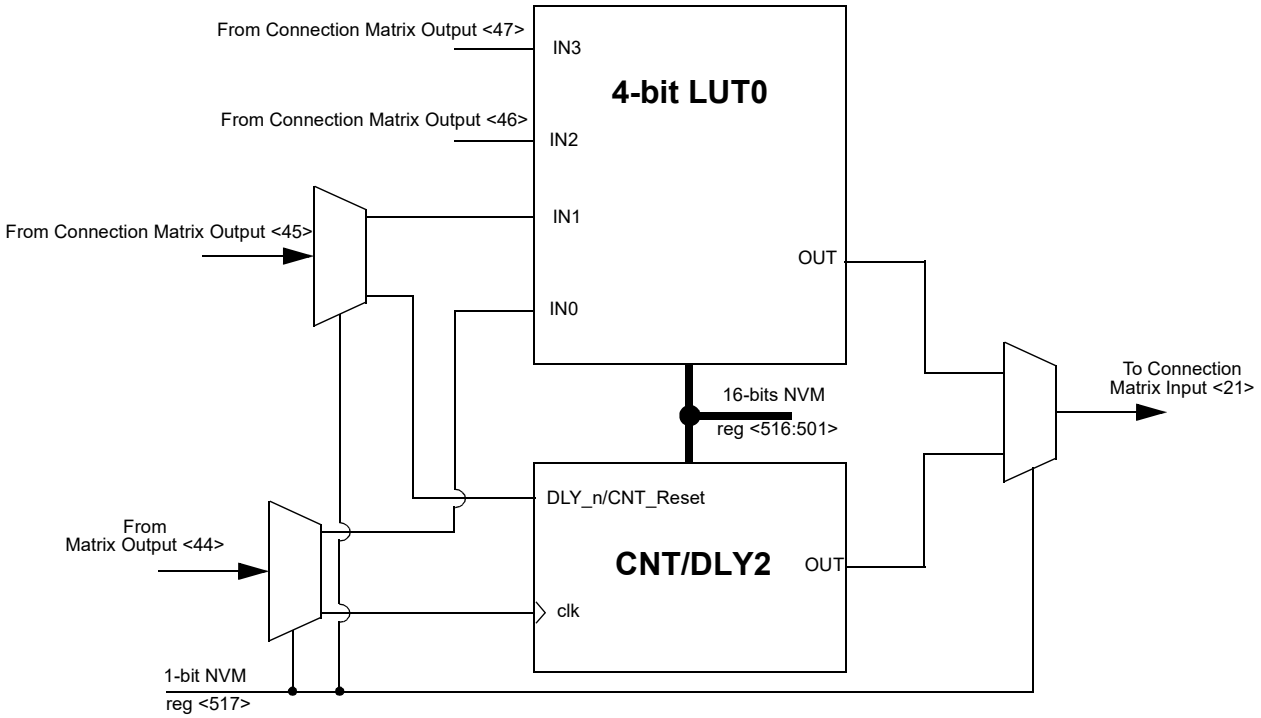


Figure 20. 4-bit LUT0 or CNT/DLY2

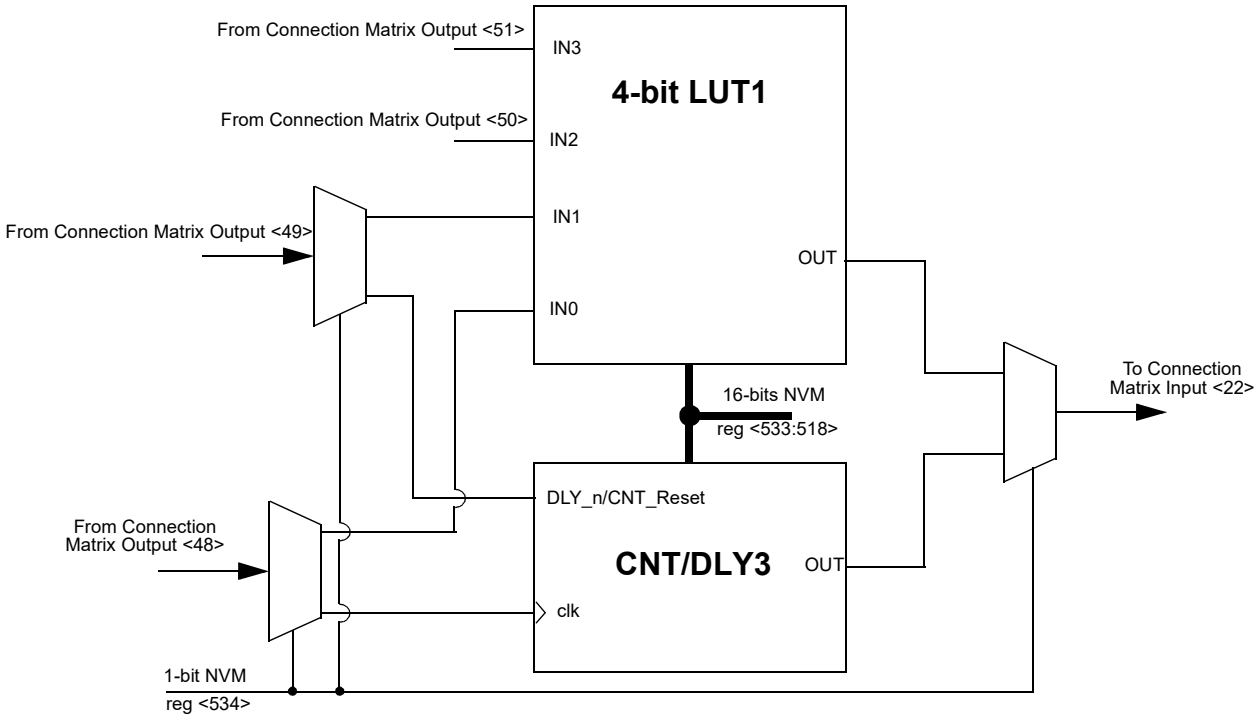


Figure 21. 4-bit LUT1 or CNT/DLY3

10.4.1 4-Bit LUT or 8-Bit Counter / Delay Macrocell Used as 4-Bit LUTs

Table 42. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <501>
0	0	0	1	reg <502>
0	0	1	0	reg <503>
0	0	1	1	reg <504>
0	1	0	0	reg <505>
0	1	0	1	reg <506>
0	1	1	0	reg <507>
0	1	1	1	reg <508>
1	0	0	0	reg <509>
1	0	0	1	reg <510>
1	0	1	0	reg <511>
1	0	1	1	reg <512>
1	1	0	0	reg <513>
1	1	0	1	reg <514>
1	1	1	0	reg <515>
1	1	1	1	reg <516>

Table 43. 4-bit LUT1 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <518>
0	0	0	1	reg <519>
0	0	1	0	reg <520>
0	0	1	1	reg <521>
0	1	0	0	reg <522>
0	1	0	1	reg <523>
0	1	1	0	reg <524>
0	1	1	1	reg <525>
1	0	0	0	reg <526>
1	0	0	1	reg <527>
1	0	1	0	reg <528>
1	0	1	1	reg <529>
1	1	0	0	reg <530>
1	1	0	1	reg <531>
1	1	1	0	reg <532>
1	1	1	1	reg <533>

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by reg <516:501>

4-Bit LUT1 is defined by reg <533:518>

Table 44. 4-bit LUT Standard Digital Functions.

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

10.4.2 4-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 8-Bit Counter / Delay Register Settings

Table 45. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay2 Mode Selection	reg <501>	0: Delay Mode 1: Counter Mode
Counter/delay2 Clock Source Select	reg <504:502>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter1 Overflow
Counter/delay2 Control Data	reg <512:505>	1 – 256 (delay time = (counter control data +2) /freq)
Delay2 Mode Select or asynchronous counter reset	reg <514:513>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset Delay) 10: on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
LUT4_0 or Counter2 select	reg <517>	0: LUT4_0 1: Counter2

Table 46. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay3 Mode Selection	reg <518>	0: Delay Mode 1: Counter Mode
Counter/delay3 Clock Source Select	reg <521:519>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter2 Overflow
Counter/delay3 Control Data	reg <529:522>	1 – 256 (delay time = (counter control data +2) /freq)
Delay3 Mode Select or asynchronous counter reset	reg <531:530>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset Delay) 10: on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edg es
LUT4_1 or Counter3 select	reg <534>	0: LUT4_1 1: Counter3

10.5 Programmable Delay / Edge Detector

The SLG46121 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

Note: *The input signal must be longer than the delay, otherwise it will be filtered out.*

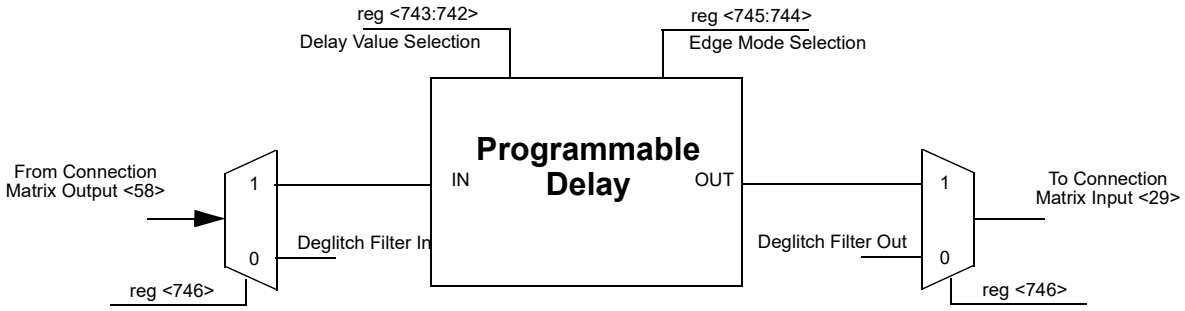


Figure 22. Programmable Delay

10.6 Programmable Delay Timing Diagram - Edge Detector Output

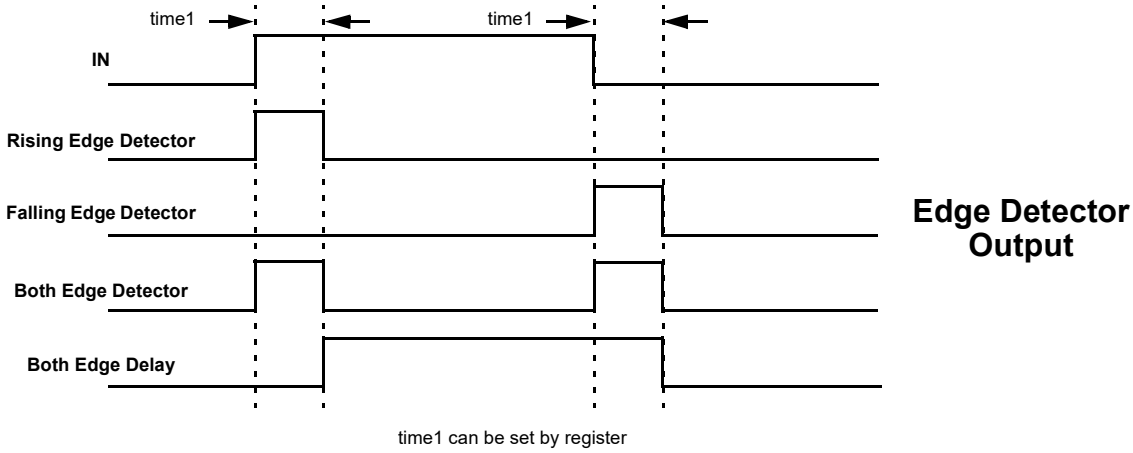


Figure 23. Edge Detector Output

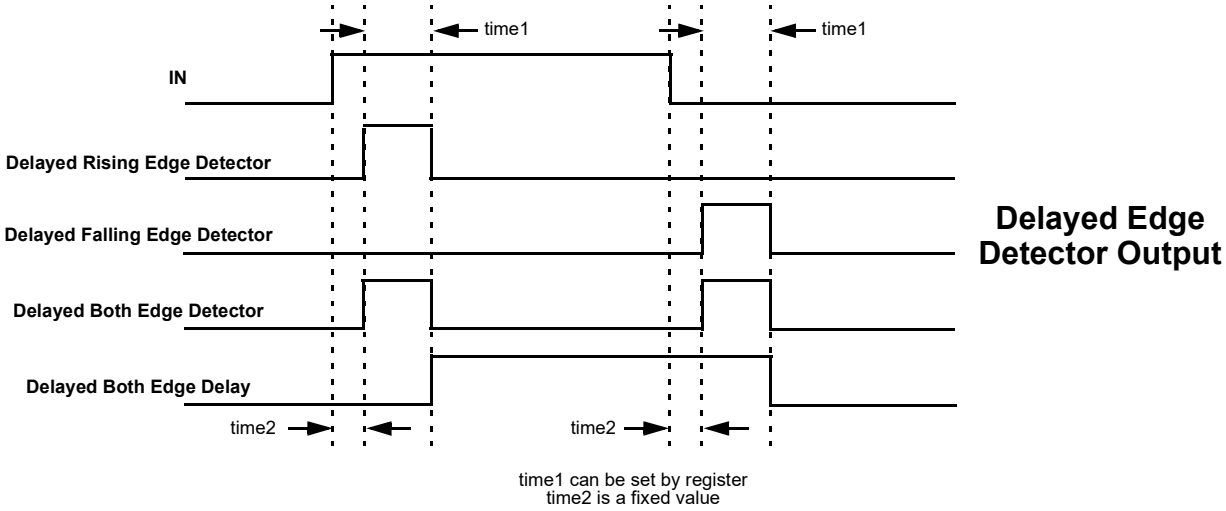


Figure 24. Delayed Edge Detector Output

Note: For delays and widths refer to *Table 4*.

10.6.1 Programmable Delay Register Settings

Table 47. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Programmable delay or filter output select	reg <746>	0: programmable delay output 1: filter output
Select the edge mode of programmable delay & edge detector	reg <745:744>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	reg <743:742>	00: 163 ns 01: 305 ns 10: 446 ns 11: 588 ns

10.7 Deglitch Filter

The SLG46121 has an additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one deglitch filter.

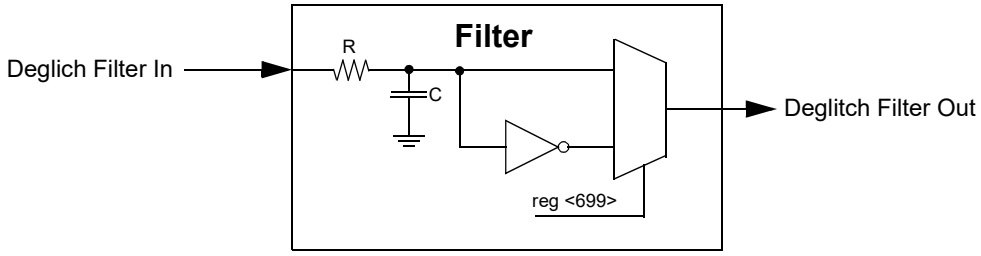


Figure 25. Deglitch Filter

11.0 Analog Comparators (ACMP)

There are two Analog Comparator (ACMP) macrocells in the SLG46120. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0_pdb and ACMP1_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by way of the external sources.

Each of the ACMP cells has a selection for the bandwidth of the input signal, which can be used to save power when low bandwidth signals are input into the analog comparator. And if input frequency > 200 kHz, the output will retain its previous value. Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV.

During powerup, the ACMP output will remain low, and then become valid 110 µs (max) after POR signal goes high, see *Figure 26*.

Note: Applies to first time power ON.
Note: Regulator and Charge Pump set to automatic ON/OFF.

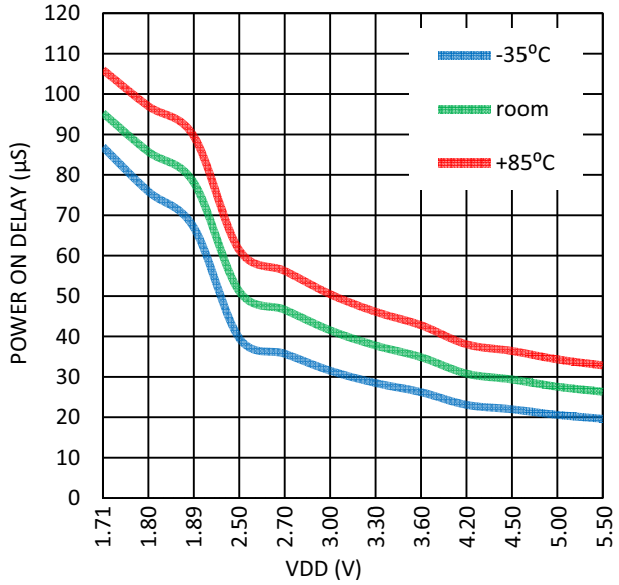


Figure 26. Maximum Power On Delay vs. VDD.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 KΩ (typ.) resistors, see *Table 48*. For gain divider accuracy refer to *Table 49*. IN- voltage range: 0 - 1.2 V. Can use Vref selection VDD/4 and VDD/3 to maintain this input range.

Table 48. Gain Divider Input Resistance (typ).

Gain	1X	0.5X	0.33X	0.25X
Input Resistance	100M	1M	0.75M	1M

Table 49. Gain Divider Accuracy.

Gain	0.5X	0.33X	0.25X
Accuracy	±0.6%	±0.9%	±0.28%

Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by the external reference/source. Internal Vref accuracy is optimized near 1000 mV selection.

Note: Power supply control options have influence on the ACMP operation.

Note: Any ACMP powered on enables the BandGap internal circuit as well. An analog voltage will appear on Vref (even when the Force BandGap option is set as Disabled).

Analog comparators have the following configurable options:

- Hysteresis: Input signal hysteresis options are Disable, 25 mV, 50 mV, 200 mV.
- Low Bandwidth: Enable, Disable;
- IN+ Gain: 1X, 0.5X, 0.33X, 0.25X;
- IN+ source:
  - ACMP0 IN+ options are PIN 3, VDD;
  - ACMP1 IN+ options are PIN 6, ACMP0 IN+;
- IN- source:
  - ACMP0 IN- options are 24 internal reference sources (50 mV – 1200 mV) and VDD/3, VDD/4, PIN 4;
  - PWR UP=0 – ACMP is powered down; PWR UP=1 – ACMP is powered up.

All ACMPs can have a common negative input. This can be achieved by configuring ACMP0 PIN 4 analog I/O connection.

11.1 ACMP0 Block Diagram

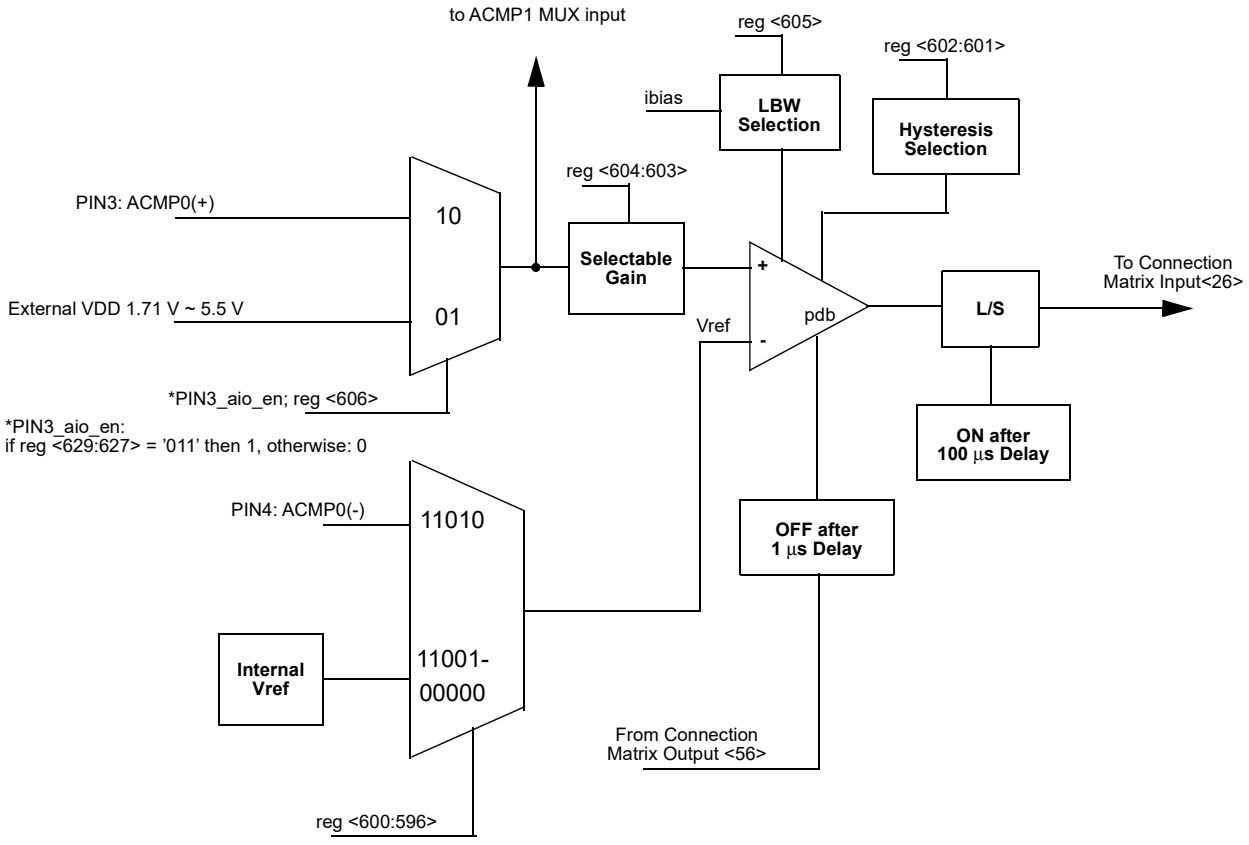


Figure 27. ACMP0 Block Diagram

11.2 ACMP0 Register Settings

Table 50. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 In Voltage Select	reg <600:596>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF (PIN4)
ACMP0 Hysteresis Enable	reg <602:601>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP0 Positive Input Divider	reg <604:603>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg <605>	0: Off 1: On
ACMP0 positive input source select PIN3 and VDD	reg <606>	0: Pin3 1: VDD

11.3 ACMP1 Block Diagram

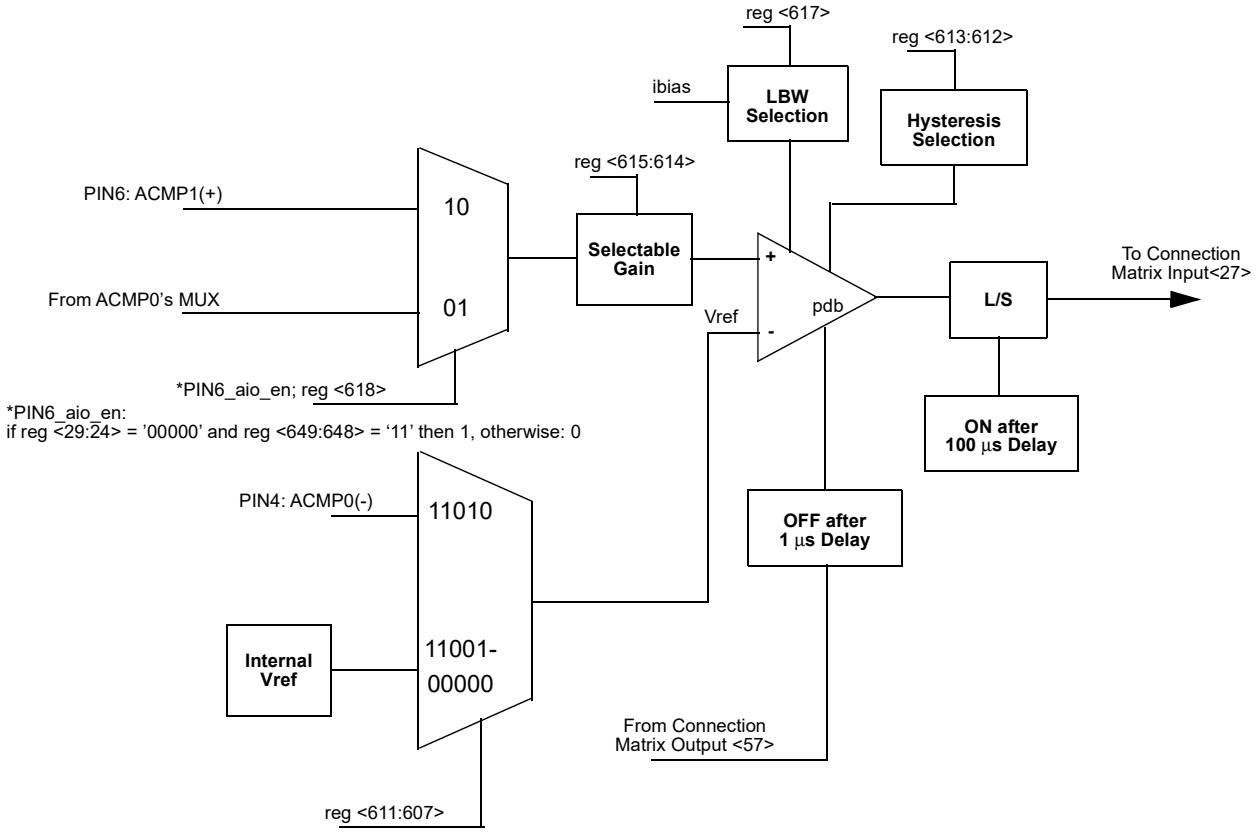


Figure 28. ACMP1 Block Diagram

11.4 ACMP1 Register Settings

Table 51. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 In Voltage Select	reg <611:607>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF (PIN4)
ACMP1 Hysteresis Enable	reg <613:612>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP1 Positive Input Divider	reg <615:614>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP1 100 µA Current Source Option	reg <616>	0: Disable 1hebrew : Enable
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg <617>	1: On 0: Off
ACMP1 positive input source select PIN3 and Pin6	reg <618>	0: Pin6 1: Pin3

11.5 Typical Performance Characteristics

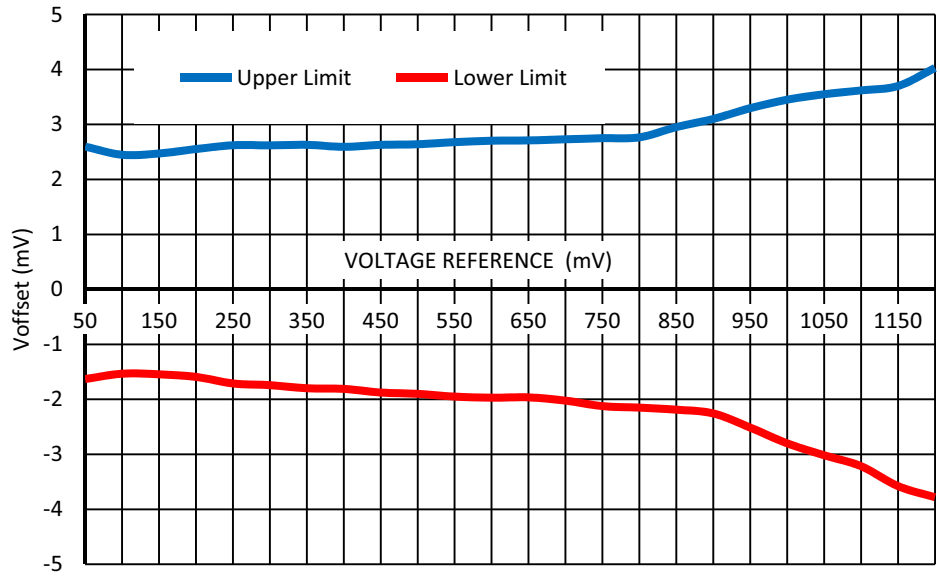


Figure 29. Typical Input Voltage Offset vs. Voltage Reference at room temperature, LBW Mode – Disable, Vhys=0 mV, VDD=(1.7 – 5.5) V.

Note: when VDD < 1.8V voltage reference should not exceed 1100 mV.

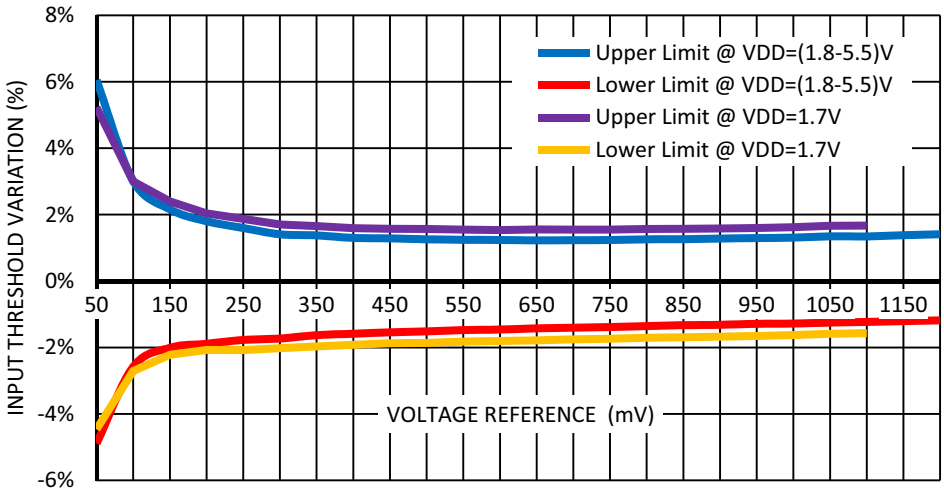


Figure 30. Typical Input Threshold Variation (including Vref variation, ACMP offset) vs. Voltage reference at room temperature, LBW Mode – Disable, Vhys=0 mV.

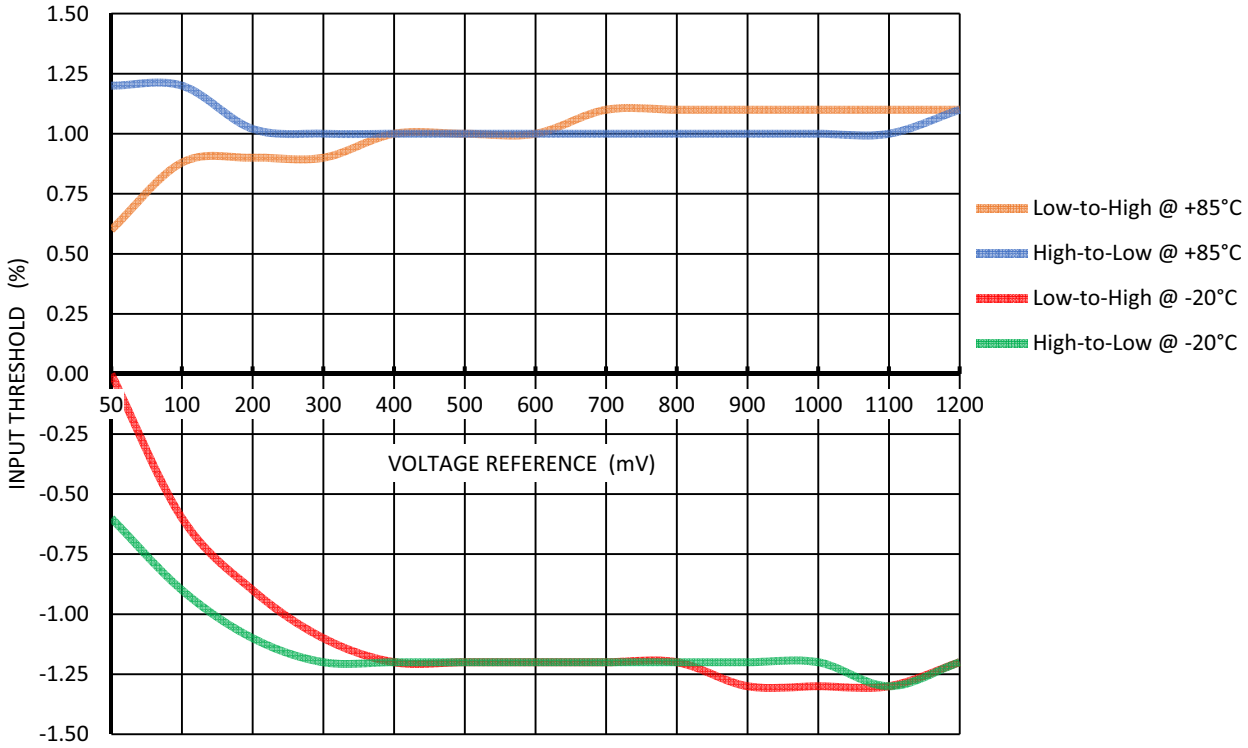


Figure 31. Input Threshold Ratio vs. Voltage Reference at VDD = (1.71 - 5.5) V, Vhys = 0, Gain = 1

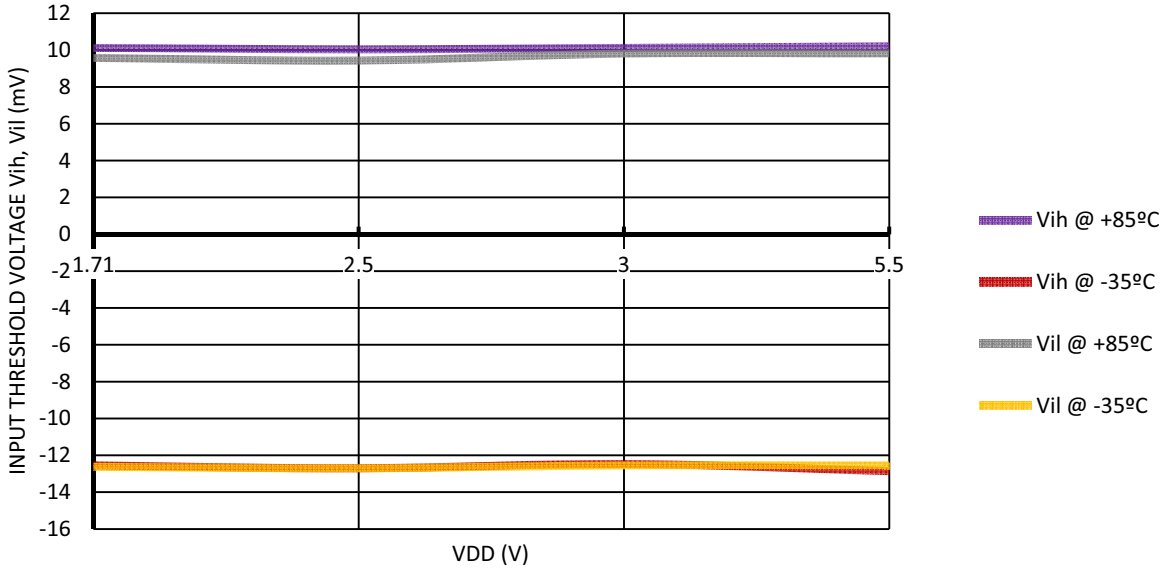


Figure 32. Input Threshold Voltage Vih, Vil vs. VDD at Vref = 1000 mV, Gain = 1

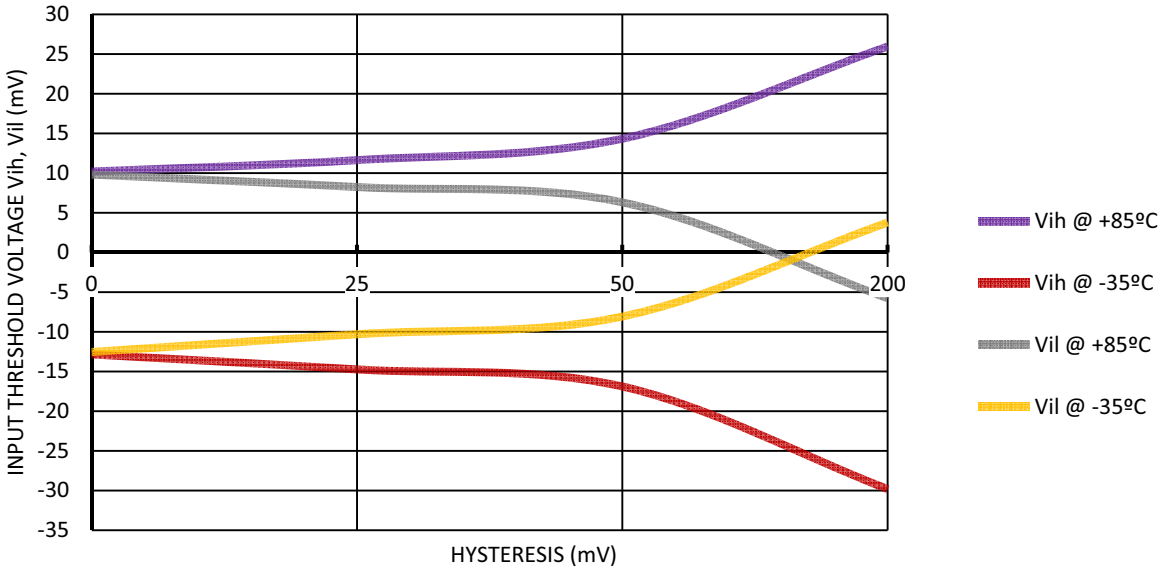


Figure 33. Input Threshold Voltage Vih, Vil vs. Hysteresis at VDD = 5.5 V, Vref = 1000 mV. Gain = 1

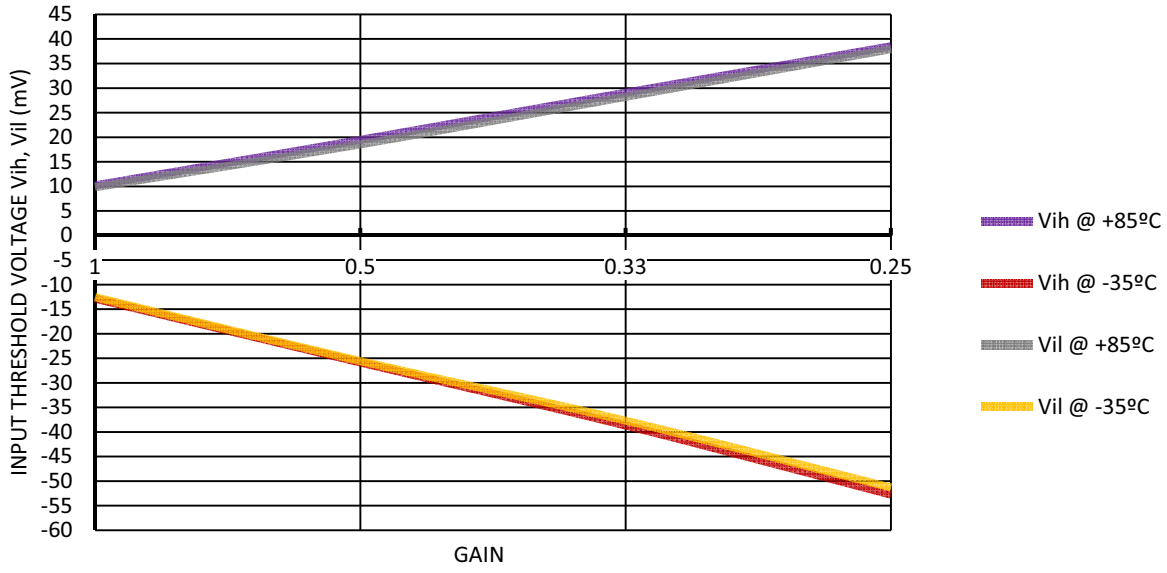


Figure 34. Input Threshold Voltage Vih, Vil vs. Gain at Hysteresis = 0, VDD = 5.5 V, Vref = 1000 mV

Table 52. Built-in Hysteresis Tolerance.

Vhys (mV)	VDD=(1.7-1.8) V						VDD=(1.89-5.5) V					
	Vref = (50-500) mV		Vref = (550-1000) mV		Vref = (1050-1200) mV		Vref = (50-500) mV		Vref = (550-1000) mV		Vref = (1050-1200) mV	
	min	max	min	max	min	max	min	max	min	max	min	max
25	18.9	26.4	17.3	26.1	13.0	24.6	18.8	26.5	17.8	26.1	15.6	25.5
50	40.3	50.4	37.9	50.1	28.9	47.7	40.3	50.5	39.5	50.1	34.5	49.5
200	180.5	208.4	172.9	210.7	153.5	217.2	180.6	207.7	180.2	210.8	166.5	211.9

11.6 Timing Characteristics

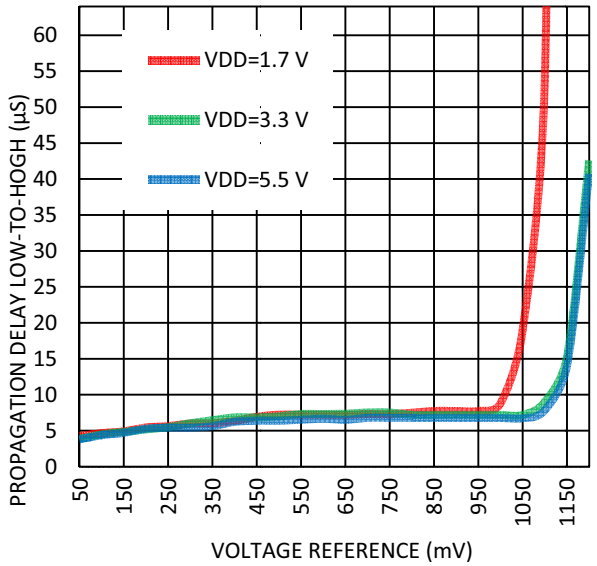


Figure 35. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, Vod = 2 mV.

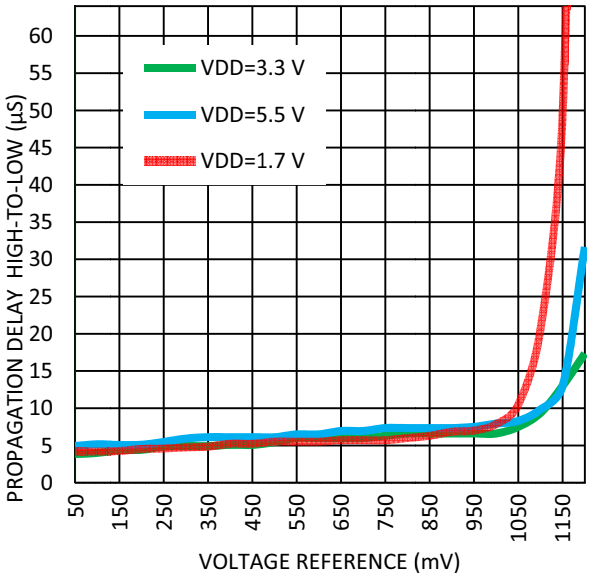


Figure 37. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, Vod = 2 mV.

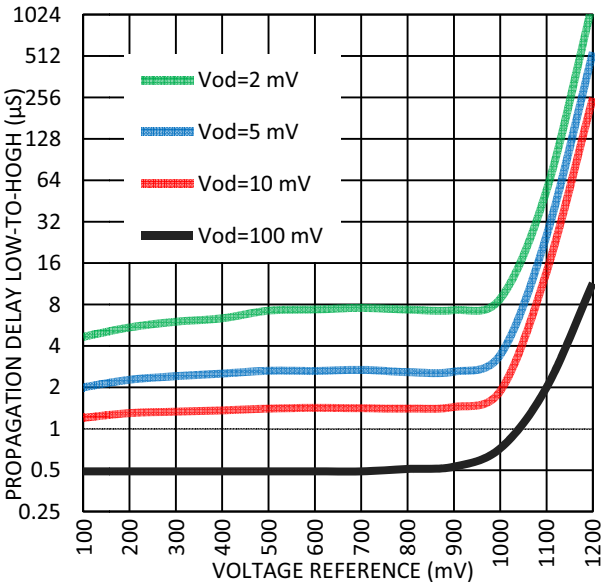


Figure 36. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, VDD=(1.71 – 1.89) V.

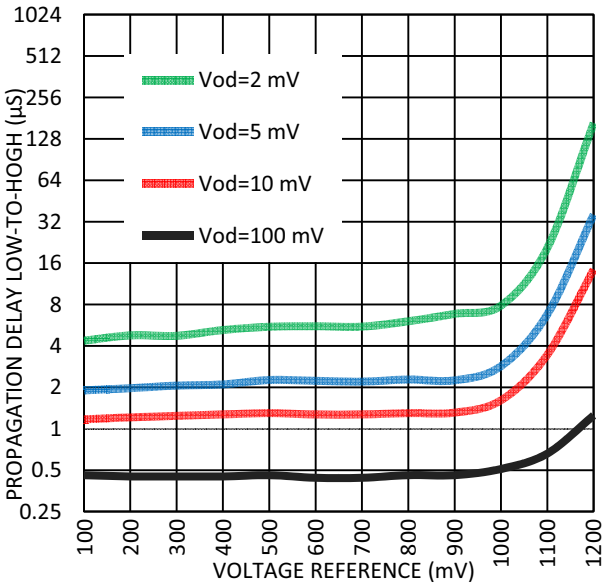


Figure 38. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, VDD=(1.71 – 1.89) V.

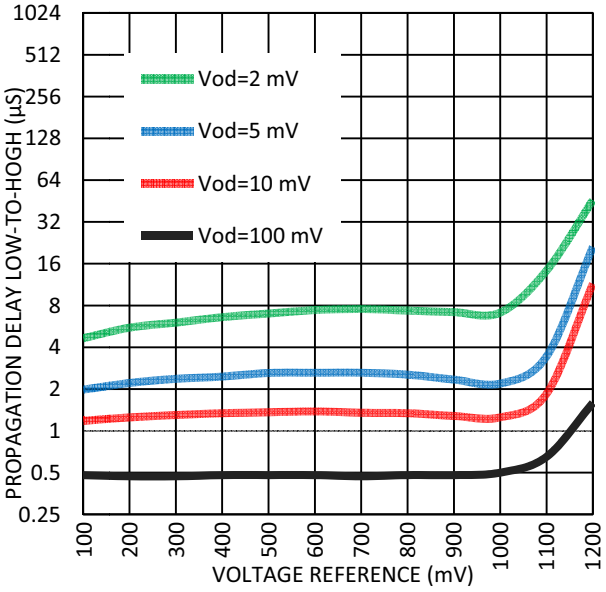


Figure 39. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, VDD = (1.89 – 3.6) V.

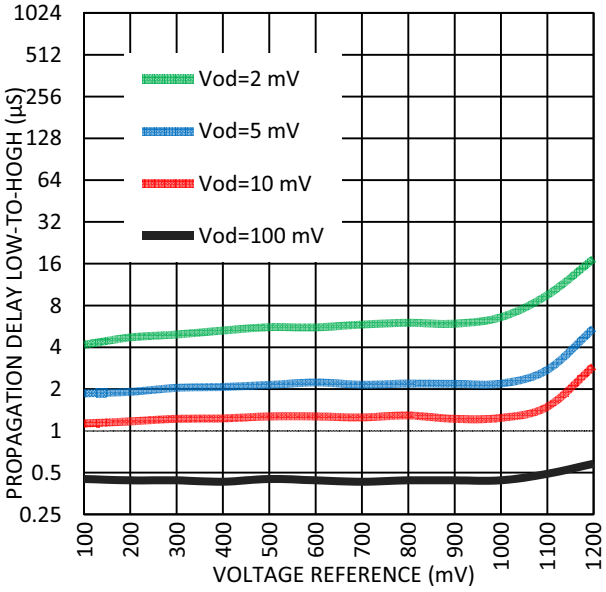


Figure 41. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, VDD = (1.89 – 3.6) V.

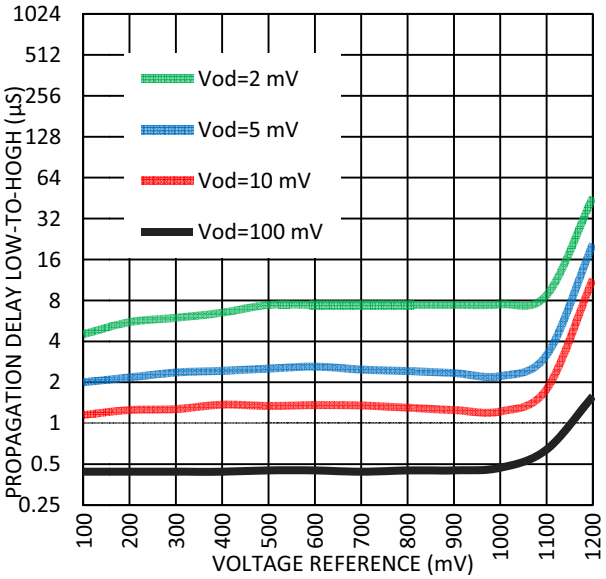


Figure 40. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, VDD = (3.6 – 5.5) V.

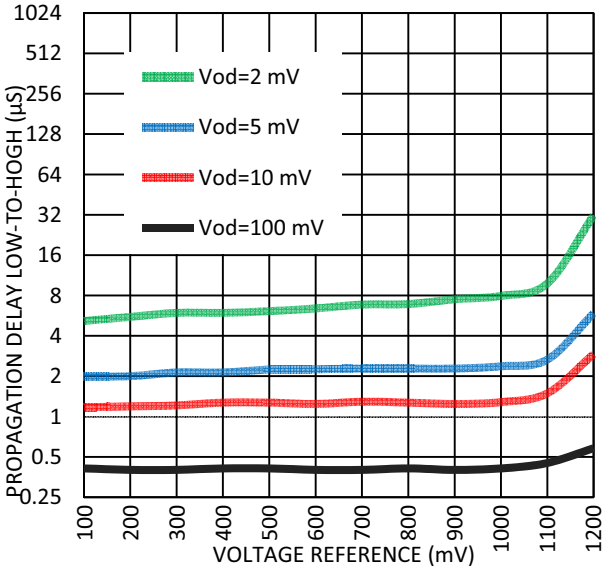


Figure 42. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, VDD = (3.6 – 5.5) V.

12.0 Counters/Delay Generators (CNT/DLY)

There are two configurable counters/delay generators in the SLG46121. CNT/DLY0 is 14-bit and CNT/DLY2 is 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

One of the counter/delay generator macrocells (CNT/DLY1) has two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source.

Note that there are also two Combination Function Macrocells that can implemented as either 4-bit LUTs or 8-bit counter / delays, For more information please see Section 10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells.

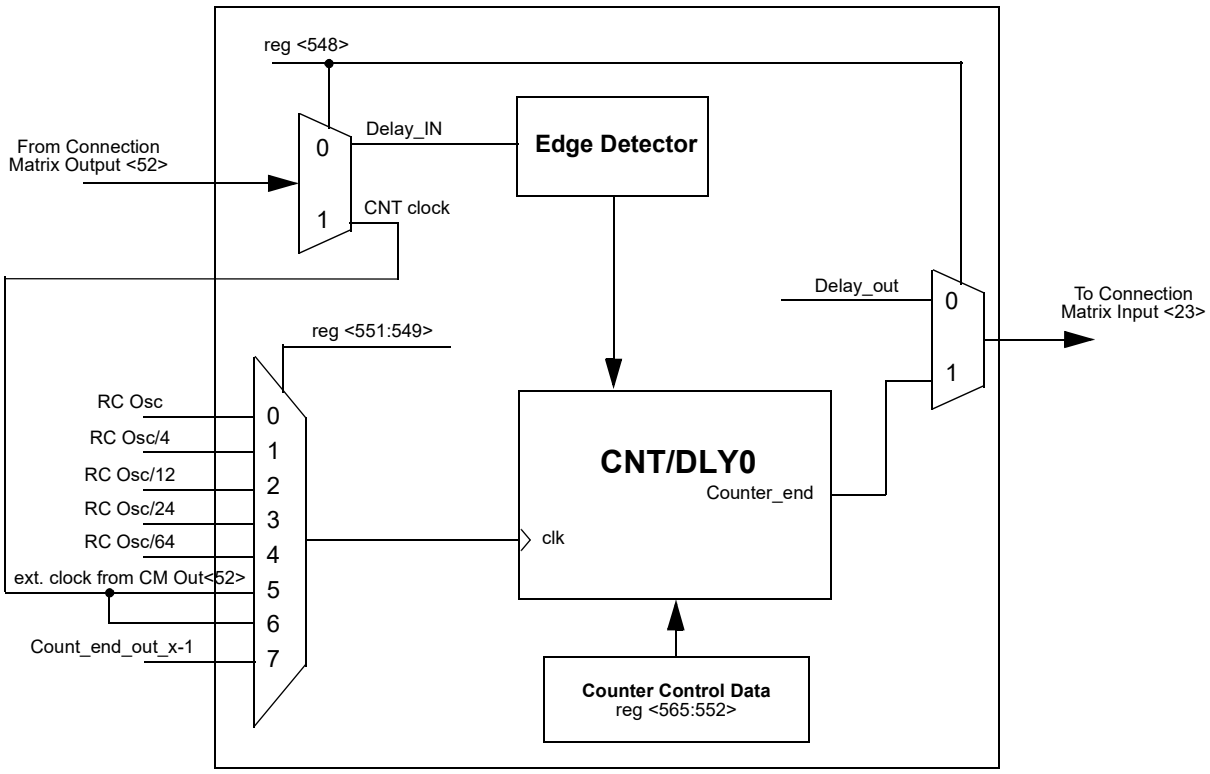


Figure 43. CNT/DLY0

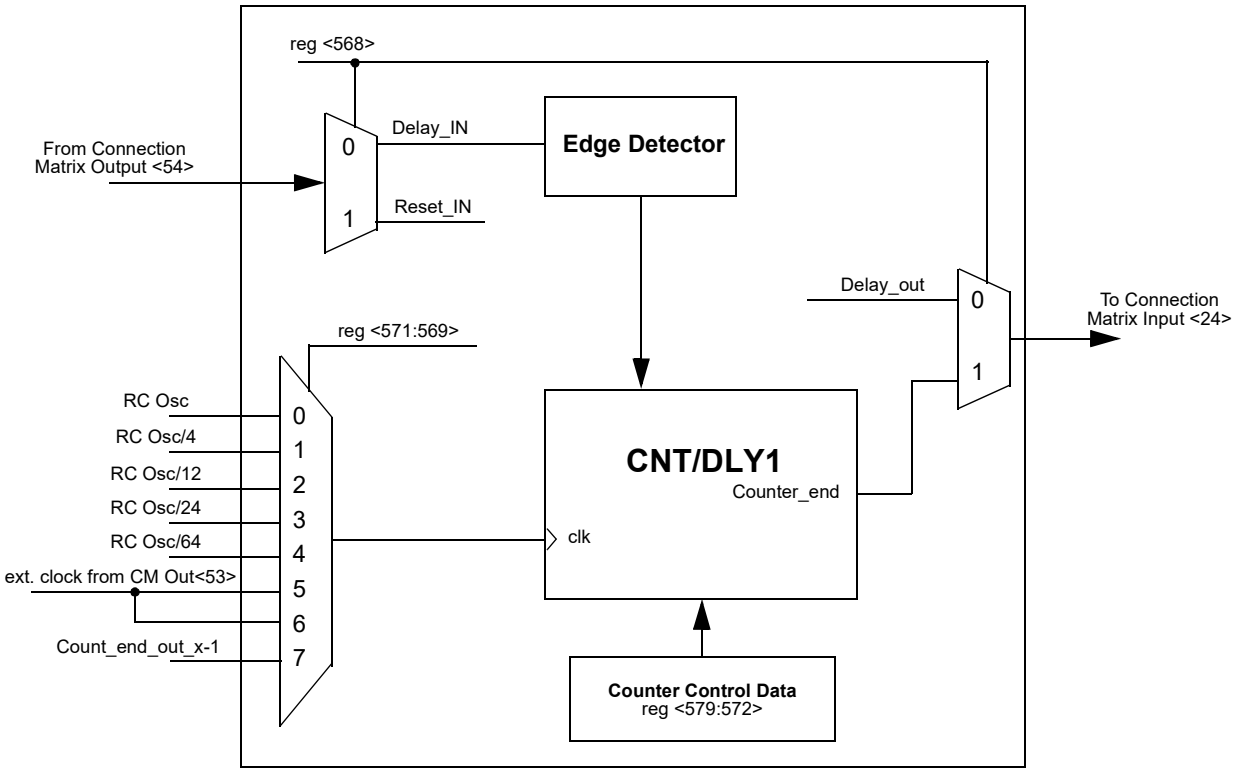


Figure 44. CNT/DLY1

12.1 CNT/DLY0 Register Settings

Table 53. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	reg <548>	0: Delay Mode 1: Counter Mode
Counter/Delay0 Clock Source Select (external clock is only for counter mode)	reg <551:549>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Reserved
Counter0 Control Data/Delay0 Time Control	reg <565:552>	1-16383: (delay time = (counter control data +2) /freq)
Delay0 Mode Select or asynchronous counter reset	reg <567:566>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

12.2 CNT/DLY1 Register Settings

Table 54. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg <568>	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source Select (external clock is only for counter mode)	reg <571:569>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter0 Overflow
Counter1 Control Data/Delay1 Time Control	reg <579:572>	1-256: (delay time = (counter control data +2) /freq)
Delay1 Mode Select or asynchronous counter reset	reg <581:580>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

13.0 Voltage Reference (VREF)

13.1 Voltage Reference Overview

The SLG46121 has a Voltage Reference Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from Pin 4. The macrocell also has the option to output reference voltages on pins 10. See table below for the available selections for each analog comparator. Also see *Figure 45* below, which shows the reference output structure.

13.2 VREF Selection Table

Table 55. VREF Selection Table.

SEL<4:0>	CMP0_VREF	CMP1_VREF
11010	ext. Vref (PIN4)	ext. Vref (PIN4)
11001	VDD / 4	VDD / 4
11000	VDD / 3	VDD / 3
10111	1.20 V	1.20 V
10110	1.15 V	1.15 V
10101	1.10 V	1.10 V
10100	1.05 V	1.05 V
10011	1.00 V	1.00 V
10010	0.95 V	0.95 V
10001	0.90 V	0.90 V
10000	0.85 V	0.85 V
01111	0.80 V	0.80 V
01110	0.75 V	0.75 V
01101	0.70 V	0.70 V
01100	0.65 V	0.65 V
01011	0.60 V	0.60 V
01010	0.55 V	0.55 V
01001	0.50 V	0.50 V
01000	0.45 V	0.45 V
00111	0.40 V	0.40 V
00110	0.35 V	0.35 V
00101	0.30 V	0.30 V
00100	0.25 V	0.25 V
00011	0.20 V	0.20 V
00010	0.15 V	0.15 V
00001	0.10 V	0.10 V
00000	0.05 V	0.05 V

VDD	Practial VREF Range	Note
3.0 V - 5.5 V	50 mV ~1.2 V	VDD > 3.6 V external Vref cannot be used

13.3 VREF Block Diagram

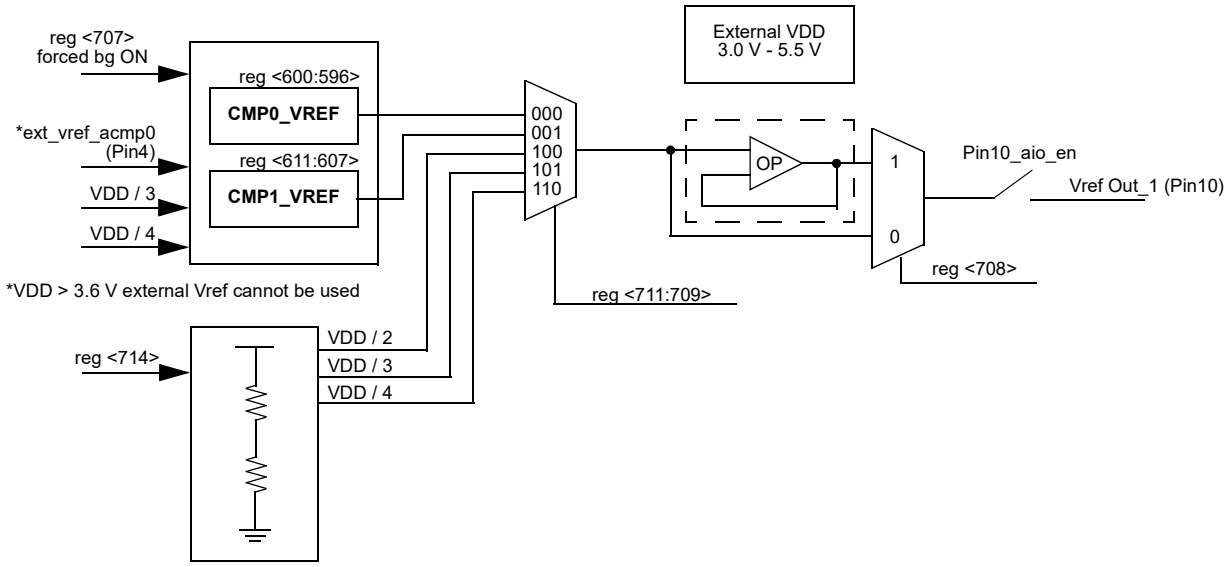


Figure 45. Voltage Reference Block Diagram

14.0 RC Oscillator (RC Osc)

14.1 RC Oscillator Overview

The SLG46121 has two internal RC oscillators, one that runs at 25 kHz and one that runs at 2 MHz. When using the chip internal RC OSC, a choice is available to “Force Power On”, meaning that the RC OSC will always run, or “Auto Power On”, meaning that the RC OSC will have an associated startup and settling time associated with it (offset). *Figure 46* and *Figure 47* show maximum power on delay vs. VDD.

Note: RC OSC power setting: "Auto Power On”.

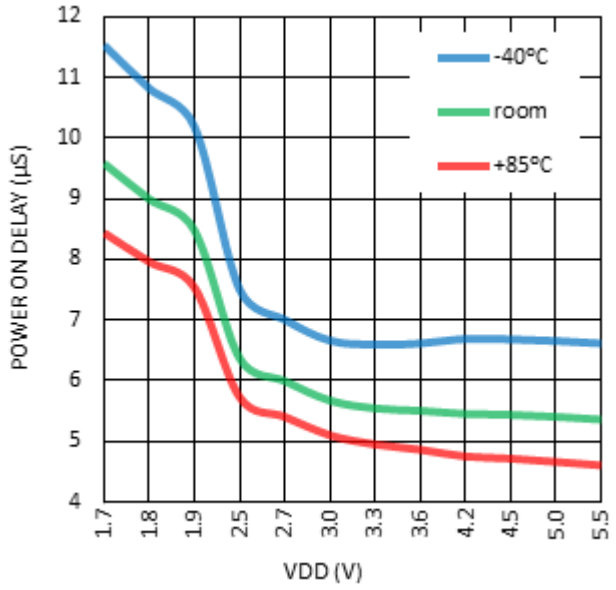


Figure 46. Maximum Power On Delay vs. VDD, RC OSC = 2 MHz.

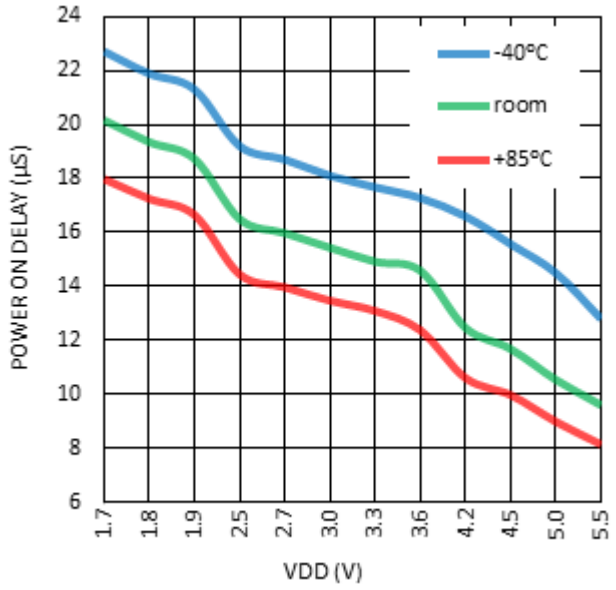


Figure 47. Maximum Power On Delay vs. VDD, RC OSC = 25 kHz.

The user can select one of these fundamental frequencies for the RC OSC Macrocell, or the fundamental frequency can also come from an external clock input (Pin 12). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The first stage divider (also known as the clock pre-divider) allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. There are two second stage divider controls (OUT0 and OUT1). Each has its own input of one frequency from the first stage divider, and outputs two different frequencies on Connection Matrix Input lines <30>, and <31>. See *Figure 48* below for details of the frequencies for each of these two Connection Matrix Inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off. The PWR DOWN signal has the highest priority.

14.2 RC OSC Block Diagram

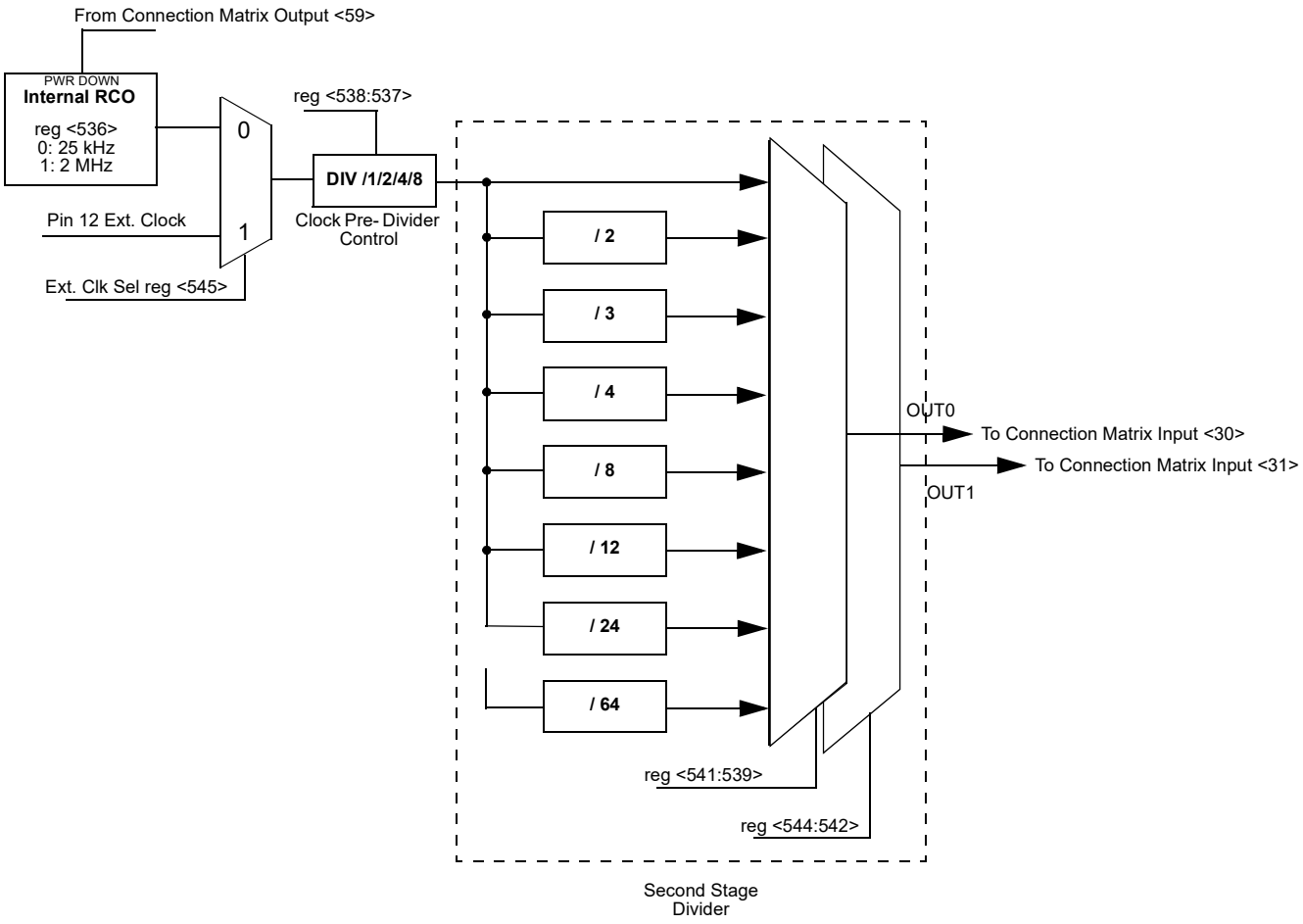


Figure 48. RC OSC Block Diagram

15.0 Additional Logic Functions

The SLG46121 has one additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one inverter which can switch the polarity of any Connection Matrix signal.

15.1 INV_0 Gate

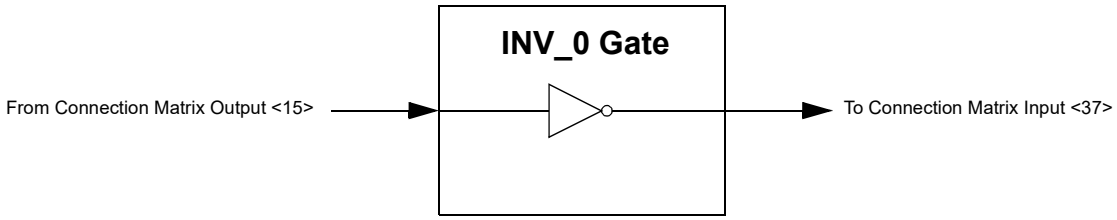


Figure 49. INV_0 Gate

16.0 Power On Reset (POR)

The SLG46121 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the VDD power is first ramping to the device, and also while the VDD is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the I/O pins. This application note is created to explain the whole process of POR operation and GreenPAK chip behavior during the time while it is powering up and powering down.

16.1 General Operation

The SLG46121 is guaranteed to be powered down and nonoperational when the VDD voltage (voltage on PIN1) is less than 0.6V, but not less than -0.6V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 1) than the VDD voltage is applied to any other PIN. For example, if VDD voltage is 0.3V, applying a voltage higher than 0.3V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1. There is a 0.6V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46121, the voltage applied on the VDD should be higher than the Power_ON threshold (see Note 2). The full operational VDD range for the SLG46121 is 1.71 V – 5.5 V (1.8 V ± 10% - 5 V ± 10%). This means that the VDD voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the VDD voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46121 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note 2. The Power_ON threshold can vary by PVT, but typically it is 1.6 V.

To power down the chip the VDD voltage should be lower than the operational and to guarantee that chip is powered down it should be less than 0.6 V.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the I/O structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can’t be bigger than the VDD, this rule also applies to the case when the chip is powered on.

Note that VDD2 has no influence on POR sequence, all internal macrocells are powered from VDD. It means, VDD2 can be switched on/off while VDD is on. If voltage on VDD2 appears after the POR sequence, pins 8, 9, 10, 12 become available when VDD2 reaches 0.6 V.

For proper power up sequence, make sure VDD2 will not exceed VDD at any point during startup.

For normal operation VDD should not be switched off while VDD2 is on, due to VDD2≤VDD,see section 5.0 Electrical Specifications.

16.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in *Figure 50*

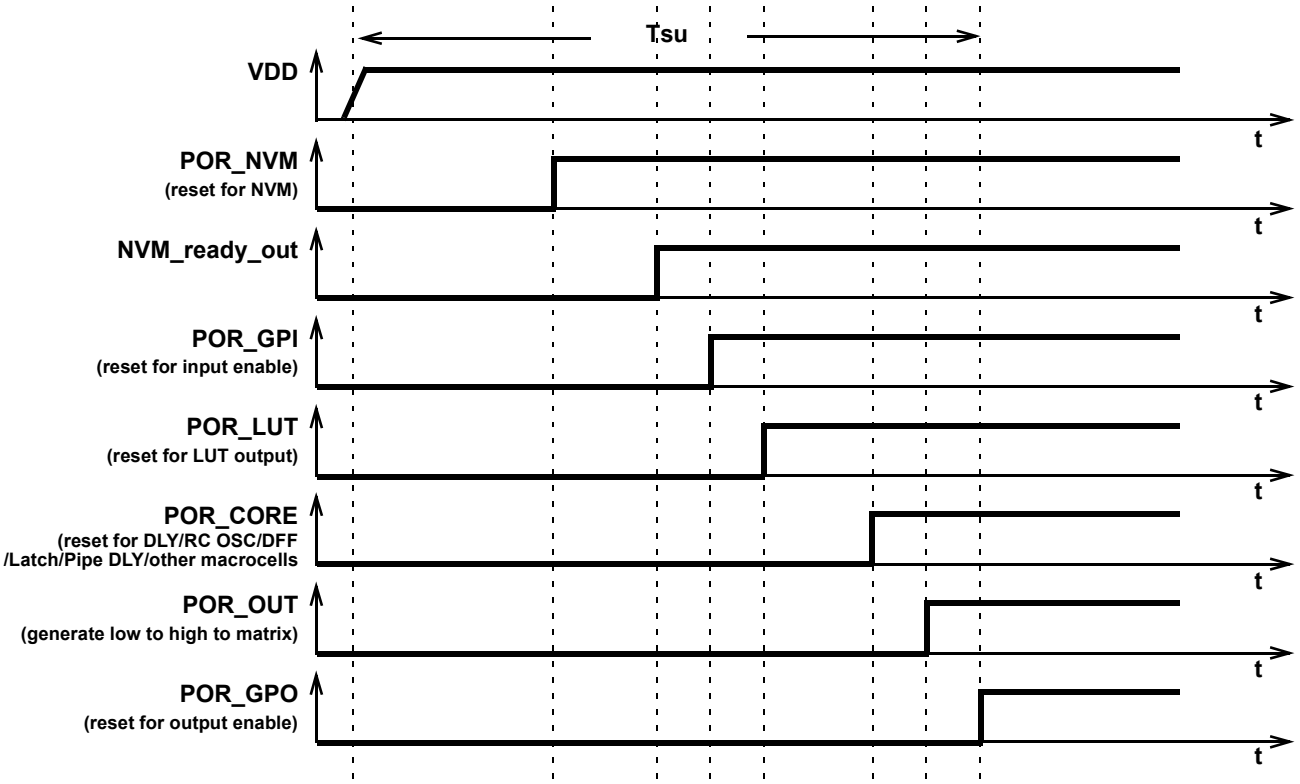


Figure 50. POR sequence

As can be seen from *Figure 50* after the VDD has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedience to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, VDD value, temperature and even will vary from chip to chip (process influence).

16.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46121 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (*Figure 51* describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

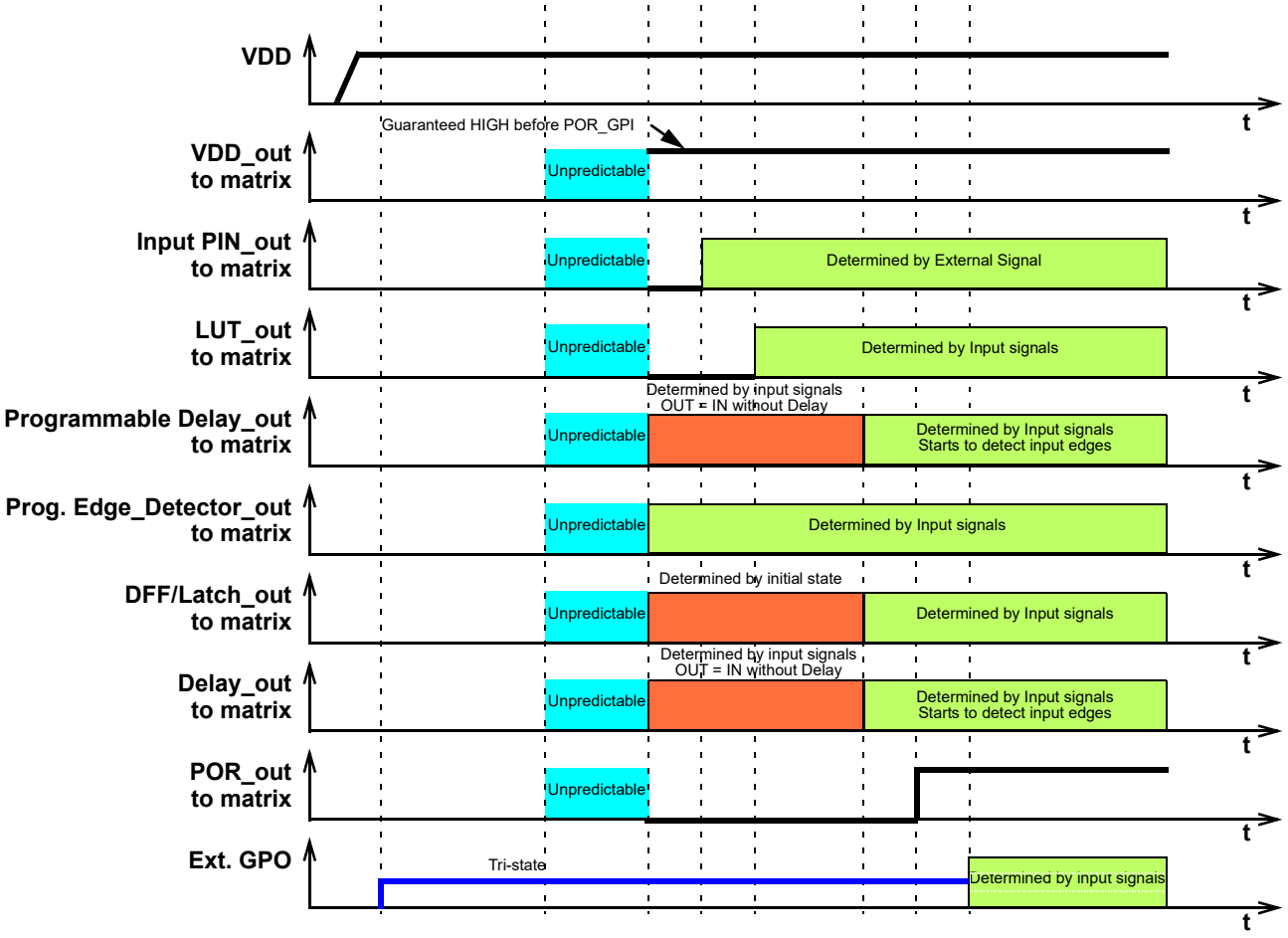


Figure 51. Internal Macrocell States during POR sequence

17.0 Appendix A - SLG46121 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg<5:0>	Matrix Out: PIN3 Digital Output Source	
reg<11:6>	Matrix Out: PIN4 Digital Output Source	
reg<17:12>	Matrix Out: PIN5 Digital Output Source	
reg<23:18>	Matrix Out: PIN6 Digital Output Source	
reg<29:24>	Matrix Out: Output Enable of PIN6	
reg<35:30>	Matrix Out: In0 of LUT2_0 or Clock Input of DFF0	
reg<41:36>	Matrix Out: In1 of LUT2_0 or Data Input of DFF0	
reg<47:42>	Matrix Out: In0 of LUT2_1 or Clock Input of DFF1	
reg<53:48>	Matrix Out: In1 of LUT2_1 or Data Input of DFF1	
reg<59:54>	Matrix Out: In0 of LUT2_2 or Clock Input of DFF2	
reg<65:60>	Matrix Out: In1 of LUT2_2 1 or Data Input of DFF2	
reg<71:66>	Matrix Out: In0 of LUT2_3 or Clock Input of DFF3	
reg<77:72>	Matrix Out: In1 of LUT2_3 1 or Data Input of DFF3	
reg<83:78>	Matrix Out: In0 of LUT2_4	
reg<89:84>	Matrix Out: In1 of LUT2_4	
reg<95:90>	Matrix Out: In0 of Inverter INV_0	
reg<101:96>	Matrix Out: PIN12 Digital Output Source	
reg<107:102>	Matrix Out: In0 of LUT3_0 or Clock Input of DFF4	
reg<113:108>	Matrix Out: In1 of LUT3_0 or Data Input of DFF4	
reg<119:114>	Matrix Out: In2 of LUT3_0 or Resetb Input of DFF4	
reg<125:120>	Matrix Out: In0 of LUT3_1 or Clock Input of DFF5	
reg<131:126>	Matrix Out: In1 of LUT3_1 or Data Input of DFF5	
reg<137:132>	Matrix Out: In2 of LUT3_1 or Resetb(Setb) of DFF5	
reg<143:138>	Matrix Out: In0 of LUT3_2 or Clock Input of DFF6	
reg<149:144>	Matrix Out: In1 of LUT3_2 or Data Input of DFF6	
reg<155:150>	Matrix Out: In2 of LUT3_2 or Resetb Input of DFF6	
reg<161:156>	Matrix Out: In0 of LUT3_3 or Clock Input of DFF7	
reg<167:162>	Matrix Out: In1 of LUT3_3 or Data Input of DFF7	
reg<173:168>	Matrix Out: In2 of LUT3_3 or Resetb(Setb) of DFF7	
reg<179:174>	Matrix Out: In0 of LUT3_4	
reg<185:180>	Matrix Out: In1 of LUT3_4	
reg<191:186>	Matrix Out: In2 of LUT3_4	
reg<197:192>	Matrix Out: In0 of LUT3_5	
reg<203:198>	Matrix Out: In1 of LUT3_5	
reg<209:204>	Matrix Out: In2 of LUT3_5	
reg<215:210>	Matrix Out: In0 of LUT3_6	
reg<221:216>	Matrix Out: In1 of LUT3_6	
reg<227:222>	Matrix Out: In2 of LUT3_6	
reg<233:228>	Matrix Out: In0 of LUT3_7	
reg<239:234>	Matrix Out: In1 of LUT3_7	
reg<245:240>	Matrix Out: In2 of LUT3_7	

Register Bit Address	Signal Function	Register Bit Definition
reg<251:246>	Matrix Out: In0 of LUT3_8 or Input of Pipe delay	
reg<257:252>	Matrix Out: In1 of LUT3_8 or Resetb of Pipe delay	
reg<263:258>	Matrix Out: In2 of LUT3_8 or Clock of Pipe delay	
reg<269:264>	Matrix Out: In0 of LUT4_0 or Input for delay2(couter2) external clock	
reg<275:270>	Matrix Out: In1 of LUT4_0 or Input for delay2 data(counter2 reset)	
reg<281:276>	Matrix Out: In2 of LUT4_0	
reg<287:282>	Matrix Out: In3 of LUT4_0	
reg<293:288>	Matrix Out: In0 of LUT4_1 or Input for delay3(couter3) external clock	
reg<299:294>	Matrix Out: In1 of LUT4_1 or Input for delay3 data(counter3 reset)	
reg<305:300>	Matrix Out: In2 of LUT4_1	
reg<311:306>	Matrix Out: In3 of LUT4_1	
reg<317:312>	Matrix Out: Input for delay0 data(counter0 external clock)	
reg<323:318>	Matrix Out: Input for delay1(counter1) external clock	
reg<329:324>	Matrix Out: Input for delay1 data(counter1 reset)	
reg<335:330>	Matrix Out: Not used	
reg<341:336>	Matrix Out: pdb(power down) for ACMP0	
reg<347:342>	Matrix Out: pdb(power down) for ACMP1	
reg<353:348>	Matrix Out: Input for programmable delay (deglitch filter input)	
reg<359:354>	Matrix Out: Power down for osc (1: Power down)	
reg<365:360>	Matrix Out: PIN8 Digital Output Source	
reg<371:366>	Matrix Out: PIN9 Digital Output Source	
reg<377:372>	Matrix Out: PIN10 Digital Output Source	
reg<383:378>	Matrix Out: Output Enable of PIN10	
reg<389:384>	Reserved	
reg<395:390>	Reserved	
LUT2_0 or DFF0		
reg<399:396>	LUT2_0 data or the following	
reg<396>	DFF0 or Latch select	0: DFF function 1: Latch function
reg<397>	DFF0 output select	0: Q output 1: nQ output
reg<398>	DFF0 initial polarity select	0: Low 1: High
LUT2_1 or DFF1		
reg<403:400>	LUT2_1 data or the following	0: DFF function 1: Latch function
reg<400>	DFF1 or Latch select	0: DFF function 1: Latch function
reg<401>	DFF1 output select	0: Q output 1: nQ output

Register Bit Address	Signal Function	Register Bit Definition
reg<402>	DFF1 initial polarity select	0: Low 1: High
LUT2_2 or DFF2		
reg<407:404>	LUT2_2 data or the following	
reg<404>	DFF2 or Latch select	0: DFF function 1: Latch function
reg<405>	DFF2 output select	0: Q output 1: nQ output
reg<406>	DFF2 initial polarity select	0: Low 1: High
LUT2_3 or DFF3		
reg<411:408>	LUT2_3 data or the following	
reg<408>	DFF3 or Latch select	0: DFF function 1: Latch function
reg<409>	DFF3 output select	0: Q output 1: nQ output
reg<410>	DFF3 initial polarity select	0: Low 1: High
LUT2_4		
reg<415:412>	LUT2_4 data	
reg<419:416>	Reserved	
LUT2/DFF Select		
reg<420>	LUT2_0 or DFF0 select	0: LUT2_0 1: DFF0
reg<421>	LUT2_1 or DFF1 select	0: LUT2_1 1: DFF1
reg<422>	LUT2_2 or DFF2 select	0: LUT2_2 1: DFF2
reg<423>	LUT2_3 or DFF3 select	0: LUT2_3 1: DFF3
LUT3_0 or DFF4		
reg<431:424>	LUT3_0 data or the following	
reg<424>	DFF4 or Latch select	0: DFF function 1: Latch function
reg<425>	DFF4 output select	0: Q output 1: nQ output
reg<426>	DFF4 rstb/setb select	0: resetb from matrix output 1: setb from matrix output
reg<427>	DFF4 initial polarity select	0: Low 1: High
LUT3_1 or DFF5		
reg<439:432>	LUT3_1 data or the following	
reg<432>	DFF5 or Latch select	0: DFF function 1: Latch function
reg<433>	DFF5 output select	0: Q output 1: nQ output
reg<434>	DFF5 rstb/setb select	0: resetb from matrix output 1: setb from matrix output

Register Bit Address	Signal Function	Register Bit Definition
reg<435>	DFF5 initial polarity select	0: Low 1: High
LUT3_2 or DFF6		
reg<447:440>	LUT3_2 data or the following	
reg<440>	DFF6 or Latch select	0: DFF function 1: Latch function
reg<441>	DFF6 output select	0: Q output 1: nQ output
reg<442>	DFF6 rstb/setb select	0: resetb from matrix output 1: setb from matrix output
reg<443>	DFF6 initial polarity select	0: Low 1: High
LUT3_3 or DFF7		
reg<455:448>	LUT3_3 data or the following	
reg<448>	DFF7 or Latch select	0: DFF function 1: Latch function
reg<449>	DFF7 output select	0: Q output 1: nQ output
reg<450>	DFF7 rstb/setb select	0: resetb from matrix output 1: setb from matrix output
reg<451>	DFF7 initial polarity select	0: Low 1: High
LUT3_4		
reg<463:456>	LUT3_4 data	
LUT3_5		
reg<471:464>	LUT3_5 data	
LUT3_6		
reg<479:472>	LUT3_6 data	
LUT3_7		
reg<487:480>	LUT3_7 data	
LUT3_8 or pip number select		
reg<495:488>	reg<490:488>: OUT0 select	data (pipe number)
	reg<493:491>: OUT1 select	data (pipe number)
	reg<495:494>: Unused if Pipe Delay selected	Unused
LUT3/DFF Select		
reg<496>	LUT3_0 or DFF4 select	0: LUT3_0 1: DFF4
reg<497>	LUT3_1 or DFF5 select	0: LUT3_1 1: DFF5
reg<498>	LUT3_2 or DFF6 select	0: LUT3_3 1: DFF6
reg<499>	LUT3_3 or DFF7 select	0: LUT3_4 1: DFF7
reg<500>	LUT3_8 or pipe delay output select	0: LUT3_8 1: pipe delay
LUT4_0 or Counter/Delay2		
reg<516:501>	LUT4_0 data data or the following	

Register Bit Address	Signal Function	Register Bit Definition
reg<501>	Counter/delay2 mode selection	0: Delay Mode 1: Counter Mode
reg<504:502>	Counter/delay2 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter1 Overflow
reg<512:505>	Counter/delay2 Control Data	1 - 256 (delay time = (counter control data +2) /freq)
reg <514:513>	Delay2 Mode Select or asynchronous counter reset	00: on both falling and rising edges(for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset for counter mode
reg<517>	LUT4_0 or Counter2 select	0: LUT4_0 1: Counter2
LUT4_1 or Counter/Delay3		
reg<533:518>	LUT4_1 data or the following	
reg<518>	Counter/delay3 mode selection	0: Delay Mode 1: Counter Mode
reg<521:519>	Counter/delay3 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter1 Overflow
reg<529:522>	Counter/delay3 Control Data	1 - 256 (delay time = (counter control data +2) /freq)
reg<531:530>	Delay3 Mode Select or asynchronous counter reset	00: on both falling and rising edges(for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges
reg<534>	LUT4_1 or Counter3 select	0: LUT4_1 1: Counter3
RC Osc		
reg<535>	Force RC oscillator on	0: Auto Power on 1: Force Power on
reg<536>	RC Oscillator frequency control	0: 25 kHz 1: 2 MHz
reg<538:537>	Osc clock pre-divider	00:div1 01:div2 10: div4 11: div8

Register Bit Address	Signal Function	Register Bit Definition
reg<541:539>	Internal Oscillator frequency divider control 0	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg<544:542>	Internal Oscillator frequency divider control 1	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg<545>	External Clock Source Select	0: Internal Oscillator 1: External Clock from Pin12
reg<546>	Manufacturing test mode	
reg<547>	Reserved	
Counter/Delay 0		
reg<548>	Counter/delay0 mode selection	0: Delay Mode 1: Counter Mode
reg<551:549>	Counter/delay0 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter3 Overflow
reg<565:552>	Counter0 Control Data/Delay0 Time Control	1-16384: (delay time = (counter control data +2) /freq)
reg<567:566>	Delay0 Mode Select or asynchronous counter reset	00: on both falling and rising edges 01: on falling edge only 10: on rising edge only 11: no delay on either falling or rising edges
Counter/Delay 1		
reg<568>	Counter/delay1 mode selection	0: Delay Mode 1: Counter Mode
reg<571:569>	Counter/delay1 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock 111: Counter0 Overflow
reg<579:572>	Counter1 Control Data/Delay1 Time Control	1-256: (delay time = (counter control data +2) /freq)

Register Bit Address	Signal Function	Register Bit Definition
reg<581:580>	Delay1 Mode Select or asynchronous counter reset	00: on both falling and rising edges(for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset for counter mode
reg<595:582>	Reserved	
ACMP0		
reg<600:596>	ACMP0 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF(PIN4)
reg<602:601>	ACMP0 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
reg<604:603>	ACMP0 positive Input divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X
reg<605>	ACMP0 low bandwidth (typ: Max.1 MHz) enable.	0: off 1: on
reg<606>	ACMP0 positive input source select PIN3 and VDD	0: PIN3 1: VDD
ACMP1		
reg<611:607>	ACMP1 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD/3 11001: VDD/4 11010: EXT_VREF(PIN4)
reg<613:612>	ACMP1 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)

Register Bit Address	Signal Function	Register Bit Definition
reg<615:614>	ACMP1 positive Input divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X
reg<616>	ACMP1 100uA current source option	0: disable 1: enable
reg<617>	ACMP1 low bandwidth (typ: Max.1Mhz) enable.	0: off 1: on
reg<618>	ACMP1 positive input source select PIN6 and PIN3	0: PIN3 1: PIN6
reg<622:619>	Reserved	Reserved
PIN 2		
reg<624:623>	PIN2 mode control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
reg<626:625 >	PIN2 pull down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
PIN 3		
reg<629:627 >	PIN3 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain
reg<631:630 >	PIN3 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
reg<632>	PIN3 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<633>	PIN3 driver strength selection	0: 1X 1: 2X
PIN 4		
reg<636:634>	PIN4 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain
reg<638:637>	PIN4 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
reg<639>	PIN4 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable

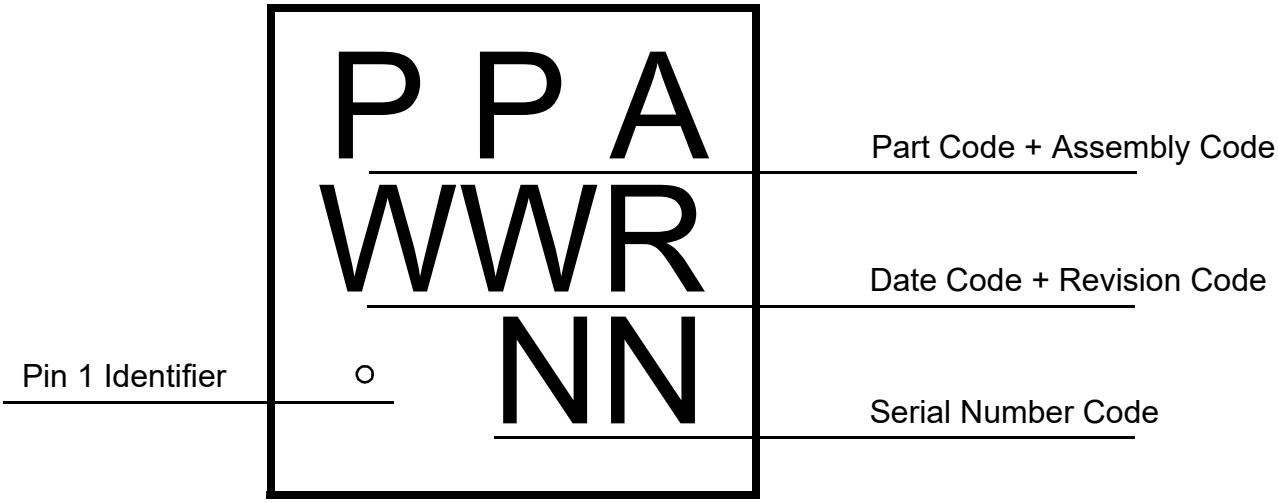
Register Bit Address	Signal Function	Register Bit Definition
reg<640>	PIN4 driver strength selection	0: 1X 1: 2X
PIN 5		
reg<643:641>	PIN5 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
reg<645:644>	PIN5 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
reg<646>	PIN5 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<647>	PIN5 driver strength selection	0: 1X 1: 2X
PIN 6		
reg<649:648>	PIN6 mode control (sig_pin6_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input / Output
reg<651:650>	PIN6 mode control (sig_pin6_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11:Open Drain NMOS 2X
reg<653:652>	PIN6 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
reg<654>	PIN6 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
PIN8		
reg<657:655>	PIN8 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
reg<659:658>	PIN8 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
reg<660>	PIN8 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<661>	PIN8 driver strength selection	0: 1X 1: 2X

Register Bit Address	Signal Function	Register Bit Definition
PIN 9		
reg<664:662>	PIN9 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
reg<666:665>	PIN9 pull down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
reg<667>	PIN9 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<668>	PIN9 driver strength selection	0: 1X 1: 2X
PIN 10		
reg<670:669>	PIN10 mode control (sig_pin10_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input / Output
reg<672:671>	PIN10 mode control (sig_pin10_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11:Open Drain NMOS 2X
reg<674:673>	PIN10 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
reg<675>	PIN10 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
Reserved		
reg<678:676>	Reserved	
reg<680:679>	Reserved	
reg<681>	Reserved	
reg<682>	Reserved	
PIN 12		
reg<685:683>	PIN12 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open drain
reg<687:686>	PIN12 pull up/down resistor value selection	00: floating 01: 10k 10: 100K 11: 1M
reg<688>	PIN12 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable

Register Bit Address	Signal Function	Register Bit Definition
reg<689>	PIN12 driver strength selection	0: 1X 1: 2X
reg<690>	Pipe delay OUT1 polarity select bit	0: Non-inverted 1: Inverted
reg<698:691>	8-bit pattern id	
reg<699>	filter0 output polarity select	0: Non-inverting 1: Inverting
reg<701:700>	Reserved	Reserved
reg<702>	GPIO quick charge enable	0: Disable 1: Enable
reg<706:703>	Reserved	Reserved
reg<707>	Force bandgap on	0: Auto-mode 1: Enable
reg<708>	VREF1 Output Active Buffer Control	0: Disabled 1: Enabled
reg<711:709>	VREF1 Output Source Select	000: ACMP0 reference voltage 001: ACMP1 reference voltage 100: VDD/2 101: VDD/3 110: VDD/4
reg<712>	NVM data read disable	0: Disable (read enable) 1: Enable (read disable)
reg<713>	NVM power down (or NVM data programming disable)	0: None (or programming enable) 1: Power Down (or programming disable)
reg<714>	Power Divider Power	0: Power down 1: Power On
reg<715>	POR Auto Power detect	0: Enable 1: Disable
reg<716>	Charge pump for analog macrocell enable (when VDD <=2.7V turn on)	0: Disable (automatic on/off control) 1: Enable (always on)
reg<717>	VDD bypass enable	0: Regulator auto on 1: Regualtor off (VDD bypass)
reg<718>	PIN2 edge detect mode	0: rising edge 1: falling edge
reg<719>	Bypass the pin2	0: PIN2 edge active 1: PIN2 high active
reg<720>	PIN2 reset enable	0: Disable 1: Enable
reg<721>	Reserved	Reserved
reg<727:722>	Reserved	Reserved
reg<735:728>	Reserved	Reserved
reg<741:736>	Reserved	Reserved
reg<743:742>	Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	00: 163 ns 01: 305 ns 10: 446 ns 11: 588 ns
reg<745:744>	Select the edge mode of programmable delay & edge detector	00: rising edge detector 01: falling edge detector 10: both edge detector 11: both edge delay

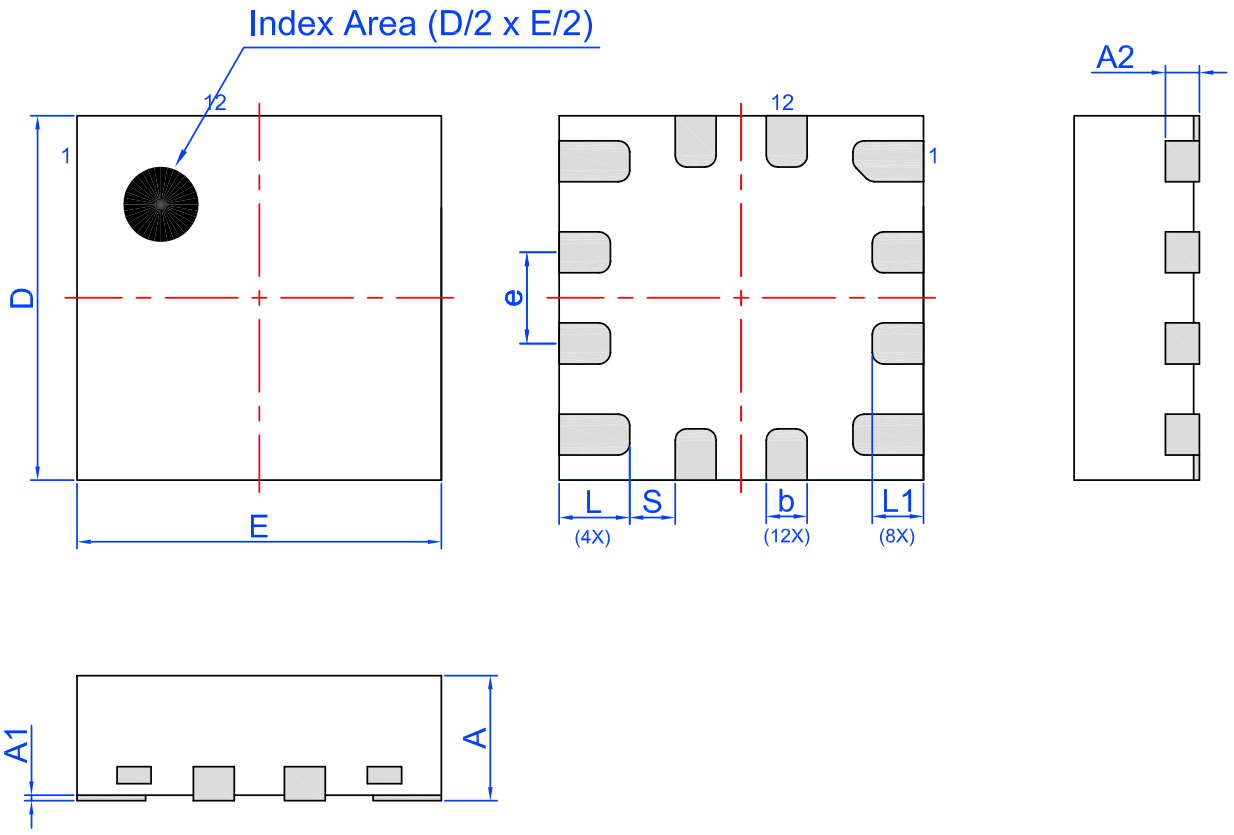
Register Bit Address	Signal Function	Register Bit Definition
reg<746>	programmable delay or filter output select	0: programmable delay output 1: filter output
reg<751:747>	Reserved	Reserved
reg<757:752>	Reserved	Reserved
reg<758>	Reserved	Reserved
reg<759>	Reserved	Reserved
reg<767:760>	Reserved	Reserved

18.0 Package Top Marking System Definition



19.0 Package Drawing and Dimensions

12 Lead STQFN FCA Package 1.6 x 1.6 mm



Unit: mm

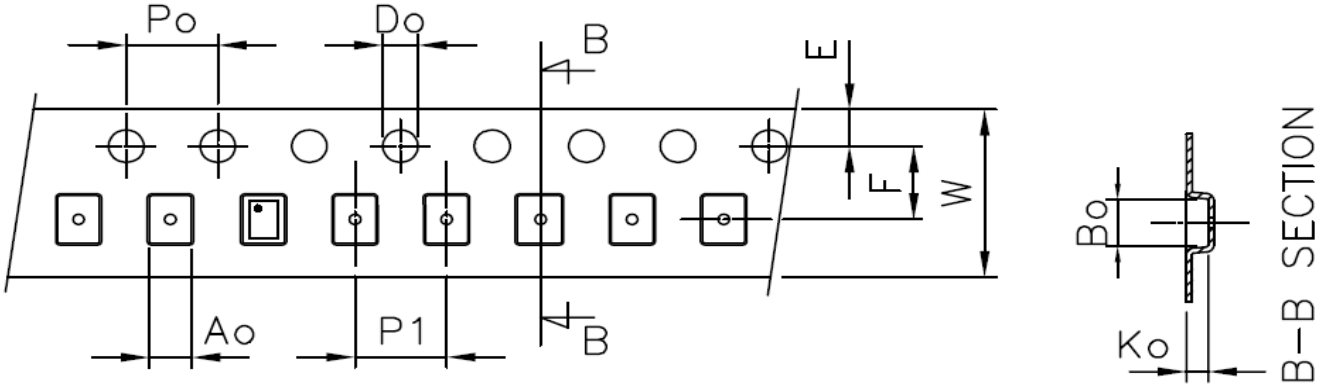
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

20.0 Tape and Reel Specifications

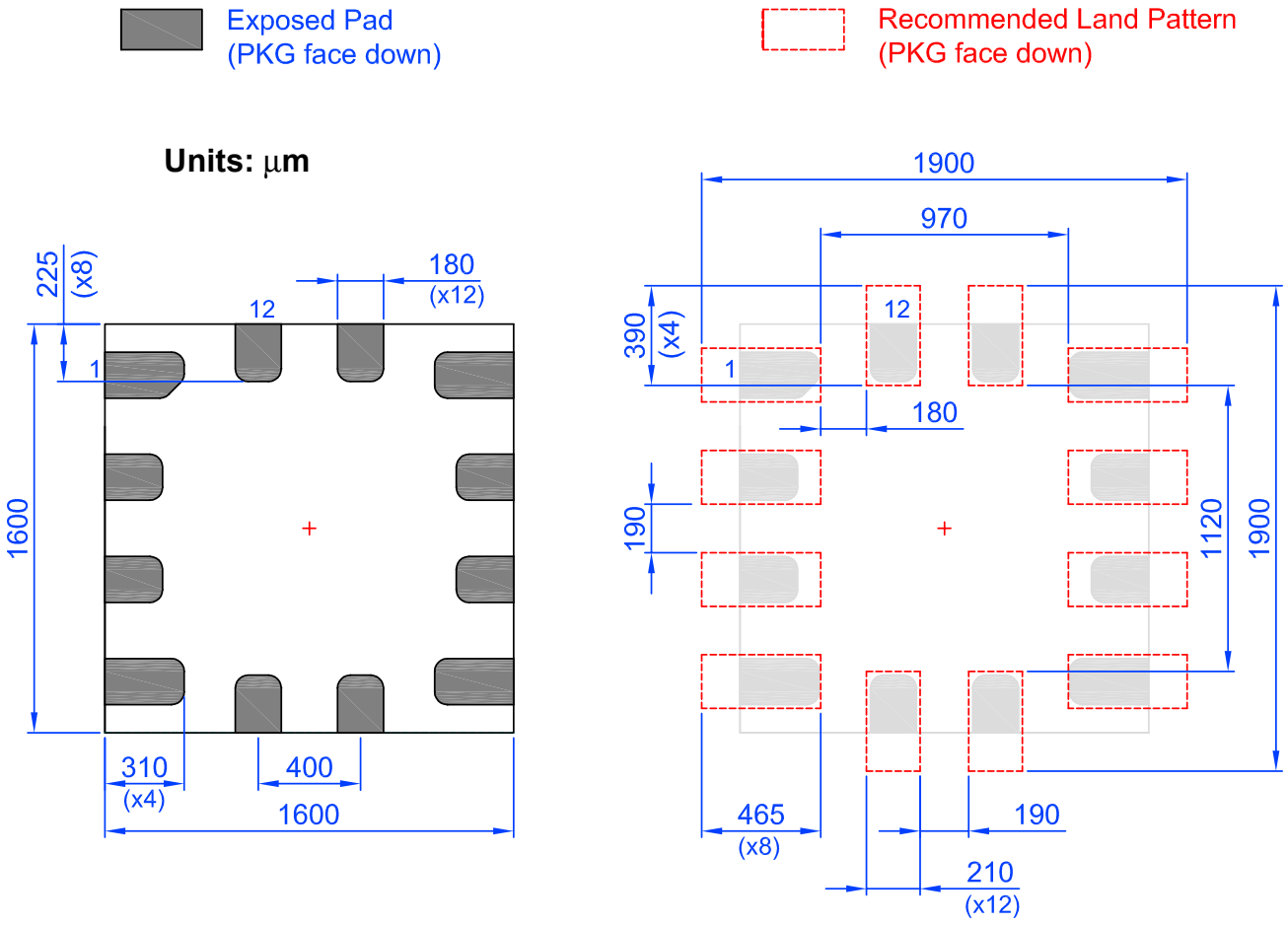
Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FCA 0.4P Green	10	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

20.1 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FCA 0.4P Green	1.9	1.9	0.8	4	4	1.5	1.75	3.5	8



21.0 Recommended Land Pattern



22.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

23.0 Revision History

Date	Version	Change
10/29/2019	1.08	Updated last page with disclaimer and contacts Added pre front page Fixed typos Added additional information about V_{DD2} to IO Pins section
2/27/2018	1.07	Fixed typos
10/11/2017	1.06	Updated Electrical Spec Fixed typos Updated POR sequence
5/7/2017	1.05	Fixed typos Updated Silego Website & Support Updated Section Programmable Delay / Edge Detector Updated Electrical Spec
5/30/2016	1.04	Updated Programmable Delay information
2/1/2016	1.03	Updated section Power On Reset
1/29/2016	1.02	Updated Silego Website & Support Fixed typos
12/29/2015	1.01	Updated Electrical Spec
12/9/2015	1.00	Production Release
12/7/2015	0.52	Updated front page
11/19/2015	0.51	Added VDD2 information to POR section Updated pin description Updated Absolute maximum conditions
11/04/2015	0.50	Preliminary Release
10/28/2015	0.15	Updated Absolute maximum conditions
10/20/2015	0.14	Fixed typos
9/16/2015	0.13	Added VDD2 tables Added Vhys, Rpup, Rpdwn, PONthr, POFFthr Added EI. Spec table for VDD = 1.8 V
8/25/2015	0.12	Updated references to VDD and VDD2 Fixed typos Updated Front Page, Sections 1, 5, 6, 7, 8 , 9, 10, 12.
7/21/2015	0.11	Updated Electrical Characteristics
6/24/2015	0.1	Initial release

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