General Description

The SLG46811 provides a small, low power component for commonly used Mixed-Signal functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG46811. This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- Multichannel Sampling Analog Comparator (MS ACMP)
  - Sampling up to Four Analog Channels
  - Selectable Voltage Reference for Each Channel
  - Different Sampling Scenarios
  - Synchronous or Asynchronous Result Appearance
- Integrated Voltage References (Vref)
- Twelve Combination Function Macrocells
  - Two 2-Bit LUT or DFF/LATCH Macrocells
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Four 3-Bit LUT or DFF/LATCH with Set/Reset
  - Four Selectable DFF/LATCH or 3-bit LUTs or Shift Registers
  - One 4-Bit LUT or DFF/LATCH with Set/Reset Macro-cell
- Six Multi-Function Macrocells
  - Five Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counter/FSM
- Extended Pattern Generator
  - Up to 8 Parallel Outputs
  - 92 bytes Pattern Stored in the NVM
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Two Oscillators (OSC)
  - Selectable 2.048 kHz or 10 kHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On Reset (POR) with CRC
- Read Back Protection (Read Lock)
- Power Supply
  - 2.3 V ≤ V_{DD} ≤ 5.5 V
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- Available Package
  - 12-pin STQFN: 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch

Applications

- Notebook and Tablet PCs
- Smartphones and Fitness Bands
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

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1 Block Diagram

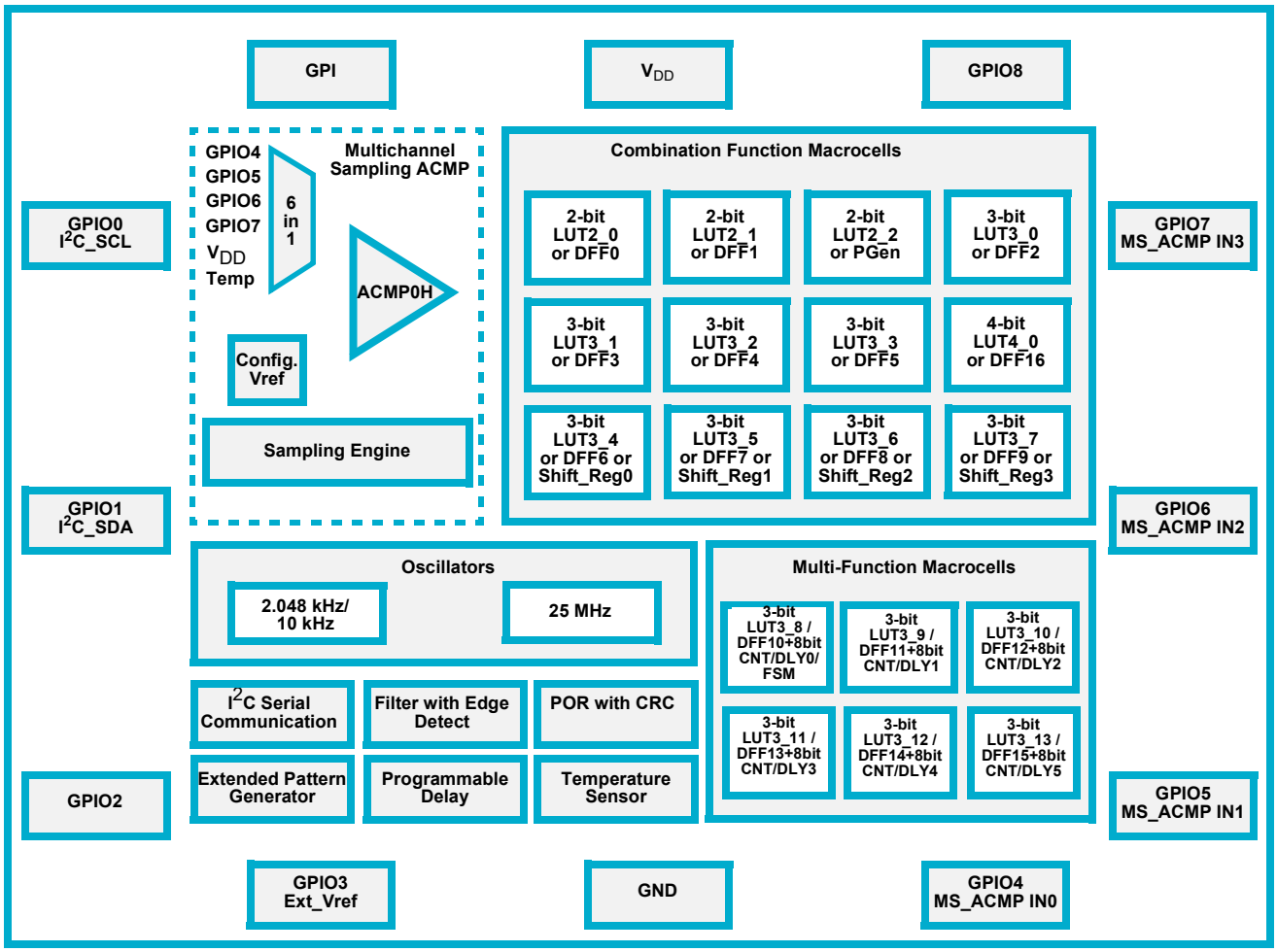
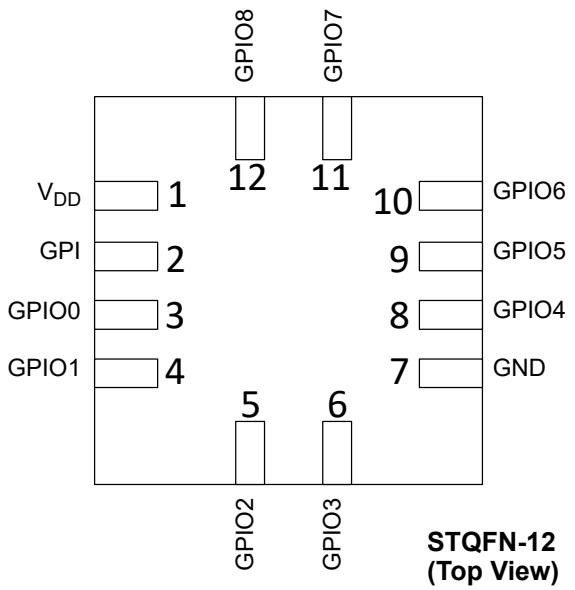


Figure 1: Block Diagram

2 Pinout

2.1 PIN CONFIGURATION - STQFN- 12



STQFN-12
(Top View)

Pin #	Pin Name	Pin Functions
1	V_{DD}	Power Supply
2	GPI	GPI, SLA_0, EXT_CLK_OSC0
3	GPIO0	GPIO, I^2C SCL
4	GPIO1	GPIO, I^2C SDA
5	GPIO2	GPIO with OE
6	GPIO3	GPIO with OE, SLA_1, EXT_Vref
7	GND	Ground
8	GPIO4	GPIO, SLA_2, MS ACMP input 0
9	GPIO5	GPIO, MS ACMP input 1
10	GPIO6	GPIO, MS ACMP input 2
11	GPIO7	GPIO with OE, MS ACMP input 3, SLA_3, EXT_CLK_OSC1
12	GPIO8	GPIO with OE

Legend:

OE: Output Enable
MS ACMP input: Multichannel Sample ACMP Positive Input
I^2C SCL: I^2C Clock Input
I^2C SDA: I^2C Data Input/Output
EXT_CLKx: External Clock Input
SLA: Slave Address

Table 1: Functional Pin Description

STQFN 12 Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	V_{DD}	V_{DD}	Power Supply	--	--
2	GPI	GPI	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		Slave Address 0		--	--
		External Clock of OSC0	External Clock Connection	--	--
3	GPIO0	GPIO	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Open-Drain NMOS (3.2x)
				Digital Input with Schmitt Trigger	
				Low Voltage Digital Input	--
		I^2C SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--

Table 1: Functional Pin Description (Continued)

STQFN 12 Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
4	GPIO1	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (3.2x)
				Digital Input with Schmitt Trigger	
				Low Voltage Digital Input	
		I^2C SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
5	GPIO2	GPIO	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
6	GPIO3	GPIO	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		EXT_Vref	ACMP Inverting Input	Analog	--
		Slave Address 1		--	--
7	GND	GND	Power Supply	--	--
8	GPIO4	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		MS_ACMP In0	Positive Input 0 of MS ACMP	Analog	--
		Slave Address 2		--	--
9	GPIO5	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		MS ACMP In1	Positive Input 1 of MS ACMP	Analog	--
10	GPIO6	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		MS ACMP In2	Positive Input 2 of MS ACMP	Analog	--

Table 1: Functional Pin Description (Continued)

STQFN 12 Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
11	GPIO7	GPIO	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		MS ACMP In 3	Positive Input 3 of MS ACMP	Analog	--
		Slave Address 3		--	--
		External Clock of OSC1	External Clock Connection	--	--
12	GPIO8	GPIO	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--

Note 1 General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure or as a 3-state output.

Table 2: Pin Type Definitions

Pin Type	Description
V_{DD}	Power Supply
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GND	Ground

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.3	7	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitive Level		1		

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		2.3	5.5	V
Operating Temperature		-40	85	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input **(Note 1)**	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger (Positive Going Threshold Voltage min = 0.4xV_{DD}, max = 0.7xV_{DD})	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input **(Note 1)**	1.25	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 1)**	GND- 0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger (Negative Going Threshold Voltage min = 0.3xV_{DD}, max = 0.6xV_{DD})	GND- 0.4	--	0.2x V_{DD}	V
		Low-Level Logic Input **(Note 1)**	GND- 0.5	--	0.5	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.18	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.68	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 5.0 V ± 10 %, I_{OH} = 5 mA	4.16	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OH} = 1 mA	2.24	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OH} = 3 mA	2.83	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 5.0 V ± 10 %, I_{OH} = 5 mA	4.33	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL}= 1 mA	--	--	0.092	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.227	V
		Push-Pull, 1x Drive, V_{DD} = 5.0 V ± 10 %, I_{OL}= 5 mA	--	--	0.283	V
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.045	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL}= 3 mA	--	--	0.111	V
		Push-Pull, 2x Drive, V_{DD} = 5.0 V ± 10 %, I_{OL} = 5 mA	--	--	0.140	V
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.036	V
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.089	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	NMOS OD, 1x Drive, V_{DD} = 5.0 V ± 10 %, I_{OL} = 5 mA	--	--	0.112	V
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ± 8 %, I_{OL} = 1 mA	--	--	0.018	V
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ± 10 %, I_{OL} = 3 mA	--	--	0.046	V
		NMOS OD, 2x Drive, V_{DD} = 5.0 V ± 10 %, I_{OL} = 5 mA	--	--	0.059	V
I_{OH}	HIGH-Level Output Pulse Current **(Note 2)**	Push-Pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	1.520	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	5.125	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5.0 V ± 10 %, V_{OH} = 2.4 V	19.589	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OH} = V_{DD} - 0.2	3.008	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, V_{OH} = 2.4 V	10.106	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5.0 V ± 10 %, V_{OH} = 2.4 V	37.960	--	--	mA
I_{OL}	LOW-Level Output Pulse Current **(Note 2)**	Push-Pull, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	1.483	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	4.622	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5.0 V ± 10 %, V_{OL} = 0.4 V	6.250	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	2.965	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	9.228	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5.0 V ± 10 %, V_{OL} = 0.4 V	12.443	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	3.676	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	11.438	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 5.0 V ± 10 %, V_{OL} = 0.4 V	15.397	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 2.5 V ± 8 %, V_{OL} = 0.15 V	7.285	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 3.3 V ± 10 %, V_{OL} = 0.4 V	22.589	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 5.0 V ± 10 %, V_{OL} = 0.4 V	30.030	--	--	mA
T_{SU}	Startup Time	T_{RAMP} =1 V/µs , From V_{DD} rising past PON_{THR}	--	1.85	3.42	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.55	1.86	2.17	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.06	1.34	1.62	V
R_{PULL}	Pull-up or Pull-down Resistance	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND for Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k For Pull-up: V_{IN} = GND for Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance	T = 25 °C		2.4		pF

Note 1 No hysteresis.
Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.5 I²C PINS ELECTRICAL CHARACTERISTICS

Table 7: EC of SDA and SCL Pins, DI Mode, at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	0.05xV_{DD}	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain or open collector) at 3 mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain or open collector) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V
I_{OL}	LOW-Level Output Current	V_{OL} = 0.4 V, V_{DD} = 2.3 V	3	--	20	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.3 V	3	--	20	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	20	--	mA
		V_{OL}= 0.6 V, V_{DD} = 5.5 V	6	--	--	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5V)	250	10x (V_{DD}/5.5V)	120	ns
t_{SP}	Input Filter Spike Suppression	Digital Input (SDA)	50	--	50	--	ns
		Digital Input (SCL)	50	--	50	--	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	--	10	pF

Note 1 Does not meet standard I²C specifications: t_{of} = 20x(V_{DD}/5.5V) (min).
Note 2 For Fast-mode Plus SDA pin must be configured as NMOS 3.2x Open-Drain, see register [613] in section 18.

Table 8: EC of SDA and SCL Pins, DILV Mode, at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
V_{IL}	LOW-level Input Voltage **(Note 1)**		--	0.7	V
V_{IH}	HIGH-level Input Voltage **(Note 1)**		1.25	--	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain or open collector) at 3 mA sink current, V_{DD} > 2 V	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain or open collector) at 2 mA sink current, V_{DD} ≤ 2 V	0	0.2xV_{DD}	V
I_{OL}	LOW-Level Output Current	V_{OL} = 0.4 V, V_{DD} = 2.3 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.3 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	mA
		V_{OL}= 0.6 V, V_{DD} = 5.5 V	6	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5V)	250	ns
t_{SP}	Input Filter Spike Suppression (SCL, SDA)	Digital Input LOW Voltage (SDA)	50	--	ns
		Digital Input LOW Voltage (SCL)	50	--	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	pF

Note 1 Does not meet standard I^2C specifications: V_{IL} = 0.3xV_{DD} (max); V_{IH} = 0.7xV_{DD} (min); t_{of} = 20x(V_{DD}/5.5V) (min).

Table 9: I^2C Bus Timing Characteristics, DI Mode, at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Speed				Unit
			400 kHz		1 MHz		
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Rise Time		--	300	--	120	ns
t_F	Inputs Fall Time		--	300	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	260	--	ns
t_{VD_ACK}	Data Out Hold Time		50	--	50	--	ns
t_{VD_DAT}	Clock Low to Data Out Valid		--	900	--	450	ns

Table 9: I²C Bus Timing Characteristics, DI Mode, at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Speed				Unit
			400 kHz		1 MHz		
			Min	Max	Min	Max	
Note 1 Timing diagram can be found in the Figure 84. **Note 2** Please follow official I²C spec UM10204.							

Table 10: I²C Bus Timing Characteristics, DILV Mode, at T = -40°C to +85°C, V_{DD} = 2.3V to 5.5V Unless Otherwise Noted

Parameter	Description	Condition	Speed		Unit
			400 kHz		
			Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	ns
t_{HD_STA}	Start Hold Time		600	--	ns
t_{SU_STA}	Start Set-up Time		600	--	ns
t_{HD_DAT}	Data Hold Time **(Note 1)**		264	--	ns
t_{SU_DAT}	Data Set-up Time **(Note 1)**		382	--	ns
t_R	Inputs Rise Time		--	300	ns
t_F	Inputs Fall Time		--	300	ns
t_{SU_STO}	Stop Set-up Time		600	--	ns
t_{VD_ACK}	Data Out Hold Time		50	--	ns
t_{VD_DAT}	Clock Low to Data Out Valid		--	900	ns
Note 1 Does not meet standard I²C specifications: t_{HD_DAT} = 0 ns, t_{SU_DAT} = 100 ns. **Note 2** Please follow official I²C spec UM10204. **Note 3** When SCL Input is in Low-Level Logic mode max frequency is 400 kHz. **Note 4** Timing diagram can be found in the Figure 84.							

3.6 MACROCELLS CURRENT CONSUMPTION

Table 11: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	PDET+I^2C	0.06	0.08	0.13	µA
		PDET+BG+I^2C	0.38	0.41	0.49	µA
		Temperature Sensor Output	15.06	15.14	15.48	µA
		OSC2 25 MHz, Pre-divider = 1	82.44	106.46	162.02	µA
		OSC2 25 MHz, Pre-divider = 4	45.97	57.00	83.21	µA
		OSC2 25 MHz, Pre-divider = 8	39.62	48.35	69.35	µA
		OSC0 2.048 kHz, Pre-divider = 1	0.33	0.36	0.44	µA
		OSC0 2.048 kHz, Pre-divider = 4	0.33	0.36	0.44	µA
		OSC0 2.048 kHz, Pre-divider = 8	0.33	0.36	0.44	µA
		OSC0 10 kHz, Pre-divider = 1	0.45	0.49	0.60	µA
		OSC0 10 kHz, Pre-divider = 4	0.44	0.48	0.57	µA
		OSC0 10 kHz, Pre-divider = 8	0.44	0.47	0.56	µA
		MS ACMP in regular mode (Vref Source - External VIN+ = 0 V, VIN- = 32 mV), level sensitive	14.44	14.83	15.95	µA
		MS ACMP in regular mode (Vref Source – Internal V_{IN+} = 0 V; V_{IN-} = 32 mV), level sensitive	21.56	21.97	23.21	µA
		MS ACMP in regular mode (Vref Source – Internal V_{IN+} = 1 M Pull-up V_{IN-} = 32 mV), level sensitive	35.40	36.11	38.18	µA
		MS ACMP in continuous sampling mode, four channels, V_{IN+} = 2.048 mV, V_{IN-} = 32 mV, 10 kHz oscillator clock (average consumption), level sensitive	35.78	36.47	38.57	µA

3.7 TIMING CHARACTERISTICS

Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1x	31	32	22	24	17	18	ns
tpd	Delay	Digital Input to PP 2x	30	32	21	23	16	17	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	31	32	22	24	17	18	ns
tpd	Delay	Low Voltage Digital Input to PP 1x	33	270	24	178	19	104	ns
tpd	Delay	Digital input to NMOS 1x	--	31	--	22	--	17	ns
tpd	Delay	Digital input to NMOS 2x	--	30	--	22	--	16	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 1	28	--	20	--	15	--	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 0	--	27	--	20	--	15	ns
tpd	Delay	1x3 State Hi-Z to 1	28	--	20	--	15	--	ns
tpd	Delay	1x3 State Hi-Z to 0	--	27	--	20	--	15	ns
tpd	Delay	2x3 State Hi-Z to 1	27	--	19	--	15	--	ns

Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C (Continued)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	2x3 State Hi-Z to 0	--	26	--	19	--	14	ns
tpd	Delay	LATCH Q	15	16	12	11	8	8	ns
tpd	Delay	LATCH nQ	16	16	11	12	9	8	ns
tpd	Delay	LATCH nRESET High Q	23	24	16	18	12	12	ns
tpd	Delay	LATCH nRESET High nQ	23	25	17	18	12	12	ns
tpd	Delay	LATCH nRESET Low Q	23	24	16	17	12	12	ns
tpd	Delay	LATCH nRESET Low nQ	23	24	16	18	12	12	ns
tpd	Delay	LATCH nSET High Q	21	23	15	16	11	11	ns
tpd	Delay	LATCH nSET High nQ	22	22	15	17	11	11	ns
tpd	Delay	LATCH nSET Low Q	21	22	14	16	10	11	ns
tpd	Delay	LATCH nSET Low nQ	21	22	16	15	11	11	ns
tpd	Delay	2-bit LUT	13	13	10	10	7	7	ns
tpd	Delay	3-bit LUT	19	21	15	14	11	10	ns
tpd	Delay	4-bit LUT	18	20	13	14	9	10	ns
tpd	Delay	Shift Register Transition	70	71	49	50	32	32	ns
tpd	Delay	Shift Register Reset	26	25	19	18	13	13	ns
tpd	Delay	Edge detect	18	18	13	13	9	9	ns
tw	Width	Edge detect	212	212	157	157	113	114	ns
tpd	Delay	Edge detect Delayed	230	232	169	170	122	122	ns
tpd	Delay	DFF Q	15	17	11	13	8	9	ns
tpd	Delay	DFF nQ	16	17	12	13	8	9	ns
tpd	Delay	DFF nRESET High Q	--	23	--	17	--	12	ns
tpd	Delay	DFF nRESET High nQ	22	--	16	--	11	--	ns
tpd	Delay	DFF nRESET Low Q	--	23	--	16	--	12	ns
tpd	Delay	DFF nRESET Low nQ	22	--	15	--	11	--	ns
tpd	Delay	DFF nSET High Q	22	--	16	--	11	--	ns
tpd	Delay	DFF nSET High nQ	--	23	--	17	--	12	ns
tpd	Delay	DFF nSET Low Q	22	--	15	--	11	--	ns
tpd	Delay	DFF nSET Low nQ	--	23	--	17	--	12	ns
tpd	Delay	CNT/DLY	81	79	59	70	43	70	ns
tpd	Delay	PGen CLK	18	16	14	12	9	9	ns
tpd	Delay	PGen nRESET Z to 0	--	19	--	14	--	10	ns
tpd	Delay	PGen nRESET Z to 1	18	--	13	--	9	--	ns
tpd	Delay	Extended PGen CLK	488	488	487	487	493	495	ns
tpd	Delay	Extended PGen nRESET Z to 0	--	67	--	48	--	35	ns
tpd	Delay	Extended PGen nRESET Z to 1	68	--	48	--	33	--	ns
tpd	Delay	Filter Q, nQ	122	125	93	95	68	69	ns

Table 13: Programmable Delay Expected Delays and Widths (Typical) at T = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse Width, 1 cell	mode: (any) edge detect, edge detect output	216	160	115	ns
tw	Pulse Width, 2 cell	mode: (any) edge detect, edge detect output	427	316	228	ns
tw	Pulse Width, 3 cell	mode: (any) edge detect, edge detect output	638	471	341	ns
tw	Pulse Width, 4 cell	mode: (any) edge detect, edge detect output	850	627	453	ns
time1	Delay, 1 cell	mode: (any) edge detect, edge detect output	18	13	9	ns
time1	Delay, 2 cell	mode: (any) edge detect, edge detect output	18	13	9	ns
time1	Delay, 3 cell	mode: (any) edge detect, edge detect output	18	13	9	ns
time1	Delay, 4 cell	mode: (any) edge detect, edge detect output	18	13	9	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	234	172	124	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	446	328	237	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	656	483	350	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	866	639	461	ns

Table 14: Typical Filter Rejection Pulse Width at T = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width, t_{block}	< 63	< 49	< 37	ns

3.8 COUNTER/DELAY CHARACTERISTICS

Table 15: Typical Counter/Delay Offset at T = 25 °C

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On time	25 MHz	auto	0.055	0.04	0.025	µs
Power-On time	2.048 kHz	auto	695	575	480	µs
Power-On time	10 kHz	auto	695	575	480	µs
Frequency Settling Time	25 MHz	auto	10	10	10	Stabilized Clk
Frequency Settling Time	2.048 kHz	auto	1	1	1	Stabilized Clk
Frequency Settling Time	10 kHz	auto	5	5	5	Stabilized Clk
Variable (CLK period)	25 MHz	forced	0-40	0-40	0-40	ns
Variable (CLK period)	2.048 kHz	forced	0-488	0-488	0-488	µs
Variable (CLK period)	10 kHz	forced	0-100	0-100	0-100	µs
Typical Propagation Delay (non-delayed edge)	25 MHz/ 2.048 kHz/ 10 kHz	either	35	25	18	ns

3.9 OSCILLATOR CHARACTERISTICS

Table 16: Oscillators Frequency Limits, V_{DD} = 2.3 V to 5.5 V

Parameter	Temperature Range					
	+25 °C			-40 °C to +85 °C		
	Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
2.048 kHz OSC0	2.015	2.081	+1.6	1.900	2.099	+2.5
			-1.6			-7.2
10 kHz OSC0	9.84	10.16	+1.6	9.46	10.16	+1.6
			-1.6			-5.4
25 MHz OSC1	24600	25400	+1.6	24000	25400	+1.6
			-1.6			-4.0

3.9.1 OSC Power-On Delay

Table 17: Oscillators Power-On Delay at T = -40 °C to +85 °C, OSC Power Setting: "Auto Power-On"

Power Supply Range (V_{DD}), V	OSC0 2.048 kHz		OSC0 10 kHz		OSC1 25 MHz		OSC1 25 MHz Start with Delay	
	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns
2.30	725	1098	725	1101	60	77	150	163
3.30	577	815	577	816	37	51	142	159
4.00	528	714	528	716	31	44	141	160
5.00	483	623	483	624	26	38	140	161
5.50	459	581	459	582	24	41	140	161

3.10 MS ACMP CHARACTERISTICS

Table 18: MS ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
V_{ACMP}	MS ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	MS ACMP Input Offset	MS ACMP Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV (regular mode)		-6.7	-0.6	5.2	mV
		MS ACMP Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV (sampling mode)		-4.3	1.1	7.2	mV
I_{LKG}	ACMP Input Leakage	$V_{IN} = V_{DD}$	V_{DD} = 2.3 V	--	1.5	6.0	nA
			V_{DD} = 3.3 V	--	1.5	6.0	nA
			V_{DD} = 5.5 V	--	1.5	6.0	nA

Table 18: MS ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
t_{start}	ACMP Startup Time	MS ACMP Power-On delay (regular mode)		--	--	70.8	µs
		MS ACMP Power-On delay (sampling mode), OSC0 = 10 kHz	Bandgap: Forced On, OSC0: Forced On	--	--	0.56	ms
		MS ACMP Power-On delay (sampling mode), OSC0 = 10 kHz	Bandgap: Auto-On, OSC0: Auto-On	--	--	2.66	ms
		MS ACMP Power-On delay (sampling mode), OSC0 = 10 kHz	Bandgap: Forced On, OSC0: Auto-On	--	--	1.23	ms
		MS ACMP Power-On delay (sampling mode), OSC0 = 10 kHz	Bandgap: Auto-On, OSC0: Forced On	--	--	2.59	ms
V_{HYS}	Built-in Hysteresis **(Note 1)**	V_{HYS} = 32 mV (sampling mode) **(Note 2)**	T = 25 °C	23.36	30.22	34.83	mV
		V_{HYS} = 64 mV (regular mode)	T = 25 °C	55.62	61.57	65.58	mV
		V_{HYS} = 64 mV (sampling mode)		55.01	62.16	66.64	mV
		V_{HYS} = 192 mV (regular mode)	T = 25 °C	182.69	189.56	193.88	mV
		V_{HYS} = 192 mV (sampling mode)		182.08	190.14	195.22	mV
		V_{HYS} = 32 mV (sampling mode) **(Note 2)**		21.08	30.22	37.44	mV
		V_{HYS} = 64 mV (regular mode)		52.29	61.57	67.63	mV
		V_{HYS} = 64 mV (sampling mode)		52.24	62.16	69.77	mV
		V_{HYS} = 192 mV (regular mode)		178.95	189.56	195.75	mV
		V_{HYS} = 192 mV (sampling mode)		179.54	190.14	198.71	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	10	--	GΩ
		Gain = 0.5x		1.6	1.9	2.4	MΩ
		Gain = 0.33x		1.6	1.9	2.4	MΩ
		Gain = 0.25x		1.6	1.9	2.4	MΩ

Table 18: MS ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parame-ter	Description	Note	Condition	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 10 mV, regular mode	Low to High	0.35	1.05	4.01	µs
			High to Low	0.53	1.45	3.30	µs
		Gain = 1, T = 25 °C, Vref = 32 mV to 2016 mV, Overdrive = 10 mV, regular mode	Low to High	0.56	1.05	2.49	µs
			High to Low	0.69	1.45	2.42	µs
		Gain = 0.25, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV, regular mode	Low to High	1.18	1.50	1.75	µs
			High to Low	2.23	2.49	2.84	µs
		Gain = 1, T = 25 °C, Vref = 32 mV to 2016 mV, Overdrive = 100 mV, regular mode	Low to High	0.23	0.34	0.48	µs
			High to Low	0.27	0.39	0.65	µs
		Gain = 0.25, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV, regular mode	Low to High	0.46	0.56	0.65	µs
			High to Low	1.33	1.48	1.70	µs
G	Gain error	G = 1		1	1	1	
		G = 0.5		0.498	0.500	0.503	
		G = 0.33		0.332	0.334	0.337	
		G = 0.25		0.249	0.251	0.253	
Vref	Vref Accuracy, Vref = 2016 mV		T = 25 °C	-0.43	-0.10	0.21	%
				-0.82	-0.10	0.24	%

Note 1 V_{IL} = Vin - V_{HYS}, V_{IH} = Vin.
Note 2 Available only in Sampling mode.

3.11 ANALOG TEMPERATURE SENSOR CHARACTERISTICS

Temperature Sensor typical nonlinearity ±0.57 % at V_{DD} = 2.3 V to 5.5 V.

Table 19: Temperature Sensor Output vs Temperature at V_{DD} = 2.3 V to 5.5 V

T, °C	TS OUT, V			Error, %
	Min	Typ	Max	
-40 °C	1.997	2.008	2.023	±0.75
-30 °C	1.951	1.963	1.979	±0.82
-20 °C	1.906	1.918	1.933	±0.78
-10 °C	1.861	1.872	1.886	±0.75
0 °C	1.814	1.826	1.840	±0.77
10 °C	1.769	1.779	1.792	±0.73
20 °C	1.722	1.733	1.745	±0.69
25 °C	1.699	1.710	1.722	±0.70
30 °C	1.675	1.686	1.698	±0.71
40 °C	1.628	1.639	1.651	±0.73
50 °C	1.579	1.591	1.603	±0.75
60 °C	1.531	1.543	1.555	±0.78
70 °C	1.482	1.494	1.507	±0.87
80 °C	1.433	1.446	1.458	±0.90
85 °C	1.409	1.421	1.433	±0.84
90 °C	1.384	1.397	1.409	±0.93
100 °C	1.335	1.347	1.359	±0.89
110 °C	1.285	1.298	1.310	±1.00
120 °C	1.235	1.249	1.260	±1.12
125 °C	1.210	1.224	1.236	±1.14
130 °C	1.185	1.200	1.211	±1.25

4 User Programmability

The SLG46811 is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

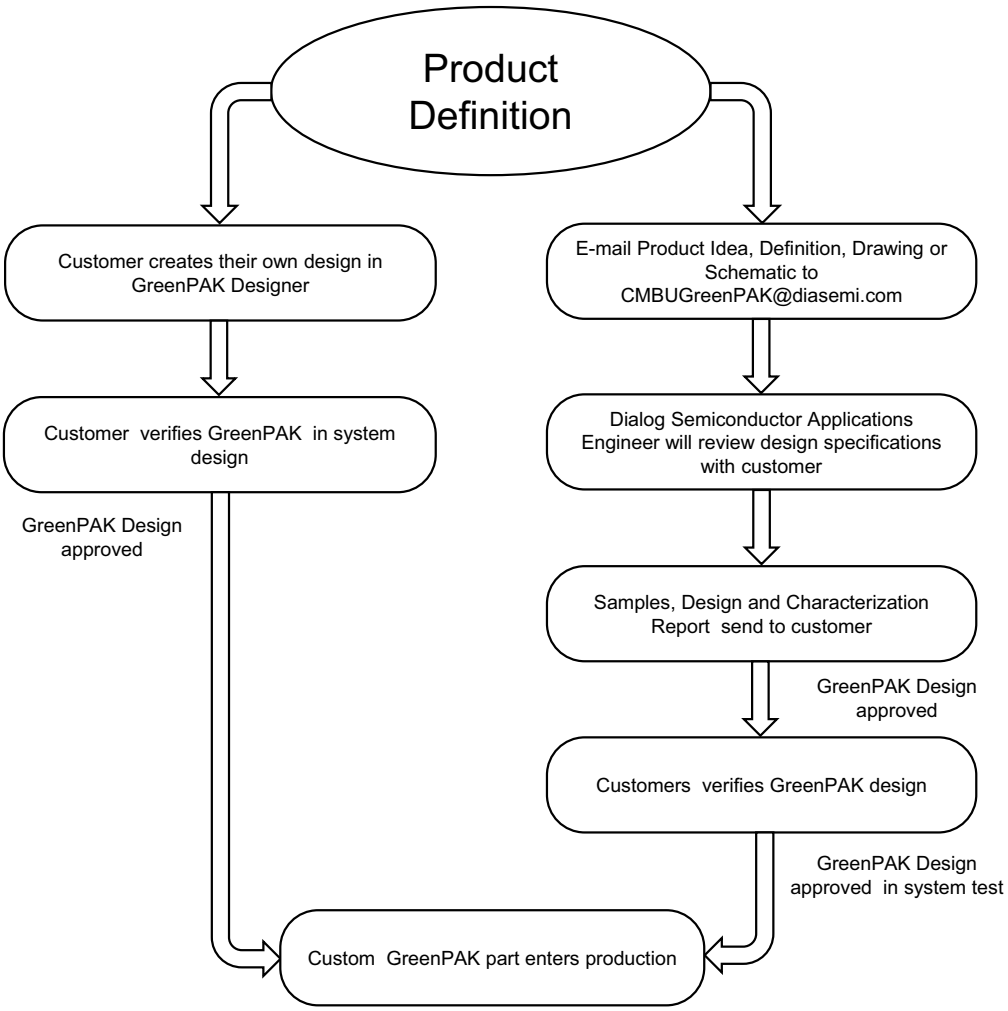


Figure 2: Steps to Create a Custom GreenPAK Device

5 IO Pins

The SLG46811 has a total of 9 GPIO and 1 GPI Pins which can function as either a user defined Input or Output.

5.1 GPIO PINS

Pins from GPIO0 to GPIO8 serve as General Purpose IO Pins. Input function of GPIO shared with I^2C virtual inputs. See Section 6.1.

5.2 GPI PINS

GPI serves as a General Purpose Input Pin.

5.3 PULL-UP/DOWN RESISTORS

All IO Pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either Pull-up or Pull-downs.

5.4 FAST PULL-UP/DOWN DURING POWER-UP

During power-up, IO Pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [594].

5.5 GPI STRUCTURE

5.5.1 GPI Structure (for GPI)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user
Note 2: OE is Matrix output, Digital In is Matrix input

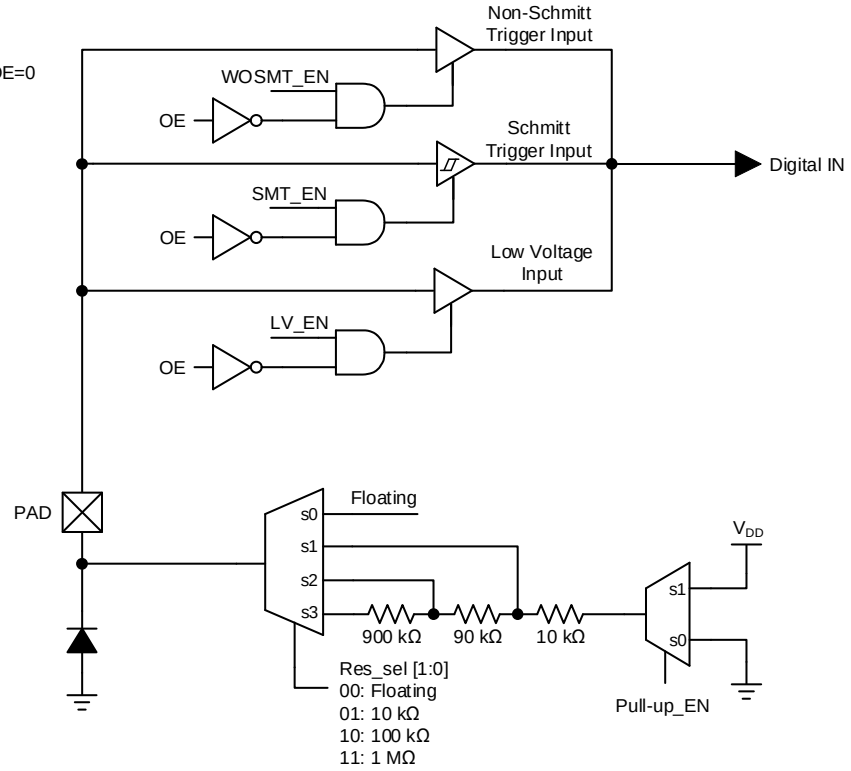


Figure 3: GPI Structure Diagram

5.6 GPIO WITH I²C MODE IO STRUCTURE

5.6.1 GPIO with I²C Mode Structure (for GPIO0 and GPIO1)

Input Mode [1:0]
00: Digital Input without Schmitt Trigger
01: Digital Input with Schmitt Trigger
10: Low Voltage Digital Input
11: Reserved

register [606]=1: Open-Drain NMOS for GPIO0
register [613]=1: Open-Drain NMOS for GPIO1

Note 1: OE cannot be selected by user and is controlled by register. Digital In is Matrix input.
Note 2: GPIO0 and GPIO1 do not support Push-Pull and PMOS Open-Drain modes.
Note 3: It is possible to apply an input voltage higher than V_{DD} to GPIO0 and GPIO1. However, this voltage should not exceed 5.5 V.
Note 4: Can be varied over PVT, for reference only.

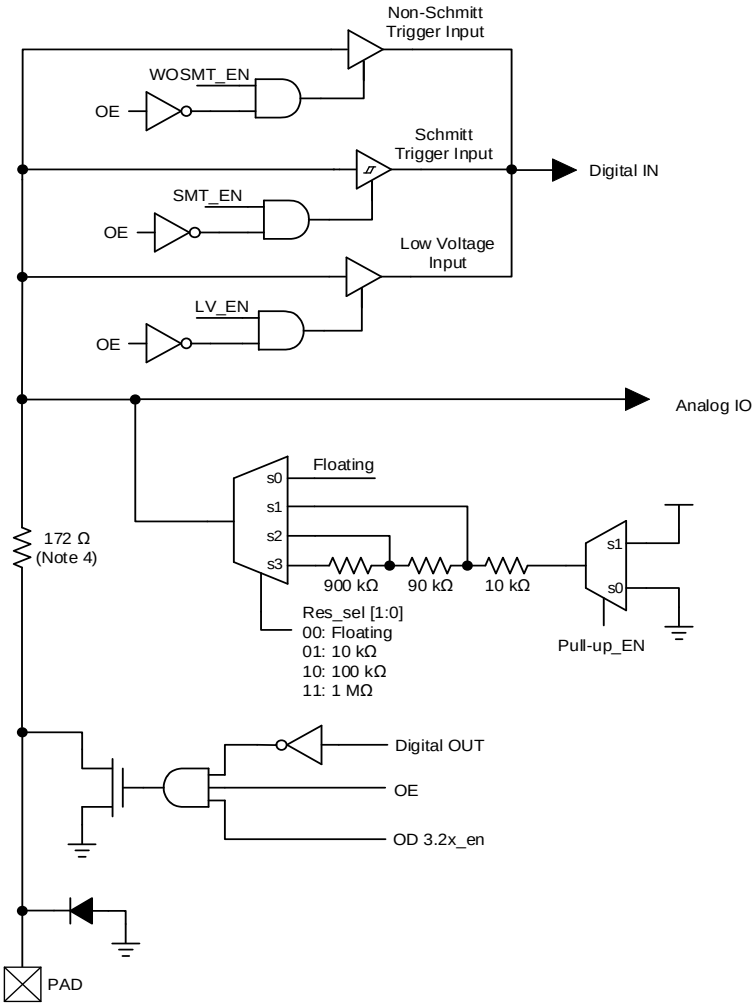


Figure 4: GPIO with I²C Mode IO Structure Diagram

5.7 MATRIX OE IO STRUCTURE

5.7.1 Matrix OE IO Structure (for GPIO2, GPIO3, GPIO7, GPIO8)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1
01: Digital In with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital In mode, lv_en = 1
11: analog IO mode

Output Mode [1:0]
00: Push-Pull 1x mode, pp1x_en = 1
01: Push-Pull 2x mode, pp2x_en = 1, pp1x_en = 1
10: NMOS 1x Open-Drain mode, od1x_en = 1
11: NMOS 2x Open-Drain mode, od2x_en = 1, od1x_en = 1

Note 1: Digital Out and OE are Matrix Output, Digital In is Matrix Input
Note 2: Can be varied over PVT, for reference only.

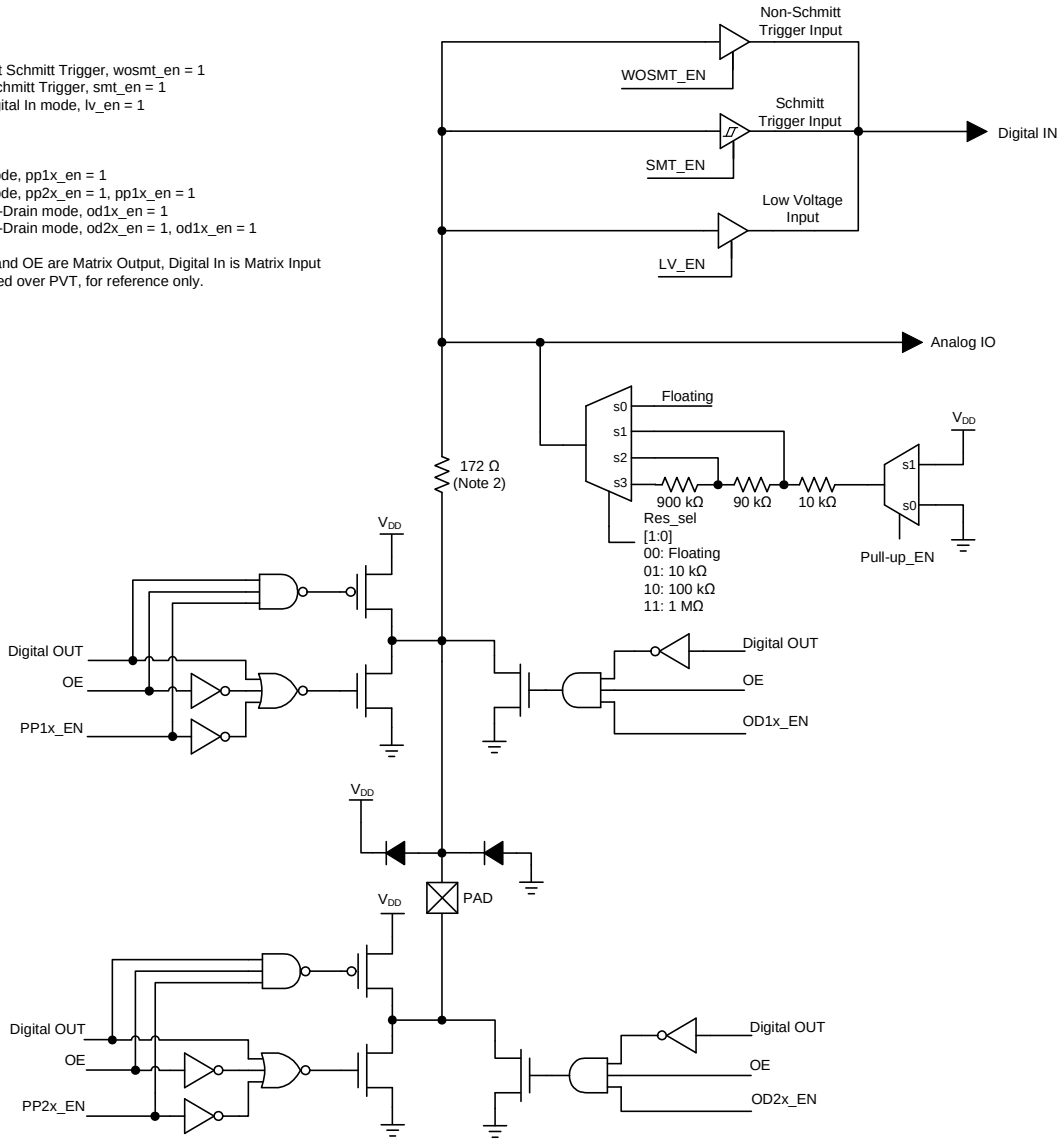


Figure 5: Matrix OE IO Structure Diagram

5.8 REGISTER OE IO STRUCTURE

5.8.1 Register OE IO Structure (for GPIO4, GPIO5, GPIO6)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1
01: Digital In with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital In mode, lv_en = 1
11: Analog IO mode

Output Mode [1:0]
00: Push-Pull 1x mode, pp1x_en = 1
01: Push-Pull 2x mode, pp2x_en = 1, pp1x_en = 1
10: NMOS 1x Open-Drain mode, od1x_en = 1
11: NMOS 2x Open-Drain mode, od2x_en = 1, od1x_en = 1

Note 1: Digital Out is Matrix Output, Digital In is Matrix Input. OE is register bit
Note 2: Can be varied over PVT, for reference only.

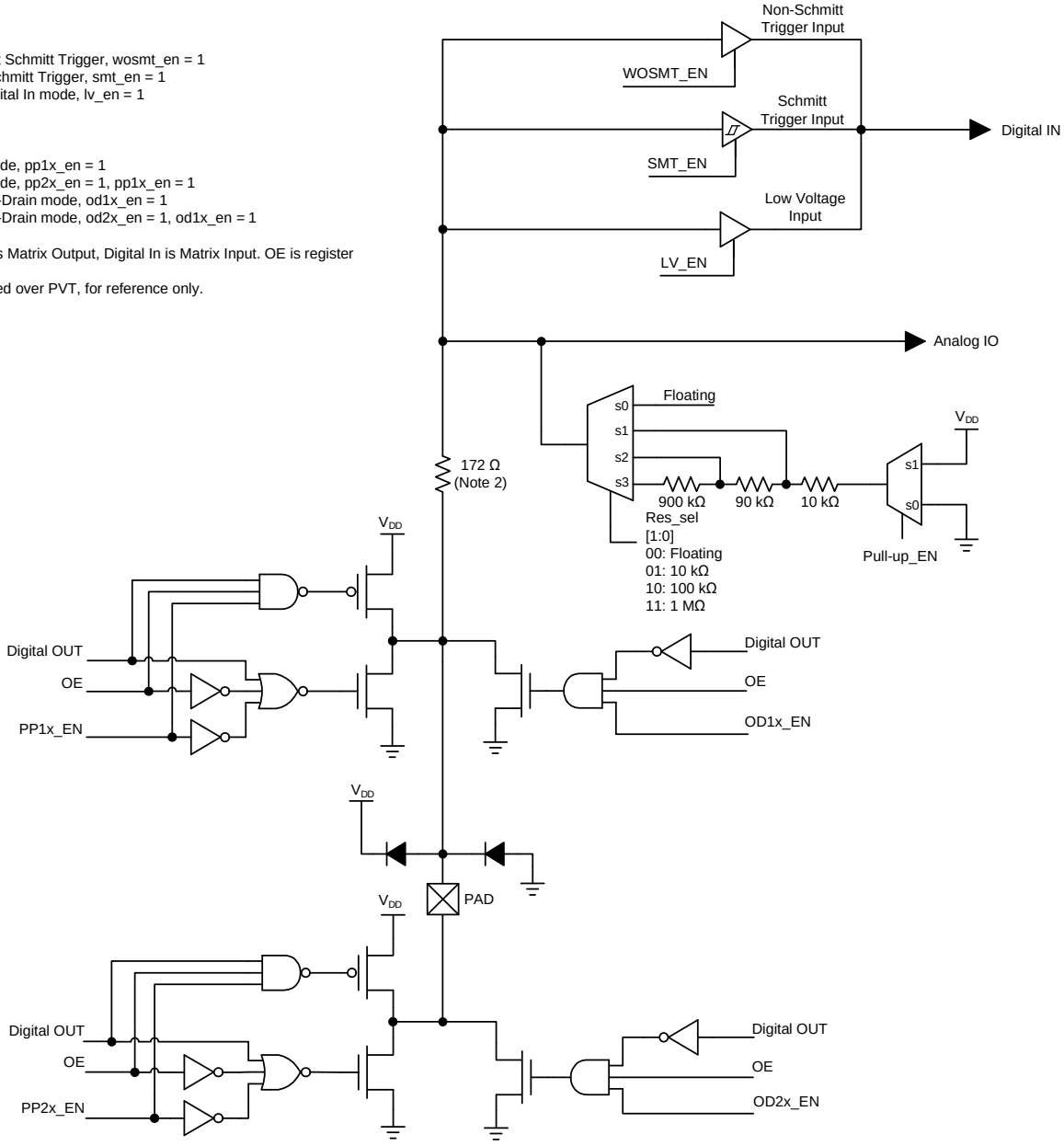


Figure 6: Register OE IO Structure Diagram

5.9 IO TYPICAL PERFORMANCE

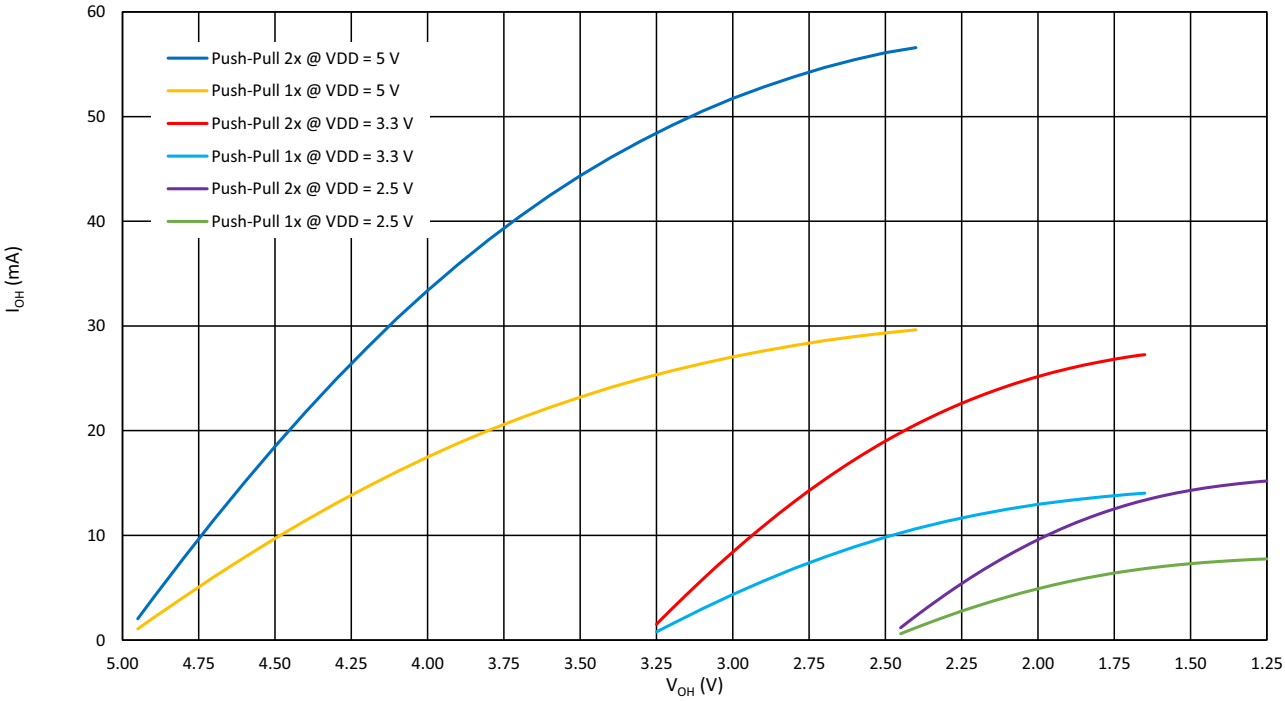


Figure 7: Typical High Level Output Current vs. High Level Output Voltage at T = 25 °C

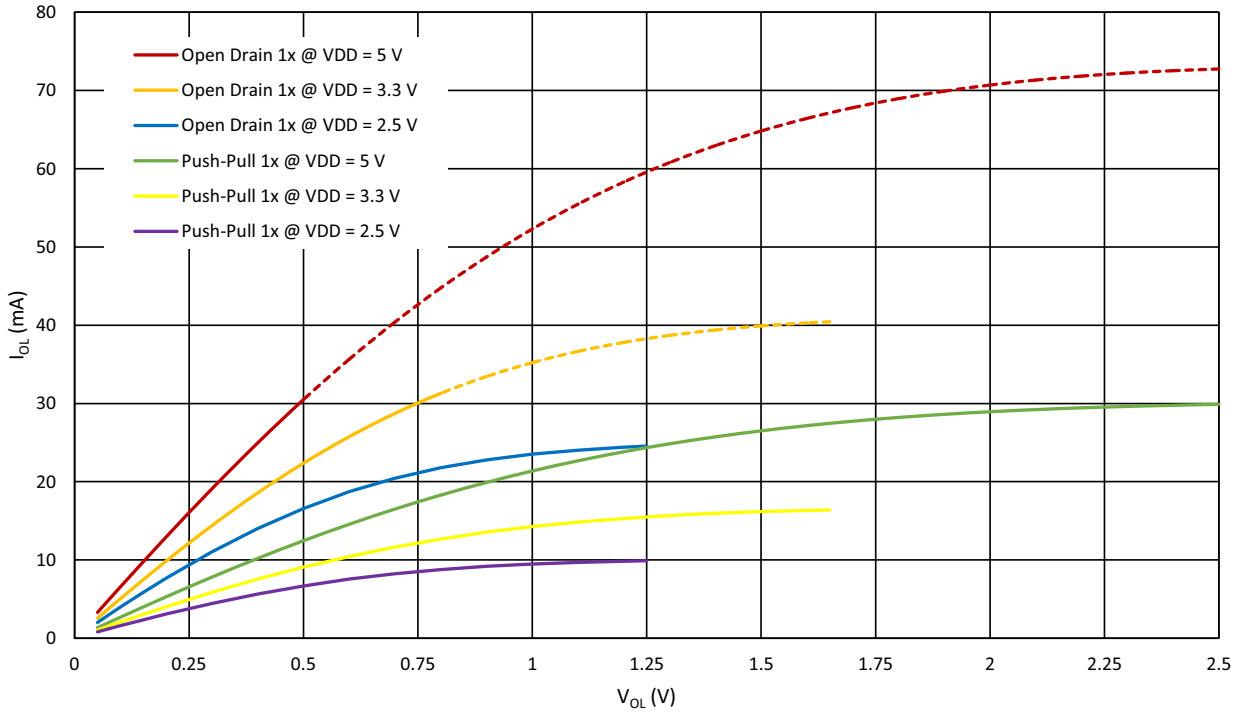


Figure 8: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C, Full Range

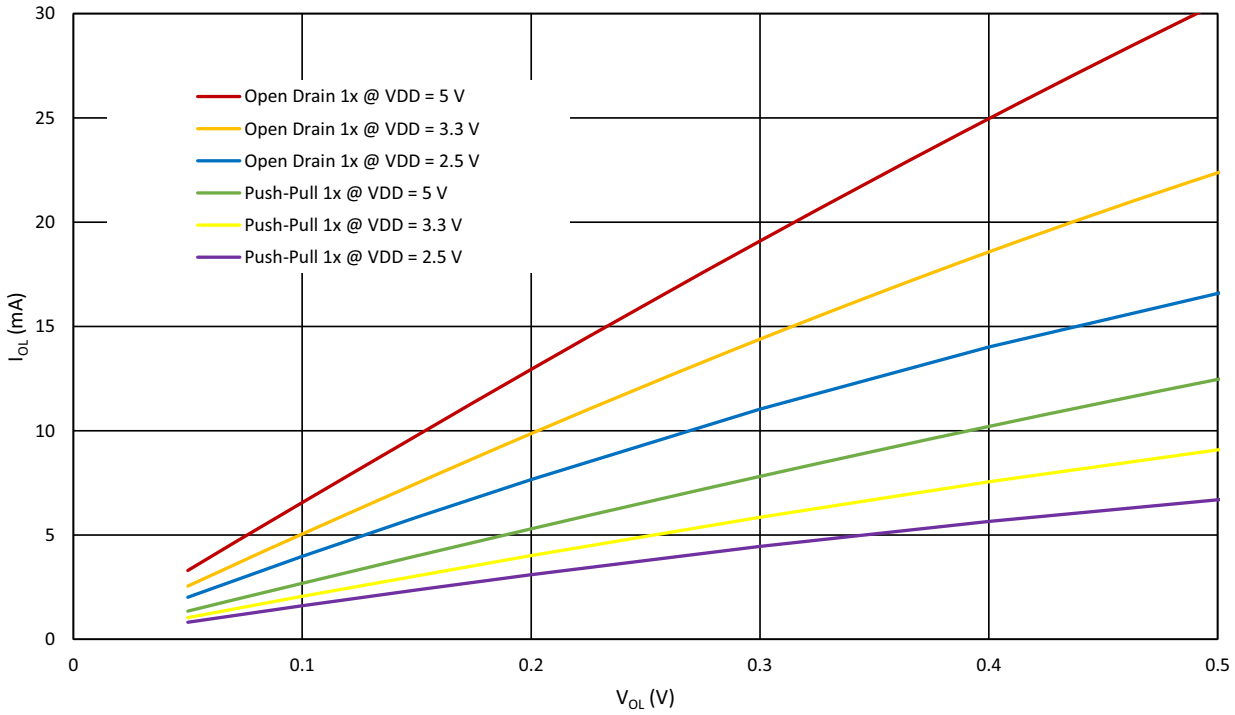


Figure 9: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C

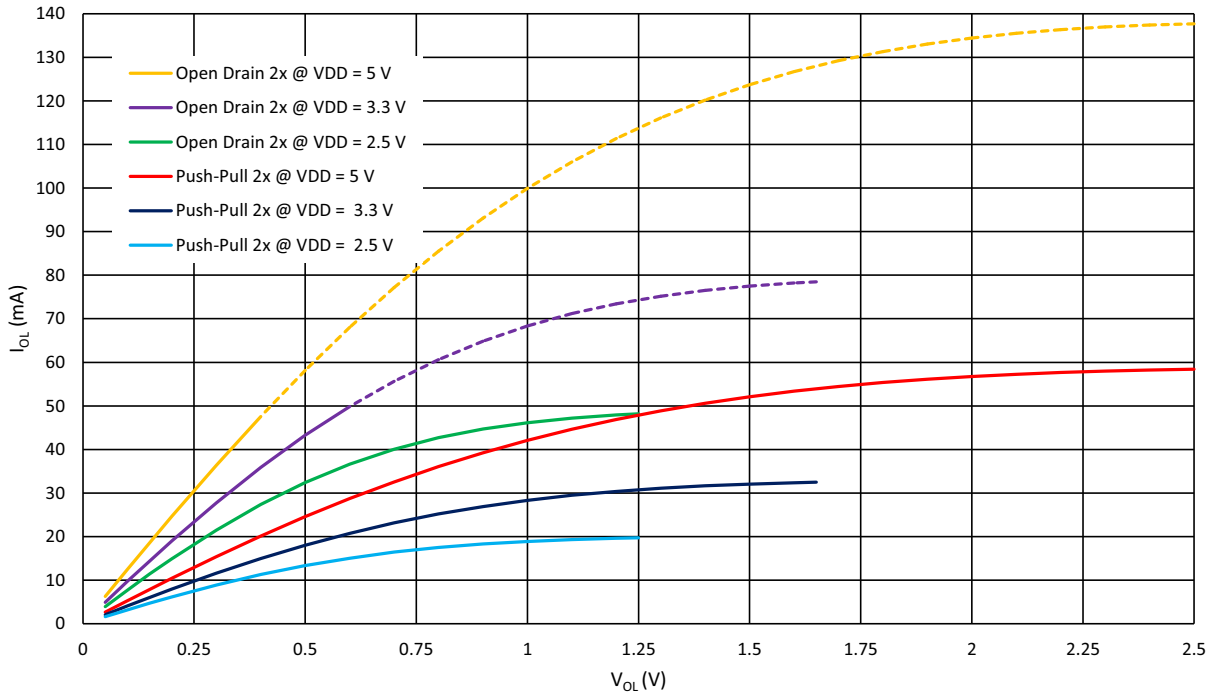


Figure 10: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C, Full Range

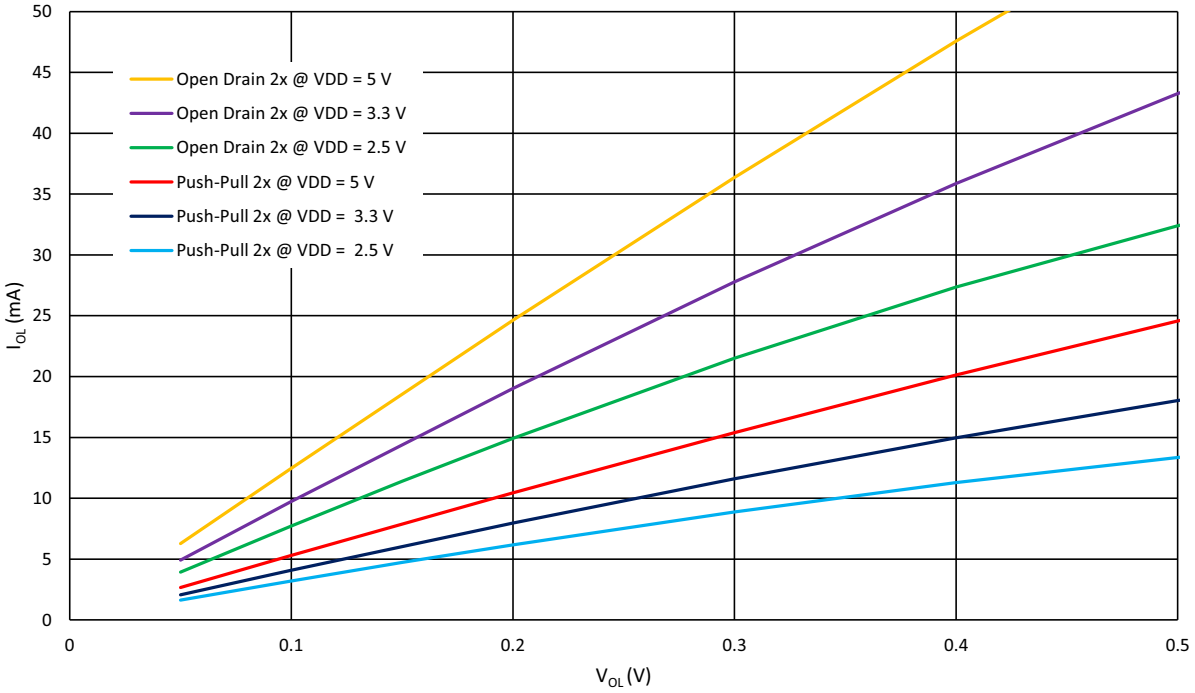


Figure 11: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C

6 Connection Matrix

The Connection Matrix in the SLG46811 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one time programmable (OTP) NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46811 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low”, based on the design that is created. Once the 1200 register bits within the SLG46811 are programmed a fully custom circuit will be created.

The Connection Matrix has 53 inputs and 72 outputs. Each of the 53 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 53 input lines.

For a complete list of the SLG46811’s register table, see Section 18.

Matrix Input Signal Functions	N
GND	0
LUT2_0/DFF0 output	1
LUT2_1/DFF1 output	2
LUT2_3/PGen output	3
⋮	⋮
POR	51
V_{DD}	52

Matrix Inputs / Matrix Outputs

N	0	1	2	…	71
Registers	registers [5:0]	registers [11:6]	registers [17:12]	…	registers [431:426]
Function	IN0 of LUT2_0 or Clock Input of DFF0	IN1 of LUT2_0 or Data Input of DFF0	IN0 of LUT2_1 or Clock Input of DFF1	…	Extended Pattern Generator nReset

Figure 12: Connection Matrix

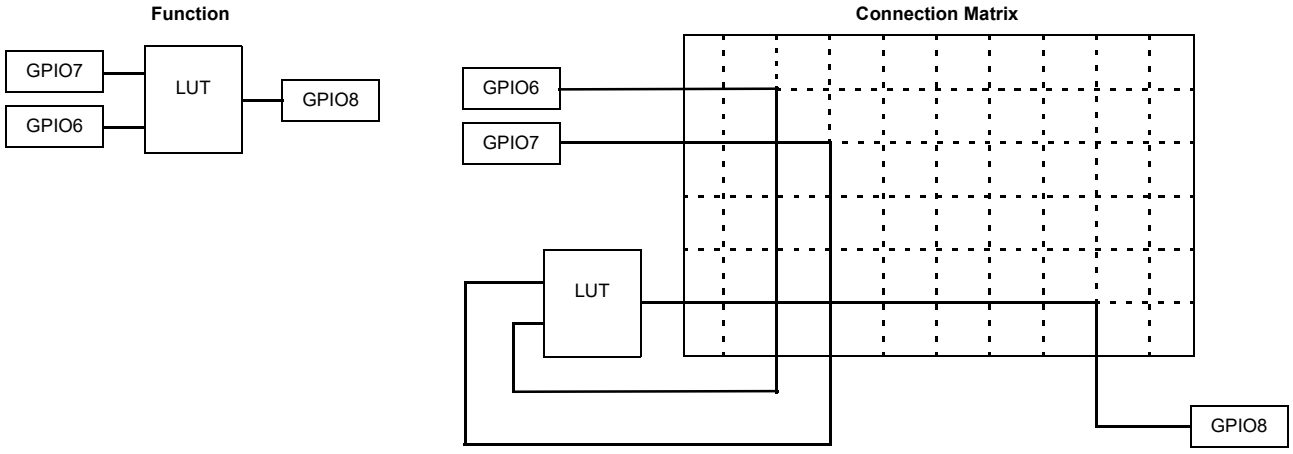


Figure 13: Connection Matrix Usage Example

6.1 MATRIX INPUT TABLE

Table 20: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	LUT2_0/DFF0 output	0	0	0	0	0	1
2	LUT2_1/DFF1 output	0	0	0	0	1	0
3	LUT2_3/PGen output	0	0	0	0	1	1
4	LUT3_0/DFF2 output	0	0	0	1	0	0
5	LUT3_1/DFF3 output	0	0	0	1	0	1
6	LUT3_2/DFF4 output	0	0	0	1	1	0
7	LUT3_3/DFF5 output	0	0	0	1	1	1
8	LUT3_4/DFF6 output/Shift_Reg0 output	0	0	1	0	0	0
9	LUT3_5/DFF7 output/Shift_Reg1 output	0	0	1	0	0	1
10	LUT3_6/DFF8 output/Shift_Reg2 output	0	0	1	0	1	0
11	LUT3_7/DFF9 output/Shift_Reg3 output	0	0	1	0	1	1
12	CNT0 output	0	0	1	1	0	0
13	MLT0_LUT3_8/DFF10_OUT	0	0	1	1	0	1
14	CNT1 output	0	0	1	1	1	0
15	MLT1_LUT3_9/DFF11_OUT	0	0	1	1	1	1
16	CNT2 output	0	1	0	0	0	0
17	MLT2_LUT3_10/DFF12_OUT	0	1	0	0	0	1
18	CNT3 output	0	1	0	0	1	0
19	MLT3_LUT3_11/DFF13_OUT	0	1	0	0	1	1
20	CNT4 output	0	1	0	1	0	0
21	MLT4_LUT3_12/DFF14_OUT	0	1	0	1	0	1
22	CNT5 output	0	1	0	1	1	0
23	MLT5_LUT3_13/DFF15_OUT	0	1	0	1	1	1
24	I^2C_virtual_0 Input, Extended Pattern Generator Output 0	0	1	1	0	0	0
25	I^2C_virtual_1 Input, Extended Pattern Generator Output 1	0	1	1	0	0	1
26	I^2C_virtual_2 Input, Extended Pattern Generator Output 2	0	1	1	0	1	0
27	I^2C_virtual_3 Input, Extended Pattern Generator Output 3	0	1	1	0	1	1
28	I^2C_virtual_4 Input, Extended Pattern Generator Output 4	0	1	1	1	0	0
29	I^2C_virtual_5 Input, Extended Pattern Generator Output 5	0	1	1	1	0	1
30	I^2C_virtual_6 Input, GPIO0 digital input, Extended Pattern Generator Output 6 or SCL	0	1	1	1	1	0
31	I^2C_virtual_7 Input, GPIO1 digital input, Extended Pattern Generator Output 7 or SDA	0	1	1	1	1	1
32	GPIO2 Digital Input or I^2C_virtual_8 Input	1	0	0	0	0	0

Table 20: Matrix Input Table (Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
33	GPIO3 Digital Input or I^2C_virtual_9 Input	1	0	0	0	0	1
34	GPIO4 Digital Input or I^2C_virtual_10 Input	1	0	0	0	1	0
35	GPIO5 Digital Input or I^2C_virtual_11 Input	1	0	0	0	1	1
36	GPIO6 Digital Input or I^2C_virtual_12 Input	1	0	0	1	0	0
37	GPIO7 Digital Input or I^2C_virtual_13 Input	1	0	0	1	0	1
38	GPIO8 Digital Input or I^2C_virtual_14 Input	1	0	0	1	1	0
39	LUT4_0/DFF16 output	1	0	0	1	1	1
40	GPI Digital Input	1	0	1	0	0	0
41	Programmable Delay Edge Detect Output	1	0	1	0	0	1
42	Edge Detect Filter Output	1	0	1	0	1	0
43	Oscillator0 output 0	1	0	1	0	1	1
44	Oscillator1 output	1	0	1	1	0	0
45	MS ACMP Output 0	1	0	1	1	0	1
46	MS ACMP Output 1	1	0	1	1	1	0
47	MS ACMP Output 2	1	0	1	1	1	1
48	MS ACMP Output 3	1	1	0	0	0	0
49	Oscillator0 output 1	1	1	0	0	0	1
50	MS ASMP Data Ready Signal	1	1	0	0	1	0
51	POR	1	1	0	0	1	1
52	V_{DD}	1	1	1	0	0	0

6.2 MATRIX OUTPUT TABLE

Table 21: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	IN0 of LUT2_0 or Clock Input of DFF0	0
[11:6]	IN1 of LUT2_0 or Data Input of DFF0	1
[17:12]	IN0 of LUT2_1 or Clock Input of DFF1	2
[23:18]	IN1 of LUT2_1 or Data Input of DFF1	3
[29:24]	IN0 of LUT2_2 or Clock Input of PGen	4
[35:30]	IN1 of LUT2_2 or nRST of PGen	5
[41:36]	IN0 of LUT3_0 or CLK Input of DFF2	6
[47:42]	IN1 of LUT3_0 or Data of DFF2	7
[53:48]	IN2 of LUT3_0 or nRST (nSET) of DFF2	8
[59:54]	IN0 of LUT3_1 or CLK Input of DFF3	9
[65:60]	IN1 of LUT3_1 or Data of DFF3	10
[71:66]	IN2 of LUT3_1 or nRST (nSET) of DFF3	11
[77:72]	IN0 of LUT3_2 or CLK Input of DFF4	12
[83:78]	IN1 of LUT3_2 or Data of DFF4	13
[89:84]	IN2 of LUT3_2 or nRST (nSET) of DFF4	14
[95:90]	IN0 of LUT3_3 or CLK Input of DFF5	15
[101:96]	IN1 of LUT3_3 or Data of DFF5	16
[107:102]	IN2 of LUT3_3 or nRST (nSET) of DFF5	17
[113:108]	IN0 of LUT3_4 or CLK Input of DFF6 or Clock Input of Shift_Reg0	18
[119:114]	IN1 of LUT3_4 or Data of DFF6 or Data Input of Shift_Reg0	19
[125:120]	IN2 of LUT3_4 or nRST (nSET) of DFF6 or nRST (nSET) of Shift_Reg0	20
[131:126]	IN0 of LUT3_5 or CLK Input of DFF7 or Clock Input of Shift_Reg1	21
[137:132]	IN1 of LUT3_5 or Data of DFF7 or Data Input of Shift_Reg1	22
[143:138]	IN2 of LUT3_5 or nRST (nSET) of DFF7 or nRST (nSET) of Shift_Reg1	23
[149:144]	IN0 of LUT3_6 or CLK Input of DFF8 or Clock Input of Shift_Reg2	24
[155:150]	IN1 of LUT3_6 or Data of DFF8 or Data Input of Shift_Reg2	25
[161:156]	IN2 of LUT3_6 or nRST (nSET) of DFF8 or nRST (nSET) of Shift_Reg2	26
[167:162]	IN0 of LUT3_7 or CLK Input of DFF9 or Clock Input of Shift_Reg3	27
[173:168]	IN1 of LUT3_7 or Data of DFF9 or Data Input of Shift_Reg3	28
[179:174]	IN2 of LUT3_7 or nRST (nSET) of DFF9 or nRST (nSET) of Shift_Reg3	29
[185:180]	IN0 of LUT3_8 or CLK Input of DFF10 Delay0 Input (or Counter0 nRST Input) Up input of FSM	30
[191:186]	IN1 of LUT3_8 or nRST (nSET) of DFF10 Delay0 Input (or Counter0 nRST Input) or DLY/CNT/FSM External CLK input	31
[197:192]	IN2 of LUT3_8 or Data of DFF10 Delay0 Input (or Counter0 nRST Input) or FSM Reset/Set input	32

Table 21: Matrix Output Table (Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[203:198]	IN0 of LUT3_9 or CLK Input of DFF11 Delay1 Input (or Counter1 nRST Input)	33
[209:204]	IN1 of LUT3_9 or nRST (nSET) of DFF11 Delay1 Input (or Counter1 nRST Input)	34
[215:210]	IN2 of LUT3_9 or Data of DFF11 Delay1 Input (or Counter1 nRST Input)	35
[221:216]	IN0 of LUT3_10 or CLK Input of DFF12 Delay2 Input (or Counter1 nRST Input)	36
[227:222]	IN1 of LUT3_10 or nRST (nSET) of DFF12 Delay2 Input (or Counter1 nRST Input)	37
[233:228]	IN2 of LUT3_10 or Data of DFF12 Delay2 Input (or Counter2 nRST Input)	38
[239:234]	IN0 of LUT3_11 or CLK Input of DFF13 Delay3 Input (or Counter3 nRST Input)	39
[245:240]	IN1 of LUT3_11 or nRST (nSET) of DFF13 Delay3 Input (or Counter3 nRST Input)	40
[251:246]	IN2 of LUT3_11 or Data of DFF13 Delay3 Input (or Counter3 nRST Input)	41
[257:252]	IN0 of LUT3_12 or CLK Input of DFF14 Delay4 Input (or Counter4 nRST Input)	42
[263:258]	IN1 of LUT3_12 or nRST (nSET) of DFF14 Delay4 Input (or Counter4 nRST Input)	43
[269:264]	IN2 of LUT3_12 or Data of DFF14 Delay4 Input (or Counter4 nRST Input)	44
[275:270]	IN0 of LUT3_13 or CLK Input of DFF15 Delay5 Input (or Counter5 nRST Input)	45
[281:276]	IN1 of LUT3_13 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)	46
[287:282]	IN2 of LUT3_13 or Data of DFF15 Delay5 Input (or Counter5 nRST Input)	47
[293:288]	IN0 of LUT4_0 or CLK Input of DFF16	48
[299:294]	IN1 of LUT4_0 or Data of DFF16	49
[305:300]	IN2 of LUT4_0 or nRST (nSET) of DFF16	50
[311:306]	IN3 of LUT4_0	51
[317:312]	Programmable Delay/Edge Detect Input	52
[323:318]	Filter/Edge Detect Input	53
[329:324]	GPIO0 Digital Output	54
[335:330]	GPIO1 Digital Output	55
[341:336]	GPIO2, Digital Output	56
[347:342]	GPIO2, Digital Output OE	57
[353:348]	GPIO3, Digital Output	58
[359:354]	GPIO3, Digital Output OE	59
[365:360]	GPIO4 Digital Output	60
[371:366]	GPIO5 Digital Output	61
[377:372]	GPIO6 Digital Output	62
[383:378]	GPIO7 Digital Output	63
[389:384]	GPIO7 Digital Output OE	64
[395:390]	GPIO8 Digital Output	65
[401:396]	GPIO8 Digital Output OE	66
[407:402]	MS ACMP Enable Input	67
[413:408]	Reset of MS ACMP DFFs	68
[419:414]	OSC Enable	69

Table 21: Matrix Output Table (Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[425:420]	Extended Pattern Generator Clock	70
[431:426]	Extended Pattern Generator nReset	71
Note 1 For each Address, the two most significant bits are unused.		

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Fifteen of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated to the inputs of other macrocells through Connection Matrix. The I^2C address for reading and writing these register values is byte 0x39, 0x3A<6:0>.

An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Connection Matrix Virtual Inputs are shared with input function of GPIO and Pattern Generator output.

If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). The I^2C disable/enable registers [1078:1072] and [1184] select whether the Connection Matrix input comes from the Pin input or from the I^2C virtual input. All I^2C virtual inputs with shared functions are listed below:

- Select Pattern Generator 0 or Virtual Input 0
- Select Pattern Generator 1 or Virtual Input 1
- Select Pattern Generator 2 or Virtual Input 2
- Select Pattern Generator 3 or Virtual Input 3
- Select Pattern Generator 4 or Virtual Input 4
- Select Pattern Generator 5 or Virtual Input 5
- Select Pattern Generator 6 or Virtual Input 6 or GPI (GPIO0)
- Select Pattern Generator 7 or Virtual Input 7 or GPI (GPIO1)
- Select Virtual Input 8 or GPI (GPIO2)
- Select Virtual Input 9 or GPI (GPIO3)
- Select Virtual Input 10 or GPI (GPIO4)
- Select Virtual Input 11 or GPI (GPIO5)
- Select Virtual Input 12 or GPI (GPIO6)
- Select Virtual Input 13 or GPI (GPIO7)
- Select Virtual Input 14 or GPI (GPIO8)

See Table for Connection Matrix Virtual Inputs.

Table 22: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
24	Extended Pattern Generator 0 or I^2C_virtual_0 Input	[456]
25	Extended Pattern Generator 1 or I^2C_virtual_1 Input	[457]
26	Extended Pattern Generator 2 or I^2C_virtual_2 Input	[458]

Table 22: Connection Matrix Virtual Inputs (Continued)

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
27	Extended Pattern Generator 3 or I²C_virtual_3 Input	[459]
28	Extended Pattern Generator 4 or I²C_virtual_4 Input	[460]
29	Extended Pattern Generator 5 or I²C_virtual_5 Input	[461]
30	Extended Pattern Generator 6 or I²C_virtual_6 Input or GPI (GPIO0)	[462]
31	Extended Pattern Generator 7 or I²C_virtual_7 Input or GPI (GPIO1)	[463]
32	GPI (GPIO2) or I²C_virtual_8 Input	[464]
33	GPI (GPIO3) or I²C_virtual_9 Input	[465]
34	GPI (GPIO4) or I²C_virtual_10 Input	[466]
35	GPI (GPIO5) or I²C_virtual_11 Input	[467]
36	GPI (GPIO6) or I²C_virtual_12 Input	[468]
37	GPI (GPIO7) or I²C_virtual_13 Input	[469]
38	GPI (GPIO8) or I²C_virtual_14 Input	[470]

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I²C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I²C addresses for reading these register values are bytes 0x36 (053) to 0x3C (060) (except for registers [470:456]). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at registers [470:456]).

7 Combination Function Macrocells

The SLG46811 has 12 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Two macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- Four macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- Four macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input or as Shift Register
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input

Inputs/Outputs for the 12 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There is one macrocell that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

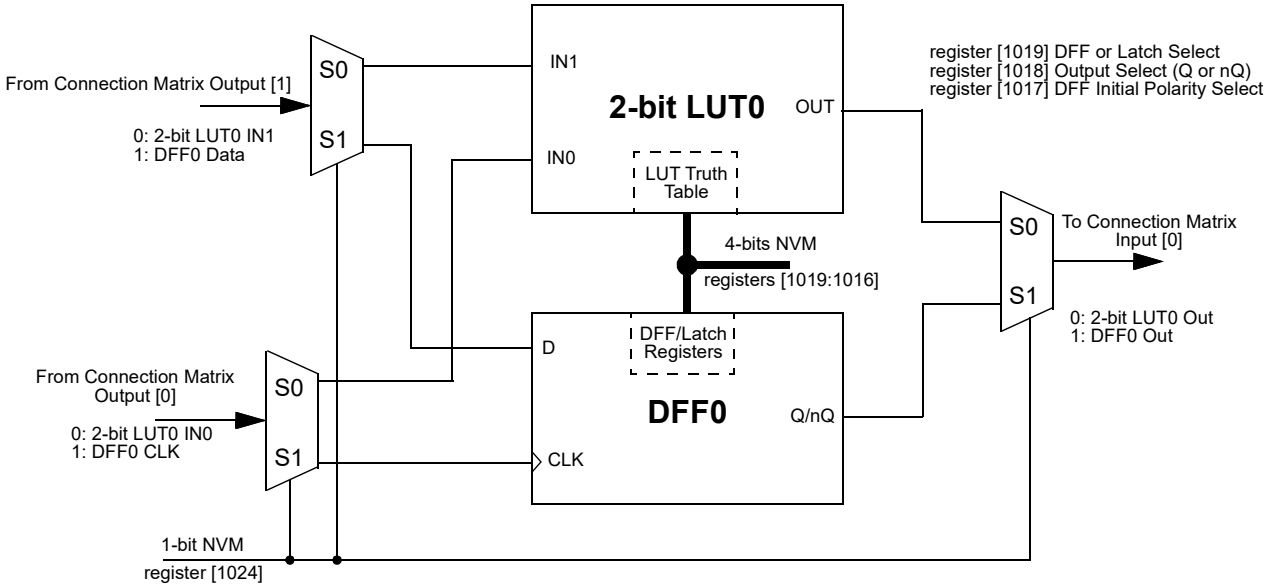


Figure 14: 2-bit LUT0 or DFF0

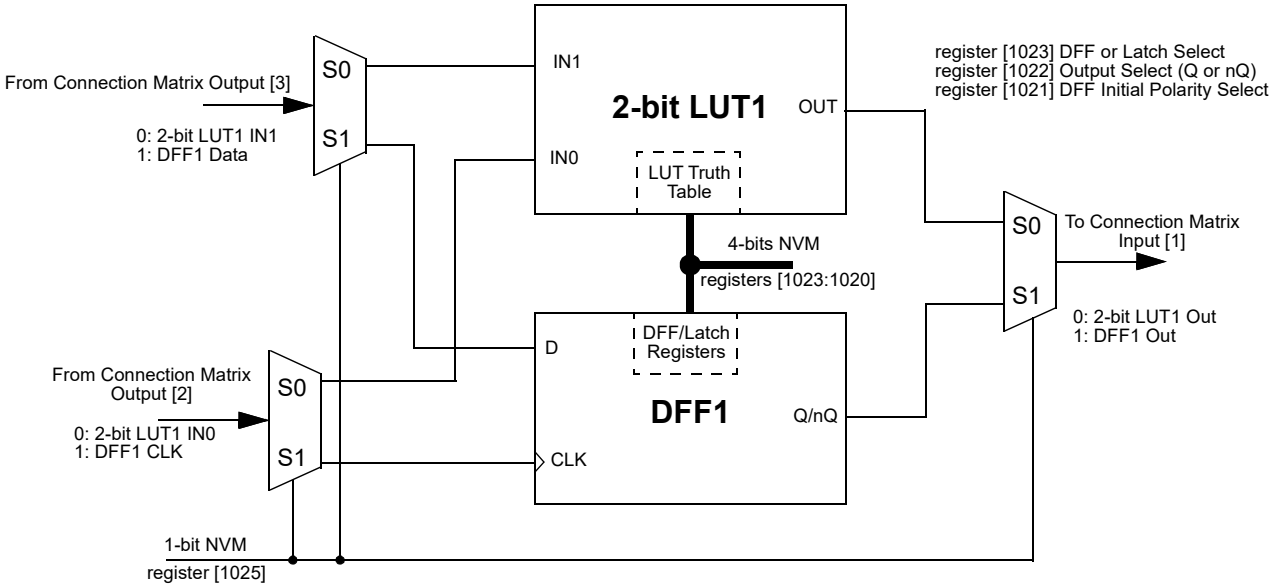


Figure 15: 2-bit LUT1 or DFF1

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by register [1019:1016]

2-Bit LUT1 is defined by register [1023:1020]

Table 23: 2-bit LUT2_0 to 2-bit LUT2_1 Truth Table

IN1	IN0	OUT LUT0	OUT LUT1	
0	0	Register [1016]	Register [1020]	LSB
0	1	Register [1017]	Register [1021]	
1	0	Register [1018]	Register [1022]	
1	1	Register [1019]	Register [1023]	MSB

Table 24 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 24: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.2 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG46811 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high level reset (RST) and a low level reset (nRST) options available which are selected by register [1027]. When operating as a Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

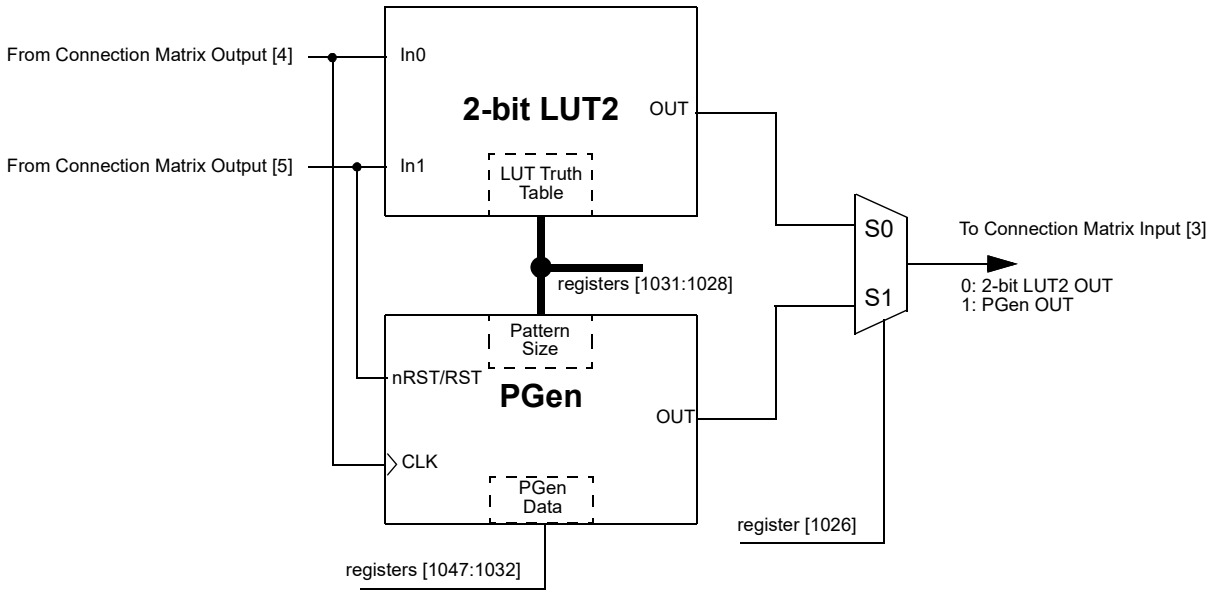


Figure 16: 2-bit LUT2 or PGen

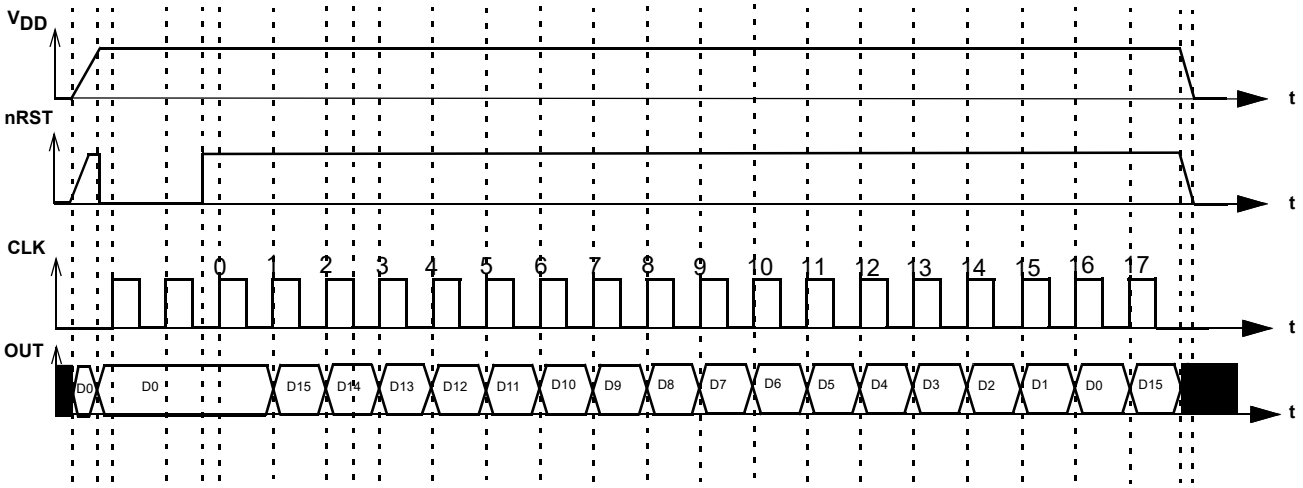


Figure 17: PGen Timing Diagram

Table 25: 2-bit LUT2_2 Truth Table

IN1	IN0	OUT	
0	0	register [1028]	LSB
0	1	register [1029]	
1	0	register [1030]	
1	1	register [1031]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT2_2 is defined by registers [1031:1028]

Table 26 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 26: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS OR SHIFT REGISTER MACROCELLS

There are four macrocells that can serve as 3-bit LUT or as DFF/LATCH or as Shift Register. It is also possible to define the active level (Q or nQ) for the macrocell's output by registers [958], [974], [990], [1006]. DFF/Shift Register or LUT are selected by registers [951:948]. When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

When used to implement Shift Register, the three input signals from the connection matrix go to the data (D_IN), clock (CLK), and Set/Reset (nSET/nRST) inputs for the Shift Register, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of Shift Register macrocell which is selected by registers [955], [971], [987], [1003]. The input data (D_IN) writes into LSB. The Shift Register length (up to 8 bits/memory cells) is selected by registers [954:952], registers [970:968], registers [986:984], and registers [1002:1000]. Shift register length = 1 (corresponding registers = 0) means that DFF/LATCH function is selected. Please note that D and CLK inputs of the Shift Register should remain unchanged while the I^2C master is reading data from the Shift Register. Otherwise, the I^2C master can read the wrong data. Signals at D and CLK inputs of the Shift Register will be ignored while I^2C master is writing a new data to the Shift Register macrocell. Also, note that the reset input of the Shift Register has higher priority to the Shift Register than the I^2C write routine.

When used to implement D Flip-Flop/LATCH function, the three input signals from the connection matrix go to the data (D_IN), clock (CLK), and Set/Reset (nSET/nRST) inputs for the Flip-Flop/LATCH, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input (nSET/nRST_sel which is selected by registers [956], [972], [988], [1004]) of DFF/LATCH macrocell. LATCH or DFF configuration is selected by registers [959], [975], [991], [1007].

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

Special care must be taken when writing new data to bytes 78h, 7Ah, 7Ch, 7Eh via I^2C. If LUT/DFF/LATCH/Shift_Register macrocells configured as DFF or LATCH, writing new data to LSB of bytes 78h, 7Ah, 7Ch, 7Eh can change the current state of DFF (LATCH).

It's possible to read/write the Shift Register content via I^2C (bytes 78h, 7Ah, 7Ch, 7Eh). Note that CLK signal of the Shift Register should be low when getting access to the Shift Register macrocell via I^2C.

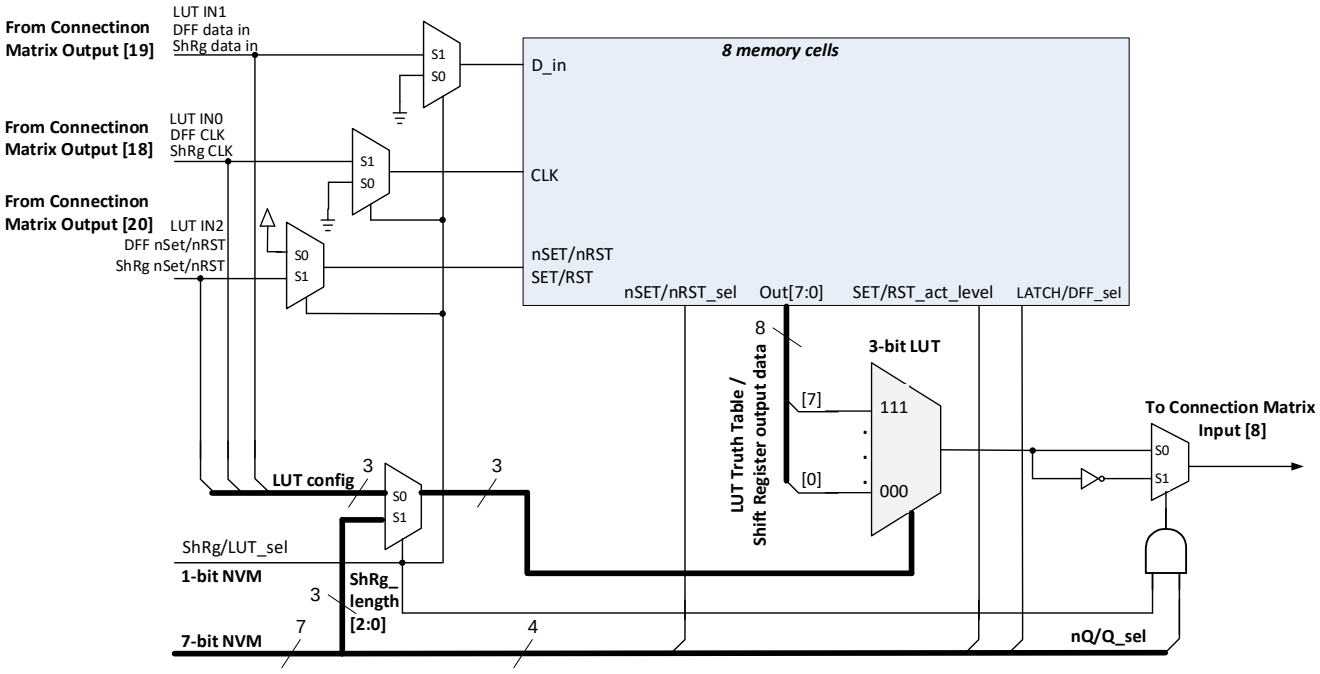


Figure 18: 3-bit LUT4 or DFF6 or Shift Register 0

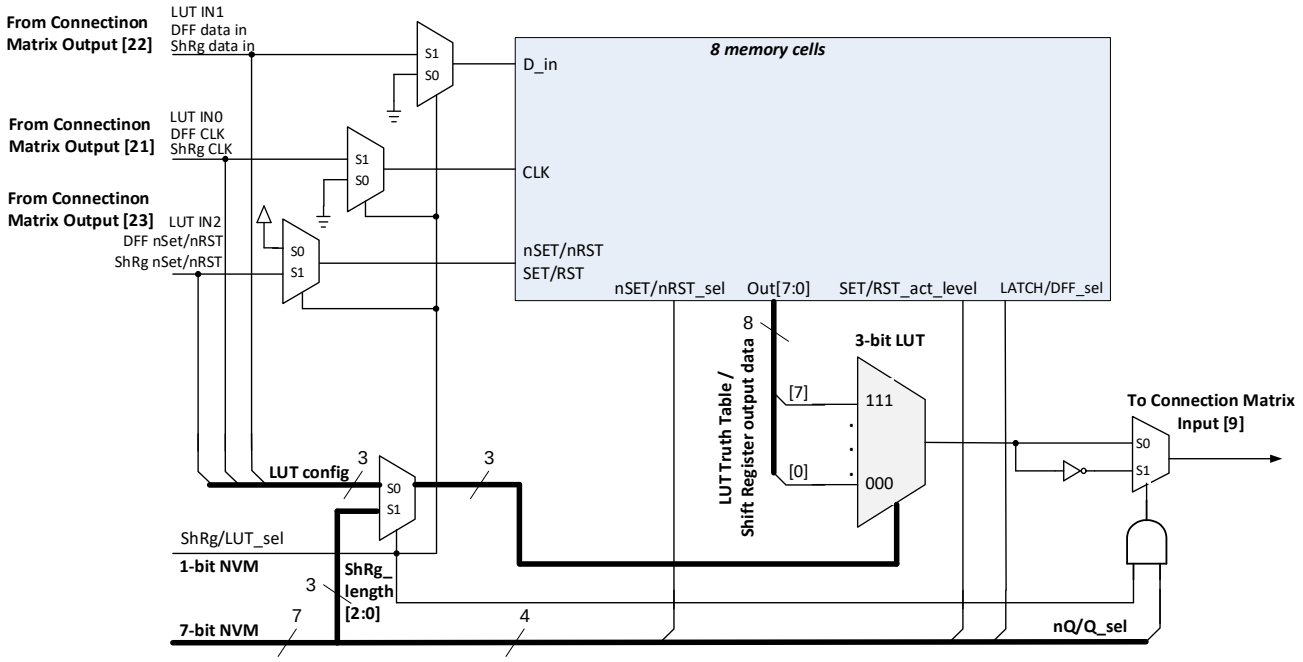


Figure 19: 3-bit LUT5 or DFF7 or Shift Register 1

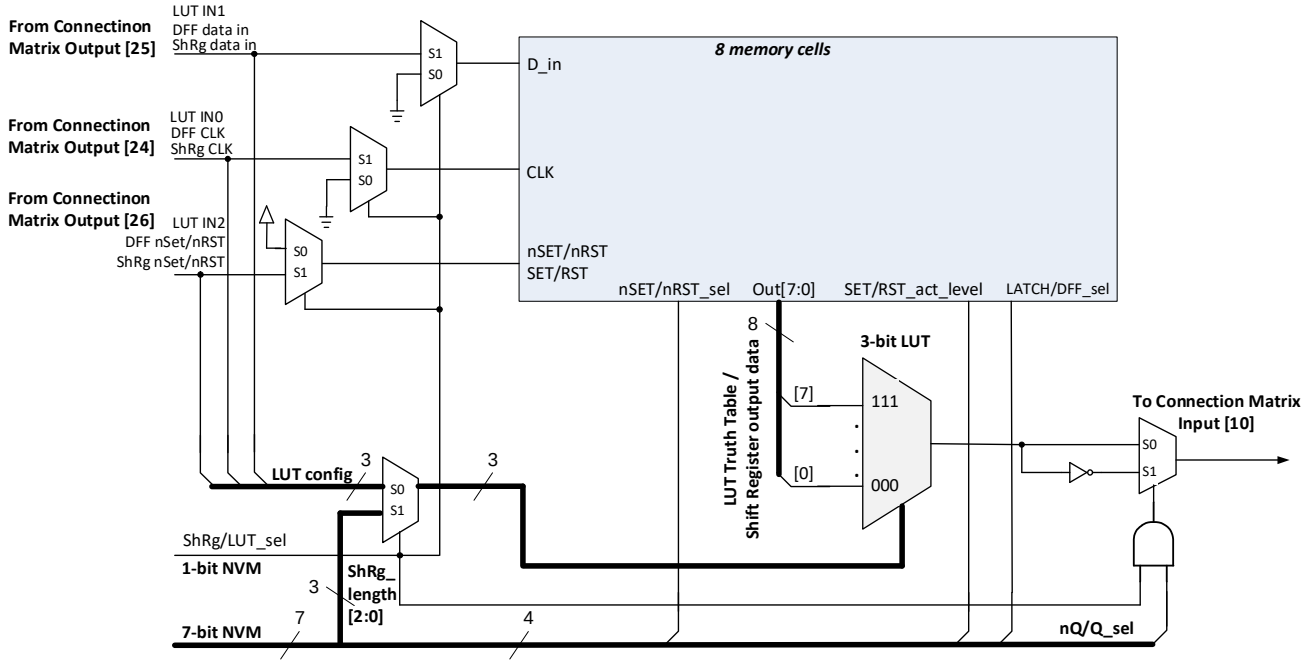


Figure 20: 3-bit LUT6 or DFF8 or Shift Register 2

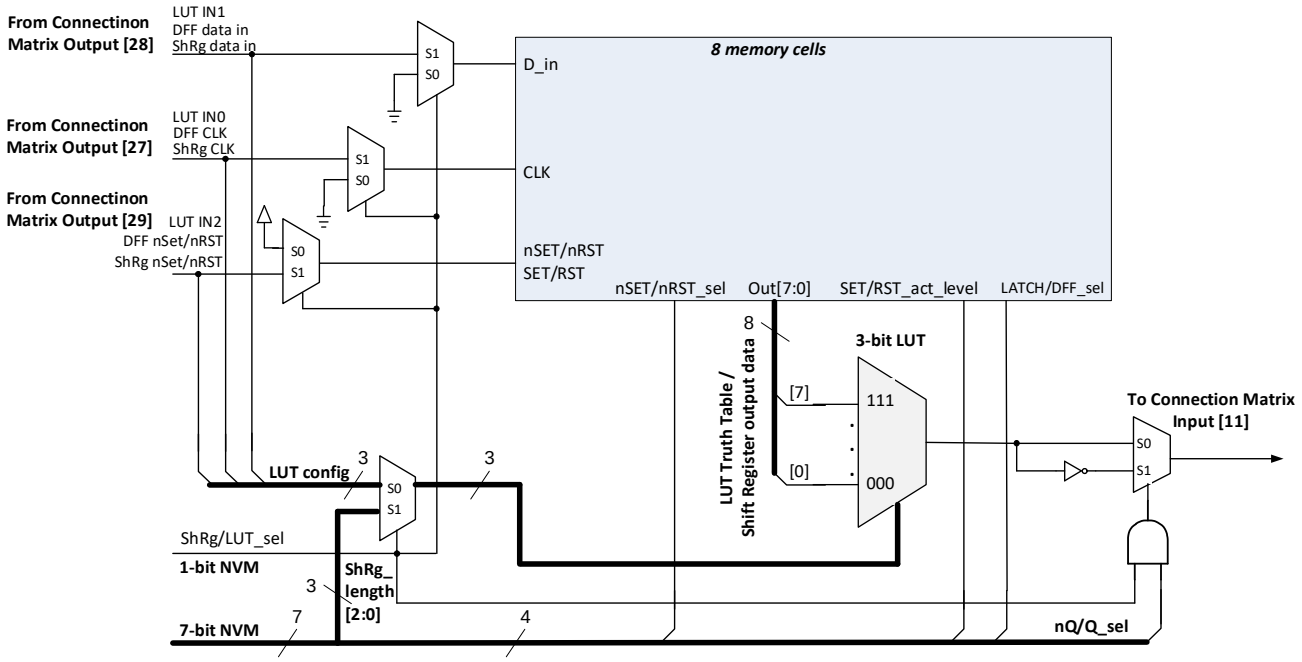
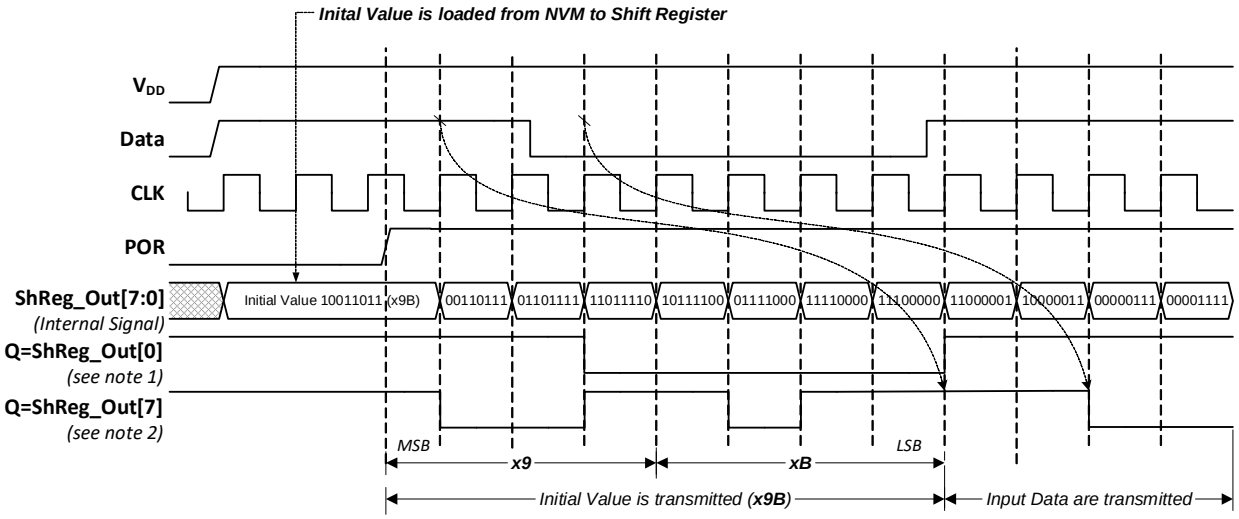
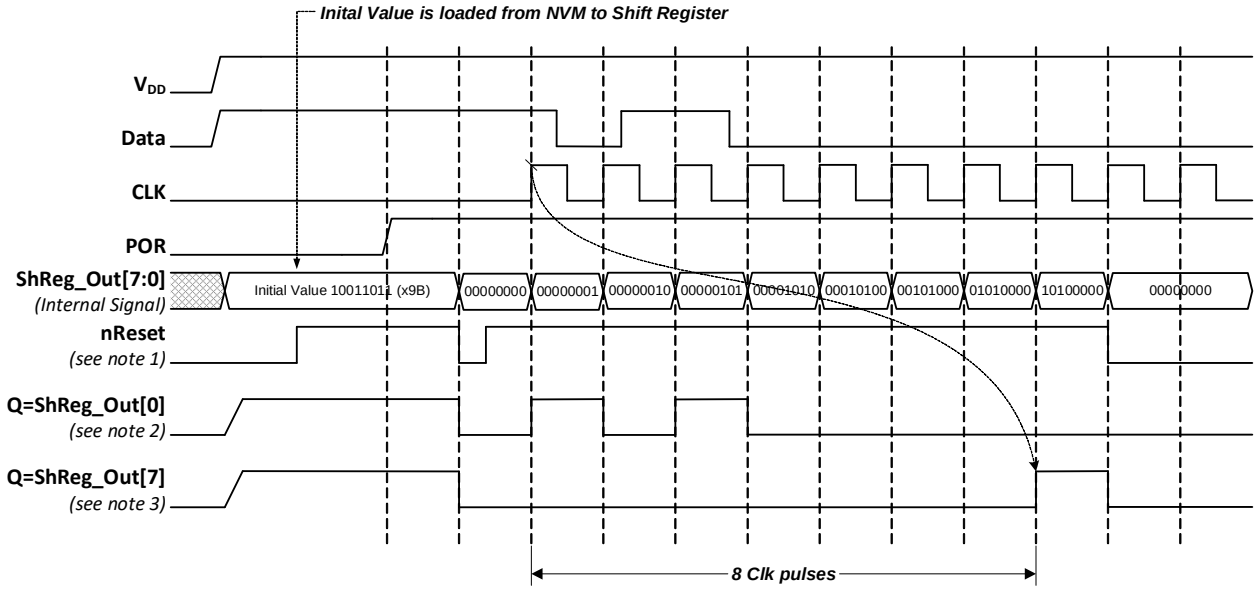


Figure 21: 3-bit LUT7 or DFF9 or Shift Register 3



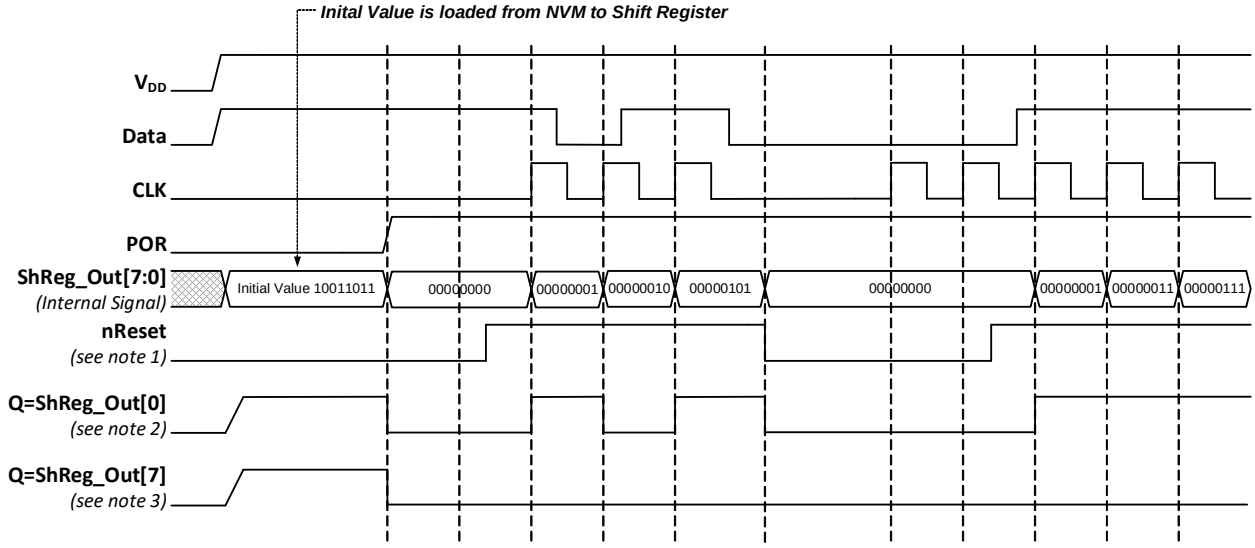
Note1 *:Macrocell is configured as DFF*
Note2 *: Macrocell is configured as 8-bit Shift Register*

Figure 22: DFF6 to DFF9 or Shift Register 0 to Shift Register 3 Operation



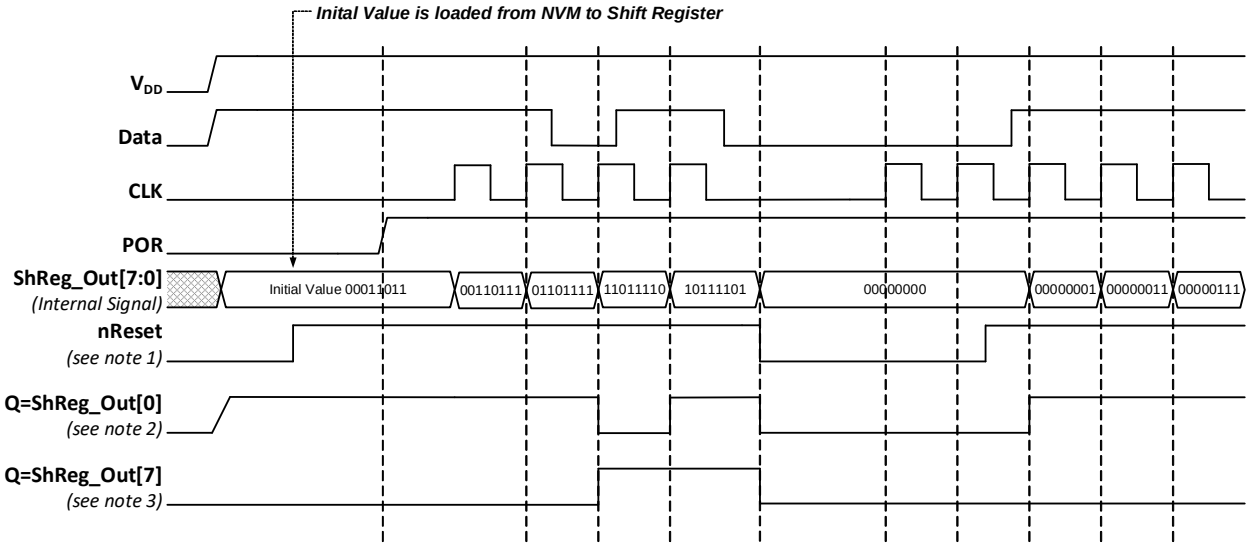
Note1 *: DFF Setting "Initial Value: 1"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 23: DFF6 to DFF9 or Shift Register 0 to Shift Register 3 Operation, nReset Option, DFF Initial Value: 1



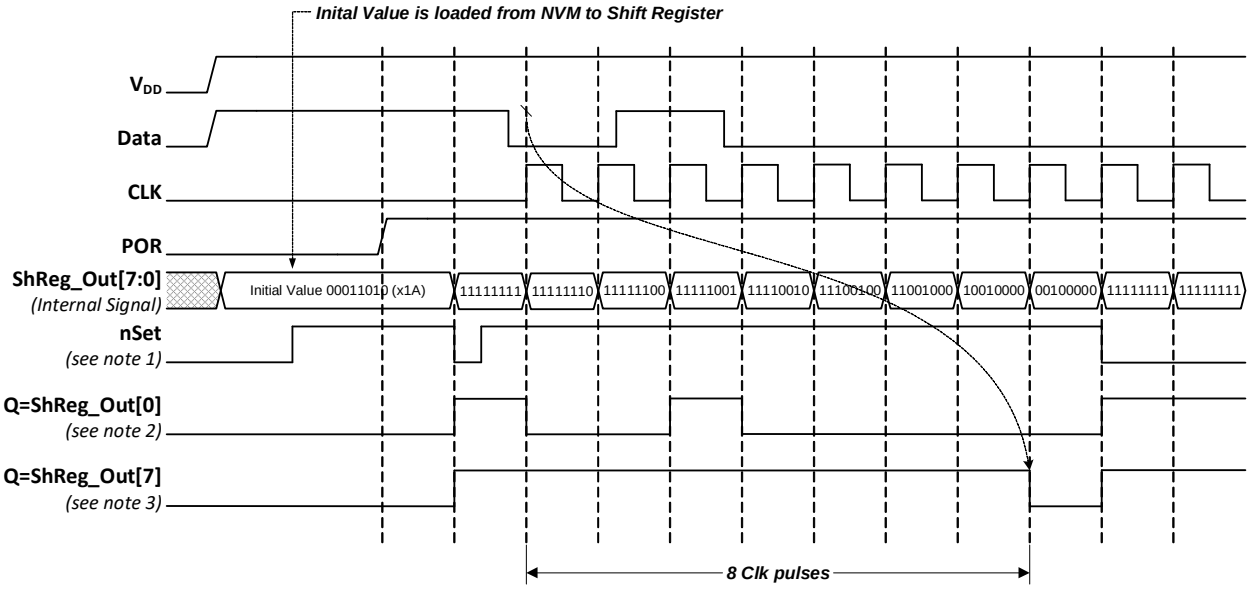
Note1 *: DFF Setting "Initial Value: 1"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 24: DFF6 to DFF9 or Shift Register 0 to Shift Register 3 Operation, nReset Option, DFF Initial Value: 1, Case 1



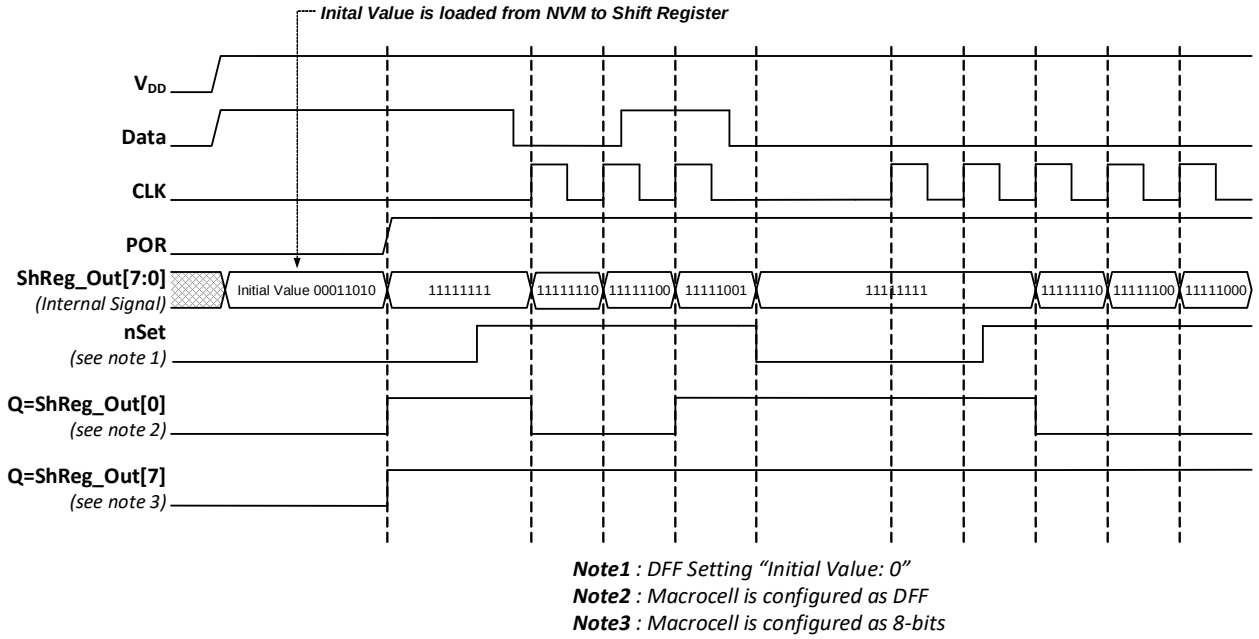
Note1 *: DFF Setting "Initial Value: 1"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 25: DFF6 to DFF9 or Shift Register 0 to Shift Register 3 Operation, nReset Option, DFF Initial Value: 1, Case 2



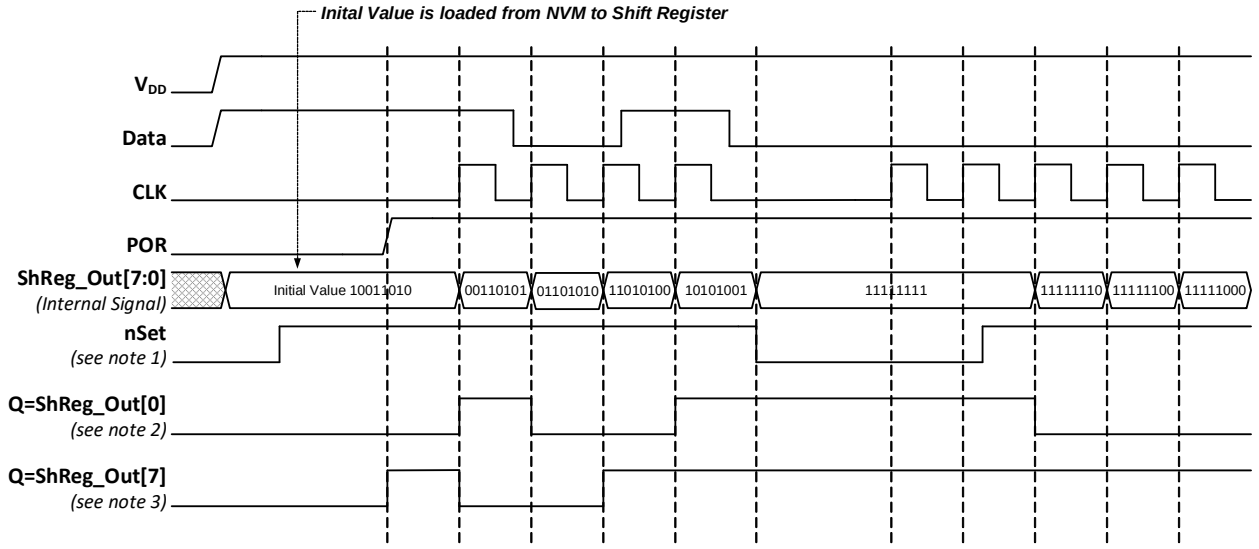
Note1 *: DFF Setting "Initial Value: 0"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 26: DFF6 to DFF9 or Shift Register 0 to Shift Register 3 Operation, nSet Option, DFF Initial Value: 0



Note1 *: DFF Setting "Initial Value: 0"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 27: DFF6 to DFF9 or Shift Register 0 to Shift Register 3 Operation, nSet Option, DFF Initial Value: 0, Case 1



Note1 *: DFF Setting "Initial Value: 0"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 28: DFF6 to DFF9 or Shift Register 0 to Shift Register 3 Operation, nSet Option, DFF Initial Value: 0, Case 2

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-Bit LUT3_0 is defined by registers [895:888]

3-Bit LUT3_1 is defined by registers [903:896]

3-Bit LUT3_2 is defined by registers [911:904]

3-Bit LUT3_3 is defined by registers [919:912]

3-Bit LUT3_4 is defined by registers [967:960]

3-Bit LUT3_5 is defined by registers [983:976]

3-Bit LUT3_6 is defined by registers [999:992]

3-Bit LUT3_7 is defined by registers [1015:1008]

Table 27: 3-bit LUT3_0 to 3-bit LUT3_9 Truth Table

IN2	IN1	IN0	OUT LUT3_0	OUT LUT3_1	OUT LUT3_2	OUT LUT3_3	OUT LUT3_4	OUT LUT3_5	OUT LUT3_6	OUT LUT3_7	
0	0	0	register [888]	register [896]	register [904]	register [912]	register [960]	register [976]	register [992]	register [1008]	LSB
0	0	1	register [889]	register [897]	register [905]	register [913]	register [961]	register [977]	register [993]	register [1009]	
0	1	0	register [890]	register [898]	register [906]	register [914]	register [962]	register [978]	register [994]	register [1010]	
0	1	1	register [891]	register [899]	register [907]	register [915]	register [963]	register [979]	register [995]	register [1011]	
1	0	0	register [892]	register [900]	register [908]	register [916]	register [964]	register [980]	register [996]	register [1012]	
1	0	1	register [893]	register [901]	register [909]	register [917]	register [965]	register [981]	register [997]	register [1013]	
1	1	0	register [894]	register [902]	register [910]	register [918]	register [966]	register [982]	register [998]	register [1014]	
1	1	1	register [895]	register [903]	register [911]	register [919]	register [967]	register [983]	register [999]	register [1015]	MSB

Table 28 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 28: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.4 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are 4 macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level Reset/Set (RST/SET) and active low level Reset/Set (nRST/nSET) options available which are selected by register [890].

DFF2 operation will flow the functional description below:

- If register [892] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [892] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

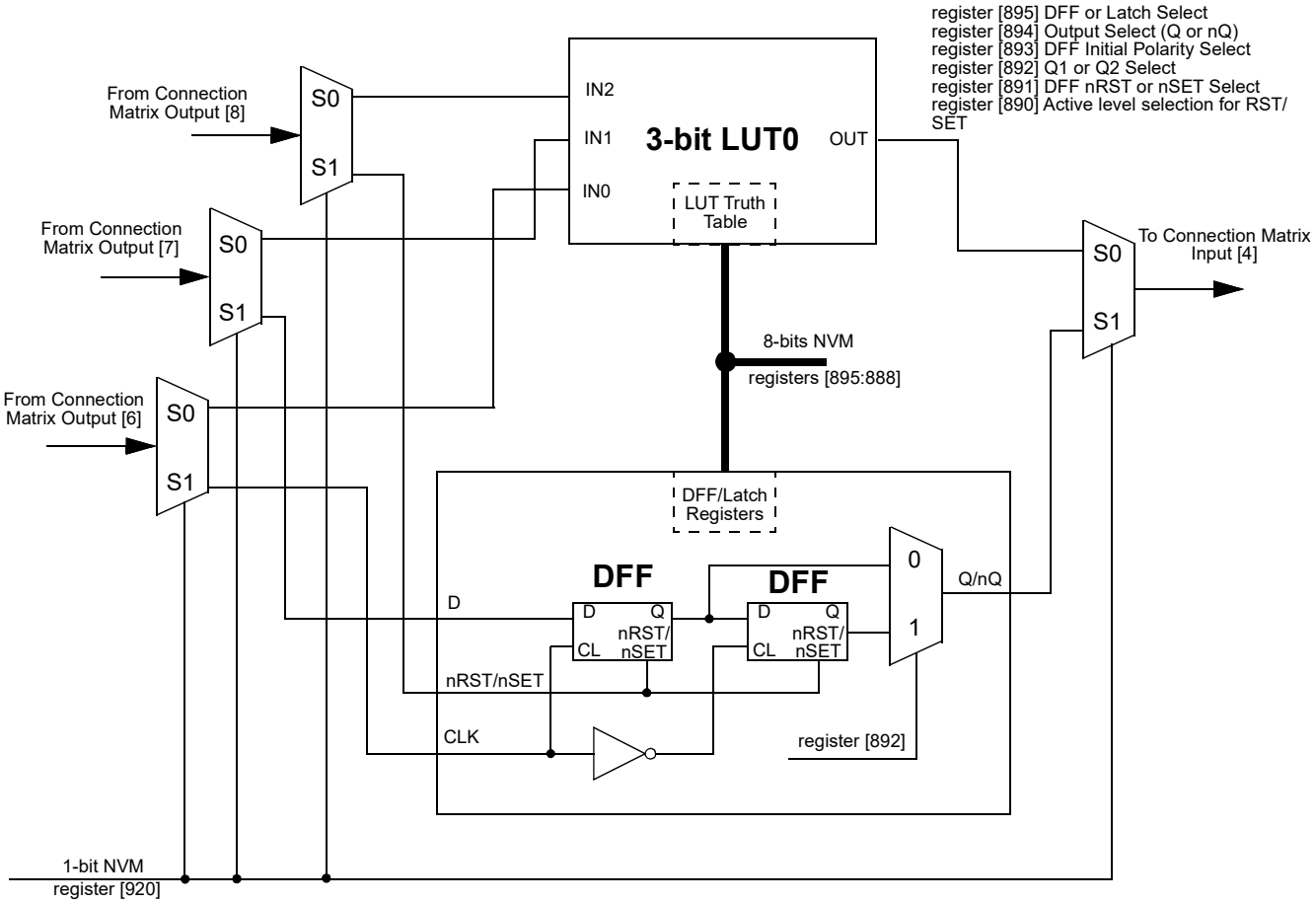


Figure 29: 3-bit LUT0 or DFF2

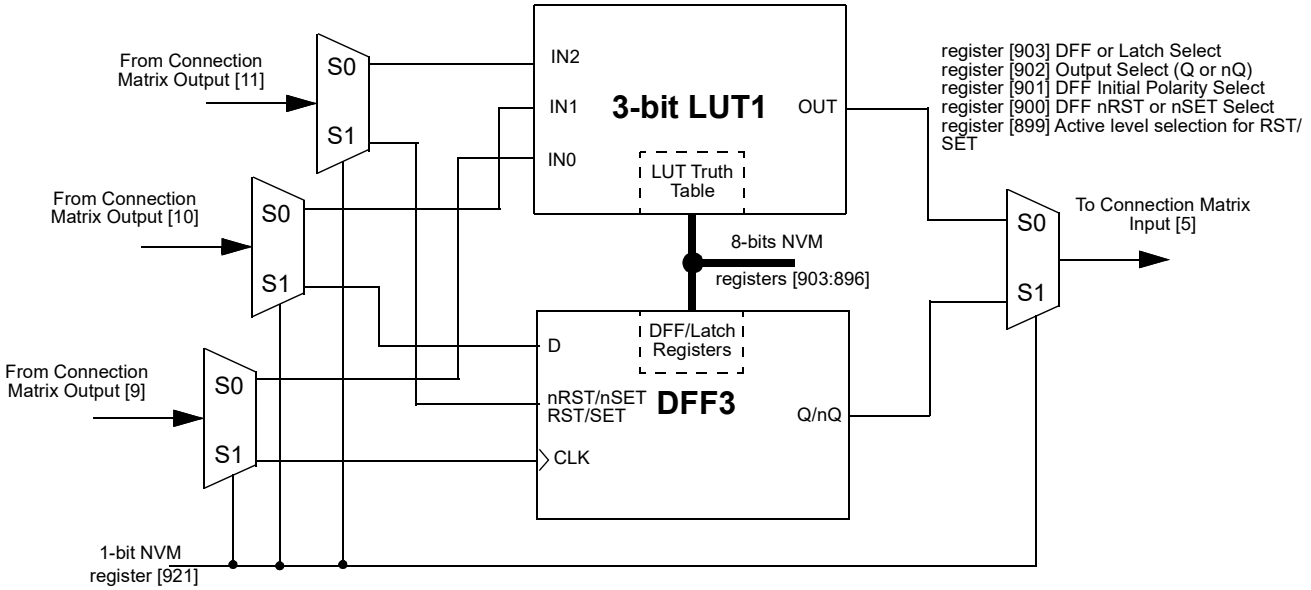


Figure 30: 3-bit LUT1 or DFF3

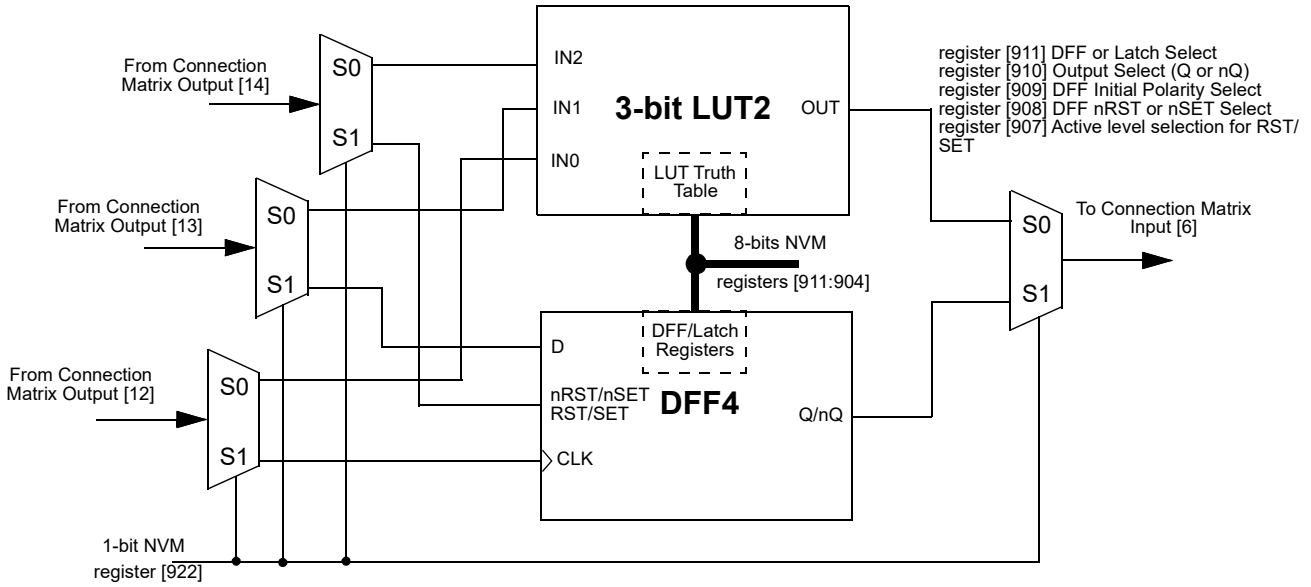


Figure 31: 3-bit LUT2 or DFF4

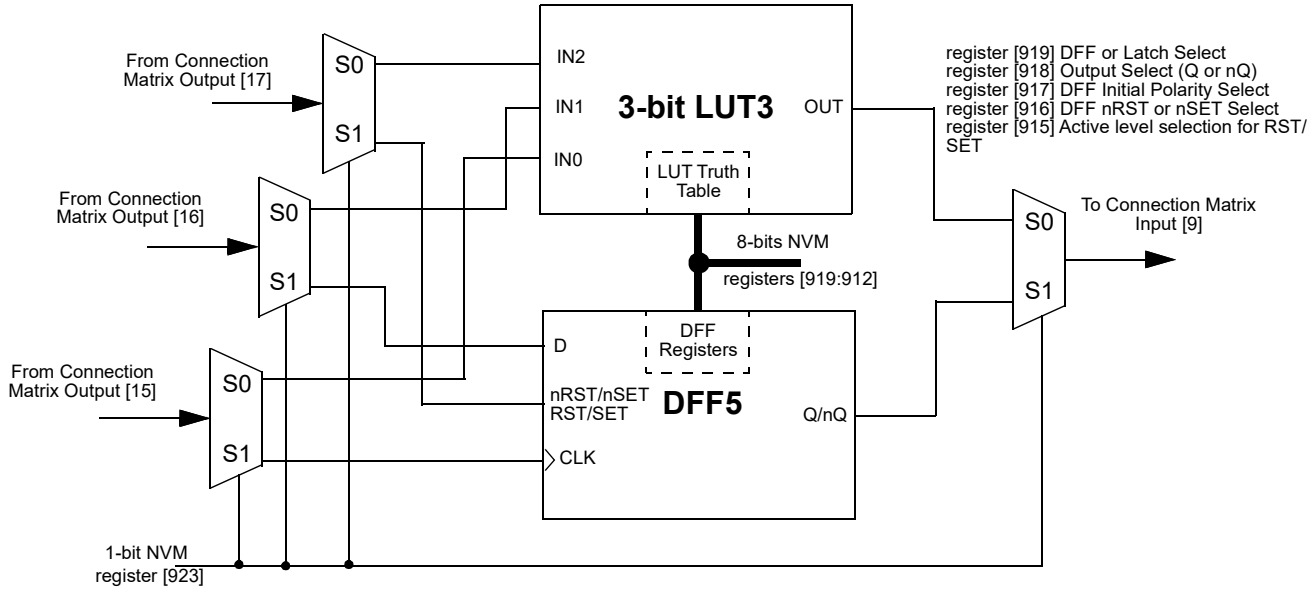


Figure 32: 3-bit LUT3 or DFF5

7.5 4-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELL

There is one macrocell that can serve as either a 4-bit LUT or as a D Flip-Flop with Set/Reset inputs. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix

- If register [943] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [943] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available which are selected by register [938].

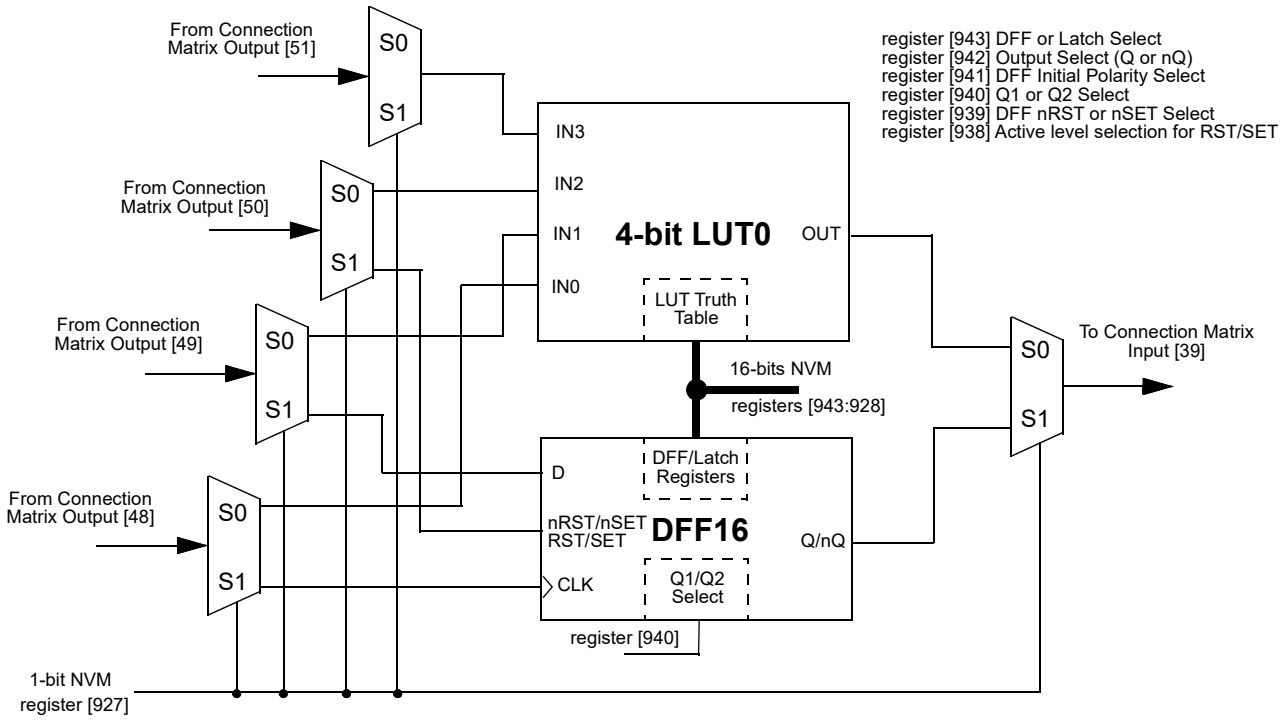


Figure 33: 4-bit LUT0 or DFF16

7.5.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 29: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [928]	LSB
0	0	0	1	register [929]	
0	0	1	0	register [930]	
0	0	1	1	register [931]	
0	1	0	0	register [932]	
0	1	0	1	register [933]	
0	1	1	0	register [934]	
0	1	1	1	register [935]	
1	0	0	0	register [936]	
1	0	0	1	register [937]	
1	0	1	0	register [938]	
1	0	1	1	register [939]	
1	1	0	0	register [940]	
1	1	0	1	register [941]	
1	1	1	0	register [942]	
1	1	1	1	register [943]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

*4-Bit LUT0 is defined by registers [*943:928*]*

Table 30: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

8 Multi-Function Macrocells

The SLG46811 has 6 Multi-Function macrocells that can serve more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 34.

See the list below for the functions that can be implemented in these macrocells:

- Five macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 3-bit LUT/D Flip-Flop and as 8-Bit Counter/Delay/FSM

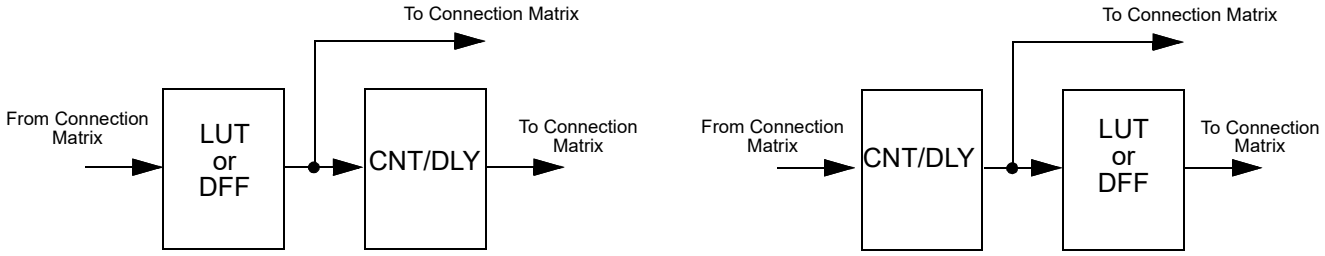


Figure 34: Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the 6 Multi-Function function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-BIT LUT OR DFF/LATCH WITH 8-BIT COUNTER/DELAY MACROCELLS

There are five macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Set/Reset (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which define its initial value after SLG46811 is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to sections 7.1 and 8.2.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

CNT/DLY0/FSM macrocell has an optional Finite State Machine (FSM) function. There is one additional Up/Down matrix input in FSM mode.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

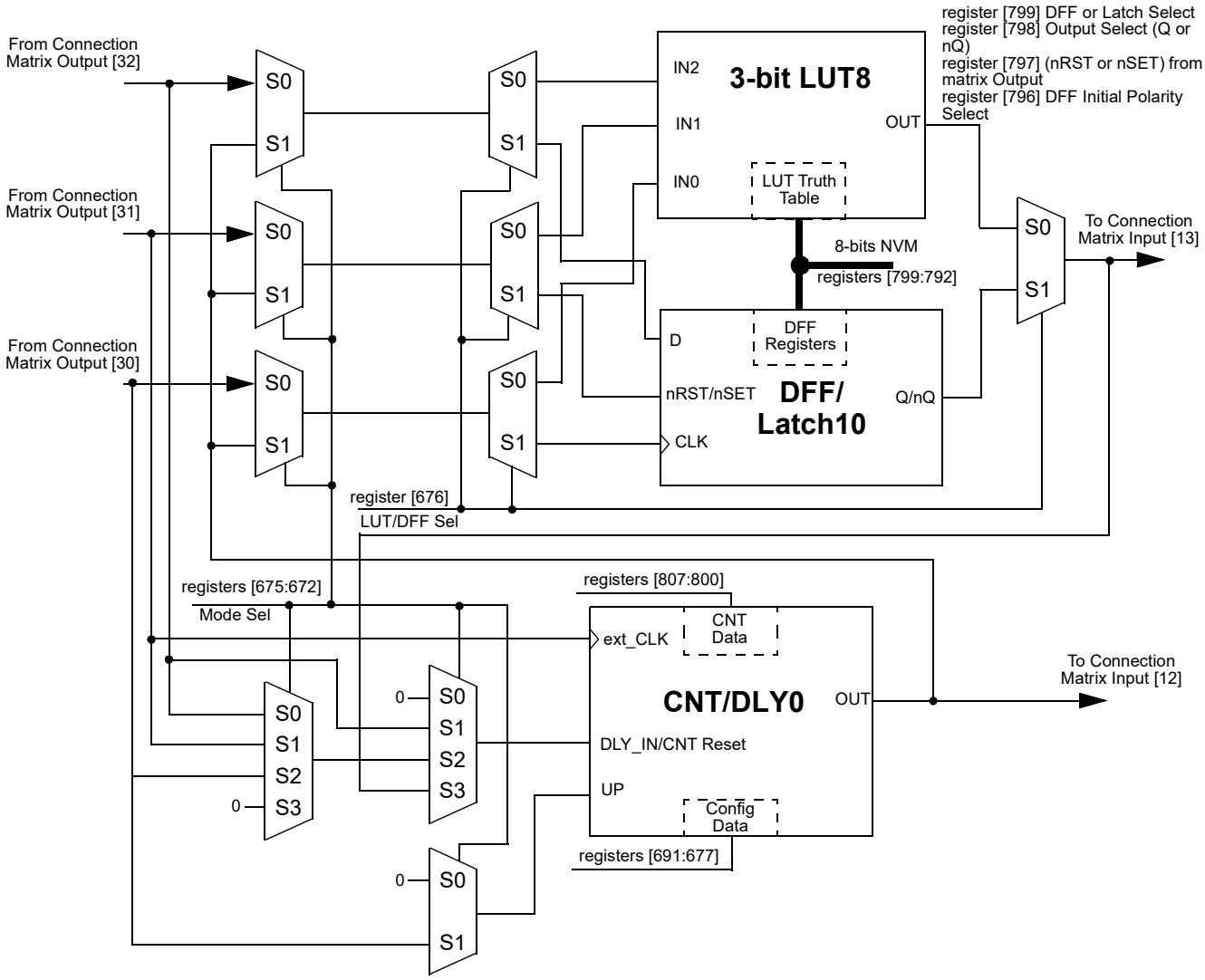


Figure 35: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF10, CNT/DLY0/FSM)

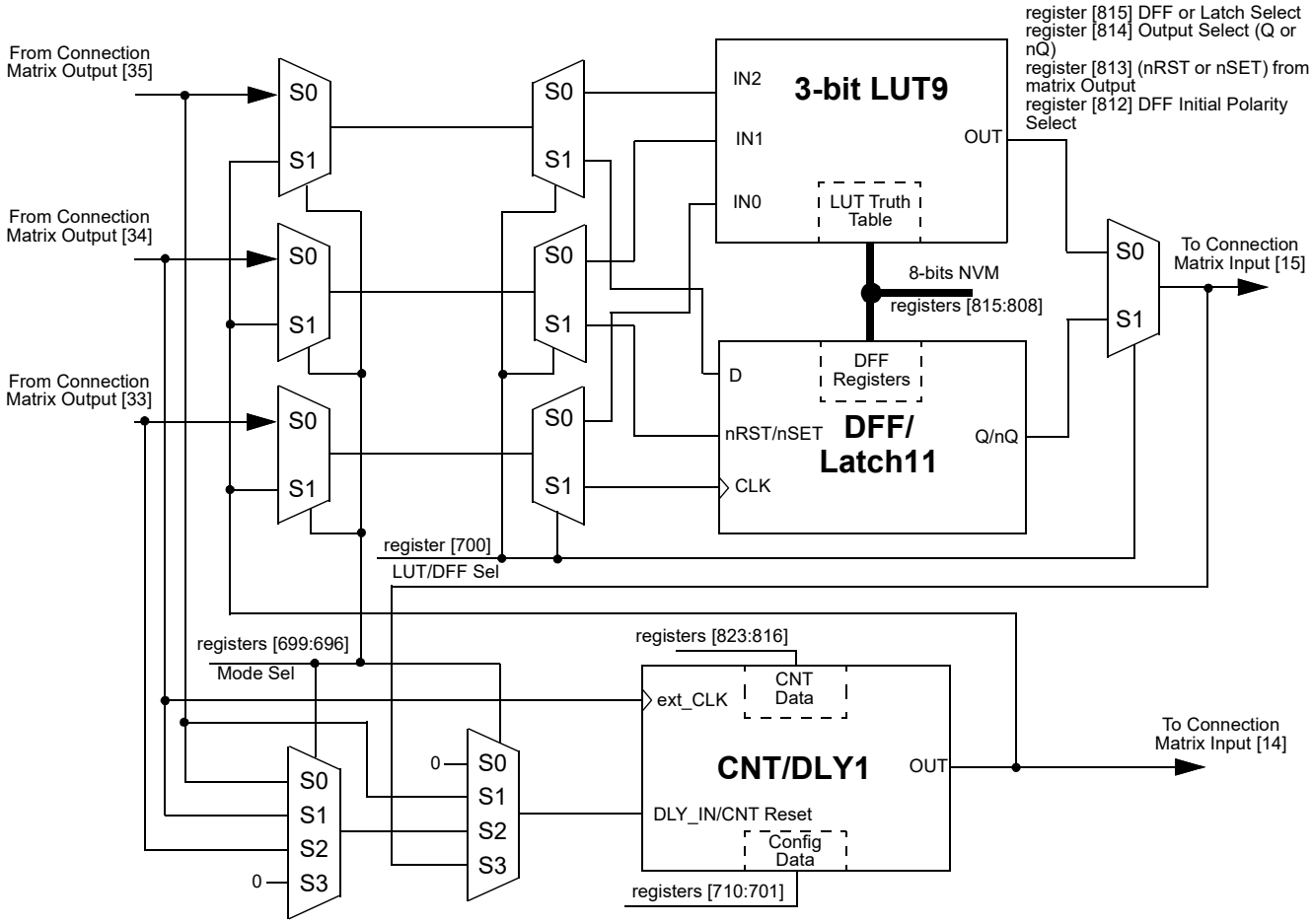


Figure 36: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF11, CNT/DLY1)

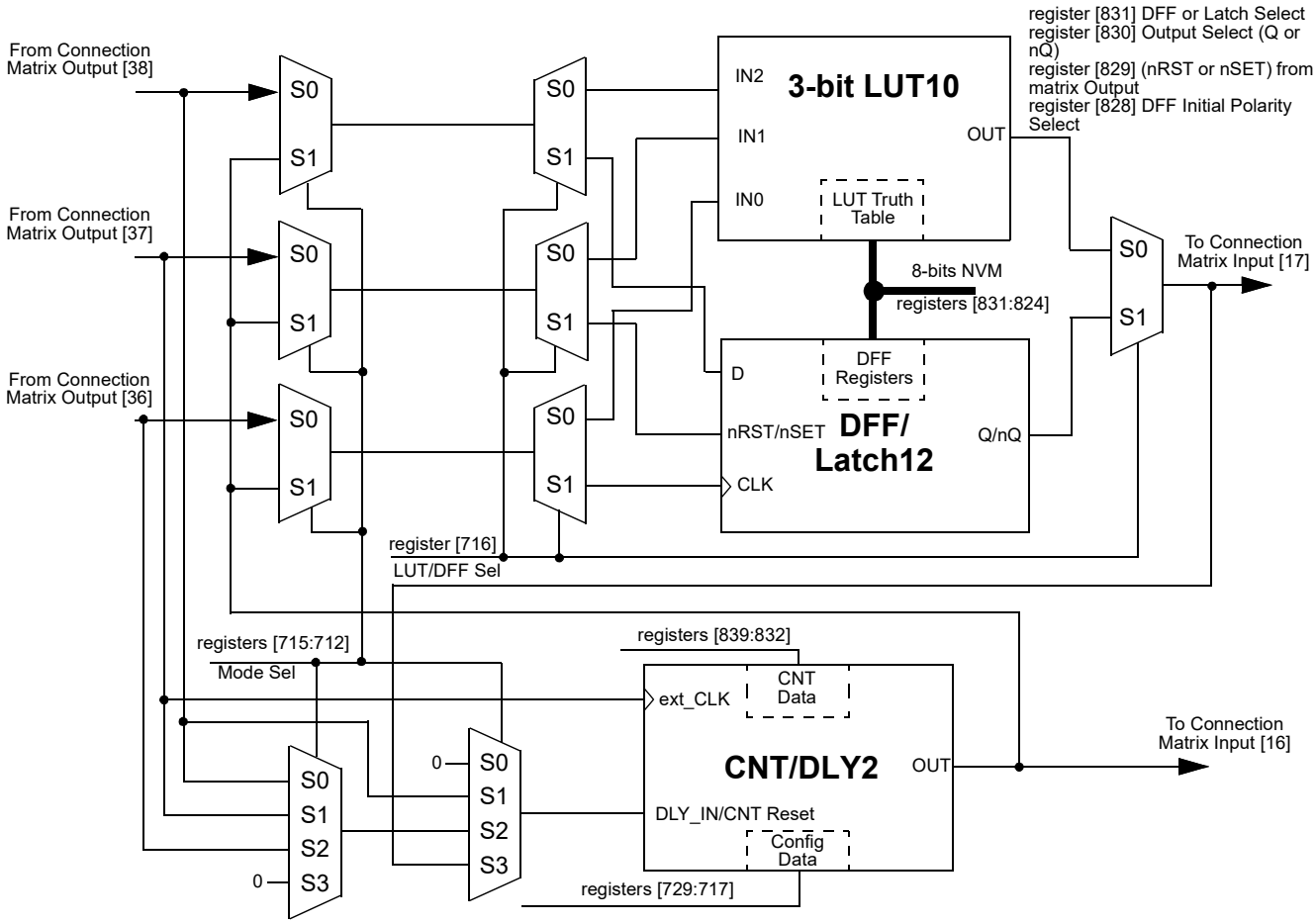


Figure 37: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF12, CNT/DLY2)

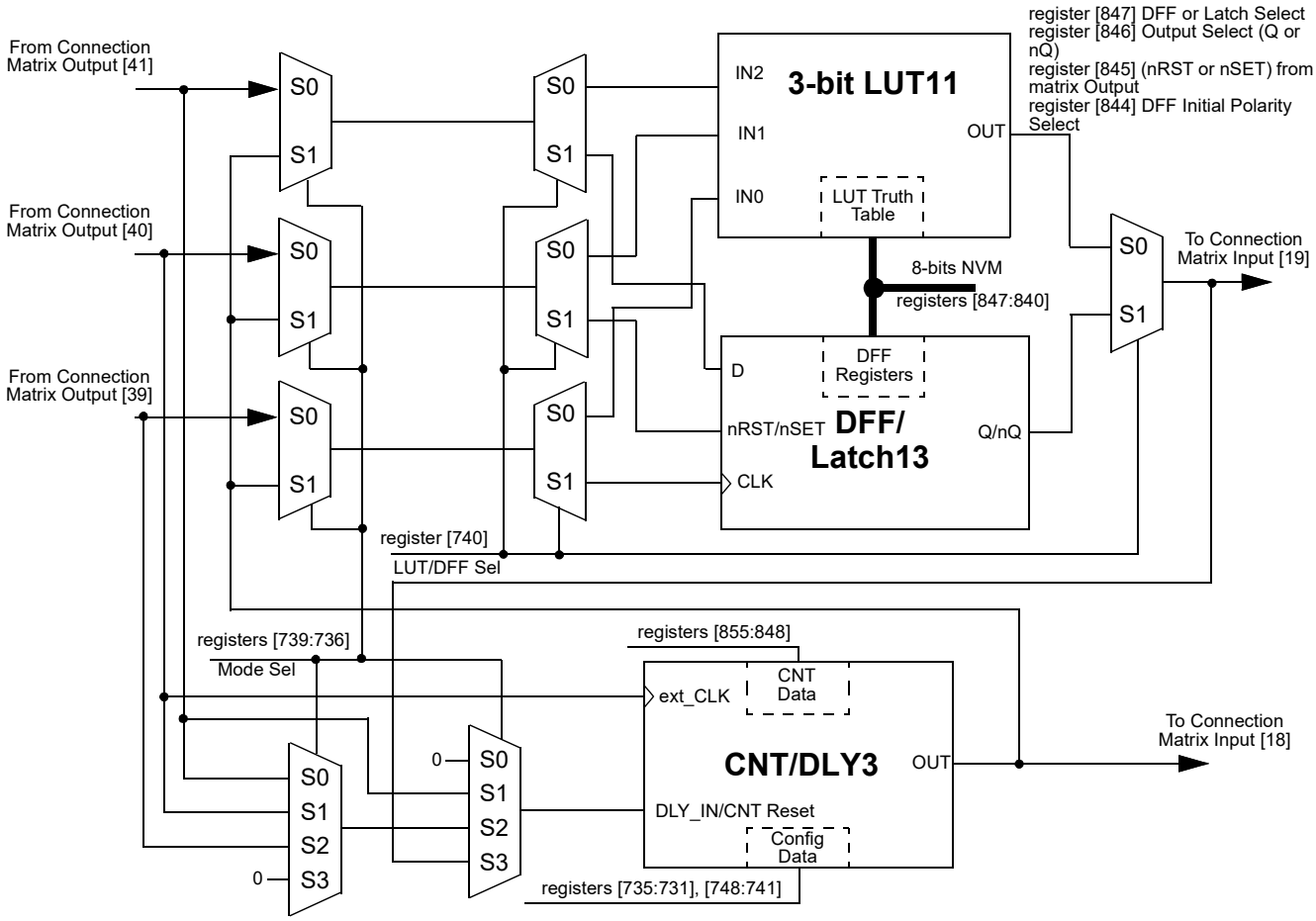


Figure 38: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF13, CNT/DLY3)

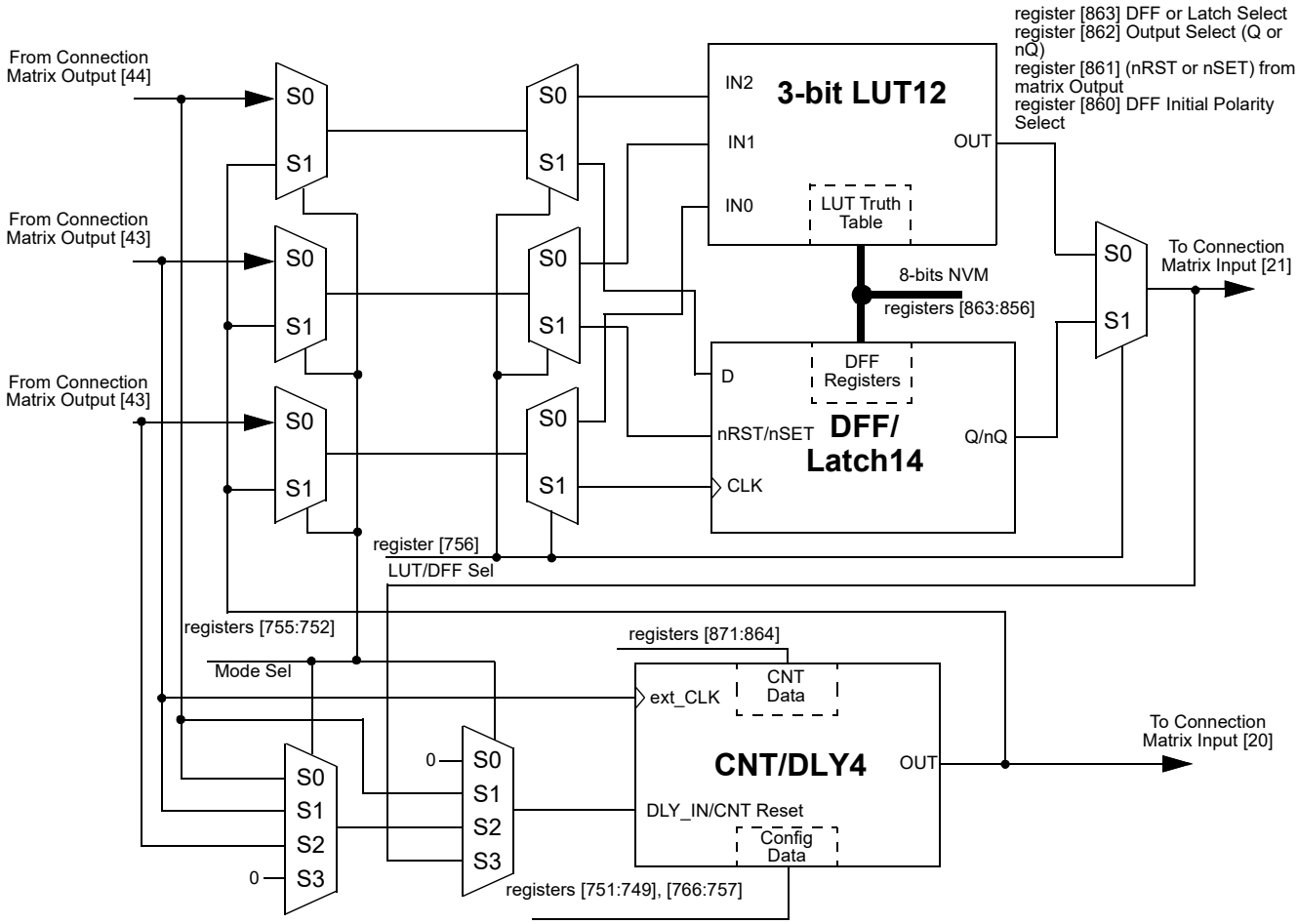


Figure 39: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF14, CNT/DLY4)

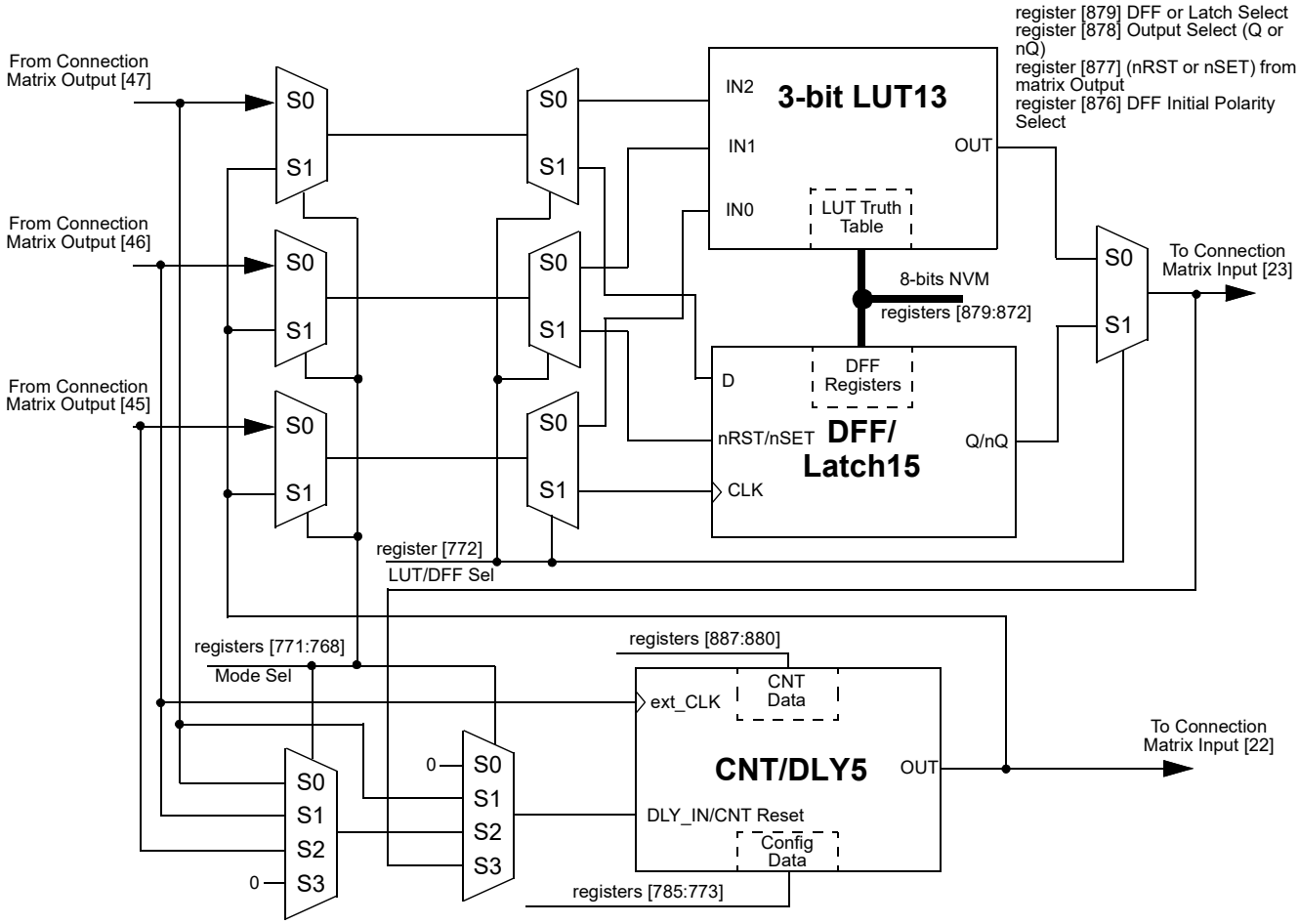


Figure 40: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF15, CNT/DLY5)

As shown in Figure 35 - Figure 40 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 31: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [792]	LSB
0	0	1	register [793]	
0	1	0	register [794]	
0	1	1	register [795]	
1	0	0	register [796]	
1	0	1	register [797]	
1	1	0	register [798]	
1	1	1	register [799]	MSB

Table 32: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [808]	LSB
0	0	1	register [809]	
0	1	0	register [810]	
0	1	1	register [811]	
1	0	0	register [812]	
1	0	1	register [813]	
1	1	0	register [814]	
1	1	1	register [815]	MSB

Table 33: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [824]	LSB
0	0	1	register [825]	
0	1	0	register [826]	
0	1	1	register [827]	
1	0	0	register [828]	
1	0	1	register [829]	
1	1	0	register [830]	
1	1	1	register [831]	MSB

Table 34: 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [840]	LSB
0	0	1	register [841]	
0	1	0	register [842]	
0	1	1	register [843]	
1	0	0	register [844]	
1	0	1	register [845]	
1	1	0	register [846]	
1	1	1	register [847]	MSB

Table 35: 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [856]	LSB
0	0	1	register [857]	
0	1	0	register [858]	
0	1	1	register [859]	
1	0	0	register [860]	
1	0	1	register [861]	
1	1	0	register [862]	
1	1	1	register [863]	MSB

Table 36: 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [872]	LSB
0	0	1	register [873]	
0	1	0	register [874]	
0	1	1	register [875]	
1	0	0	register [876]	
1	0	1	register [877]	
1	1	0	register [878]	
1	1	1	register [879]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

*3-Bit LUT8 is defined by registers [*799:792*]*

*3-Bit LUT9 is defined by registers [*815:808*]*

*3-Bit LUT10 is defined by registers [*831:824*]*

*3-Bit LUT11 is defined by registers [*847:840*]*

*3-Bit LUT12 is defined by registers [*863:856*]*

*3-Bit LUT13 is defined by registers [*879:872*]*

Optional Finite State Machine (FSM) function. There is additional matrix input Up to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

This macrocell can also operate in a frequency detection or edge detection mode.

8.2 CNT/DLY TIMING DIAGRAMS

8.2.1 Delay Mode CNT/DLY0 to CNT/DLY5

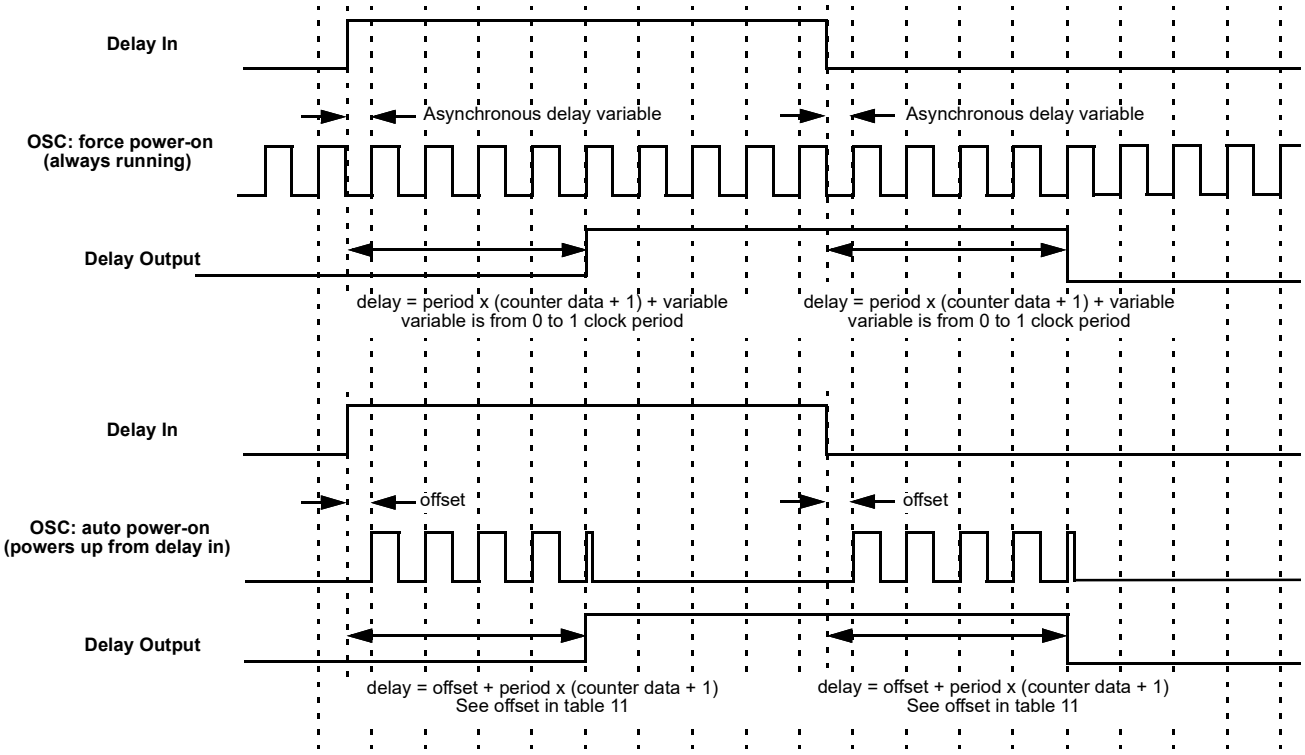


Figure 41: Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter, if the input signal is shorter than the delay time.

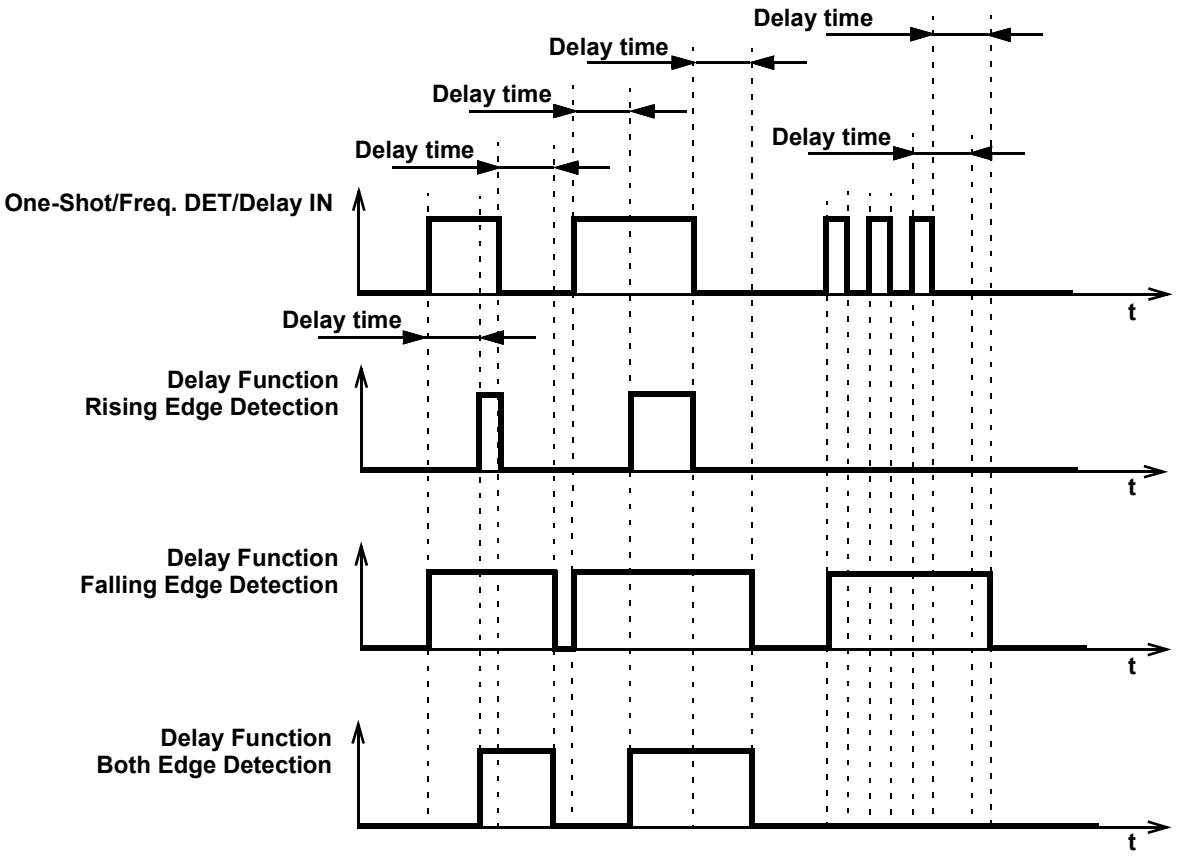


Figure 42: Delay Mode Timing Diagram for Different Edge Select Modes

8.2.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY5

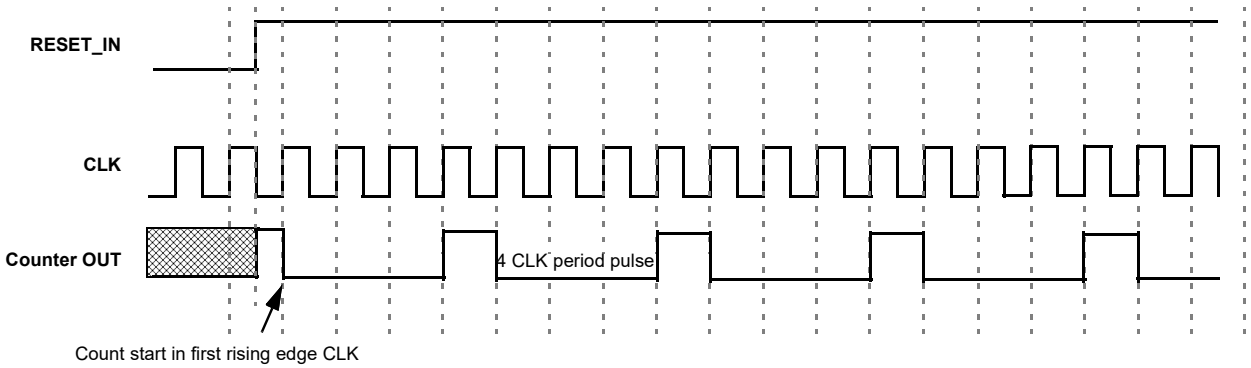


Figure 43: Counter Mode Timing Diagram without Two DFFs Synced Up

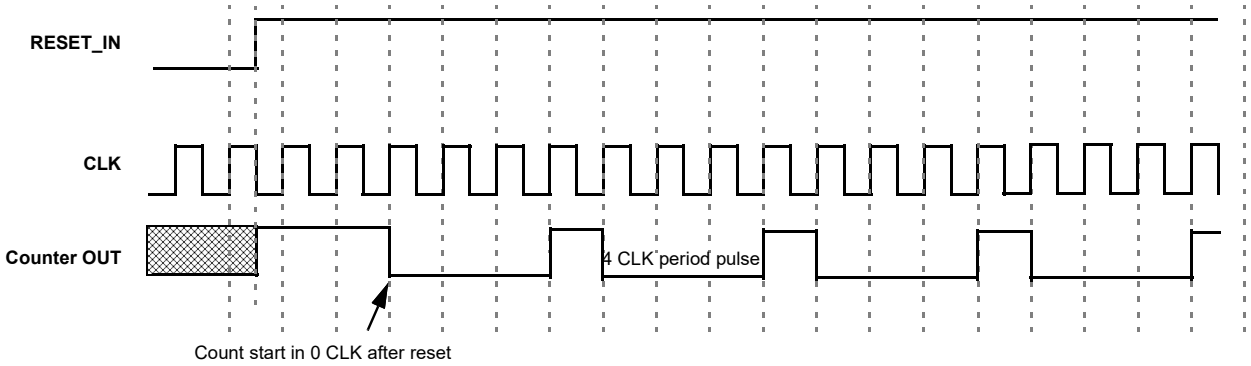


Figure 44: Counter Mode Timing Diagram with Two DFFs Synced Up

8.2.3 One-Shot Mode CNT/DLY0 to CNT/DLY5

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

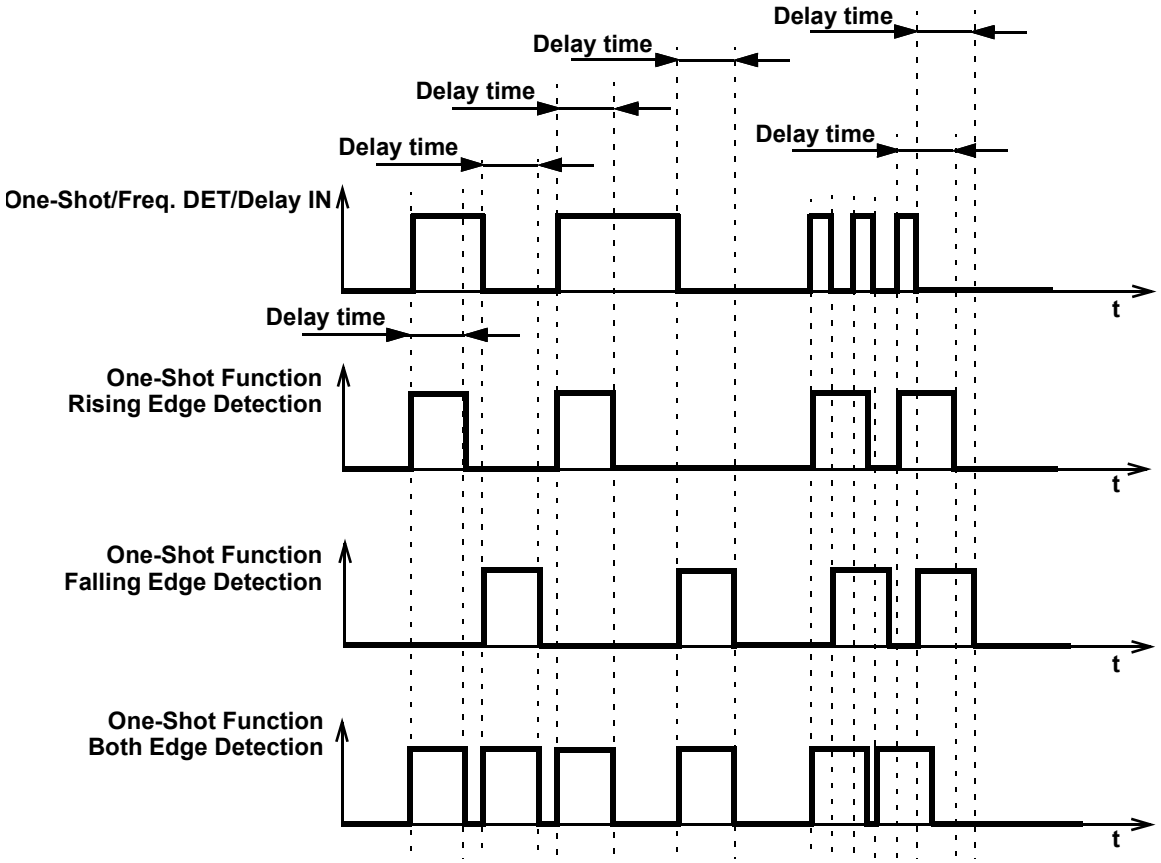


Figure 45: One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

8.2.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY5

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

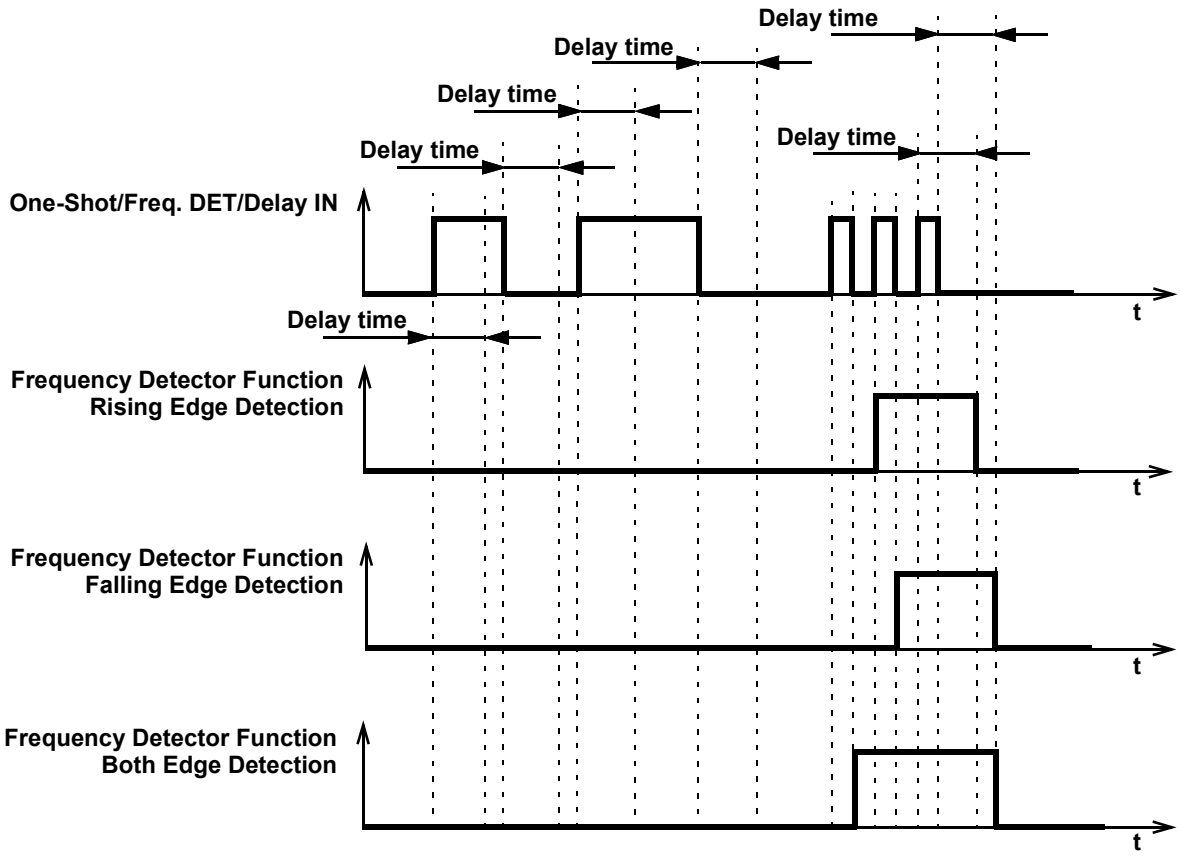


Figure 46: Frequency Detection Mode Timing Diagram

8.2.5 Edge Detection Mode CNT/DLY1 to CNT/DLY5

The macrocell generates high level short pulse when detecting the respective edge. See Figure 47.

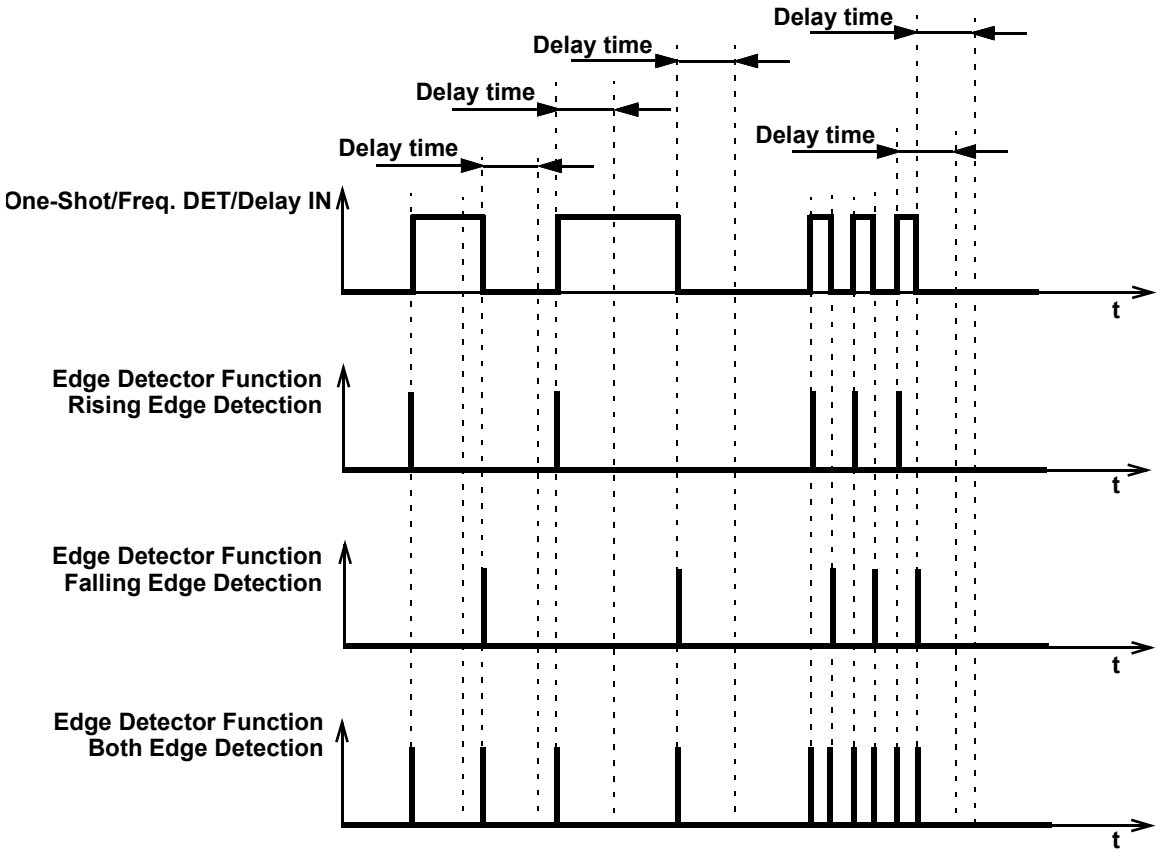


Figure 47: Edge Detection Mode Timing Diagram

8.2.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY5

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 48.

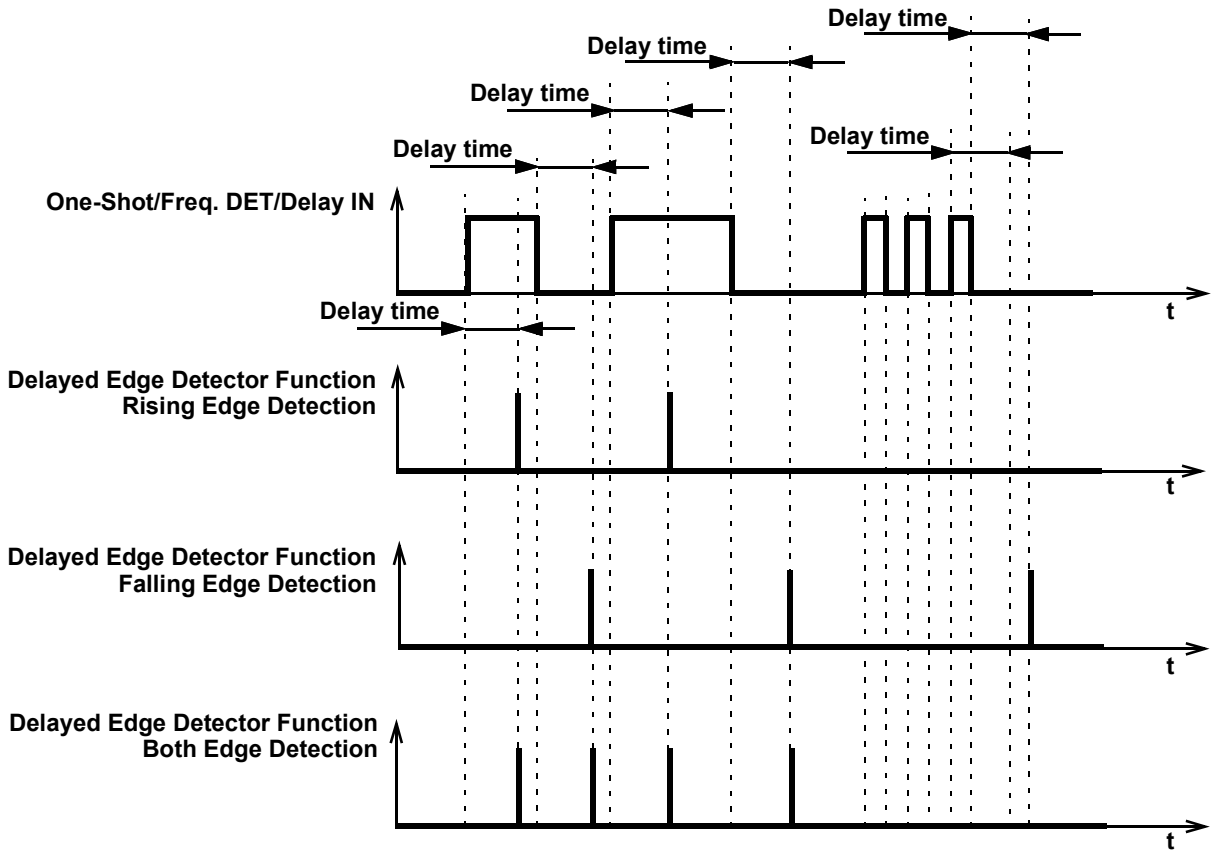


Figure 48: Delayed Edge Detection Mode Timing Diagram

8.2.7 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 49:

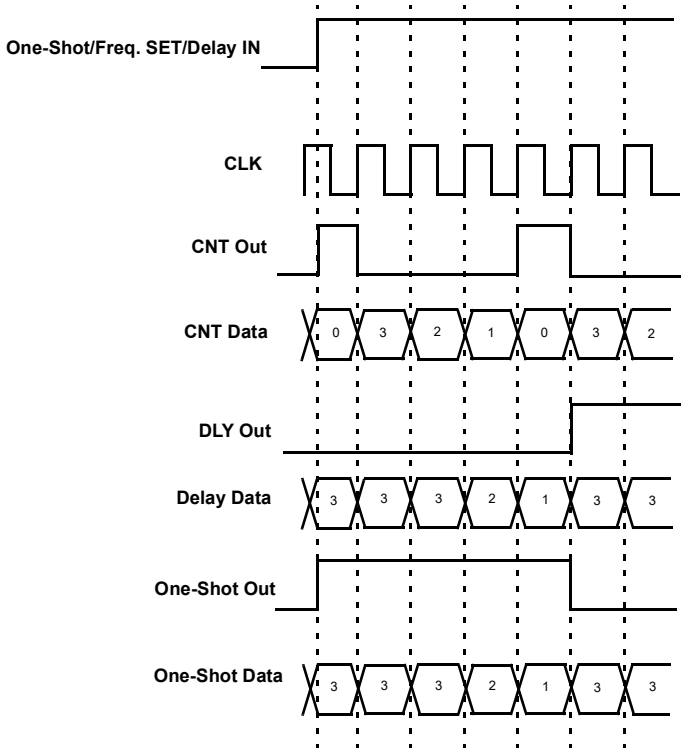


Figure 49: Counter Value, Counter Data = 3

8.3 FSM TIMING DIAGRAMS

The behavior of FSM macrocell with low level at Up input is the same as the behavior of other multifunction macrocells in corresponding modes (Counter, Delay, One Shot, Freq. Detector, Delayed Edge Detector).

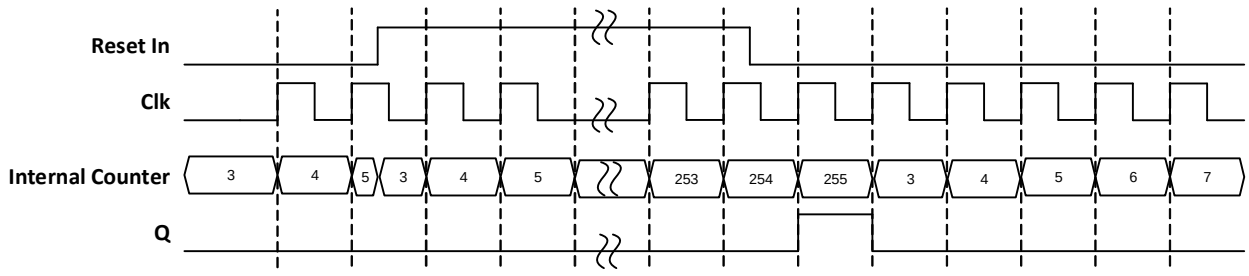


Figure 50: CNT/FSM Mode Timing Diagram (Set Rising Edge Mode, Oscillator Is Forced On, UP = 1) for CNT Data = 3

9 Multichannel Sampling Analog Comparator

The SLG46811 has one multichannel sampling ACMP that can make periodical samples of up to four input channels and latch the results at four outputs. The input sources for MS ACMP can be GPIO4, GPIO5, GPIO6, GPIO7, V_{DD}, Temperature sensor. User can select any number of channels to be sampled from one up to four, for example, Channel0, Channel2 and Channel3. Note that the channels are sampled in fixed order from 0 to 3rd. Each channel has separate configurable voltage reference and hysteresis. Vref range is from 32 mV to 2016 mV with 32 mV step in sampling mode and from 64 mV to 2016 mV with 32 mV step in regular mode. Hysteresis options are: no hysteresis, 32 mV (available only in sampling mode), 64 mV, 192 mV.
Non-inverting input of MS ACMP has the input divider that can be configured for each channel separately. The options for the divider are: Vin, Vin / 2, Vin / 3, Vin / 4.

MS ACMP uses internal oscillator0 to switch between channels, change Vref and latch the results. Clock from the oscillator0 can be divided by 2, 4, or 8 inside the MS ACMP. If "Auto power on" setting of oscillator is selected, High voltage level (or rising edge, depending on setting) on Enable input starts the internal oscillator. Please use MS ACMP clock frequencies from Table 37 when interfacing the sensor with high output impedance with SLG46811.

Table 37: Recommended MS ACMP Clock Frequencies

Parameter	Range 1	Range 2	Range 3	Range 4	Range 5	Unit
Sensor Output Resistance	< 1	1 to 2	2 to 4	4 to 6	> 6	MΩ
MS ACMP Clock Frequency	≤ 10	≤ 5	≤ 2.5	≤ 1.25	≤ 0.5	kHz

User can select the way the results appear at the outputs of MS ACMP. In asynchronous mode (register [499] = 0) results appear continuously after each channel is sampled. In synchronous mode (register [499] = 1) results at the output appear simultaneously after the last selected channel was sampled. The signal Sync data ready (matrix input [50]) generates a pulse of 100 ns approximate width when the sequence of selected channels was sampled.

Basic modes for MS ACMP are the next:

- Regular mode, register [497] = 0. In this mode MS ACMP operates as conventional ACMP. One selected channel is measured continuously when logic level at Enable input is High
- Sampling mode, register [497] = 1. Enable input is level sensitive, register [498] = 0. In this mode MS ACMP changes sampled channels and latches the result every pulse at Clk input while Enable input is High. When Enable becomes Low level MS ACMP finishes sampling the sequence and goes power down.
- Sampling mode, register [497] = 1. Enable input is edge sensitive, register [498] = 1. In this mode, when rising edge comes at Enable input, MS ACMP samples selected channels (up to four) every rising edge at Clk input and goes power down until the next pulse at Enable input.

9.1 MULTICHANNEL SAMPLING ACMP BLOCK DIAGRAM

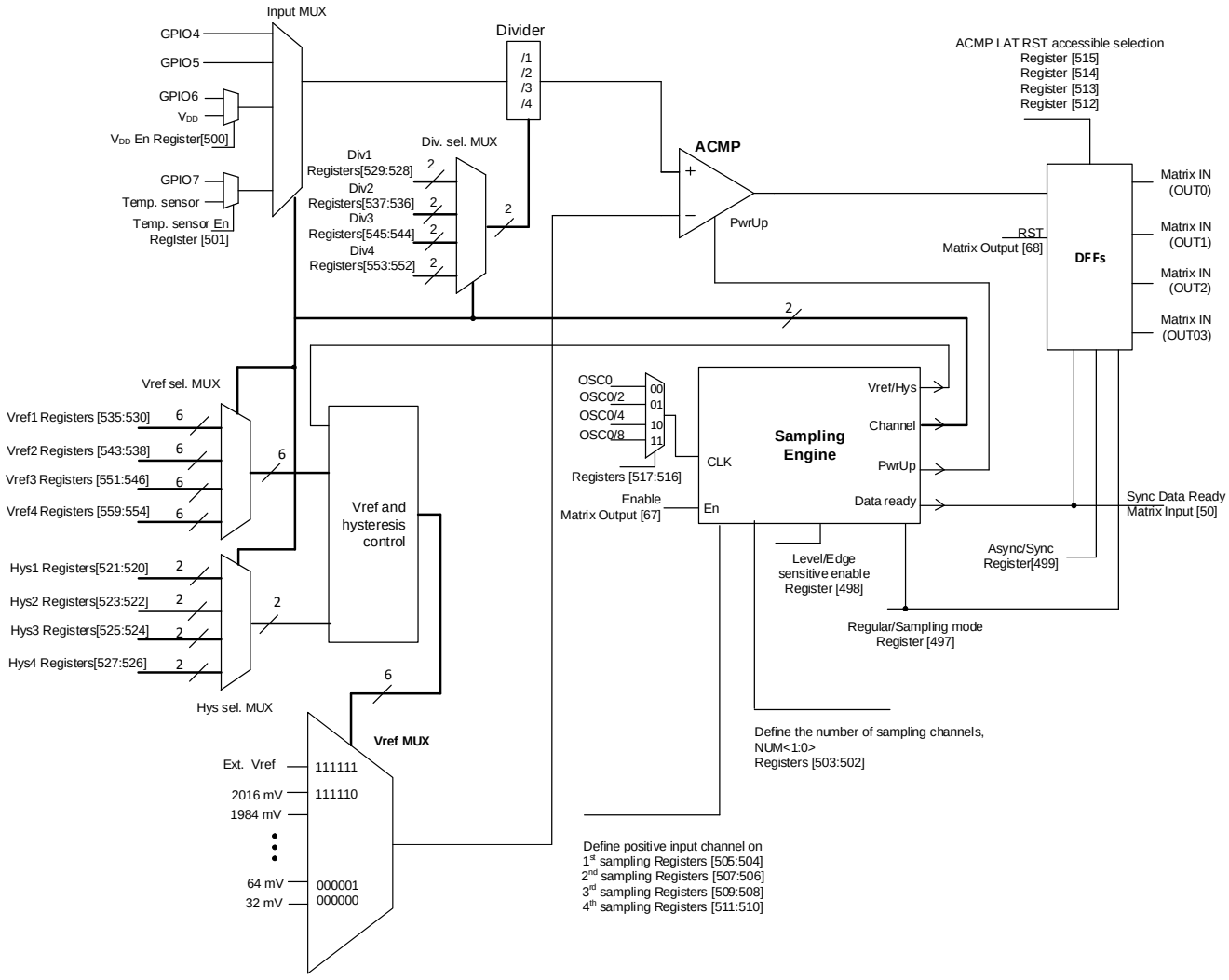


Figure 51: Multichannel Sampling ACMP Block Diagram

9.2 MS ACMP TIMING DIAGRAMS

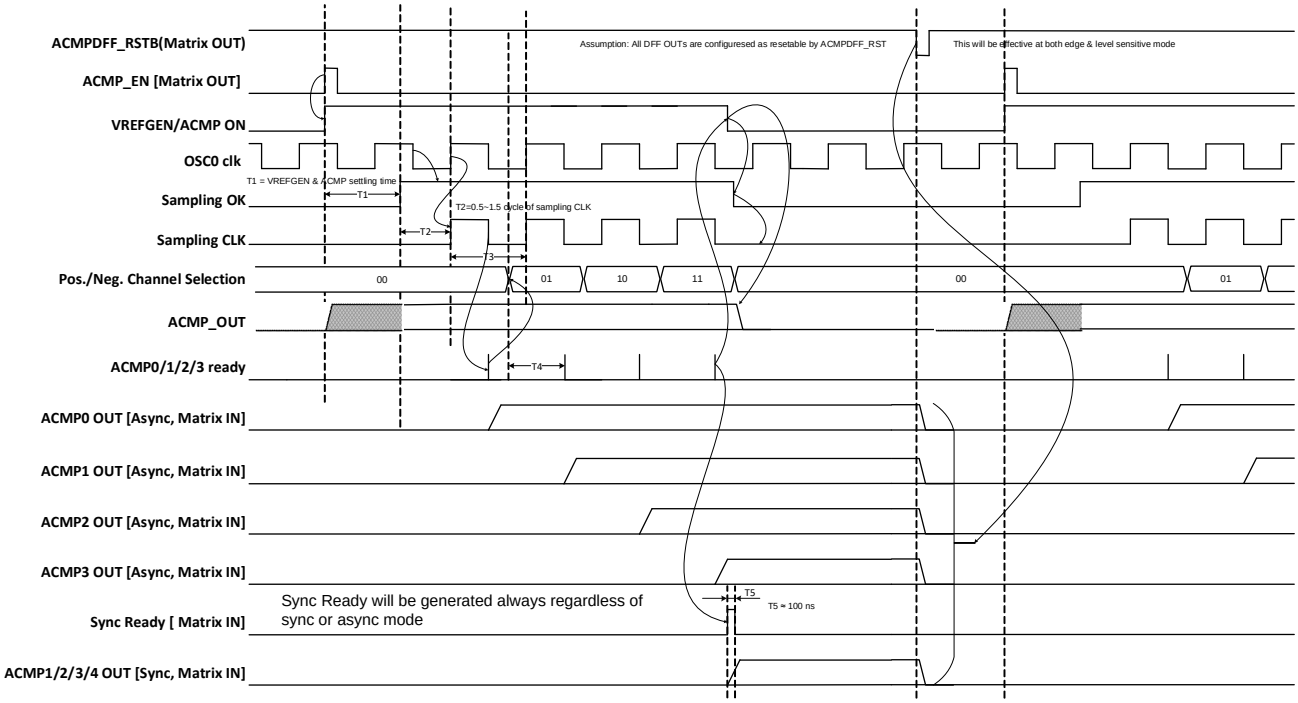


Figure 52: Timing Diagrams for MS ACMP. Edge Sensitive Mode. OSC0 and BG are Forced On

.

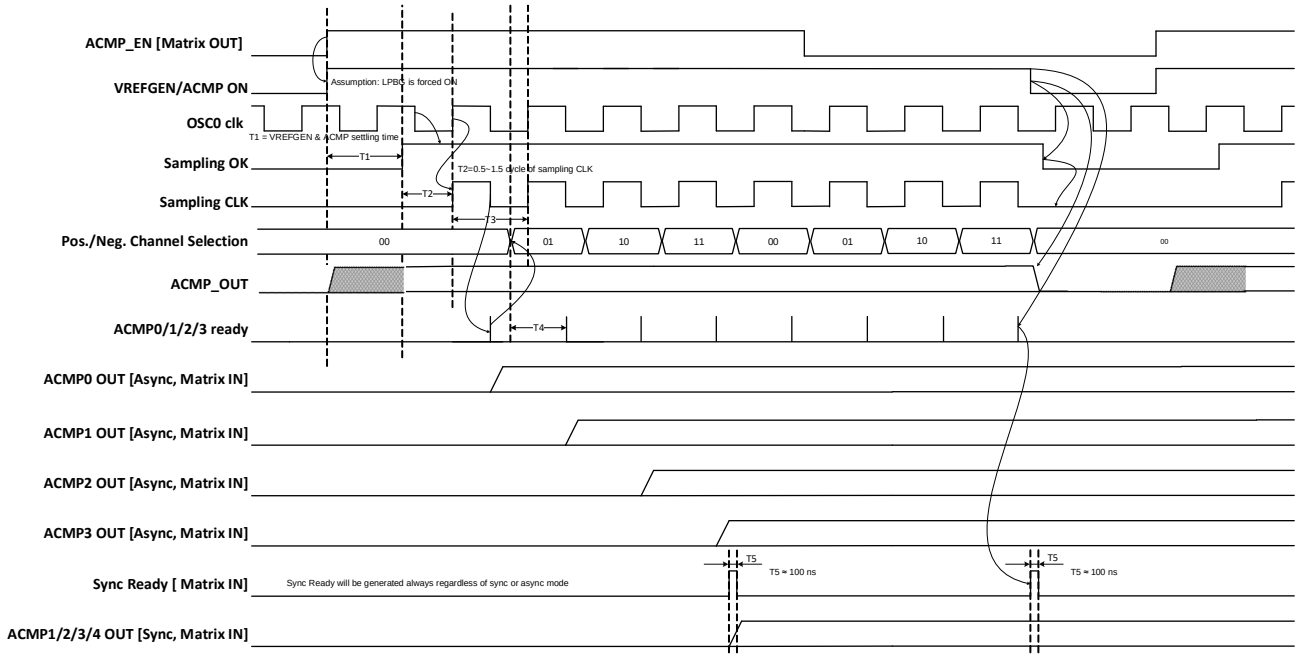


Figure 53: Timing Diagrams for MS ACMP. Level Sensitive Mode. OSC0 and BG are Forced On

.

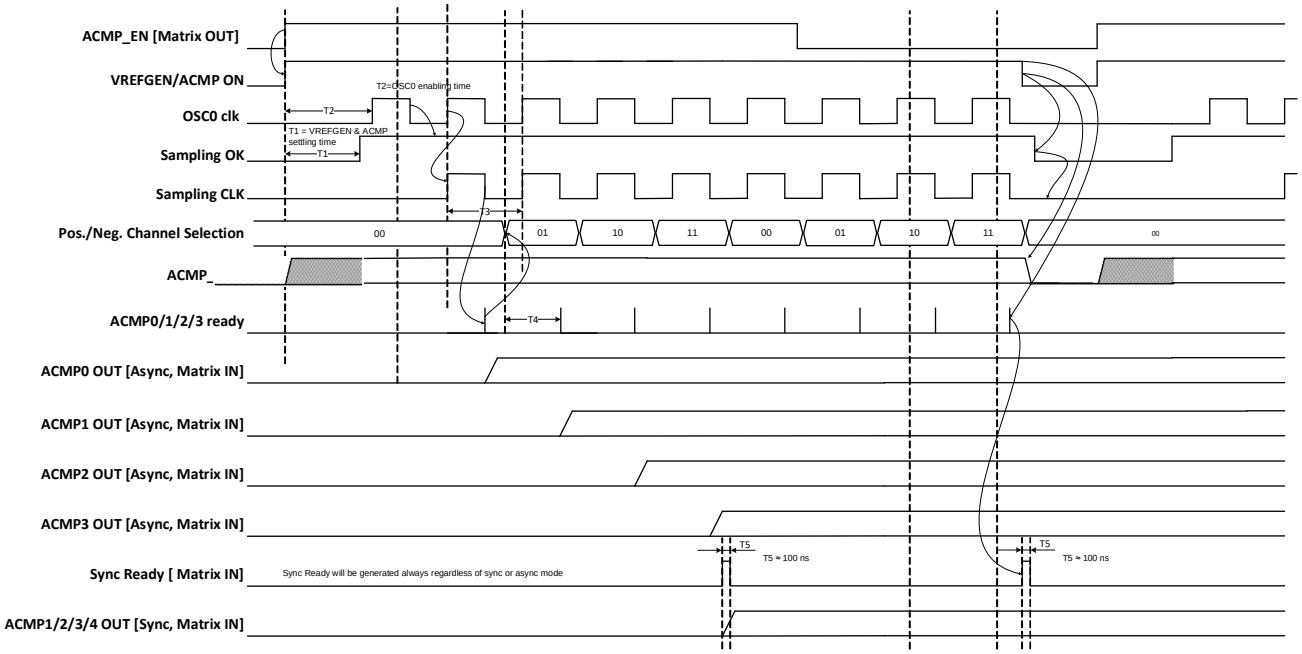


Figure 54: Timing Diagrams for MS ACMP. Level Sensitive Mode. OSC0 is in Auto Power On Mode. BG is Forced On

9.3 ACMP TYPICAL PERFORMANCE

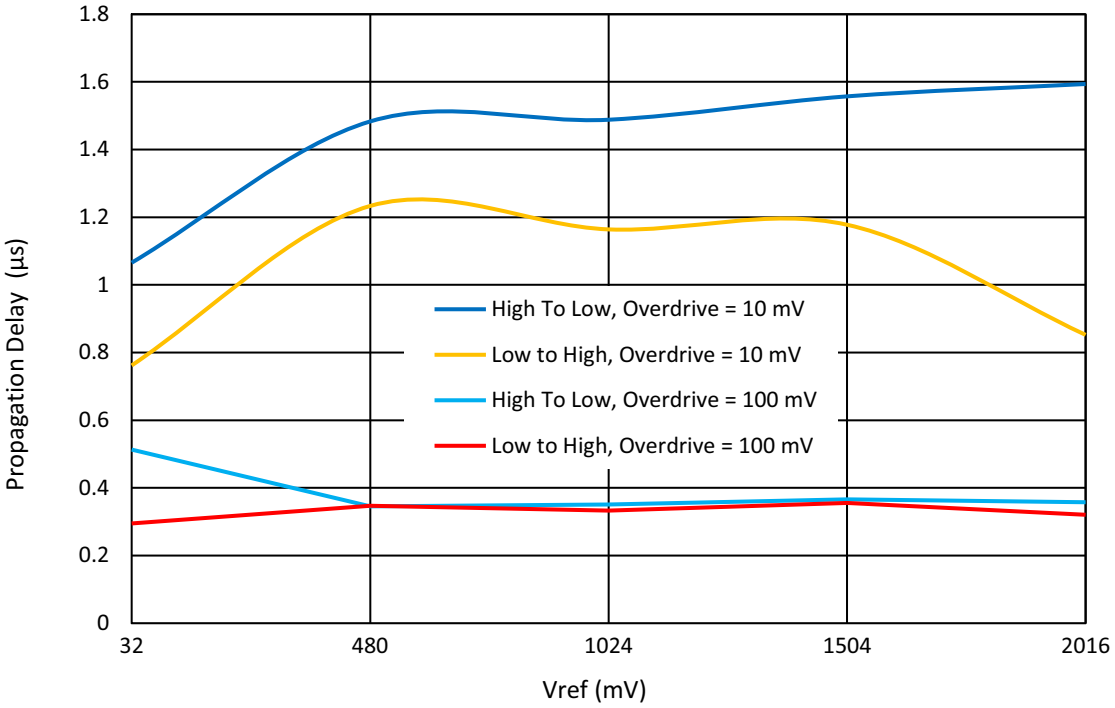


Figure 55: Typical Propagation Delay vs. Vref for MS ACMP at T = 25 °C, Gain = 1, Hysteresis = 0, Regular Mode

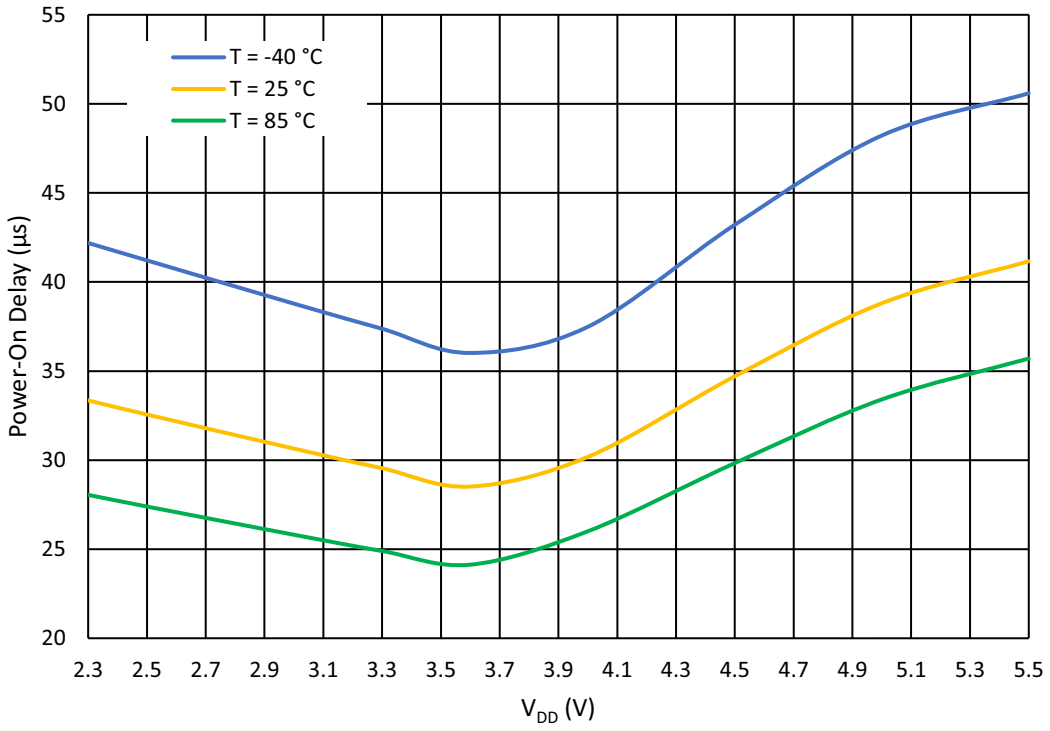


Figure 56: MS ACMP Power-On Delay vs. V_{DD}, Regular Mode

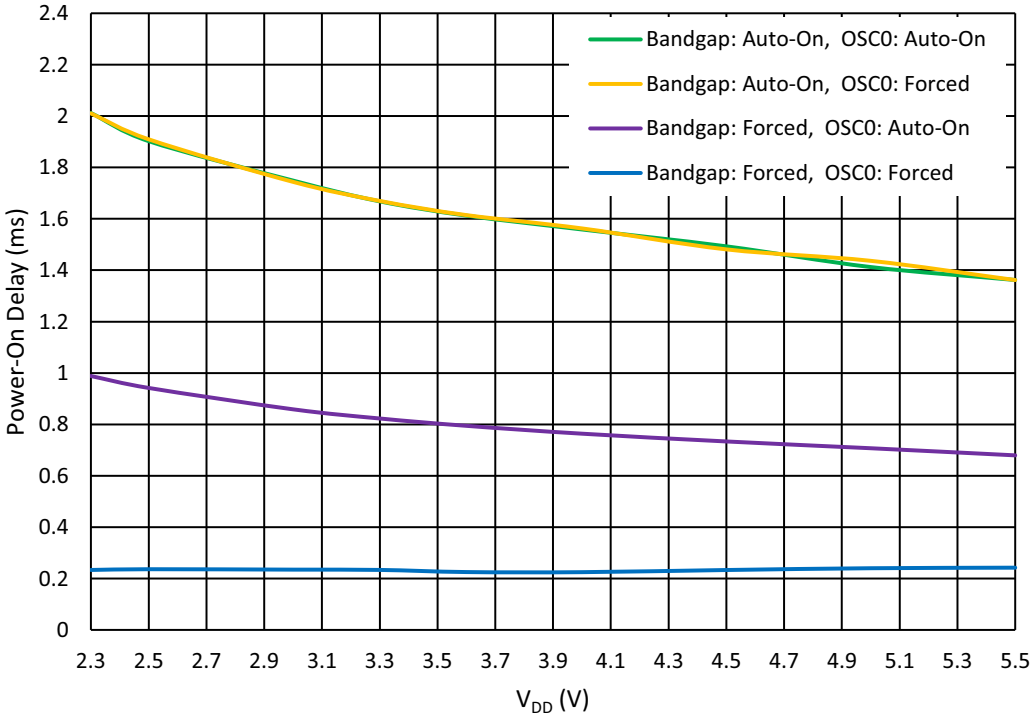


Figure 57: MS ACMP Power-On Delay vs. V_{DD}, Sampling Mode, T = -40 °C to 85 °C

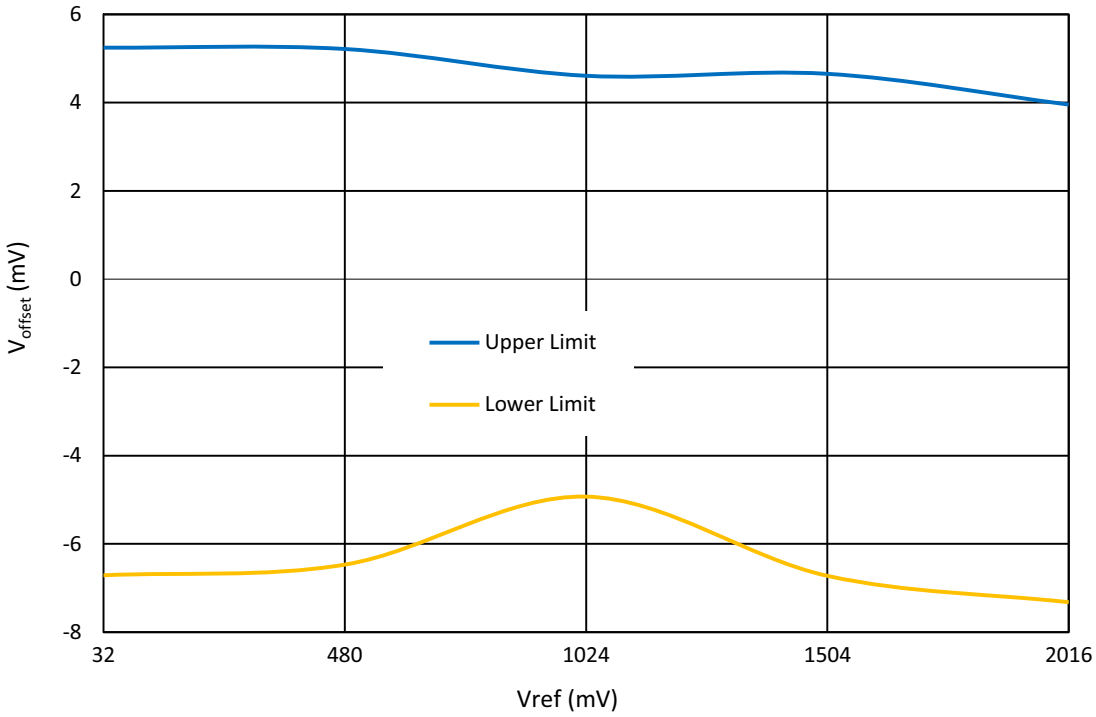


Figure 58: MS ACMP Input Offset Voltage vs. Vref at T = -40 °C to 85 °C

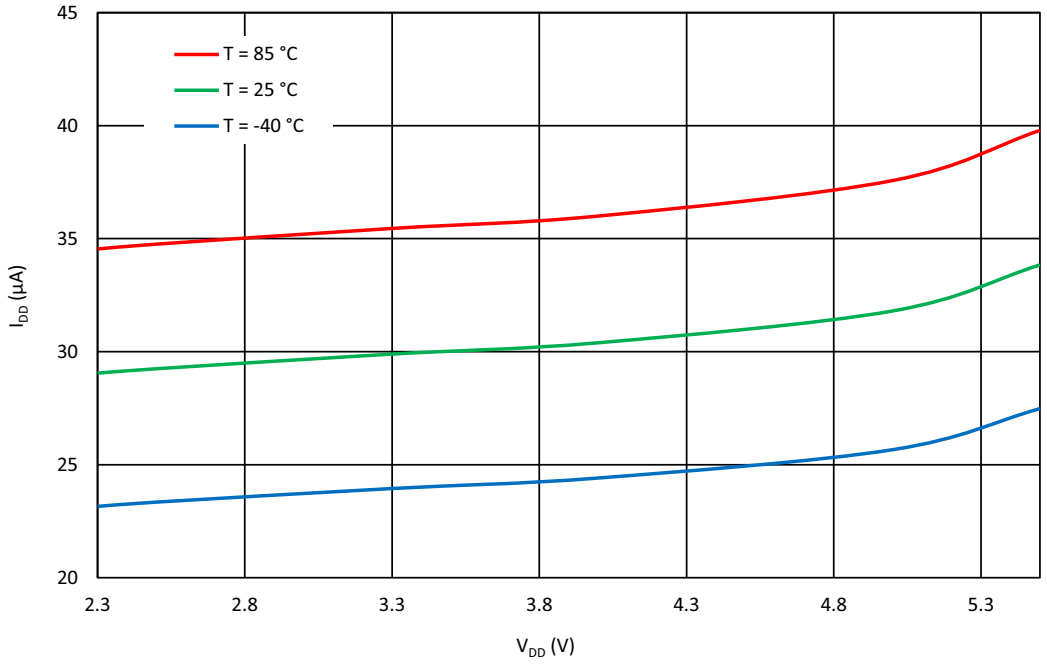


Figure 59: Current Consumption vs. V_{DD} for Regular Mode, External Vref, V_{IN+} = V_{DD}, V_{IN-} = GND

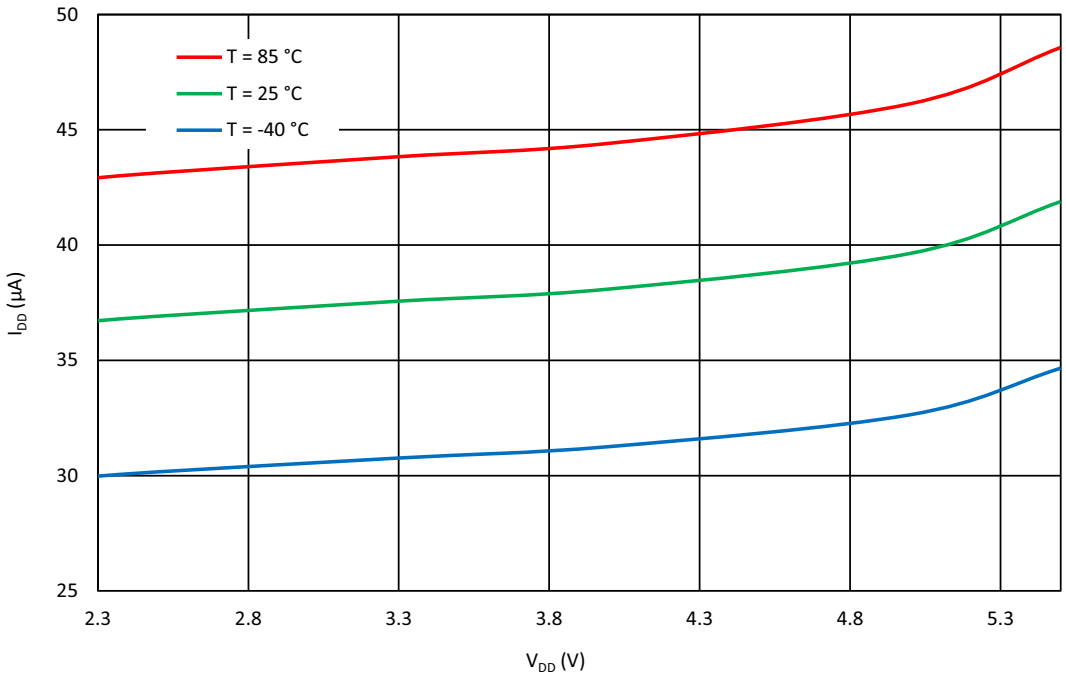


Figure 60: Current Consumption vs. V_{DD} for Sampling Mode, 4 Channels, V_{IN+} = 2048 mV, V_{IN-} = 32 mV, Clock = 10 kHz

10 Programmable Delay/Edge Detector

The SLG46811 has a programmable time delay logic cell that can generate a delay that is selectable from one of four timings (time2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 62 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

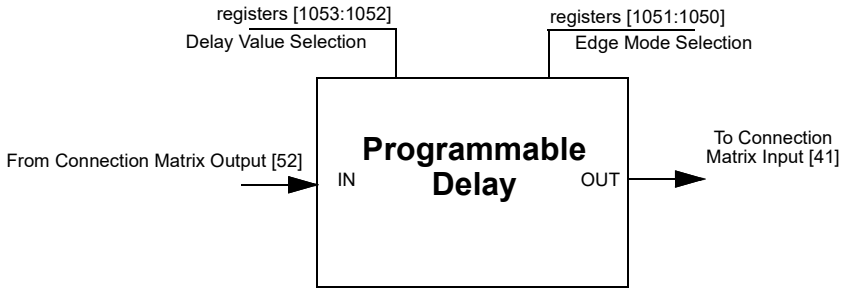


Figure 61: Programmable Delay

10.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

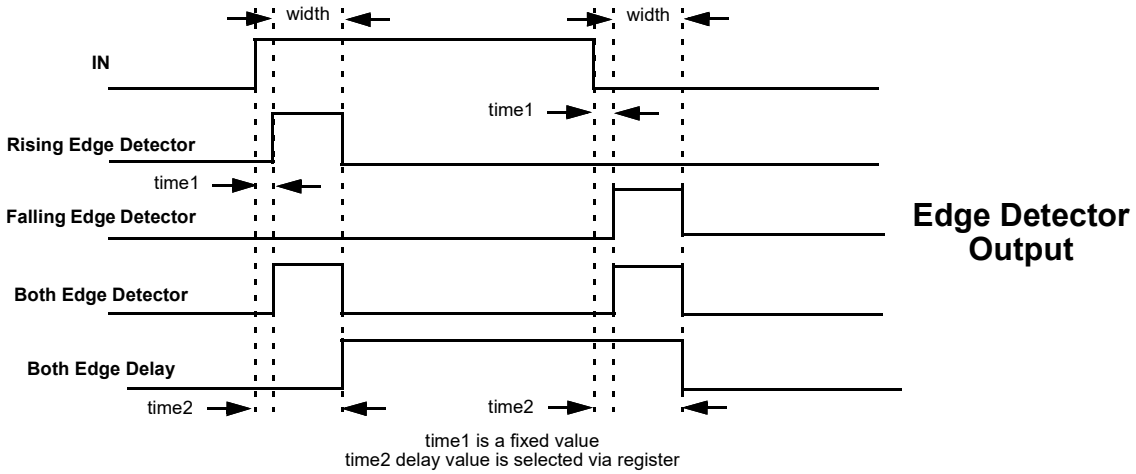


Figure 62: Edge Detector Output

Please refer to Table 12.

11 Additional Logic Function. Deglitch Filter

The SLG46811 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. The filter pass the input signal for pulse width > tpass (at typical temperature 25 °C. See Table 14).

In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

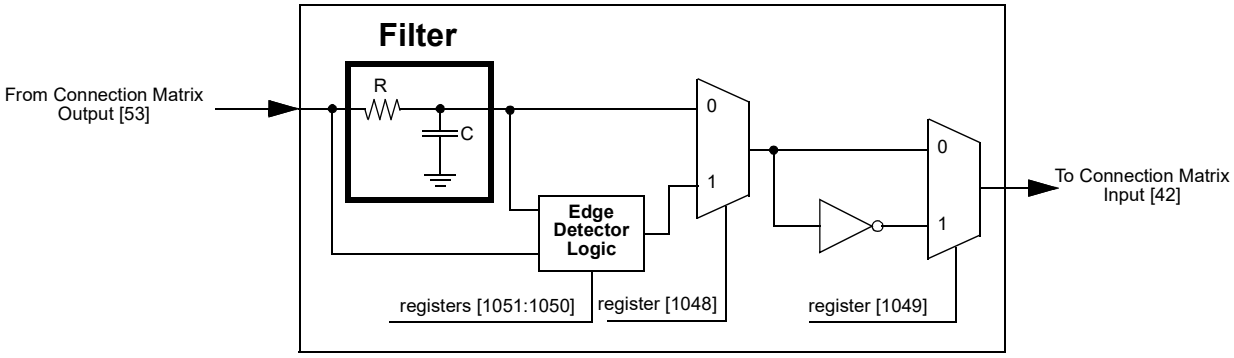


Figure 63: Deglitch Filter/Edge Detector Simplified Structure

12 Voltage Reference

12.1 VOLTAGE REFERENCE OVERVIEW

The SLG46811 has a Voltage Reference (Vref) macrocell to provide references to the Multichannel Sampling Analog Comparator. See Table 38 for the available selections for Multichannel Sampling Analog Comparator.

12.2 VREF SELECTION TABLE

Table 38: Vref Selection Table

SEL[5:0]	Vref	SEL[5:0]	Vref
0	0.032	32	1.056
1	0.064	33	1.088
2	0.096	34	1.12
3	0.128	35	1.152
4	0.16	36	1.184
5	0.192	37	1.216
6	0.224	38	1.248
7	0.256	39	1.28
8	0.288	40	1.312
9	0.32	41	1.344
10	0.352	42	1.376
11	0.384	43	1.408
12	0.416	44	1.44
13	0.448	45	1.472
14	0.48	46	1.504
15	0.512	47	1.536
16	0.544	48	1.568
17	0.576	49	1.6
18	0.608	50	1.632
19	0.64	51	1.664
20	0.672	52	1.696
21	0.704	53	1.728
22	0.736	54	1.76
23	0.768	55	1.792
24	0.8	56	1.824
25	0.832	57	1.856
26	0.864	58	1.888
27	0.896	59	1.92
28	0.928	60	1.952
29	0.96	61	1.984
30	0.992	62	2.016
31	1.024	63	External

13 Clocking

13.1 OSC GENERAL DESCRIPTION

The SLG46811 has two internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz or 10 kHz optional selection)
- Oscillator1 (25 MHz).

The Oscillator0 can operate in one of two modes (2.048 kHz or 10 kHz) selected by register [581]. There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to connection matrix, as well as various other macrocells. The pre-divider (first stage) for Oscillator0 is clock /1, /2, /4 or /8. The pre-divider (first stage) for Oscillator1 is clock /1, /2, /4, /8, /12, /24, /48. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines [43], [49]. Please see Figure 64, Figure 65 and Figure 66 for more details on the SLG46811 clock scheme.

Oscillator1 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [592]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillators using an external pin (see Table 39). The Matrix Power-down/Force On (Connection Matrix Output [579]) signal has the highest priority.

Table 39: Oscillator Control Input Modes

Registers [567:566]	Description
b00	OSC0 (2kHz/10kHz): Controlled by register [578] OSC1 (25MHz): Controlled by register [568]
b01	OSC0 (2kHz/10kHz): Controlled by Matrix Output OSC1 (25MHz): Controlled by register [568]
b10	OSC0 (2kHz/10kHz): Controlled by register [578] OSC1 (25MHz): Controlled by Matrix Output
b11	OSC0 (2kHz/10kHz): Controlled by Matrix Output OSC1 (25MHz): Controlled by Matrix Output

The OSC operates according to the Table 40:

Table 40: Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF
Note 1 The OSC will run only when any macrocell that uses OSC is powered on.						

13.2 OSCILLATOR0 (2.048 KHZ/10 KHZ)

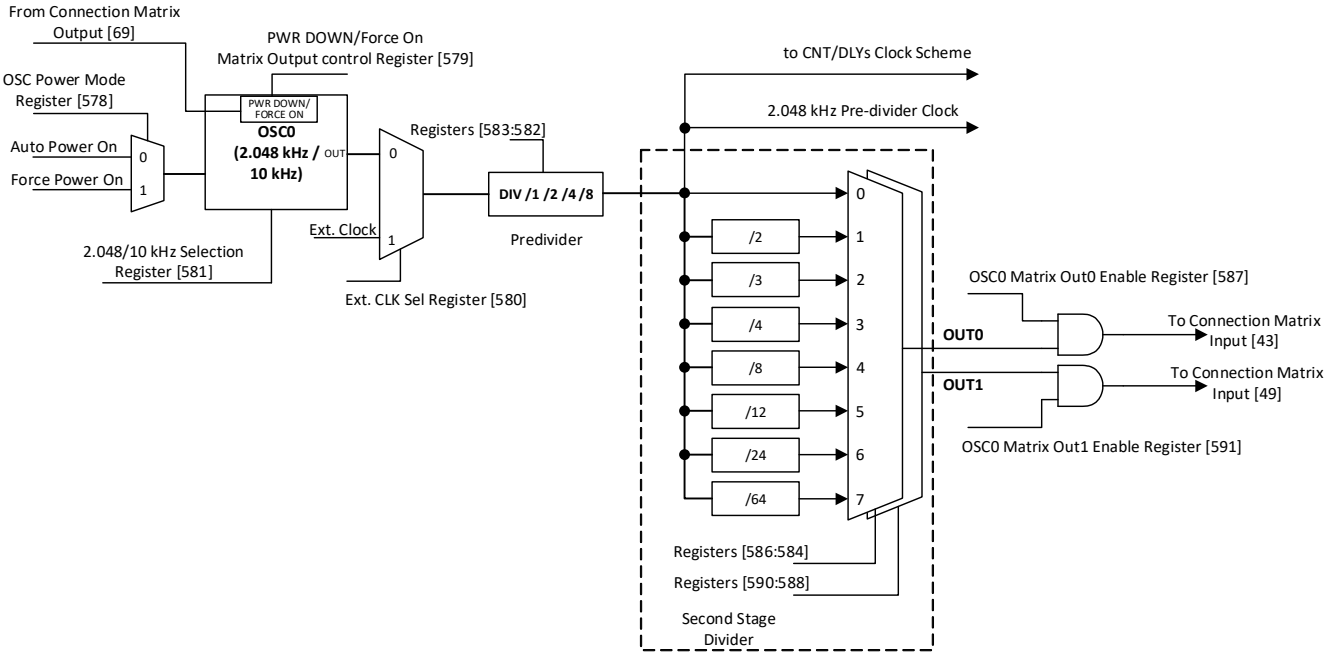


Figure 64: Oscillator0 Block Diagram

13.3 OSCILLATOR1 (25 MHZ)

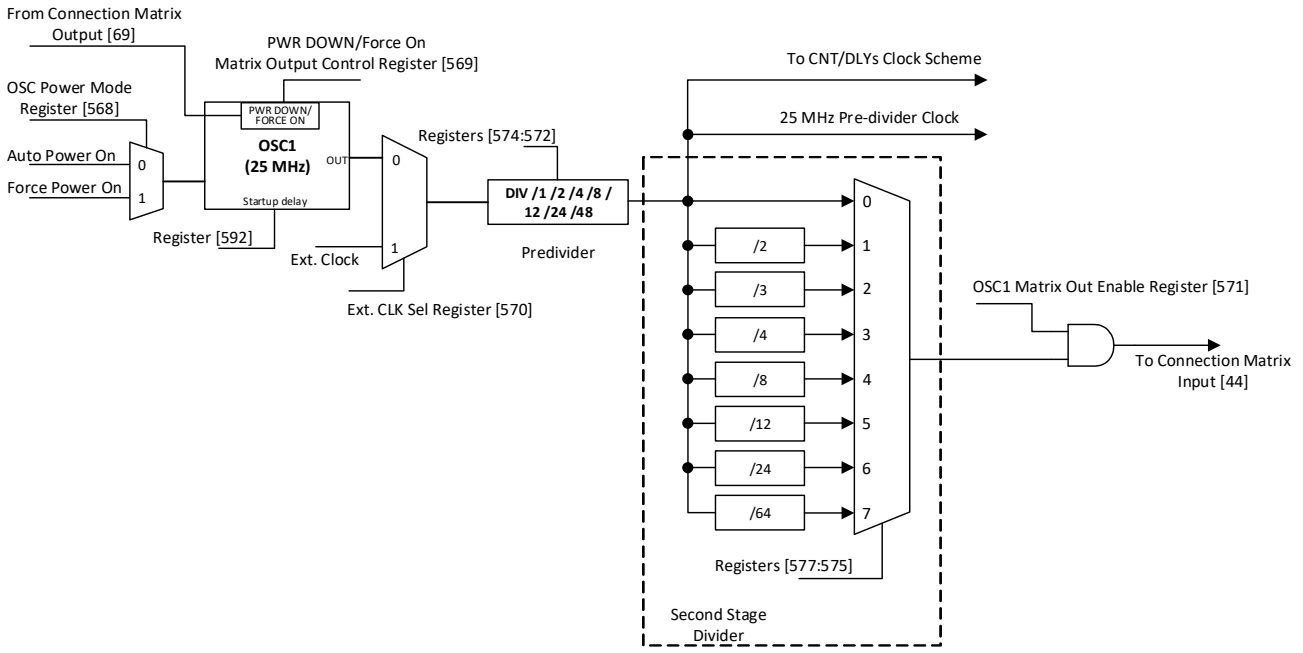


Figure 65: Oscillator1 Block Diagram

13.4 CNT/DLY CLOCK SCHEME

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/12, OSC0/24, OSC0/64, OSC0/512, OSC0/4096
- OSC1/1, OSC1/4, OSC1/8, OSC1/64, OSC1/512

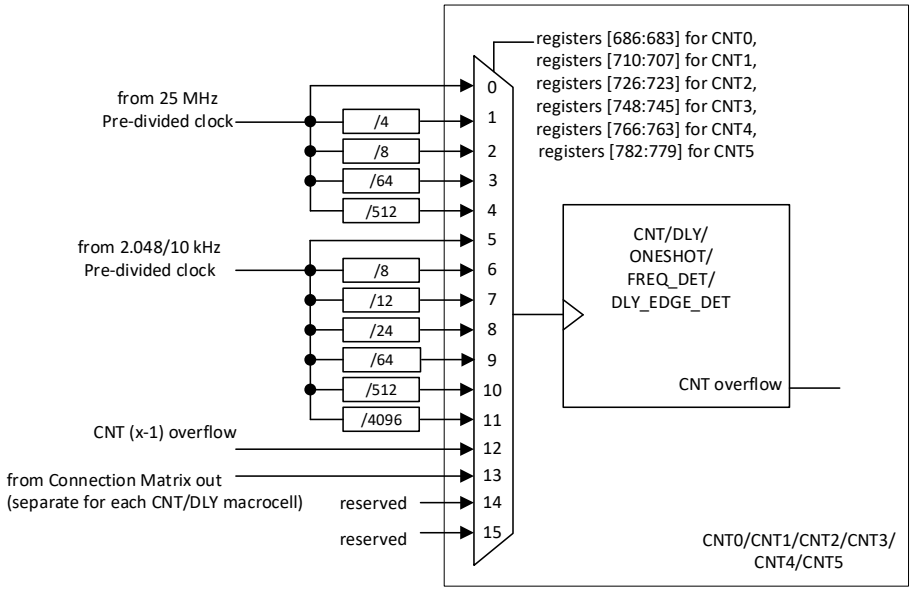


Figure 66: Clock Scheme

13.5 EXTERNAL CLOCKING

The SLG46811 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.5.1 GPI Source for Oscillator0 (2.048kHz/10 kHz)

When register [580] is set to 1, an external clocking signal on GPI will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 64. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

13.5.2 GPIO7 Source for Oscillator1 (25 MHz)

When register [570] is set to 1, an external clocking signal on GPIO7 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 65. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.3 V, 30 MHz at V_{DD} = 3.3 V, 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC1, the oscillator's output signal will be inverted with respect to the GPIO7 input signal.

13.6 OSCILLATORS POWER-ON DELAY

When OSC power mode is "Auto Power-On" "OSC enable" signal appears when any macrocell that uses OSC is powered on (see Figure 67). The values of Power-On Delay are in Table 17.

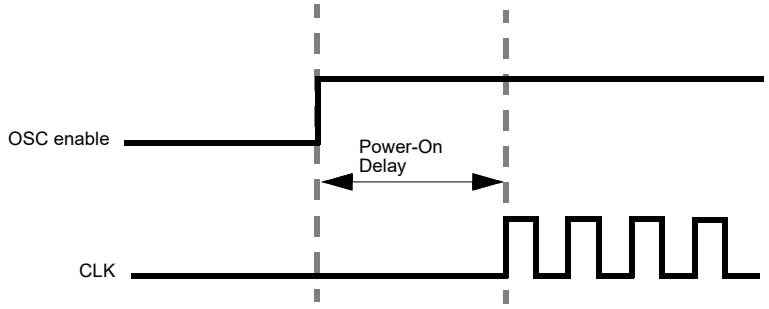


Figure 67: Oscillator Startup Diagram

Note 1 OSC power mode: “Auto Power-On”.

Note 2 “OSC enable” signal appears when any macrocell that uses OSC is powered on.

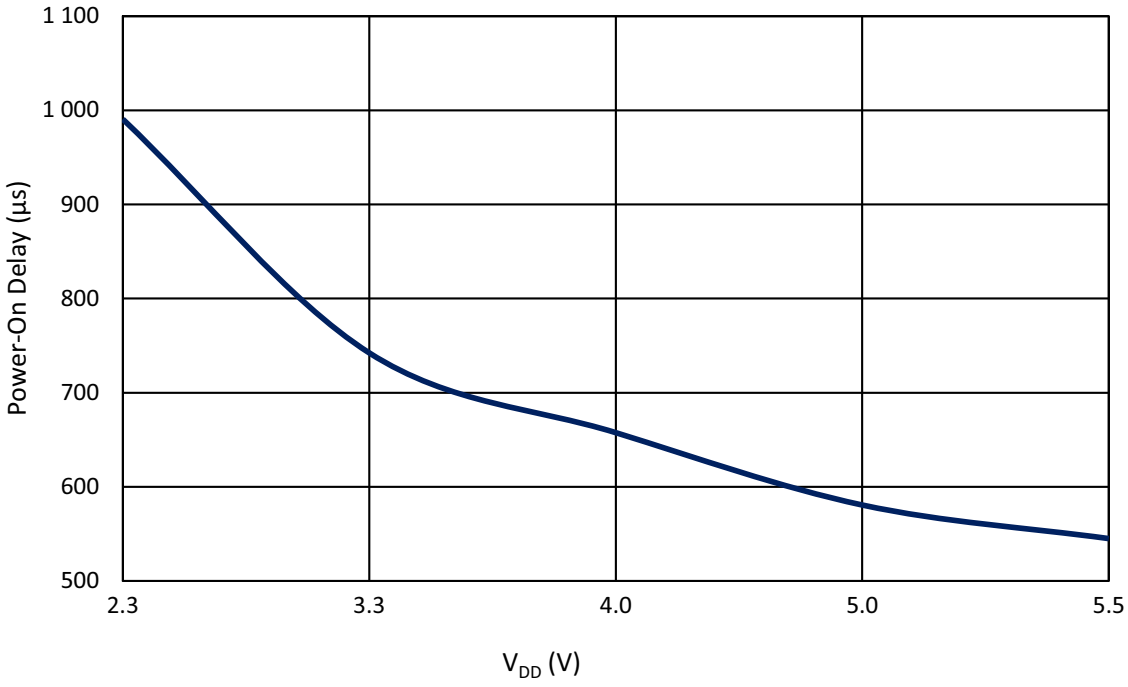


Figure 68: Oscillator0 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 2.048 kHz/10 kHz

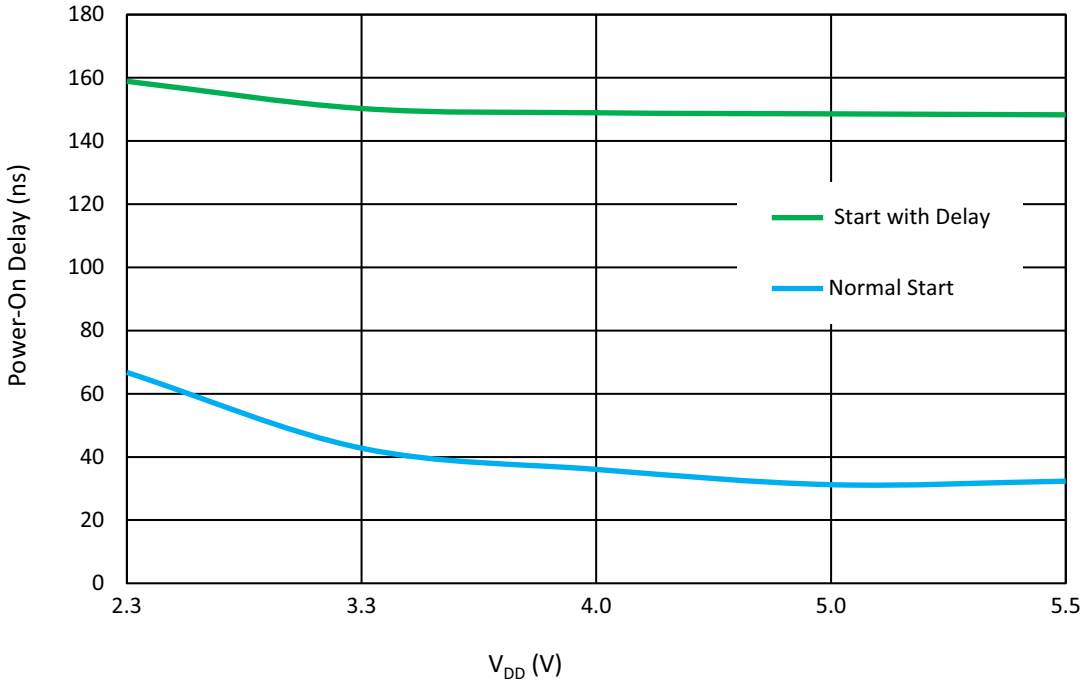


Figure 69: Oscillator1 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC1 = 25 MHz

13.7 OSCILLATORS ACCURACY

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

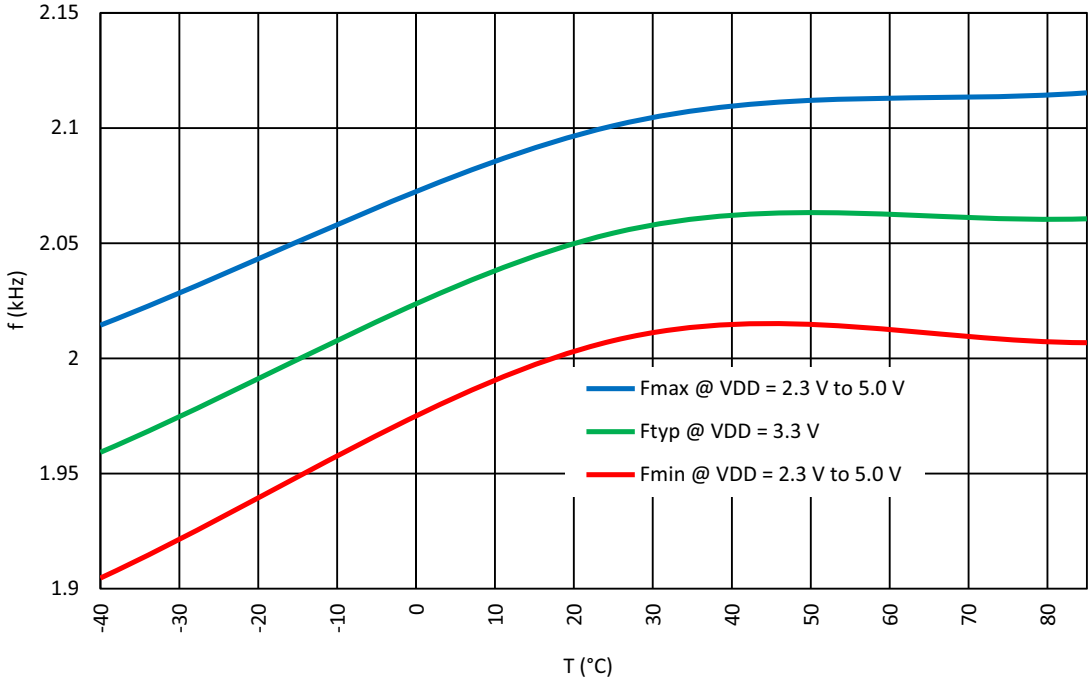


Figure 70: Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz

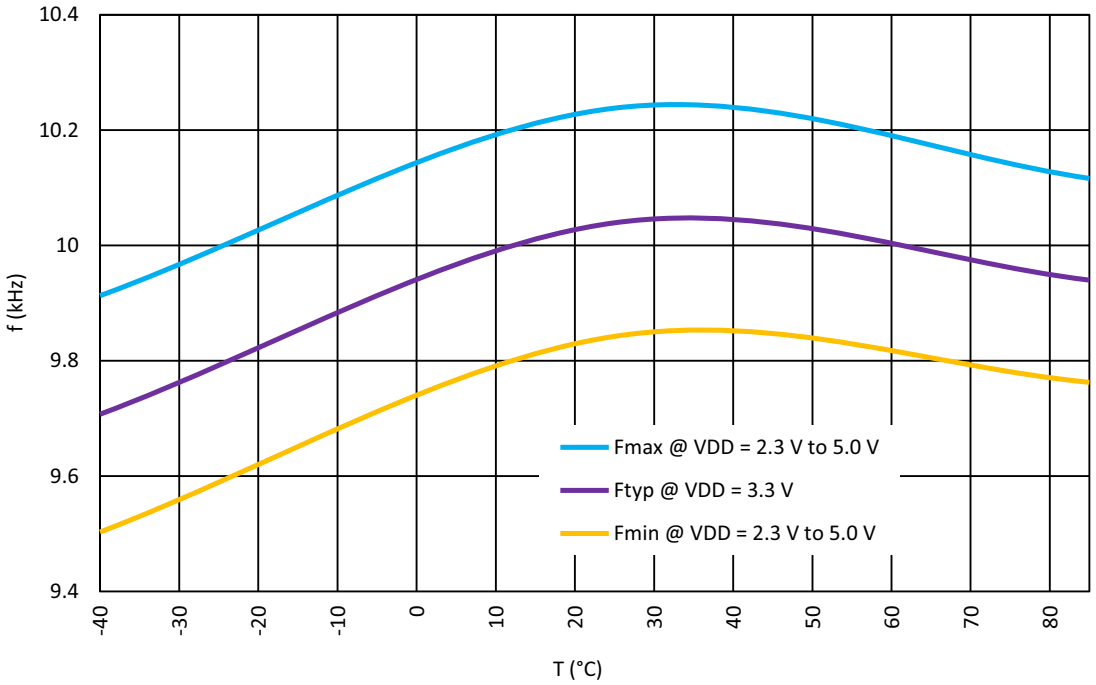


Figure 71: Oscillator0 Frequency vs. Temperature, OSC0 = 10 kHz

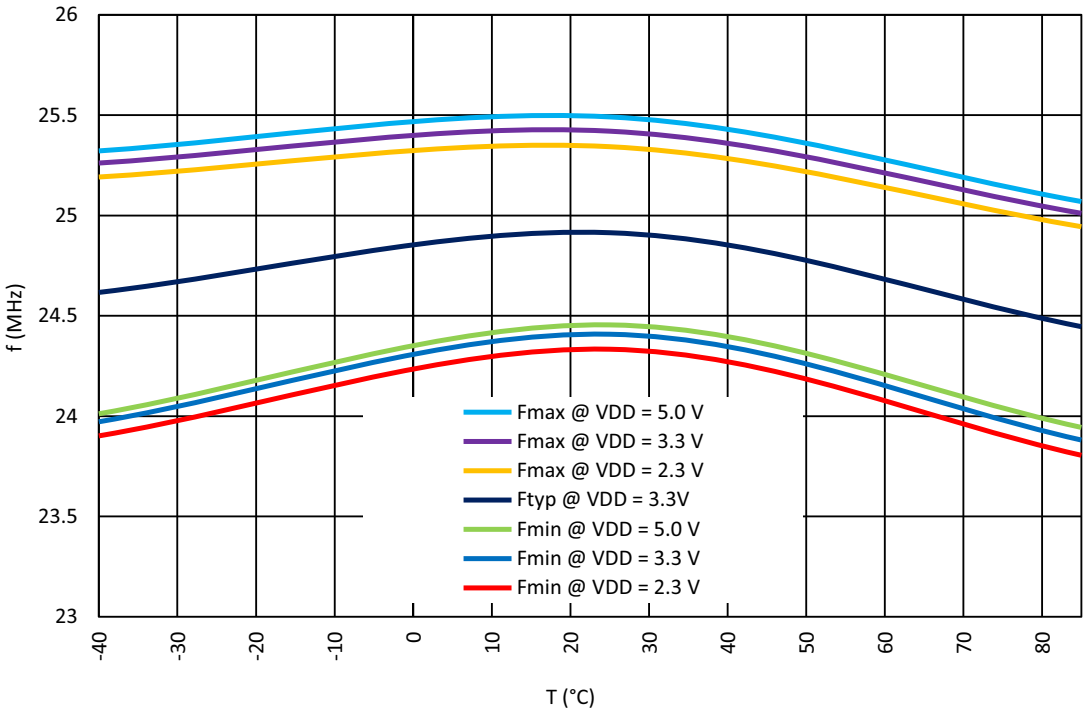


Figure 72: Oscillator1 Frequency vs. Temperature, OSC1 = 25 MHz

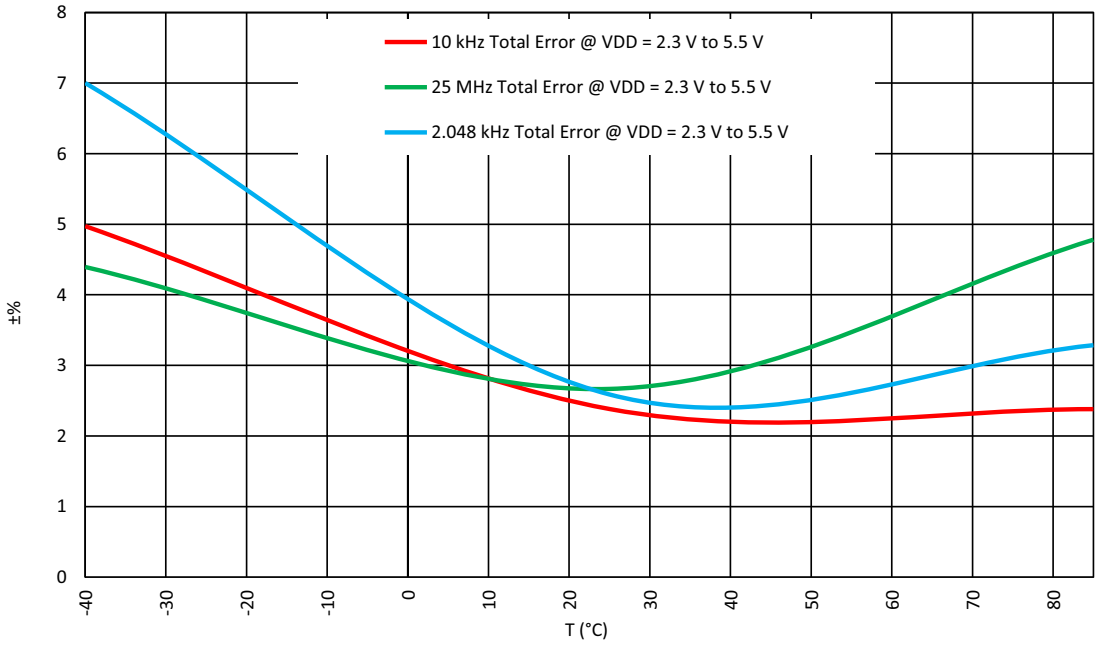


Figure 73: Oscillators Total Error vs. Temperature

Note: For more information see Section 3.9.

13.8 OSCILLATORS SETTLING TIME

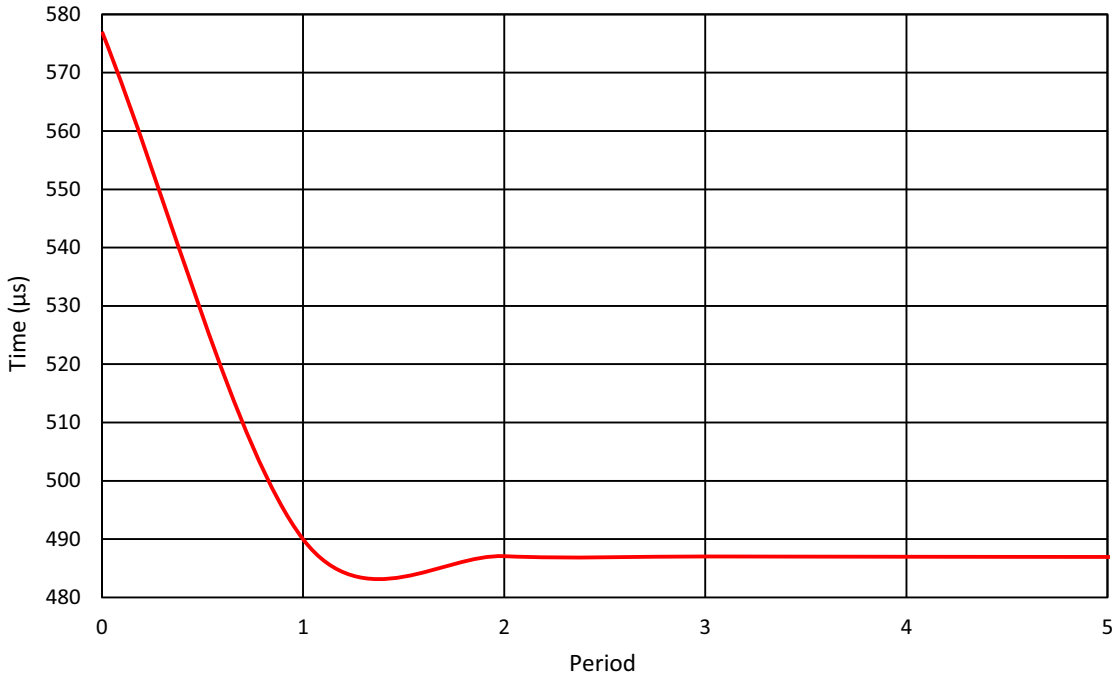


Figure 74: Oscillator0 Settling Time, V_{DD} = 3.3 V, T = 25 °C, OSC0 = 2.048 kHz

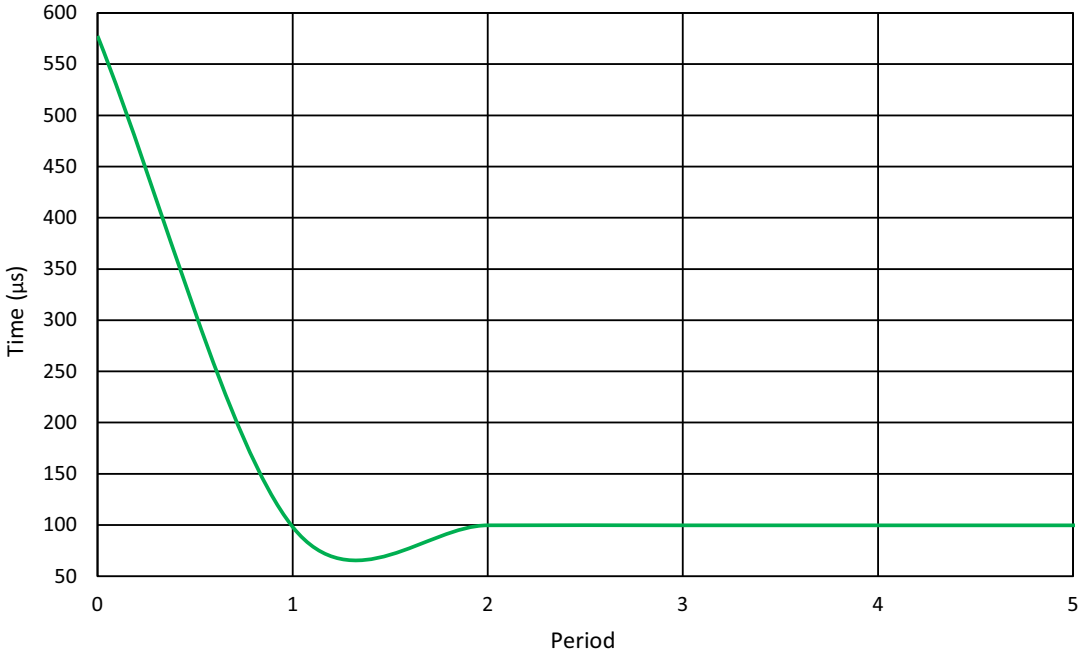


Figure 75: Oscillator0 Settling Time, V_{DD} = 3.3 V, T = 25 °C, OSC0 = 10 kHz

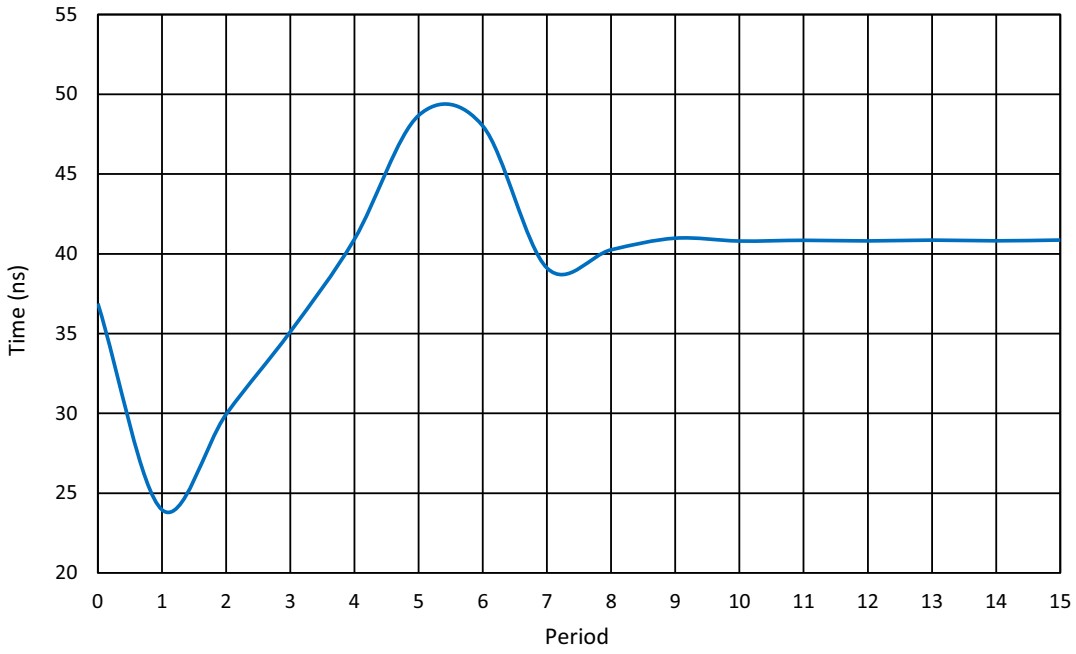


Figure 76: Oscillator1 Settling Time, V_{DD} = 3.3 V, T = 25 °C, OSC1 = 25 MHz (Normal Start)

13.9 OSCILLATORS CURRENT CONSUMPTION

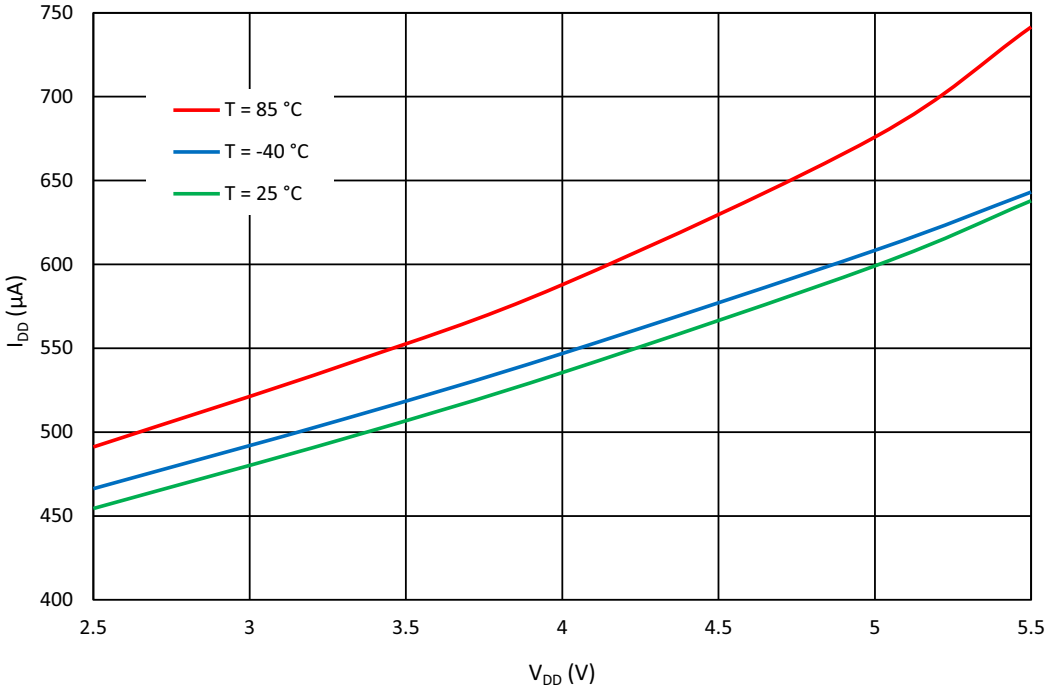


Figure 77: OSC0 Current Consumption vs. V_{DD} (All Pre-Dividers), OSC0 = 2.048 kHz

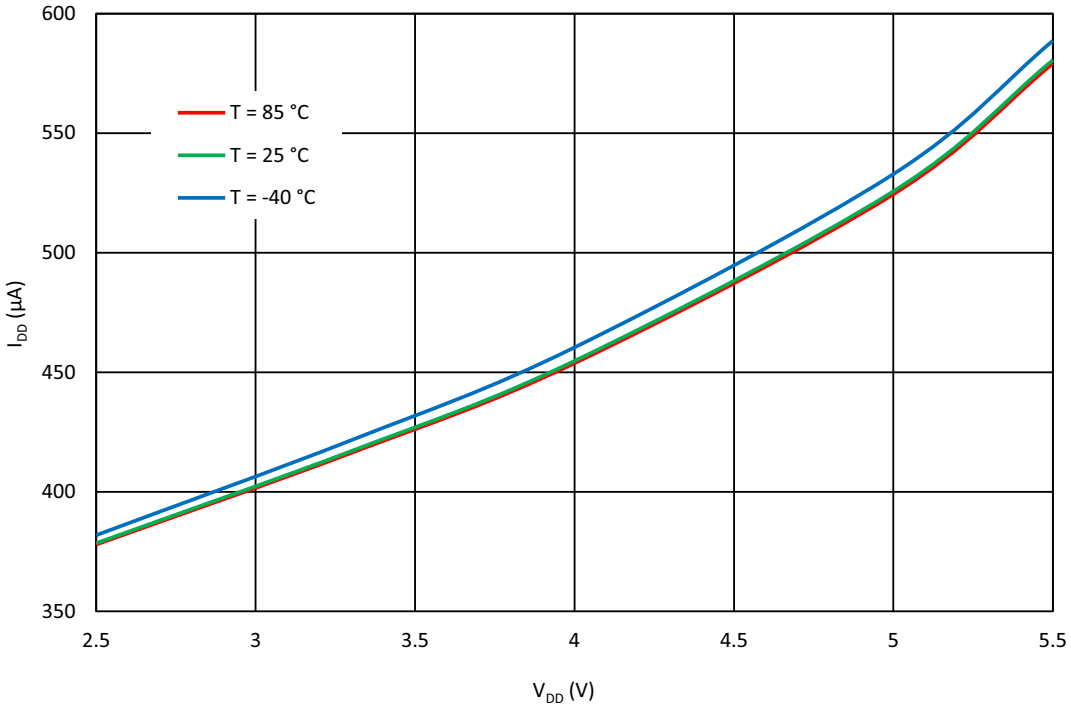


Figure 78: OSC0 Current Consumption vs. V_{DD} (All Pre-Dividers), OSC0 = 10 kHz

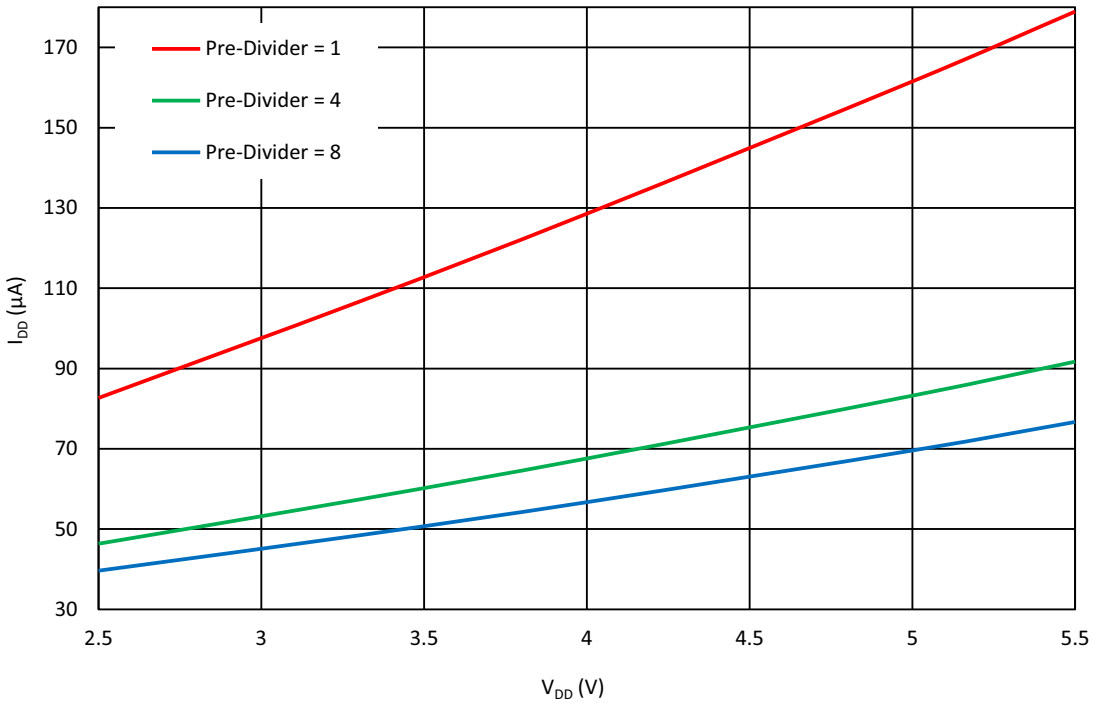


Figure 79: OSC1 Current Consumption vs. V_{DD}, T = -40 °C to 85 °C, OSC1 = 25 MHz

14 Power-On Reset

The SLG46811 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

14.1 GENERAL OPERATION

The SLG46811 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN1) is less than Power-Off Threshold (see in Table 6), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46811, the voltage applied on the V_{DD} should be higher than the Power-On threshold (Note). The full operational V_{DD} range for the SLG46811 is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence has started, the SLG46811 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On threshold is defined in Table 6.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

14.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 80.

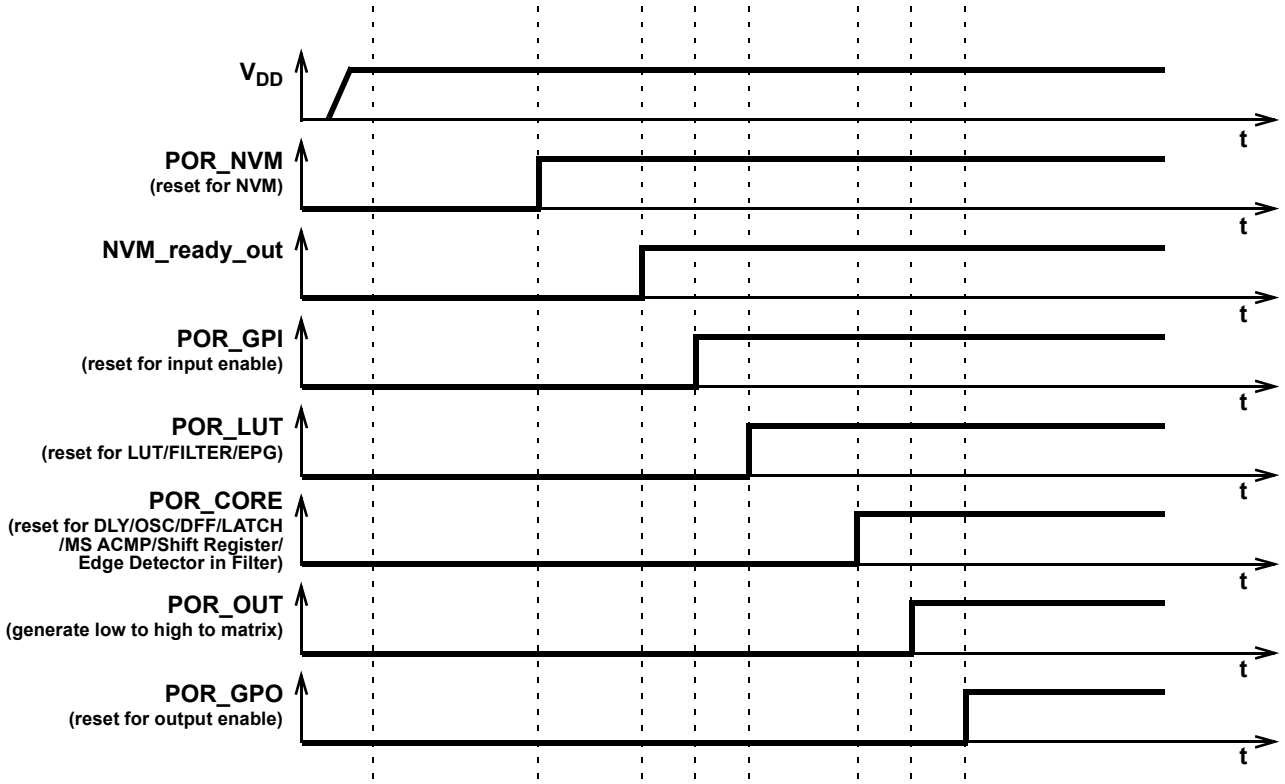


Figure 80: POR Sequence

As can be seen from Figure 80 after the V_{DD} has start ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to a CMOS LATCH that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, OSCs, DFFs, and LATCHES are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

14.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46811 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 81 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P_DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled.

Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

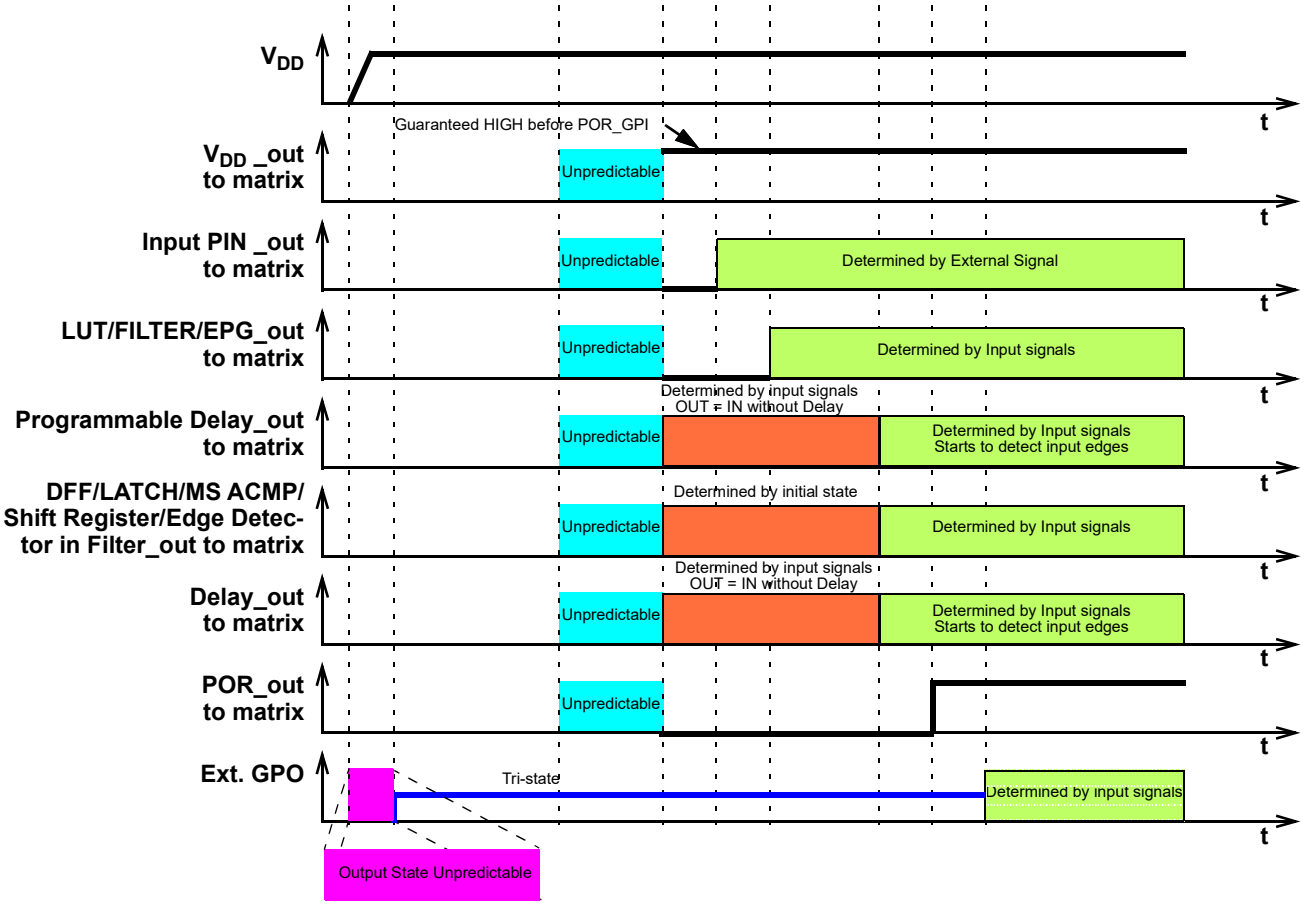


Figure 81: Internal Macrocell States During POR Sequence

14.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.84 V (typical), macrocells in SLG46811 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, ACMP, Pull-up/down.
2. LUTs.
3. DFFs, Delays/Counters.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin →V_{DD} and pin → GND on each pin. So, if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

14.3.2 Power-Down

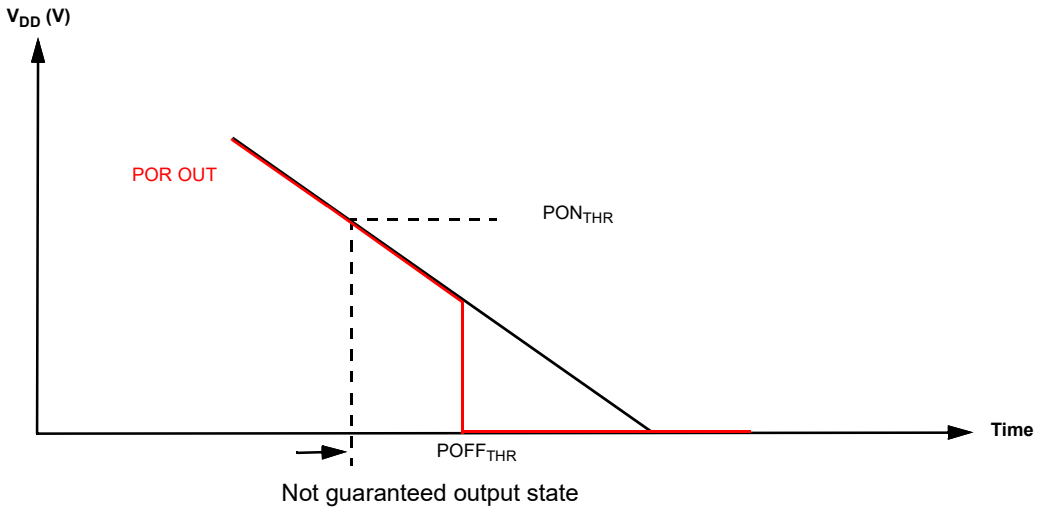


Figure 82: Power-Down

During Power-down, macrocells in SLG46811 are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

15 I²C Serial Communications Macrocell

15.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1119:1117]. See Section 15.5 for more details on I²C read/write memory protection.

15.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 83. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally GPI0, GPIO2, GPIO4, and GPIO5. The LSB of the control code is defined by the value of GPI0, while the MSB is defined by the value of GPIO5. The address source (either register bit or PIN) for each bit in the control code is defined by registers [1179:1176]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to insure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46811 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46811.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 83 shows this basic command structure.

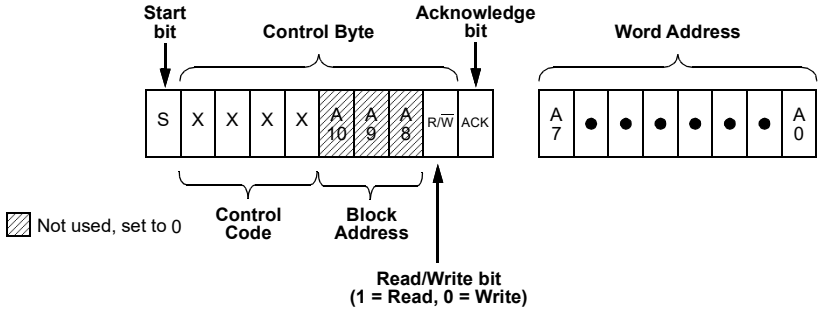


Figure 83: Basic Command Structure

15.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 84. Timing specifications can be found in the AC Characteristics section.

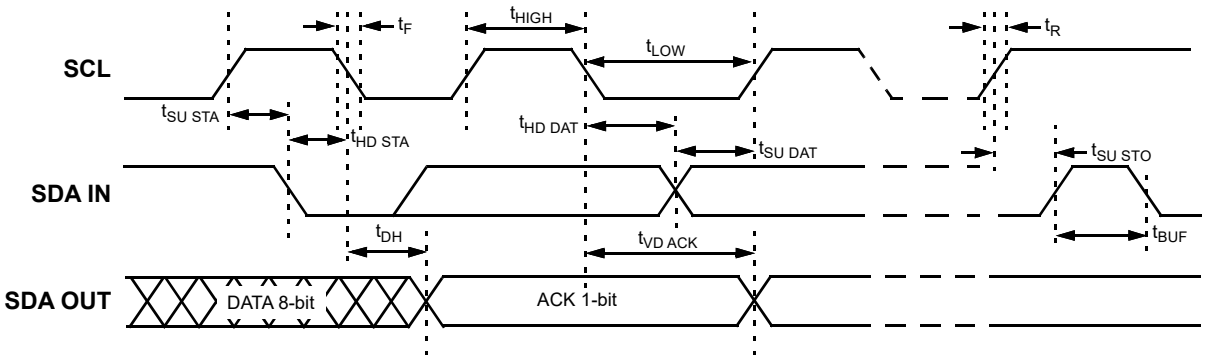


Figure 84: I²C General Timing Characteristics

15.4 I²C SERIAL COMMUNICATIONS COMMANDS

15.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG46811 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46811, where the data byte is to be written. After the SLG46811 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46811 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46811 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1113] = 1 - Enable. It means that IOs will remain their state until the write command is done.

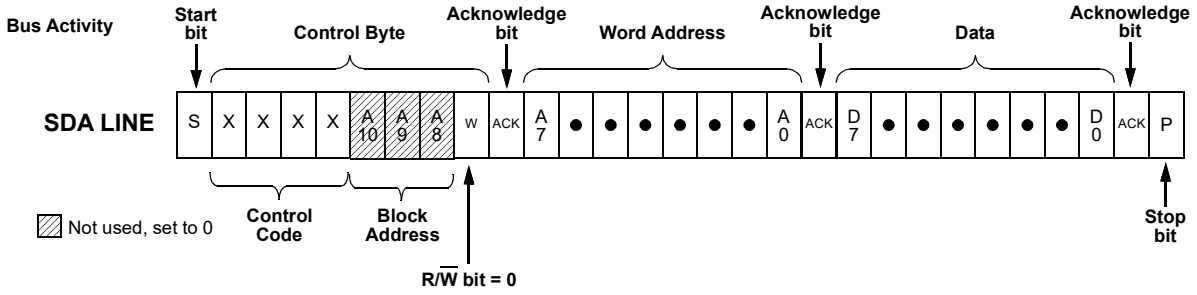


Figure 85: Byte Write Command, R/$\overline{W}$ = 0

15.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG46811 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG46811. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46811 generates the Acknowledge bit.

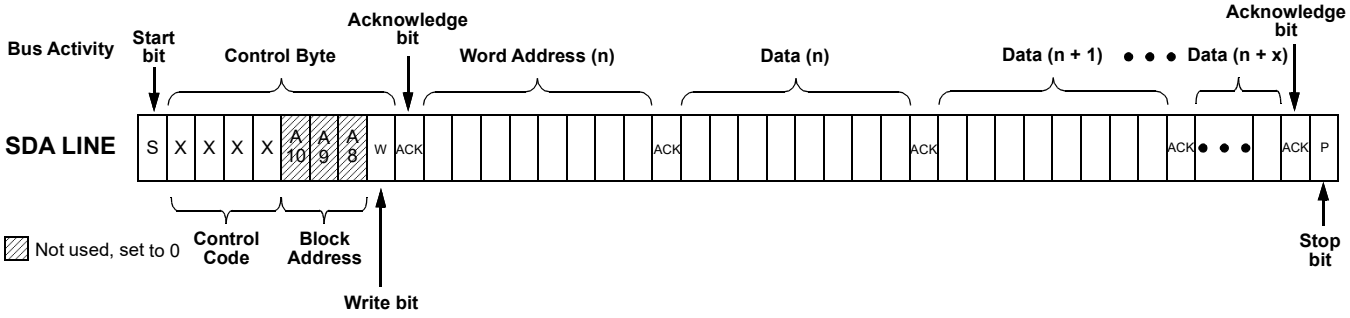


Figure 86: Sequential Write Command

15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG46811 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

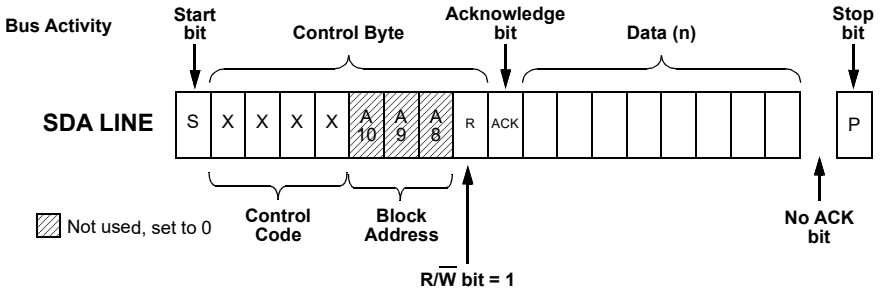


Figure 87: Current Address Read Command, R/$\overline{W}$ = 1

15.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46811 issues an Acknowledge bit, followed by the requested eight data bits.

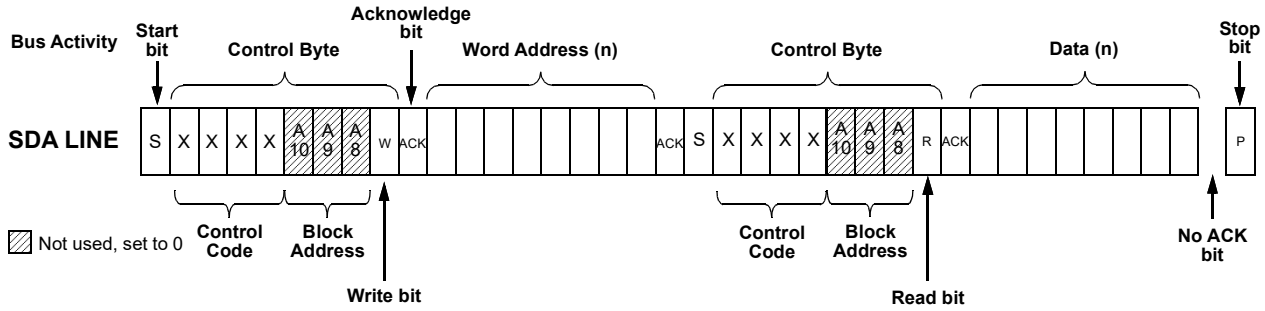


Figure 88: Random Read Command

15.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG46811 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

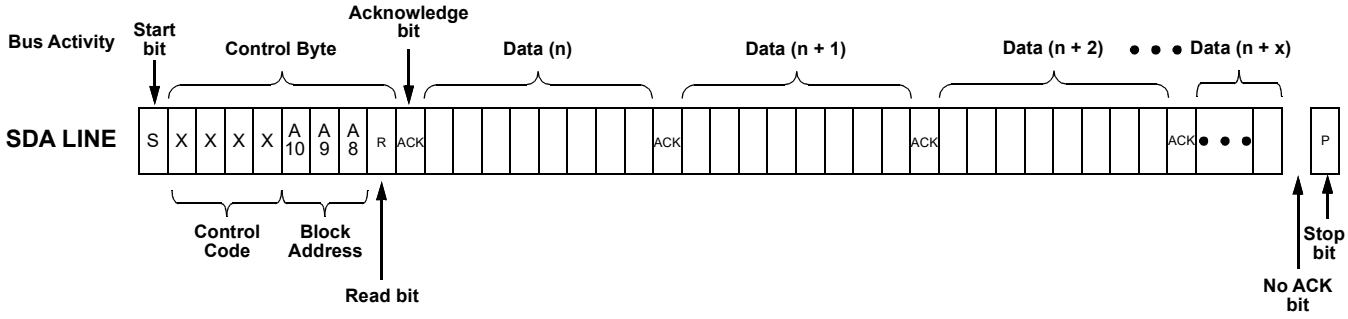


Figure 89: Sequential Read Command

15.4.6 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1112] I²C reset bit to "1", which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1112] will be set to "0" automatically. The Figure 90 illustrates the sequence of events for this reset function.

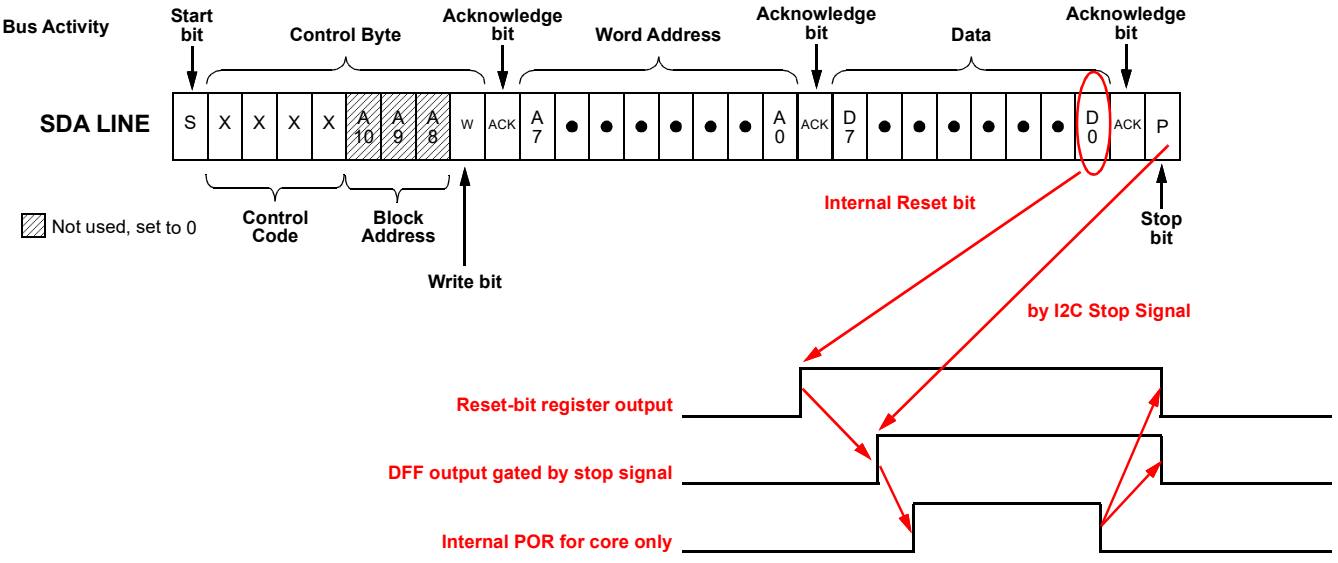


Figure 90: Reset Command Timing

15.5 I²C SERIAL COMMAND REGISTER MAP

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 40 for details.

Table 41: Read/Write Protection Options

Configurations	Protection Modes Configuration							Register Address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write	
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)	
I²C Byte Write Bit Masking (section 15.6.1)	R/W	R/W	R/W	R/W	W	R	-	8C
I²C Serial Reset Command (section 15.4.6)	R/W	R/W	R/W	R/W	R/W	R	R	8B, b'0
Outputs Latching During I²C Write	R/W	R/W	R/W	R/W	R/W	R	R	8B, b'1
Connection Matrix Virtual Inputs (section 6.3)	R/W	R/W	R/W	R/W	W	R	-	39; 3A, b'6~0
Configuration Bits for All Macrocells (IO Pins, ACMPs, Combination Function Macrocells, etc.)	R/W	R/W	W	-	W	R	-	3D~83, 85, 86
Macrocells Inputs Configuration (Connection Matrix Outputs, section 6.2)	R/W	W	W	-	W	R	-	0~35
Protection Mode Enable	R	R	R	R	R	R	R	8B, b'3
Protection Mode Selection	R/W	R	R	R	R	R	R	8B, b'7~5
Macrocells Output Values (Connection Matrix Inputs, section 6.1)	R	R	R	R	-	R	-	36~38; 3A,b'7; 3B; 3C,'b4~0
I²C Control Code (section 15.2)	R	R	R	R	R	R	R	93, b'3~0
Pin Slave Address Select	R	R	R	R	R	R	R	93, b'7~4
I²C Disable/Enable	R	R	R	R	R	R	R	94, b'0
Programming disable	R	R	R	R	R	R	R	94, b'1
Code Compare Enable	R	R	R	R	R	R	R	94, b'2

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as connection matrix, Shift Registers State, and connection matrix virtual inputs. The I^2C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, and others.

See Section 18 for detailed information on all registers.

15.6 I^2C ADDITIONAL OPTIONS

When Output latching during I^2C write, register [1113] = 1 allows all PINs output value to be latched until I^2C write is done. It will protect the output change due to configuration process during I^2C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I^2C write.

If the user sets GPIO0 and GPIO1 function to a selection other than SDA and SCL, all access via I^2C will be disabled.

Note: Any write commands that come to the device via I^2C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section 18 for detailed information on all registers.

15.6.1 I²C Byte Write Bit Masking

The I²C macrocell inside SLG46811 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 15.4.1 for details) on the I²C Byte Write Mask Register (address 0F6H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to "1" in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 91 shows an example of this function.

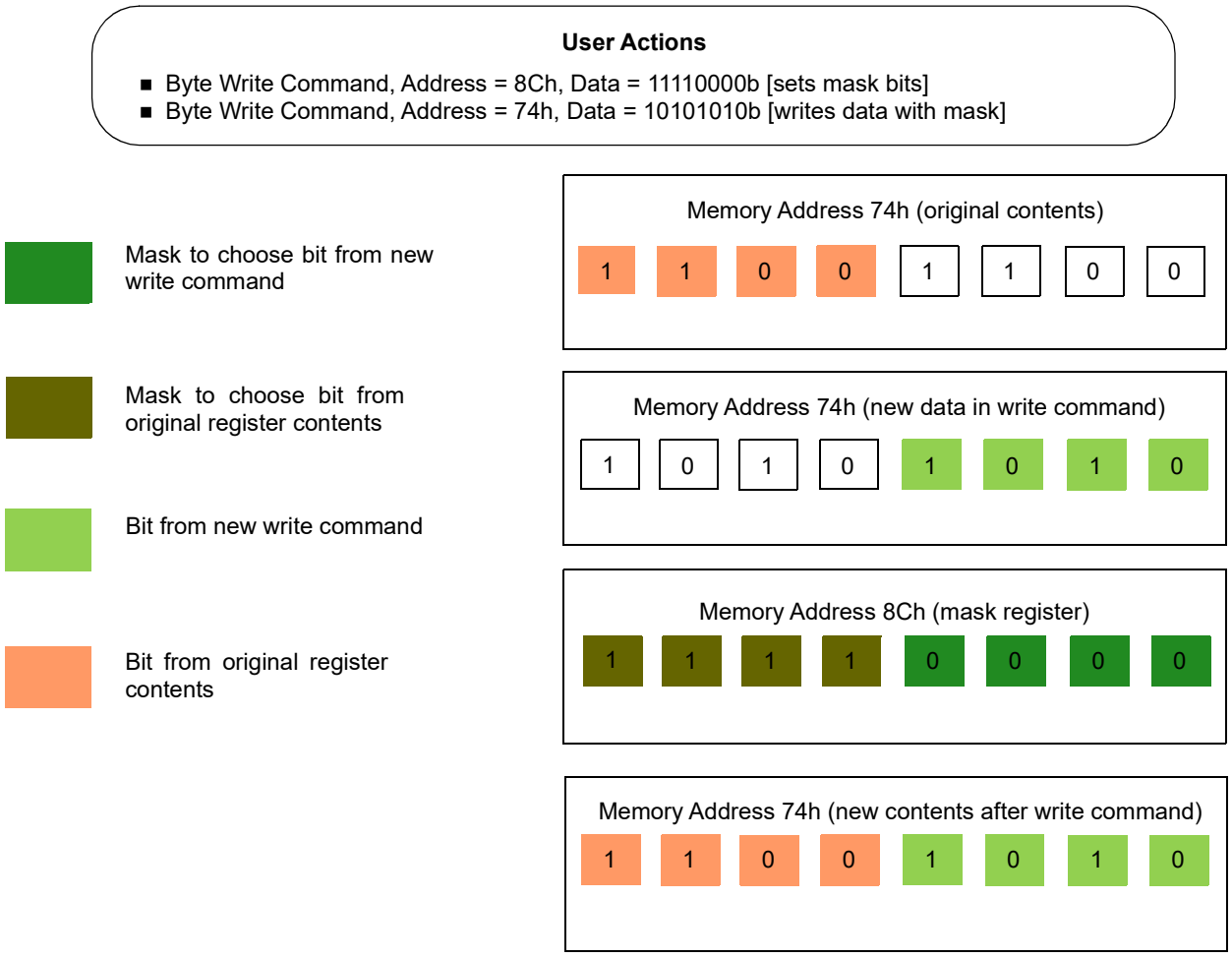


Figure 91: Example of I²C Byte Write Bit Masking

16 Extended Pattern Generator

SLG46811 has an ability to read the data from the part of NVM and to set this data to the matrix inputs. This is done with help of Extended Pattern Generator that shares its output with I²C virtual inputs. Figure 92 shows I²C General block diagram with shared outputs. Registers [1078:1064] define I²C block configuration as Virtual Inputs or Pattern Generator, or GPI.

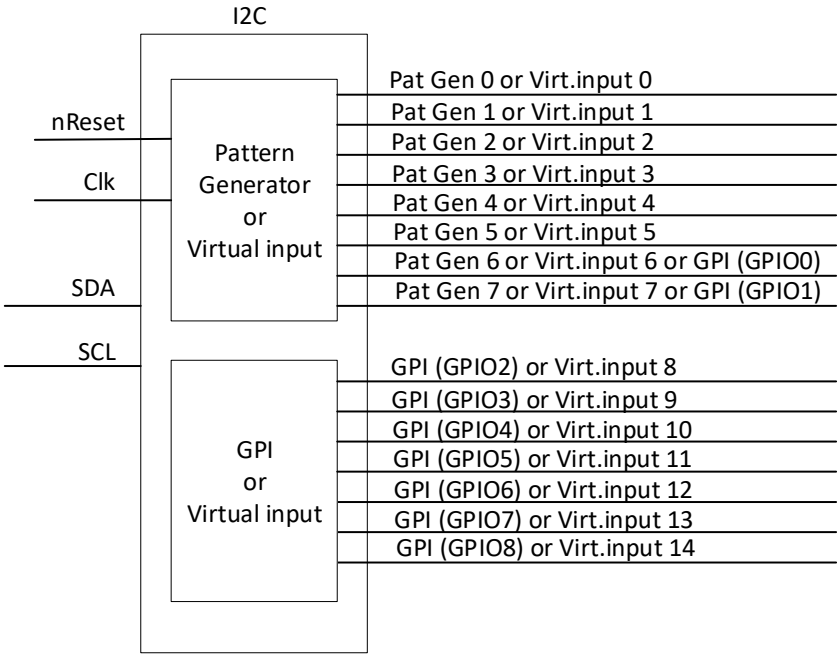


Figure 92: I²C General Block Diagram

Initial value of Extended Pattern Generator is defined by registers [495:488]. This value appears at the output of the macrocell after power up event and after applying low level at nReset input.

Every rising edge at Clk input generator loads byte from the NVM and this data appears at Pattern Generator outputs. The internal NVM pointer increases by 1. At the next rising edge new data from the next NVM byte will be loaded. The range of the data for the Extended Pattern Generator is 92 bytes from the NVM bit [1280] to the NVM bit [2015]. User can select the behavior of the Generator when the internal pointer reaches the last address of the NVM:

- If register [564] = 0, the internal counter will overflow.
- If register [564] = 1, the internal counter will stop when reaching the last byte of the NVM.

The maximum allowable speed of the EPG is 1 MHz.

The minimum duration of the clock pulse low and high level is 100 ns.

Low level at nReset input sets NVM pointer to the beginning and loads the initial value to the outputs.
User can select any of Pattern Generator outputs to operate as Virtual Inputs.

17 Analog Temperature Sensor

The SLG46811 has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. TS output can be selected as a source of MS ACMP channel. The TS is rated to operate over a -40°C to 85°C temperature range. The error in the whole temperature range does not exceed 5.96 %. For more detail refer to section 3.11.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input for V_{DD} = 2.3 V to 5.5 V . It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_T = -4.8xT + 1825.2$$

where:

V_{TS} (mV) - TS Output Voltage.

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis.

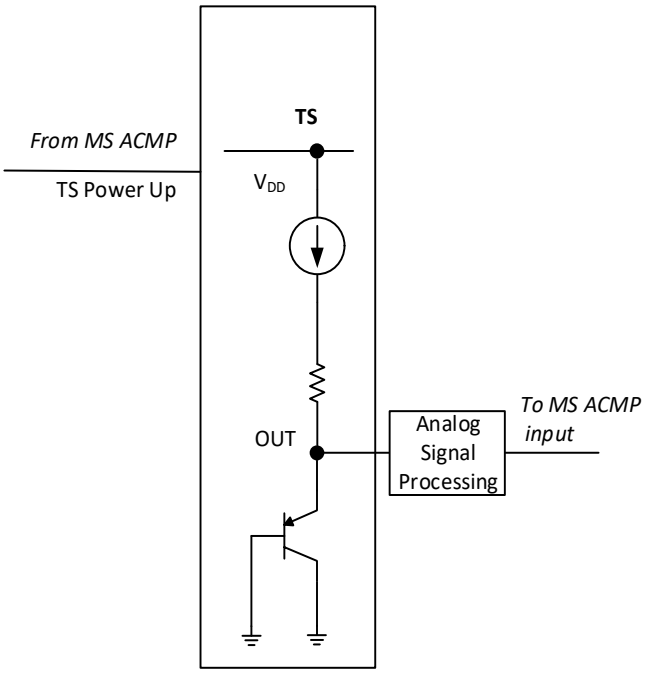


Figure 93: Analog Temperature Sensor Structure Diagram

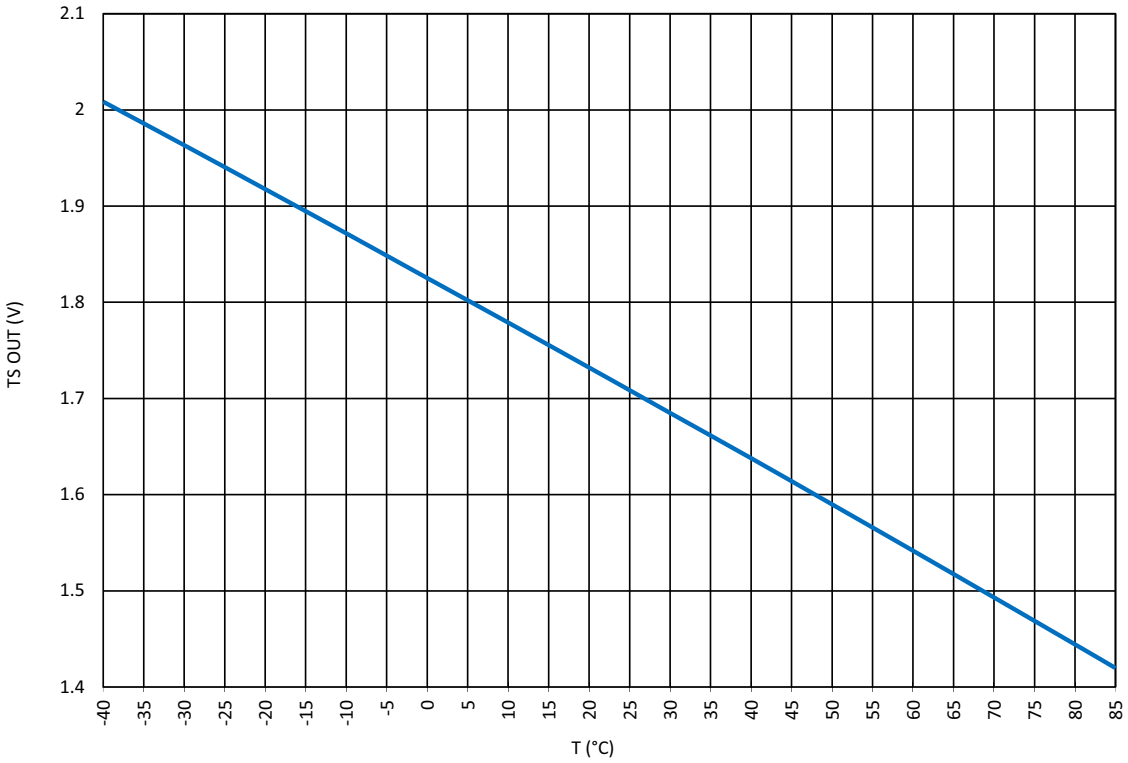


Figure 94: TS Output vs. Temperature, V_{DD} = 2.3 V to 5.5 V

18 Register Definitions

18.1 REGISTER MAP

Table 42: Register Map

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
Matrix Output			
0	0	LUT2_0 & DFF0	OUT0: IN0 of LUT2_0 or Clock Input of DFF0
	1		
	2		
	3		
	4		
	5		
	6		OUT1: IN1 of LUT2_0 or Data Input of DFF0
	7		
1	8		
	9		
	10		
	11		
	12	LUT2_1 & DFF1	OUT2: IN0 of LUT2_1 or Clock Input of DFF1
	13		
	14		
	15		
2	16		
	17		
	18		OUT3: IN1 of LUT2_1 or Data Input of DFF1
	19		
	20		
	21		
	22		
	23		
3	24	LUT2_2 & PGen	OUT4: IN0 of LUT2_2 or Clock Input of PGen
	25		
	26		
	27		
	28		
	29		
	30		OUT5: IN1 of LUT2_2 or RSTB of PGen
	31		
4	32		
	33		
	34		
	35		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
4	36	LUT3_0 & DFF2	OUT6: IN0 of LUT3_0 or CLK Input of DFF2
	37		
	38		
	39		
5	40		OUT7: IN1 of LUT3_0 or Data of DFF2
	41		
	42		
	43		
	44		
	45		
	46		
	47		
6	48		OUT8: IN2 of LUT3_0 or RSTB (SETB) of DFF2
	49		
	50		
	51		
	52		
	53		
	54	LUT3_1 & DFF3	OUT9: IN0 of LUT3_1 or CLK Input of DFF3
	55		
7	56		
	57		
	58		
	59		
	60		OUT10: IN1 of LUT3_1 or Data of DFF3
	61		
	62		
	63		
8	64		
	65		
	66		
	67		OUT11: IN2 of LUT3_1 or RSTB (SETB) of DFF3
	68		
	69		
	70		
	71		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9	72	LUT3_2 & DFF4	OUT12: IN0 of LUT3_2 or CLK Input of DFF4
	73		
	74		
	75		
	76		
	77		
	78		OUT13: IN1 of LUT3_2 or Data of DFF4
	79		
A	80		
	81		
	82		
	83		
	84		OUT14: IN2 of LUT3_2 or RSTB (SETB) of DFF4
	85		
	86		
	87		
B	88		
	89		
	90	LUT3_3 & DFF5	OUT15: IN0 of LUT3_3 or CLK Input of DFF5
	91		
	92		
	93		
	94		
	95		
C	96		OUT16: IN1 of LUT3_3 or Data of DFF5
	97		
	98		
	99		
	100		
	101		
	102		OUT17: IN2 of LUT3_3 or RSTB (SETB) of DFF5
	103		
D	104		
	105		
	106		
	107		
	108	LUT3_4 & DFF6 & SR0	OUT18: IN0 of LUT3_4 or CLK Input of DFF6 or CLK input of SR0
	109		
	110		
	111		
E	112		
	113		
	114		OUT19: IN1 of LUT3_4 or Data Input of DFF6 or Data Input of SR0
	115		
	116		
	117		
	118		
	119		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F	120	LUT3_4 & DFF6 & SR0	OUT20: IN2 of LUT3_4 or RSTB (SETB) of DFF6 or RSTB(SETB) input of SR0
	121		
	122		
	123		
	124		
	125		
	126	LUT3_5 & DFF7 & SR1	OUT21: IN0 of LUT3_5 or CLK Input of DFF7 or CLK input of SR1
	127		
10	128		
	129		
	130		
	131		
	132		OUT22: IN1 of LUT3_5 or Data of DFF7 or Data Input of SR1
	133		
	134		
	135		
11	136		
	137		
	138		OUT23: IN2 of LUT3_5 or RSTB (SETB) of DFF7 or RSTB(SETB) input of SR1
	139		
	140		
	141		
	142		
	143		
12	144	LUT3_6 & DFF8 & SR2	OUT24: IN0 of LUT3_6 or CLK Input of DFF8 or CLK input of SR2
	145		
	146		
	147		
	148		
	149		
	150		OUT25: IN1 of LUT3_6 or Data of DFF8 or Data Input of SR2
	151		
13	152		
	153		
	154		
	155		
	156		OUT26: IN2 of LUT3_6 or RSTB (SETB) of DFF8 or RSTB(SETB) input of SR2
	157		
	158		
	159		
14	160		
	161		
	162	LUT3_7 & DFF9 & SR3	OUT27: IN0 of LUT3_7 or CLK Input of DFF9 or CLK input of SR3
	163		
	164		
	165		
	166		
	167		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
15	168	LUT3_7 & DFF9 & SR3	OUT28: IN1 of LUT3_7 or Data of DFF9 or Data Input of SR3
	169		
	170		
	171		
	172		
	173		
	174		OUT29: IN2 of LUT3_7 or RSTB (SETB) of DFF9 or RSTB(SETB) input of SR3
	175		
16	176		
	177		
	178		
	179		
	180	Multi_function0	OUT30: IN0 of LUT3_8 or CLK Input of DFF10 Delay0 Input (or Counter5 RSTB Input)
	181		
	182		
	183		
17	184		
	185		
	186		
	187		OUT31: IN1 of LUT3_8 or RSTB (SETB) of DFF10 Delay0 Input (or Counter5 RSTB Input)
	188		
	189		
	190		
	191		
18	192		OUT32: IN2 of LUT3_8 or Data of DFF10 Delay0 Input (or Counter5 RSTB Input)
	193		
	194		
	195		
	196		
	197		
	198	Multi_function1	OUT33: IN0 of LUT3_9 or CLK Input of DFF111 Delay1 Input (or Counter1 RSTB Input)
	199		
19	200		
	201		
	202		
	203		
	204		OUT34: IN1 of LUT3_9 or RSTB (SETB) of DFF11 Delay1 Input (or Counter1 RSTB Input)
	205		
	206		
	207		
1A	208		
	209		
	210		
	211		OUT35: IN2 of LUT3_9 or Data of DFF11 Delay1 Input (or Counter1 RSTB Input)
	212		
	213		
	214		
	215		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1B	216	Multi_function2	OUT36: IN0 of LUT3_10 or CLK Input of DFF12 Delay2 Input (or Counter2 RSTB Input)
	217		
	218		
	219		
	220		
	221		
	222		OUT37: IN1 of LUT3_10 or RSTB (SETB) of DFF12 Delay2 Input (or Counter2 RSTB Input)
	223		
1C	224		
	225		
	226		
	227		
	228		OUT38: IN2 of LUT3_10 or Data of DFF12 Delay2 Input (or Counter2 RSTB Input)
	229		
	230		
	231		
1D	232		
	233		
	234	Multi_function3	OUT39: IN0 of LUT3_11 or CLK Input of DFF13 Delay3 Input (or Counter3 RSTB Input)
	235		
	236		
	237		
	238		
	239		
1E	240		OUT40: IN1 of LUT3_11 or RSTB (SETB) of DFF13 Delay3 Input (or Counter3 RSTB Input)
	241		
	242		
	243		
	244		
	245		
	246		OUT41: IN2 of LUT3_11 or Data of DFF13 Delay3 Input (or Counter3 RSTB Input)
	247		
1F	248		
	249		
	250		
	251		
	252	Multi_function4	OUT42: IN0 of LUT3_12 or CLK Input of DFF14 Delay4 Input (or Counter5 RSTB Input)
	253		
	254		
	255		
20	256		
	257		
	258		OUT43: IN1 of LUT3_12 or RSTB (SETB) of DFF14 Delay4 Input (or Counter5 RSTB Input)
	259		
	260		
	261		
	262		
	263		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
21	264	Multi_function4	OUT44: IN2 of LUT3_12 or Data of DFF14 Delay4 Input (or Counter5 RSTB Input)
	265		
	266		
	267		
	268		
	269		
	270	Multi_function5	OUT45: IN0 of LUT3_13 or CLK Input of DFF15 Delay5 Input (or Counter5 RSTB Input)
	271		
22	272		
	273		
	274		
	275		
	276		OUT46: IN1 of LUT3_13 or RSTB (SETB) of DFF15 Delay5 Input (or Counter5 RSTB Input)
	277		
	278		
	279		
23	280		
	281		
	282		
	283		OUT47: IN2 of LUT3_13 or Data of DFF15 Delay5 Input (or Counter5 RSTB Input)
	284		
	285		
	286		
	287		
24	288	LUT4_0_DFF16	OUT48: IN0 of LUT4_0 or CLK Input of DFF16
	289		
	290		
	291		
	292		
	293		
	294		OUT49: IN1 of LUT4_0 or Data of DFF16
	295		
25	296		
	297		
	298		
	299		
	300		OUT50: IN2 of LUT4_0 or RSTB (SETB) of DFF16
	301		
	302		
	303		
26	304		
	305		
	306		OUT51: IN3 of LUT4_0
	307		
	308		
	309		
	310		
	311		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
27	312	Programmable Delay	OUT52: Programmable Delay/Edge Detect Input
	313		
	314		
	315		
	316		
	317		
	318	Filter/Edge Detect	OUT53: Filter/Edge Detect Input
	319		
28	320		
	321		
	322		
	323		
	324	GPIO0	OUT54: GPIO0 DOUT
	325		
	326		
	327		
29	328	GPIO1	OUT55: GPIO1 DOUT
	329		
	330		
	331		
	332		
	333		
	334		
	335		
2A	336	GPIO2	OUT56: GPIO2 DOUT
	337		
	338		
	339		
	340		
	341		
	342		
	343		
2B	344		OUT57: GPIO2 DOUT OE
	345		
	346		
	347		
	348	GPIO3	OUT58: GPIO3 DOUT
	349		
	350		
	351		
2C	352		
	353		
	354		OUT59: GPIO3 DOUT OE
	355		
	356		
	357		
	358		
	359		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
2D	360	GPIO4	OUT60: GPIO4 DOUT
	361		
	362		
	363		
	364		
	365		
	366	GPIO5	OUT61: GPIO5 DOUT
	367		
2E	368		
	369		
	370		
	371		
	372	GPIO6	OUT62: GPIO6 DOUT
	373		
	374		
	375		
2F	376		
	377		
	378	GPIO7	OUT63: GPIO7 DOUT
	379		
	380		
	381		
	382		
	383		
30	384		OUT64: GPIO7 DOUT OE
	385		
	386		
	387		
	388		
	389		
	390	GPIO8	OUT65: GPIO8 DOUT
	391		
31	392		
	393		
	394		
	395		
	396		OUT66: GPIO8 DOUT OE
	397		
	398		
	399		
32	400		
	401		
	402	MS ACMP	OUT67: EN of MS ACMP
	403		
	404		
	405		
	406		
	407		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
33	408	MS ACMP	OUT68: RSTB of ACMP LATs
	409		
	410		
	411		
	412		
	413		
	414	OSC0/1	OUT69: Oscillator Enable/Disable Input
	415		
34	416		
	417		
	418		
	419		
	420	EPG (Embedded Input Pattern Generator)	OUT70: Clock of Pattern Generator
	421		
	422		
	423		
35	424		
	425		
	426		
	427		OUT71: RESETB of Pattern Generator
	428		
	429		
	430		
	431		
36	432	Matrix Input 0	GND
	433	Matrix Input 1	LUT2_0/DFF0 output
	434	Matrix Input 2	LUT2_1/DFF1 output
	435	Matrix Input 3	LUT2_2/PGen output
	436	Matrix Input 4	LUT3_0/DFF2 output
	437	Matrix Input 5	LUT3_1/DFF3 output
	438	Matrix Input 6	LUT3_2/DFF4 output
	439	Matrix Input 7	LUT3_3/DFF5 output
37	440	Matrix Input 8	LUT3_4/DFF6/SR0 output
	441	Matrix Input 9	LUT3_5/DFF7/SR1 output
	442	Matrix Input 10	LUT3_6/DFF8/SR2 output
	443	Matrix Input 11	LUT3_7/DFF9/SR3 output
	444	Matrix Input 12	CNT0 output
	445	Matrix Input 13	MLT0_LUT3_8/DFF10_OUT
	446	Matrix Input 14	CNT1 output
	447	Matrix Input 15	MLT1_LUT3_9/DFF11_OUT
38	448	Matrix Input 16	CNT2 output
	449	Matrix Input 17	MLT2_LUT3_10/DFF12_OUT
	450	Matrix Input 18	CNT3 output
	451	Matrix Input 19	MLT3_LUT3_11/DFF13_OUT
	452	Matrix Input 20	CNT4 output
	453	Matrix Input 21	MLT4_LUT3_12/DFF14_OUT
	454	Matrix Input 22	CNT5 output
	455	Matrix Input 23	MLT5_LUT3_13/DFF15_OUT

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
39	456	Virtual_0 Input	I2C_virtual_0 Input data value
	457	Virtual_1 Input	I2C_virtual_1 Input data value
	458	Virtual_2 Input	I2C_virtual_2_Input data value
	459	Virtual_3 Input	I2C_virtual_3_input data value
	460	Virtual_4 Input	I2C_virtual_4 Input data value
	461	Virtual_5 Input	I2C_virtual_5 Input data value
	462	Virtual_6 Input	I2C_virtual_6 Input data value
	463	Virtual_7 Input	I2C_virtual_7 Input data value
3A	464	Virtual_8 Input	I2C_virtual_8 Input data value
	465	Virtual_9 Input	I2C_virtual_9 Input data value
	466	Virtual_10 Input	I2C_virtual_10 Input data value
	467	Virtual_11 Input	I2C_virtual_11 Input data value
	468	Virtual_12 Input	I2C_virtual_12 Input data value
	469	Virtual_13 Input	I2C_virtual_13 Input data value
	470	Virtual_14 Input	I2C_virtual_14 Input data value
	471	Matrix Input 39	LUT4_0/DFF16 output
3B	472	Matrix Input 40	GPI Digital Input
	473	Matrix Input 41	progdly_edgedet output
	474	Matrix Input 42	edgedet_filter output
	475	Matrix Input 43	OSC0 output 0
	476	Matrix Input 44	OSC1 output
	477	Matrix Input 45	ACMP0 Output
	478	Matrix Input 46	ACMP1 Output
	479	Matrix Input 47	ACMP2 Output
3C	480	Matrix Input 48	ACMP3 Output
	481	Matrix Input 49	OSC0 output 1
	482	Matrix Input 50	ACMP sync mode ready
	483	Matrix Input 51	Reset_core_matrix
	484	Matrix Input 52	V_{DD}
	485	Reserved	
	486	Reserved	
	487	Reserved	
3D	488	EPG (Extended Pattern Generator)	Initial Value at POR & EPG RESETB
	489		
	490		
	491		
	492		
	493		
	494		
	495		
MS ACMP			

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
3E	496	Bandgap power down control	0: always on, 1: power down if no function enable it (ACMP, Vref, TS)
	497	Sampling enable	0: regular mode, 1: multi-channel sampling mode
	498	Edge enable	0: level sensitive mode, 1: edge sensitive mode
	499	Sync enable	0: ACMPs out async, 1: ACMPs out sync
	500	V_{DD} input enable (ACMP positive input selected as V_{DD})	0: disable, 1: enable
	501	Temp sensor enable (ACMP positive input selected as TS)	0: disable, 1: enable
	502	Define the number of sampling channels, NUM[1:0]	00: 1 channel, 01: 2 channels, 10: 3 channels, 11: 4 channels
	503		
3F	504	Define positive input channel on 1st sampling, CHS0[1:0]	00: APIO0, 01: APIO1, 10: APIO2 (or V_{DD} decided by register [500]), 11: APIO3 (or TS decided by register [501])
	505		
	506	Define positive input channel on 2nd sampling, CHS1[1:0]	00: APIO0, 01: APIO1, 10: APIO2 (or V_{DD} decided by register [500]), 11: APIO3 (or TS decided by register [501])
	507		
	508	Define positive input channel on 3rd sampling, CHS2[1:0]	00: APIO0, 01: APIO1, 10: APIO2 (or V_{DD} decided by register [500]), 11: APIO3 (or TS decided by register [501])
	509		
	510	Define positive input channel on 4th sampling, CHS3[1:0]	00: APIO0, 01: APIO1, 10: APIO2 (or V_{DD} decided by register [500]), 11: APIO3 (or TS decided by register [501])
	511		
40	512	ACMP LAT0 RST accessible selection	0: not accessible, 1: accessible
	513	ACMP LAT1 RST accessible selection	0: not accessible, 1: accessible
	514	ACMP LAT2 RST accessible selection	0: not accessible, 1: accessible
	515	ACMP LAT3 RST accessible selection	0: not accessible, 1: accessible
	516	Sampling CK selection	00: div1, 01: div2, 10: div4, 11:div8
	517		
	518	Reserved	
	519	Reserved	

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
41	520	ACMP0 hysteresis	00: 0 mV, 01: 32 mV, 10: 64mV; 11: 192 mV
	521		
	522	ACMP1 hysteresis	00: 0 mV, 01: 32 mV, 10: 64 mV, 11: 192 mV
	523		
	524	ACMP2 hysteresis	00: 0 mV, 01: 32 mV, 10: 64 mV, 11: 192 mV
	525		
	526	ACMP3 hysteresis	00: 0mV, 01: 32 mV, 10: 64 mV, 11: 192 mV
	527		
42	528	ACMP0 Gain Divider	ACMP Gain Divider Select: 00: 1x; 01: 0.5x; 10: 0.33x; 11: 0.25x
	529		
	530	ACMP0 Vref	ACMP Vref Select: 000000: 32 mV ~ 111110: 2.016 V/step = 32 mV; 111111: External Vref
	531		
	532		
	533		
	534		
	535		
43	536	ACMP1 Gain Divider	ACMP Gain Divider Select: 00: 1x; 01: 0.5x; 10: 0.33x; 11: 0.25x
	537		
	538	ACMP1 Vref	ACMP Vref Select: 000000: 32 mV ~ 111110: 2.016 V/ step = 32 mV; 111112: External Vref
	539		
	540		
	541		
	542		
	543		
44	544	ACMP2 Gain Divider	ACMP Gain Divider Select: 00: 1x; 01: 0.5x; 10: 0.33x; 11: 0.25x
	545		
	546	ACMP2 Vref	ACMP Vref Select: 000000: 32 mV ~ 111110: 2.016 V/ step = 32 mV; 111111: External Vref
	547		
	548		
	549		
	550		
	551		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
45	552	ACMP3 Gain Divider	ACMP Gain Divider Select: 00: 1x; 01: 0.5x; 10: 0.33x; 11: 0.25x
	553		
	554	ACMP3 Vref	ACMP Vref Select: 000000: 32 mV ~ 111110: 2.016 V/ step = 32 mV; 111111: External Vref
	555		
	556		
	557		
	558		
	559		
46	560	Reserved	Reserved
	561	Reserved	Reserved
	562	Reserved	Reserved
	563	Reserved	Reserved
	564	EPG	EPG CNT overflow/keep selection 0: overflow to A0, 1: keep at FB
	565	Reserved	Reserved
OSC0/1			
46	566	Oscillator Enable/Disable Input Selection from Matrix Output	00: OSC0 (2kHz/10kHz): Controlled by register OSC1 (25MHz): Controlled by register 01: OSC0 (2kHz/10kHz): Controlled by Matrix Output OSC1 (25MHz): Controlled by register 10: OSC0 (2kHz/10kHz): Controlled by register OSC1 (25MHz): Controlled by Matrix Output 11: OSC0 (2kHz/10kHz): Controlled by Matrix Output OSC1 (25MHz): Controlled by Matrix Output
	567		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
47	568	OSC1 turn on by register	0: auto on by delay cells, 1: always on
	569	Matrix power down or on select	0: matrix down, 1: matrix on
	570	External clock source enable	0: internal OSC1, 1: external clock from GPIO7
	571	Output enable to matrix in 44	0: disable, 1: enable
	572	Pre-divider ratio control	000: /1, 001: /2, 010: /4, 011: /8, 100: /12, 101: /24, 110: /48, 111: N/A
	573		
	574		
	575	Output mux control to matrix in 44	000: /1, 001:/2, 010:/3, 011: /4, 100: /8, 101: /12, 110: /24, 111: /64
48	576		
	577		
	578	OSC0 turn on by register	0: auto on by delay cells 1: always on
	579	Matrix power down or on select	0: matrix down, 1: matrix on
	580	External clock source enable	0: internal OSC0, 1: external clock from GPI
	581	OSC0 frequency selection	0: 2.048 kHz, 1: 10 kHz
	582	Pre-divider ratio control	00: div 1; 01: div 2; 10: div 4; 11: div 8
	583		
49	584	Output mux control to matrix in 43	000: /1, 001:/2, 010:/3, 011: /4, 100: /8, 101: /12, 110: /24, 111: /64
	585		
	586		
	587	Output enable to matrix in 43	0: disable, 1: enable
	588	OSC0 2nd output mux control to matrix in 49	000: /1, 001:/2, 010:/3, 011: /4, 100: /8, 101: /12, 110: /24, 111: /64
	589		
	590		
	591	2nd output enable to matrix in 49	0: disable, 1: enable
4A	592	OSC1 startup delay with 100 ns	0: enable, 1: disable
	593	Reserved	Reserved
	594	IO fast Pull-up/down enable	0: disable, 1: enable
GPI			
4A	595	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: Reserved
	596		
	597	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	598		
	599	Pull-up/down selection	0: Pull-down, 1: Pull-up
GPIO0			

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
4B	600	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: reserved
	601		
	602	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	603		
	604	Pull-up/down selection	0: Pull-down, 1: Pull-up
	605	I^2C mode selection	0: I2C fast mode +, 1: I2C standard/fast mode
	606	Open-drain output enable (3.2x drivability)	0: disable, 1: enable (3.2x)
	607	Reserved	
GPIO1			
4C	608	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: reserved
	609		
	610	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	611		
	612	Pull-up/down selection	0: Pull-down, 1: Pull-up
	613	Open-drain output enable (3.2x drivability)	0: disable, 1: enable (3.2x)
	614	Reserved	
	615	Reserved	
GPIO2			
4D	616	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: reserved
	617		
	618	Output mode configuration	00: Push-Pull 1x, 01: Push-Pull 2x, 10: 1x Open-Drain, 11: 2x Open-Drain
	619		
	620	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	621		
	622	Pull-up/down selection	0: Pull-down, 1: Pull-up
	623	Reserved	
GPIO3			
4E	624	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: analog IO
	625		
	626	Output mode configuration	00: Push-Pull 1x, 01: Push-Pull 2x, 10: 1x Open-Drain, 11: 2x Open-Drain
	627		
	628	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	629		
	630	Pull-up/down selection	0: Pull-down, 1: Pull-up
	631	Reserved	

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
GPIO4			
4F	632	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: analog IO
	633		
	634	Output mode configuration	00: Push-Pull 1x, 01: Push-Pull 2x, 10: 1x Open-Drain, 11: 2x Open-Drain
	635		
	636	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	637		
	638	Pull-up/down selection	0: Pull-down, 1: Pull-up
	639	Input mode/output mode selection	0: input, 1: output
GPIO5			
50	640	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: analog IO
	641		
	642	Output mode configuration	00: Push-Pull 1x, 01: Push-Pull 2x, 10: 1x Open-Drain, 11: 2x Open-Drain
	643		
	644	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	645		
	646	Pull-up/down selection	0: Pull-down, 1: Pull-up
	647	Input mode/output mode selection	0: input, 1: output
GPIO6			
51	648	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: analog IO
	649		
	650	Output mode configuration	00: Push-Pull 1x, 01: Push-Pull 2x, 10: 1x Open-Drain, 11: 2x Open-Drain
	651		
	652	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	653		
	654	Pull-up/down selection	0: Pull-down, 1: Pull-up
	655	Input mode/output mode Selection	0: input, 1: output
GPIO7			
52	656	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: analog IO
	657		
	658	Output mode configuration	00: Push-Pull 1x, 01: Push-Pull 2x, 10: 1x Open-Drain, 11: 2x Open-Drain
	659		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
52	660	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	661		
	662	Pull-up/down selection	0: Pull-down, 1: Pull-up
	663	Analog input enable for ACMP3 IP	0: disable, 1: enable
GPIO8			
53	664	Input mode configuration	00: digital without Schmitt Trigger, 01: digital with Schmitt Trigger, 10: low voltage digital in, 11: Reserved
	665		
	666	Output mode configuration	00: Push-Pull 1x, 01: Push-Pull 2x, 10: 1x Open-Drain, 11: 2x Open-Drain
	667		
	668	Pull-up/down resistance selection	00: floating, 01: 10K, 10: 100K, 11: 1M
	669		
	670	Pull-up/down selection	0: Pull-down, 1: Pull-up
	671	Reserved	
54	676:672	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
54	677	CNT0 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset cnt; 1101: falling edge reset cnt; 1110: rising edge reset cnt; 1111: high level reset cnt
	678		
	679		
55	680		
	681	CNT0 initial value selection	00: bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	682		
	683	DLY/CNT0 Clock Source Select	Clock source sel [3:0] 0000: OSC1(25MHz); 0001: OSC1/4; 0010: OSC1/8; 0011: OSC1/64; 0100: OSC1/512; 0101: OSC0(2K/10KHz); 0110: OSC0/8; 0111: OSC0/12; 1000: OSC0/24; 1001: OSC0/64; 1010: OSC0/512; 1011: OSC0/4096 1100: CNT4_END; 1101: External;
	684		
	685		
	686		
	687	CNT0 output pol selection	0: Default Output, 1: Inverted Output
56	688	CNT0 CNT mode SYNC selection	0: bypass; 1: after two DFF
	689	CNT0 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection (registers [679:677] = 0000/0001/0010)
	690	CNT0 SET/RST Selection	0: Reset to 0 (High CNT output at CNT reset), 1: Set to data (Low CNT output at CNT reset)
	691	FSM0 UP signal SYCN selection	0: bypass; 1: after two DFF
	692	Reserved	
	693	CNT1 output pol selection	0: Default Output, 1: Inverted Output
	694	CNT1 CNT mode SYNC selection	0: bypass; 1: after two DFF
	695	CNT1 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection (register [703:701] = 0000/0001/0010)

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
57	700:696	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	701	CNT1 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset cnt; 1101: falling edge reset cnt; 1110: rising edge reset cnt; 1111: high level reset cnt
	702		
	703		
58	704		
	705	CNT1 initial value selection	00: bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	706		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
58	707	DLY/CNT1 Clock Source Select	Clock source sel [3:0] 0000: OSC1(25MHz); 0001: OSC1/4; 0010: OSC1/8; 0011: OSC1/64; 0100: OSC1/512; 0101: OSC0(2K/10KHz); 0110: OSC0/8; 0111: OSC0/12; 1000: OSC0/24; 1001: OSC0/64; 1010: OSC0/512; 1011: OSC0/4096 1100: CNT4_END; 1101: External;
	708		
	709		
	710		
	711	Reserved	
59	716:712	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
59	717	CNT2 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset cnt; 1101: falling edge reset cnt; 1110: rising edge reset cnt; 1111: high level reset cnt
	718		
	719		
5A	720		
	721	CNT2 initial value selection	00: bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	722		
	723	DLY/CNT2 Clock Source Select	Clock source sel [3:0] 0000: OSC1(25MHz); 0001: OSC1/4; 0010: OSC1/8; 0011: OSC1/64; 0100: OSC1/512; 0101: OSC0(2K/10KHz); 0110: OSC0/8; 0111: OSC0/12; 1000: OSC0/24; 1001: OSC0/64; 1010: OSC0/512; 1011: OSC0/4096; 1100: CNT4_END; 1101:External;
	724		
	725		
	726		
	727	CNT2 output pol selection	0: Default Output, 1: Inverted Output
5B	728	CNT2 CNT mode SYNC selection	0: bypass; 1: after two DFF
	729	CNT2 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection (register [719:717] = 0000/0001/0010)
	730	Reserved	
	731	CNT3 output pol selection	0: Default Output, 1: Inverted Output
	732	CNT3 CNT mode SYNC selection	0: bypass; 1: after two DFF
	733	CNT3 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection (registers [743:742] = 0000/0001/0010)
	734	CNT3 initial value selection	00: bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	735		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
5C	740:736	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	741	CNT3 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset cnt; 1101: falling edge reset cnt; 1110: rising edge reset cnt; 1111: high level reset cnt
	742		
	743		
5D	744		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
5D	745	DLY/CNT3 Clock Source Select	Clock source sel [3:0] 0000: OSC1(25MHz); 0001: OSC1/4; 0010: OSC1/8; 0011: OSC1/64; 0100: OSC1/512; 0101: OSC0 (2K/10KHz); 0110: OSC0/8; 0111: OSC0/12; 1000: OSC0/24; 1001: OSC0/64; 1010: OSC0/512; 1011: OSC0/4096 1100: CNT4_END; 1101:External;
	746		
	747		
	748		
	749	CNT4 output pol selection	0: Default Output, 1: Inverted Output
	750	CNT4 CNT mode SYNC selection	0: bypass; 1: after two DFF
	751	CNT4 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection (registers [759:757] = 0000/0001/0010)
5E	756:752	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
5E	757	CNT4 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset cnt; 1101: falling edge reset cnt; 1110: rising edge reset cnt; 1111: high level reset cnt
	758		
	759		
5F	760		
	761	CNT4 initial value selection	00: bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	762		
	763	DLY/CNT4 Clock Source Select	Clock source sel [3:0] 0000: OSC1(25MHz); 0001: OSC1/4; 0010: OSC1/8; 0011: OSC1/64; 0100: OSC1/512; 0101: OSC0(2K/10KHz); 0110: OSC0/8; 0111: OSC0/12; 1000: OSC0/24; 1001: OSC0/64; 1010: OSC0/512; 1011: OSC0/4096 1100: CNT4_END; 1101: External;
	764		
	765		
	766		
	767	Reserved	
60	772:768	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
60	772:768	CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	773	CNT5 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset cnt; 1101: falling edge reset cnt; 1110: rising edge reset cnt; 1111: high level reset cnt
	774		
	775		
61	776		
	777	CNT5 initial value selection	00: bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	778		
	779	DLY/CNT5 Clock Source Select	Clock source sel [3:0] 0000: OSC1(25MHz); 0001: OSC1/4; 0010: OSC1/8; 0011: OSC1/64; 0100: OSC1/512; 0101: OSC0 (2K/10KHz); 0110: OSC0/8; 0111: OSC0/12; 1000: OSC0/24; 1001: OSC0/64; 1010: OSC0/512; 1011: OSC0/4096 1100: CNT4_END; 1101:External;
	780		
	781		
	782		
	783	CNT5 output pol selection	0: Default Output, 1: Inverted Output
62	784	CNT5 CNT mode SYNC selection	0: bypass; 1: after two DFF
	785	CNT5 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection (registers [775:773] = 0000/0001/0010)
	786	Reserved	Reserved
	787	Reserved	Reserved
	788	Reserved	Reserved
	789	Reserved	Reserved
	790	Reserved	Reserved
	791	Reserved	Reserved

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
63	792 793 794 795 796 797 798 799	Multi0_LUT3_8_DFF10 setting	[7]:LUT3_8 [7]/DFF10 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_8 [6]/DFF10 Output Select 0: Q output, 1: QB output [5]:LUT3_8 [5]/DFF10 0: RSTB from Matrix Output, 1: SETB from Matrix Output [4]:LUT3_8 [4]/DFF10 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_8 [3:0]
64	800 801 802 803 804 805 806 807	REG_CNT0_D[7:0]	Data[7:0]
65	808 809 810 811 812 813 814 815	Multi1_LUT3_9_DFF11 setting	[7]:LUT3_9 [7]/DFF11 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_9 [6]/DFF11 Output Select 0: Q output, 1: QB output [5]:LUT3_9 [5]/DFF11 0: RSTB from Matrix Output, 1: SETB from Matrix Output [4]:LUT3_9 [4]/DFF11 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_9 [3:0]
66	816 817 818 819 820 821 822 823	REG_CNT1_D[7:0]	Data[7:0]
67	824 825 826 827 828 829 830 831	Multi2_LUT3_10_DFF12 setting	[7]:LUT3_10 [7]/DFF12 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_10 [6]/DFF12 Output Select 0: Q output, 1: QB output [5]:LUT3_10 [5]/DFF12 0: RSTB from Matrix Output, 1: SETB from Matrix Output [4]:LUT3_10 [4]/DFF12 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_10 [3:0]
68	832 833 834 835 836 837 838 839	REG_CNT2_D[7:0]	Data[7:0]

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
69	840 841 842 843 844 845 846 847	Multi3_LUT3_11_DFF13 setting	[7]:LUT3_11 [7]/DFF13 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_11 [6]/DFF13 Output Select 0: Q output, 1: QB output [5]:LUT3_11 [5]/DFF13 0: RSTB from Matrix Output, 1: SETB from Matrix Output [4]:LUT3_11 [4]/DFF13 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_11 [3:0]
6A	848 849 850 851 852 853 854 855	REG_CNT3_D[7:0]	Data [7:0]
6B	856 857 858 859 860 861 862 863	Multi4_LUT3_12_DFF14 setting	[7]:LUT3_12 [7]/DFF14 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_12 [6]/DFF14 Output Select 0: Q output, 1: QB output [5]:LUT3_12 [5]/DFF14 0: RSTB from Matrix Output, 1: SETB from Matrix Output [4]:LUT3_12 [4]/DFF14 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_12 [3:0]
6C	864 865 866 867 868 869 870 871	REG_CNT4_D[7:0]	Data [7:0]
6D	872 873 874 875 876 877 878 879	Multi5_LUT3_13_DFF15 setting	[7]:LUT3_13 [7]/DFF15 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_13 [6]/DFF15 Output Select 0: Q output, 1: QB output [5]:LUT3_13 [5]/DFF15 0: RSTB from Matrix Output, 1: SETB from Matrix Output [4]:LUT3_13 [4]/DFF15 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_13 [3:0]
6E	880 881 882 883 884 885 886 887	REG_CNT5_D[7:0]	Data[7:0]

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
6F	888	LUT3_0_DFF2 setting	[7]:LUT3_0 [7]/DFF2 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_0 [6]/DFF2 Output Select 0: Q output, 1: QB output [5]:LUT3_0 [5]/DFF2 Initial Polarity Select 0: Low, 1: High [4]:LUT3_0 [4]/DFF2 stage selection 0: Q of first DFF; 1: Q of second DFF [3]:LUT3_0 [3]/DFF2 0: RSTB from Matrix Output, 1: SETB from Matrix Output [2]:LUT3_0 [2]/DFF2 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [1:0]: LUT3_0 [1:0]
	889		
	890		
	891		
	892		
	893		
	894		
	895		
70	896	LUT3_1_DFF3 setting	[7]:LUT3_1 [7]/DFF3 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_1 [6]/DFF3 Output Select 0: Q output, 1: QB output [5]:LUT3_1 [5]/DFF3 Initial Polarity Select 0: Low, 1: High [4]:LUT3_1 [4]/DFF3 0: RSTB from Matrix Output, 1: SETB from Matrix Output [3]:LUT3_1 [3]/DFF3 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_1 [2:0]
	897		
	898		
	899		
	900		
	901		
	902		
	903		
71	904	LUT3_2_DFF4 setting	[7]:LUT3_2 [7]/DFF4 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_2 [6]/DFF4 Output Select 0: Q output, 1: QB output [5]:LUT3_2 [5]/DFF4 Initial Polarity Select 0: Low, 1: High [4]:LUT3_2 [4]/DFF4 0: RSTB from Matrix Output, 1: SETB from Matrix Output [3]:LUT3_2 [3]/DFF4 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_2 [2:0]
	905		
	906		
	907		
	908		
	909		
	910		
	911		
72	912	LUT3_3_DFF5 setting	[7]:LUT3_3 [7]/DFF5 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_3 [6]/DFF5 Output Select 0: Q output, 1: QB output [5]:LUT3_3 [5]/DFF5 Initial Polarity Select 0: Low, 1: High [4]:LUT3_3 [4]/DFF5 0: RSTB from Matrix Output, 1: SETB from Matrix Output [3]:LUT3_3 [3]/DFF5 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_3 [2:0]
	913		
	914		
	915		
	916		
	917		
	918		
	919		
73	920	LUT3_0 or DFF2 Select	0: LUT3_0, 1: DFF2
	921	LUT3_1 or DFF3 Select	0: LUT3_1, 1: DFF3
	922	LUT3_2 or DFF4 Select	0: LUT3_2, 1: DFF4
	923	LUT3_3 or DFF5 Select	0: LUT3_3, 1: DFF5
	924	Reserved	
	925	Reserved	
	926	Reserved	
	927	LUT4_0 or DFF16 Select	0: LUT4_0, 1: DFF16

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
74	928	LUT4_0_DFF16 setting	[15]:LUT4_0 [15]/DFF16 or LATCH Select 0: DFF function, 1: LATCH function [14]:LUT4_0 [14]/DFF16 Output Select 0: Q output, 1: QB output [13]:LUT4_0 [13]/DFF16 Initial Polarity Select 0: Low, 1: High [12]:LUT4_0 [12]/DFF16 stage selection 0: Q of first DFF; 1 Q of second DFF [11]:LUT4_0 [11]/DFF16 0: RSTB from Matrix Output, 1: SETB from Matrix Output [10]:LUT4_0 [10]/DFF16 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [9:0]: LUT4_0 [9:0]
	929		
	930		
	931		
	932		
	933		
	934		
	935		
75	936		
	937		
	938		
	939		
	940		
	941		
	942		
	943		
76	944	Reserved	
	945	Reserved	
	946	Reserved	
	947	Reserved	
	948	LUT3_4 or DFF6/LATCH6/SR0 selection	0: LUT3_4 1: DFF6/LATCH6/SR0
	949	LUT3_5 or DFF7/LATCH7/SR1 selection	0: LUT3_5 1: DFF7/LATCH7/SR1
	950	LUT3_6 or DFF8/LATCH8/SR2 selection	0: LUT3_6 1: DFF8/LATCH8/SR2
	951	LUT3_7 or DFF9/LATCH9/SR3 selection	0: LUT3_7 1: DFF9/LATCH9/SR3
77	952	DFF6/SR0 setting	[7]:DFF or LATCH Select 0: DFF function, 1: LATCH function [6]:DFF/LATCH/SR/Output polarity select 0: non-inverted output, 1: inverted output [5] Reserved [4]:DFF/LATCH/SR RSTB or SETB selection 0: RSTB from Matrix Output, 1: SETB from Matrix Output [3]:DFF/LATCH/SR Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0] SR Output Select 000: DFF/1st SR output, 001: 2nd SR output 010: 3rd SR output, 011: 4th SR output 100: 5th SR output, 101: 6th SR output 110: 7th SR output, 111: 8th SR output
	953		
	954		
	955		
	956		
	957		
	958		
	959		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
78	960 961 962 963 964 965 966 967	LUT3_4/DFF6/SR0 setting	[7:1]:LUT [7:1] or Shift Register initial value[7:1] [0]:LUT [0] or Shift Register initial value [0] (= DFF/LATCH Initial polarity select) 0: Low, 1: High
79	968 969 970 971 972 973 974 975	DFF7/SR1 setting	[7]:DFF or LATCH Select 0: DFF function, 1: LATCH function [6]:DFF/LATCH/SR/Output polarity select 0: non-inverted output, 1: inverted output [5] Reserved [4]:DFF/LATCH/SR RSTB or SETB selection 0: RSTB from Matrix Output, 1: SETB from Matrix Output [3]:DFF/LATCH/SR Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0] SR Output Select 000: DFF/1st SR output, 001: 2nd SR output 010: 3rd SR output, 011: 4th SR output 100: 5th SR output, 101: 6th SR output 110: 7th SR output, 111: 8th SR output
7A	976 977 978 979 980 981 982 983	LUT3_5/DFF7/SR1 setting	[7:1]:LUT [7:1] or Shift Register initial value[7:1] [0]:LUT [0] or Shift Register initial value [0] (= DFF/LATCH Initial polarity select) 0: Low, 1: High

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
7B	984 985 986 987 988 989 990 991	DFF8/SR2 setting	[7]: DFF or LATCH Select 0: DFF function, 1: LATCH function [6]:DFF/LATCH/SR/Output polarity select 0: non-inverted output, 1: inverted output [5] Reserved [4]:DFF/LATCH/SR RSTB or SETB selection 0: RSTB from Matrix Output, 1: SETB from Matrix Output [3]:DFF/LATCH/SR Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0] SR Output Select 000: DFF/1st SR output, 001: 2nd SR output 010: 3rd SR output, 011: 4th SR output 100: 5th SR output, 101: 6th SR output 110: 7th SR output, 111: 8th SR output
7C	992 993 994 995 996 997 998 999	LUT3_6/DFF8/SR2 setting	[7:1]:LUT [7:1] or Shift Register initial value[7:1] [0]:LUT [0] or Shift Register initial value [0] (= DFF/LATCH Initial polarity select) 0: Low, 1: High
7D	1000 1001 1002 1003 1004 1005 1006 1007	DFF9/SR3 setting	[7]:DFF or LATCH Select 0: DFF function, 1: LATCH function [6]:DFF/LATCH/SR/Output polarity select 0: non-inverted output, 1: inverted output [5] Reserved [4]:DFF/LATCH/SR RSTB or SETB selection 0: RSTB from Matrix Output, 1: SETB from Matrix Output [3]:DFF/LATCH/SR Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0] SR Output Select 000: DFF/1st SR output, 001: 2nd SR output 010: 3rd SR output, 011: 4th SR output 100: 5th SR output, 101: 6th SR output 110: 7th SR output, 111: 8th SR output

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
7E	1008	LUT3_7/DFF9/SR3 setting	[7:1]:LUT [7:1] or Shift Register initial value[7:1] [0]:LUT [0] or Shift Register initial value [0] (= DFF/LATCH Initial polarity select) 0: Low, 1: High
	1009		
	1010		
	1011		
	1012		
	1013		
	1014		
	1015		
7F	1016	LUT2_0/DFF0 setting	[3]:LUT2_0 [3]/DFF0 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_0 [2]/DFF0 Output Select 0: Q output, 1: QB output [1]:LUT2_0 [1]/DFF0 Initial Polarity Select 0: Low, 1: High [0]:LUT2_0 [0]
	1017		
	1018		
	1019		
	1020	LUT2_1/DFF1 setting	[3]:LUT2_1 [3]/DFF1 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_1 [2]/DFF1 Output Select 0: Q output, 1: QB output [1]:LUT2_1 [1]/DFF1 Initial Polarity Select 0: Low, 1: High [0]:LUT2_1 [0]
	1021		
	1022		
	1023		
80	1024	LUT2_0 or DFF0 Select	0: LUT2_0, 1: DFF0
	1025	LUT2_1 or DFF1 Select	0: LUT2_1, 1: DFF1
	1026	LUT2_2 or PGen Select	0: LUT2_3, 1: PGen
	1027	Active level selection for RST/SET for LUT2_2 or PGen	0: Active low level reset/set, 1: Active high level reset/set
	1028	LUT2_2_VAL or PGEN_BIT_NUMBER	LUT2_2[3:0] or PGen BIT NUMBER[3:0]
	1029		
	1030		
	1031		
81	1032	PGen data	PGen Data [15:0]
	1033		
	1034		
	1035		
	1036		
	1037		
	1038		
	1039		
82	1040		
	1041		
	1042		
	1043		
	1044		
	1045		
	1046		
	1047		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
83	1048	Filter or Edge Detector Selection	0, filter, 1, edge det
	1049	Output Polarity Select	0: output non-invert, 1: output invert
	1050	Select the edge mode	00: Rising Edges Det 01: Falling Edge Det 10: Both Edge Det 11: Both Edge DLY
	1051		
	1052	Delay Value Select for Programmable Delay & Edge Detector	00: 125 ns, 01: 250 ns, 10: 375 ns, 11: 500 ns
	1053		
	1054	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector, 01: Falling Edge Detector, 10: Both Edge Detector, 11: Both Edge Delay
	1055		
84	1056	Reserved	Reserved
	1057	Reserved	Reserved
	1058	Reserved	Reserved
	1059	Reserved	Reserved
	1060	Reserved	Reserved
	1061		
	1062		
	1063		
Matrix Virtual Data			
85	1064	Pat Gen 0/I^{2}C_virtual input [0] select	0: matrix in 24 select Pat Gen 0 1: matrix in 24 select I^{2}C_virtual Input [0]
	1065	Pat Gen 1/I2C_virtual input [1] digital input select	0: matrix in 25 select Pat Gen 1 1: matrix in 25 select I^{2}C_virtual Input [1]
	1066	Pat Gen 2/I2C_virtual input [2] digital input select	0: matrix in 26 select Pat Gen 2 1: matrix in 26 select I^{2}C_virtual Input [2]
	1067	Pat Gen 3/I2C_virtual input [3] digital input select	0: matrix in 27 select Pat Gen 3 1: matrix in 27 select I^{2}C_virtual Input [3]
	1068	Pat Gen 4/I2C_virtual input [4] digital input select	0: matrix in 28 select Pat Gen 4 1: matrix in 28 select I^{2}C_virtual Input [4]
	1069	Pat Gen 5/I2C_virtual input [5] digital input select	0: matrix in 28 select Pat Gen 5 1: matrix in 29 select I^{2}C_virtual Input [5]
	1070	Pat Gen 6/I^{2}C_virtual input [6] digital input select	0: matrix in 30 select Pat Gen 6 1: matrix in 30 select I^{2}C_virtual Input [6] or GPIO0 (at non-i2c mode)
	1071	Pat Gen 7/I^{2}C_virtual input [7] digital input select	0: matrix in 31 select Pat Gen 7 1: matrix in 31 select I^{2}C_virtual Input [7] or GPIO1 (at non-i2c mode)

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
86	1072	GPIO2/I²C_virtual input [8] select	0: matrix in 32 select GPIO2 digital input (GPIO2) 1: matrix in 32 select I²C_virtual Input [8]
	1073	GPIO3 /I²C_virtual input [9] digital input select	0: matrix in 33 select GPIO3 digital input (GPIO3) 1: matrix in 33 select I²C_virtual Input [9]
	1074	GPIO4/I²C_virtual input [10] digital input select	0: matrix in 34 select GPIO4 digital input (GPIO4) 1: matrix in 34 select I²C_virtual Input [10]
	1075	GPIO5/I²C_virtual input [11] digital input select	0: matrix in 35 select GPIO5 digital input (GPIO5) 1: matrix in 35 select I²C_virtual Input [11]
	1076	GPIO6/I²C_virtual input [12] digital input select	0: matrix in 36 select GPIO6 digital input (GPIO6) 1: matrix in 36 select I²C_virtual Input [12]
	1077	GPIO7/I²C_virtual input [13] digital input select	0: matrix in 37 select GPIO7 digital input (GPIO7) 1: matrix in 37 select I²C_virtual Input [13]
	1078	GPIO8/I²C_virtual input [14] digital input select	0: matrix in 38 select GPIO8 digital input (GPIO8) 1: matrix in 38 select I²C_virtual Input [14]
	1079	Reserved	Reserved
87	1080	Reserved	
	1081	Reserved	
	1082	Reserved	
	1083	Reserved	
	1084	Reserved	
	1085	Reserved	
	1086	Reserved	
	1087	Reserved	
88	1088	Reserved	
	1089	Reserved	
	1090	Reserved	
	1091	Reserved	
	1092	Reserved	
	1093	Reserved	
	1094	Reserved	
	1095	Reserved	
89	1096	Reserved	
	1097	Reserved	
	1098	Reserved	
	1099	Reserved	
	1100	Reserved	
	1101	Reserved	
	1102	Reserved	
	1103	Reserved	
8A	1104	Reserved	
	1105	Reserved	
	1106	Reserved	
	1107	Reserved	
	1108	Reserved	
	1109	Reserved	
	1110	Reserved	
	1111	Reserved	

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
8B	1112	I2C reset bit with reloading NVM into Data register (soft reset)	0: Keep existing condition, 1: Reset execution
	1113	IO Latching Enable During I2C Write Interface	0: Disable, 1: Enable
	1114	Reserved	
	1115	Reserved	
	1116	Reserved	
	1117	Reserved	
	1118	Reserved	
	1119	Reserved	
8C	1120	I^2C write mask bits	1: mask, 0: overwrite
	1121		
	1122		
	1123		
	1124		
	1125		
	1126		
	1127		
8D	1128	Reserved	
	1129	Reserved	
	1130	Reserved	
	1131	Reserved	
	1132	Testmode EPG	0: partial OTP read (A0 to FB) 1: all OTP read (00 to FF)
	1133	Reserved	
	1134	Reserved	
	1135	Reserved	
8E	1136	Reserved	
	1137	Reserved	
	1138	Reserved	
	1139	Reserved	
	1140	Reserved	
	1141	Reserved	
	1142	Reserved	
	1143	Reserved	
8F	1144	Reserved	
	1145	Reserved	
	1146	Reserved	
	1147	Reserved	
	1148	Reserved	
	1149	Reserved	
	1150	Reserved	
	1151	Reserved	

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
90	1152	Reserved	
	1153	Reserved	
	1154	Reserved	
	1155	Reserved	
	1156	Reserved	
	1157	Reserved	
	1158	Reserved	
	1159	Reserved	
91	1160	Reserved	
	1161	Reserved	
	1162	Reserved	
	1163	Reserved	
	1164	Reserved	
	1165	Reserved	
	1166	Reserved	
	1167	Reserved	
92	1168	Reserved	
	1169	Reserved	
	1170	Reserved	
	1171	Reserved	
	1172	Reserved	
	1173	Reserved	
	1174	Reserved	
	1175	Reserved	
93	1176	I^2C slave address	
	1177		
	1178		
	1179		
	1180	Slave address selection bit0	0: from register [1176], 1: from GPI
	1181	Slave address selection bit1	0: from register [1177], 1: from GPIO3
	1182	Slave address selection bit2	0: from register [1178], 1: from GPIO4
	1183	Slave address selection bit3	0: from register [1179], 1: from GPIO7
94	1184	I^2C operation disable bit	0: I2C operation enable; matrix in 26(27) select I^2C_virtual_0(1) Input 1: I^2C operation disable; matrix in 26(27) select GPIO3(4) digital input
	1185	Reserved	
	1186	Reserved	
	1187	Reserved	
	1188	Reserved	
	1189	Reserved	
	1190	Reserved	
	1191	Reserved	

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
95	1192	Reserved	
	1193	Reserved	
	1194	Reserved	
	1195	Reserved	
	1196	Reserved	
	1197	Reserved	
	1198	Reserved	
	1199	Reserved	
96	1200	Reserved	
	1201		
	1202		
	1203		
	1204		
	1205		
	1206		
	1207		
97	1208	Reserved	
	1209		
	1210		
	1211		
	1212		
	1213		
	1214		
	1215		
98	1216	Reserved	
	1217		
	1218		
	1219		
	1220		
	1221		
	1222		
	1223		
99	1224	Reserved	
	1225	Reserved	
	1226	Reserved	
	1227	Reserved	
	1228	Reserved	
	1229	Reserved	
	1230	Reserved	
	1231	Reserved	
9A	1232	Reserved	
	1233	Reserved	
	1234	Reserved	
	1235	Reserved	
	1236	Reserved	
	1237	Reserved	
	1238	Reserved	
	1239	Reserved	

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9B	1240	Reserved	
	1241	Reserved	
	1242	Reserved	
	1243	Reserved	
	1244	Reserved	
	1245	Reserved	
	1246	Reserved	
	1247	Reserved	
9C	1248	Reserved	
	1249	Reserved	
	1250	Reserved	
	1251	Reserved	
	1252	Reserved	
	1253	Reserved	
	1254	Reserved	
	1255	Reserved	
9D	1256	Reserved	
	1257	Reserved	
	1258	Reserved	
	1259	Reserved	
	1260	Reserved	
	1261	Reserved	
	1262	Reserved	
	1263	Reserved	
9E	1264	Reserved	
	1265	Reserved	
	1266	Reserved	
	1267	Reserved	
	1268	Reserved	
	1269	Reserved	
	1270	Reserved	
	1271	Reserved	
9F	1272	Reserved	
	1273	Reserved	
	1274	Reserved	
	1275	Reserved	
	1276	Reserved	
	1277	Reserved	
	1278	Reserved	
	1279	Reserved	
A0	1280	EPG Data Byte 0	
	1281		
	1282		
	1283		
	1284		
	1285		
	1286		
	1287		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A1	1288	EPG Data Byte 1	
	1289		
	1290		
	1291		
	1292		
	1293		
	1294		
	1295		
A2	1296	EPG Data Byte 2	
	1297		
	1298		
	1299		
	1300		
	1301		
	1302		
	1303		
A3	1304	EPG Data Byte 3	
	1305		
	1306		
	1307		
	1308		
	1309		
	1310		
	1311		
A4	1312	EPG Data Byte 4	
	1313		
	1314		
	1315		
	1316		
	1317		
	1318		
	1319		
A5	1320	EPG Data Byte 5	
	1321		
	1322		
	1323		
	1324		
	1325		
	1326		
	1327		
A6	1328	EPG Data Byte 6	
	1329		
	1330		
	1331		
	1332		
	1333		
	1334		
	1335		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A7	1336	EPG Data Byte 7	
	1337		
	1338		
	1339		
	1340		
	1341		
	1342		
	1343		
A8	1344	EPG Data Byte 8	
	1345		
	1346		
	1347		
	1348		
	1349		
	1350		
	1351		
A9	1352	EPG Data Byte 9	
	1353		
	1354		
	1355		
	1356		
	1357		
	1358		
	1359		
AA	1360	EPG Data Byte 10	
	1361		
	1362		
	1363		
	1364		
	1365		
	1366		
	1367		
AB	1368	EPG Data Byte 11	
	1369		
	1370		
	1371		
	1372		
	1373		
	1374		
	1375		
AC	1376	EPG Data Byte 12	
	1377		
	1378		
	1379		
	1380		
	1381		
	1382		
	1383		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
AD	1384	EPG Data Byte 13	
	1385		
	1386		
	1387		
	1388		
	1389		
	1390		
	1391		
AE	1392	EPG Data Byte 14	
	1393		
	1394		
	1395		
	1396		
	1397		
	1398		
	1399		
AF	1400	EPG Data Byte 15	
	1401		
	1402		
	1403		
	1404		
	1405		
	1406		
	1407		
B0	1408	EPG Data Byte 16	
	1409		
	1410		
	1411		
	1412		
	1413		
	1414		
	1415		
B1	1416	EPG Data Byte 17	
	1417		
	1418		
	1419		
	1420		
	1421		
	1422		
	1423		
B2	1424	EPG Data Byte 18	
	1425		
	1426		
	1427		
	1428		
	1429		
	1430		
	1431		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B3	1432	EPG Data Byte 19	
	1433		
	1434		
	1435		
	1436		
	1437		
	1438		
	1439		
B4	1440	EPG Data Byte 20	
	1441		
	1442		
	1443		
	1444		
	1445		
	1446		
	1447		
B5	1448	EPG Data Byte 21	
	1449		
	1450		
	1451		
	1452		
	1453		
	1454		
	1455		
B6	1456	EPG Data Byte 22	
	1457		
	1458		
	1459		
	1460		
	1461		
	1462		
	1463		
B7	1464	EPG Data Byte 23	
	1465		
	1466		
	1467		
	1468		
	1469		
	1470		
	1471		
B8	1472	EPG Data Byte 24	
	1473		
	1474		
	1475		
	1476		
	1477		
	1478		
	1479		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B9	1480	EPG Data Byte 25	
	1481		
	1482		
	1483		
	1484		
	1485		
	1486		
	1487		
BA	1488	EPG Data Byte 26	
	1489		
	1490		
	1491		
	1492		
	1493		
	1494		
	1495		
BB	1496	EPG Data Byte 27	
	1497		
	1498		
	1499		
	1500		
	1501		
	1502		
	1503		
BC	1504	EPG Data Byte 28	
	1505		
	1506		
	1507		
	1508		
	1509		
	1510		
	1511		
BD	1512	EPG Data Byte 29	
	1513		
	1514		
	1515		
	1516		
	1517		
	1518		
	1519		
BE	1520	EPG Data Byte 30	
	1521		
	1522		
	1523		
	1524		
	1525		
	1526		
	1527		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
BF	1528	EPG Data Byte 31	
	1529		
	1530		
	1531		
	1532		
	1533		
	1534		
	1535		
C0	1536	EPG Data Byte 32	
	1537		
	1538		
	1539		
	1540		
	1541		
	1542		
	1543		
C1	1544	EPG Data Byte 33	
	1545		
	1546		
	1547		
	1548		
	1549		
	1550		
	1551		
C2	1552	EPG Data Byte 34	
	1553		
	1554		
	1555		
	1556		
	1557		
	1558		
	1559		
C3	1560	EPG Data Byte 35	
	1561		
	1562		
	1563		
	1564		
	1565		
	1566		
	1567		
C4	1568	EPG Data Byte 36	
	1569		
	1570		
	1571		
	1572		
	1573		
	1574		
	1575		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
C5	1576	EPG Data Byte 37	
	1577		
	1578		
	1579		
	1580		
	1581		
	1582		
	1583		
C6	1584	EPG Data Byte 38	
	1585		
	1586		
	1587		
	1588		
	1589		
	1590		
	1591		
C7	1592	EPG Data Byte 39	
	1593		
	1594		
	1595		
	1596		
	1597		
	1598		
	1599		
C8	1600	EPG Data Byte 40	
	1601		
	1602		
	1603		
	1604		
	1605		
	1606		
	1607		
C9	1608	EPG Data Byte 41	
	1609		
	1610		
	1611		
	1612		
	1613		
	1614		
	1615		
CA	1616	EPG Data Byte 42	
	1617		
	1618		
	1619		
	1620		
	1621		
	1622		
	1623		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
CB	1624	EPG Data Byte 43	
	1625		
	1626		
	1627		
	1628		
	1629		
	1630		
	1631		
CC	1632	EPG Data Byte 44	
	1633		
	1634		
	1635		
	1636		
	1637		
	1638		
	1639		
CD	1640	EPG Data Byte 45	
	1641		
	1642		
	1643		
	1644		
	1645		
	1646		
	1647		
CE	1648	EPG Data Byte 46	
	1649		
	1650		
	1651		
	1652		
	1653		
	1654		
	1655		
CF	1656	EPG Data Byte 47	
	1657		
	1658		
	1659		
	1660		
	1661		
	1662		
	1663		
D0	1664	EPG Data Byte 48	
	1665		
	1666		
	1667		
	1668		
	1669		
	1670		
	1671		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
D1	1672	EPG Data Byte 49	
	1673		
	1674		
	1675		
	1676		
	1677		
	1678		
	1679		
D2	1680	EPG Data Byte 50	
	1681		
	1682		
	1683		
	1684		
	1685		
	1686		
	1687		
D3	1688	EPG Data Byte 51	
	1689		
	1690		
	1691		
	1692		
	1693		
	1694		
	1695		
D4	1696	EPG Data Byte 52	
	1697		
	1698		
	1699		
	1700		
	1701		
	1702		
	1703		
D5	1704	EPG Data Byte 53	
	1705		
	1706		
	1707		
	1708		
	1709		
	1710		
	1711		
D6	1712	EPG Data Byte 54	
	1713		
	1714		
	1715		
	1716		
	1717		
	1718		
	1719		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
D7	1720	EPG Data Byte 55	
	1721		
	1722		
	1723		
	1724		
	1725		
	1726		
	1727		
D8	1728	EPG Data Byte 56	
	1729		
	1730		
	1731		
	1732		
	1733		
	1734		
	1735		
D9	1736	EPG Data Byte 57	
	1737		
	1738		
	1739		
	1740		
	1741		
	1742		
	1743		
DA	1744	EPG Data Byte 58	
	1745		
	1746		
	1747		
	1748		
	1749		
	1750		
	1751		
DB	1752	EPG Data Byte 59	
	1753		
	1754		
	1755		
	1756		
	1757		
	1758		
	1759		
DC	1760	EPG Data Byte 60	
	1761		
	1762		
	1763		
	1764		
	1765		
	1766		
	1767		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
DD	1768	EPG Data Byte 61	
	1769		
	1770		
	1771		
	1772		
	1773		
	1774		
	1775		
DE	1776	EPG Data Byte 62	
	1777		
	1778		
	1779		
	1780		
	1781		
	1782		
	1783		
DF	1784	EPG Data Byte 63	
	1785		
	1786		
	1787		
	1788		
	1789		
	1790		
	1791		
E0	1792	EPG Data Byte 64	
	1793		
	1794		
	1795		
	1796		
	1797		
	1798		
	1799		
E1	1800	EPG Data Byte 65	
	1801		
	1802		
	1803		
	1804		
	1805		
	1806		
	1807		
E2	1808	EPG Data Byte 66	
	1809		
	1810		
	1811		
	1812		
	1813		
	1814		
	1815		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E3	1816	EPG Data Byte 67	
	1817		
	1818		
	1819		
	1820		
	1821		
	1822		
	1823		
E4	1824	EPG Data Byte 68	
	1825		
	1826		
	1827		
	1828		
	1829		
	1830		
	1831		
E5	1832	EPG Data Byte 69	
	1833		
	1834		
	1835		
	1836		
	1837		
	1838		
	1839		
E6	1840	EPG Data Byte 70	
	1841		
	1842		
	1843		
	1844		
	1845		
	1846		
	1847		
E7	1848	EPG Data Byte 71	
	1849		
	1850		
	1851		
	1852		
	1853		
	1854		
	1855		
E8	1856	EPG Data Byte 72	
	1857		
	1858		
	1859		
	1860		
	1861		
	1862		
	1863		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E9	1864	EPG Data Byte 73	
	1865		
	1866		
	1867		
	1868		
	1869		
	1870		
	1871		
EA	1872	EPG Data Byte 74	
	1873		
	1874		
	1875		
	1876		
	1877		
	1878		
	1879		
EB	1880	EPG Data Byte 75	
	1881		
	1882		
	1883		
	1884		
	1885		
	1886		
	1887		
EC	1888	EPG Data Byte 76	
	1889		
	1890		
	1891		
	1892		
	1893		
	1894		
	1895		
ED	1896	EPG Data Byte 77	
	1897		
	1898		
	1899		
	1900		
	1901		
	1902		
	1903		
EE	1904	EPG Data Byte 78	
	1905		
	1906		
	1907		
	1908		
	1909		
	1910		
	1911		

Table 42: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
EF	1912	EPG Data Byte 79	
	1913		
	1914		
	1915		
	1916		
	1917		
	1918		
	1919		
F0	1920	EPG Data Byte 80	
	1921		
	1922		
	1923		
	1924		
	1925		
	1926		
	1927		
F1	1928	EPG Data Byte 81	
	1929		
	1930		
	1931		
	1932		
	1933		
	1934		
	1935		
F2	1936	EPG Data Byte 82	
	1937		
	1938		
	1939		
	1940		
	1941		
	1942		
	1943		
F3	1944	EPG Data Byte 83	
	1945		
	1946		
	1947		
	1948		
	1949		
	1950		
	1951		
F4	1952	EPG Data Byte 84	
	1953		
	1954		
	1955		
	1956		
	1957		
	1958		
	1959		

Table 42: Register Map (Continued)

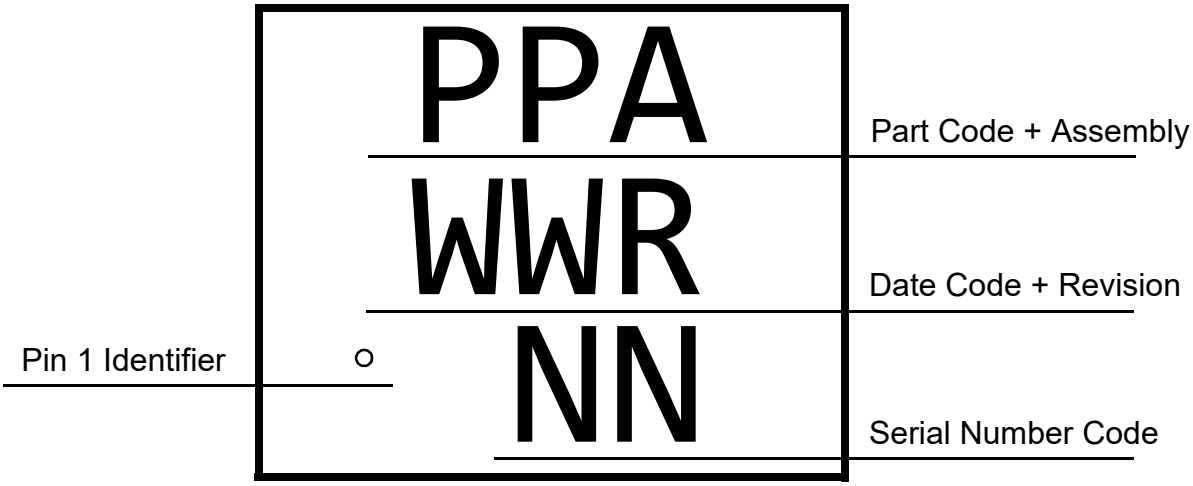
Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F5	1960	EPG Data Byte 85	
	1961		
	1962		
	1963		
	1964		
	1965		
	1966		
	1967		
F6	1968	EPG Data Byte 86	
	1969		
	1970		
	1971		
	1972		
	1973		
	1974		
	1975		
F7	1976	EPG Data Byte 87	
	1977		
	1978		
	1979		
	1980		
	1981		
	1982		
	1983		
F8	1984	EPG Data Byte 88	
	1985		
	1986		
	1987		
	1988		
	1989		
	1990		
	1991		
F9	1992	EPG Data Byte 89	
	1993		
	1994		
	1995		
	1996		
	1997		
	1998		
	1999		
FA	2000	EPG Data Byte 90	
	2001		
	2002		
	2003		
	2004		
	2005		
	2006		
	2007		

Table 42: Register Map (Continued)

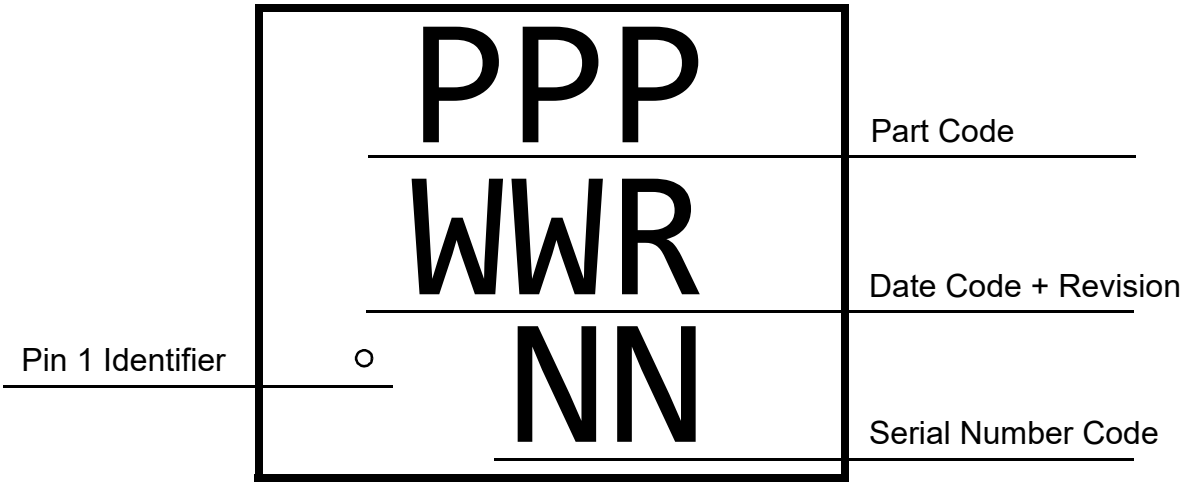
Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
FB	2008	EPG Data Byte 91	
	2009		
	2010		
	2011		
	2012		
	2013		
	2014		
	2015		
FC	2016	Reserved	
	2017	Reserved	
	2018	Reserved	
	2019	Reserved	
	2020	Reserved	
	2021	Reserved	
	2022	Reserved	
	2023	Reserved	
FD	2024	NVM CRC Remainder	
	2025		
	2026		
	2027		
	2028		
	2029		
	2030		
	2031		
FE	2032	NVM CRC Remainder	
	2033		
	2034		
	2035		
	2036		
	2037		
	2038		
	2039		
FF	2040	NVM CRC Remainder	
	2041		
	2042		
	2043		
	2044		
	2045		
	2046		
	2047		

19 Package Top Marking Definitions

19.1 STQFN 12L 1.6 MM X 1.6 MM 0.4P FC, BEFORE FEBRUARY 1, 2021



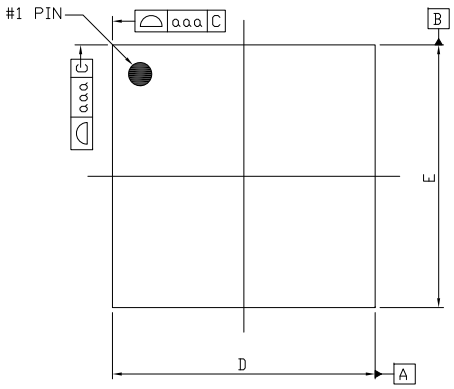
19.2 STQFN 12L 1.6 MM X 1.6 MM 0.4P FC, AFTER FEBRUARY 1, 2021



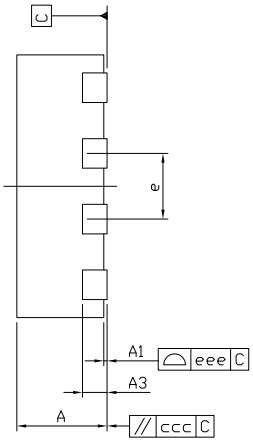
20 Package Information

20.1 PACKAGE OUTLINES FOR STQFN 12L 1.6 MM X 1.6 MM X 0.55 MM 0.4P FC PACKAGE

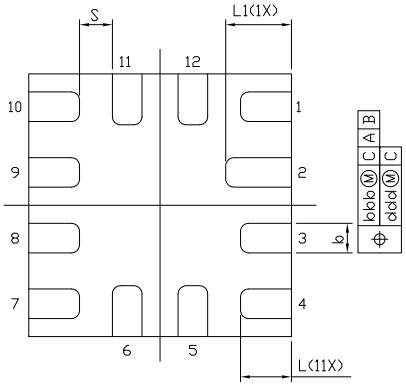
JEDEC MO-220IC Net Weight: 0.0035 g



Top View



Side View



Bottom View

Controlling dimensions: mm

Symbol	MILLIMETER			INCH		
	Min	Nom.	Max	Min	Nom.	Max
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.55	1.60	1.65	0.061	0.063	0.065
e	0.40 BSC			0.016 BSC		
L	0.26	0.31	0.36	0.010	0.012	0.014
L1	0.35	0.40	0.45	0.014	0.016	0.018
b	0.13	0.18	0.23	0.005	0.007	0.009
S	0.200 REF			0.008 REF		
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

“A1” max lead coplanarity 0.05 mm
Standard tolerance: ±0.05

Notes:

1. All dimensions are in millimeters.

2. Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

20.2 MOISTURE SENSITIVITY LEVEL

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 43.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from: http://www.jedec.org.

The <PACKAGE_NAME> package is qualified for MSL <n>.

Table 43: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

20.3 SOLDERING INFORMATION

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

21 Ordering Information

Part Number	Type
SLG46811V	12-pin STQFN
SLG46811VTR	12-pin STQFN - Tape and Reel (3k units)

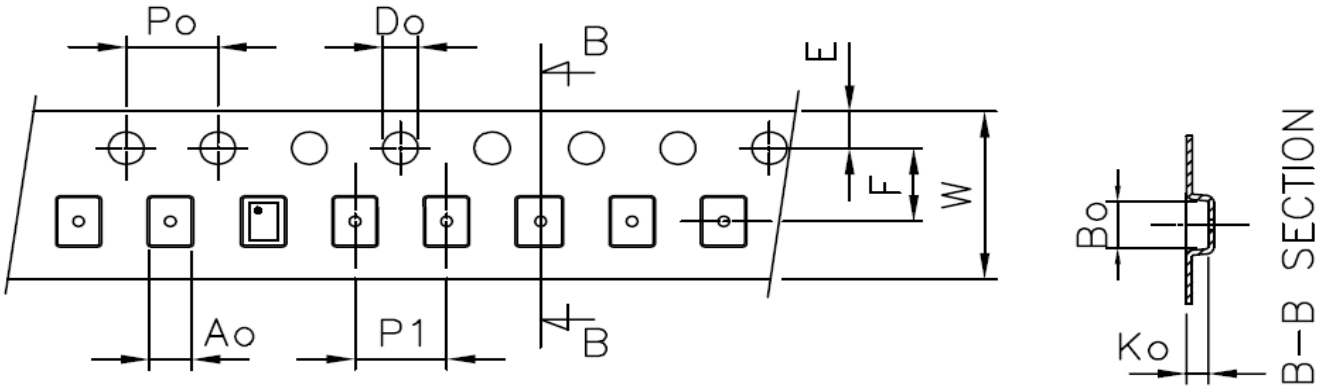
Note 1 Use SLG46811V to order. Shipments are automatically in Tape and Reel.
Note 2 “TR” suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

21.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 12L 1.6 mm x 1.6mm x 0.55 mm 0.4P FC Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

21.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L 1.6 mm x 1.6mm x 0.55 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8

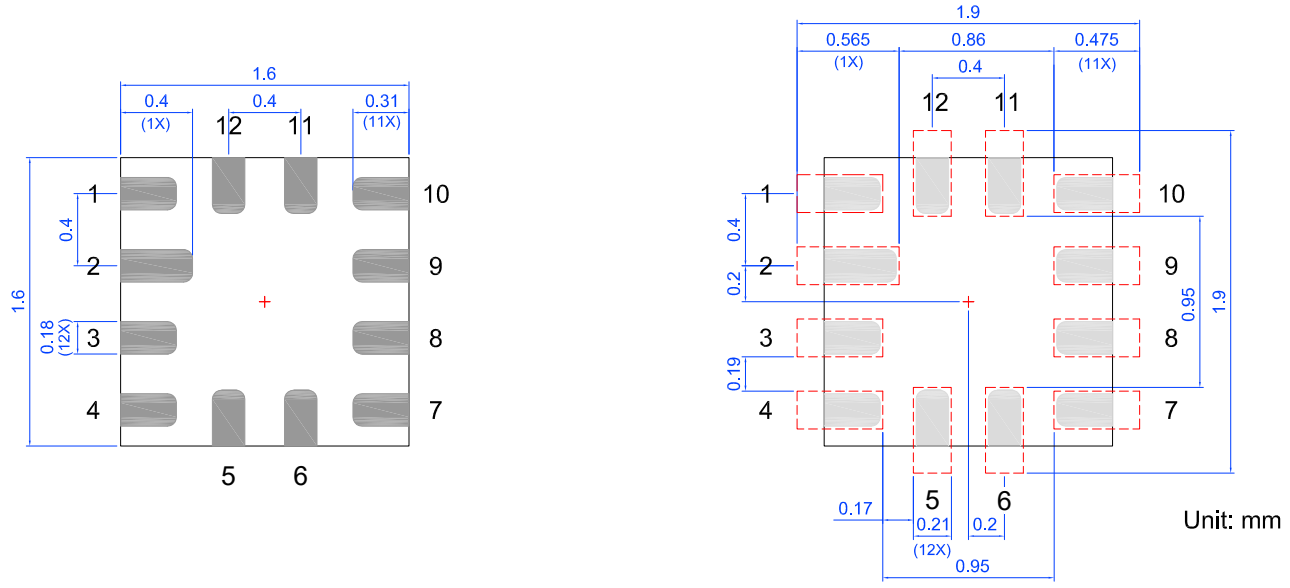


22 Layout Guidelines

22.1 STQFN 12L 1.6 MM X 1.6 MM X 0.55 MM 0.4P FC PACKAGE

Expose Pad
(Package face down)

Recommended Landing Pattern
(Package face down)



Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator

B

BG	Bandgap

C

CLK	Clock
CMO	Connection matrix output

D

DFF	D Flip-Flop
DLY	Delay

E

EPG	Extended Pattern Generator
ESD	Electrostatic discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage

M

MS ACMP	Multichannel Sampling Analog Comparator
MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-Pull
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SV	nSET Value

T

TS	Temperature Sensor

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger

Revision History

Revision	Date	Description
3.4	27-Feb-2023	Added notes to Ordering Information Fixed typos
3.3	8-Dec-2022	Fixed typos Updated section 3-Bit LUT or DFF with Set/Reset Macrocells Or Shift Register Macrocells
3.2	7-Mar-2022	Renesas re-branding Updated Pull-up or Pull-down Resistance Parameter in EC table
3.1	29-Dec-2021	Corrected Layout Guidelines Added IC Net Weight in Package Information section Added information about SCL and SDA Pins' Schmitt Trigger Updated section GPIO7 Source for Oscillator1 (25 MHz)
3.0	14-Apr-2021	Final version

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
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