SLG5NT1757V

An Adjustable Turn-on Time, 5 mΩ, 4 A Ultra Low Power Switch with Fast Discharge

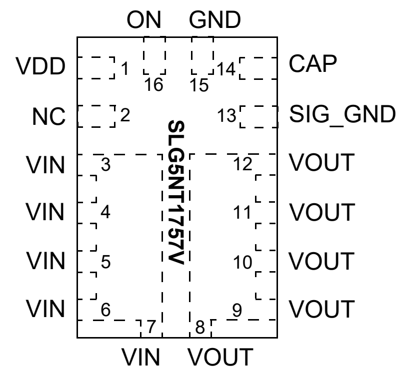
General Description

Operating from a 3.0 V to 5.5 V power supply and fully specified over the -40 °C to 85 °C temperature range, the SLG5NT1757V is a high-performance 5 mΩ, 4 A single-channel nFET integrated power switch. Using a proprietary MOSFET design, the SLG5NT1757V achieves a stable 5 mΩ RDS_{ON} across a wide input/supply voltage range. The SLG5NT1757V is designed for all 0.6 V to 1.98 V power rail applications. Using Dialog's advanced assembly techniques for high-current operation, the SLG5NT1757V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.6 mm x 2.5 mm STQFN package.

Features

- Low Typical RDS_{ON} nFET: 5 mΩ
- Maximum Continuous Switch Current: Up to 4 A
- Supply Voltage: 3.0 V ≤ V_{DD} ≤ 5.5 V
- Input Voltage Range: 0.6 V ≤ V_{IN} ≤ 1.98 V
- Fast Turn-on:
  - 48 µs when tune C_{SLEW} = 4.7 nF, R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF, V_{DD} = 5 V, V_{IN} = 1 V
  - 168 µs when tune C_{SLEW} = 22 nF, R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF, V_{DD} = 5 V, V_{IN} = 1 V
- Low θ_{JA}, 16-pin 1.6 mm x 2.5 mm STQFN Packaging
  - Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

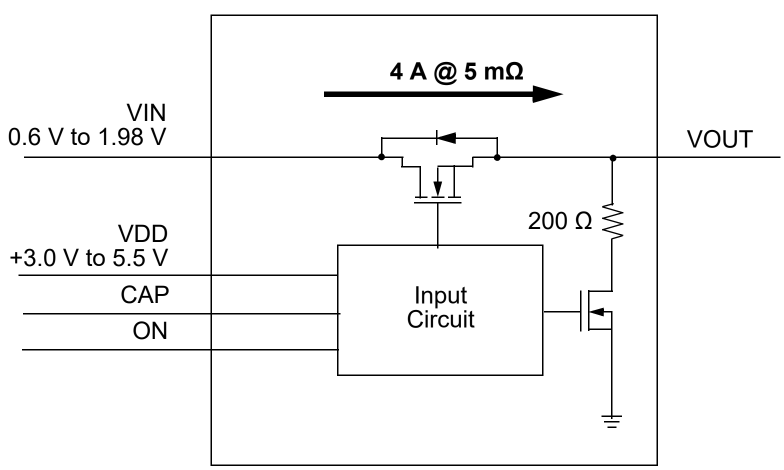


16-pin FC-STQFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	VDD supplies the power for the operation of the power switch and internal control circuitry where its range is 3.0 V ≤ V_{DD} ≤ 5.5 V. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor
2	NC	NC	No Connect - make no external connection to this pin.
3-7	VIN	MOSFET	Drain terminal of Power MOSFET (Pins 3-7 fused together). Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at VIN should be rated at 10 V or higher.
8-12	VOUT	MOSFET	Source terminal of Power MOSFET (Pins 8-12 fused together) Connect a low ESR capacitor (up to 10 µF) from this pin to GND. Capacitors used at VOUT should be rated at 10 V or higher.
13	SIG_GND	GND	Analog signal ground.
14	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount tuning capacitor C_{SLEW} connected from CAP pin to GND sets the V_{OUT} slew rate and overall turn-on time of the SLG5NT1757V. Capacitors used at the CAP pin should be rated at 10 V or higher.
15	GND	GND	Analog or Power ground.
16	ON	Input	A low-to-high transition on this pin closes the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 0.85 V. As the ON pin input circuit has an internal 4 MΩ pull-down, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.

Ordering Information

Part Number	Type	Production Flow
SLG5NT1757V	STQFN 16L	Industrial, -40 °C to 85 °C
SLG5NT1757VTR	STQFN 16L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage to GND		--	--	6	V
V_{IN} to GND	Power Switch Input Voltage to GND		-0.3	--	6	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON to GND	ON Pin Voltages to GND		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1.6 x 2.5 mm 16L STQFN; Determined using 1 in^2, 1.2 oz. copper pads under each VIN and VOUT on FR4 pcb material	--	35	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1.2	W
IDS_{MAX}	Max Continuous Switch Current		--	--	4	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

3.0 V ≤ V_{DD} ≤ 5.5 V; 0.6 V ≤ V_{IN} ≤ 1.98 V; T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-40 to 85°C	3.0	--	5.5	V
I_{DD}	Power Supply Current (PIN 1)	when OFF, T_A = 25°C	--	0.001	0.02	µA
		when ON, No load, ON = V_{DD}, T_A = 25°C	--	0.007	0.08	µA
		when OFF, T_A = 85°C	--	0.017	0.12	µA
		when ON, No load, ON = V_{DD}, T_A = 85°C	--	0.25	1.8	µA
RDS_{ON}	ON Resistance	T_A = 25°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 2.0 V	--	6.8	8.5	mΩ
		T_A = 25°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 2.5 V	--	5.6	7.1	mΩ
		T_A = 25°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 3.0 V	--	5.0	6.2	mΩ
		T_A = 25°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 3.5V	--	4.6	5.7	mΩ
		T_A = 25°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 4.0 V	--	4.3	5.3	mΩ

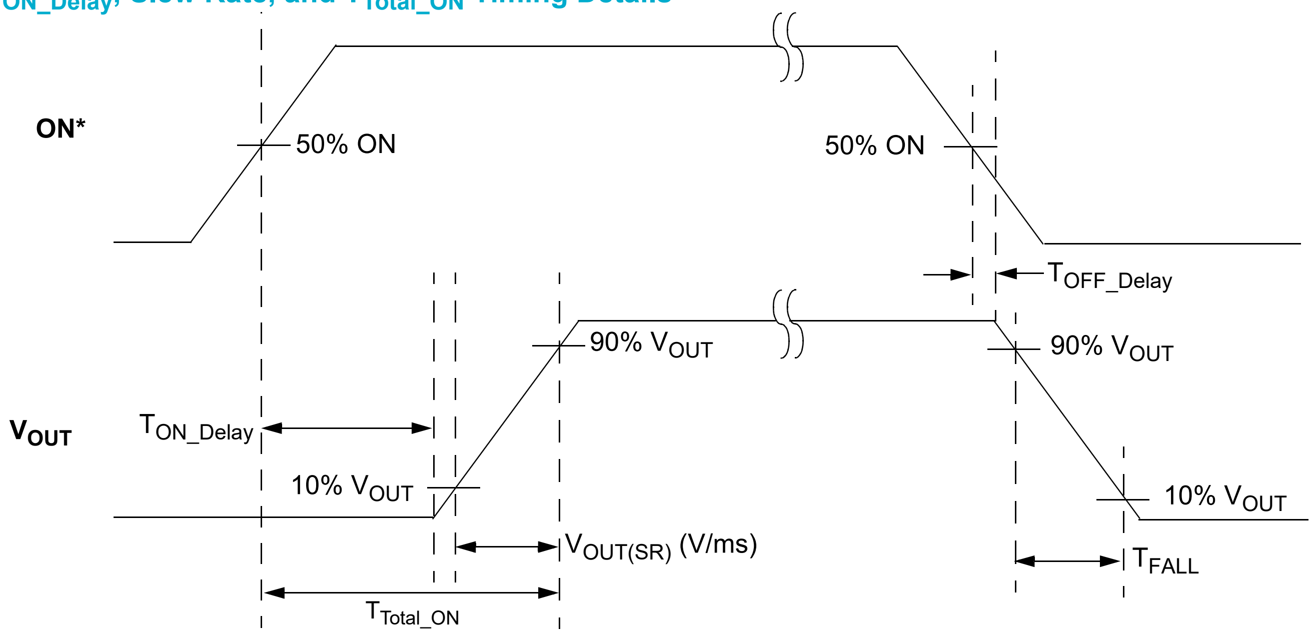
Electrical Characteristics **(continued)**

3.0 V ≤ V_{DD} ≤ 5.5 V; 0.6 V ≤ V_{IN} ≤ 1.98 V; T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
RDS_{ON}	ON Resistance	T_A = 85°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 2.0 V	--	8.1	10.3	mΩ
		T_A = 85°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 2.5 V	--	6.8	8.6	mΩ
		T_A = 85°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 3.0 V	--	6.0	7.6	mΩ
		T_A = 85°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 3.5V	--	5.5	7.0	mΩ
		T_A = 85°C, I_{DS} = 300 mA, V_{DD} - V_{IN} = 4.0 V	--	5.2	6.5	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	4	A
V_{IN}	Operating Input Voltage		0.6	--	1.98[1]	V
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_{OUT}	Set by External C_{SLEW}			
		50% ON to 90% $V_{OUT,}$ V_{DD} = 5 V, V_{IN} = 1.0 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω, C_{SLEW} = 4.7 nF	--	48	65	µs
		50% ON to 90% $V_{OUT,}$ V_{DD} = 5 V, V_{IN} = 1.0 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω, C_{SLEW} = 22 nF	--	168	230	µs
$V_{OUT(SR)}$	Slew Rate	10% V_{OUT} to 90% V_{OUT}	Set by External C_{SLEW}			
		10% V_{OUT} to 90% $V_{OUT,}$ V_{DD} = 5 V, V_{IN} = 1.0 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω, C_{SLEW} = 4.7 nF	--	31	46	V/ms
		10% V_{OUT} to 90% $V_{OUT,}$ V_{DD} = 5 V, V_{IN} = 1.0 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω, C_{SLEW} = 22 nF	--	9	11.5	V/ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start; V_{DD} = 5 V; V_{IN} = 1.0 V; R_{LOAD} = 20 Ω, no C_{LOAD}, C_{SLEW} = 22 nF	--	45	65	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	--	--	10	µF
$R_{DISCHRG}$	Output Discharge Resistance	3.0 V ≤ V_{DD} ≤ 5.5 V; V_{OUT} < 0.4 V	160	200	250	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
$I_{ON(LKG)}$	ON Pin Leakage Current	ON = ON_V_{IH} or ON = GND	--	1.5	--	µA

Notes:
1. But not higher than V_{DD} - 1.5 V

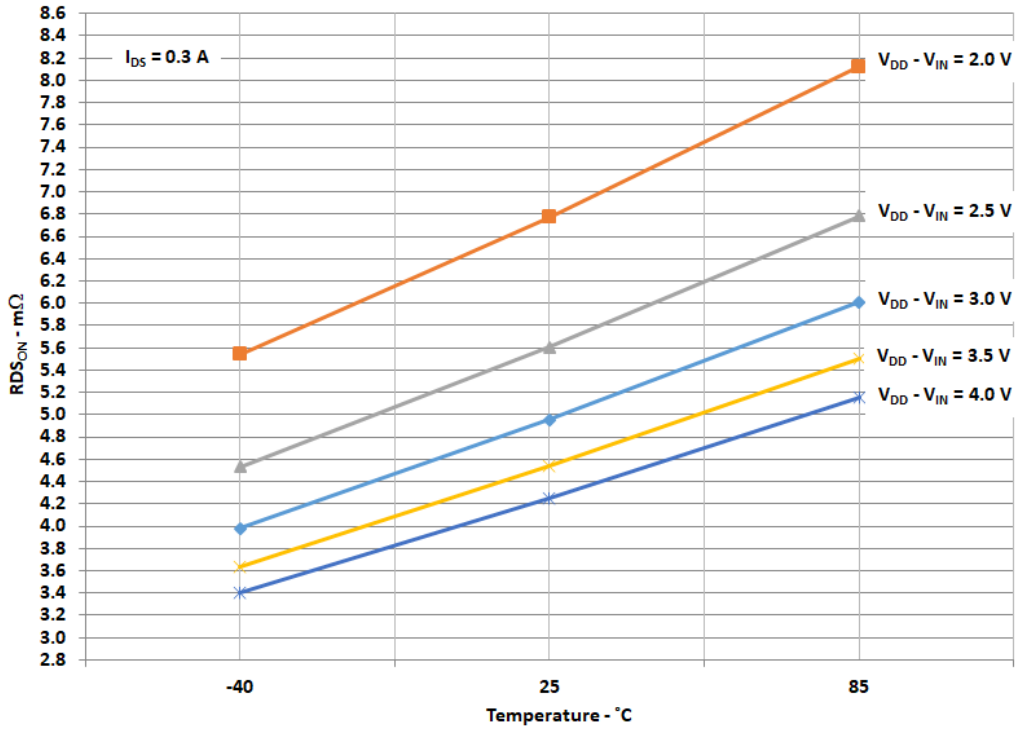
T_{ON_Delay}, Slew Rate, and T_{Total_ON} Timing Details



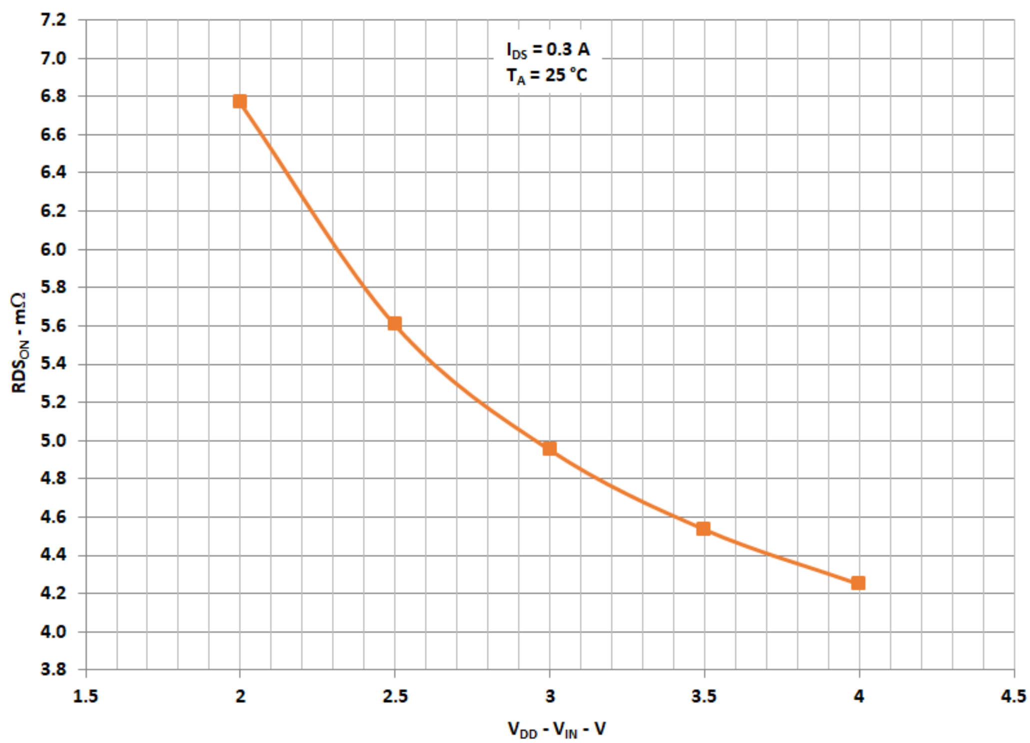
* Rise and Fall times of the ON signal are 100 ns

Typical Performance Characteristics

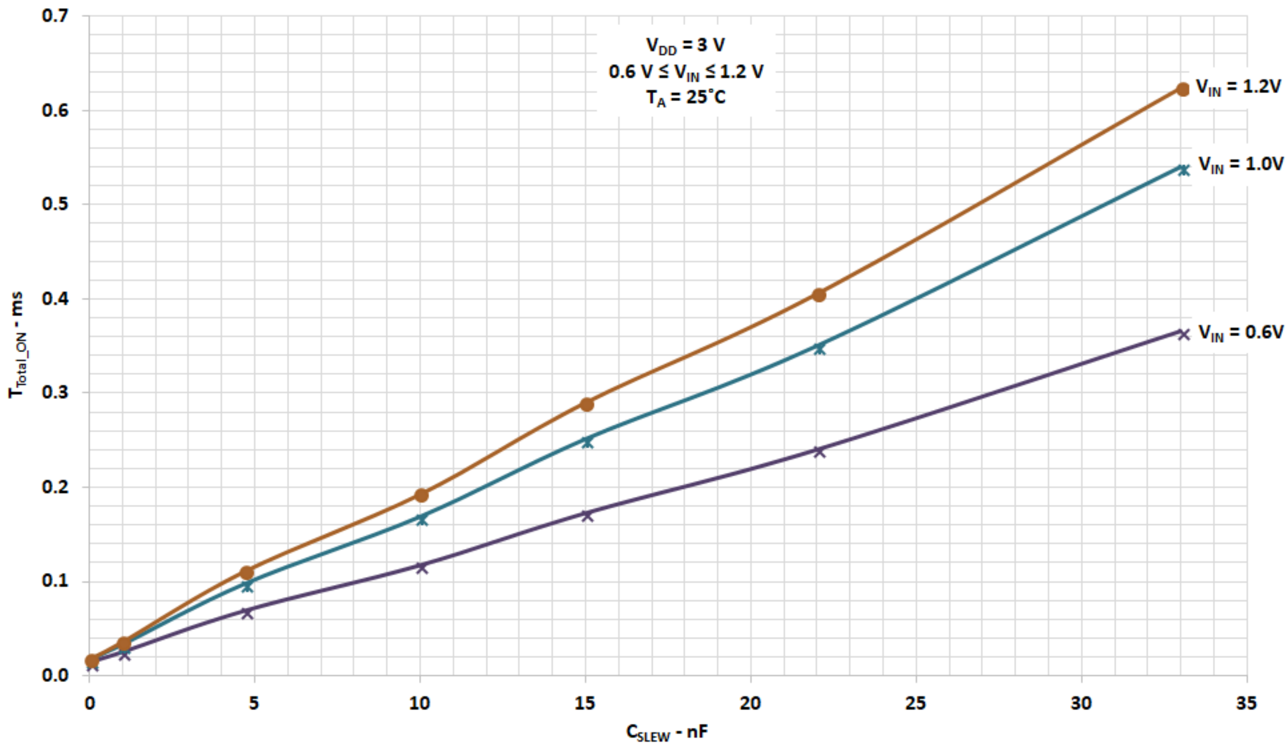
RDS_{ON} vs. Temperature and V_{DD} - V_{IN}



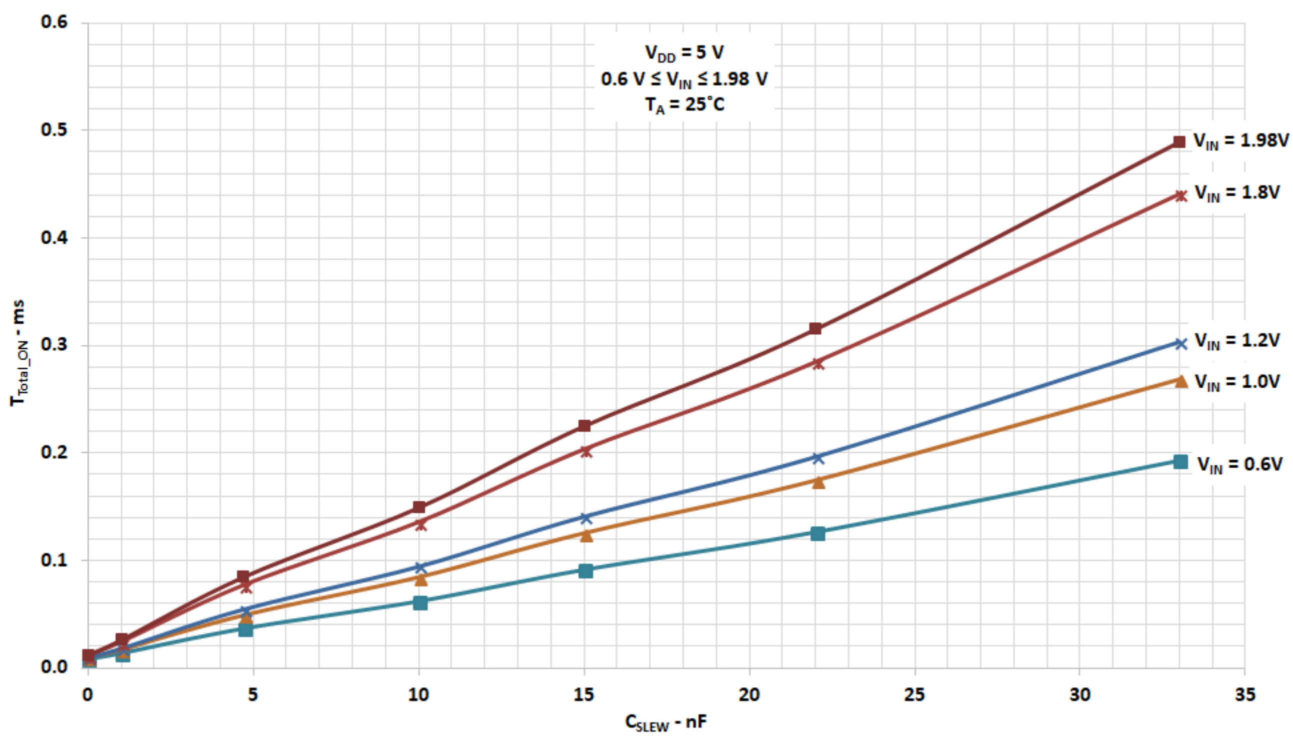
RDS_{ON} vs. V_{DD} - V_{IN}



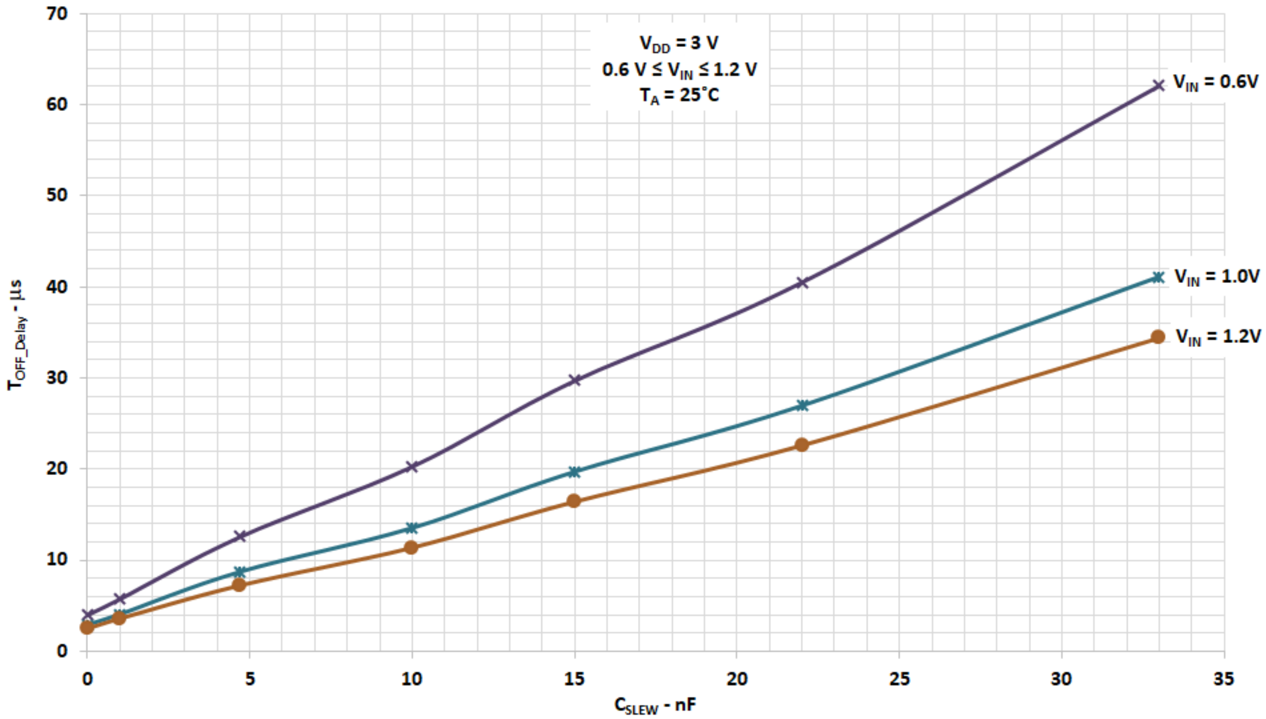
T_{Total_ON} vs. C_{SLEW} and V_{IN} at V_{DD} = 3 V



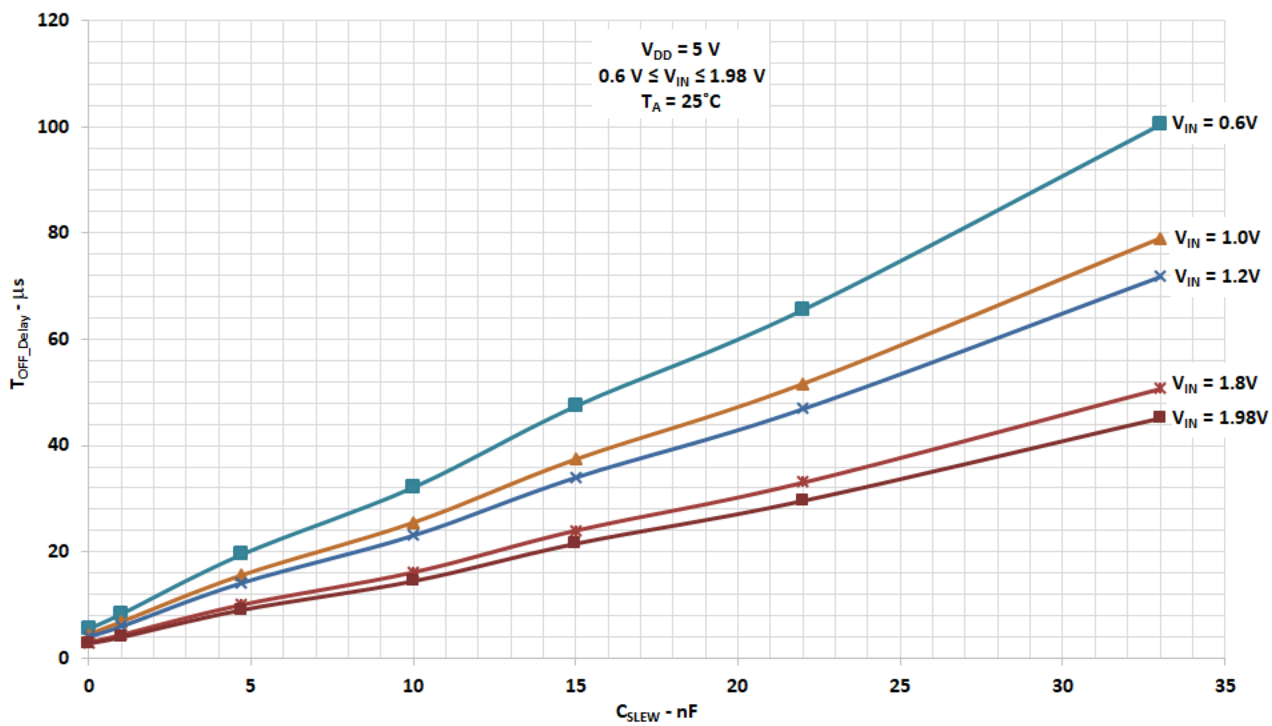
T_{Total_ON} vs. C_{SLEW} and V_{IN} at V_{DD} = 5 V



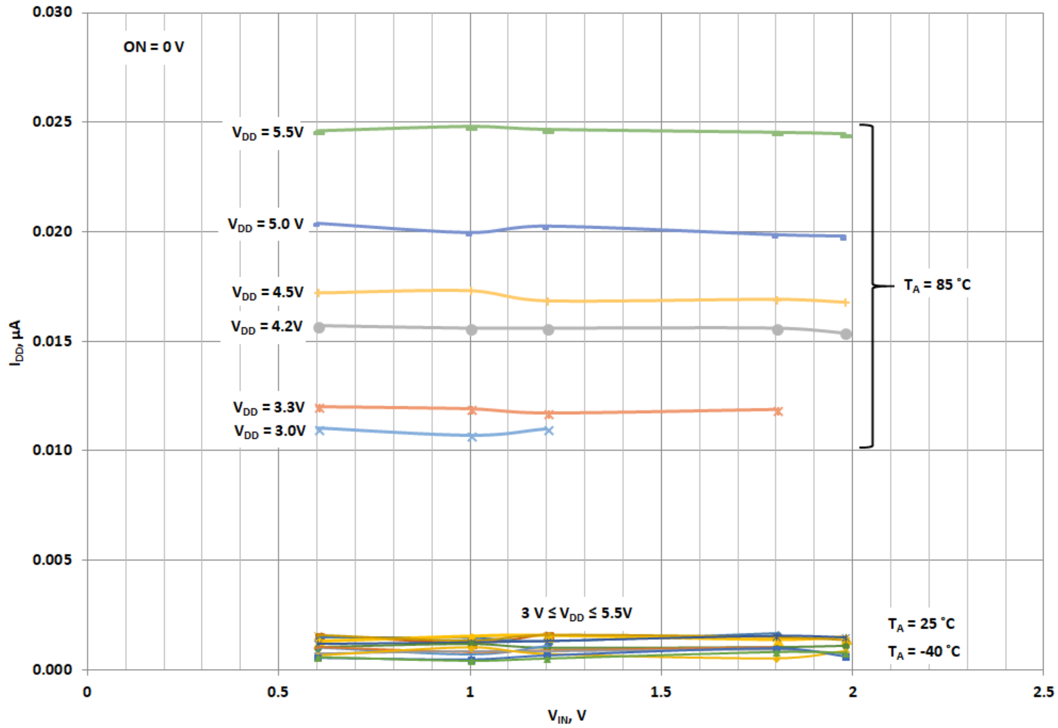
T_{OFF_Delay} vs. C_{SLEW} and V_{IN} at V_{DD} = 3 V



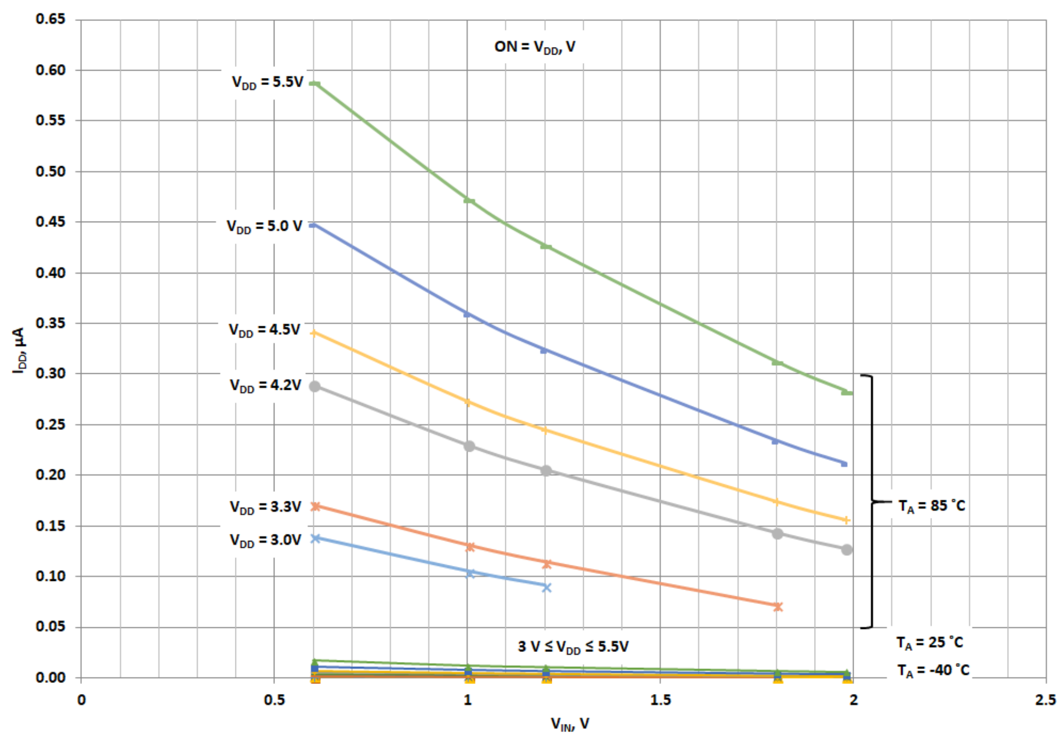
T_{OFF_Delay} vs. C_{SLEW} and V_{IN} at V_{DD} = 5 V



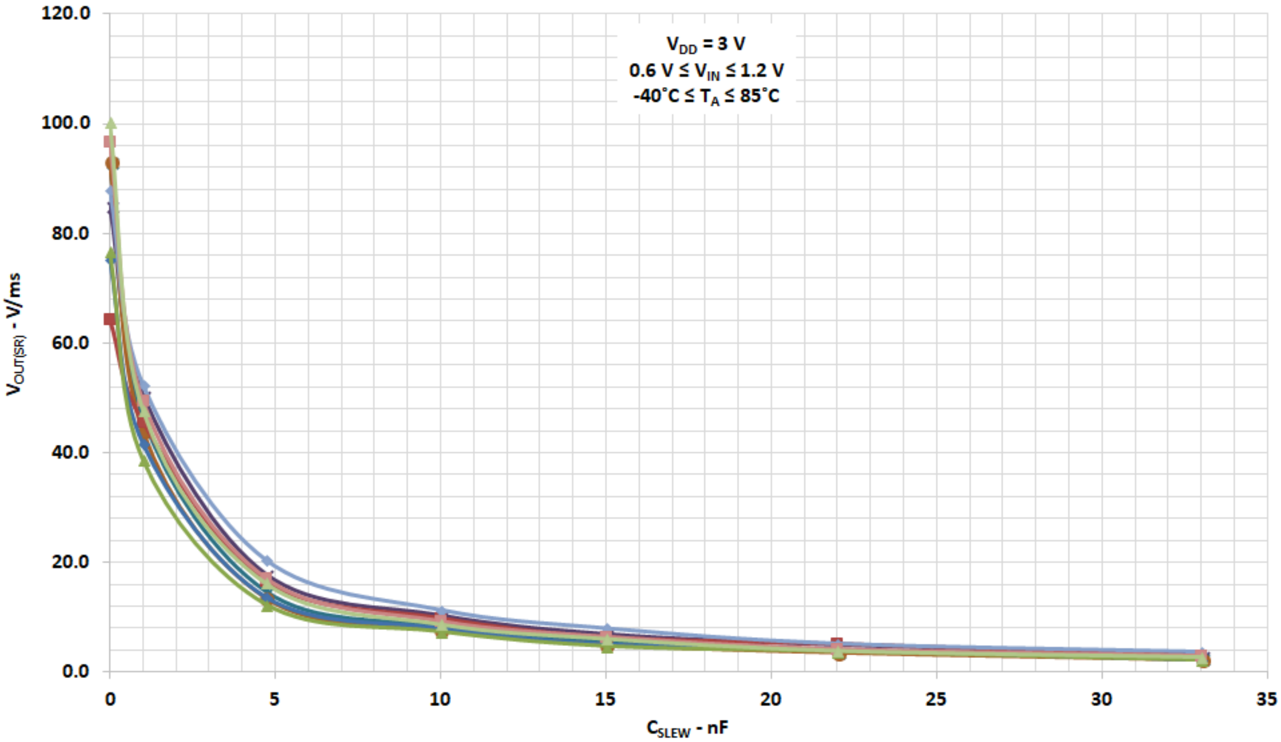
I_{DD} when OFF vs. V_{IN}, V_{DD}, and Temperature



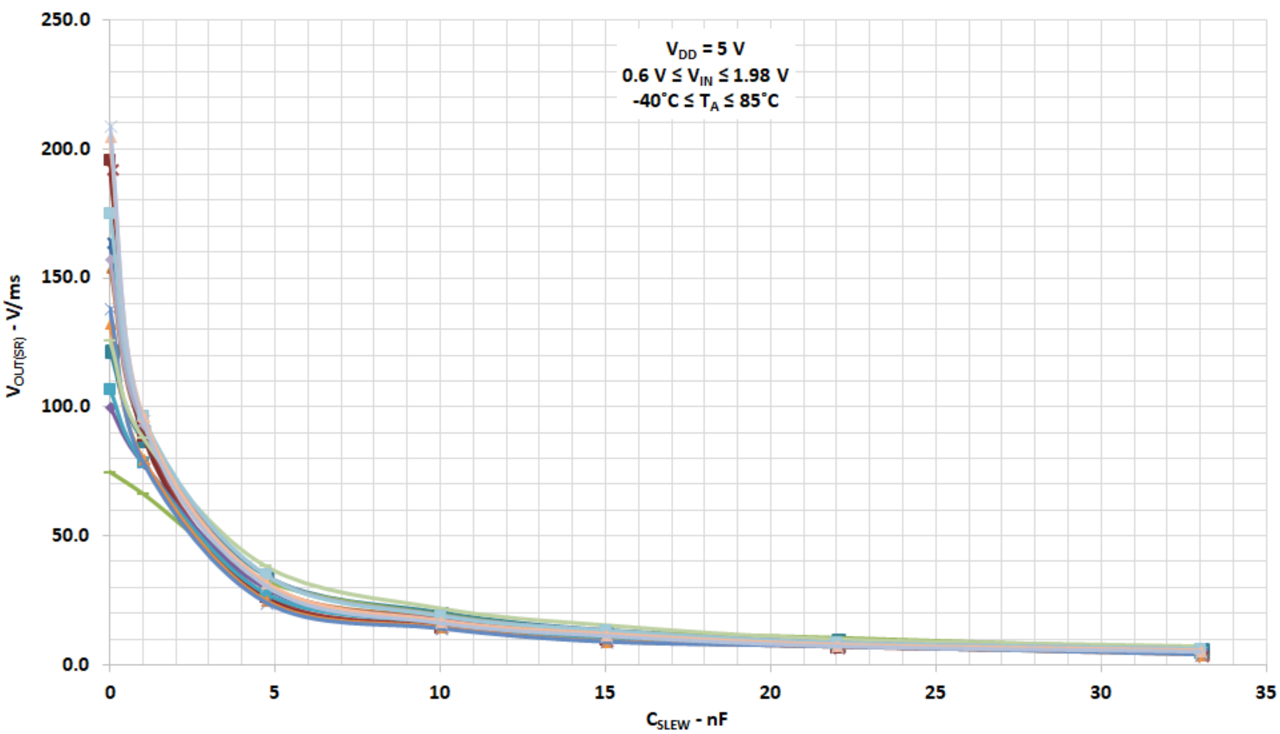
I_{DD} when ON vs. V_{IN}, V_{DD}, and Temperature



$V_{OUT(SR)}$ vs. C_{SLEW}, Temperature, and V_{IN} at V_{DD} = 3 V



$V_{OUT(SR)}$ vs. C_{SLEW}, Temperature, and V_{IN} at V_{DD} = 5 V



Typical Turn-on Waveforms

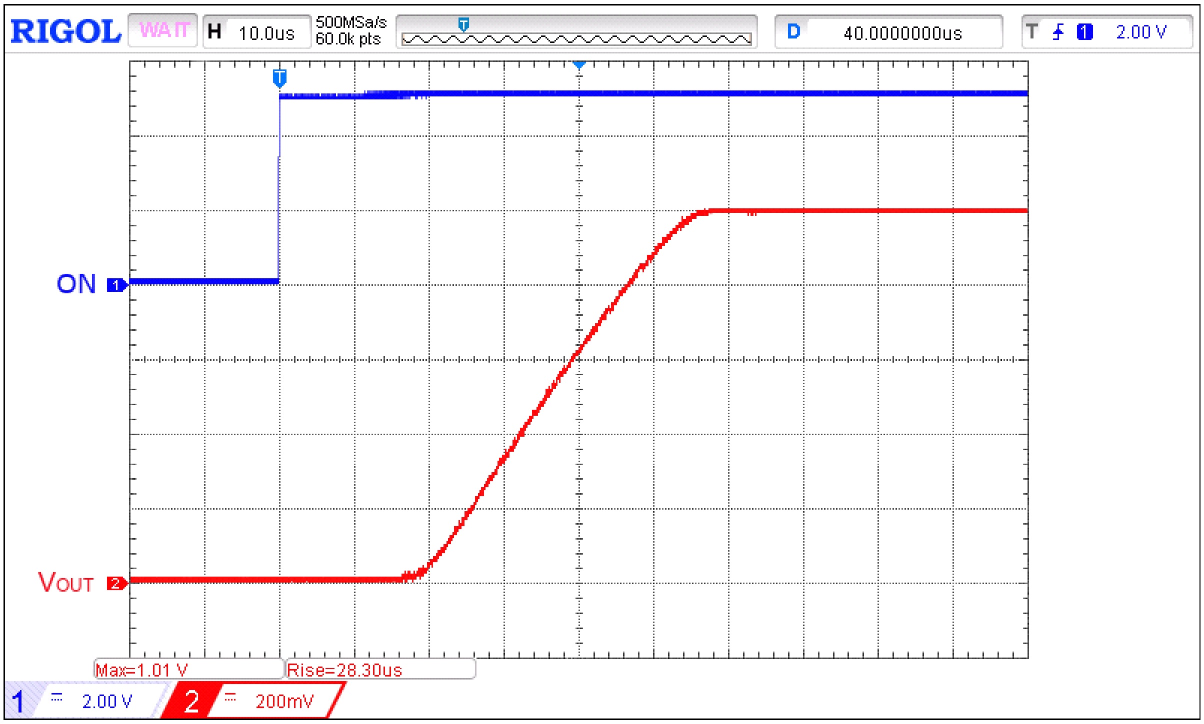


Figure 1. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 1 V, C_{SLEW} = 4.7 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

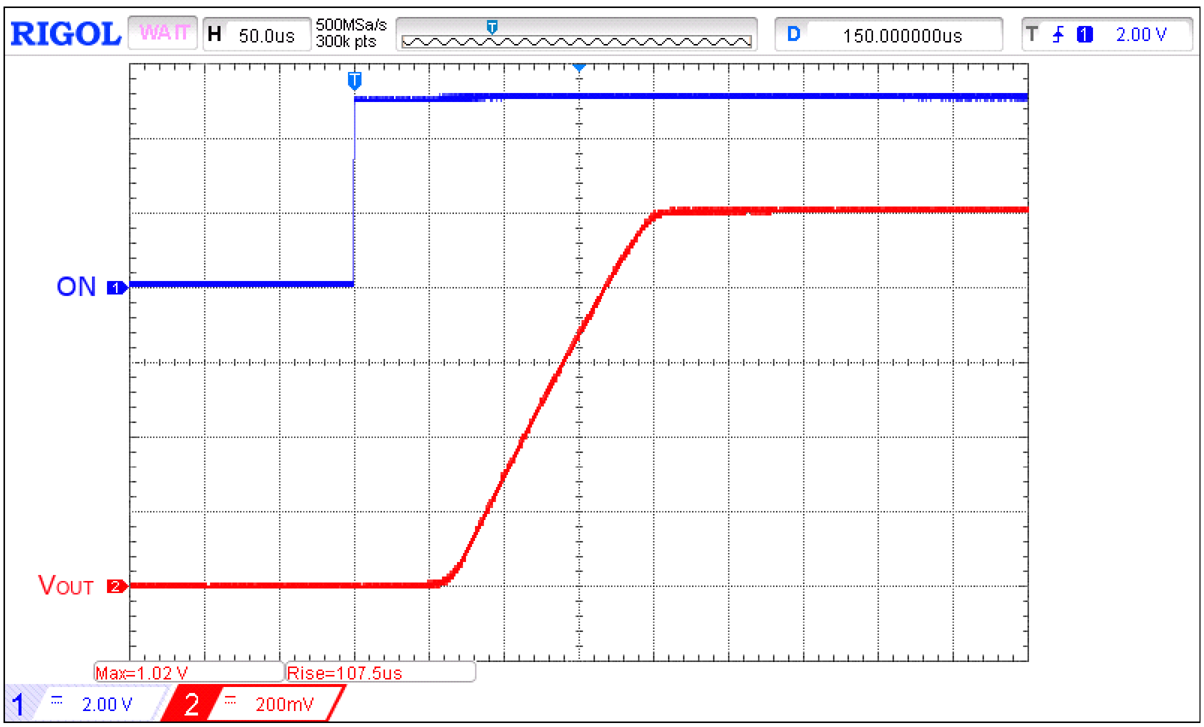


Figure 2. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 1 V, C_{SLEW} = 22 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

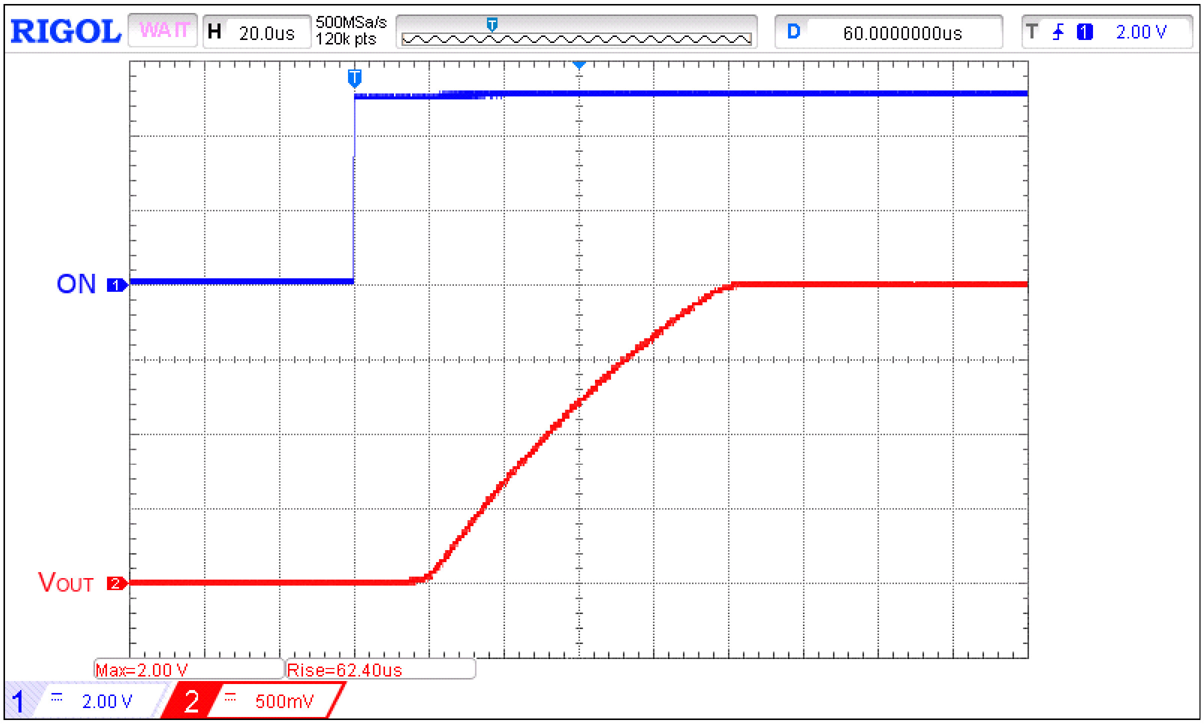


Figure 3. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 1.98 V, C_{SLEW} = 4.7 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

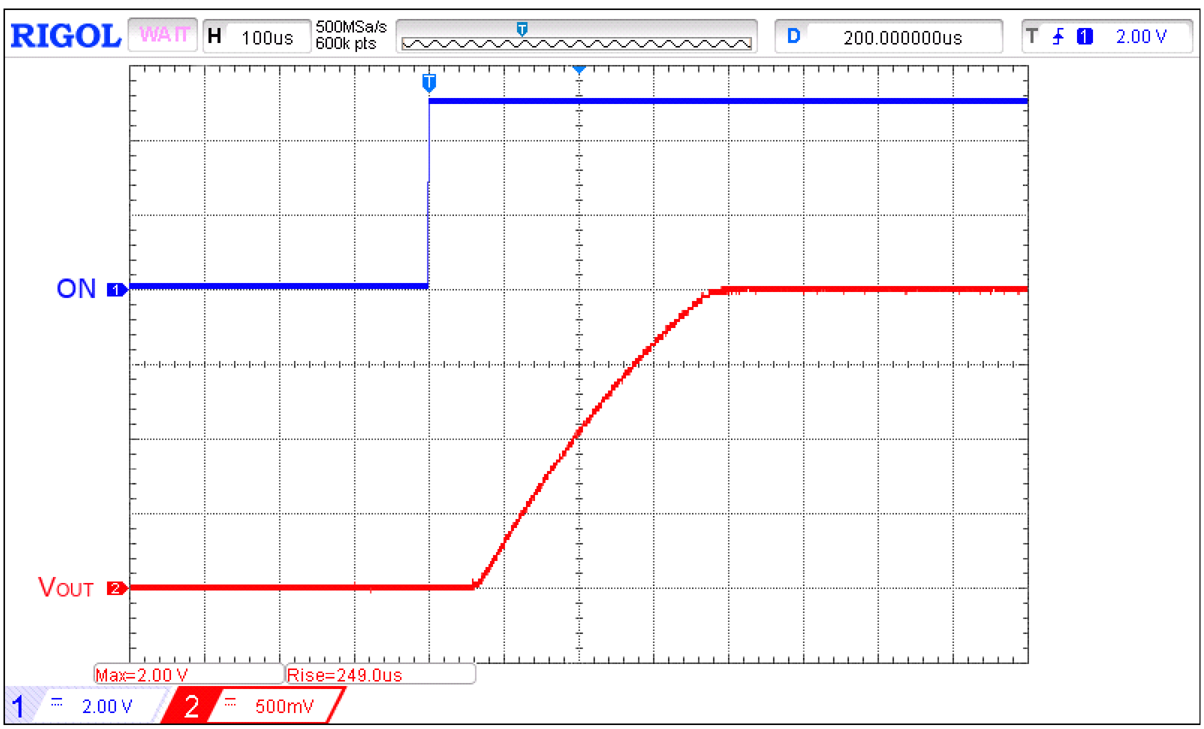


Figure 4. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 1.98 V, C_{SLEW} = 22 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

Typical Turn-off Waveforms

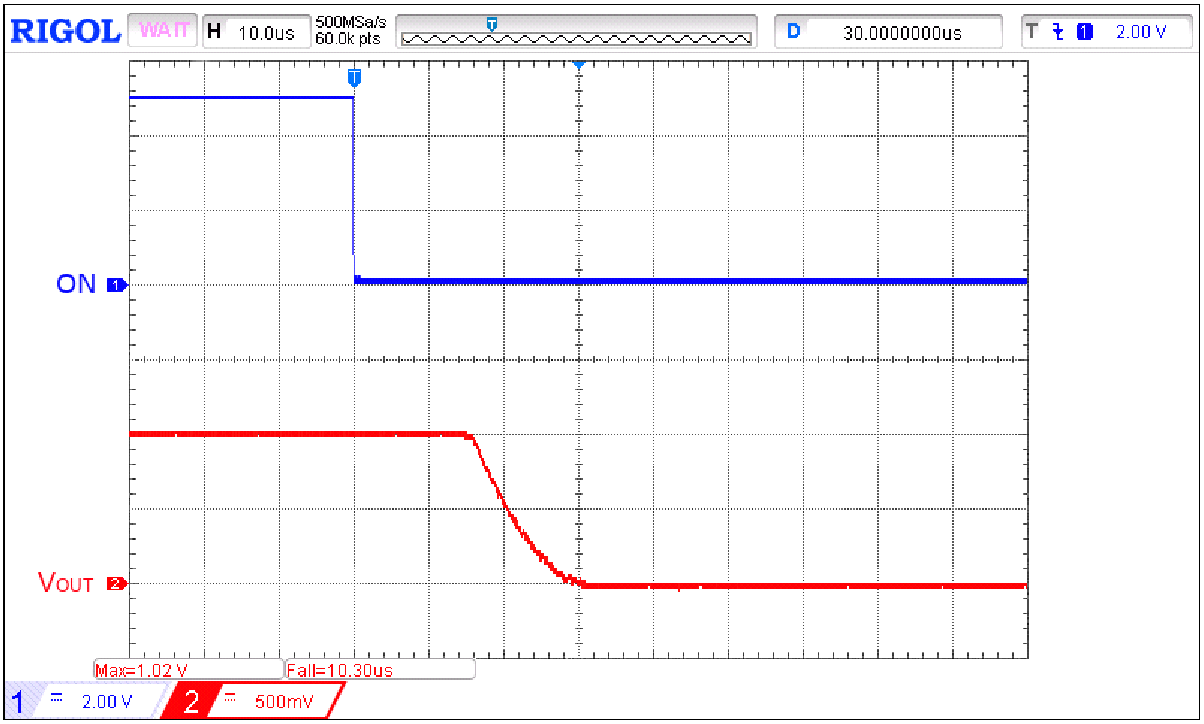


Figure 5. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1 V, C_{SLEW} = 4.7 nF, no C_{LOAD}, R_{LOAD} = 20 Ω

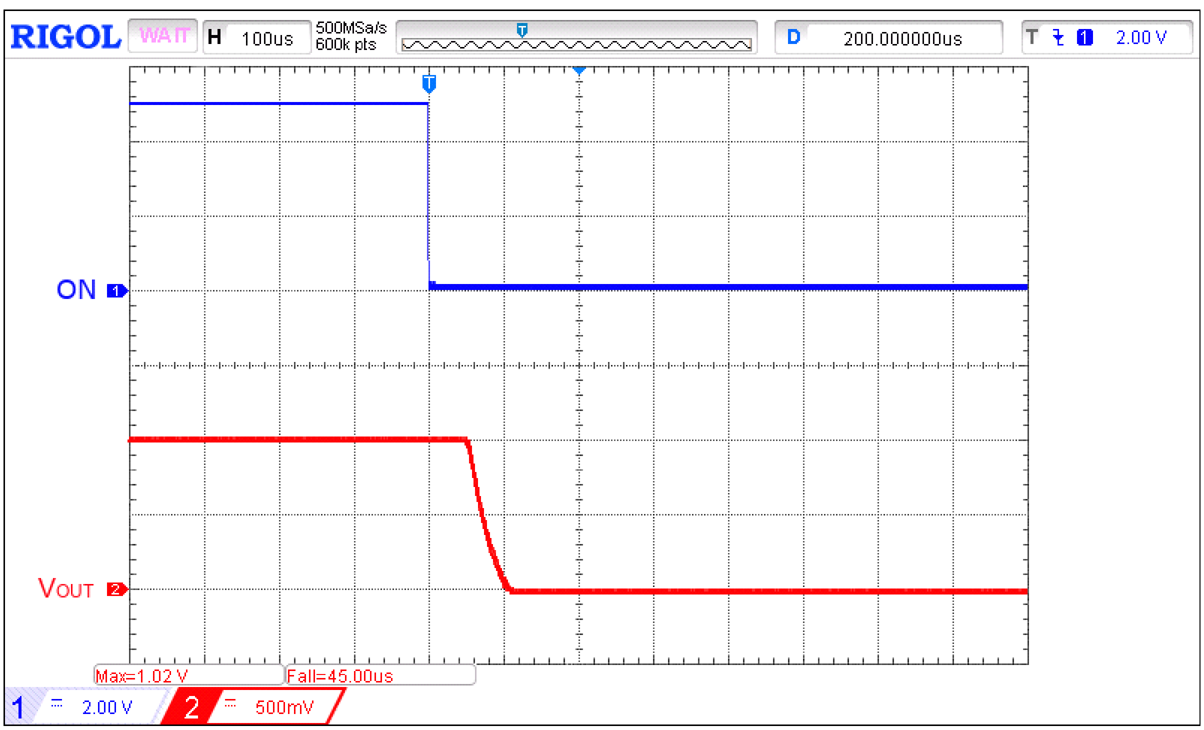


Figure 6. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1 V, C_{SLEW} = 22 nF, no C_{LOAD}, R_{LOAD} = 20 Ω

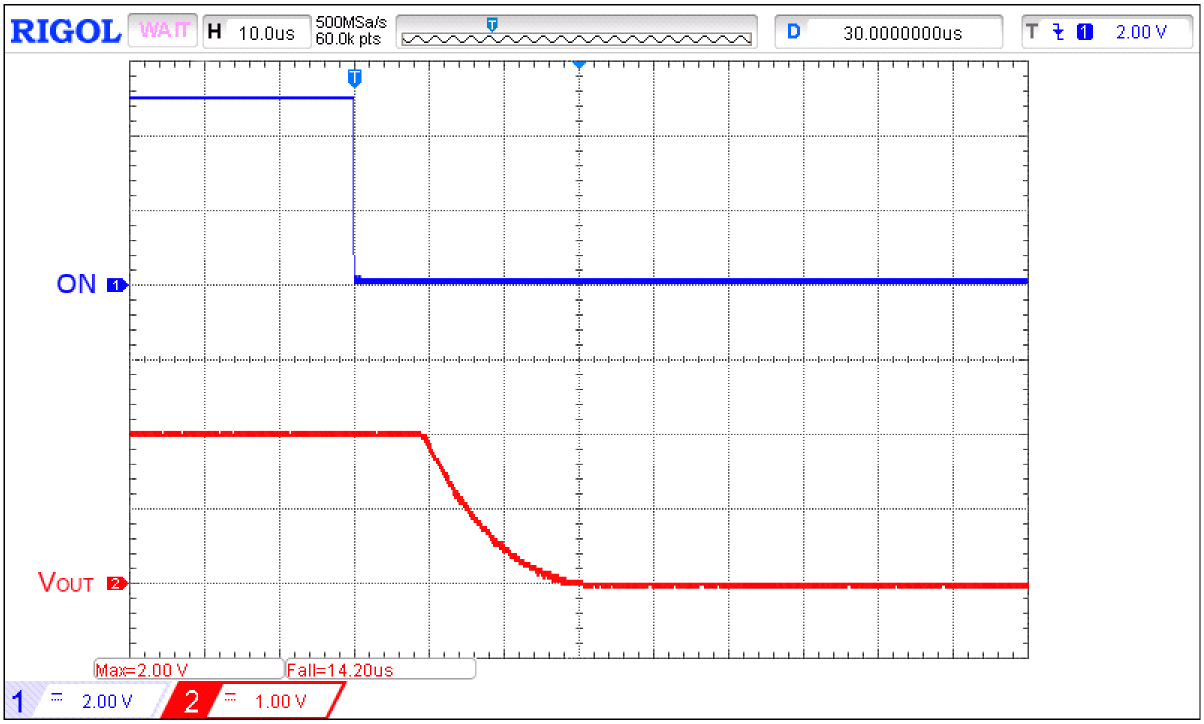


Figure 7. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1.98 V, C_{SLEW} = 4.7 nF, no C_{LOAD}, R_{LOAD} = 20 Ω

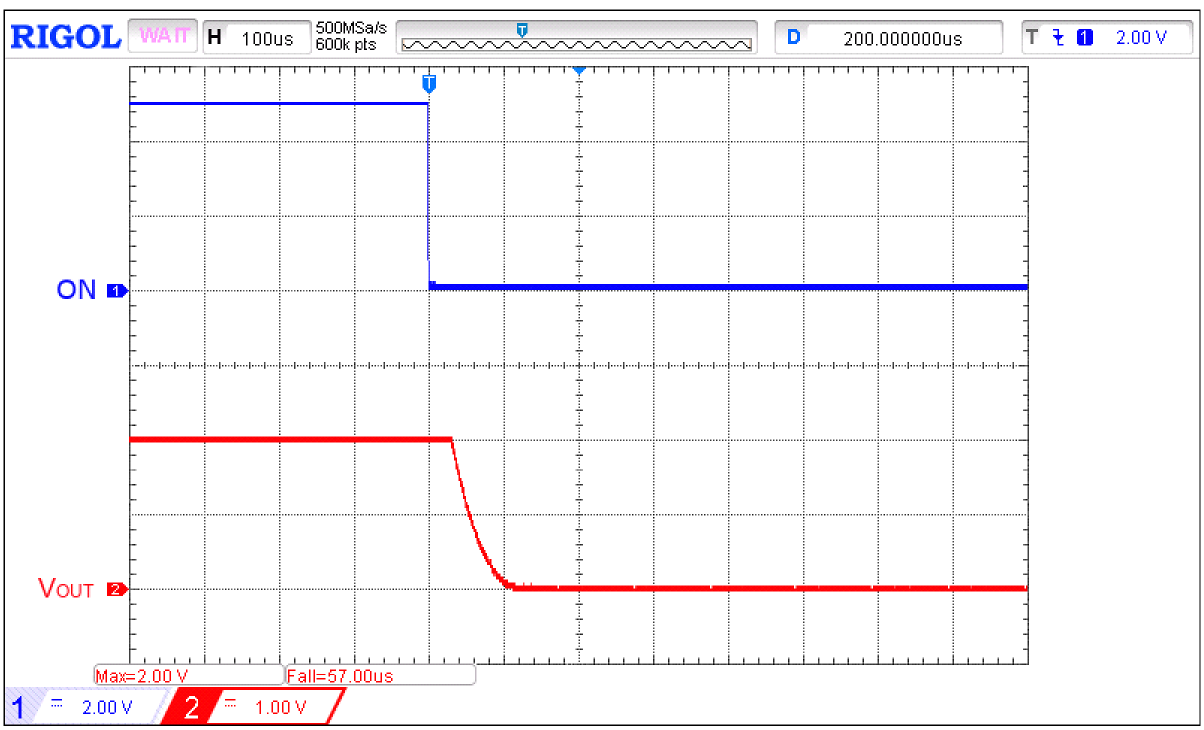


Figure 8. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1.98 V, C_{SLEW} = 22 nF, no C_{LOAD}, R_{LOAD} = 20 Ω

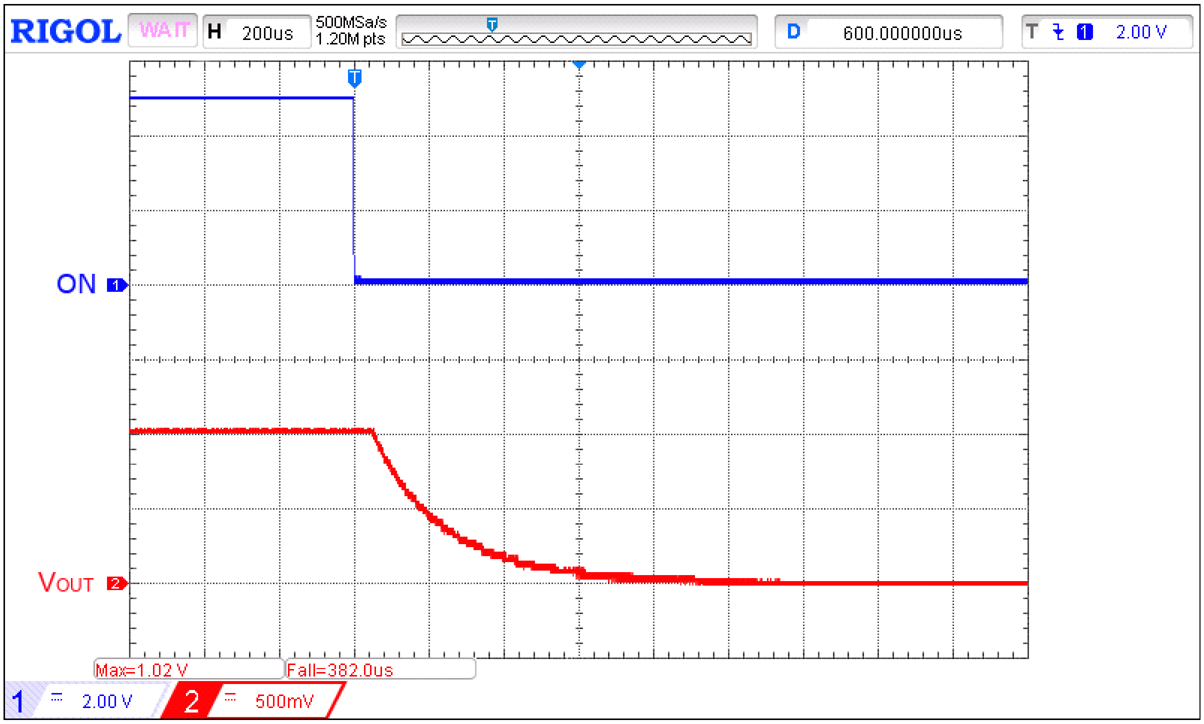


Figure 9. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1 V, C_{SLEW} = 4.7 nF, C_{LOAD} = 10 μF, R_{LOAD} = 20 Ω

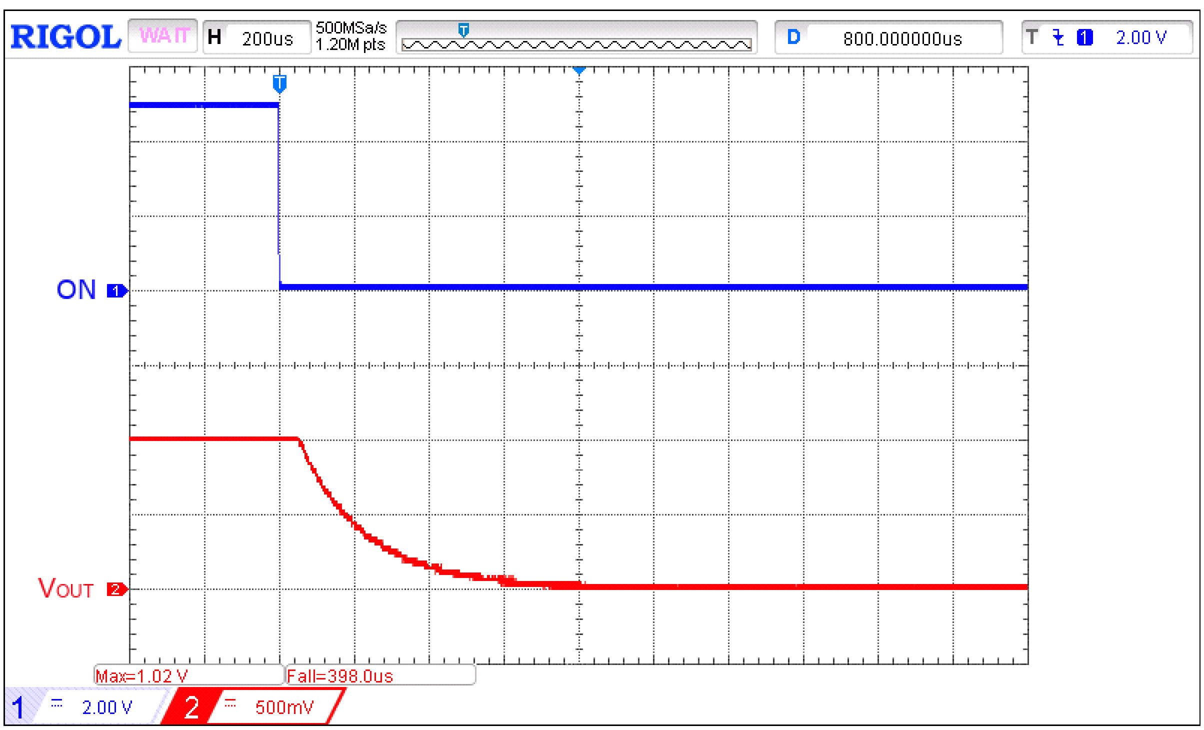


Figure 10. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1 V, C_{SLEW} = 22 nF, C_{LOAD} = 10 μF, R_{LOAD} = 20 Ω

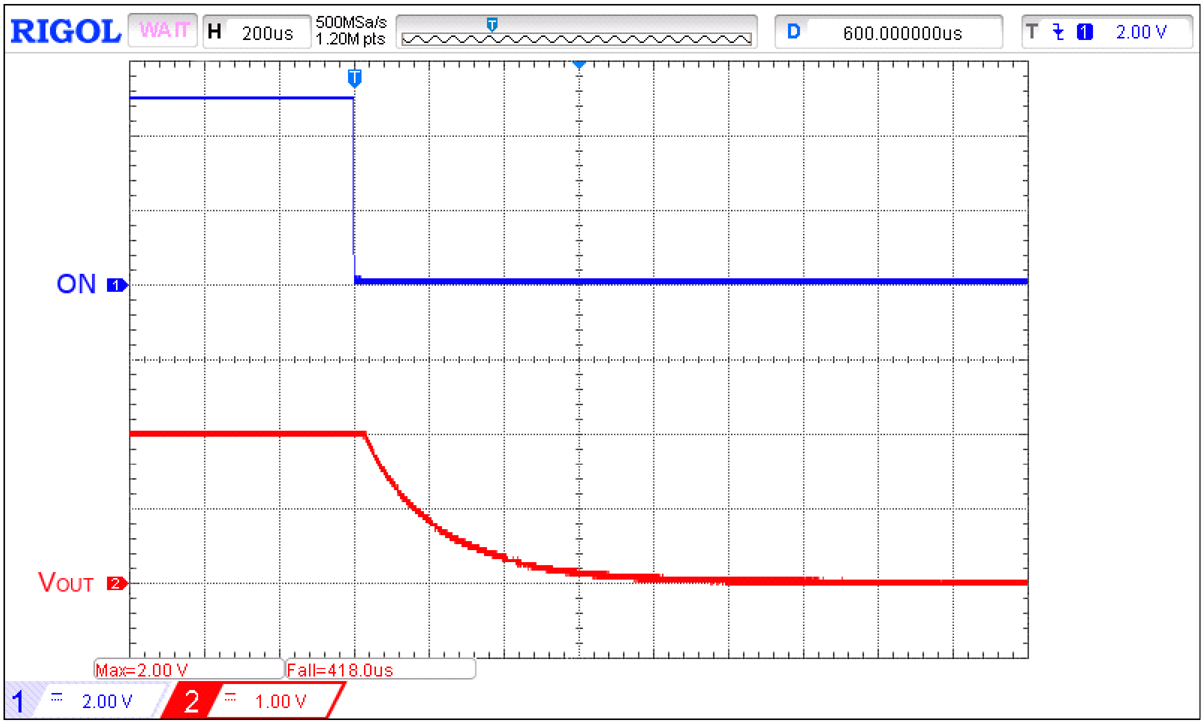


Figure 11. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1.98 V, C_{SLEW} = 4.7 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

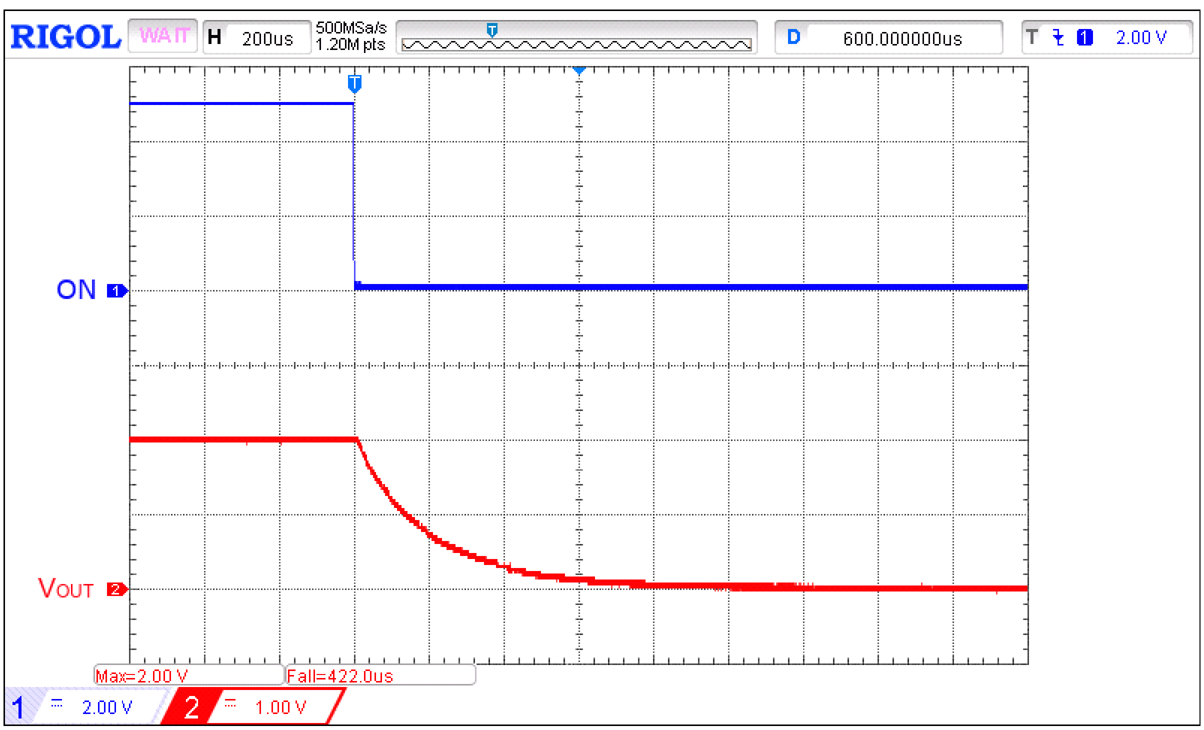


Figure 12. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 1.98 V, C_{SLEW} = 22 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

SLG5NT1757V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_{DD} first, followed by V_{IN} only after V_{DD} is > 90 % of final V_{DD}, and finally toggling the ON pin LOW-to-HIGH after V_{IN} is at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order.

If V_{DD} and V_{IN} are applied at the same time, a voltage glitch may appear on the output pin at V_{OUT}. To prevent glitches at the output, it is recommended to connect at least a 1 µF capacitor from the VOUT pin to GND and to keep the V_{DD} and V_{IN} ramp times higher than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_{IN} have reached their steady-state values the IPS timing parameters may differ from datasheet specifications.

The slew rate of output V_{OUT} follows a linear ramp set by a capacitor connected to the CAP pin. An expression for inrush current as a function of slew rate and load capacitance is:

$$V_{IN} \text{ Inrush Current} = C_{LOAD} \times \text{Slew Rate } (C_{SLEW})$$

While a larger capacitor value at the CAP pin produces a slower ramp, inrush current from V_{IN} is reduced.

Power Dissipation

The junction temperature of the SLG5NT1757V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG5NT1757V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:
PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:
T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

For more information on Dialog GreenFET3 integrated power switch features, please visit our Documents search page at our website and see App Note “AN-1068 GreenFET3 Integrated Power Switch Basics”.

Layout Guidelines:

1. The VDD pin needs a 0.1μF (or larger) external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG5NT1757V's pin 1.

2.Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 13, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3.To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG5NT1757V's VIN and VOUT pins;

4.The GND pin should be connected to system analog or power ground plane.

5. 2 oz. copper is recommended for high current operation.

SLG5NT1757V Evaluation Board:

A GFET3 Evaluation Board for SLG5NT1757V is designed according to the statements above and is illustrated on Figure 13. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

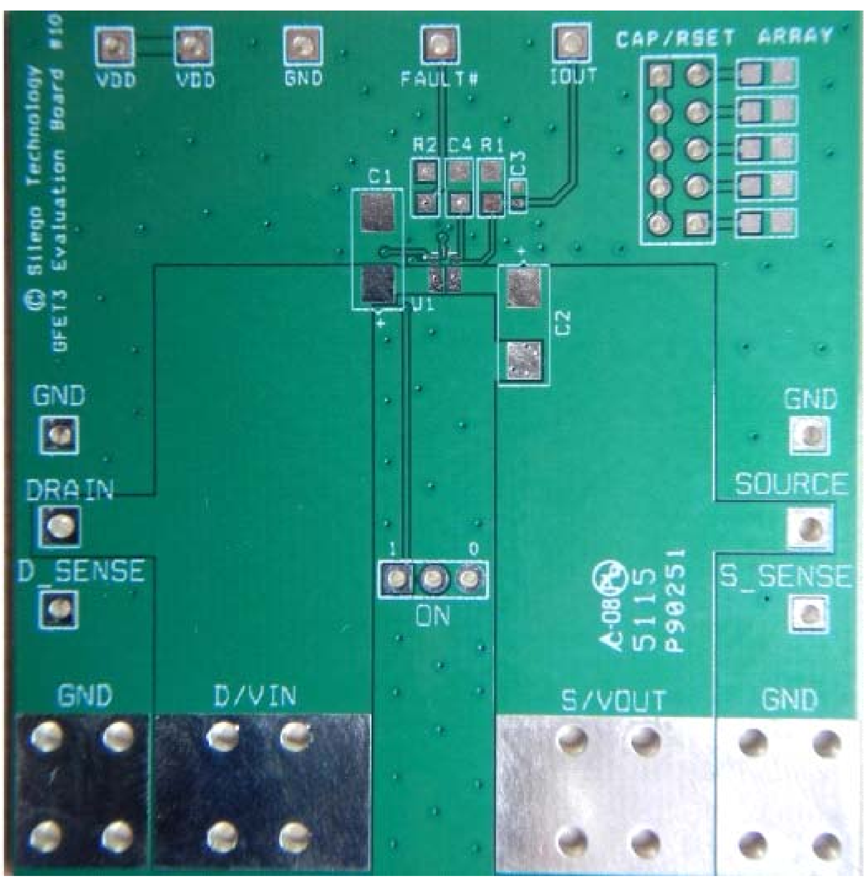


Figure 13. SLG5NT1757V Evaluation Board

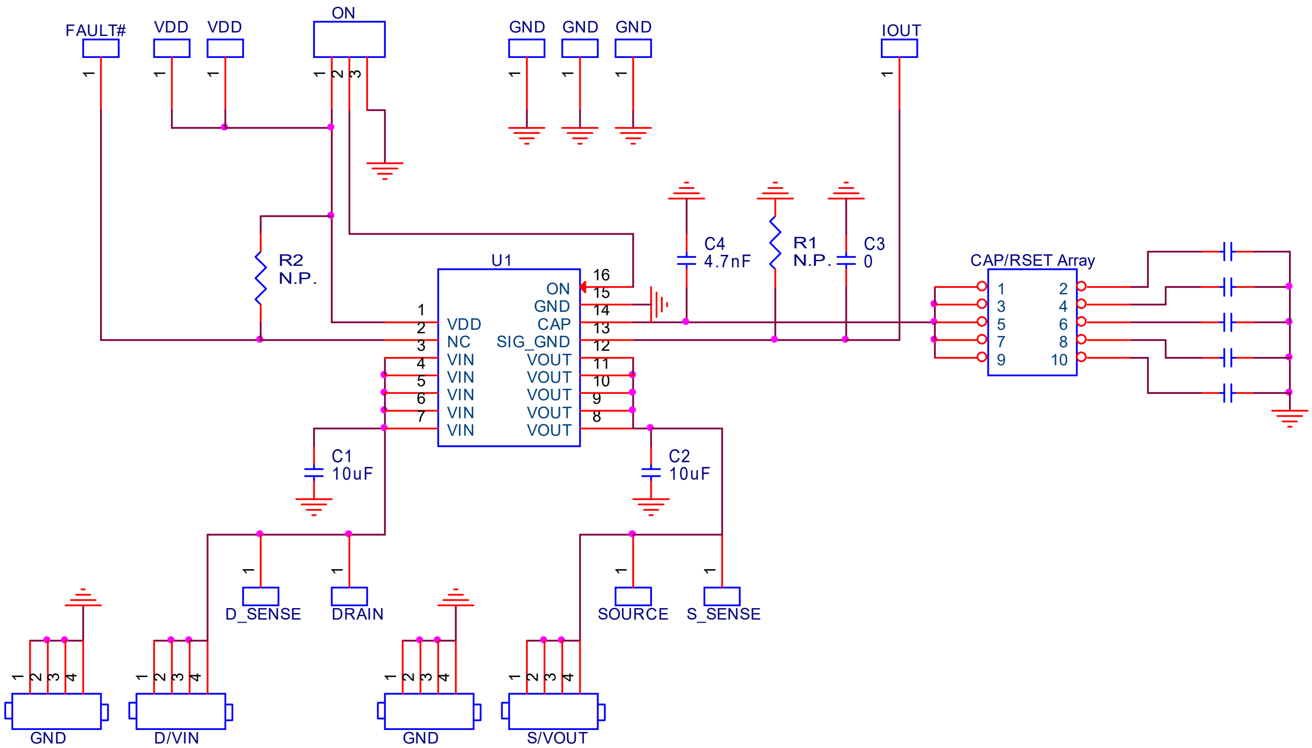


Figure 14. SLG5NT1757V Evaluation Board Connection Circuit

Basic Test Setup and Connections

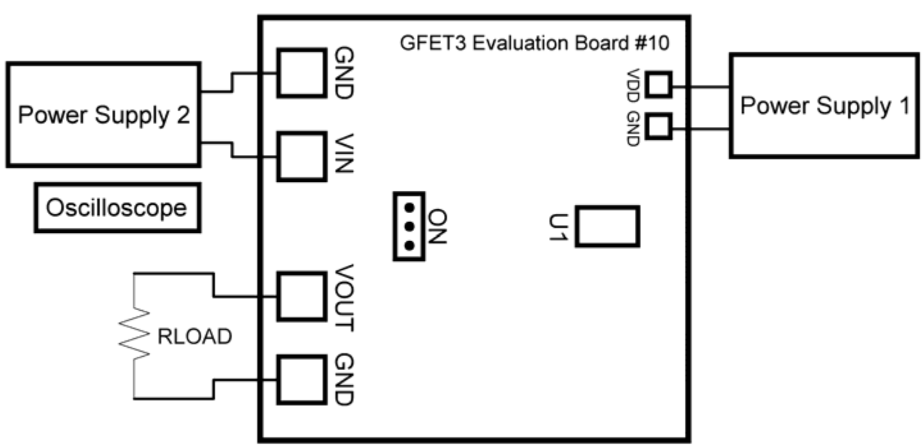


Figure 15. SLG5NT1757V Evaluation Board Connection Circuit

EVB Configuration

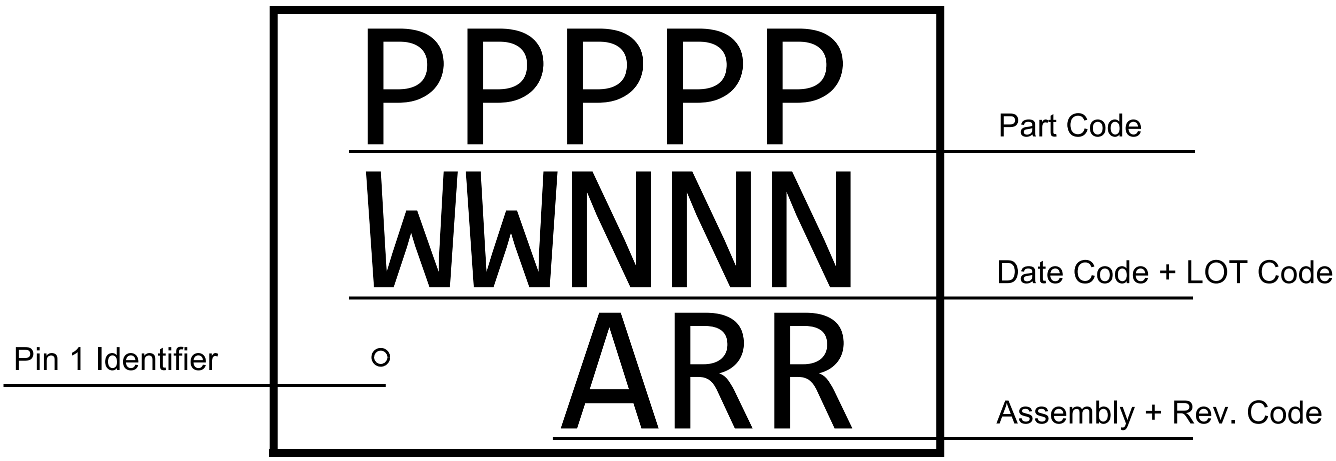
1. Connect oscilloscope probes to VIN, VOUT, ON, etc.;

2. Turn on Power Supply 1 and set desired V_{DD} from 3 V…5.5 V range;

3. Turn on Power Supply 2 and set desired V_{IN} from 0.6 V…1.98 V range;

4 .Toggle the ON signal High or Low to observe SLG5NT1757V operation.

Package Top Marking System Definition

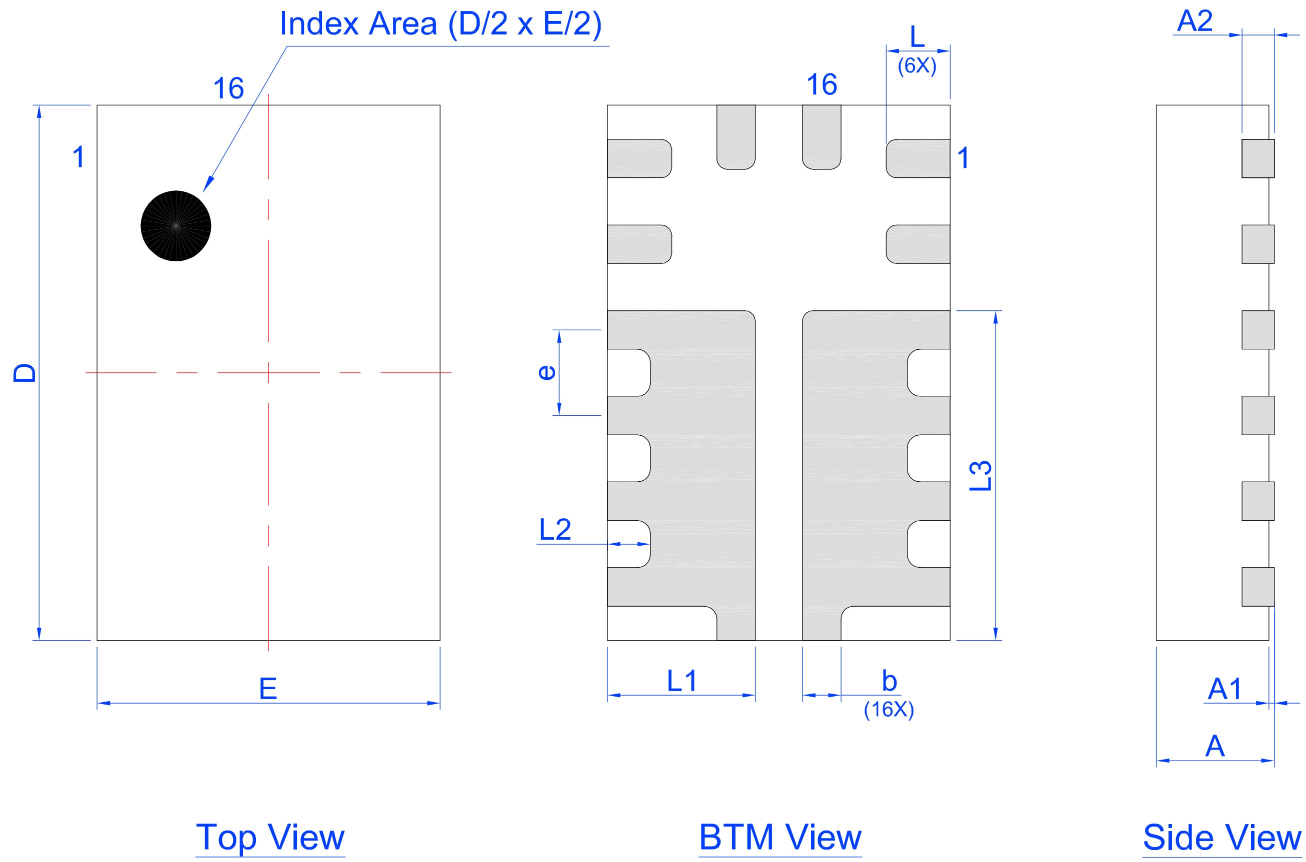


PPPPP - Part ID Field
WW - Date Code Field[1]
NNN - Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
RR - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

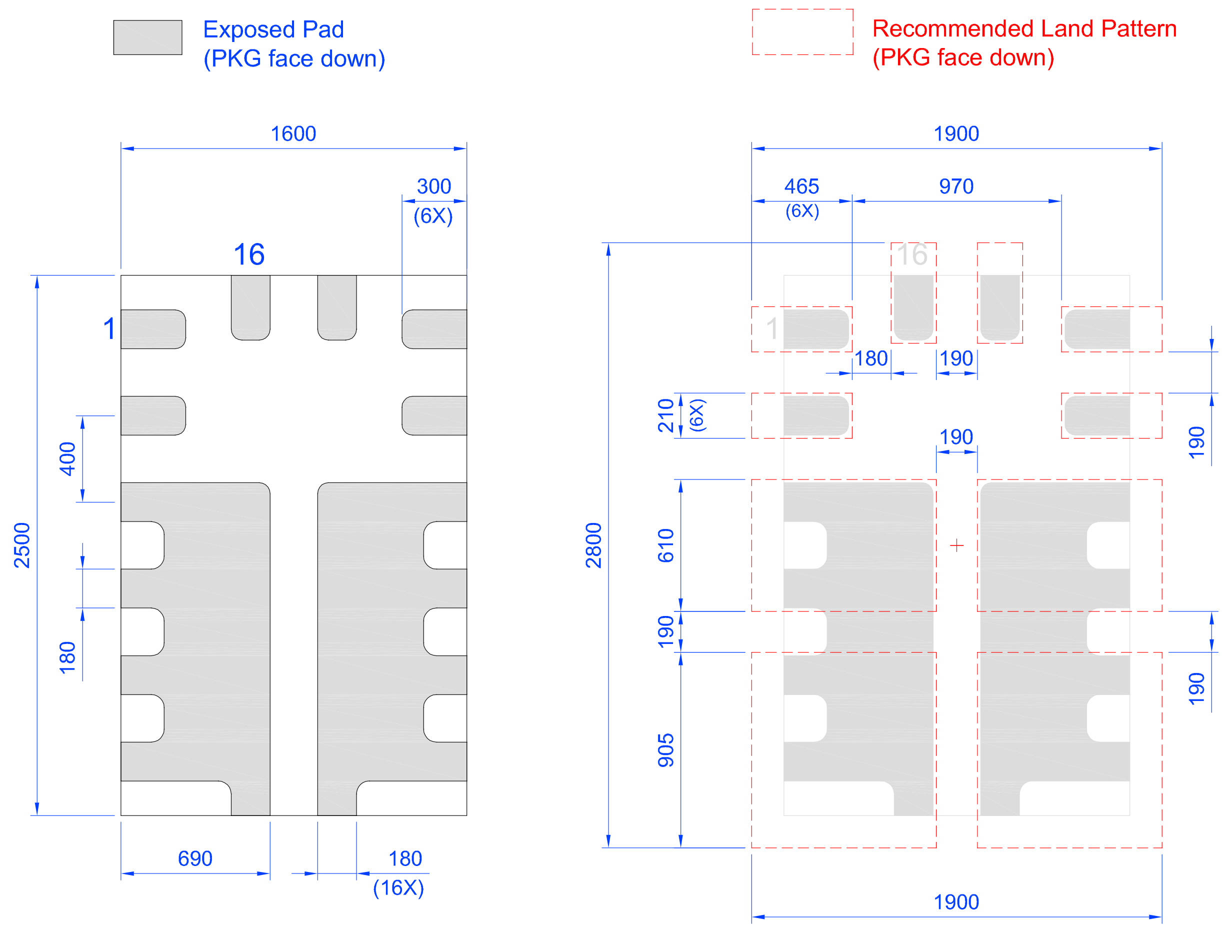
16 Lead STQFN Package 1.6 mm x 2.5 mm (Fused Lead)



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.45	2.50	2.55
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
				L3	1.49	1.54	1.59

SLG5NT1757V 16-pin STQFN PCB Landing Pattern



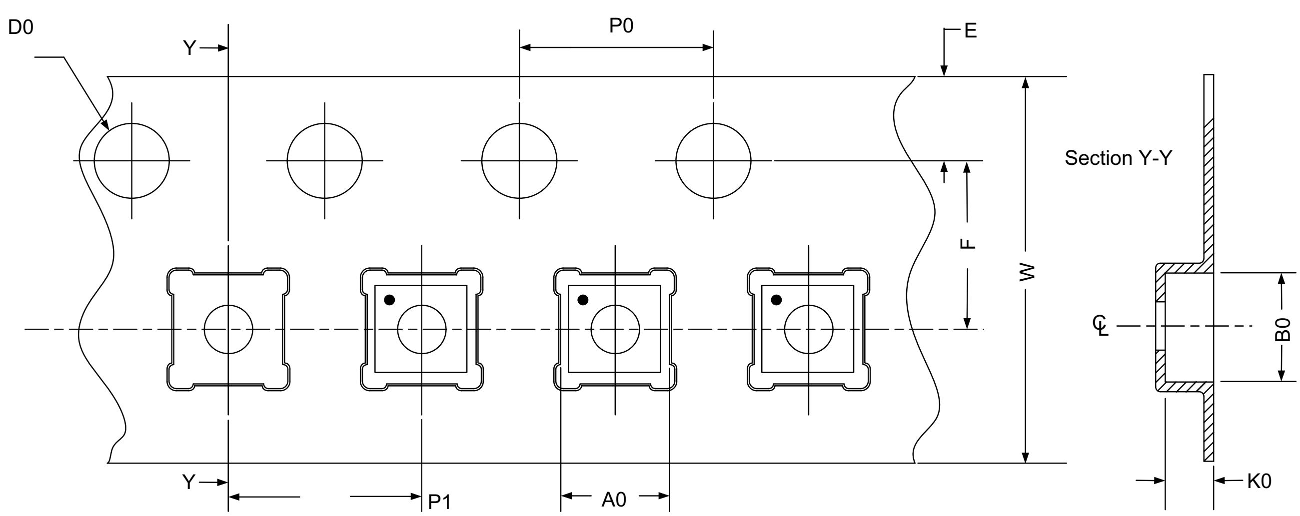
Unit: um

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 16L 1.6x2.5mm 0.4P FCA Green	16	1.6x2.5x 0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 16L 1.6x2.5mm 0.4P FCA Green	1.8	2.8	0.7	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
02/24/2020	1.03	Updated Toff_delay charts
12/21/2018	1.02	Updated RDSon and related charts
11/28/2018	1.01	Added Layout Guidelines Fixed typos
6/21/2018	1.00	Production Release