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PmodAD5™ Reference Manual

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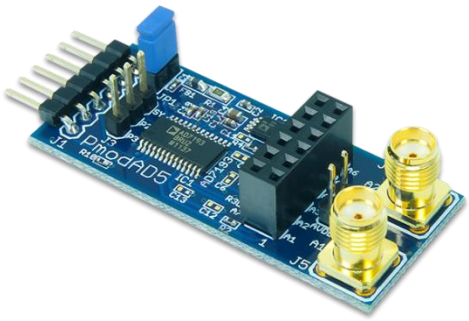
This manual applies to the PmodAD5 rev. A

Overview

The Digilent PmodAD5 is an analog-to-digital converter (ADC) that utilizes a fourth order Σ-Δ modulator, a programmable gain array, and on-chip digital filtering including a variety of sinc filters and zero latency features.



The PmodAD5.

Features include:

- High precision 24-bit Sigma-Delta analog-to-digital converter
- 4 differential or 8 pseudo differential input channels
- Ultra-low noise
- Programmable gain (1 to 128)
- Flexible digital filter with fast settling option
- Two SMA connectors
- Small PCB size for flexible designs 1.9“ × 0.8” (4.8 cm × 2.0 cm)
- 6-pin Pmod connector with SPI interface
- Follows Digilent Interface Specification Type 2

1 Functional Description

The PmodAD5 utilizes Analog Devices AD7193 to provide 4 differential or 8 pseudo differential analog inputs. With 24-bit resolution and rms noise as low as 11 nV, highly accurate voltage measurements can be taken.

2 Interfacing with the Pmod

The PmodAD5 communicates with the host board via the SPI protocol. By driving the Chip Select line low, users can transfer information to and from the device with the most significant bit (MSB) first.

The default setting of the AD7193 upon power-up is that a single analog-to-digital conversion is made comparing the voltage difference between pins A1 (+) and A2 (-) on header J2. The input voltage that is allowed with the default settings is ±19.53 mV with respect to the on-board reference voltage of 2.5V. Users are able to receive the

24 bits of data by first pulling the chip select line low and waiting the required conversion and settling time (100 ms by default). Users can then write to the communications register to indicate that they want to read the data and then clock in the 24 bits of data from the data register and finally pull the chip select line back to a high voltage state. An example of what the data stream might look like is given below:

Communications Register							
~Wen	R/~W	Data Register Address			CREAD	0	0
0	1	0	1	1	0	0	0
Data Register							
Read Bits D23-D0							

Table 1. Example data stream of the measured differential voltage.

Some users may wish to have a wider voltage range than 2.5V ±19.53 mV that they are able to analyze. This can be adjusted by changing specific values within the Configuration register; namely, the Reference Select bit (D20) and the three gain bits (D2-D0).

An example bit stream that changes the Reference Select bit from the default reference of 2.5V to the user supplied reference voltage between pins REFIN2+ and REFIN2- and changes the gain from the default of 128 to 1 is provided below:

Communications Register							
~Wen	R/~W	Configuration Register Address			CREAD	0	0
0	0	0	1	0	0	0	0
Configuration Register (first 8 of 24 bits)							
Chop	0	0	REFSEL	0	Pseudo	Short	TEMP
0	0	0	1	0	0	0	0
Configuration Register (second 8 of 24 bits)							
Channel Enable bits for CH7 - CH0							
0	0	0	0	0	0	0	1
Configuration Register (last 8 of 24 bits)							
Burn	REFDET	0	BUF	U/~B	G2	G1	G0
0	0	0	1	0	0	0	0

Table 2. Example data stream of the measured differential voltage.

2.1 Pinout Description Table

Pin	Signal	Description
1	CS	Chip Select
2	MOSI	Master-Out-Slave-In
3	MISO	Master-In-Slave-Out
4	SCK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V/5V)

Table 3. Pmod header J1.

Pin	Signal	Description
1	A1	Analog Input 7
2	A2	Analog Input 8
3	A3	Analog Input 3
4	A4	Analog Input 4
5	A5	Analog Input 5
6	A6	Analog Input 6
7	A7	Analog Input 7
8	A8	Analog Input 8
9	AINCOM	Common Analog Input
10	REFIN2+	Reference Input 2 +
11	REFIN2-	Reference Input 2 -
12	BPDSW	Bridge Power-down Switch

Table 4. Pmod header J2 (note that pin 1 is on the lower-right hand corner of the header).

Any incoming input voltage to be measured must be within ±(AV_{DD}-1.25V)/gain. As AV_{DD} must be within 3V and 5.25V, if a 5V power supply is used, the largest possible range of incoming input voltage is -3.75V to 3.75V. By default, the jumper on JP1 is loaded such that the AVDD voltage matches the DVDD voltage. If users want to apply a higher AVDD voltage to header J4 so that they are able to utilize larger reference voltages, the jumper block from JP1 must be removed so that the two voltage sources are disconnected.

Any external power applied to the PmodAD5 must be within 3V and 5.25V; however, it is recommended that Pmod is operated at 3.3V.

3 Physical Dimensions

The pins on the pin header are spaced 100 mil apart. The PCB is 1.9 inches long on the sides parallel to the pins on the pin header and 0.8 inches long on the sides perpendicular on the pin header.

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