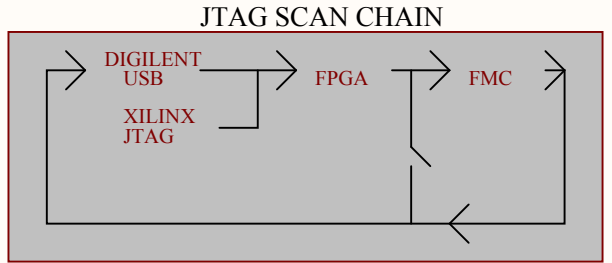
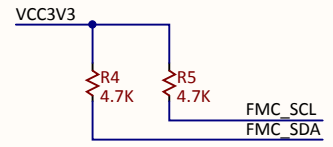
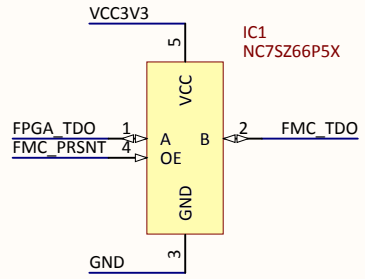
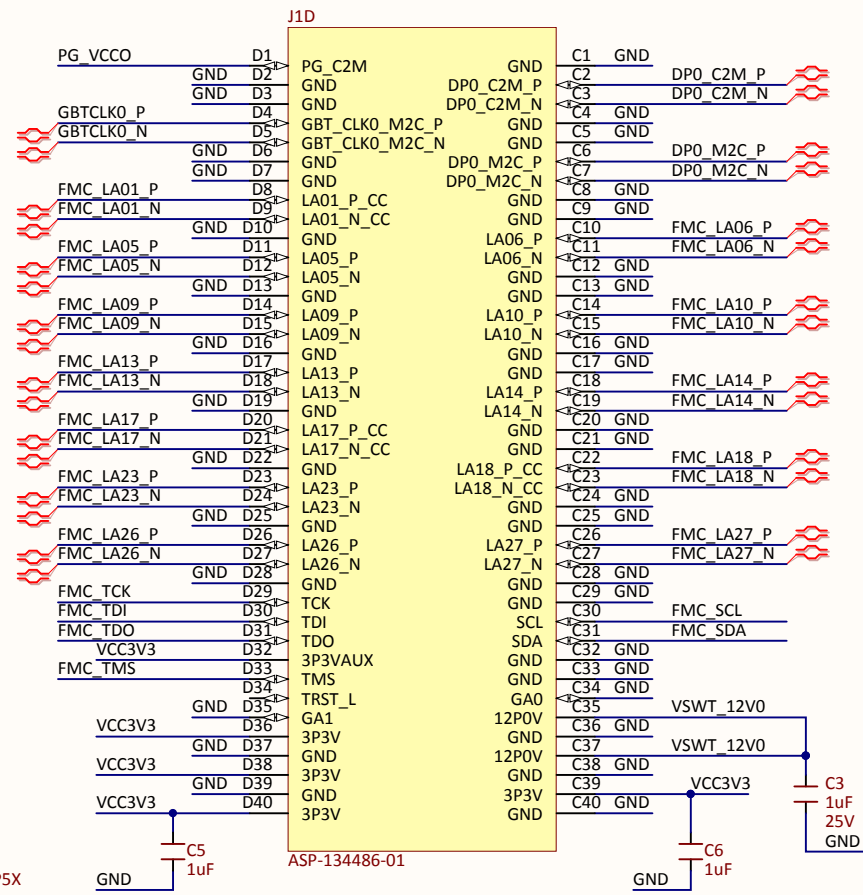
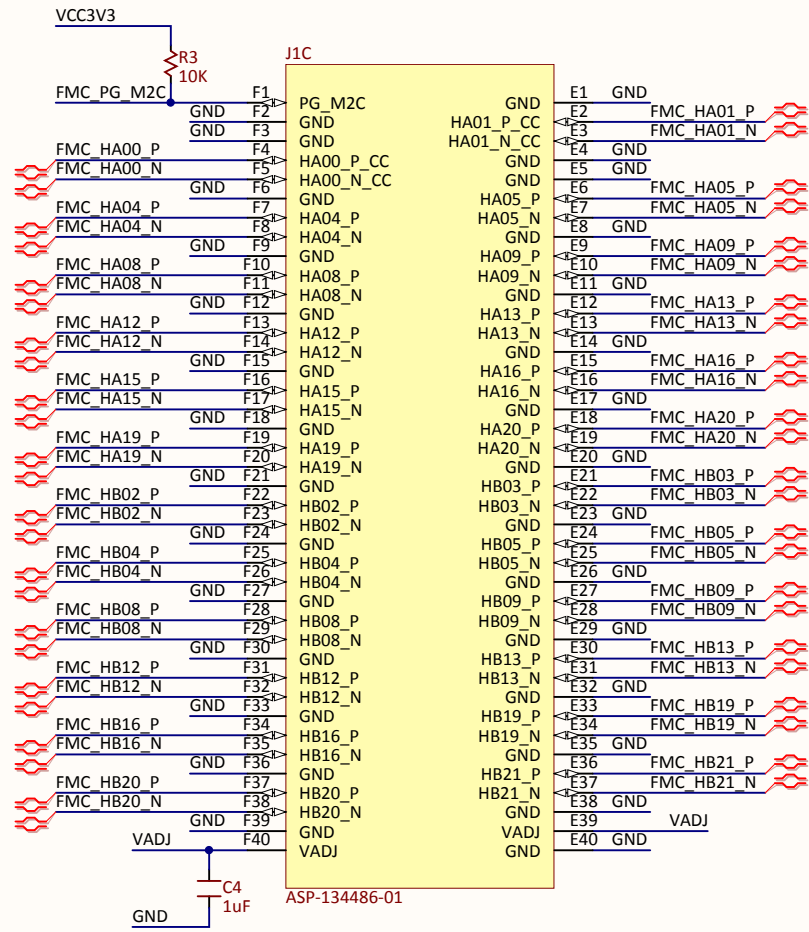


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- SHIELD F Foot F2
- SHIELD F Foot F3
- SHIELD F Foot F4
- F5 Heatsink

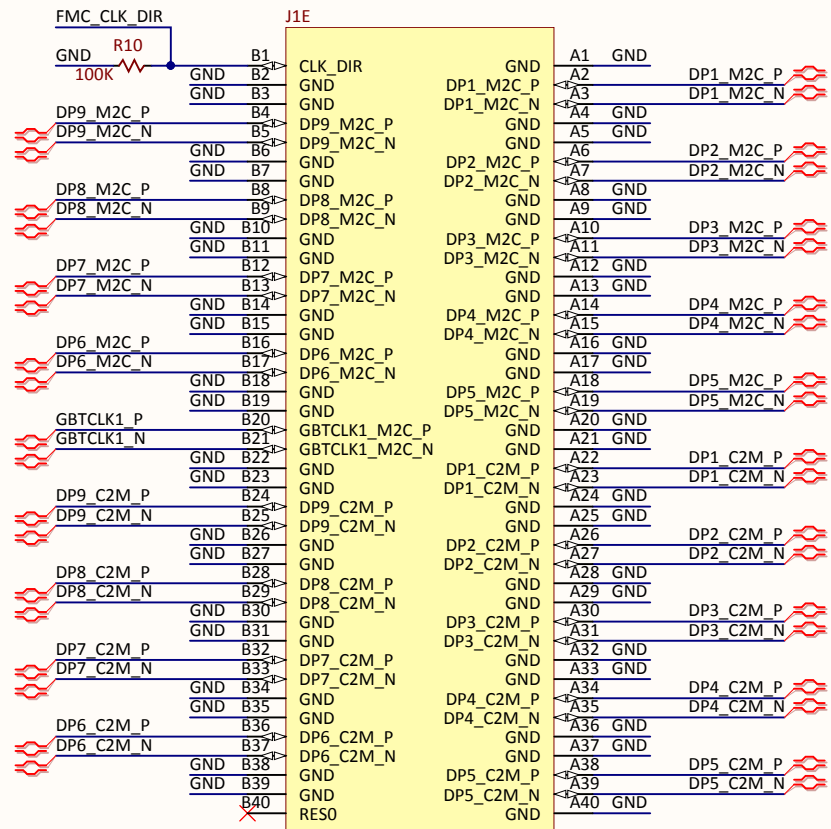
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- Genesys2
- Digilent Inc.
- Linear Tech
- Chinese ROHS

Malico MBF31035-24P + Sunon MC30101V1-0000-G99

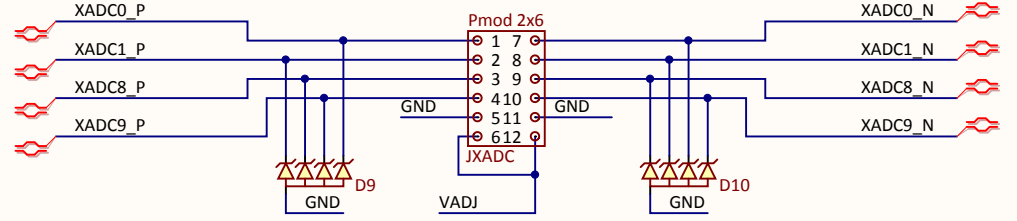
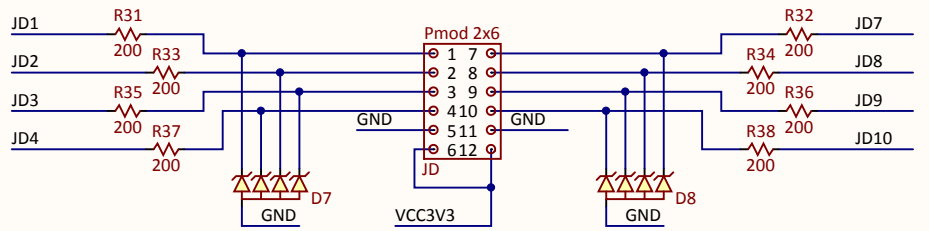
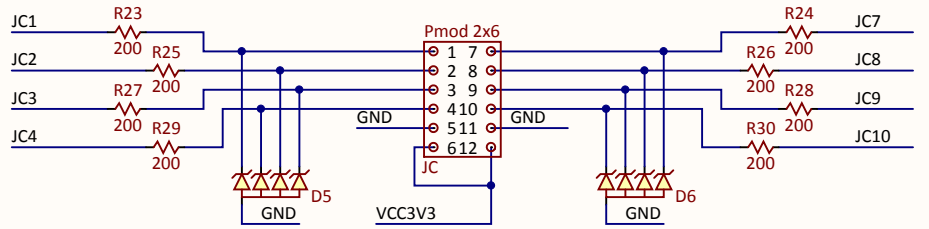
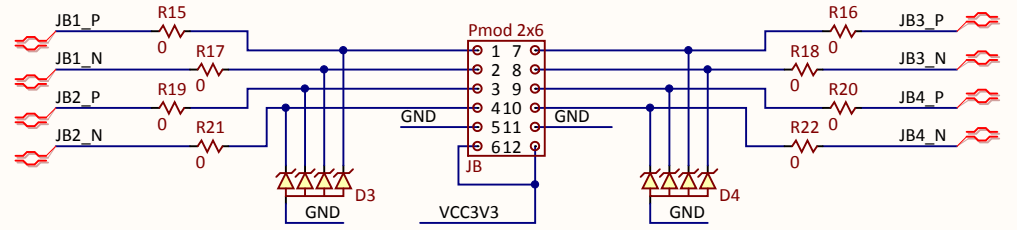
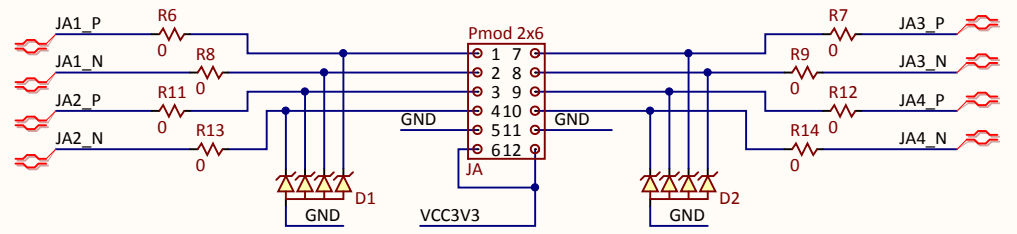
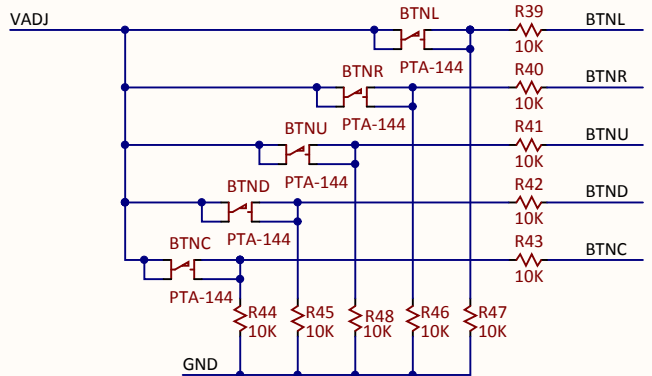
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Circuit		FMC CONNECTOR	
Doc#	500-300		
Engineer	EG		
Author	DL		
Date	7/17/2015		
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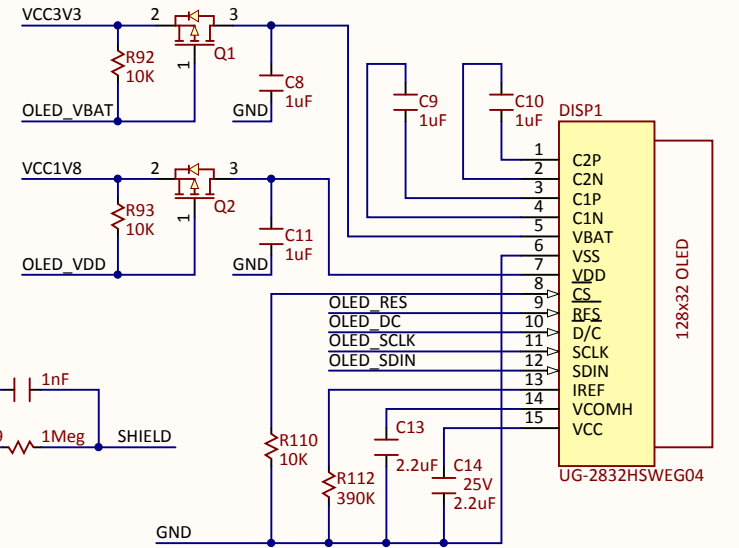
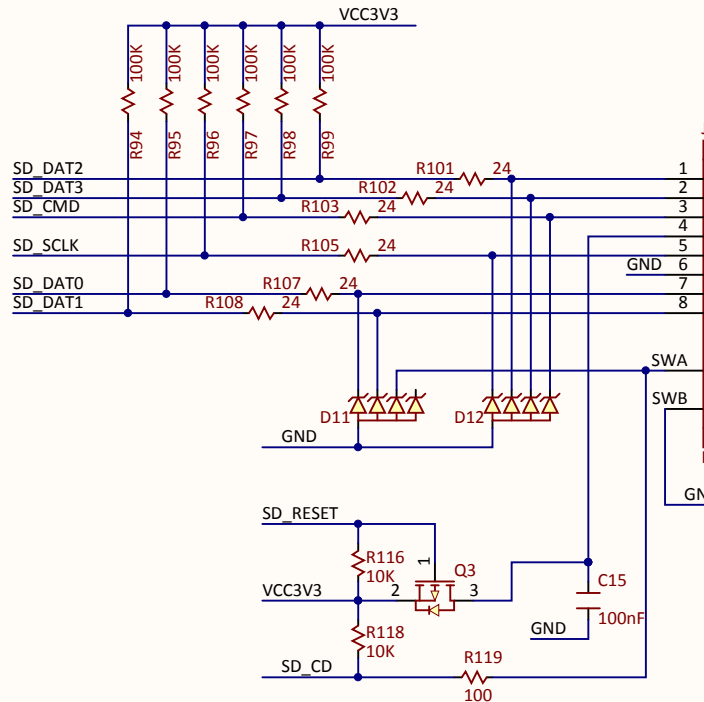
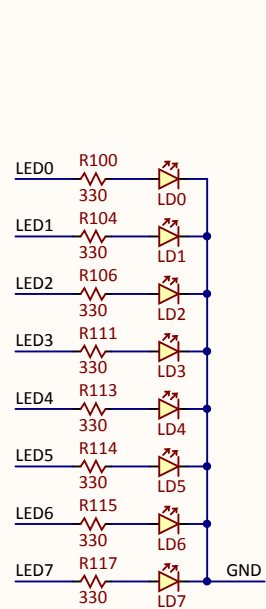
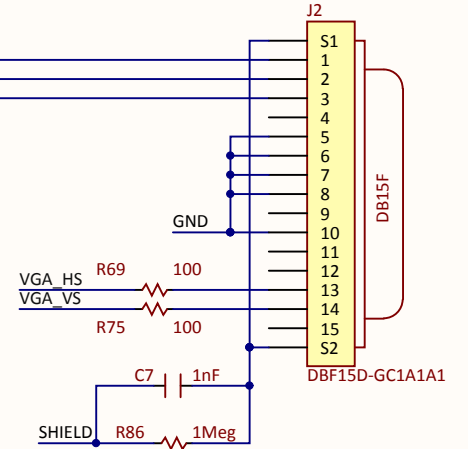
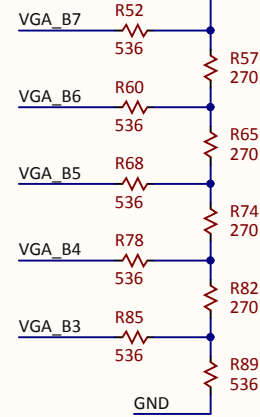
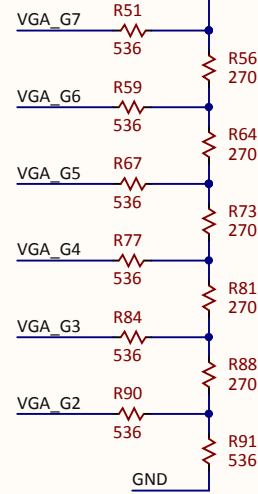
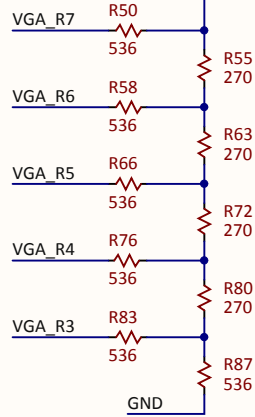
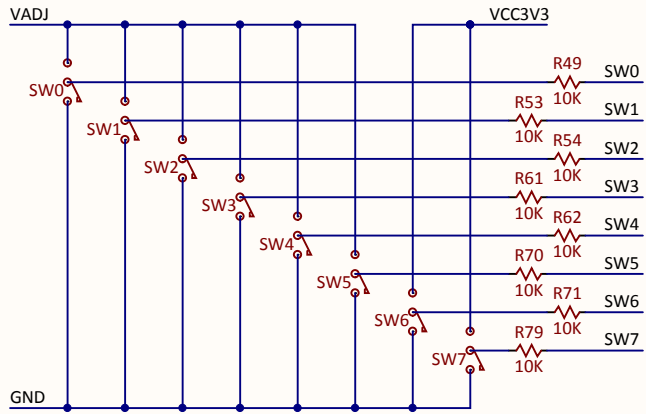
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Genesys 2		H.1	
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FMC CONNECTOR			
Doc# 500-300			
Engineer EG			
Author DL			
Date 7/17/2015			
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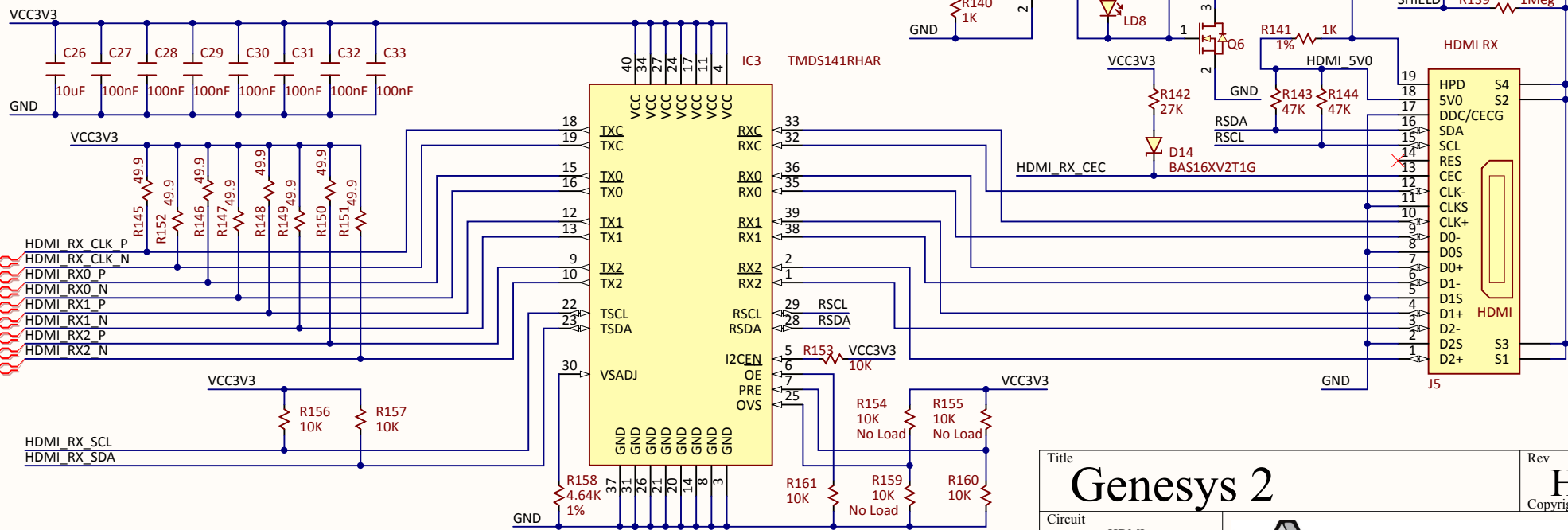
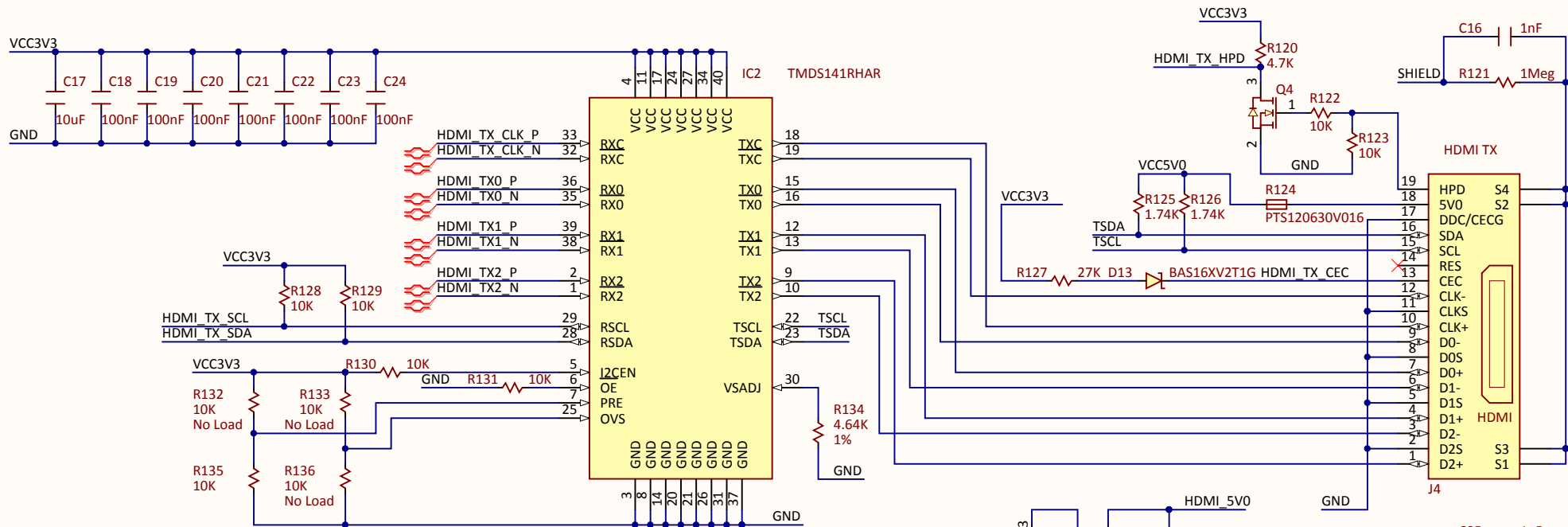
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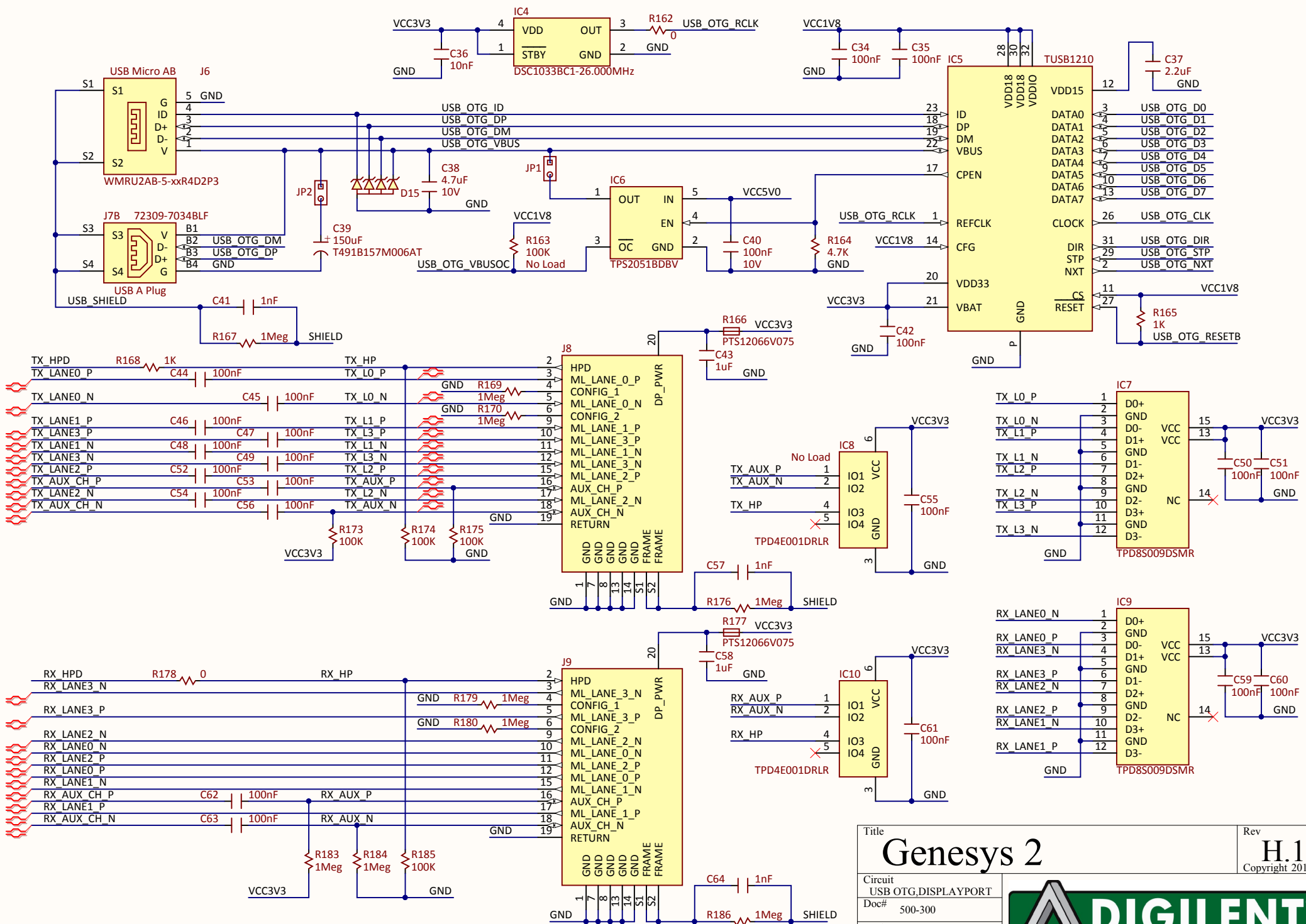
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Genesis 2		H.1
Circuit		Copyright 2015
FMC, PMods, GPIO		
Doc#	500-300	
Engineer	EG	
Author	DL	
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Genesis 2		H.1
Circuit VGA, OLED, SD, GPIO		Copyright 2015
Doc#	500-300	
Engineer	EG	
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Genesis 2		H.1	
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Circuit	HDMI		
Doc#	500-300		
Engineer	EG		
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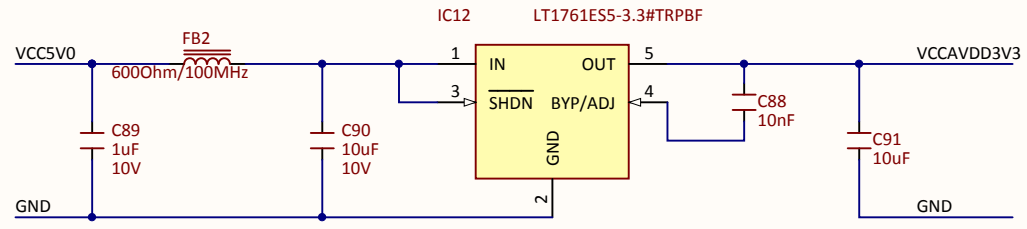
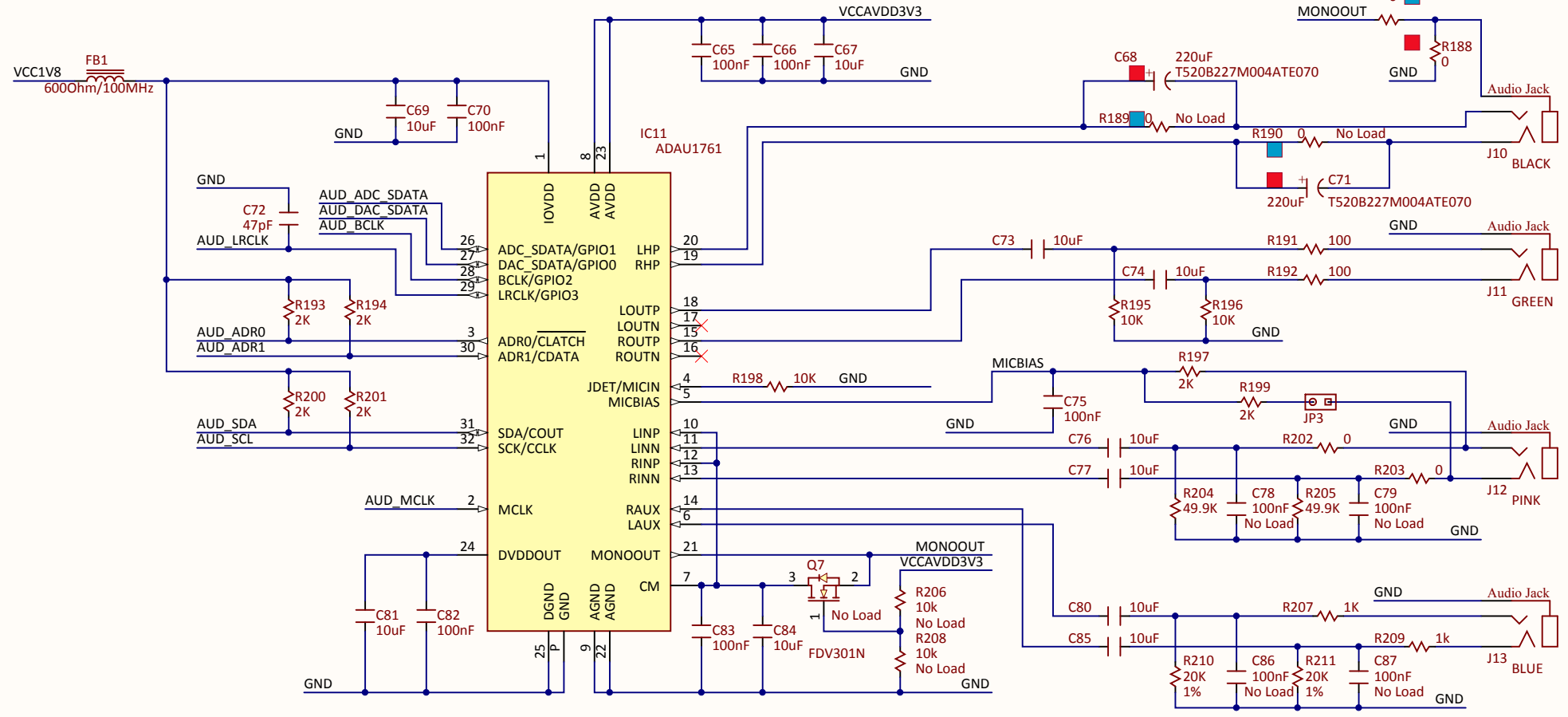


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Author	DL		
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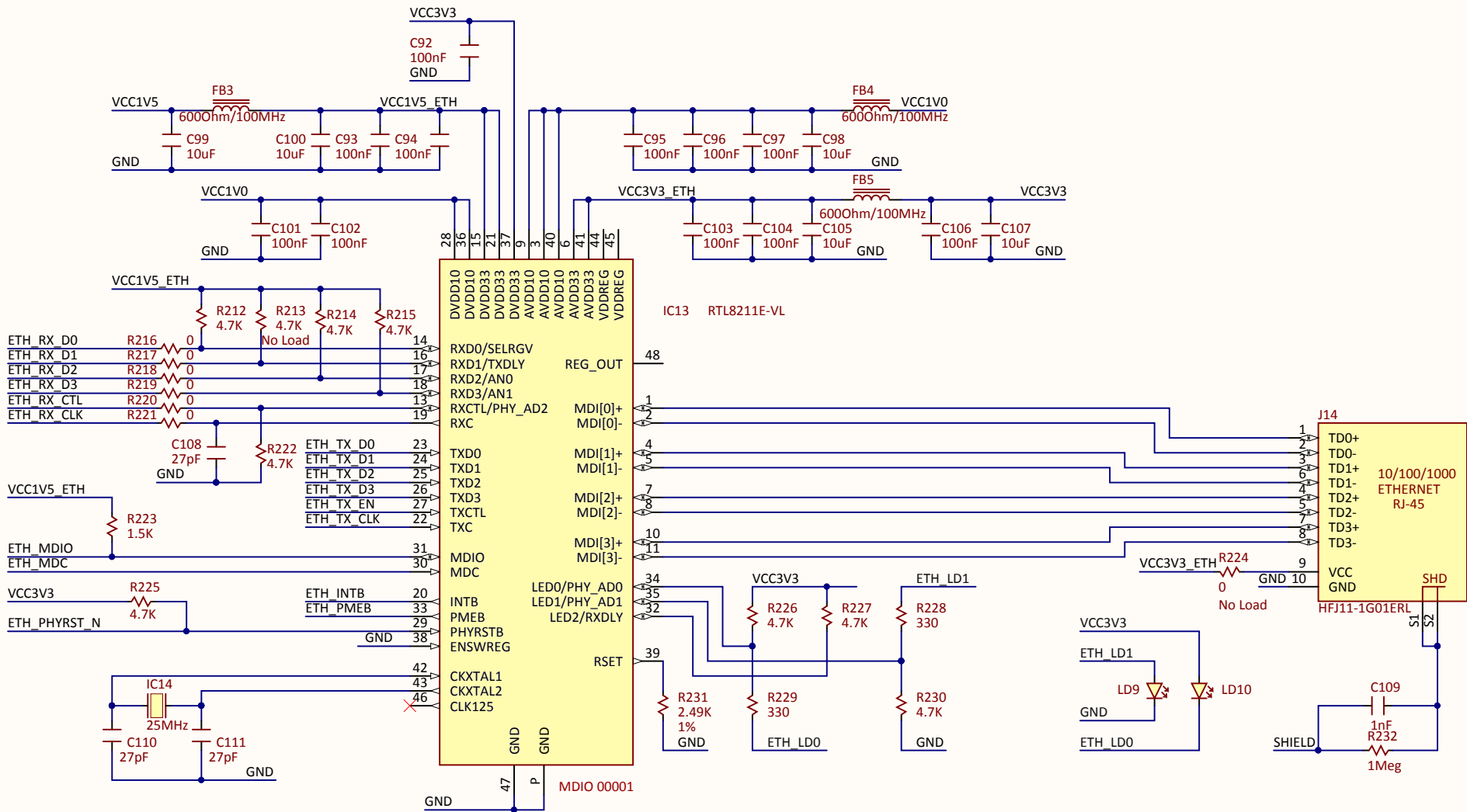
DIGILENT
BEYOND THEORY

NOTE: Load No Load
 Capless Headphone ■ ■
 AC-Coupled Headphone ■ ■




Title		Rev	
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Circuit	AUDIO		
Doc#	500-300		
Engineer	EG		
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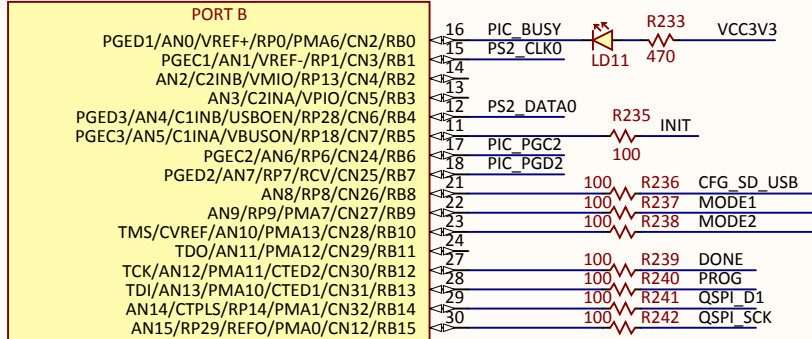


Title		Genesys 2		Rev		H.1	
Circuit		ETHERNET		Doc#		500-300	
Author		DL		Date		7/17/2015	
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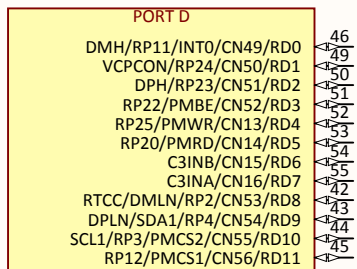
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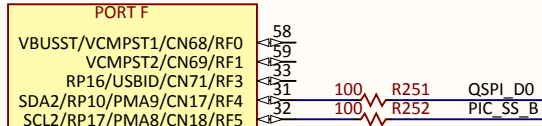
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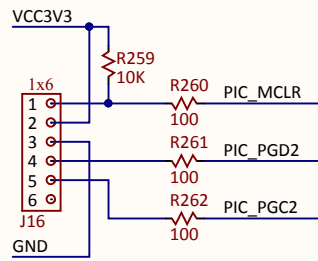
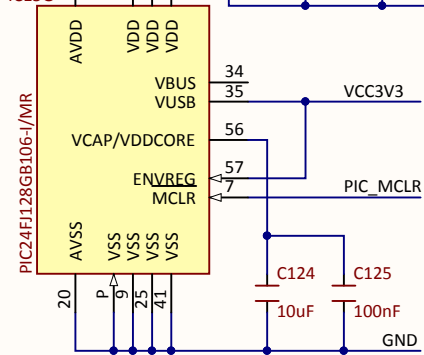
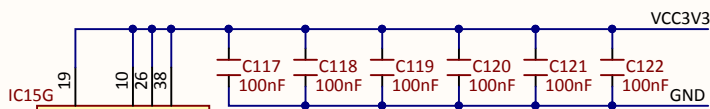


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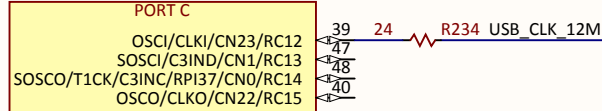
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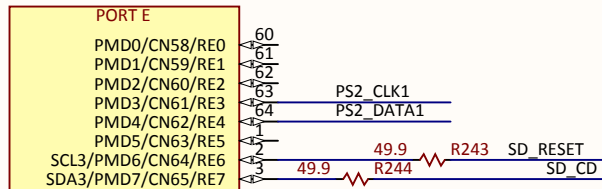


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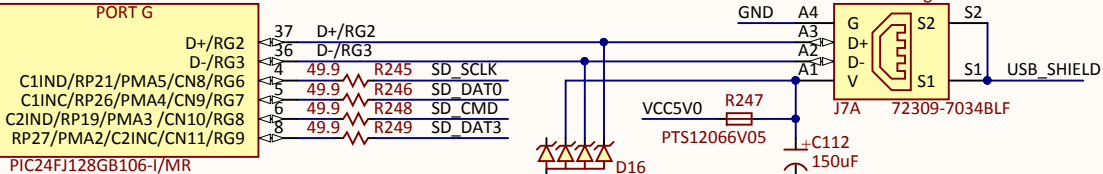
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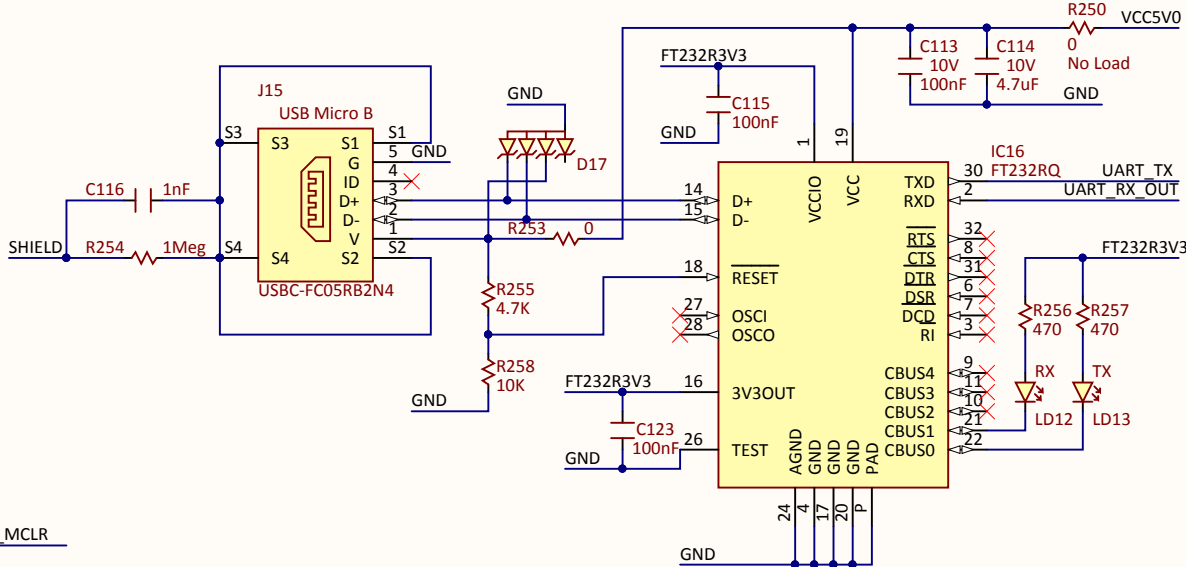


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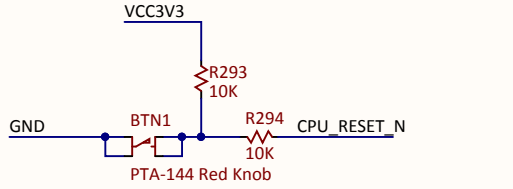
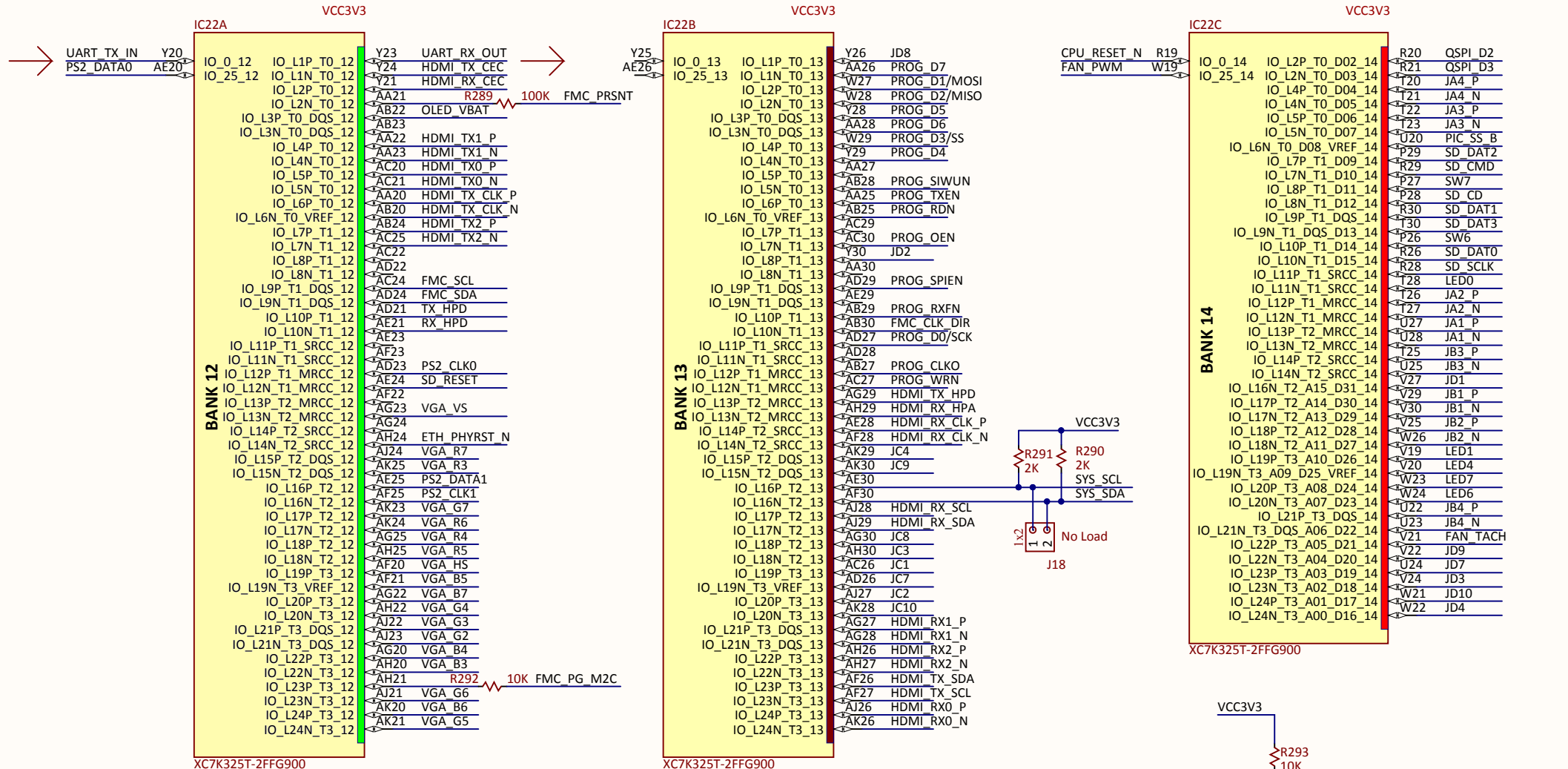


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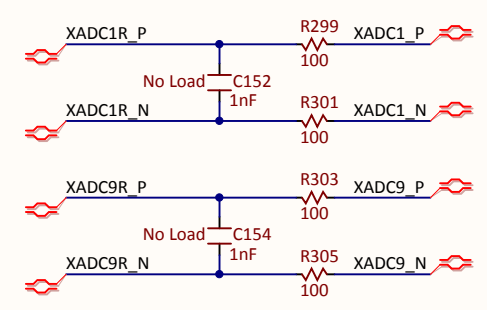
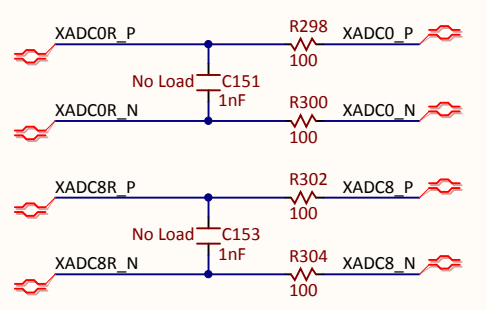
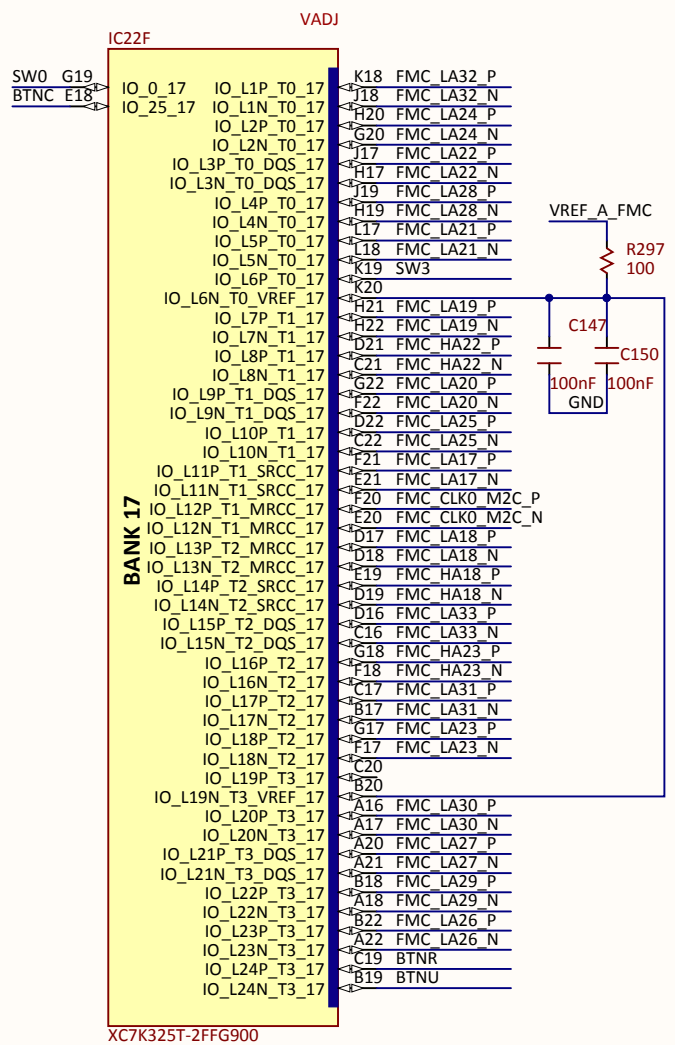
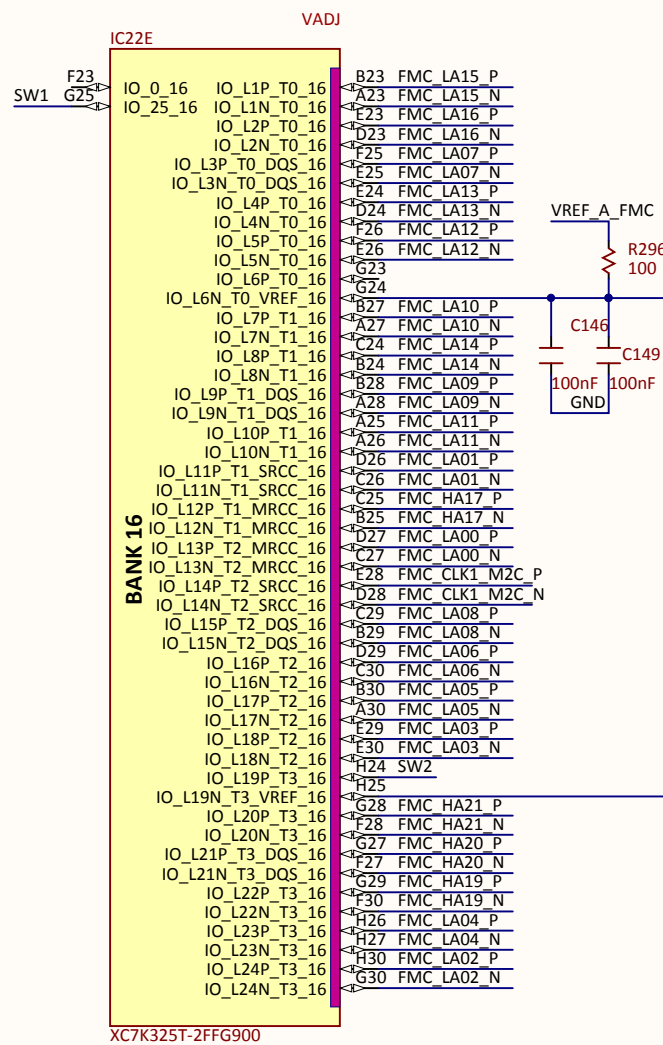
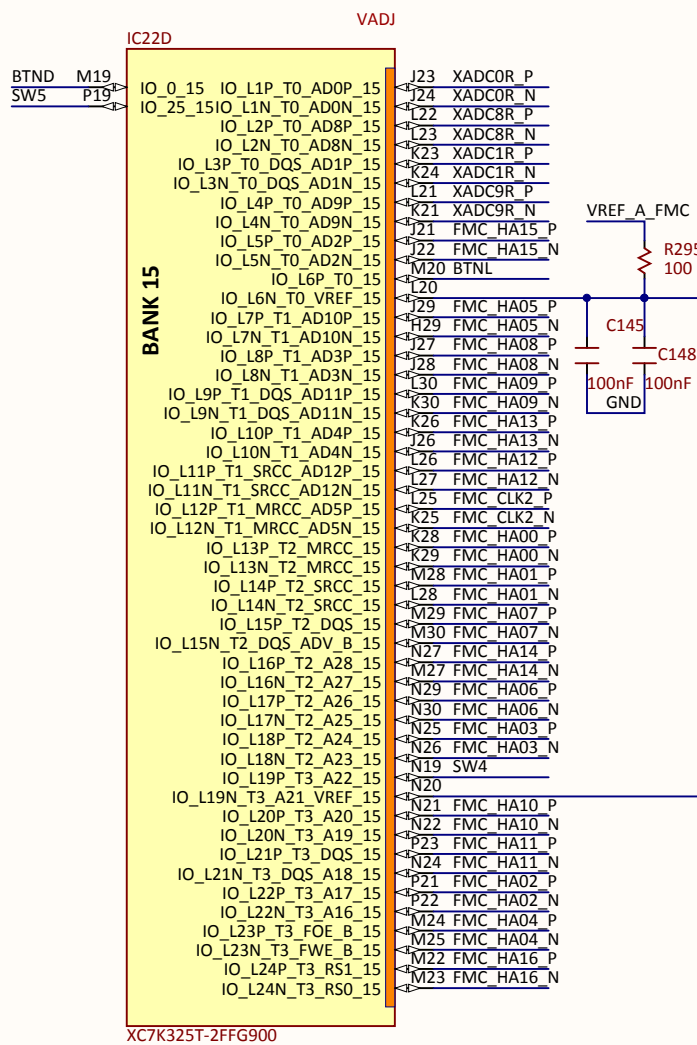


Title		Rev
Genesis 2		H.1
Circuit		Copyright 2015
USB HID, UART		
Doc#	500-300	
Engineer	EG	
Author	DL	
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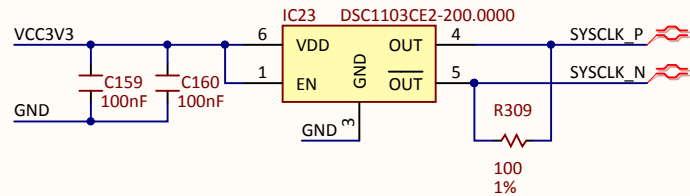
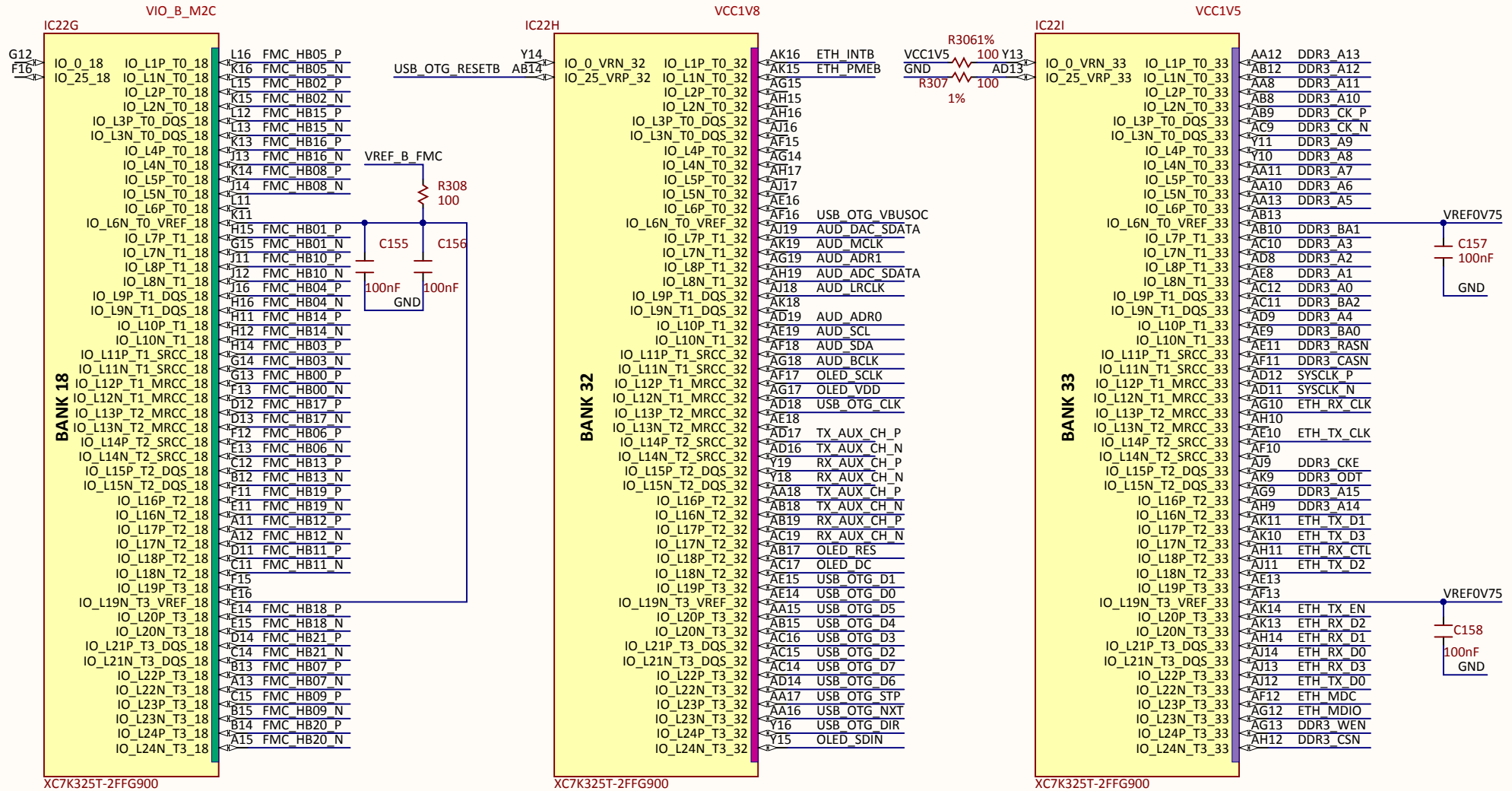


Title Genesys 2		Rev H.1 Copyright 2015
Circuit FPGA BANKS	Doc# 500-300	
Engineer EG	Author DL	
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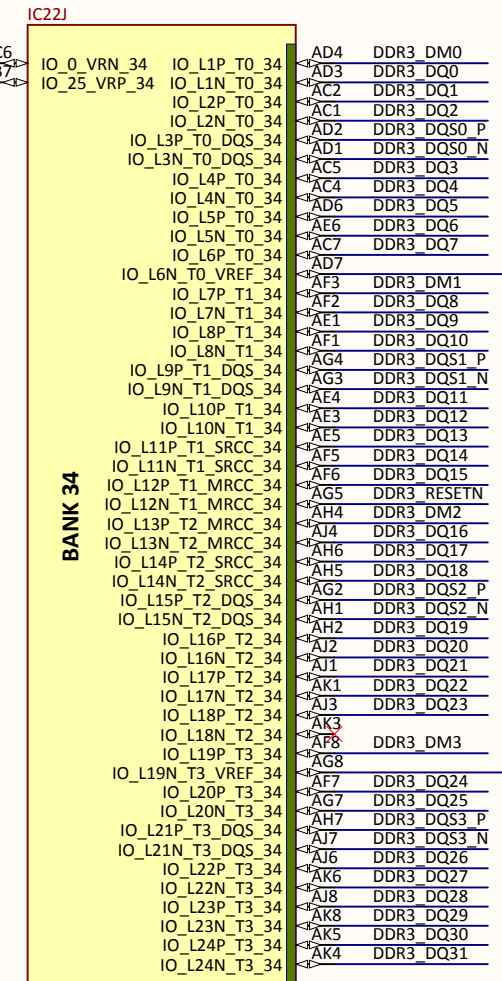


Title		Rev
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Author	DL	
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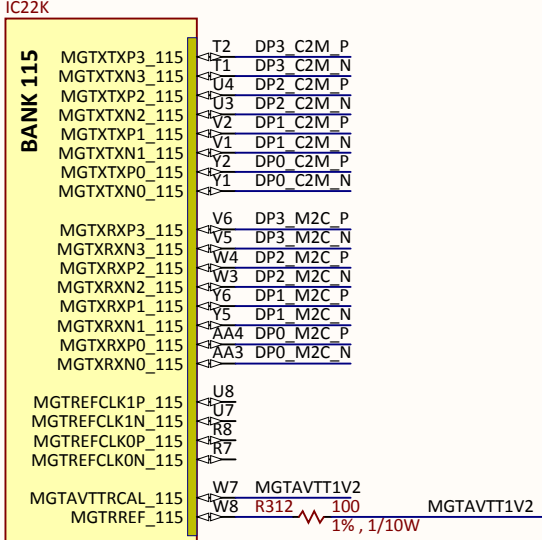




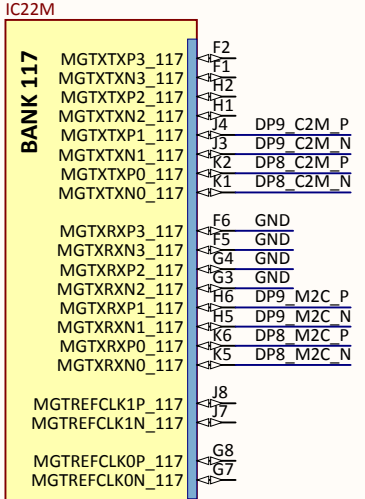
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Circuit		Copyright 2015
FPGA BANKS		
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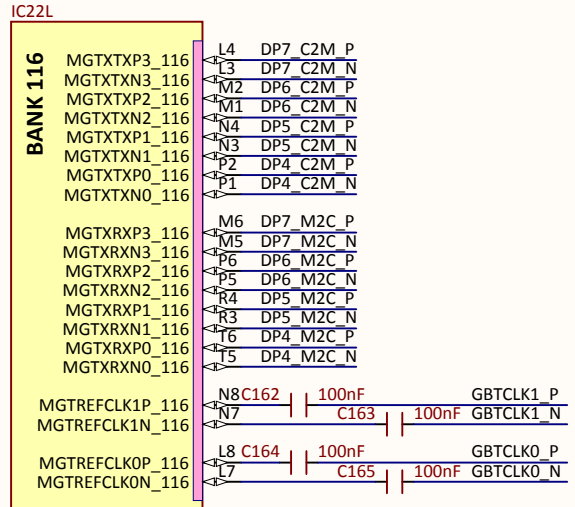
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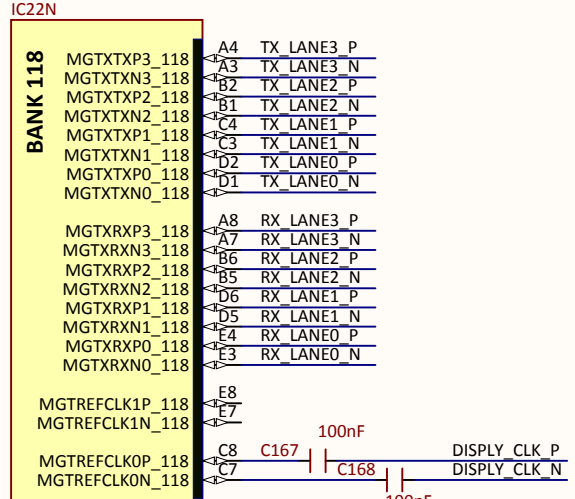
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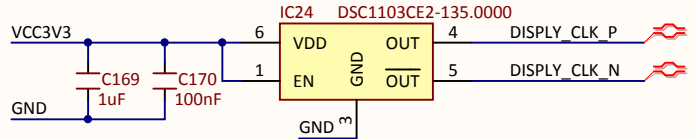
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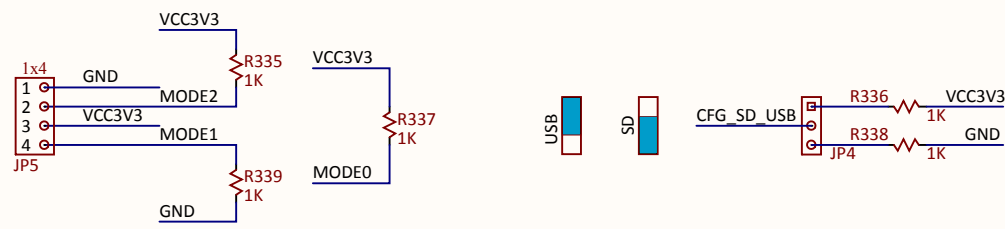
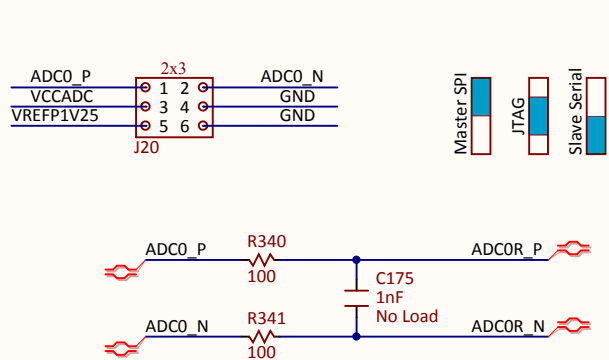
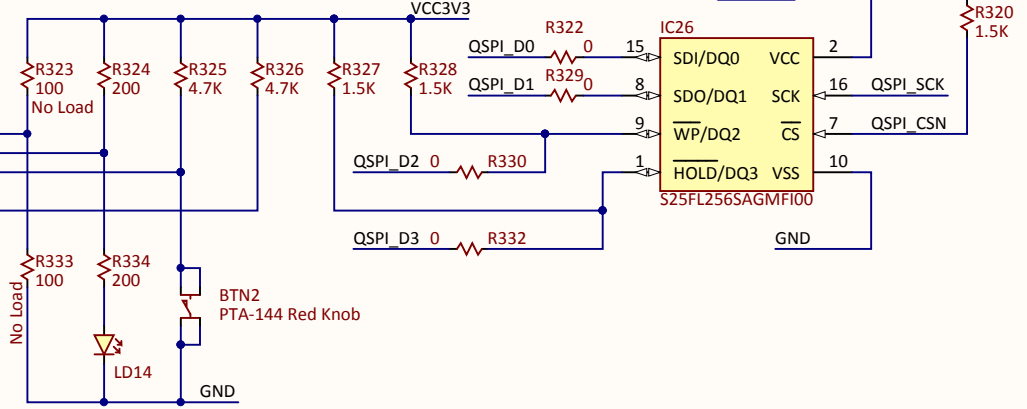
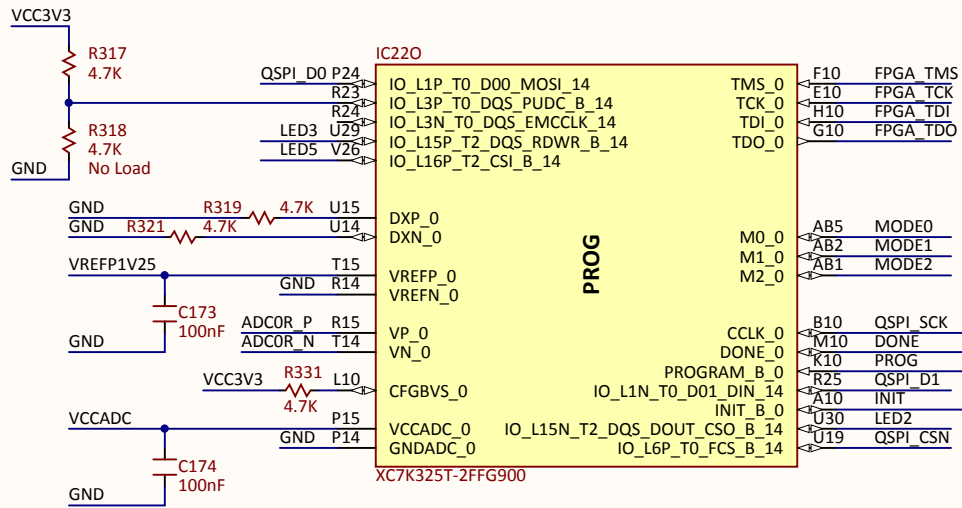
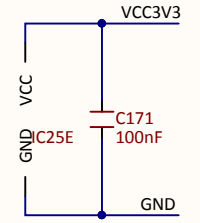
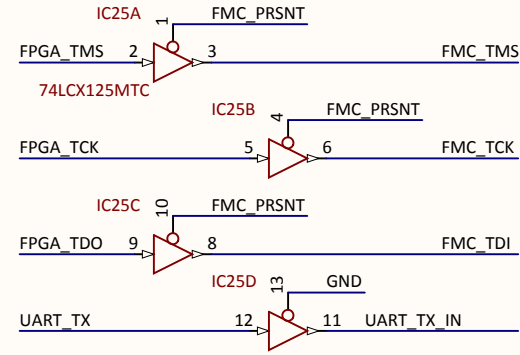
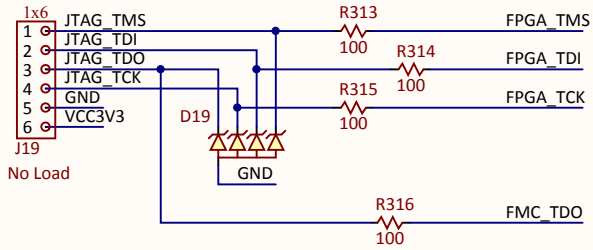
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XC7K325T-2FFG900



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Circuit	FPGA BANKS	
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Circuit CONFIG, SPI FLASH		
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A

B

C

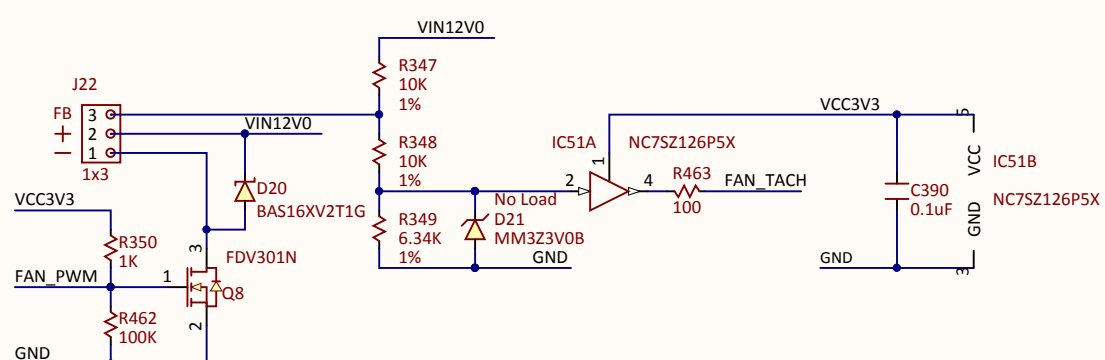
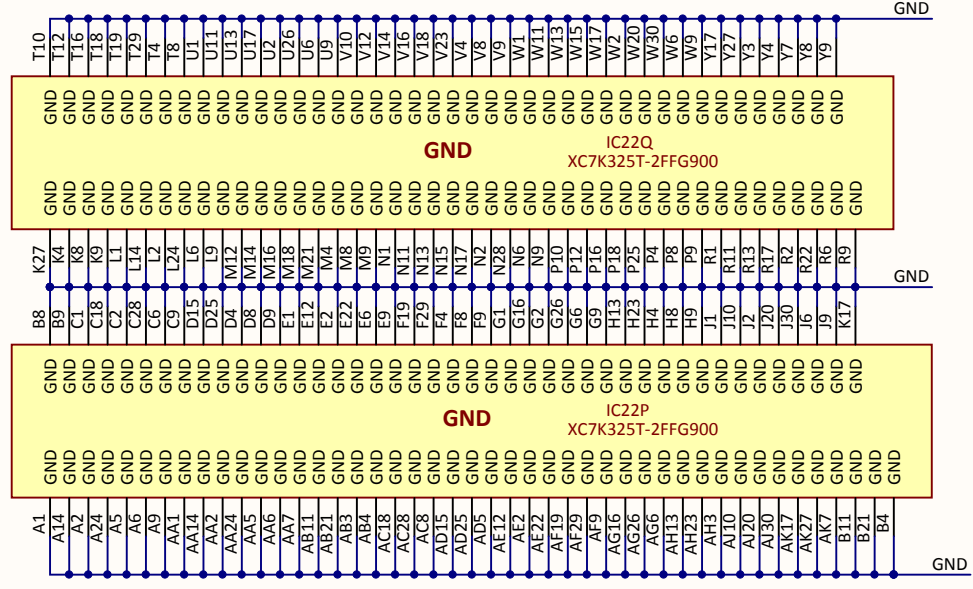
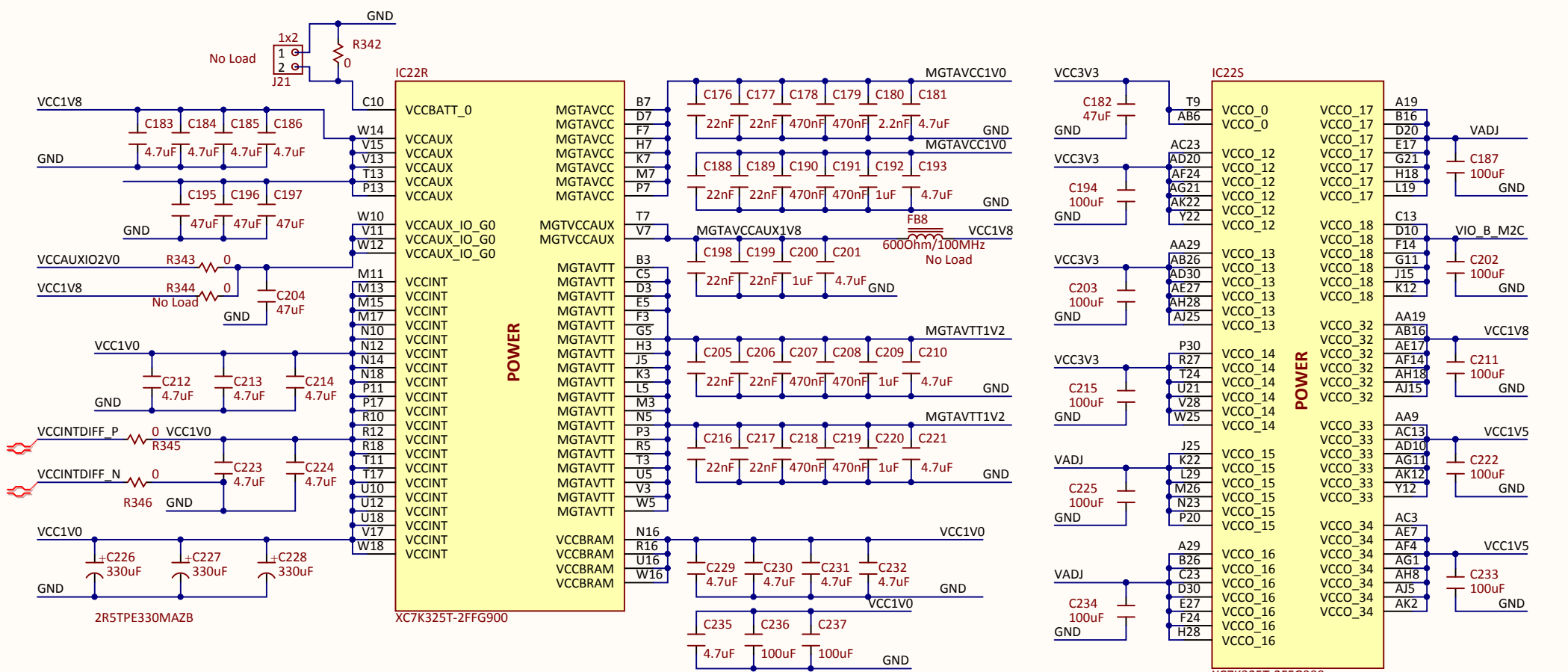
D

A

B

C

D



Title		Rev	
Genesys 2		H.1	
Circuit		Copyright 2015	
FPGA POWER			
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A

A

B

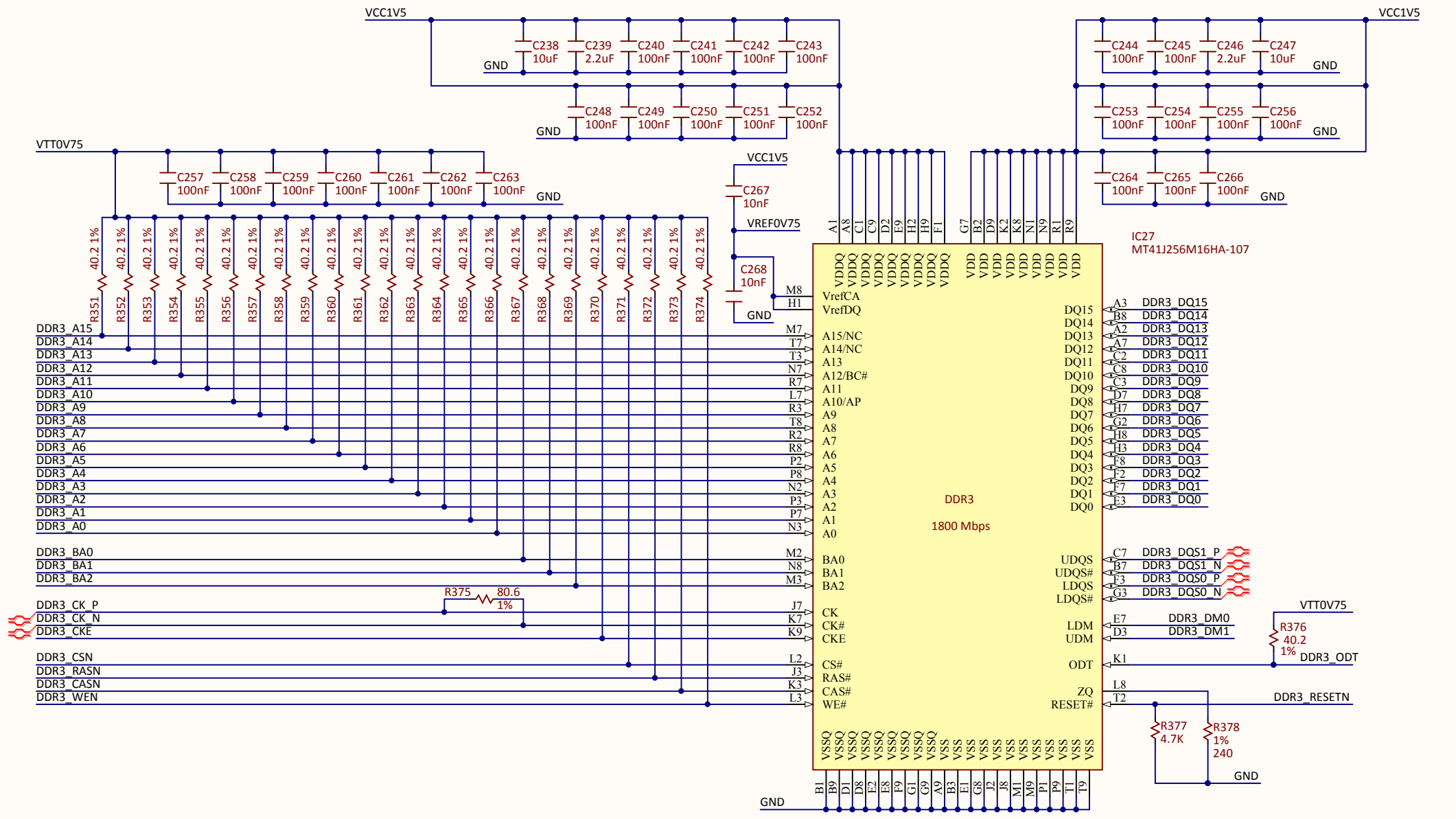
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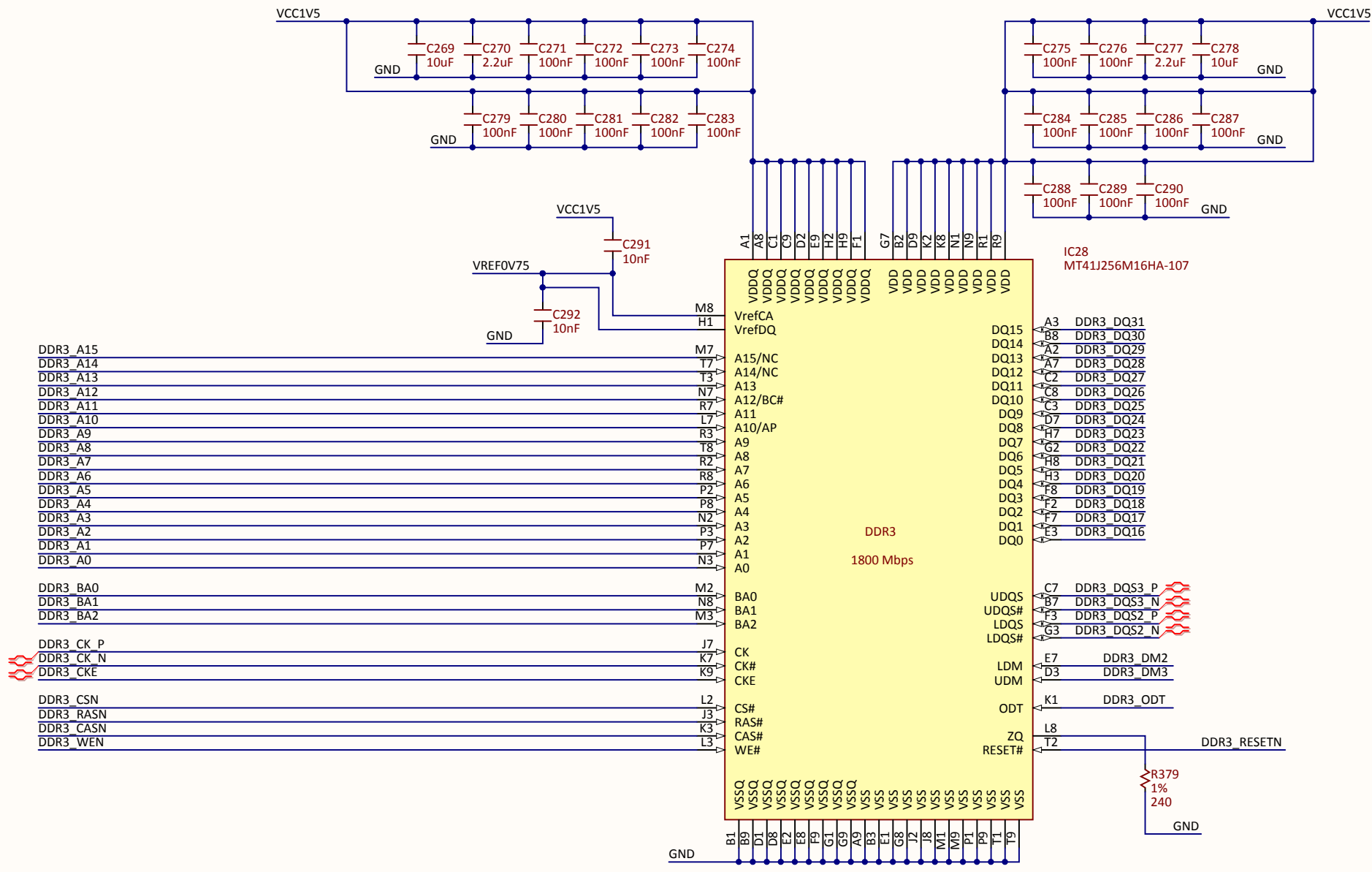
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D

D



Title Genesis 2		Rev H.1 Copyright 2015
Circuit DDR3	Doc# 500-300	
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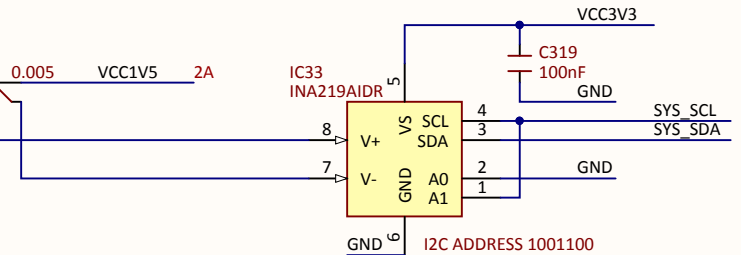
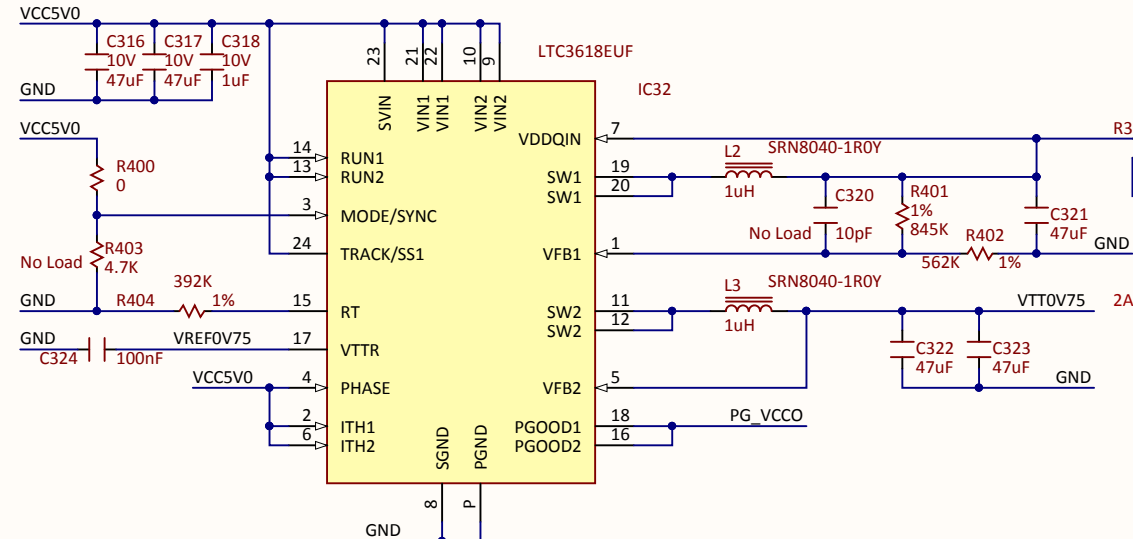
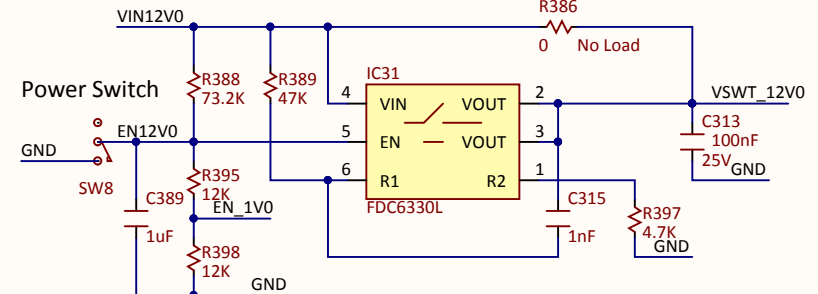
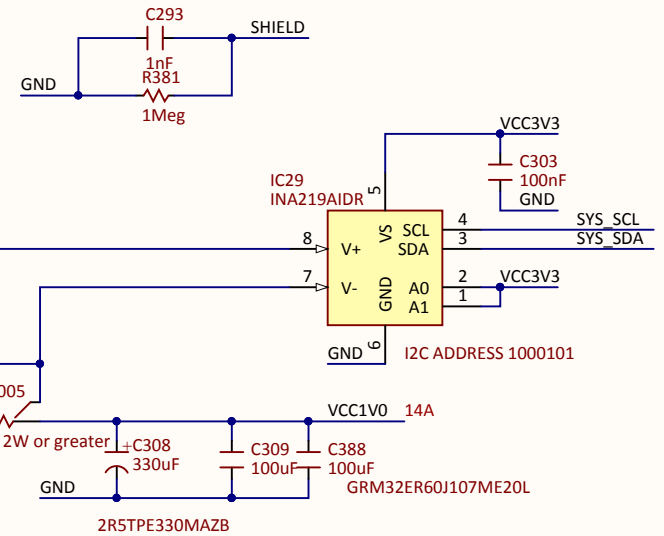
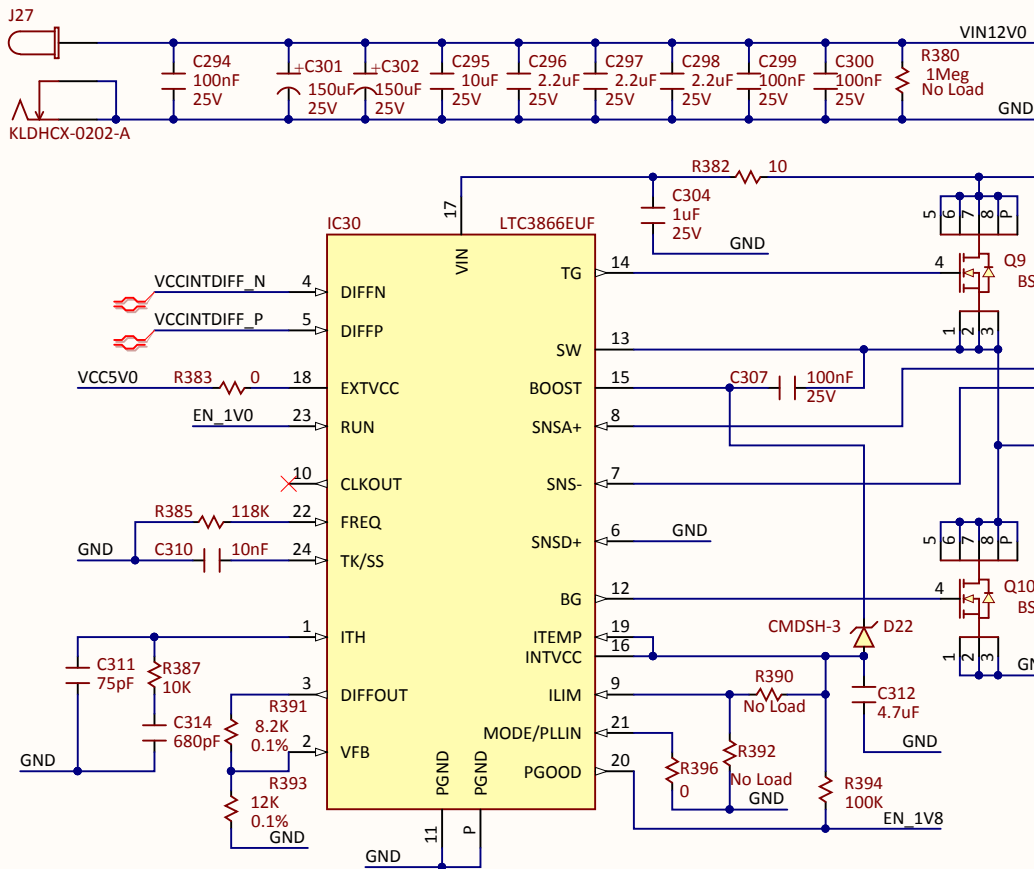
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- DDR3_A12
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- DDR3_A8
- DDR3_A7
- DDR3_A6
- DDR3_A5
- DDR3_A4
- DDR3_A3
- DDR3_A2
- DDR3_A1
- DDR3_A0

- DDR3_BA0
- DDR3_BA1
- DDR3_BA2

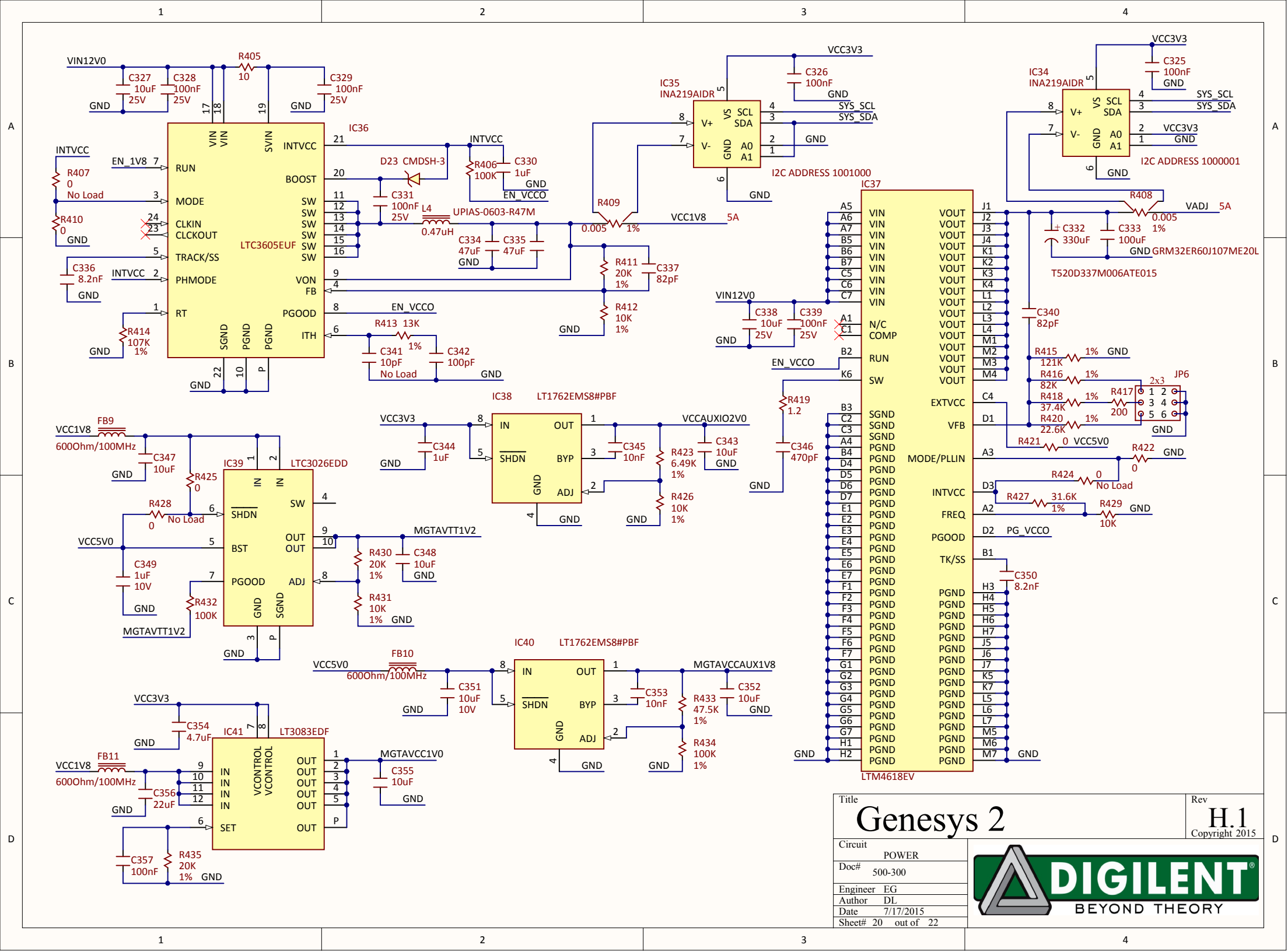
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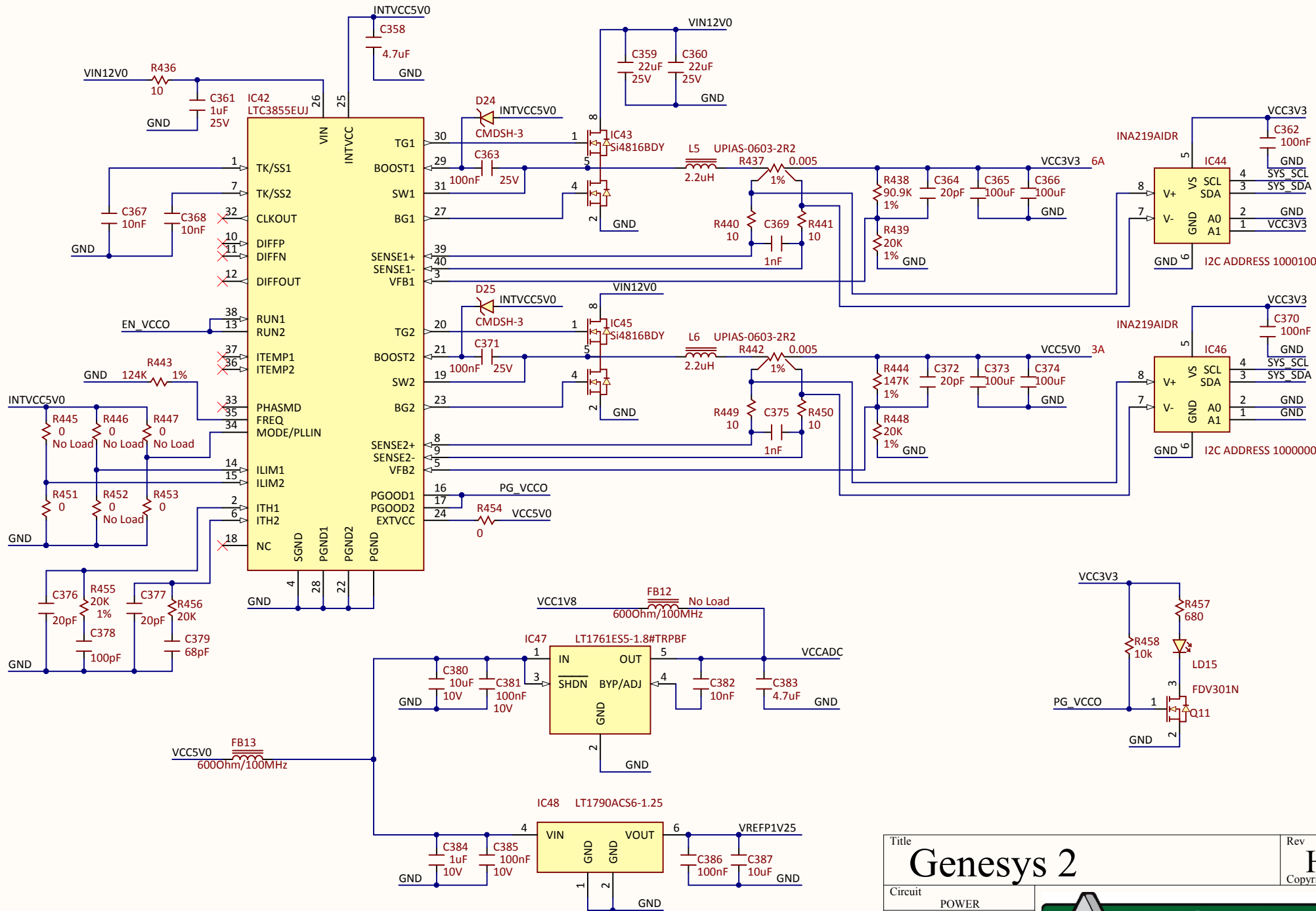
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Circuit DDR3	Doc# 500-300	
Engineer EG	Author DL	
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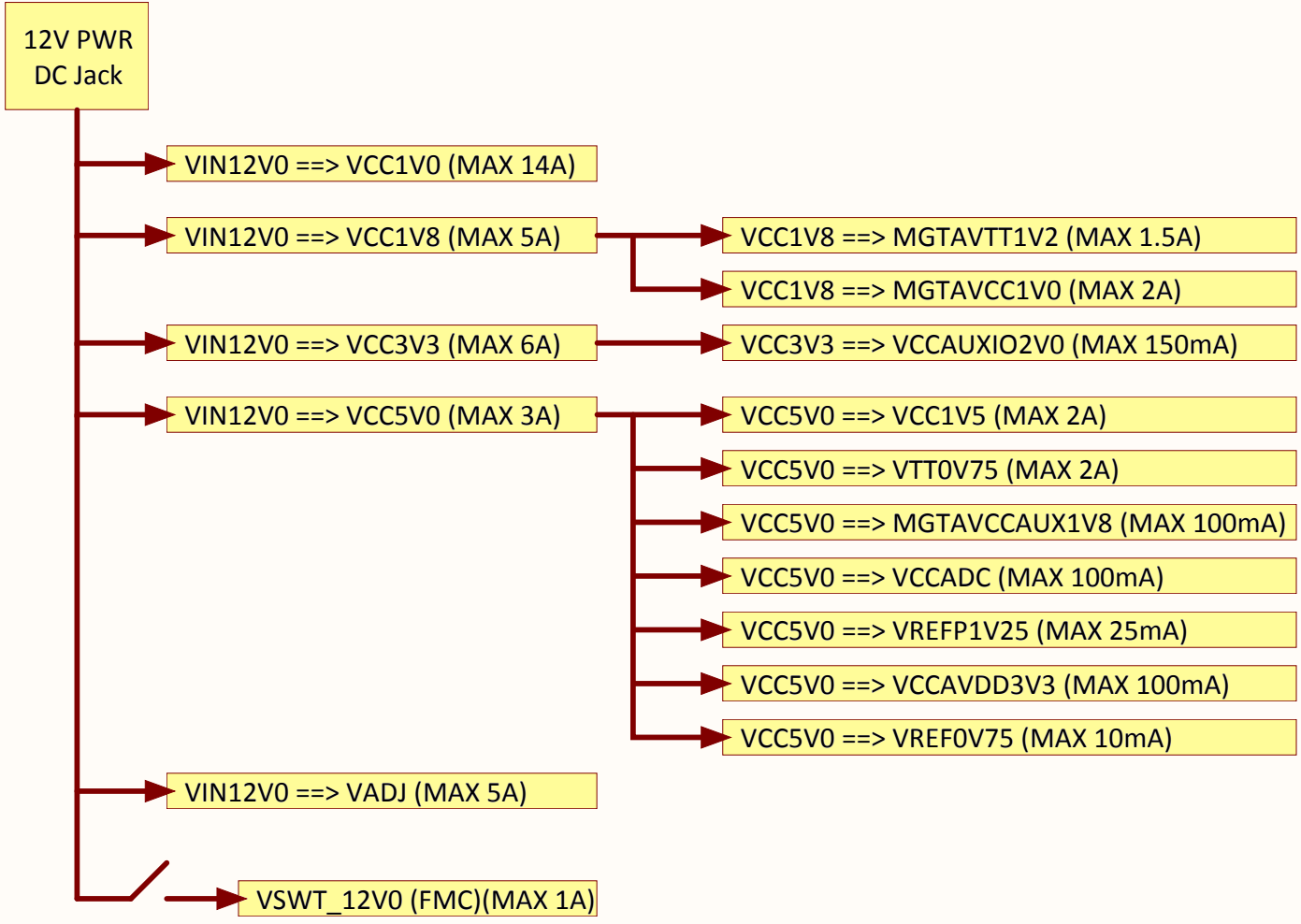
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Circuit	POWER	Author	DL
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