

TRIPLE INVERTER WITH OPEN-DRAIN OUTPUTS

Description

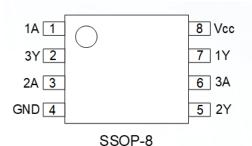
The 74LVC3G06 is a triple inverter with open-drain outputs. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

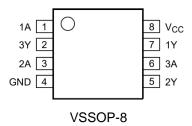
Each of the inverters performs the positive Boolean function:

$$Y = A$$

A pullup resistor is required for a logical HIGH output.

Pin Assignments





Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- -24mA Output Drive at 3.3V
- CMOS Low-Power Consumption
- Ioff Supports Partial Power Down Mode Operation
- Inputs Accept up to 5.5V
- ESD Protection Tested per JESD 22
 Exceeds 2000V Human Body Model (A114)
 Exceeds 1000V Charged Device Model (C101)
- Latch-Up Exceeds 100mA per JESD 78, Class I
- Range of Package Options
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please <u>contact us</u> or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

Applications

- · Voltage-level shifting
- General-purpose logic
- · Power down signal isolation
- Wide array of products such as:
 - · PCs, networking, notebooks, netbooks, PDAs
 - · Computer peripherals, hard drives, CD/DVD ROM
 - TV, DVD, DVR, set top boxes
 - Cell phones, personal navigation / GPS
 - MP3 players, cameras, video recorders

Notes:

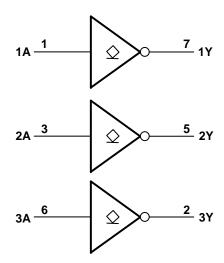
- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



Pin Descriptions

Pin Name	Pin NO.	Description
1A	1	Data Input
3Y	2	Data Output
2A	3	Data Input
GND	4	Ground
2Y	5	Data Output
3A	6	Data Input
1Y	7	Data Output
Vcc	8	Supply Voltage

Logic Diagram



Function Table

Inputs	Output
Α	Y
Н	L
L	Z

Absolute Maximum Ratings (Notes 4, 5)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
Vcc	Supply Voltage Range	-0.5 to 6.5	V
VI	Input Voltage Range	-0.5 to 6.5	V
Vo	Voltage Applied to Output in High Impedance or IOFF State	-0.5 to 6.5	V
Vo	Voltage Applied to Output in High or Low State	-0.5 to 6.5	V
lıĸ	Input Clamp Current V _I < 0	-50	mA
lok	Output Clamp Current V _O < 0	-50	mA
lo	Continuous Output Current	±50	mA
Icc, Ignd	Continuous Current Through Vcc or GND	±100	mA
TJ	Junction Temperature	+150	°C
Tstg	Storage Temperature	-65 to +150	°C

Notes:

- 4. Stresses beyond the absolute maximum can result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.
 5. Forcing the maximum allowed voltage could cause a condition exceeding the maximum current or conversely forcing the maximum current could cause a condition exceeding the maximum voltage. The ratings of both current and voltage must be maintained within the controlled range.



Recommended Operating Conditions (Note 6)

Symbol	Parameter	Conditions	Min	Max	Unit	
	On a notice a Malta are	Operating	1.65	5.5	V	
Vcc	Operating Voltage	Data Retention Only	1.5	_	V	
		Vcc = 1.65V to 1.95V	0.65 X Vcc	_		
	High Lavel lagest Valtage	Vcc = 2.3V to 2.7V	1.7	_	V	
ViH	High-Level Input Voltage	Vcc = 3V to 3.6V	2	_	ľ	
		Vcc = 4.5V to 5.5V	0.7 X Vcc	_		
		V _{CC} = 1.65V to 1.95V	_	0.35 X V _{CC}		
	Low-Level Input Voltage	Vcc = 2.3V to 2.7V	_	0.7	V	
VIL		Vcc = 3V to 3.6V	_	0.8		
		V _{CC} = 4.5V to 5.5V	_	0.3 X V _{CC}		
VI	Input Voltage	_	0	5.5	V	
Vo	Output Voltage	_	0	5.5	V	
		V _{CC} = 1.65V	_	4		
		V _{CC} = 2.3V	_	8		
loL	Low-Level Output Current	V 2V	_	16	mA	
		Vcc = 3V	_	24		
		V _{CC} = 4.5V	_	32		
		$Vcc = 1.8V \pm 0.15V, 2.5V \pm 0.2V$	_	20		
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	Vcc = 1.65V to 2.7V	_	10	ns/V	
		V _{CC} = 2.7V to 5V	_	5		
TA	Operating Free-Air Temperature	<u> </u>	-40	+125	°C	

Note:

6. Unused inputs should be held at V_{CC} or Ground for device proper operation.



Electrical Characteristics

Cumbal	Parameter	T . O . II.:	.,	-40°C t	o +85ºC	-40°C to	+125°C	Unit
Symbol	Parameter	Test Conditions	Vcc	Min	Max	Min	Max	Unit
		I _{OL} = 100μA	1.65V to 5.5V	_	0.1	_	0.1	
		IoL = 4mA	1.65V	_	0.45	_	0.45	
V/	Low Lovel Output Voltage	IoL = 8mA	2.3V	_	0.3	_	0.3	V
VoL	Low-Level Output Voltage	IoL = 16mA	3V	_	0.4	_	0.4	V
		IoL = 24mA	3 V	_	0.55	_	0.75	
		IoL = 32mA	4.5V	_	0.55	_	0.75	
lı	Input Current	V _I = 5.5V or GND	0 to 5.5V	_	±5	_	±5	μA
loff	Power Down Leakage Current	V _I or V _O = 5.5V	0	_	±10	_	±10	μA
Icc	Supply Current	$V_I = 5.5V$ of GND, $I_O = 0$	1.65V to 5.5V	_	10	_	10	μA
ΔI _{CC}	Additional Supply Current	Input at V _{CC} – 0.6V	3V to 5.5V	_	500	_	500	μA
Cı	Input Capacitance	V _I = V _{CC} or GND	3.3V	_	3.5 (Typ)	_	_	pF

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Тур	Max	Unit
0	Thermal Resistance Junction-to-Ambient	SSOP-8	Note 7	_	130	_	°C/W
ӨЈА	Thermal Resistance Junction-to-Ambient	VSSOP-8	Note 7	_	155	_	°C/W
0	Thermal Resistance Junction-to-Case	SSOP-8	Note 7	_	36	_	°C/W
Өлс	Thermal Resistance Junction-to-Case	VSSOP-8	Note 7	_	38	_	°C/W

Note: 7. Test condition: Device mounted on JEDEC 2s2p High-K board, FR-4 substrate PCB, 2oz copper with minimum recommended pad layout.

Operating Characteristics (T_A = +25°C, V_{CC} = 3.3V)

Symbol	Parameter	Test Conditions	Vcc = 1.8V Typ	Vcc = 2.5V Typ	Vcc = 3.3V Typ	Vcc = 5V Typ	Unit
CPD	Power Dissipation Capacitance	f = 10MHz, 1 Input Switching	2	2	3	4	pF

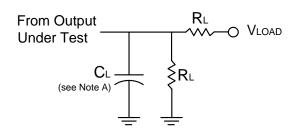
Switching Characteristics

Figure 1

Parameter	From Input	То	Vaa	T _A = -40°C	to +85°C	T _A = -40°C	to +125°C	Unit
Parameter		Output	V _{CC}	Min	Max	Min	Max	Unit
			1.8V ± 0.15V	1.8	7.2	1.8	7.8	
4		V	2.5V ± 0.2V	1	3.9	1	4.5	no
tpD	A	A Y	3.3V ± 0.3V	1	3.4	1	4.0	ns
			5.0V ± 0.5V	1	2.9	1	3.5	



Parameter Measurement Information (Notes B, C)



TEST	Condition
tpLz (see Notes D and F) tpzL (see Notes D and E)	Vload Vload

Vcc	Inputs		Vm	VLOAD	CL	R∟	V Δ
	Vı	t _r /t _f					
1.8V ± 0.15V	Vcc	≤2ns	Vcc / 2	2 X Vcc	30pF	1kΩ	0.15V
2.5V ± 0.2V	Vcc	≤2ns	Vcc / 2	2 X Vcc	30pF	500Ω	0.15V
$3.3V \pm 0.3V$	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V ± 0.5V	Vcc	≤2.5ns	Vcc / 2	2 X Vcc	50pF	500Ω	0.3V

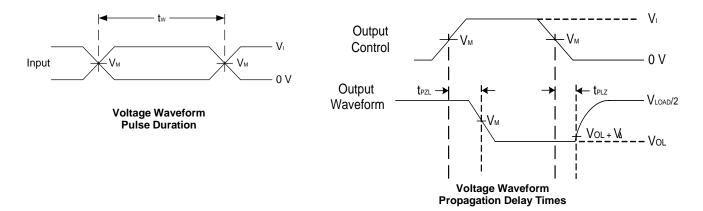


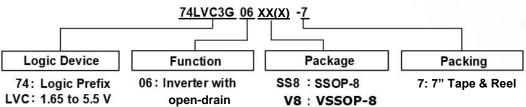
Figure 1. Load Circuit and Voltage Waveforms

Notes: A. Includes test lead and test apparatus capacitance.

- B. All pulses are supplied at pulse repetition rate ≤ 10MHz.
- C. The inputs are measured one at a time with one transition per measurement.
- D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD} .
- E. t_{PZL} is measured at V_M.
- F. t_{PLZ} is measured at V_{OL} +V $_{\!\Delta}.$



Ordering Information



LVC: 1.65 to 5.5 V Family

3G: Triple Gate

5 (1)	Bart Namel and Barton Carlo			Packing		
Part Number	Package Code	Package	Qty.	Carrier		
74LVC3G06SS8-7	SS8	SSOP-8	3000	7" Tape and Reel (Note 8)		
74LVC3G06V8-7	V8	VSSOP-8	3000	7" Tape and Reel (Note 8)		

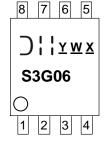
Note: 8. The taping orientation is located on our website at http://www.diodes.com/package-outlines.html.

Marking Information

SSOP-8

output

(Top View)



 $\underline{\underline{Y}}$: Year : 0 to 9 $\underline{\underline{W}}$: Week : A to Z : 1 to 26 week;

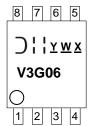
a to z: 27 to 52 week; z represents 52 and 53 week

X: Internal Code

Part Number	Package	Identification Code	
74LVC3G06SS8-7	SSOP-8	S3G06	

VSSOP-8

(Top View)



 $\underline{\underline{Y}}$: Year : 0 to 9 $\underline{\underline{W}}$: Week : A to Z : 1 to 26 week; a to z: 27 to 52 week; z represents

52 and 53 week X: Internal Code

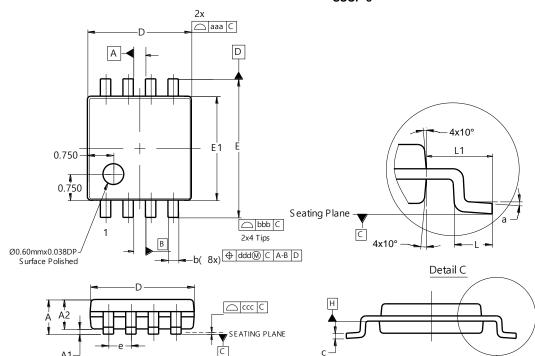
Part Number	Package	Identification Code
74LVC3G06V8-7	VSSOP-8	V3G06



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

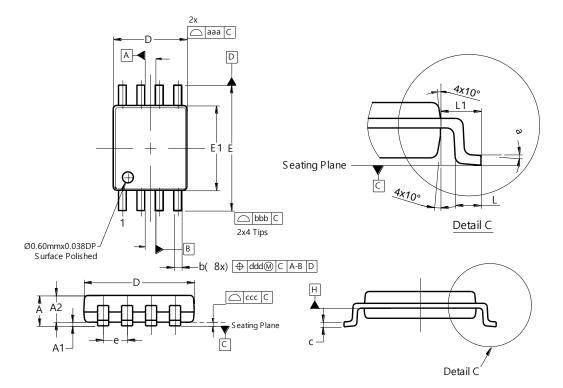
SSOP-8



SSOP-8				
Dim	Min	Max	Тур	
Α		1.30		
A 1	0.05	0.15		
A2	0.95	1.20	1.05	
b	0.15	0.30	0.225	
O	0.08	0.23		
D	2.75	3.15	2.95	
Е	3.75	4.25	4.00	
E1	2.70	2.90	2.80	
е			0.65	
L	0.20	0.60	0.40	
Ľ	0.525	0.675	0.60	
а	0°	8°	4°	
aaa	0.20			
bbb	0.25			
CCC	0.10			
ddd	0.13			
All Dimensions in mm				

See Detail C

VSSOP-8



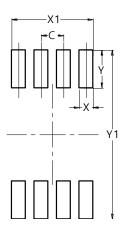
VSSOP-8				
Dim	Min	Max	Тур	
Α	0.60	0.90		
A1		0.10		
A2	0.60	0.80		
b	0.17	0.25	0.21	
С	0.08	0.13		
D	1.90	2.10	2.00	
Е	3.20	3.60	3.40	
E1	2.20	2.40	2.30	
е			0.50	
L	0.30	0.40	0.35	
L1	0.50	0.60	0.55	
а	0°	6°	3°	
aaa	0.20			
bbb	0.25			
CCC	0.10			
ddd	0.13			
All Dimensions in mm				



Suggested Pad Layout

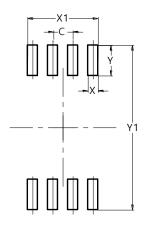
Please see http://www.diodes.com/package-outlines.html for the latest version.

SSOP-8



Dimensions	Value (in mm)
С	0.650
Х	0.400
X 1	2.350
Y	1.100
Y1	4.900

VSSOP-8



Dimensions	Value (in mm)	
С	0.500	
	0.500	
Х	0.250	
X1	1.750	
Y	0.750	
Y1	4.050	

Mechanical Data

SSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Mate Tin Plated Leads, Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.0169 grams (Approximate)

VSSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Mate Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.011 grams (Approximate)



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